Tips for using Timers

1. **Pre scaling:**

As you may be aware the clock frequency of Atmega 2560 is 14.745600 MHz and the counter/Timer will increment by 1 for each clock pulse.

Consider that the timer/counter is 16 bit, therefore maximum possible count value will be 65535 (starting from 0). The time period for each clock pulse is 1/14.745600 MHz is **0.0678 µsecs.**

Maximum delay that can be generated will be **65536 X 0.0678 µsecs = 4.44 milliseconds**. Hence, we need a prescalar to divide this clock frequency by 8/64/256/1024 to generate greater delay. As shown below in fig no. 1,

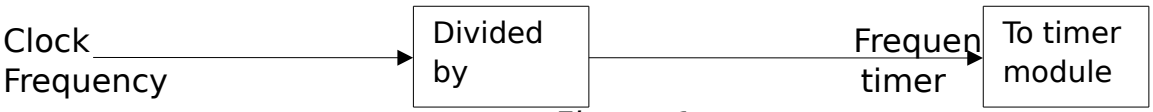

Fig no. 1

You need to select an appropriate prescalar value so that a delay of 1 second can be generated.

Prescalar value can be selected by setting the **CSn2 – CSn0 bits** in **TCCRnB** register, where n is the timer you are using. As shown below in fig no. 2,

CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{I/O}$/1 (No prescaling
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

Fig no. 2

2. **Count Value:**

Assume we are using Timer 1. Timer 1 is an Up counter. Assume that the clock frequency after division is 10Khz and a delay of 1ms is needed. Therefore the timer 1 has to count 10 pulses of the input clock (1 ms is 1 Khz and 10khz/1khz = 10).

Count value to be loaded = 65535 - 10 = 65525
= 65526 (+1 reason below)
The calculated count value has to be loaded in the TCNT1 register (TCNT1H and TCNT1L).

The counter starts with initial count = 65526, counts 9 pulses reaches 65535 and on the 10 pulse it overflows and generates an interrupt to indicate the same.
Once an interrupt occurs program jumps to **ISR** (ISR(TIMER1_OVF_vect)), where you can again reload the initial value of the count to generate another 1 ms delay.

3. **TCCR1A and TCCR1B:**

TCCR1A contains two Wave form generator mode bits, while TCCR1B contains other 2 waveform generator mode bits along with pre scalar selection.

Bit	7	6	5	4	3	2	1	0	
(0x80)	COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10	TCCR1A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Fig no. 3

Bit	7	6	5	4	3	2	1	0	
(0x81)	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Fig no. 4

Note: Timer 1 will start as soon as you set the pre scalar bits.

Appropriate bits have to be set in these registers so that Timer 1 operates in Normal mode with required pre scalar. To operate in Normal mode the waveform generator bits have to set as follows.

Table 17-2. Waveform Generation Mode Bit Description(1)

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation	TOP	Update of OCRnX at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP

Fig no. 5

For more information refer to page no. **148, 158-162** of the datasheet.

Note: You have to set the COMnA1, COMnA0, COMnB1, COMnB0, COMnC1, COMnC0 bits of TCCRnA as 0 to keep the OCnA, OCnB, OCnC in "Normal Port Operation Mode". (where 'n' is the number of 'timer' you are using)