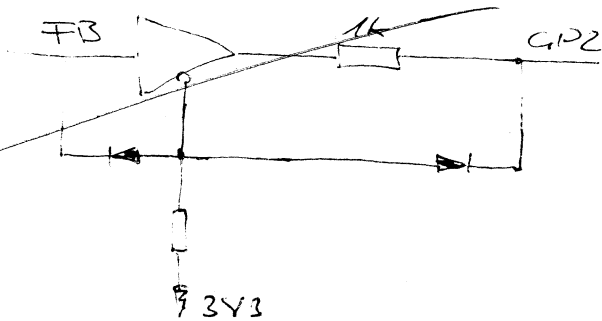


FB	GP2	OE
1	1	1
0	1	1
1	0	1
0	0	1
1	Z	0
0	Z	0



if $d-w < 22$
DST = 0

late = 27. nanz
early = 22. nanz

if $d-w \geq 22$
DST = 1

SO = 0
WC = 1
DI = 2
MI = 3
PC = 4
FZ = 5
SA = 6

if $m \geq 3$ then

if $w = 0$ then

if $d \geq 22$ then
DAG

else

$$5 \times \bullet = 5$$

$$+ 4 \times 7 \times 1 = 28$$

5x 744LS95 23/35
25-2
GND

		28
		22
22 =	25	24
23 =	76	29
24 =	50	24
25 =	61	26
26 =	02	28
27 =	13	30
28 =	24	32

1, 4, 8, 13

3, 4, 5

6. Pinning information

6.1 Pinning

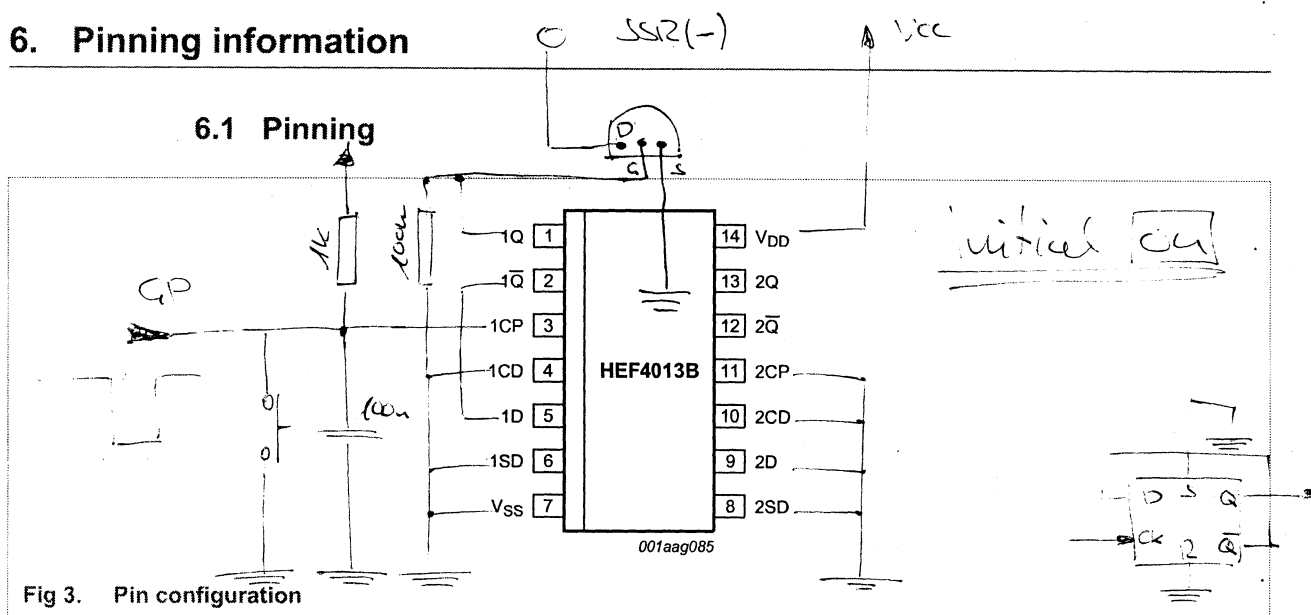


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q, 2Q	1, 13	true output
1Q̄, 2Q̄	2, 12	complement output
1CP, 2CP	3, 11	clock input (LOW to HIGH edge-triggered)
1CD, 2CD	4, 10	asynchronous clear-direct input (active HIGH)
1D, 2D	5, 9	data input
1SD, 2SD	6, 8	asynchronous set-direct input (active HIGH)
Vss	7	ground (0 V)
VDD	14	supply voltage

7. Functional description

Table 3. Function table^[1]

Control			Input	Output	
nSD	nCD	nCP	nD	nQ	nQ̄
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	↑	L	L	H
L	L	↑	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition.

2 light
0 ws

6. Pinning information

6.1 Pinning

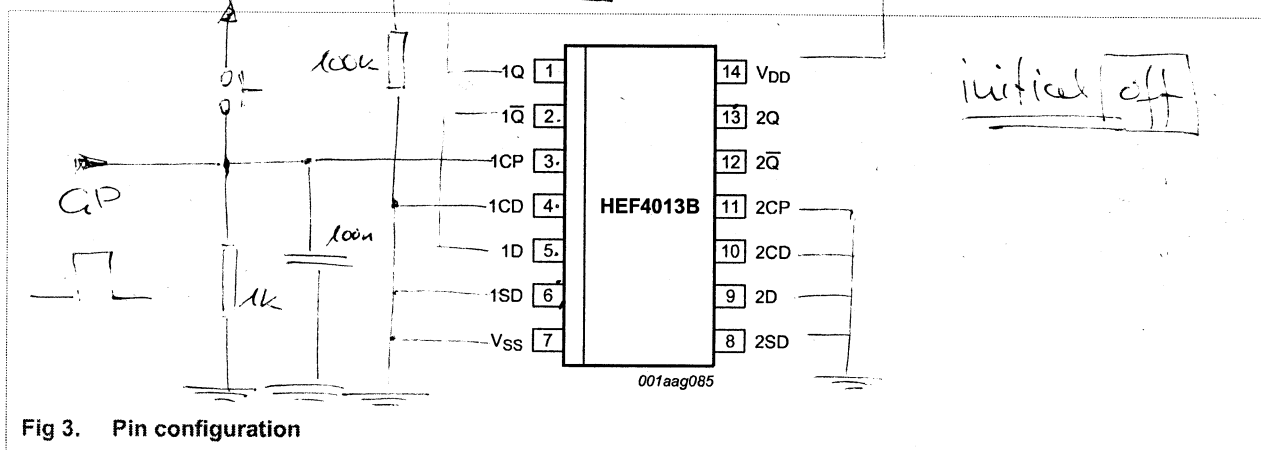


Fig 3. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q, 2Q	1, 13	true output
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1SD, 2SD	6, 8	asynchronous set-direct input (active HIGH)
V _{SS}	7	ground (0 V)
V _{DD}	14	supply voltage

7. Functional description

Table 3. Function table^[1]

Control			Input	Output	
nSD	nCD	nCP	nD	nQ	nQ̄
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H
L	L	↑	L	L	H
L	L	↑	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition.