CV181xC_CV181xH

PCB Layout Guide

Version: 0.2

Release date: 2022/09/13

Outline

- Checklist
- Stackup
- DDR 电源绕线
- Serdes讯号绕线
  - MIPI/USB/EPHY
- Single-end讯号绕线
  - GPIO/SDIO
  - EMMC/AUD/XTAL/WIFI
- 模拟/数字电源绕线
  - VDDC
  -模拟IO电源

CV181xC/CV181xH PCB Type

- PCB 依照支持不同PKG型式, 分成以下PCB layout:
  (1) QFN PKG: CV1810C/CV1811C/CV1812C, DDR3/DDR2 SIP on PKG (4-Layer/6-Layer PCB)
  (2) BGA PKG: CV1810H/CV1811H/CV1812H/CV1813H, DDR2/DDR3 SIP on PKG (4-Layer/6-Layer PCB)

- Layout rule 分成以下两部份:
  (1) **DDR Layout rule (2 types)**
  (2) **Serdes/Single-end/Power Layout rule (common rule)**

- PKG型式与叠构相对应PCB layout rule如下:

Type	Stackup	DDR layout rule	Serdes/Single-end/Power Layout rule
QFN PKG	(1) 4-layer PCB (2) 6-layer PCB (真6层)	QFN 电源绕线	4-layer/6-layer (真6层) PCB layout rule (common rule)
BGA PKG	(1) 4-layer PCB (2) 6-layer PCB (真6层)	BGA 电源绕线	

Checklist

Checklist – Stackup – 4L-PCB/6L-PCB

No.	Rule	Description	Requirement	Check
1	4L-PCB 叠构要求	介电层/铜 厚度限制	1. 确认介电层厚度 – pp/core (1) pp<=5mils (Cu与pp 压合后, pp不含Cu的厚度) (2) L2/L3 Core 厚度>=25mils, 2. 每层Cu厚度1oz.	
2	6L-PCB 叠构要求	介电层/铜 厚度限制	1. 确认介电层厚度 – pp/core (1) L1/L2, L3/L4, L5/L6: pp<=5mils (Cu与pp 压合后, pp不含Cu的厚度) (3) all core 厚度>11mils 2. 每层Cu厚度1oz.	

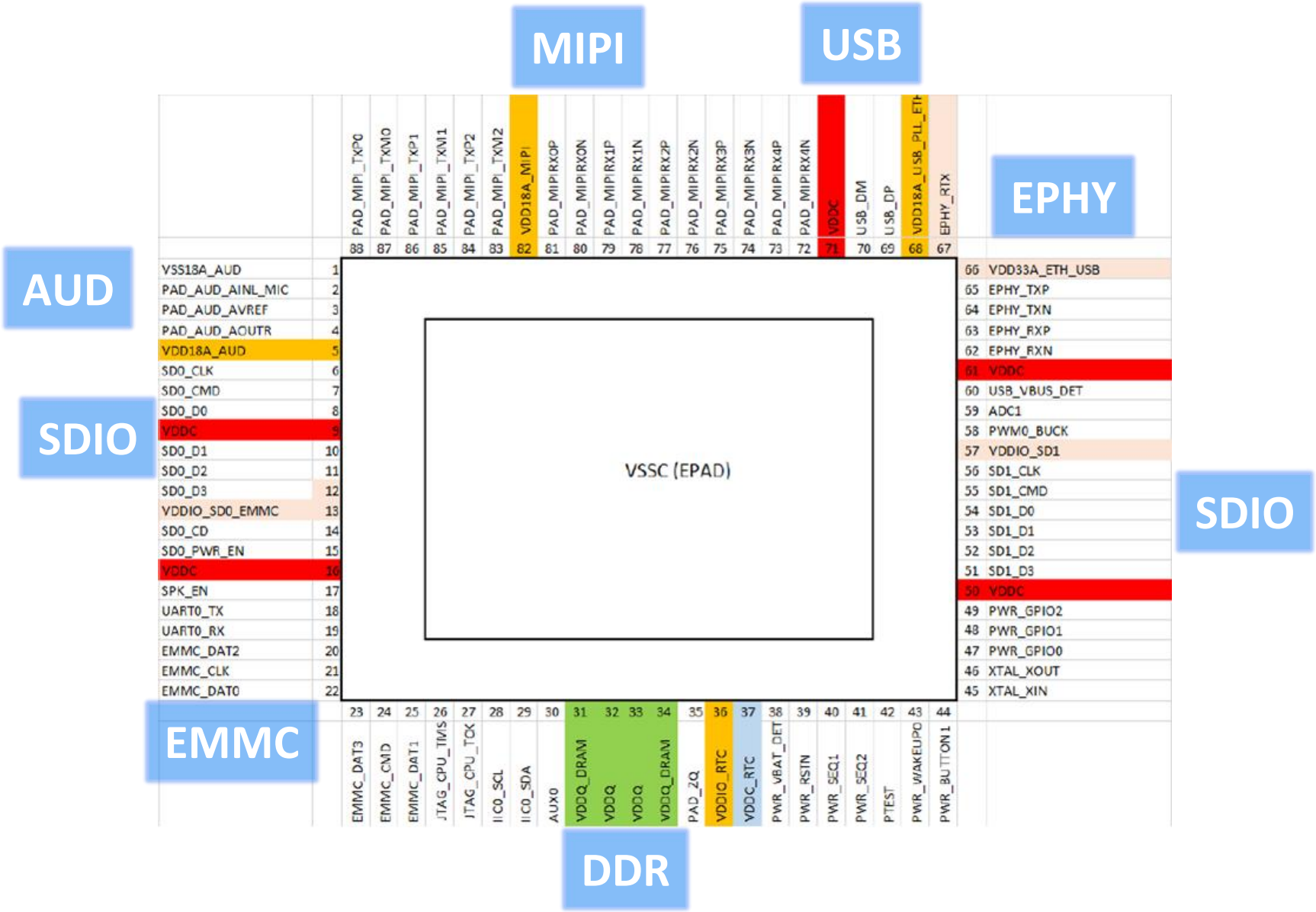
Checklist - Layout rule

No.	Rule	Description	Requirement	Check
1	DDR routing	DDR3Q_1.5V rule	1. 确认QFN PKG E-pad solder mask 覆盖区 (7.6x7.6mm2) 3 颗VIA 2. 建议贴上SOC PKG 下方DDR 走线/VIA/Cap layout	
2	MIPI routing	表层/内层 阻抗控制	与PCB vendor 确认polar 结果: (1) 表层: Diff Coated Coplanar Strips with GND 1B (2) 内层: Diff Offset Coplanar Strips 1B1A	
3		表层走线 Lane to lane NO GND shielding	Lane to lane NO GND shielding 走线长度<3.5mm	
4		BGA PKG, GND plane rule – 确保MIPI 讯号 return path.	TX/RX在SOC ball下方GND plane预留3通道以上	
5		Length matching rule	确认TX/RX length matching	
6	USB	表层/内层 阻抗控制	与PCB vendor 确认polar 结果: (1) 表层: Diff Coated Coplanar Strips with GND 1B (2) 内层: Diff Offset Coplanar Strips 1B1A	
7		Length matching rule	P/N length matching	
8	EPHY routing	表层/内层 阻抗控制	与PCB vendor 确认polar 结果: (1) 表层: Diff Coated Coplanar Strips with GND 1B (2) 内层: Diff Offset Coplanar Strips 1B1A	
9		Length matching rule	P/N length matching	

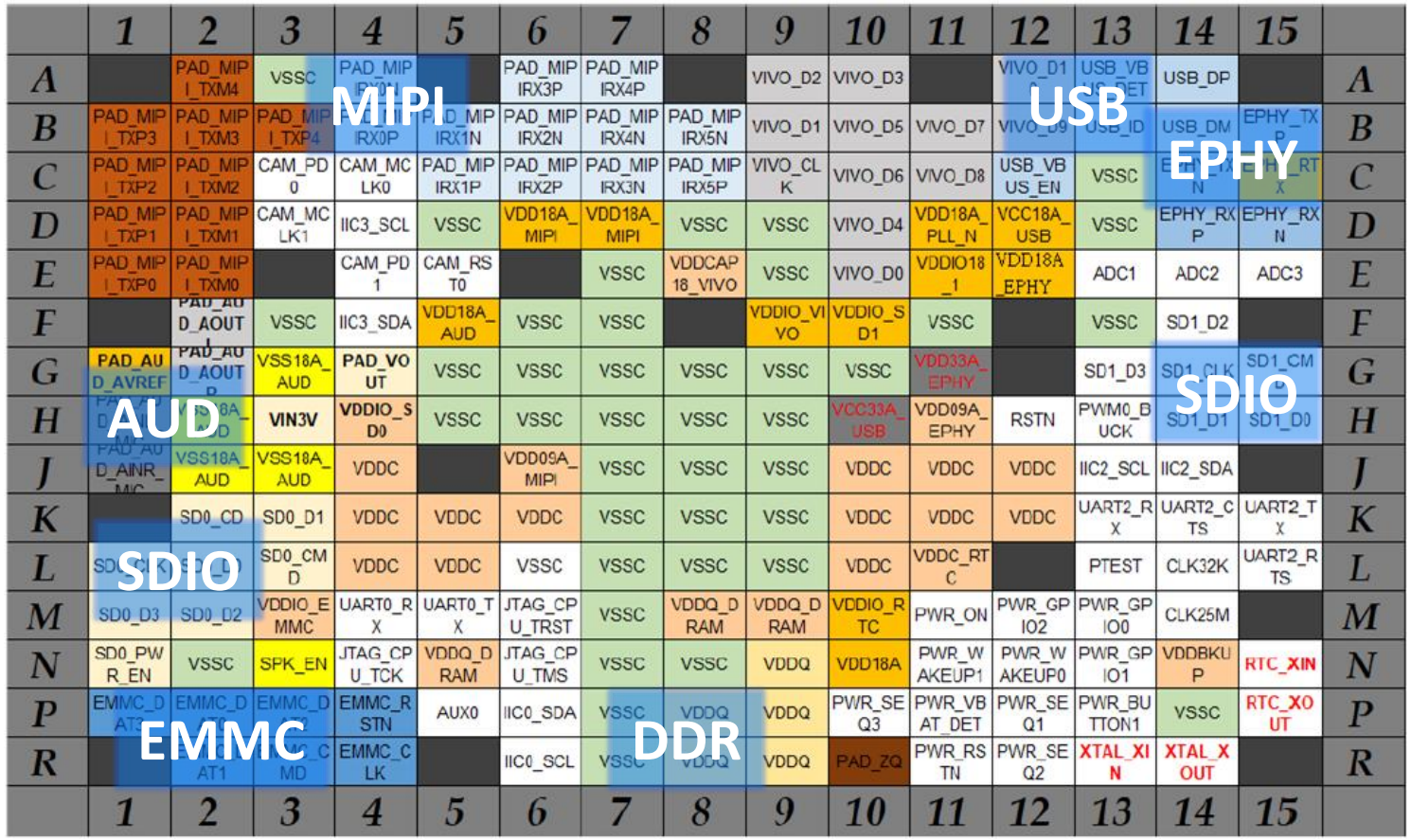
Checklist - Layout rule

No.	Rule	Description	Requirement	Check
10	Single-end rule	表层/内层 shielding rule	Shielding rule	
11	EMMC rule	表层/内层 shielding rule	Shielding rule	
12	AUD rule	表层 shielding rule	Shielding rule	
13	XTAL rule	表层 shielding rule	Shielding rule	
14	RTC rule	表层 shielding rule	Shielding rule	
15	WIFI_ANT rule	表层阻抗控制	与PCB vendor 确认polar 结果: (1) 表层: Coated Coplanar Strips with GND 1B	
16	VDC rule	1. 确认Cap数量与位置, VIA数量 2. 通道宽度	1. Rule1: (1) SOC/PMIC 处VIA 数量 (2) SOC处Cap pin VDDC/GND VIA rule 2. 通道宽度参照 rule2 3. 建议贴上SOC PKG 下方VDDC 走线/VIA/Cap layout	
17	Analog IO Power rule	1. 线宽rule 2. 确认Cap数量与位置, VIA数量	1. Rule1: (1) SOC/PMIC 处VIA 数量 (2) SOC处Cap pin power/GND VIA rule 2. 通道宽度参照 rule2 3. 建议贴上SOC PKG 下方power走线/VIA/Cap layout	

QFN Ball Map


MIPI
USB
EPHY
AUD
SDIO
SDIO
EMMC
DDR
VSSC (EPAD)
88 PAD_MIPI_TXP0
87 PAD_MIPI_TXM0
86 PAD_MIPI_TXP1
85 PAD_MIPI_TXM1
84 PAD_MIPI_TXP2
83 PAD_MIPI_TXM2
82 VDD18A_MIPI
81 PAD_MIPIRX0P
80 PAD_MIPIRX0N
79 PAD_MIPIRX1P
78 PAD_MIPIRX1N
77 PAD_MIPIRX2P
76 PAD_MIPIRX2N
75 PAD_MIPIRX3P
74 PAD_MIPIRX3N
73 PAD_MIPIRX4P
72 PAD_MIPIRX4N
71 VDDC
70 USB_DM
69 USB_DP
68 VDD18A_USB_PLL_ETH
67 EPHY_RTX
1 VSS18A_AUD
2 PAD_AUD_AINL_MIC
3 PAD_AUD_AVREF
4 PAD_AUD_AOUTR
5 VDD18A_AUD
6 SD0_CLK
7 SD0_CMD
8 SD0_D0
9 VDDC
10 SD0_D1
11 SD0_D2
12 SD0_D3
13 VDDIO_SD0_EMMC
14 SD0_CD
15 SD0_PWR_EN
16 VDDC
17 SPK_EN
18 UART0_TX
19 UART0_RX
20 EMMC_DAT2
21 EMMC_CLK
22 EMMC_DAT0
66 VDD33A_ETH_USB
65 EPHY_TXP
64 EPHY_TXN
63 EPHY_RXP
62 EPHY_RXN
61 VDDC
60 USB_VBUS_DET
59 ADC1
58 PWM0_BUCK
57 VDDIO_SD1
56 SD1_CLK
55 SD1_CMD
54 SD1_D0
53 SD1_D1
52 SD1_D2
51 SD1_D3
50 VDDC
49 PWR_GPIO2
48 PWR_GPIO1
47 PWR_GPIO0
46 XTAL_XOUT
45 XTAL_XIN
23 EMMC_DAT3
24 EMMC_CMD
25 EMMC_DAT1
26 JTAG_CPU_TMS
27 JTAG_CPU_TCK
28 IIC0_SCL
29 IIC0_SDA
30 AUX0
31 VDDQ_DRAM
32 VDDQ
33 VDDQ
34 VDDQ_DRAM
35 PAD_ZQ
36 VDDIO_RTC
37 VDDC_RTC
38 PWR_VBAT_DET
39 PWR_RSTN
40 PWR_SEQ1
41 PWR_SEQ2
42 PTEST
43 PWR_WAKEUP0
44 PWR_BUTTON1

BGA Ball Map



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A		PAD_MIPI_TXM4	VSSC	PAD_MIPI_RXM0P		PAD_MIPI_IRX3P	PAD_MIPI_IRX4P		VIVO_D2	VIVO_D3		VIVO_D1	USB_VBUS_DET	USB_DP		A
B	PAD_MIPI_TXP3	PAD_MIPI_TXM3	PAD_MIPI_TXP4	PAD_MIPI_IRX0P	PAD_MIPI_IRX1N	PAD_MIPI_IRX2N	PAD_MIPI_IRX4N	PAD_MIPI_IRX5N	VIVO_D1	VIVO_D5	VIVO_D7	VIVO_D9	USB_ID	USB_DM	EPHY_TXP	B
C	PAD_MIPI_TXP2	PAD_MIPI_TXM2	CAM_PD0	CAM_MCLK0	PAD_MIPI_IRX1P	PAD_MIPI_IRX2P	PAD_MIPI_IRX3N	PAD_MIPI_IRX5P	VIVO_CLK	VIVO_D6	VIVO_D8	USB_VBUS_EN	VSSC	EPHY_RXN	EPHY_RTX	C
D	PAD_MIPI_TXP1	PAD_MIPI_TXM1	CAM_MCLK1	IIC3_SCL	VSSC	VDD18A_MIPI	VDD18A_MIPI	VSSC	VSSC	VIVO_D4	VDD18A_PLL_N	VCC18A_USB	VSSC	EPHY_RXP	EPHY_RXN	D
E	PAD_MIPI_TXP0	PAD_MIPI_TXM0		CAM_PD1	CAM_RST0		VSSC	VDDCAP18_VIVO	VSSC	VIVO_D0	VDDIO18_1	VDD18A_EPHY	ADC1	ADC2	ADC3	E
F		PAD_AUD_AOUT	VSSC	IIC3_SDA	VDD18A_AUD	VSSC	VSSC		VDDIO_VIVO	VDDIO_SD1	VSSC		VSSC	SD1_D2		F
G	PAD_AUD_AVREF	PAD_AUD_AOUTR	VSS18A_AUD	PAD_VOUT	VSSC	VSSC	VSSC	VSSC	VSSC	VSSC	VDD33A_EPHY		SD1_D3	SD1_CLK	SD1_CMD	G
H	PAD_AUD_AINL_MIC	PAD_AUD_AINR_MIC	VIN3V	VDDIO_SD0	VSSC	VSSC	VSSC	VSSC	VSSC	VCC33A_USB	VDD09A_EPHY	RSTN	PWM0_BUCK	SD1_D1	SD1_D0	H
J		VSS18A_AUD	VSS18A_AUD	VDDC		VDD09A_MIPI	VSSC	VSSC	VSSC	VDDC	VDDC	VDDC	IIC2_SCL	IIC2_SDA		J
K		SD0_CD	SD0_D1	VDDC	VDDC	VDDC	VSSC	VSSC	VSSC	VDDC	VDDC	VDDC	UART2_RX	UART2_CTS	UART2_TX	K
L	SD0_CLK	SD0_CMD	SD0_CMD	VDDC	VDDC	VSSC	VSSC	VSSC	VSSC	VDDC	VDDC_RTC		PTEST	CLK32K	UART2_RTS	L
M	SD0_D3	SD0_D2	VDDIO_EMMC	UART0_RX	UART0_TX	JTAG_CPU_TRST	VSSC	VDDQ_DRAM	VDDQ_DRAM	VDDIO_RTC	PWR_ON	PWR_GPIO2	PWR_GPIO0	CLK25M		M
N	SD0_PWR_EN	VSSC	SPK_EN	JTAG_CPU_TCK	VDDQ_DRAM	JTAG_CPU_TMS	VSSC	VSSC	VDDQ	VDD18A	PWR_WAKEUP1	PWR_WAKEUP0	PWR_GPIO1	VDDBKUP	RTC_XIN	N
P	EMMC_DAT2	EMMC_DAT3	EMMC_DAT0	EMMC_RSTN	AUX0	IIC0_SDA	VSSC	VDDQ	VDDQ	PWR_SEQ3	PWR_VBAT_DET	PWR_SEQ1	PWR_BUTTON1	VSSC	RTC_XOUT	P
R		EMMC_DAT1	EMMC_CMD	EMMC_CLK		IIC0_SCL	VSSC	VDDQ	VDDQ	PAD_ZQ	PWR_RSTN	PWR_SEQ2	XTAL_XIN	XTAL_XOUT		R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Stackup

QFN/BGA PKG: CV181xC/CV181xH
4-layer/6-layer PCB

PCB 4-Layer Stackup

- 叠构层数: 4层
- 叠构厚度: 1mm +/-10% <=厚度 <=1.6mm +/-10%
- 每层Cu采用1oz.
- 介电层厚度限制:

层号	材质	厚度限制
L1/L2	Prepreg	<=5mils (Cu与pp 压合后, pp不含cu厚度)
L3/L4		
L2/L3	Core	>=25mils

参考叠构

Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

PCB 6-Layer Stackup

- 叠构层数: 6层
- 叠构厚度: 1.2mm +/-10% <= 厚度 <=1.6mm +/-10%
- 每层Cu采用1oz.
- 介电层厚度限制:

层号	材质	厚度限制
L1/L2	Prepreg	<=5mils (Cu与pp 压合后, pp不含cu厚度)
L5/L6		
L3/L4		
L2/L3	Core	>=11mils
L4/L5		

参考叠构

Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48	

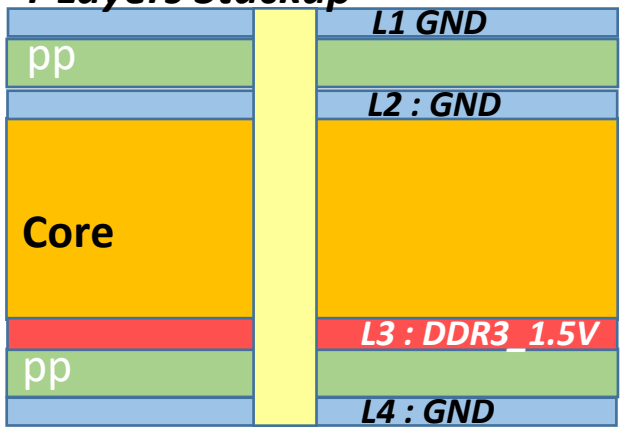
DDR 电源绕线 (DDR3_1.5V)

QFN PKG: CV181xC
4-layer/6-layer PCB

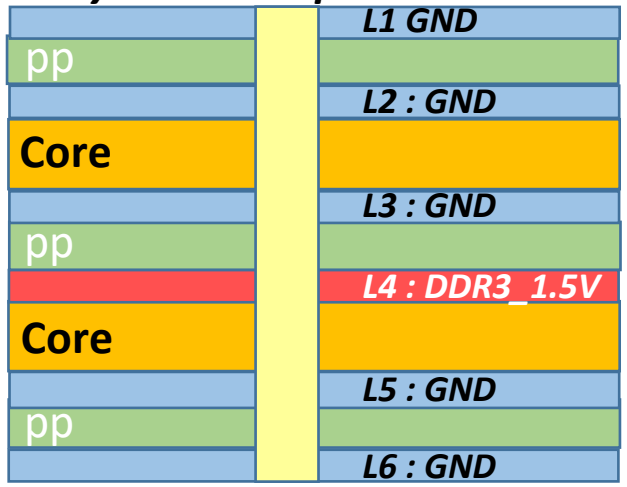
QFN - 4L/6L-PCB DDR Layout

- Stackup:
  (1) 4L-PCB: GND@L1/L2/L4 (plane), 6L-PCB: GND@L1/L2/L3/L4/L6 (plane)
  (2) 4L-PCB: DDR3_1.5V@L3 (shape), 6L-PCB: DDR3_1.5V@L4 (shape)

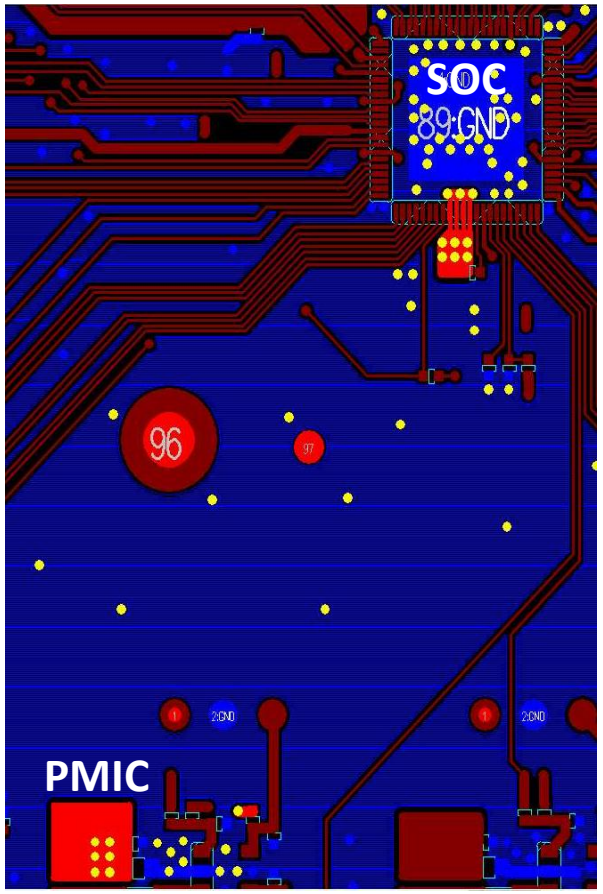
4-Layers Stackup



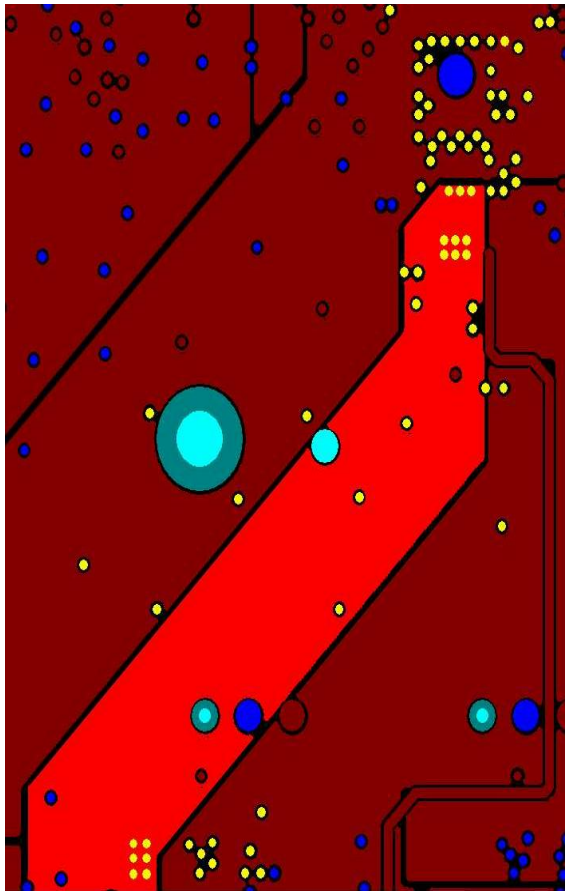
6-layers Stackup



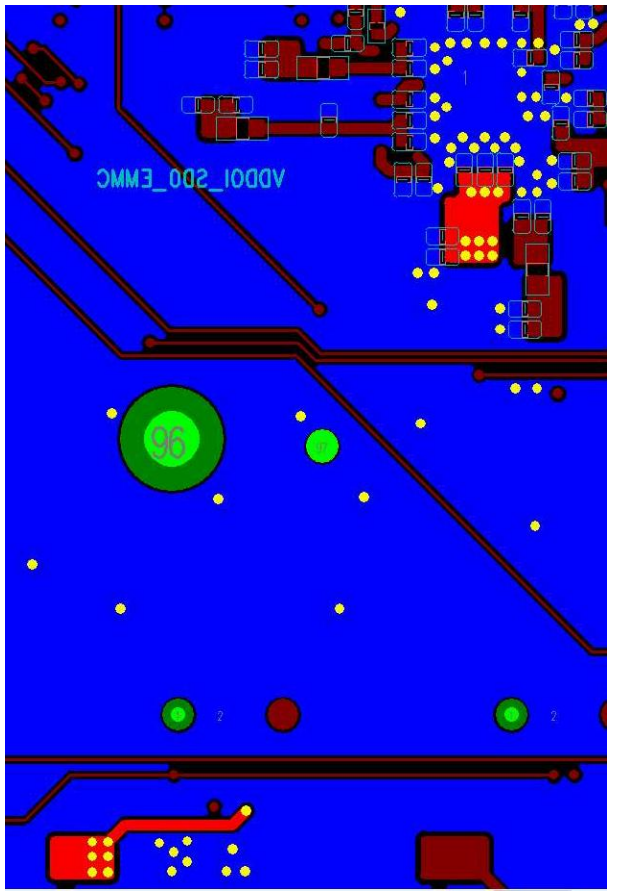
DDR3_1.5V@Top



4L-PCB: DDR3_1.5V@L3
6L-PCB: DDR3_1.5V@L4



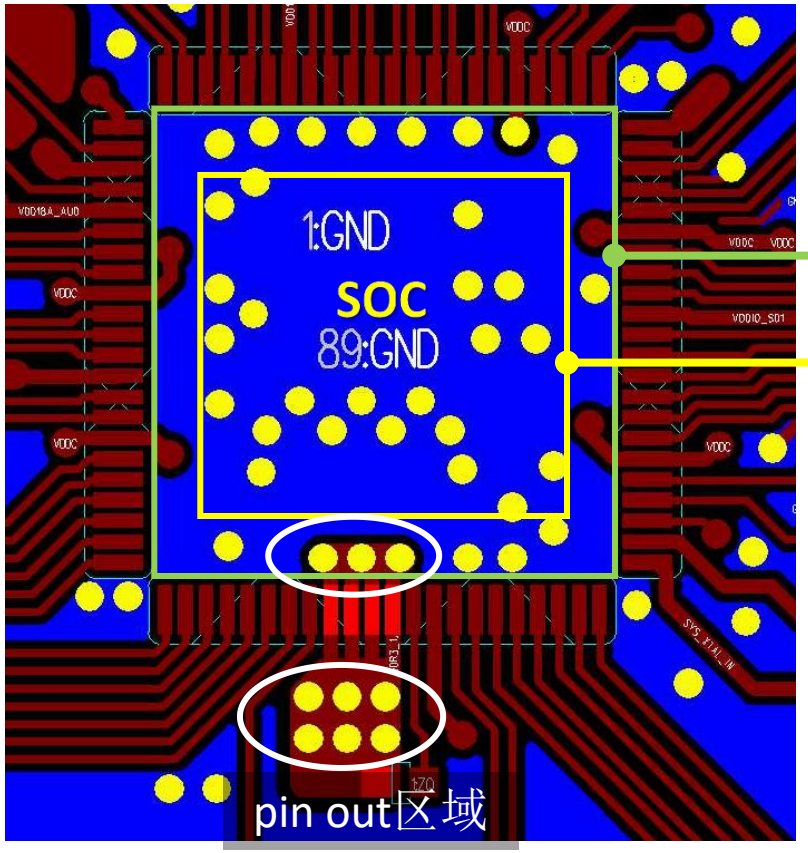
DDR3_1.5V@Bottom



QFN - 4L/6L-PCB - DDR3_1.5V - Rule 1

Power	Layer	SOC VIA count	Layout rule
DDR3_1.5V	Top	(1) @E-pad 7.6x7.6mm2区域: VIA 数量: 3 (2) pin out区域: VIA 数量: 6	(1) 覆盖Solder mask区域: E-pad 7.6x7.6mm2 (2) 非覆盖Solder mask区域: E-pad 6x6mm2 (3) 确认DDR3_1.5V SOC 端VIA数量

DDR3_1.5V@Top



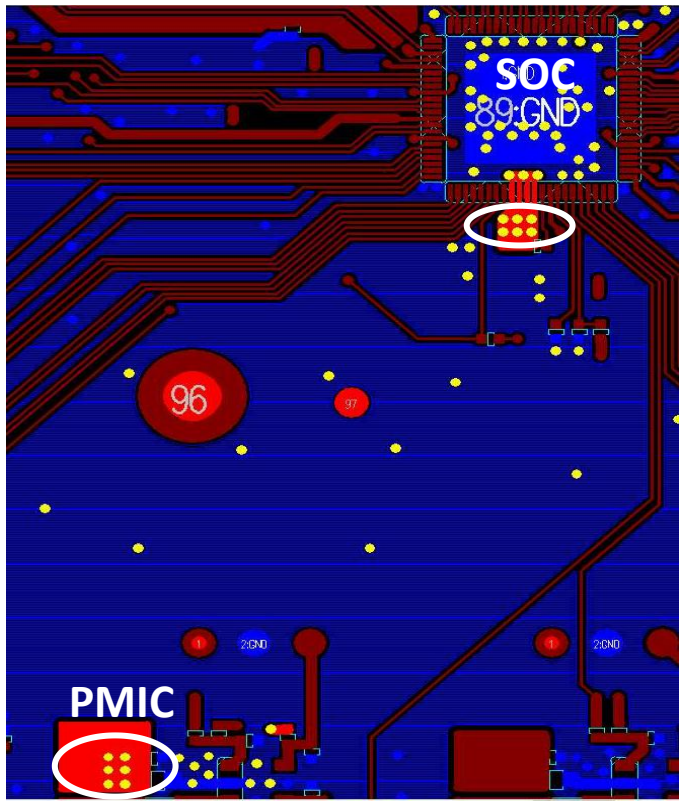
E-pad aera 7.6x7.6mm2 (solider mask)

E-pad aera 6x6mm2 (uncover solider mask)

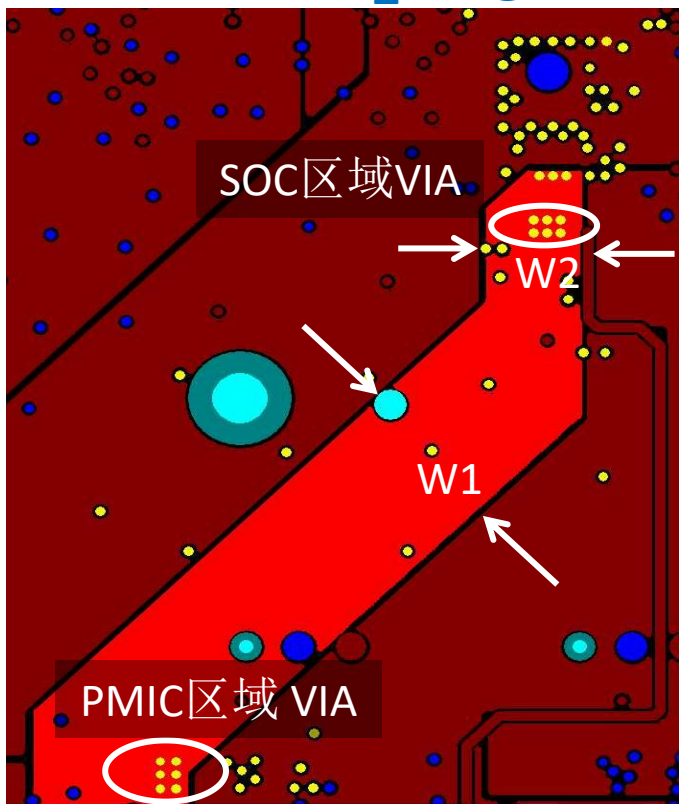
QFN - 4L/6L-PCB – DDR3_1.5V - Rule 2

Power	Layer	Layout rule
DDR3_1.5V	4L-PCB: DDR3_1.5V@L3 6L-PCB: DDR3_1.5V@L4	DDR3_1.5V main route, (1) 确认SOC与PMIC处有下各6颗VIA (2) , 扣除破孔有效宽度: W1>=1.5mm, W2>=1.5mm

DDR3_1.5V@Top



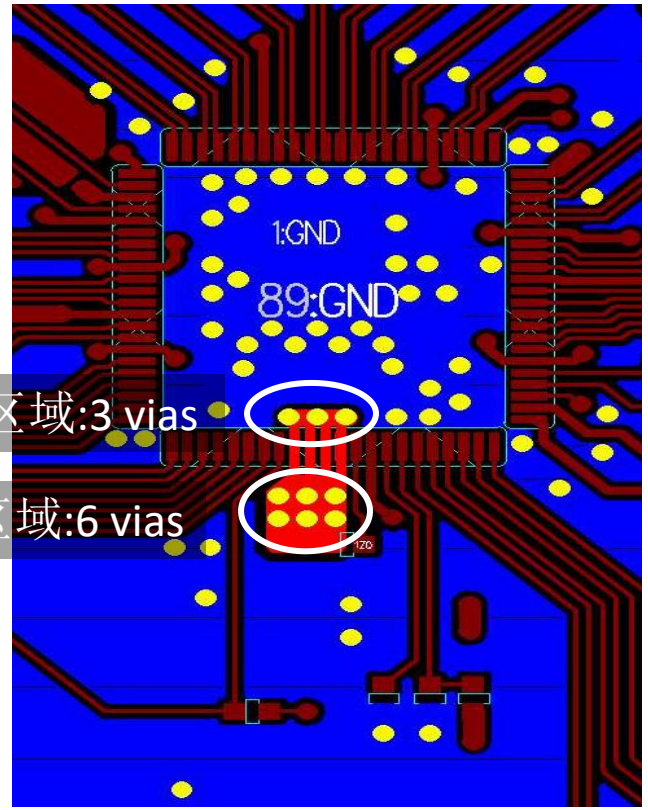
4L-PCB: DDR3_1.5V@L3
6L-PCB: DDR3_1.5V@L4



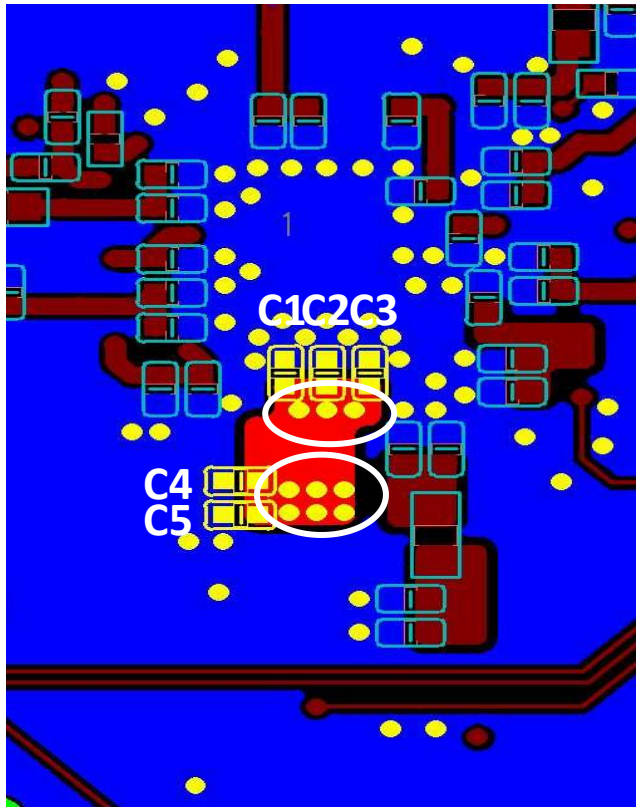
QFN - 4L/6L-PCB - DDR3Q_1.5V - Rule 3

Power	Layer	DeCap@Dram area	Layout rule
DDR3Q_1.5V	Top/Bottom	DDR3Q_1.5V@Bottom: (1) 0402 0.1uF: C1/C2 (2) 0402 1uF: C3/C4 (3) 0402 4.7uF: C1	(1) DDR3_1.5V VIA rule E-pad 区域 3 颗via紧连C1/C2/C3 Pin-out 区域 6颗 via紧连C4/C5 (1) GND VIA rule 确认每颗Cap旁至少1颗GND via

DDR3_1.5V@Top



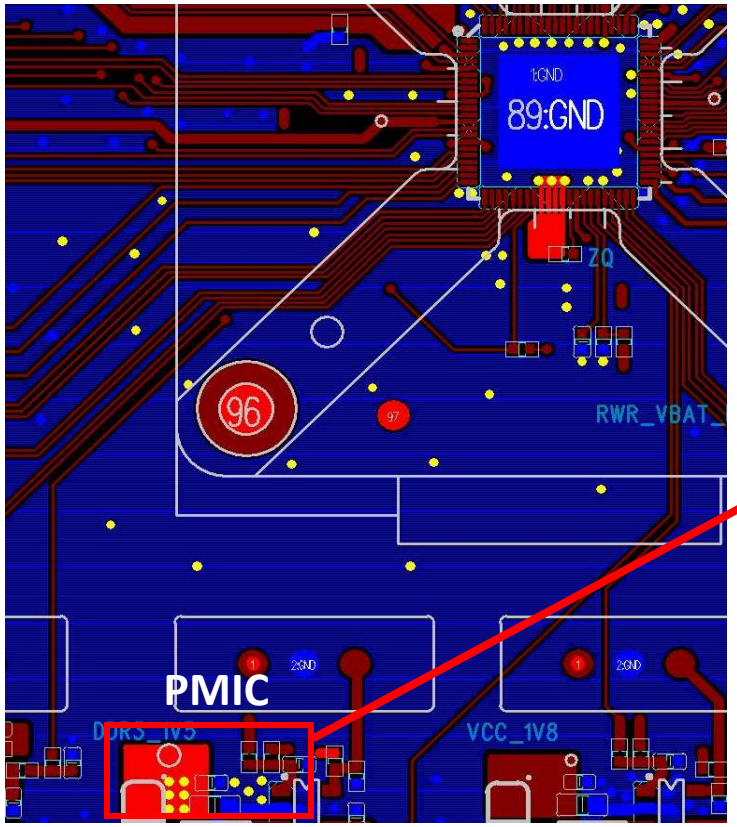
DDR3_1.5V@Bottom



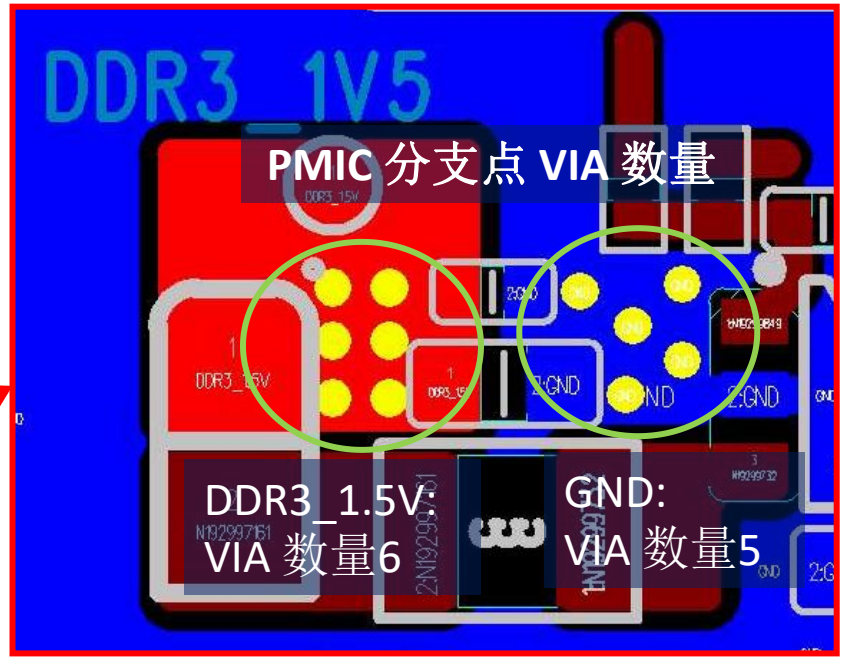
QFN - 4L/6L-PCB - DDR3_1.5V - Rule 4

Power	PMIC 分支点 VIA 数量
DDR3_1.5V	(1) DDR3_1.5V: VIA 数量>=6 (2) GND: VIA 数量>=5

DDR3_1.5V@Top



PMIC routing area



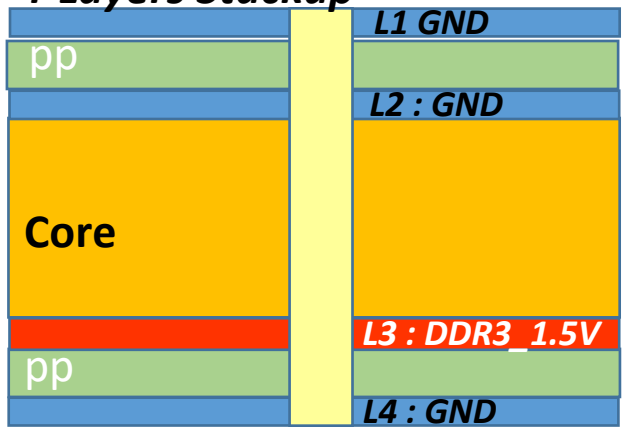
DDR 电源绕线 (DDR3_1.5V)

BGA PKG: CV181xH
4-layer/6-layer PCB

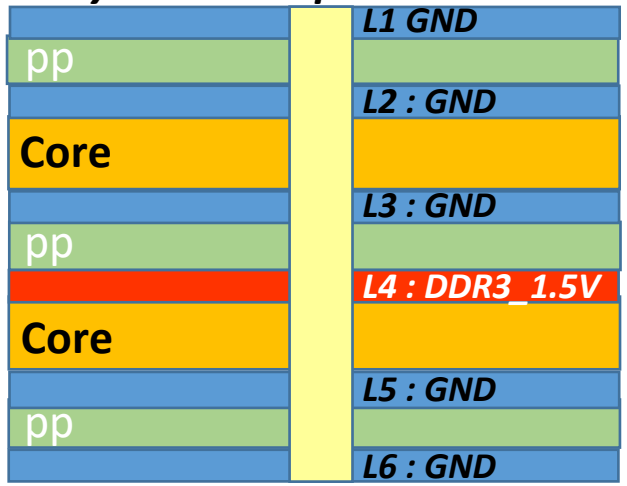
BGA – 4L/6L-PCB DDR Layout

- Stackup:
  (1) 4L-PCB: GND@L1/L2/L4 (plane), 6L-PCB: GND@L1/L2/L3/L4/L6 (plane)
  (2) 4L-PCB: DDR3_1.5V@L3 (shape), 6L-PCB: DDR3_1.5V@L4 (shape)

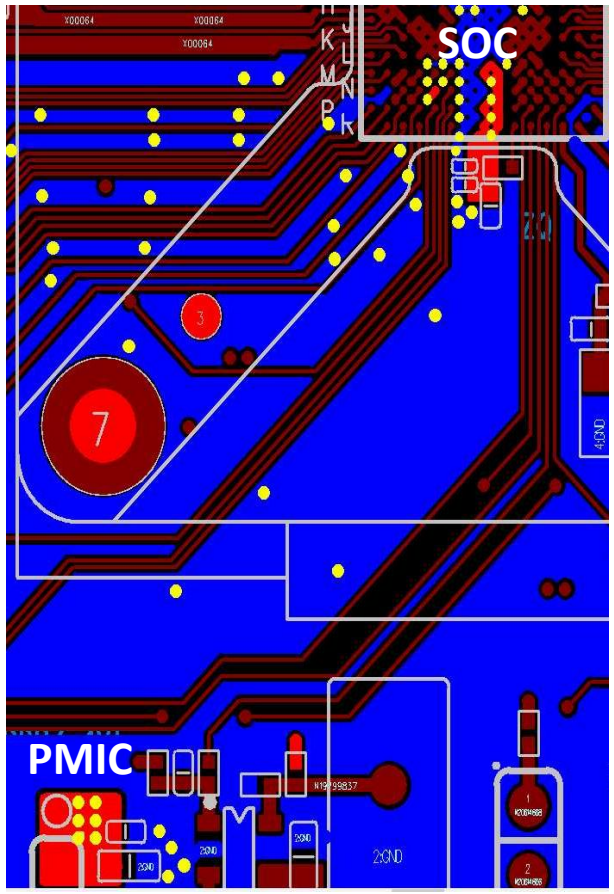
4-Layers Stackup



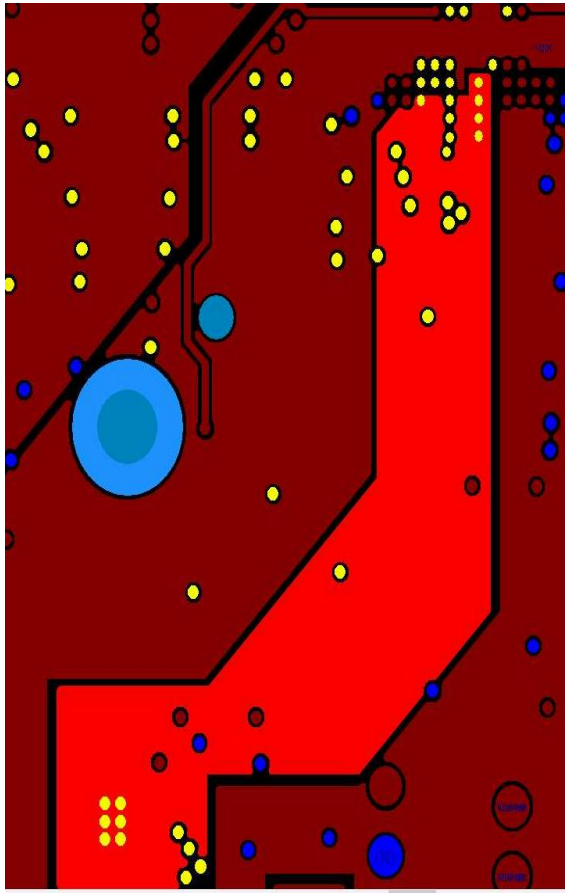
6-layers Stackup



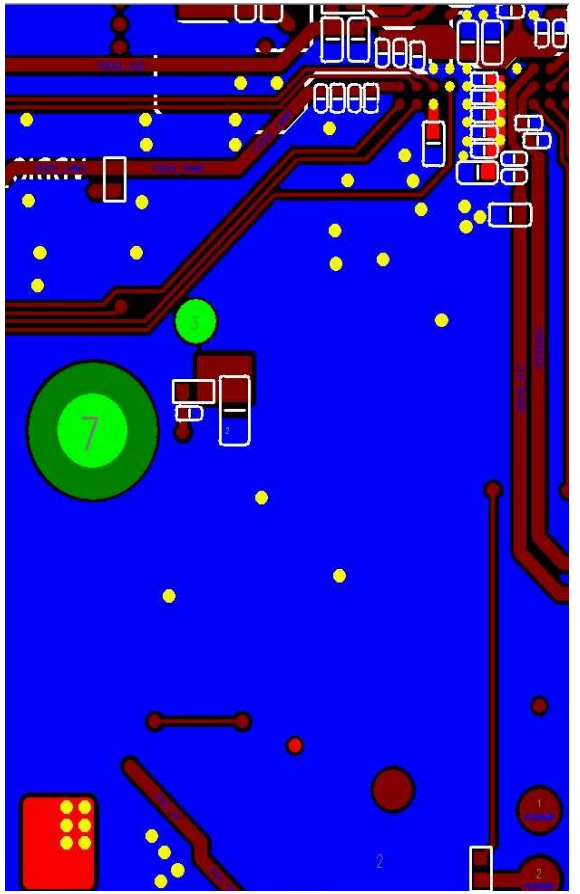
DDR3_1.5V@Top



4L-PCB: DDR3_1.5V@L3
6L-PCB: DDR3_1.5V@L4



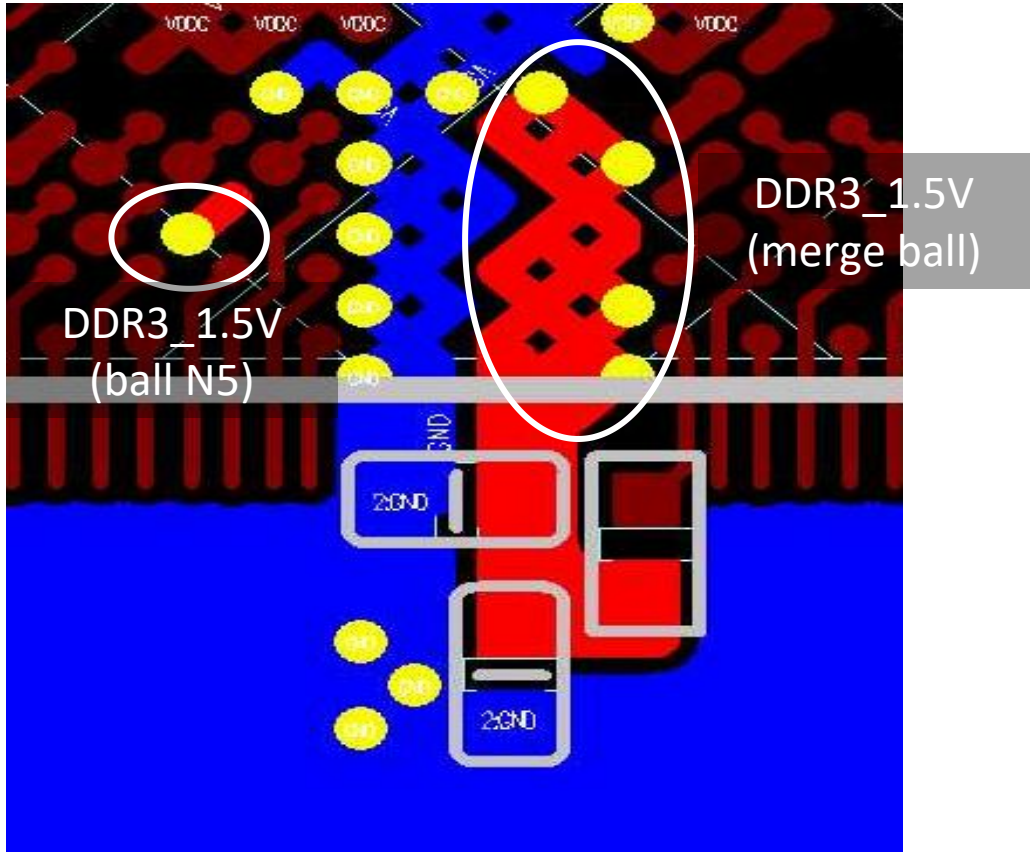
DDR3_1.5V@Bottom



BGA – 4L/6L-PCB - DDR3_1.5V - Rule 1

Power	Layer	SOC VIA count	Layout rule
DDR3_1.5V	Top	(1) DDR3_1.5V (ball N5): 1 (2) DDR3_1.5V (merge ball): 4	(1) 确认DDR3_1.5V SOC 端VIA数量 (2) Ball N5 VIA: 连接bottom Cap (3) Merge ball VIA: 连接内层main route trace

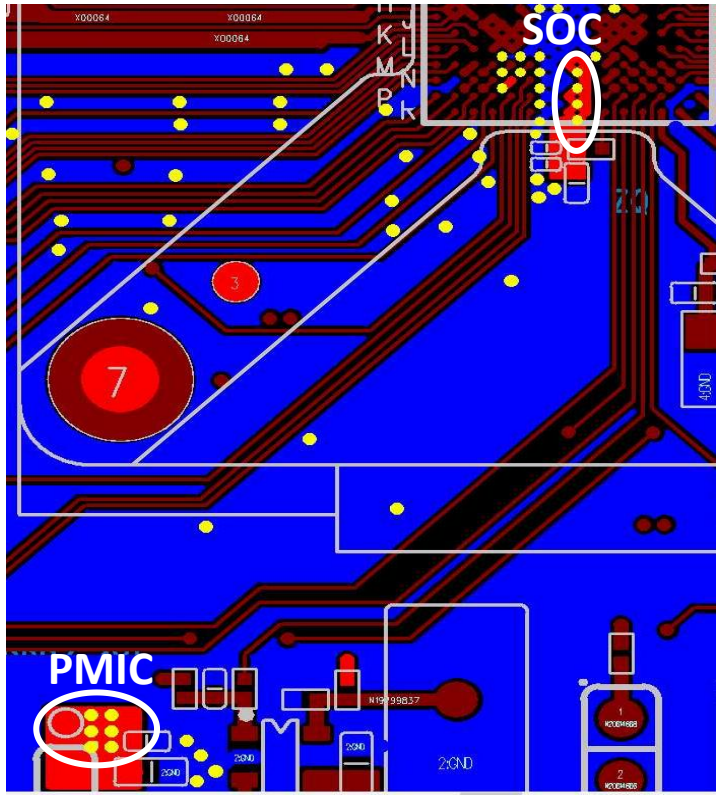
DDR3_1.5V@Top



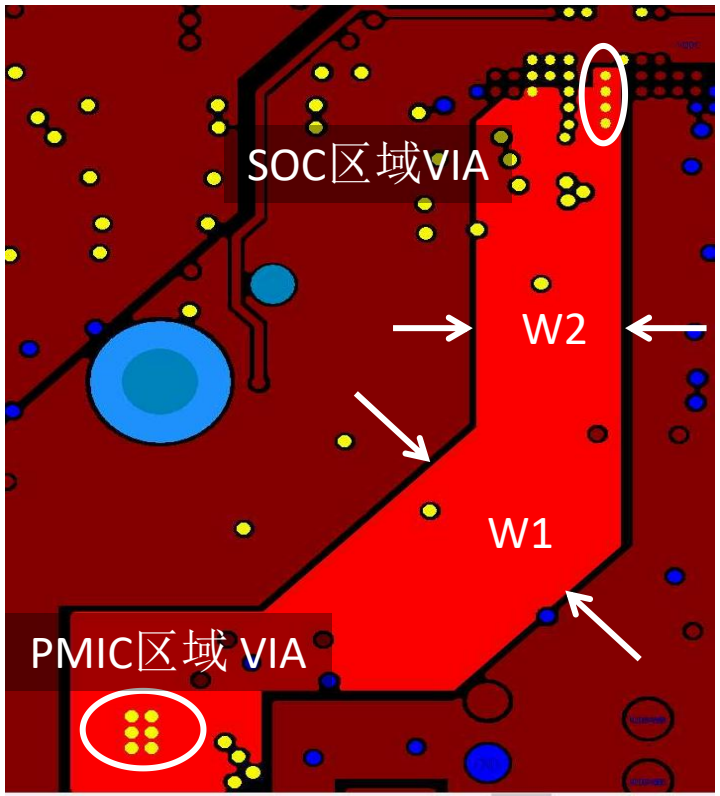
BGA – 4L/6L-PCB - DDR3_1.5V - Rule 2

Power	Layer	Layout rule
DDR3_1.5V	4L-PCB: DDR3_1.5V@L3 6L-PCB: DDR3_1.5V@L4	DDR3_1.5V main route: (1) 确认SOC处有下4颗VIA, PMIC处有下大于等于5颗VIA (2) 扣除破孔有效宽度: W1>=1.5mm, W2>=1.5mm

DDR3_1.5V@Top



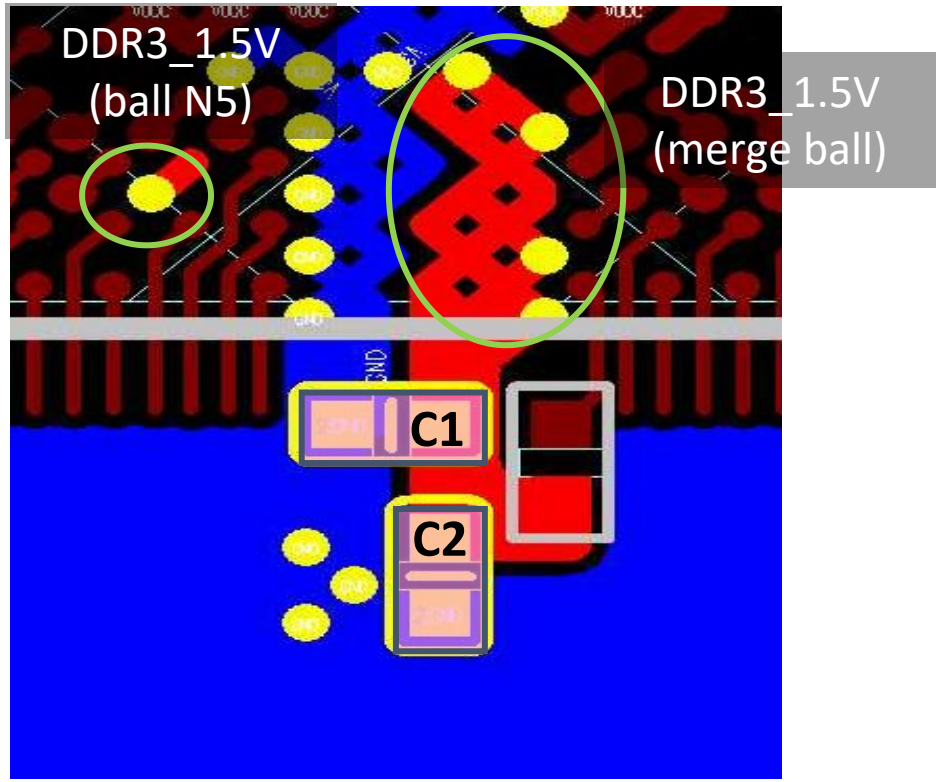
4L-PCB: DDR3_1.5V@L3
6L-PCB: DDR3_1.5V@L4



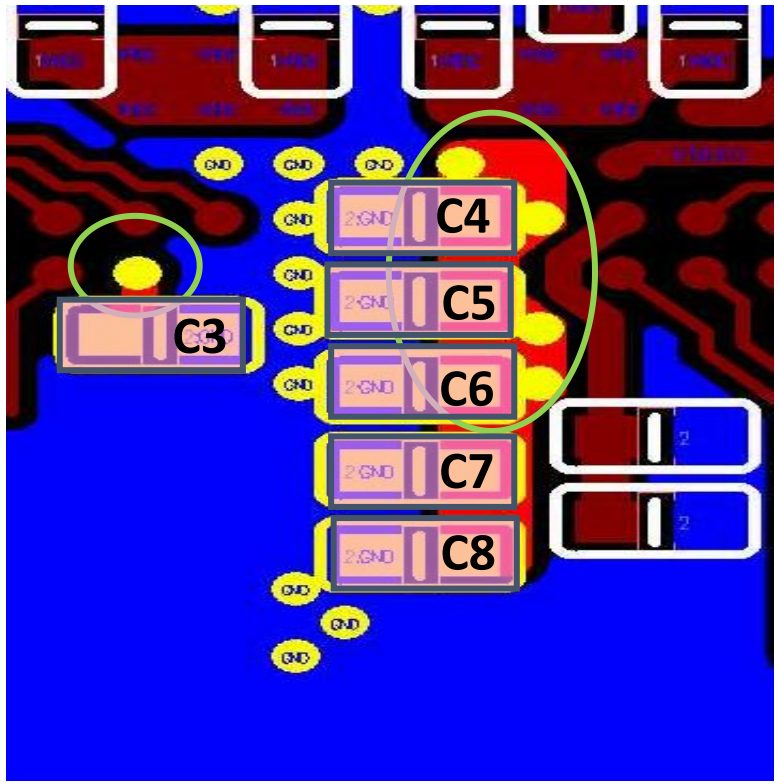
BGA – 4L/6L-PCB - DDR3Q_1.5V - Rule 3

Power	Layer	DeCap@Dram area	Layout rule
DDR3Q_1.5V	Top/Bottom	**DDR3Q_1.5V@Top:** (1) 0402 1uF: C1/C2 **DDR3Q_1.5V@Bottom:** (1) 0402 0.1uF: C4/C5 (2) 0402 1uF: C3/C7/C6 (3) 0402 4.7uF: C8	(1) DDR3_1.5V VIA rule 确认每颗Cap旁至少1颗DDR3_1.5V via (2) GND VIA rule 确认每颗Cap旁至少1颗GND via

DDR3_1.5V@Top



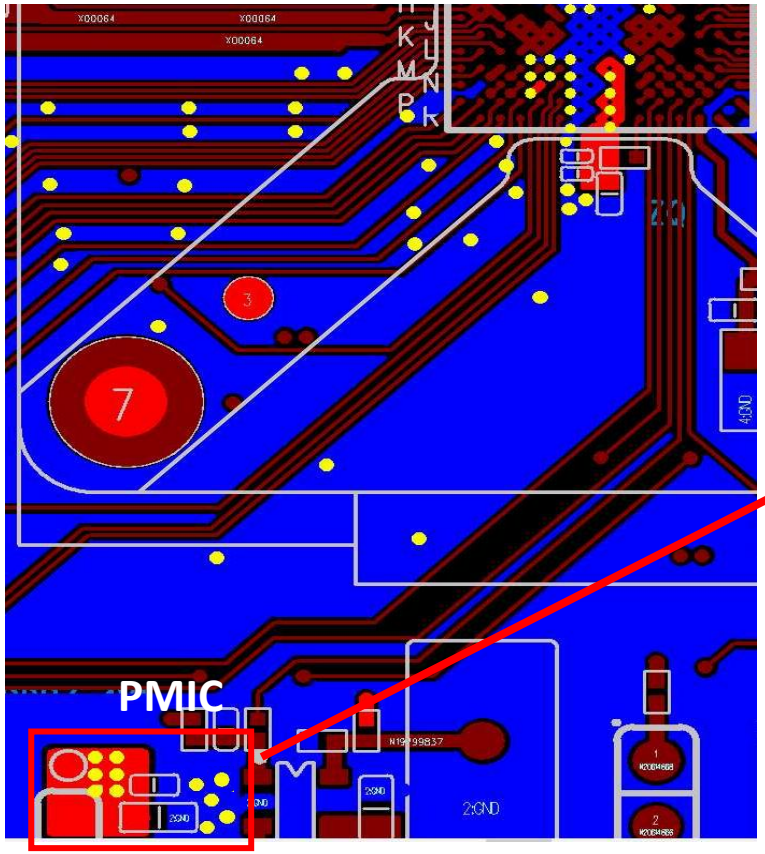
DDR3_1.5V@Bottom



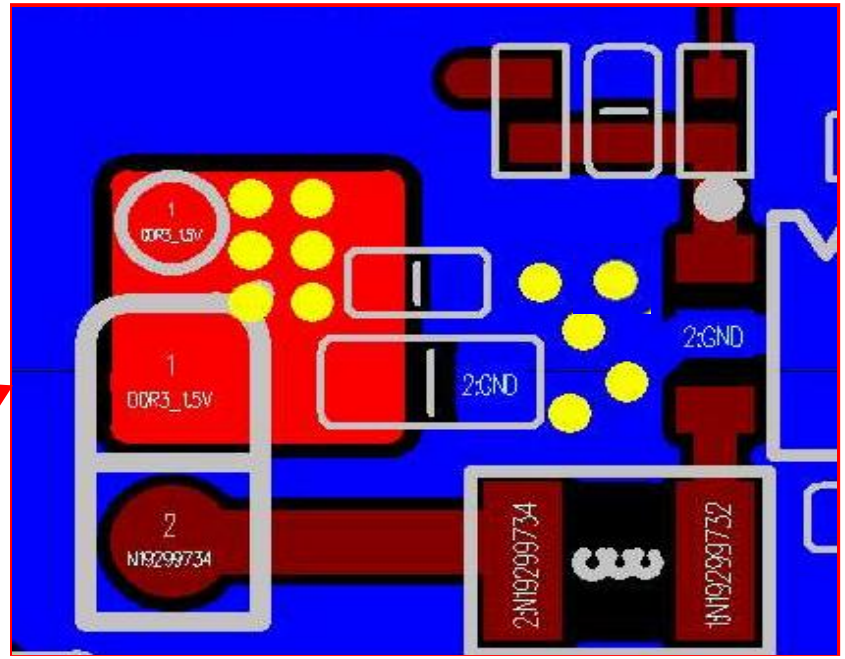
BGA – 4L/6L-PCB - DDR3_1.5V - Rule 4

Power	PMIC 分支点 VIA 数量
DDR3_1.5V	(1) DDR3_1.5V: VIA 数量>=6 (2) GND: VIA 数量>=5

DDR3_1.5V@Top



PMIC routing area

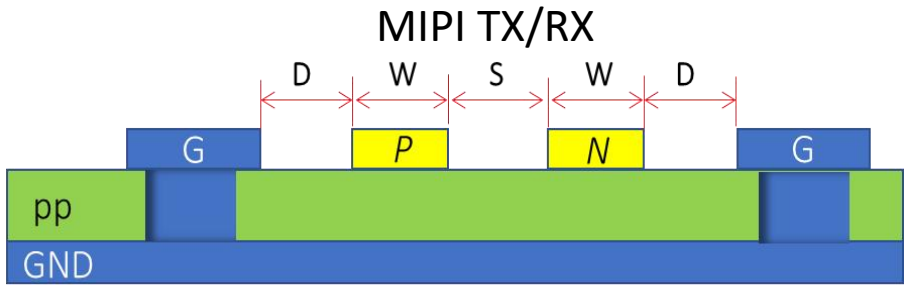


Serdes 讯号绕线

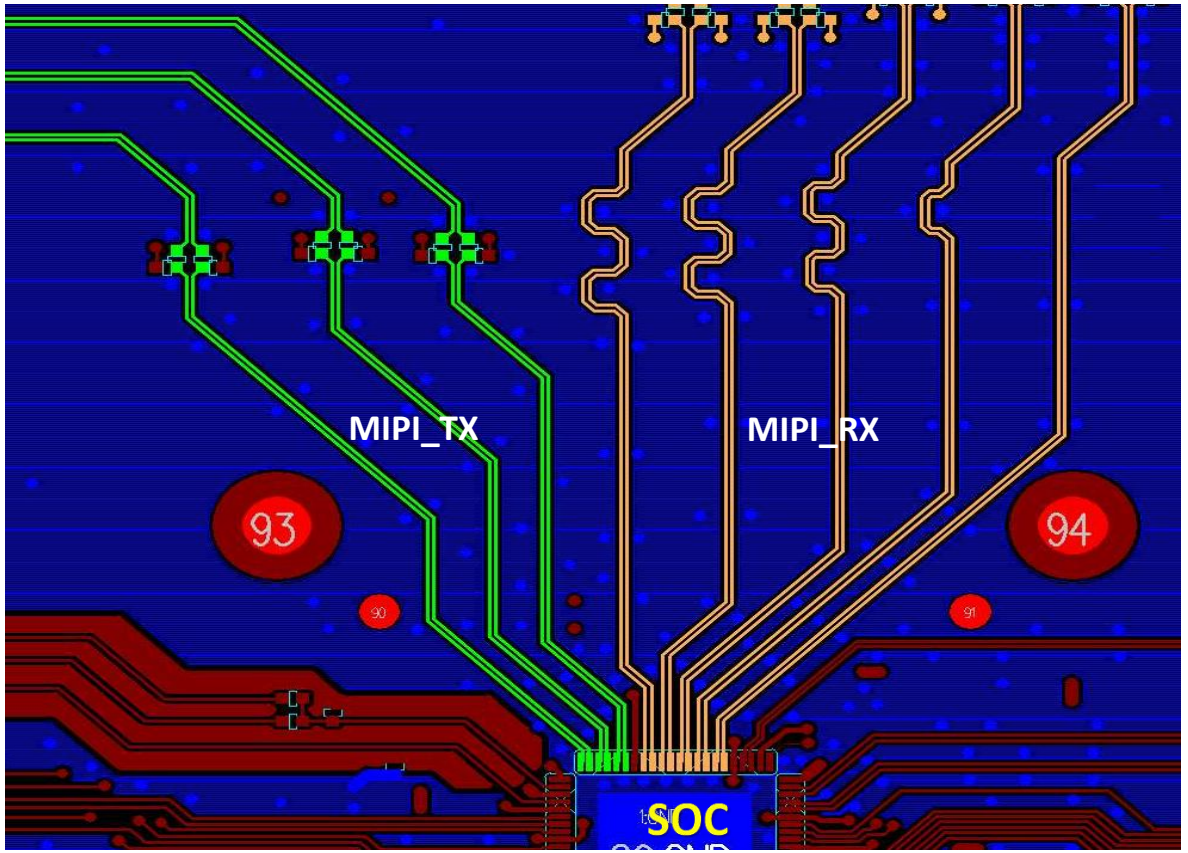
QFN/BGA PKG: CV181xC/CV181xH
4-layer/6-layer PCB

QFN/BGA – 4L/6L-PCB- MIPI Routing – 表层走线 Option1 Rule 1

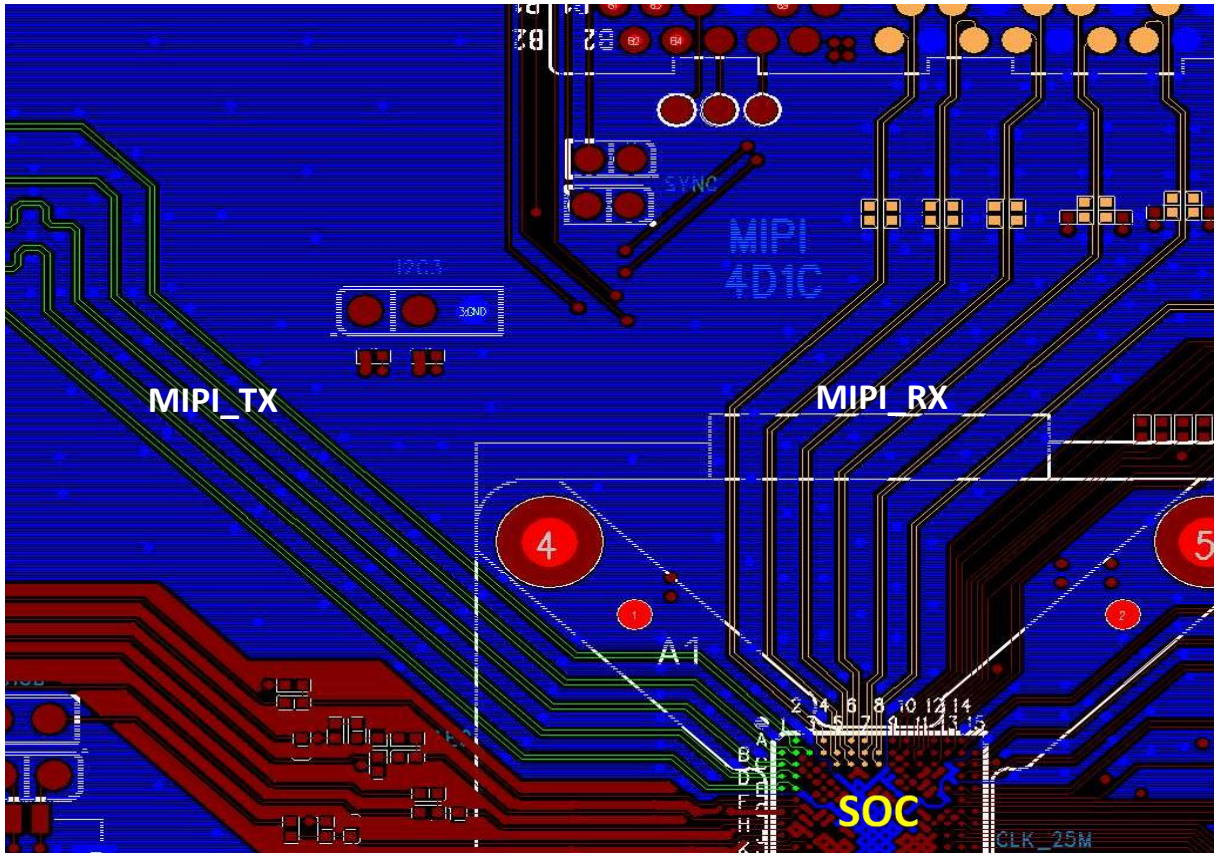
Signal	Layer	Zo	Trace width/spacing (mm)	Shielding Rule
MIPI_TX/RX Diff pair	Top/ Bottom	100 ohm	0.125/0.125/0.15 (W/S/D)	Lane to Lane GND shielding



QFN MIPI TX/RX differential signals layout@Top



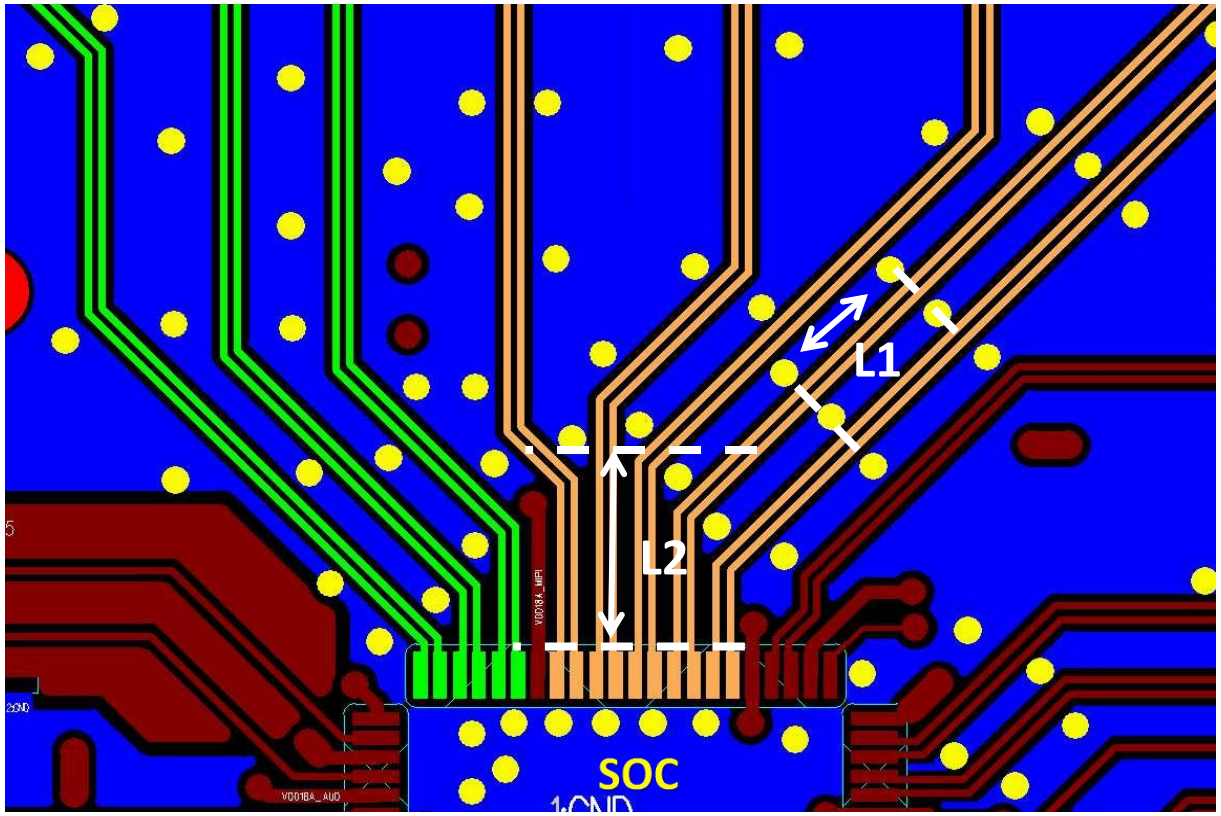
BGA MIPI TX/RX differential signals layout@Top



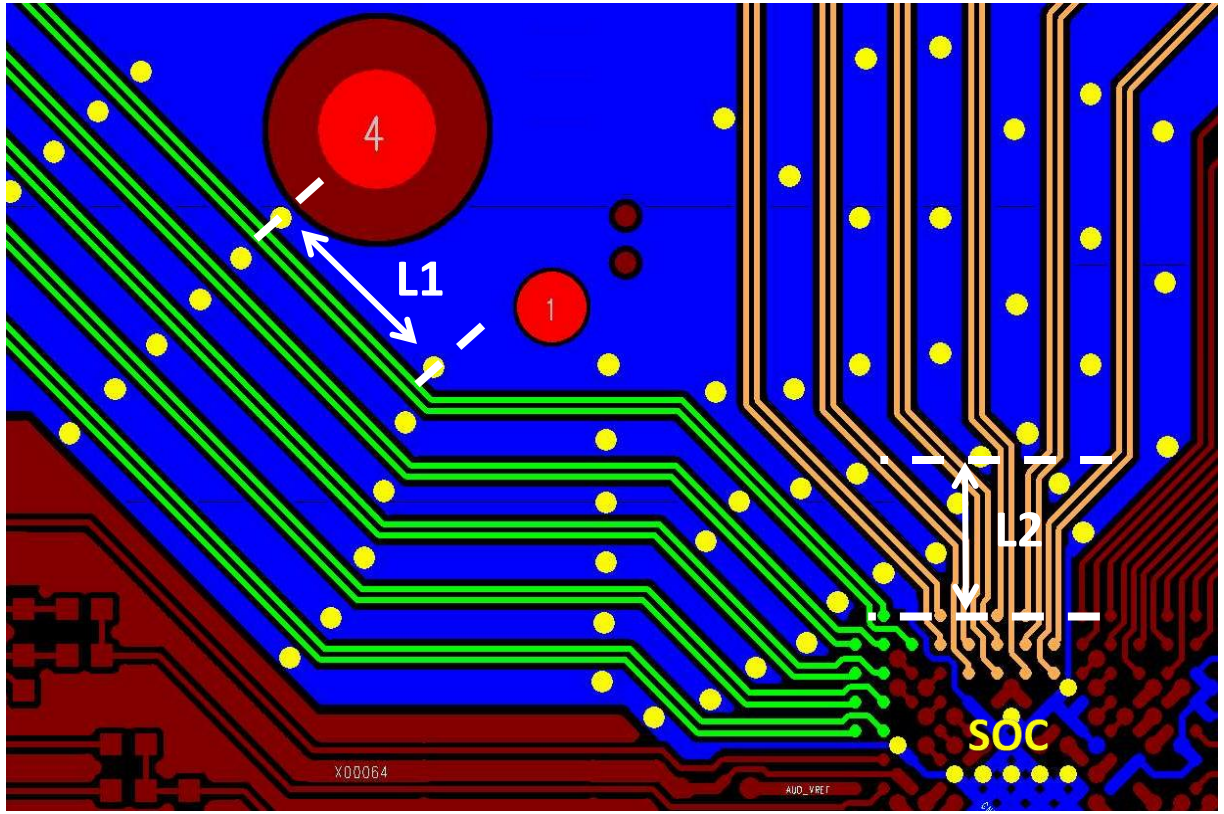
QFN/BGA – 4L/6L-PCB – MIPI Routing – 表层走线
Option1 - Rule 2

Signal	Layer	Requirement	Layout Rule
MIPI_TX/RX Diff pair	Top/ Bottom	Lane to lane shielding GND VIA distance	(1) L1 (GND stitching VIA) < 7.5mm (2) NO GND shielding length L2 < 3.5mm

QFN MIPI TX/RX shielding GND VIA distance@Top



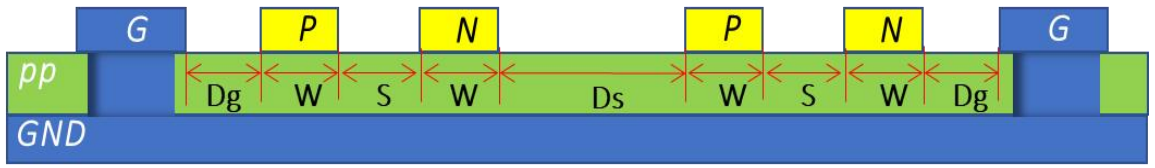
BGA MIPI TX/RX shielding GND VIA distance@Top



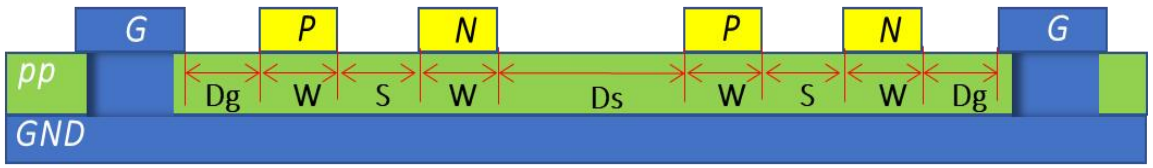
QFN/BGA – 4L/6L-PCB – MIPI Routing – 表层走线
Option2 - Rule

Signal	Layer	Zo	Trace width/spacing (mm)	Shielding Rule
MIPI_TX/RX Diff pair	Top/ Bottom	100ohm	0.125/0.125/0.3/0.3 (W/S/Ds/Dg)	(1) Lane to Lane NO GND shielding, 确认diff底下GND plane完整 (2) TX/RX Group GND shielding, GND shielding必须下VIA: **VIA to VIA 距离<7.5mm** (3) Lane to lane 距离限制: 1) 绕线长度>=10mm, Ds=3W, Dg=3W (可允许Dg=2W) 2) 绕线长度<10mm, Ds>=2W, Dg>=2W

MIPI TX



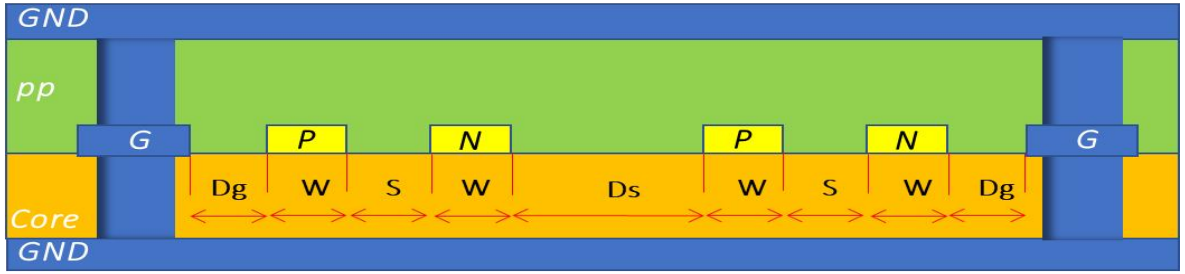
MIPI RX



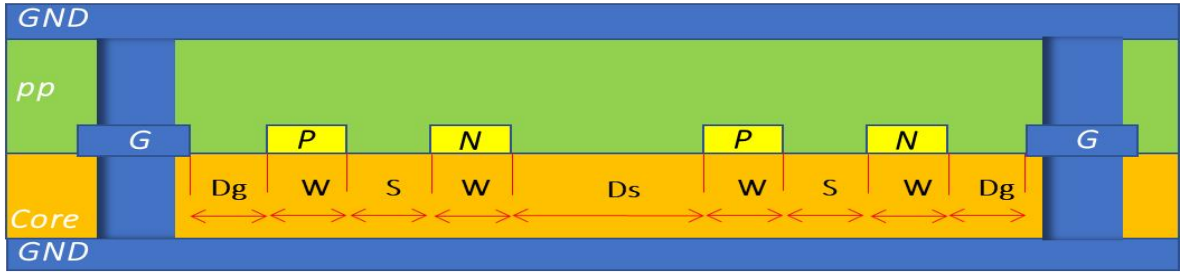
QFN/BGA – 4L/6L-PCB – MIPI Routing – 内层走线 - Rule

Signal	Layer	Zo (ohm)	Trace width/spacing (mm) (W/S/Ds/Dg)	Shielding Rule
MIPI_TX/RX Diff pair	4L-PCB: L2 6L-PCB: L3	100	4L-PCB: 0.125/0.25/0.3/0.3 6L-PCB: 0.125/0.25/0.3/0.3	(1) Lane to Lane NO GND shielding, 确认diff底下 GND plane完整 (2) TX/RX Group GND shielding, GND shielding必须下VIA: **VIA to VIA 距离<7.5mm** (3) Lane to lane 距离限制: 1) 绕线长度>=10mm, Ds=3W, Dg=3W (可允许Dg=2W) 2) 绕线长度<10mm, Ds>=2W, Dg>=2W

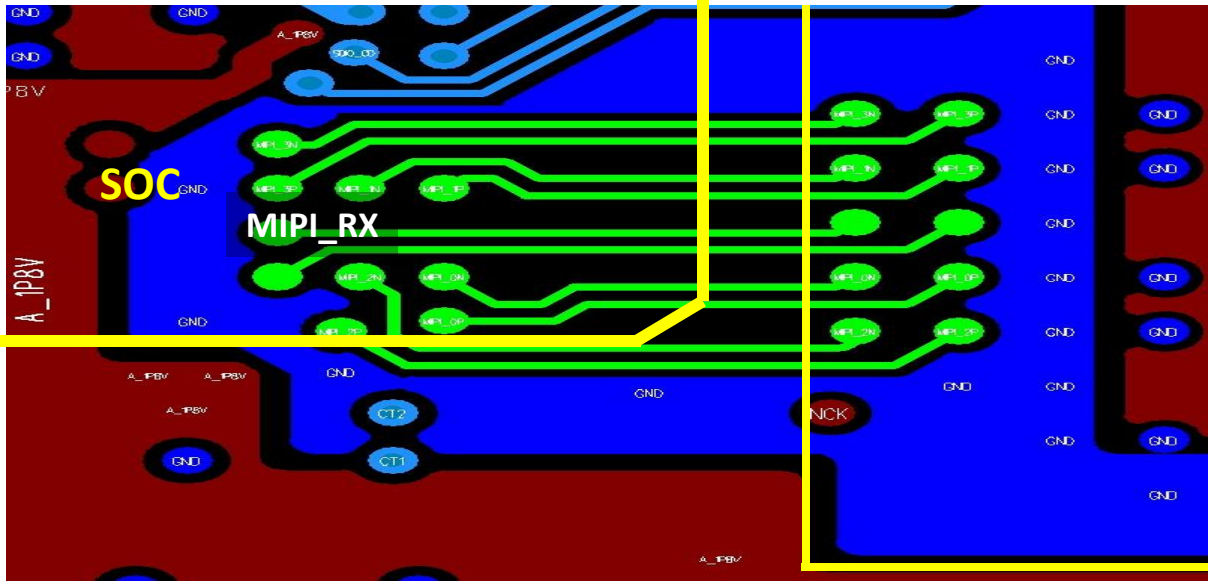
MIPI TX



MIPI RX



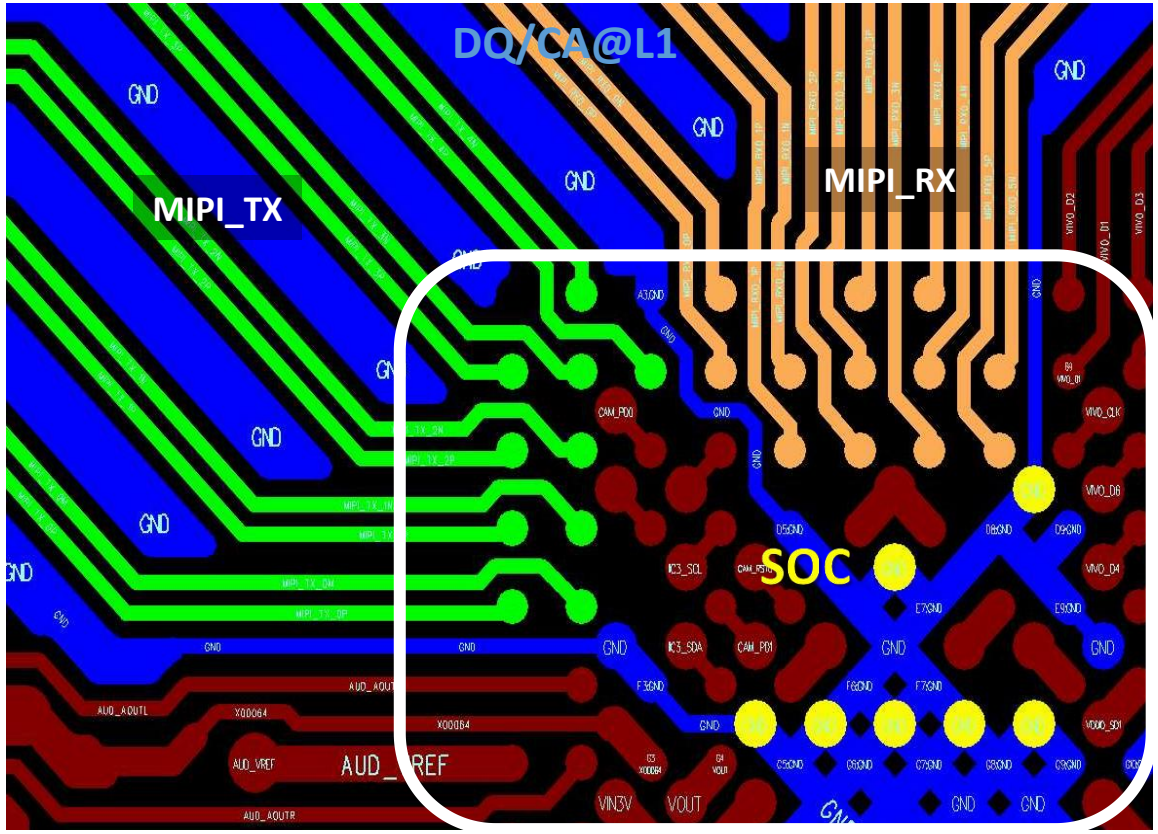
RX@内层, Option2, RX group GND shielding



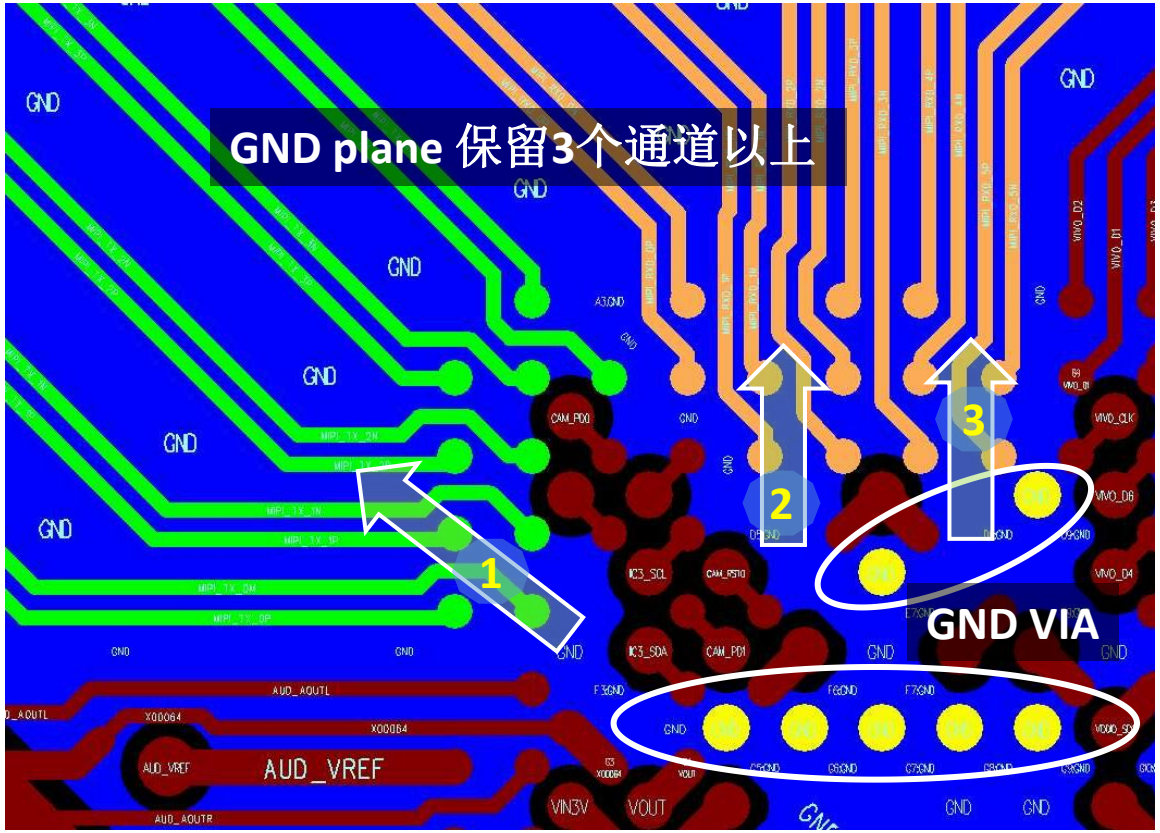
BGA – 4L/6L-PCB – MIPI Routing – GND Plane Rule

Signal	Layer	Layout rule
TX/RX GND plane	L2	确认TX/RX@SOC 下方GND plane@L2 的破孔会保留3组通道以上 (Layer2 GND plane 请参照下图)

MIPI TX/RX@Top



MIPI TX/RX@Top + GND plane@L2



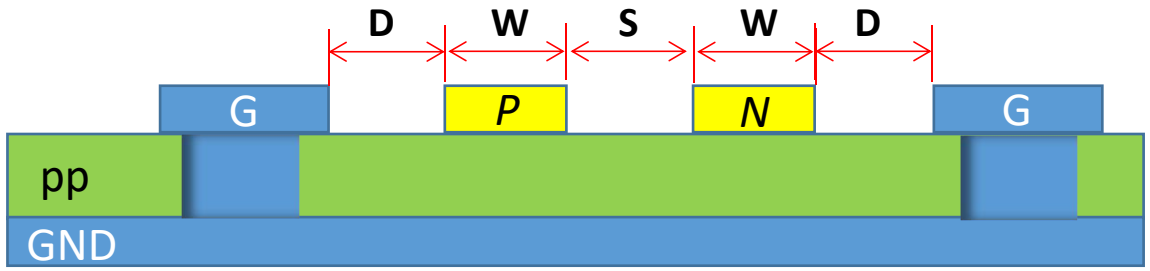
MIPI Routing – Length Matching Rule

Signal	Matching Reference	Matching Length
TX	inter skew	<=2.5mm (100mils)
RX	inter skew	
TX	P/N intra skew	<=0.5mm (20mils)
RX	P/N intra skew	

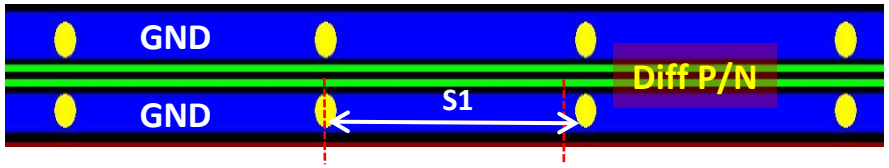
QFN/BGA – 4L/6L-PCB – USB Routing – 表层走线-Rule

Signal	Layer	Zo	Trace width/spacing (mm)	Shielding Rule
USB Diff pair	Top/ Bottom	90ohm	0.125/0.1/0.15 (W/S/D)	(1) Lane to lane GND shielding. (2) Shielding GND VIA: Lane to Lane GND shielding必须下VIA (VIA to VIA 距离<=7.5mm)

USB Diff pair



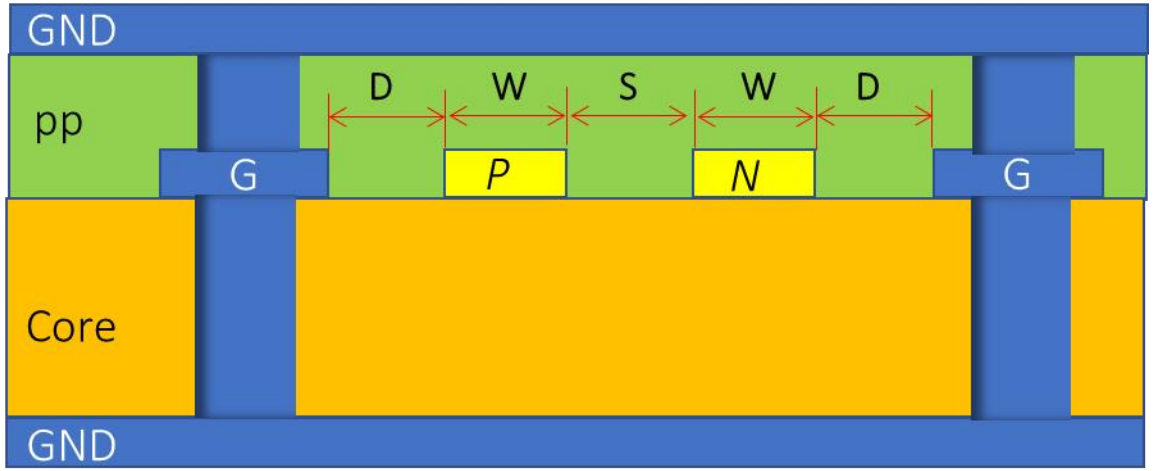
Shielding GND VIA



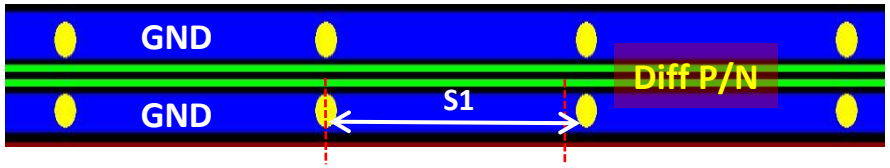
QFN/BGA – 4L/6L-PCB – USB Routing – 内层走线-Rule

Signal	Layer	Zo	Trace width/spacing (mm)	Shielding Rule
USB **Diff pair**	4L-PCB: L2 6L-PCB: L3	90ohm	4L-PCB: 0.125/0.175/0.15 (W/S/D) 6L-PCB: 0.125/0.175/0.15 (W/S/D)	(1) Lane to lane GND shielding. (2) Shielding GND VIA: Lane to Lane GND shielding必须下VIA (VIA to VIA 距离 S1<=7.5mm)

USB Diff pair



Shielding GND VIA



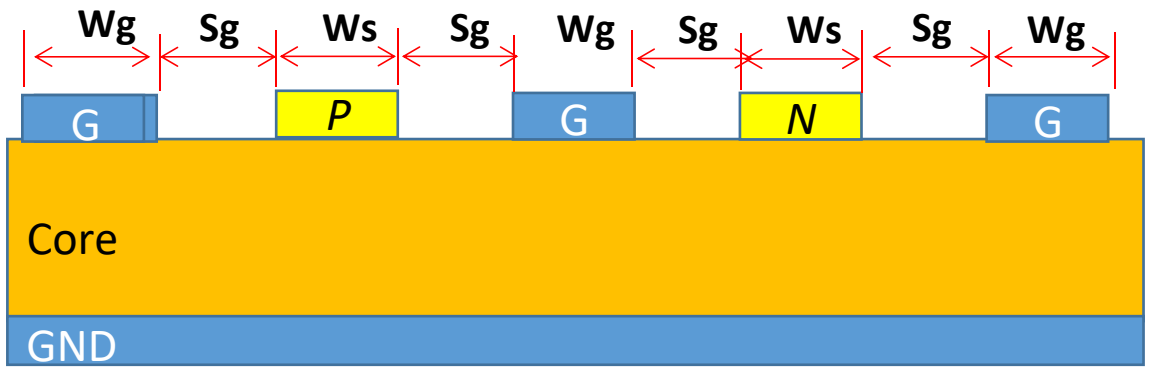
USB Routing – Length Matching Rule

Signal	Matching Reference	Matching Length
USB_DM **USB_DP**	P/N intra skew	<=0.5mm (20mils)

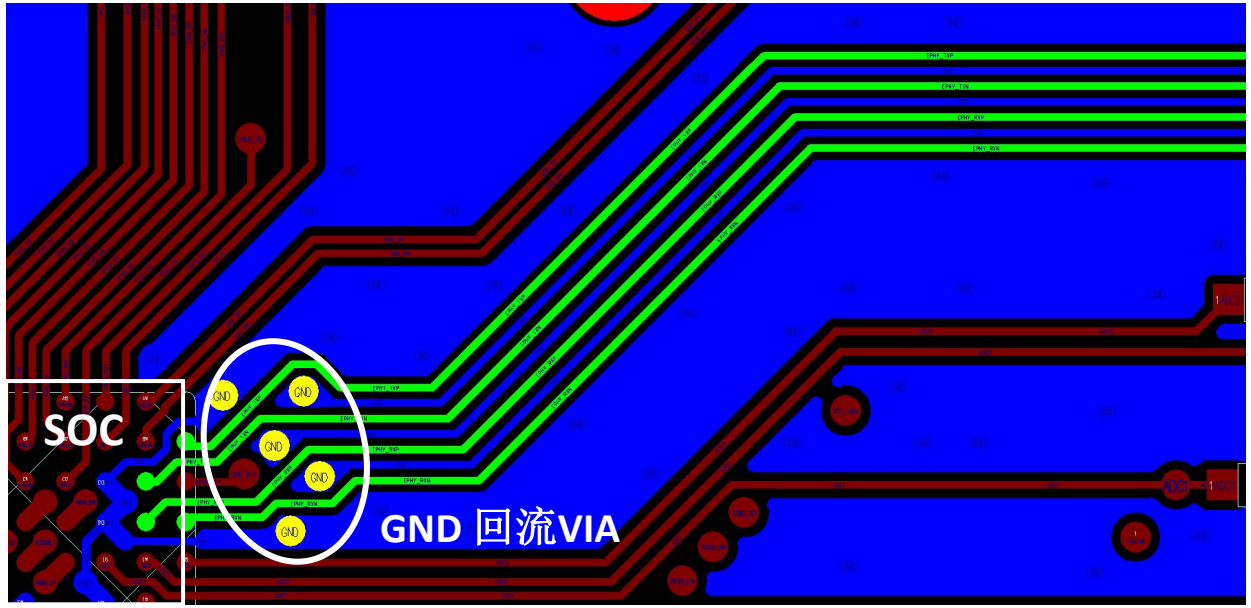
QFN/BGA – 4L/6L-PCB - EPHY Routing – 表层走线 - Rule1

Signal	Layer	Zo	Trace width/spacing (mm)	Shielding Rule
EPHY TX/RX Diff pair	Top	No control	0.125/0.125/0.125 (Ws/Sg/Wg)	(1) P/N 之间须有GND trace shielding (2) TX/RX 之间须有GND trace shielding (3) GND trace VIA rule: 1) 需确认靠近SOC端的GND trace 至少有一颗VIA与SOC PKG GND 构成回路 2) 需确认靠近transformer端的GND trace至少有一颗VIA与transformer GND pin构成回路

EPHY TX/RX



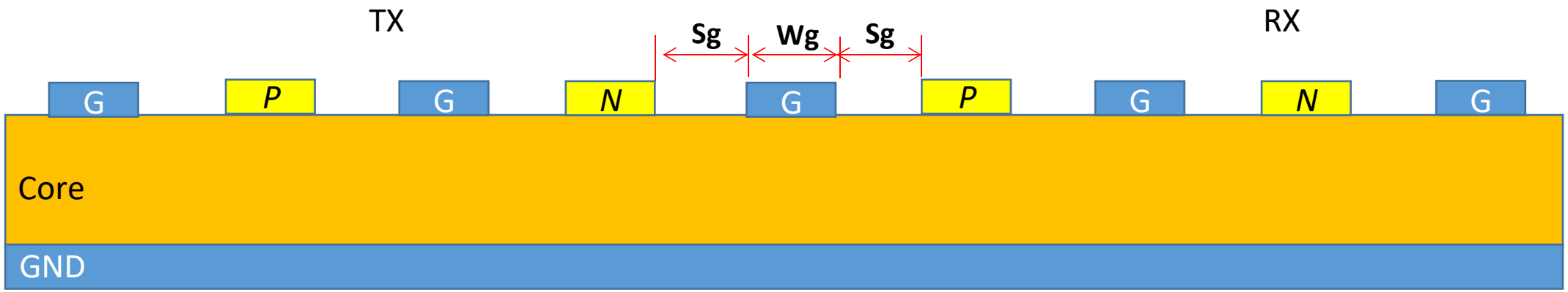
Shielding GND VIA



QFN/BGA – 4L/6L-PCB - EPHY Routing – 表层走线 - Rule2

Signal	Layer	Requirement	Layout Rule
EPHY TX/RX	Top	TX to RX GND shielding 0.125/0.125 (Wg/Sg)	GND trace VIA rule: 1) 需确认靠近SOC端的GND trace 至少有一颗VIA与SOC PKG E-pad构成回路 2) 需确认靠近transformer端的GND trace至少有一颗VIA与transformer GND pin构成回路

EPHY TX/RX Isolation



EPHY Routing – Length Matching Rule

Signal	Matching Reference	Matching Length
EPHY TX/RX Diff pair	P/N intra skew	<=0.5mm (20mils)

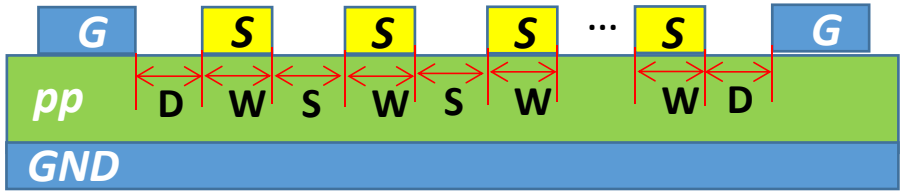
Single-end 讯号绕线

QFN/BGA PKG: CV181xC/CV181xH
4-layer/6-layer PCB

QFN/BGA – 4L/6L-PCB - Single-end – Rule

Signal	Layer	Shielding Rule	Trace width/spacing (mm)
SDIO **RTC**	4L-PCB: Top/Bottom/L3 6L-PCB: Top/Bottom/L3	Break out (fan-out) region: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.1/0.1 (S/D) (0.1mm spacing)
		Main rout: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.15/0.1 (S/D) (0.15mm spacing)

NO GND trace shielding

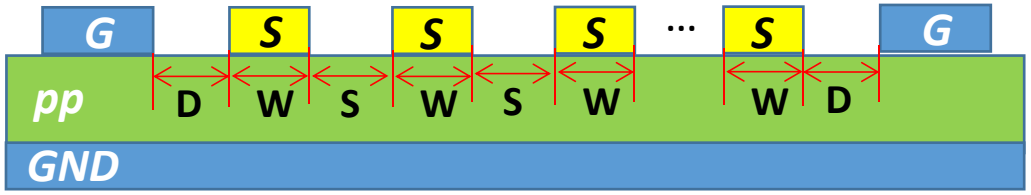


QFN/BGA - 4L/6L-PCB– EMMC – Rule

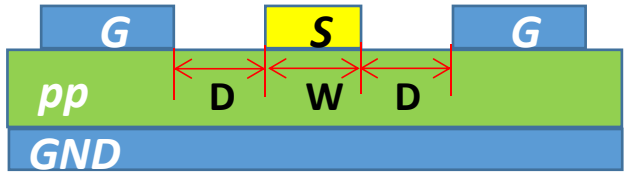
Signal	Layer	Shielding Rule	Trace width/spacing (mm)
EMMC **D0~D3**	Top	Break out (fan-out) region: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.1/0.1 (S/D) (0.1mm spacing)
		Main rout: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.15/0.1 (S/D) (0.15mm spacing)

Signal	Layer	Shielding Rule	Trace width/spacing (mm)
EMMC_CLK **EMMC_CMD** **EMMC_RST_N (BGA)**	4L-PCB: Top/Bottom/L3 6L-PCB: Top/Bottom/L3	Break out (fan-out) region: NO GND trace shielding, **ref GND plane**	(1) W>=0.1 (2) 0.1/0.1 (S/D)
		per trace shielding, **ref GND plane**	(1) W>=0.1 (2) D=0.1

NO GND trace shielding



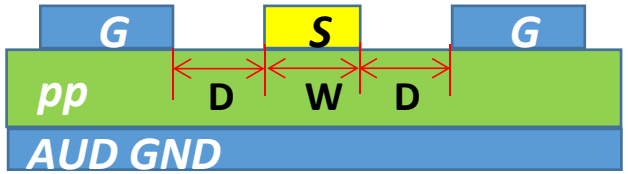
Per trace shielding



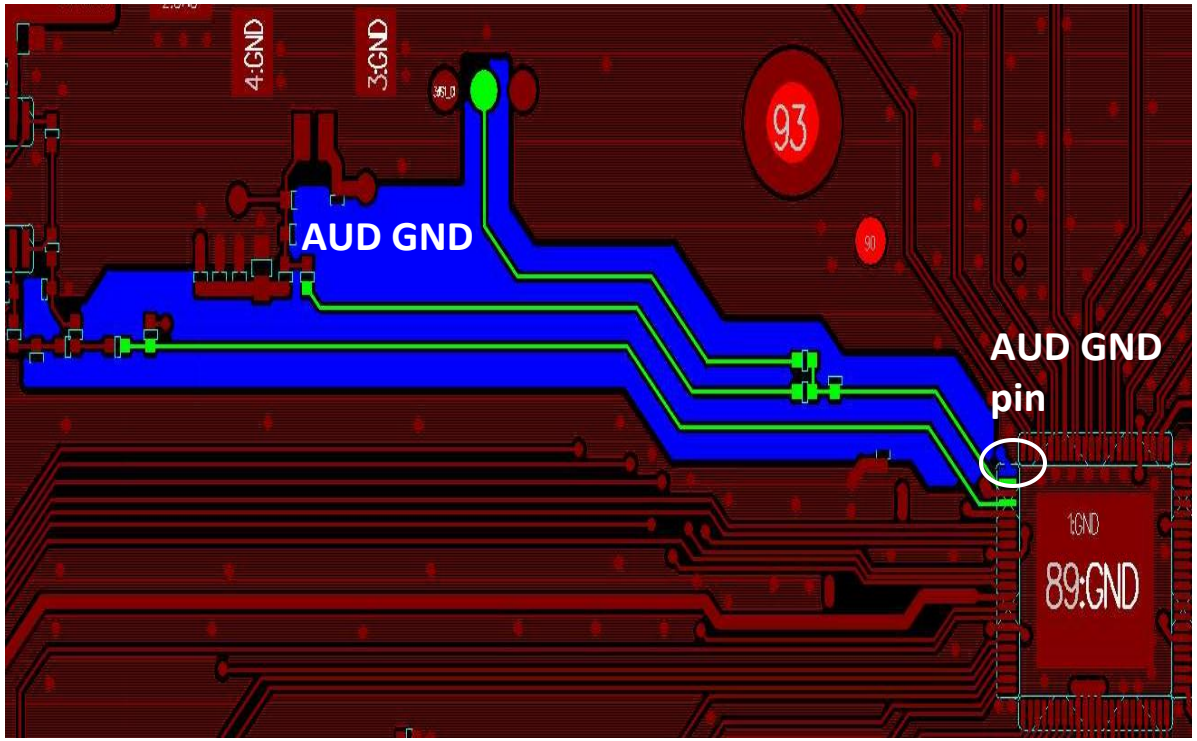
QFN 4L/6L-PCB – AUD – Rule

Signal	Layer	Shielding Rule	Trace width/spacing (mm)
AUD_MIC_L **AUD_MIC** **AUD_OUT**	Top	(1) per trace shielding **(2) ref AUD GND plane** **(3) 确认AUD 讯号线下方有完整AUD GND plane**	(1) W>=0.1 (2) D=0.1

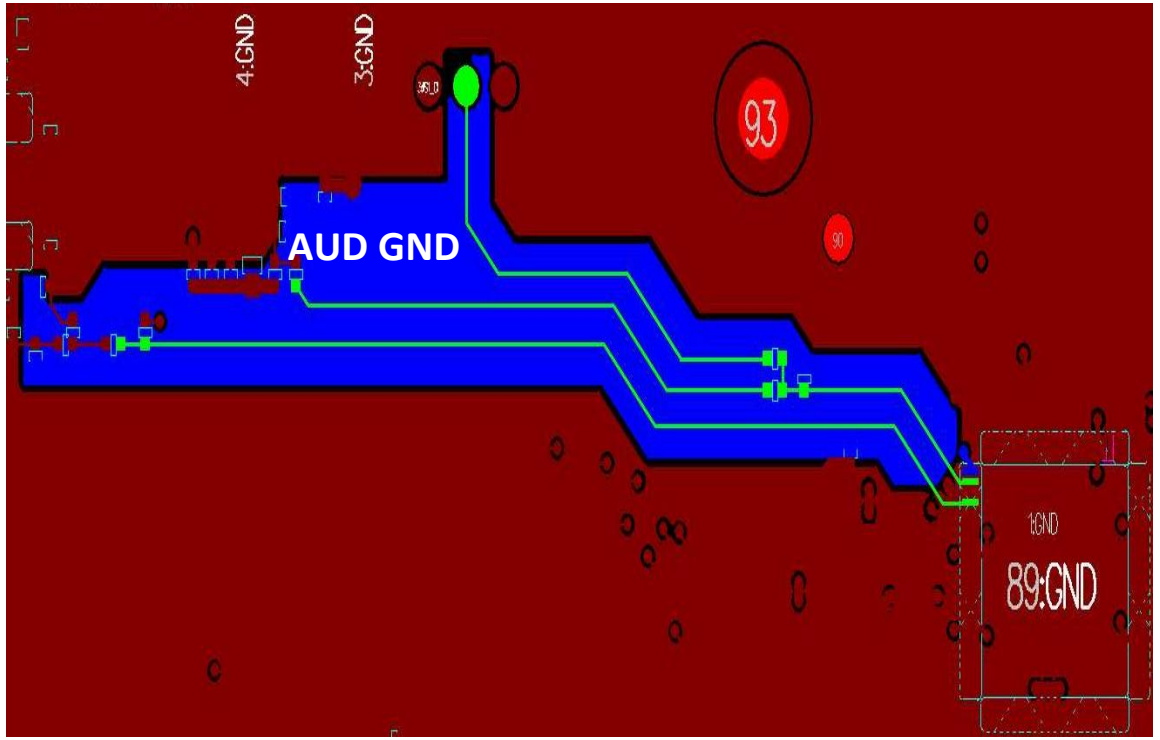
Per trace shielding



AUD@Top



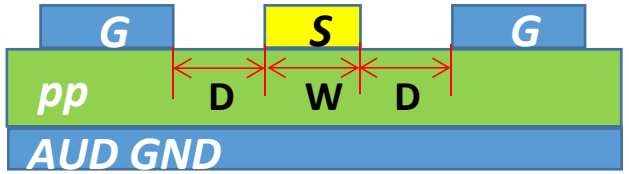
AUD@L1/L2



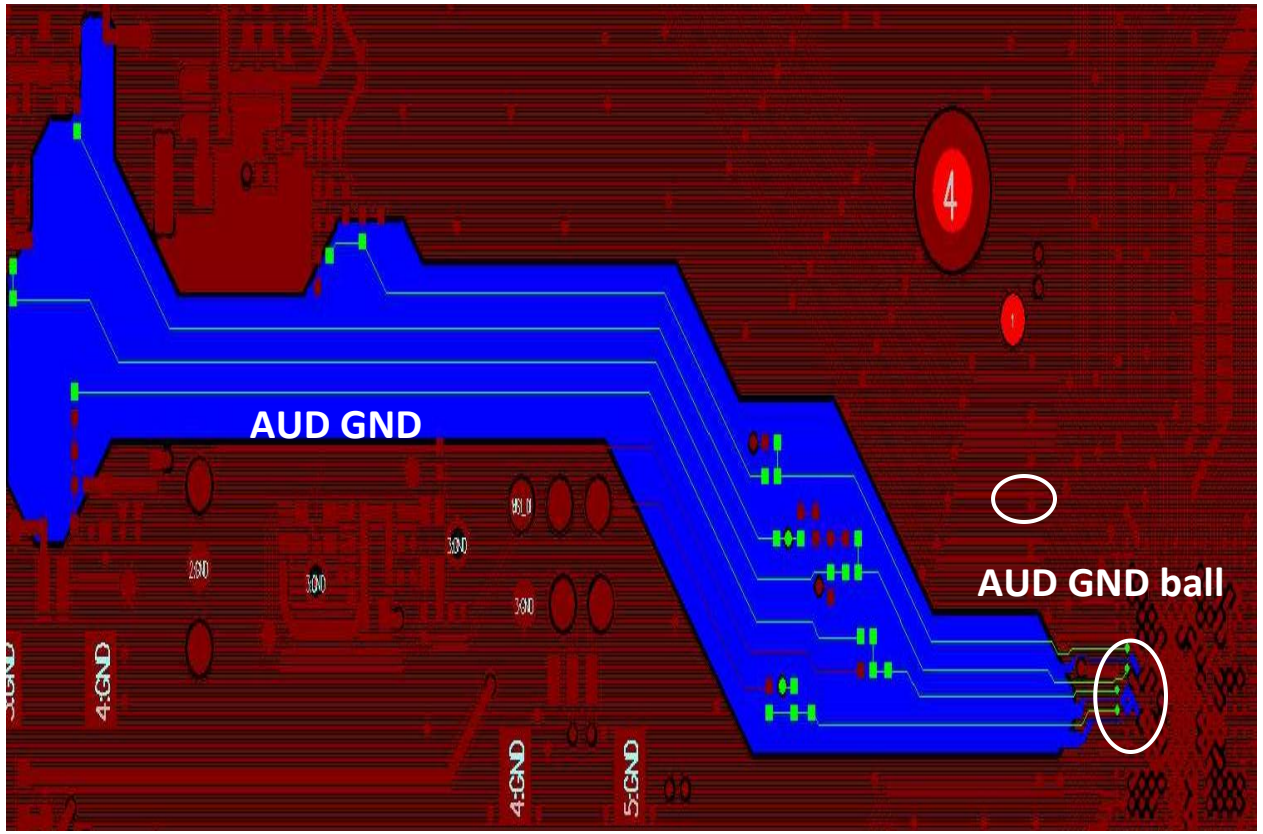
BGA – 4L/6L-PCB – AUD – Rule

Signal	Layer	Shielding Rule	Trace width/spacing (mm)
AUD_MIC_L/AUD_MIC_R AUD_MICL/AUD_MICR AUD_AOUTL/AUD_AOUR AC_AOUTL/AC_AOUR	Top	(1) per trace shielding **(2) ref AUD GND plane** **(3) 确认AUD 讯号线下方有完整AUD GND plane**	(1) W>=0.1 (2) D=0.1

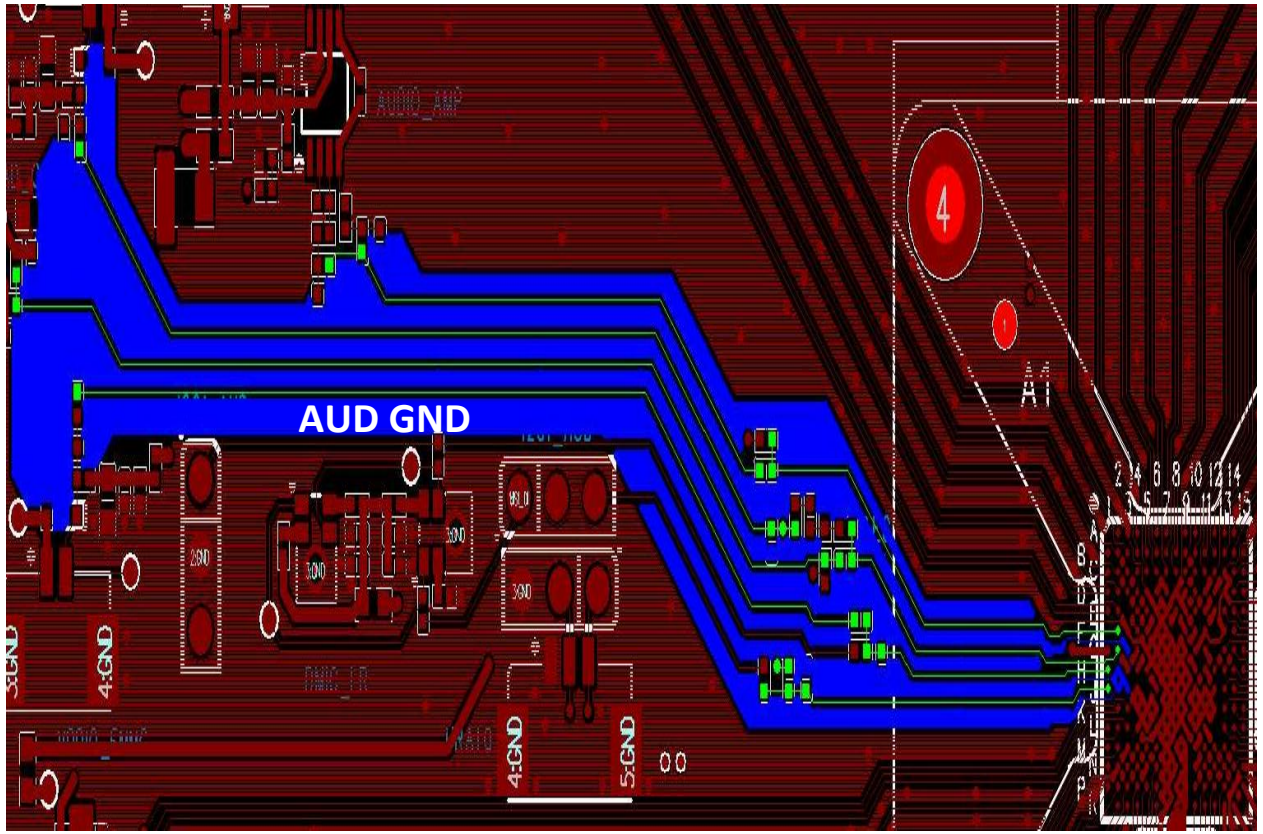
Per trace shielding



AUD@Top



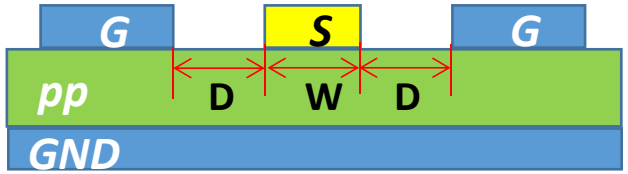
AUD@L1/L2



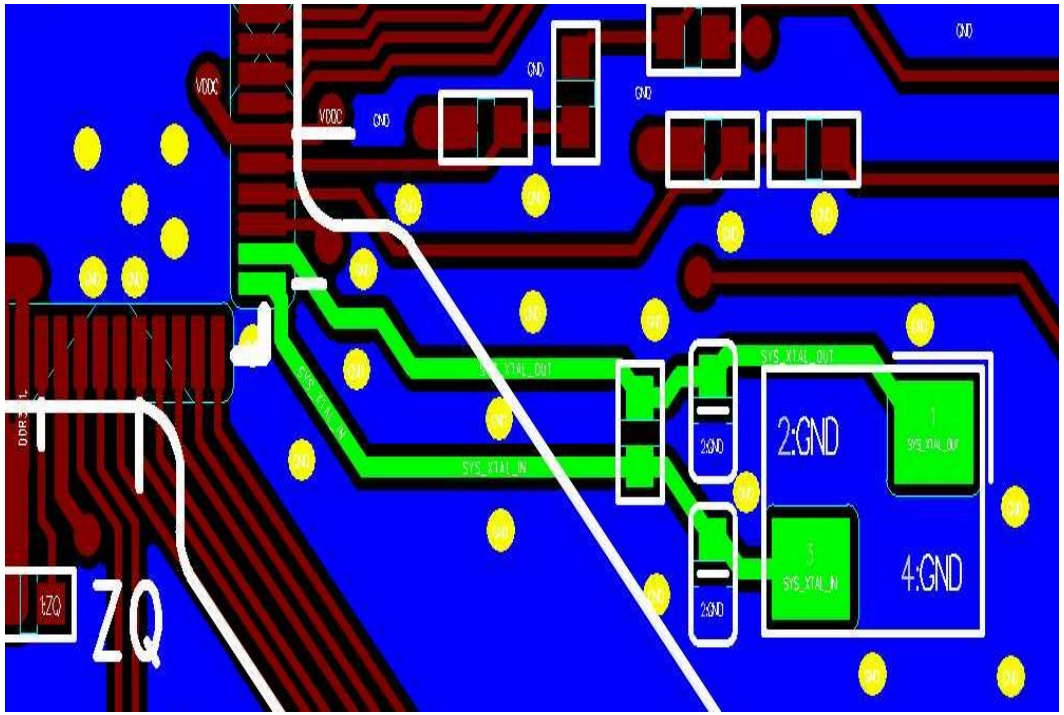
QFN/BGA – 4L/6L-PCB – XTAL_IN/OUT - Rule

Signal	Layer	Shielding Rule	Trace width/spacing (mm)
SYS_XTAL_IN **SYS_XTAL_OUT**	Top	**(1) per trace shielding** **(2) ref GND plane**	0.25/0.25 (W/D)

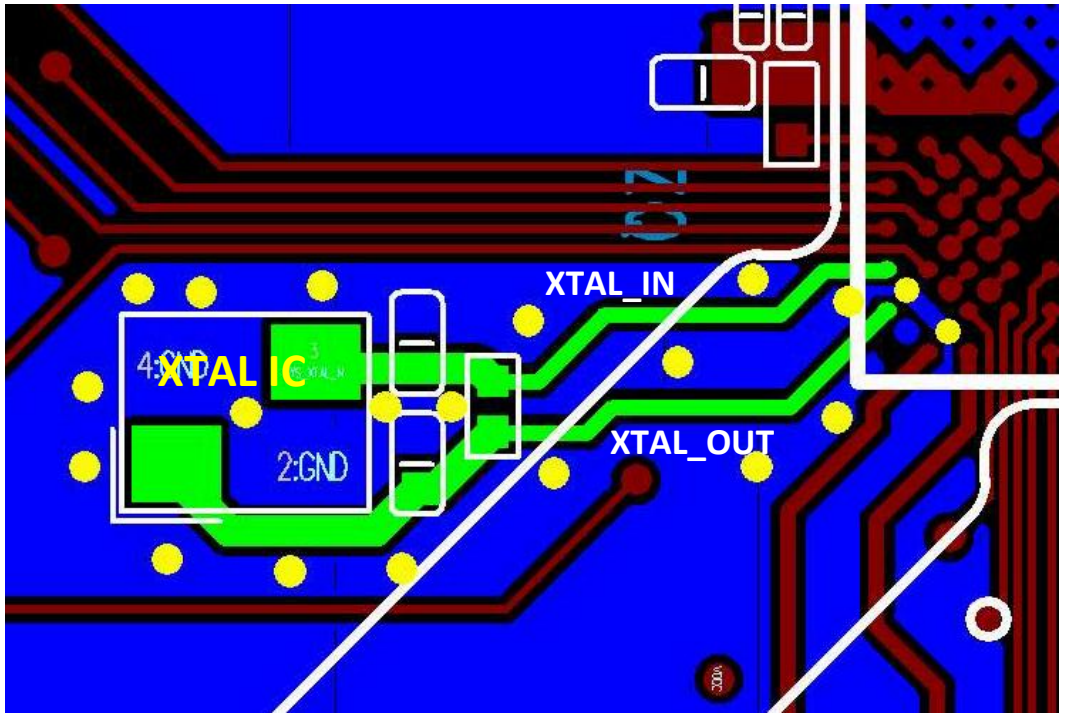
Per trace shielding



QFN XTAL@Top



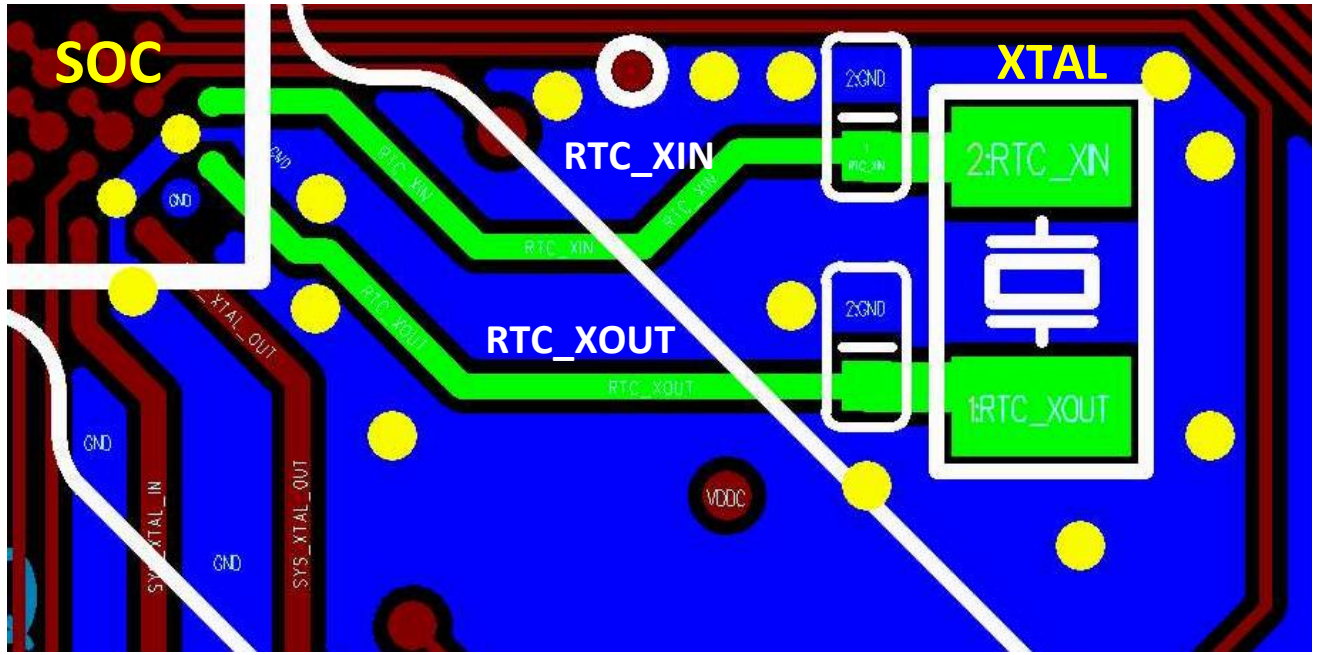
BGA XTAL@Top



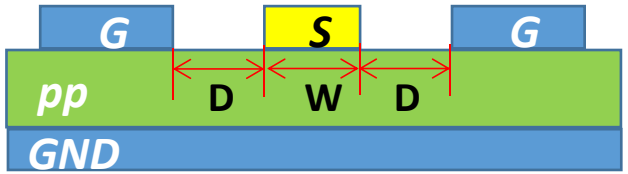
BGA only – 4L/6L-PCB – RTC_XIN/XOUT - Rule

Signal	Layer	Shielding Rule	Trace width/spacing (mm)
RTC_IN **RTC_OUT**	Top	电容 to XTAL: per trace shielding	0.25/0.1 (W/D)

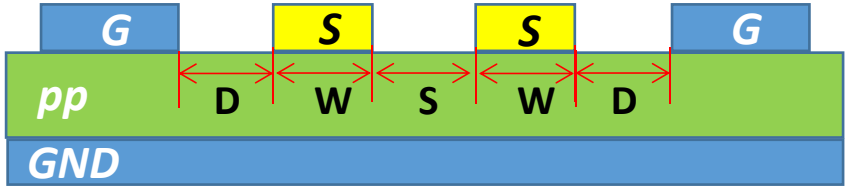
XTAL@L1



Per trace shielding



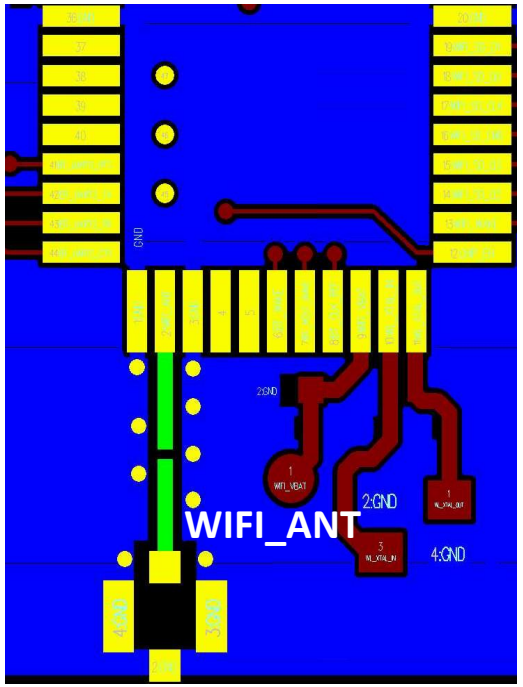
Two trace shielding



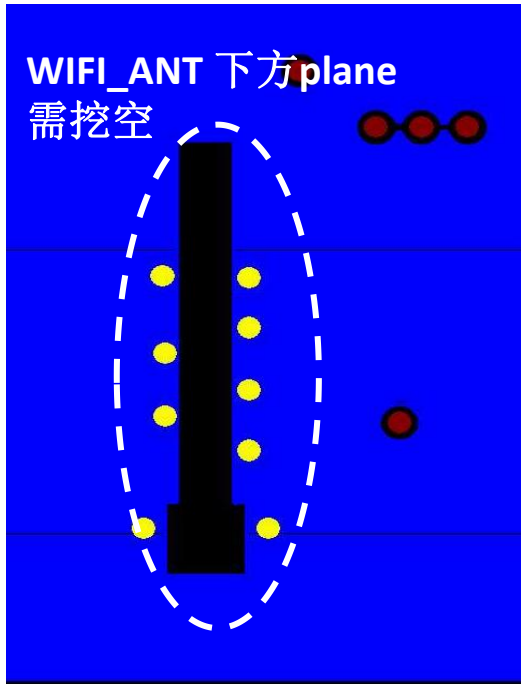
QFN/BGA – 4L/6L-PCB – WIFI_ANT Layout Rule

Signal	Layer	Zo	Shielding Rule	Trace width/spacing (mm)
WIFI_ANT	Top	50ohm	Per trace shielding	0.75/0.15/0.3 (W/D1/D2)

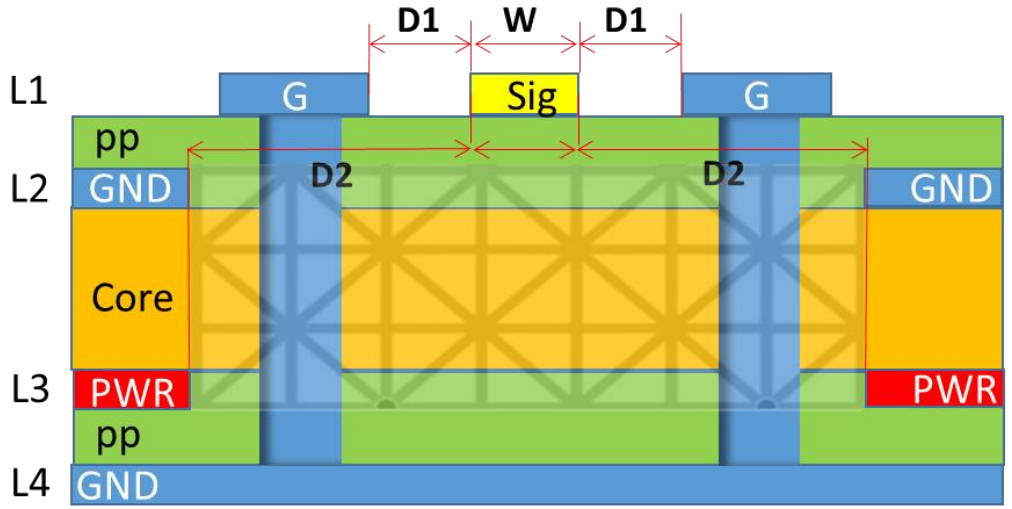
WIFI_ANT@Top



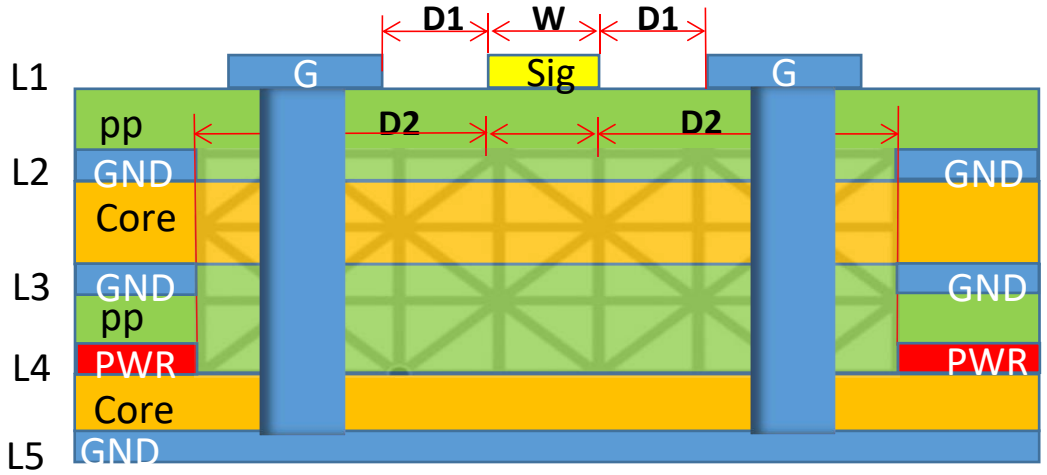
WIFI_ANT@GND/PWR plane



4L-PCB



6L PCB



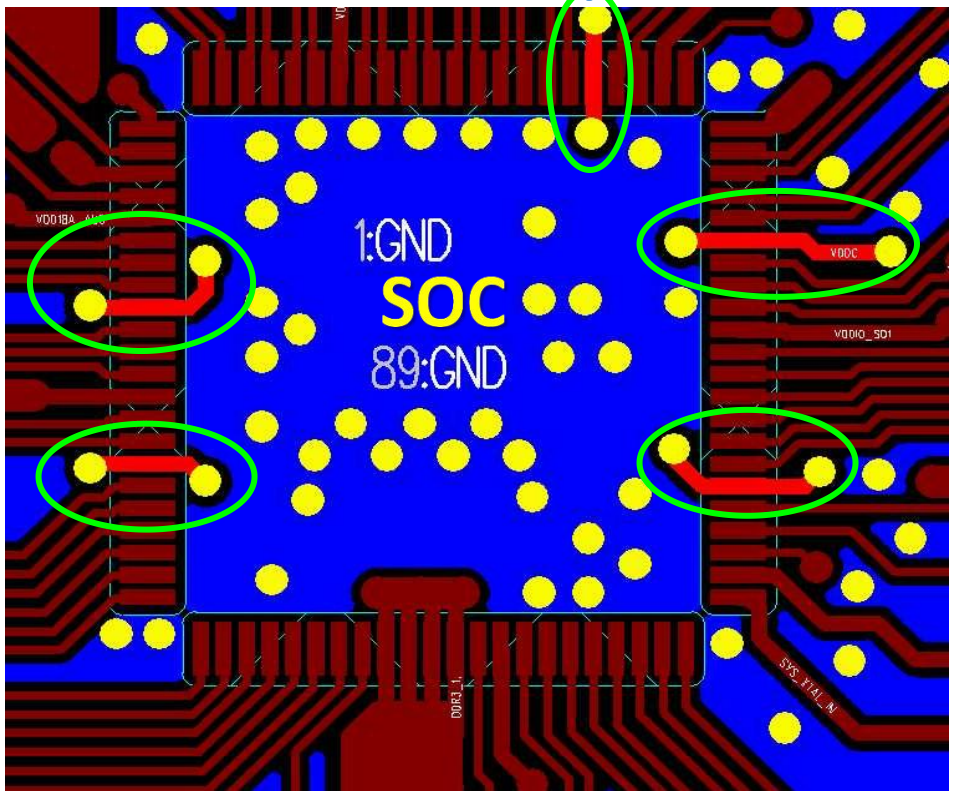
模拟/数字电源绕线

QFN PKG: CV181xC
4-layer/6-layer PCB

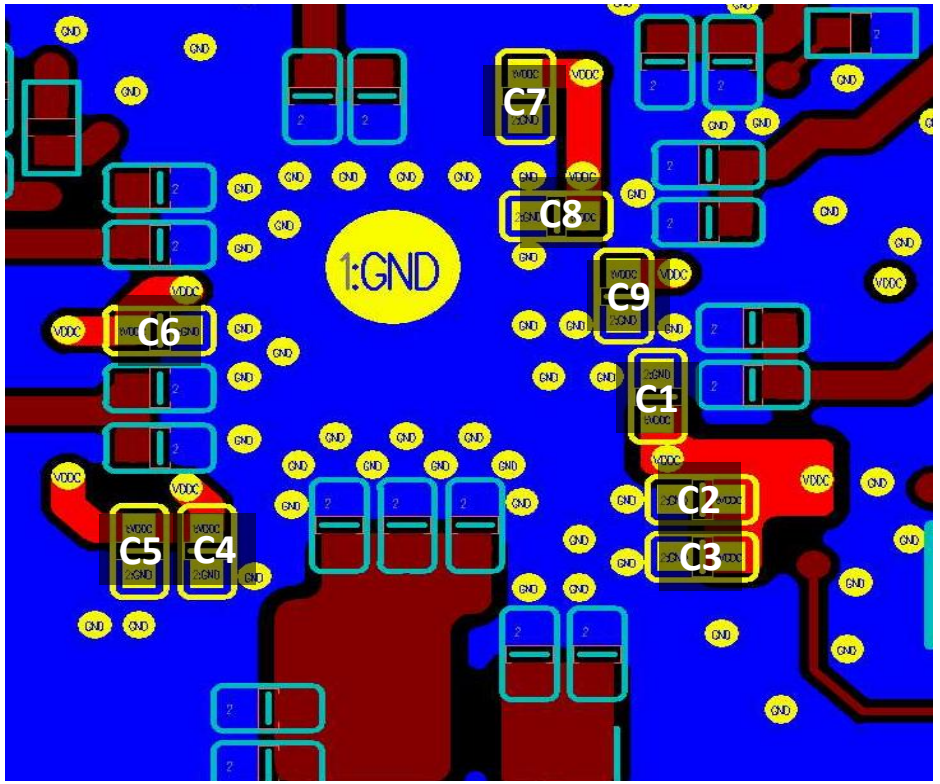
QFN – 4L/6L-PCB – VDDC – Rule 1

Power	Layer	SOC VIA count	DeCap	Layout rule
VDDC	Top/Bottom	10	(1) 0402 0.1uF: C1/C2/C6/C8/ (2) 0402 1uF: C3/C4/C9 (3) 0402 4.7uF: C5/C7	(1) VDDC VIA rule 1) 每根VDDC pin 需连接两颗VIA 2) 确认每颗Cap旁至少1颗VDDC via (2) GND VIA rule 确认每颗Cap旁至少1颗GND via

VDDC@Top



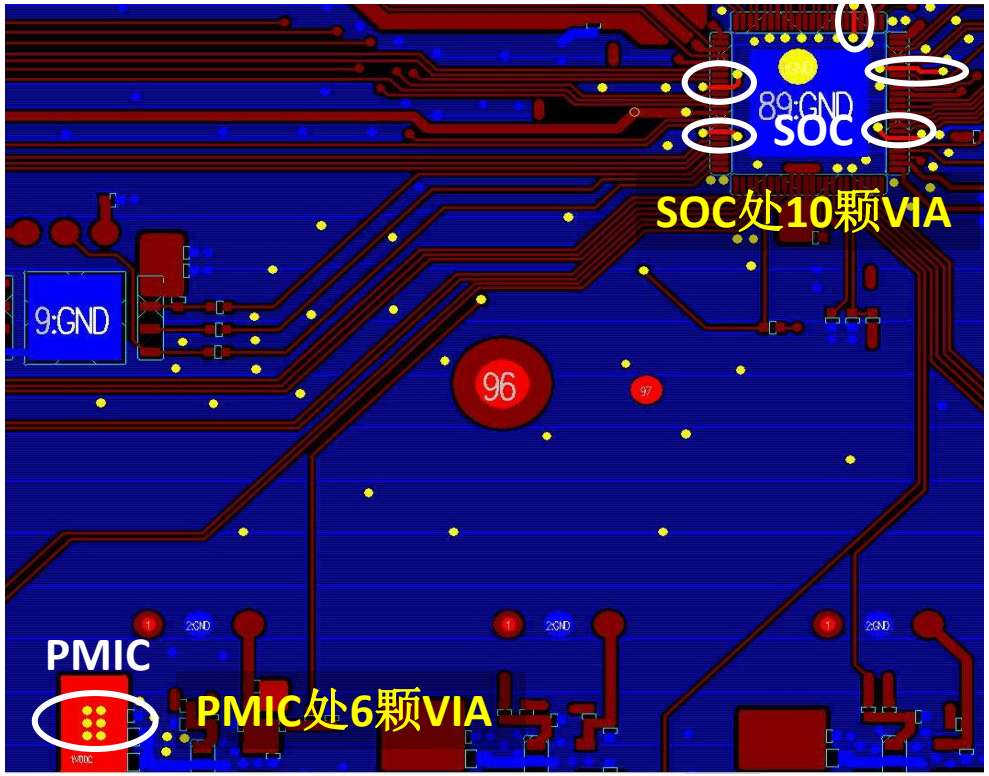
VDDC@Bottom



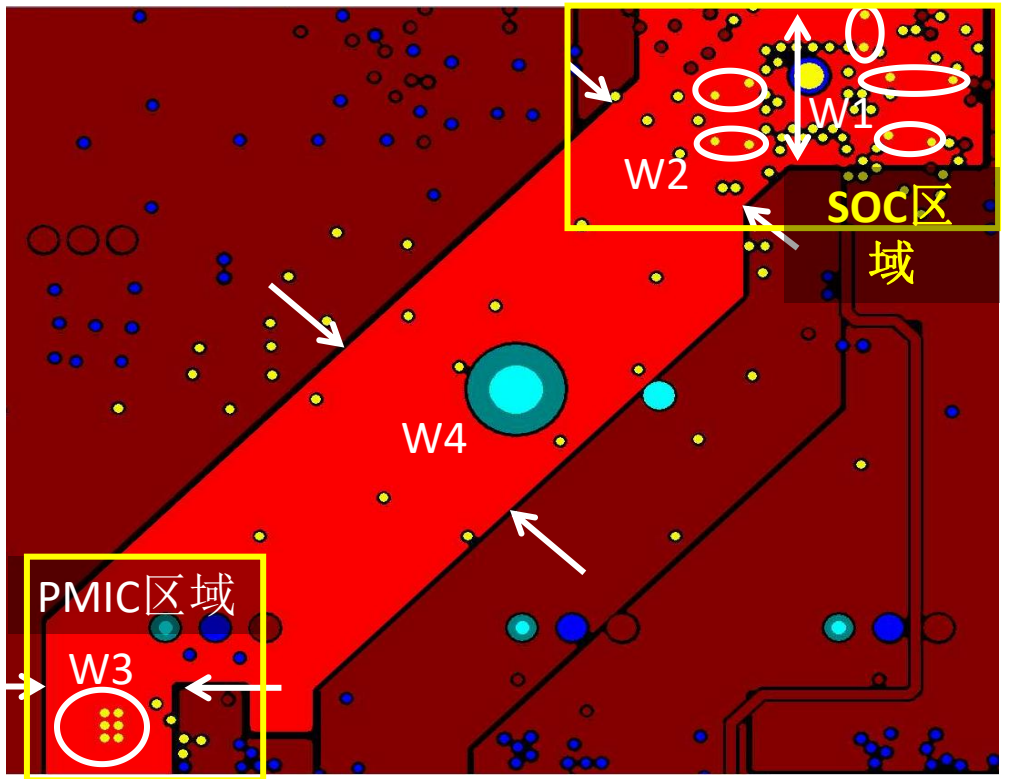
QFN – 4L/6L-PCB – VDDC – Rule 2

Power	Layer	Layout rule
VDDC	VDDC main routing, 4L-PCB: DDR3_1.5V@L3 6L-PCB: DDR3_1.5V@L4	DDR3_1.5V 内层绕线: (1) 确认SOC处10颗VIA, PMIC处6颗VIA (2) **SOC区域扣除破孔有效宽度: W1>=4mm (SOC QFN正下方),** W2>=1.5mm (进入SOC 区域) (3) PMIC区域扣除破孔有效宽度: W3>=1.5mm (4) Main route 扣除破孔有效宽度 : W4>=1.5mm

VDDC@Top



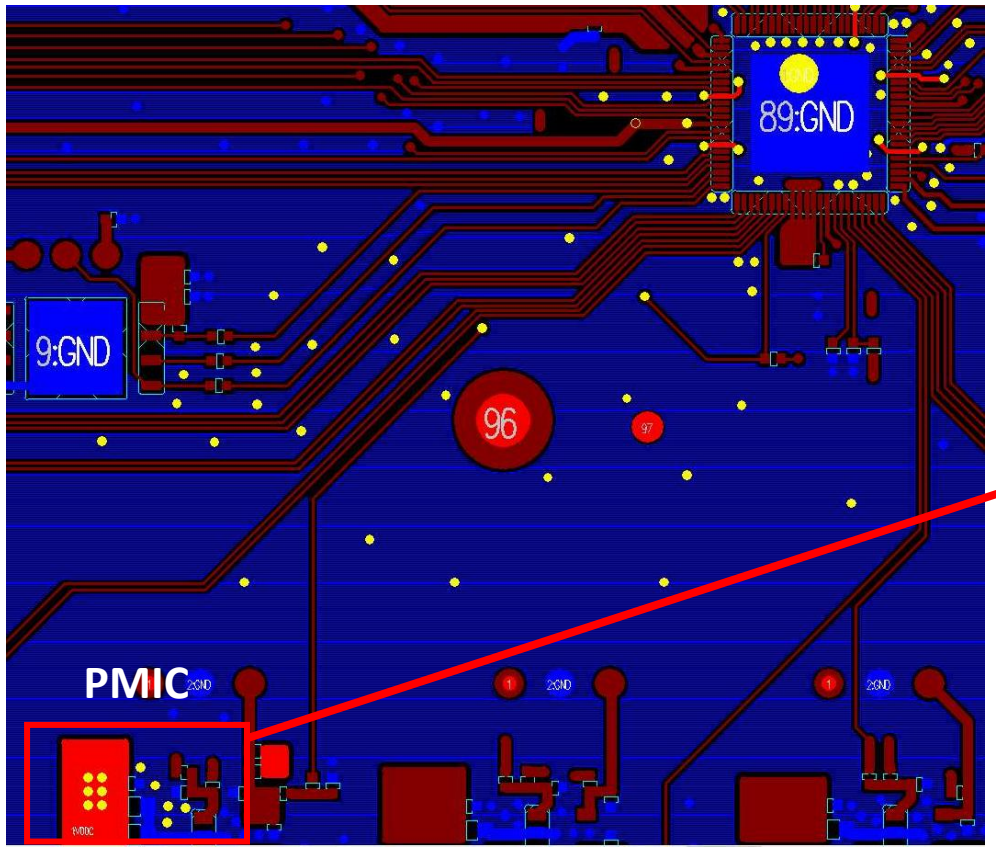
4L-PCB: VDDC@L3
6L-PCB: VDDC@L4



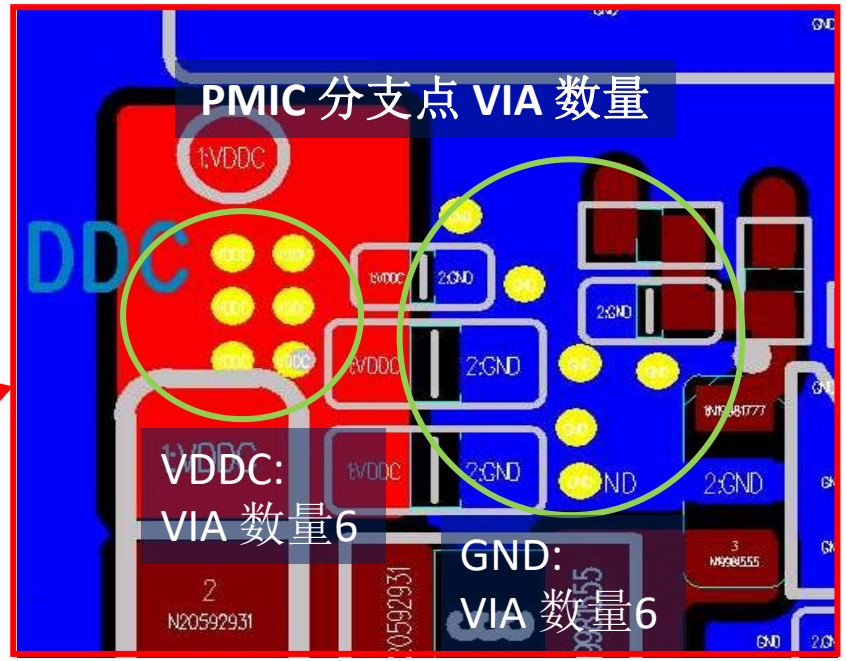
QFN – 4L/6L-PCB – VDDC – Rule 3

Power	PMIC 分支点 VIA 数量
VDDC	(1) VDDC: VIA 数量>=6 (2) GND: VIA 数量>=5

VDDC@Top



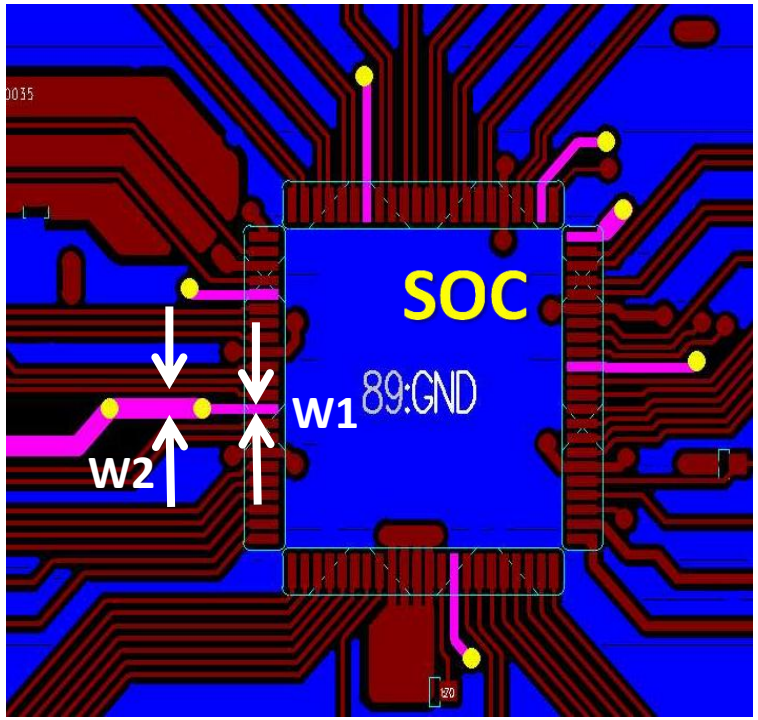
PMIC routing area



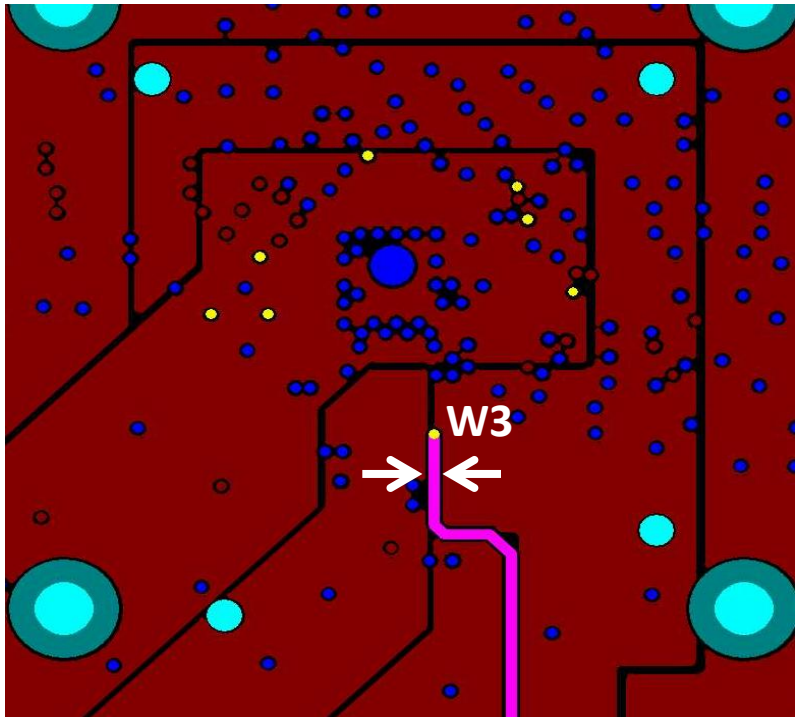
QFN – 4L/6L-PCB – Analog IO Power – Rule 1

Power	Layer	Layout rule
VDD18A_AUD/VDD_18A_MIPI **VDD18A_USB_PLL_ETH** **VDD33A_EPH_USB** **VDDIO_RTC** **VDDIO_SD0_A/VDDIO_SD1**	4L-PCB: Top/Bottom/L3 6L-PCB: Top/Bottom/L4	@Top: (1) Break out (fan-out):线宽 W1>=0.25mm (2) Main route:线宽 W2>=0.5mm @内层：所有线宽 W3>=0.5mm @Bottom:所有线宽 W4>=0.5mm

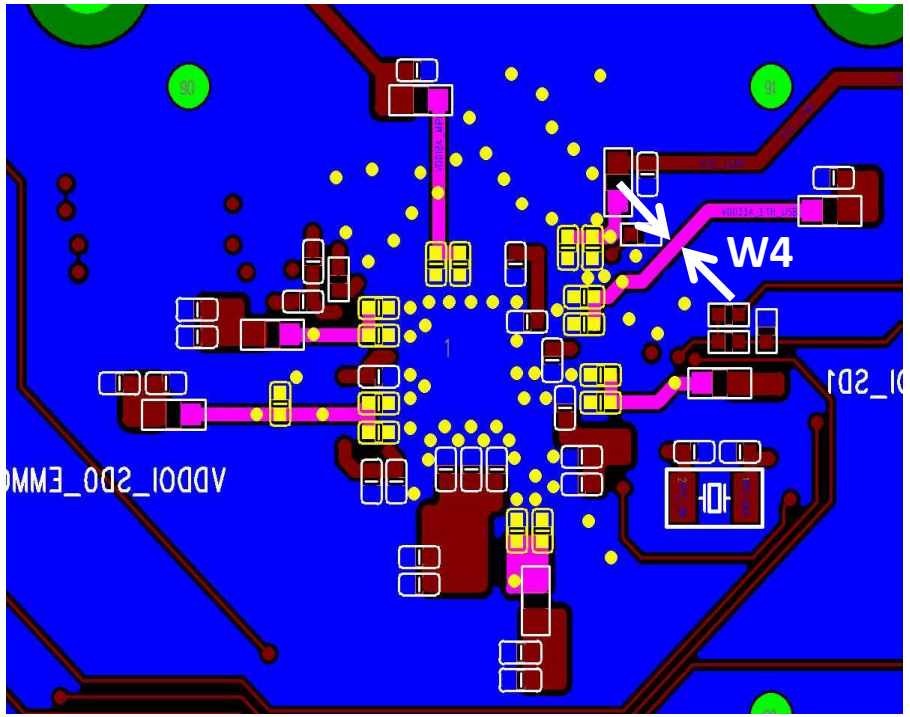
Analog IO power@Top



Analog IO power@内层



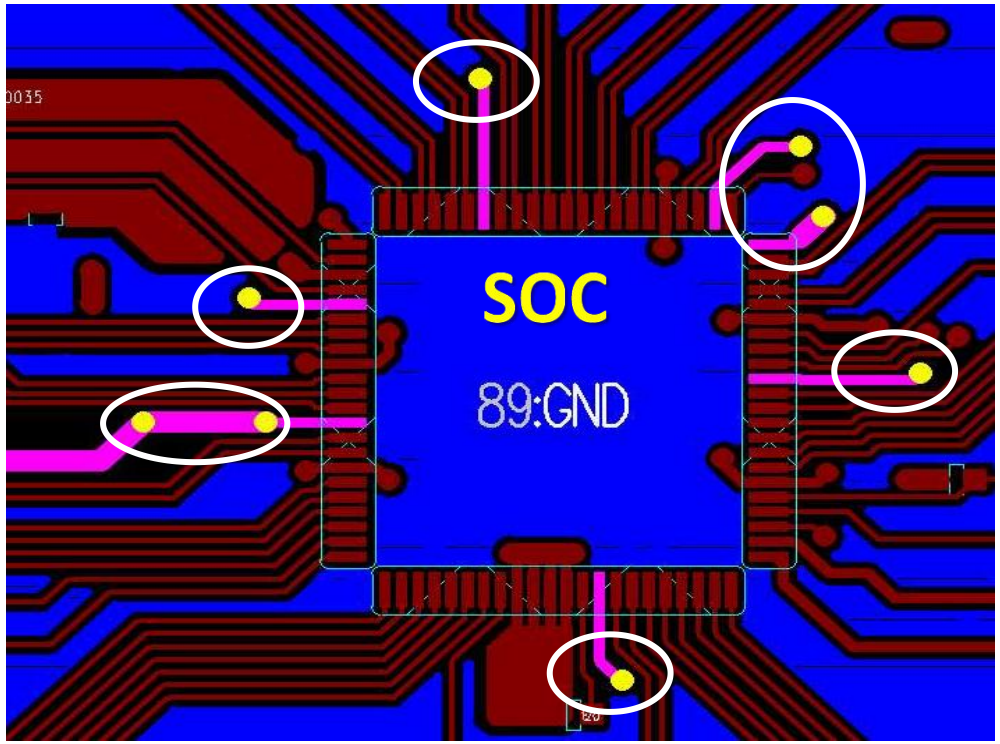
Analog IO power@Bottom



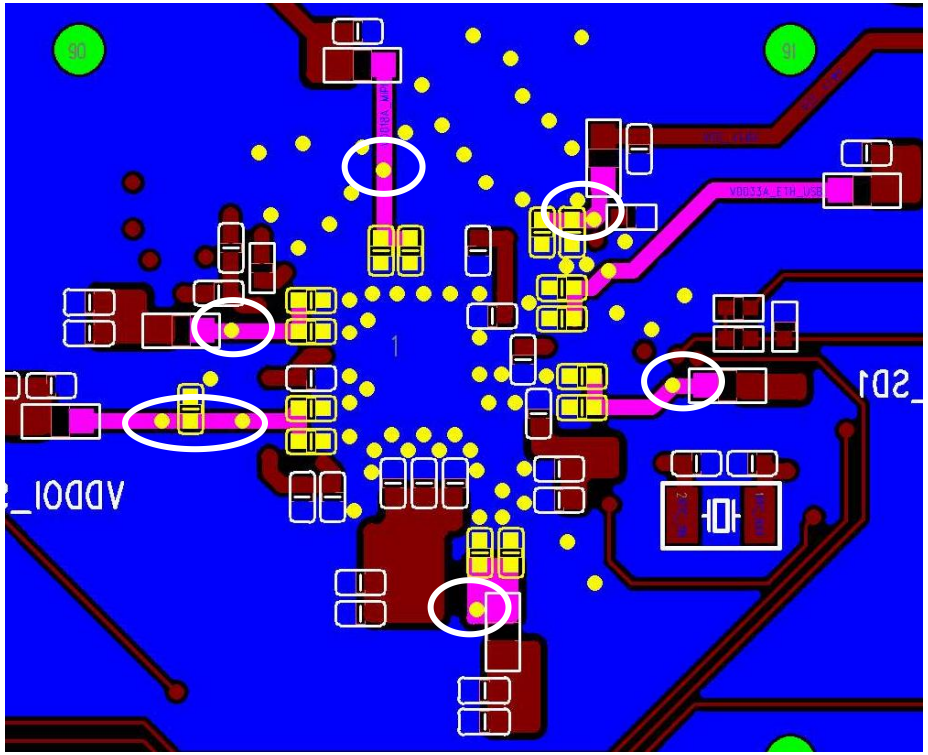
QFN – 4L/6L-PCB – Analog IO Power – Rule 2

Power	Layer	Layout rule
VDD18A_AUD/VDD_18A_MIPI **VDD18A_USB_PLL_ETH** **VDD33A_EPH_USB** **VDDIO_RTC** **VDDIO_SD0_A/VDDIO_SD1**	Top/Bottom	(1) Analog IO power VIA rule 确认每颗Cap旁至少1颗analog IO power via (2) GND VIA rule 确认每颗Cap旁至少1颗GND via

Analog IO power@Top



Analog IO power@Bottom



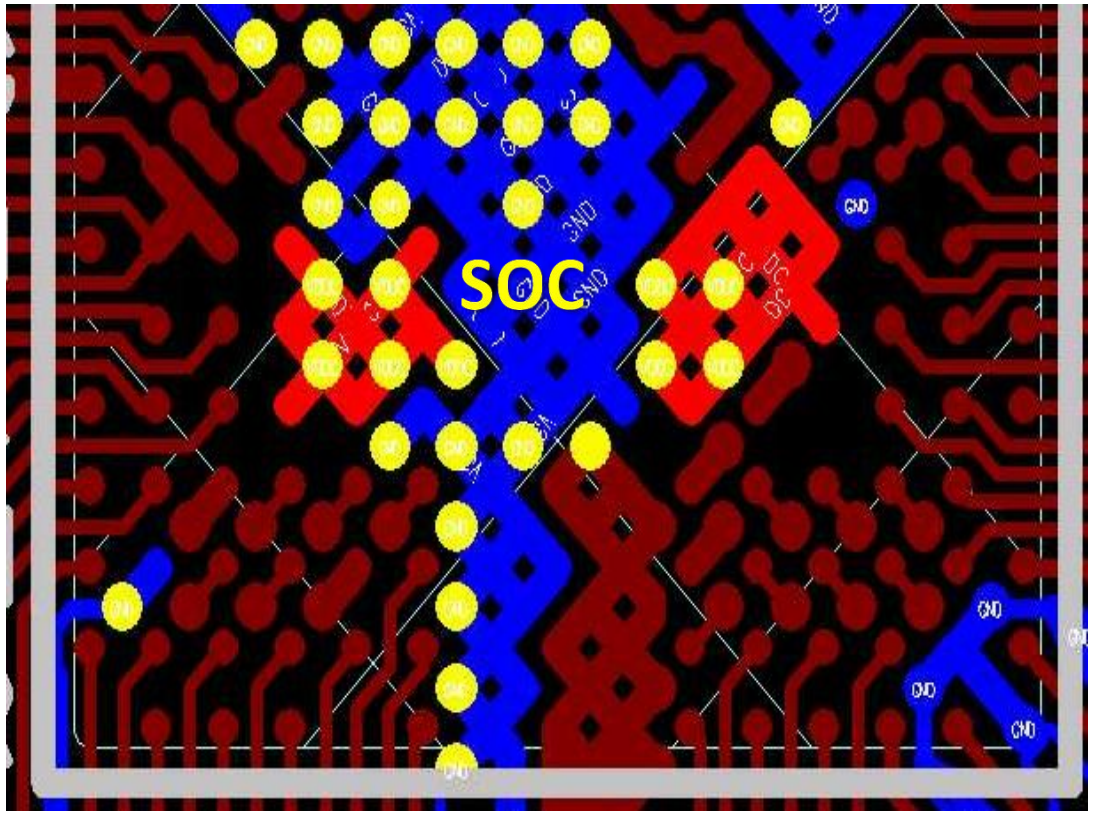
模拟/数字电源绕线

BGA PKG: CV181xH
4-layer/6-layer PCB

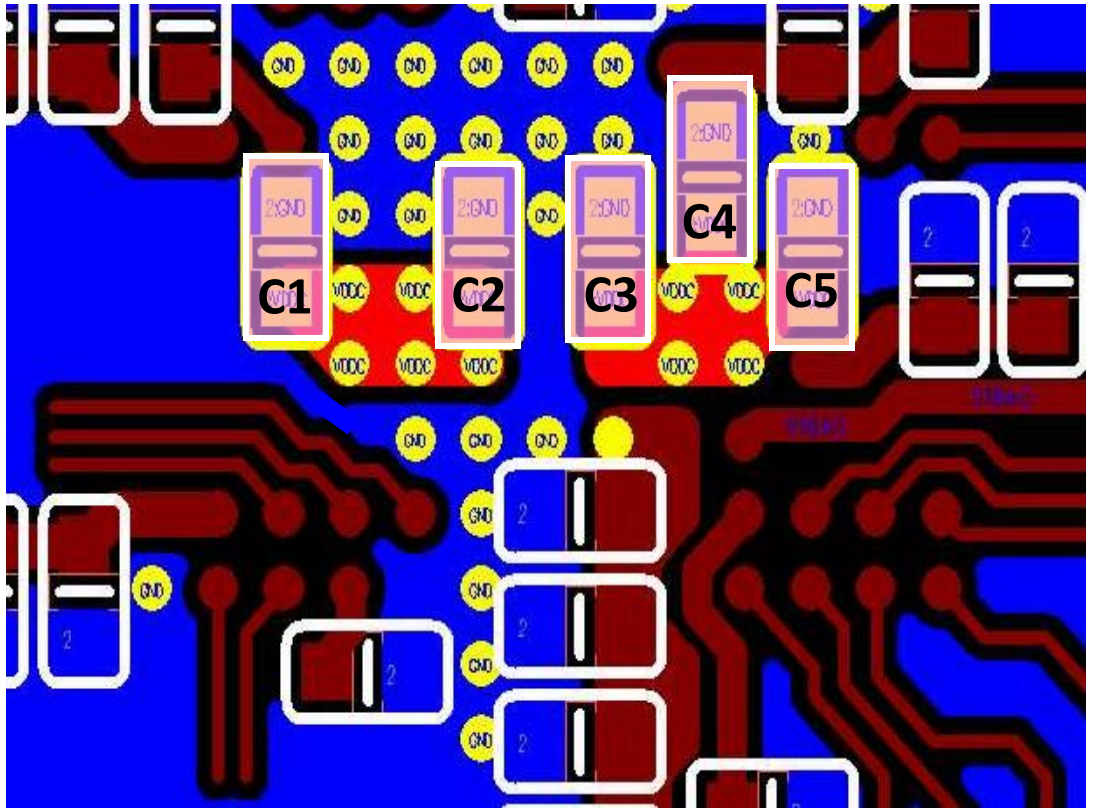
BGA – 4L/6L-PCB – VDDC – Rule 1

Power	Layer	SOC VIA count	DeCap	Layout rule
VDDC	Top/Bottom	9	(1) 0402 0.1uF: C1 (2) 0402 1uF: C3/C4/C5 (3) 0402 4.7uF: C2	(1) VDDC VIA rule 确认VDDC via紧连CAP (2) GND VIA rule 确认GND via紧连CAP

VDDC@Top



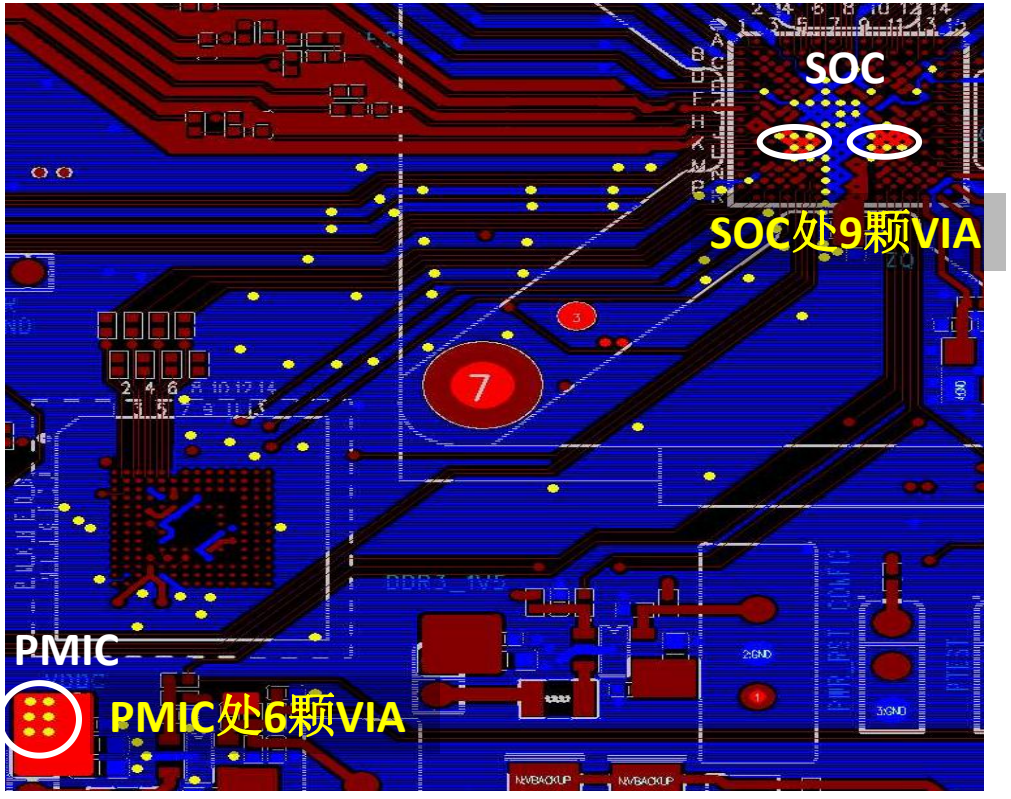
VDDC@Bottom



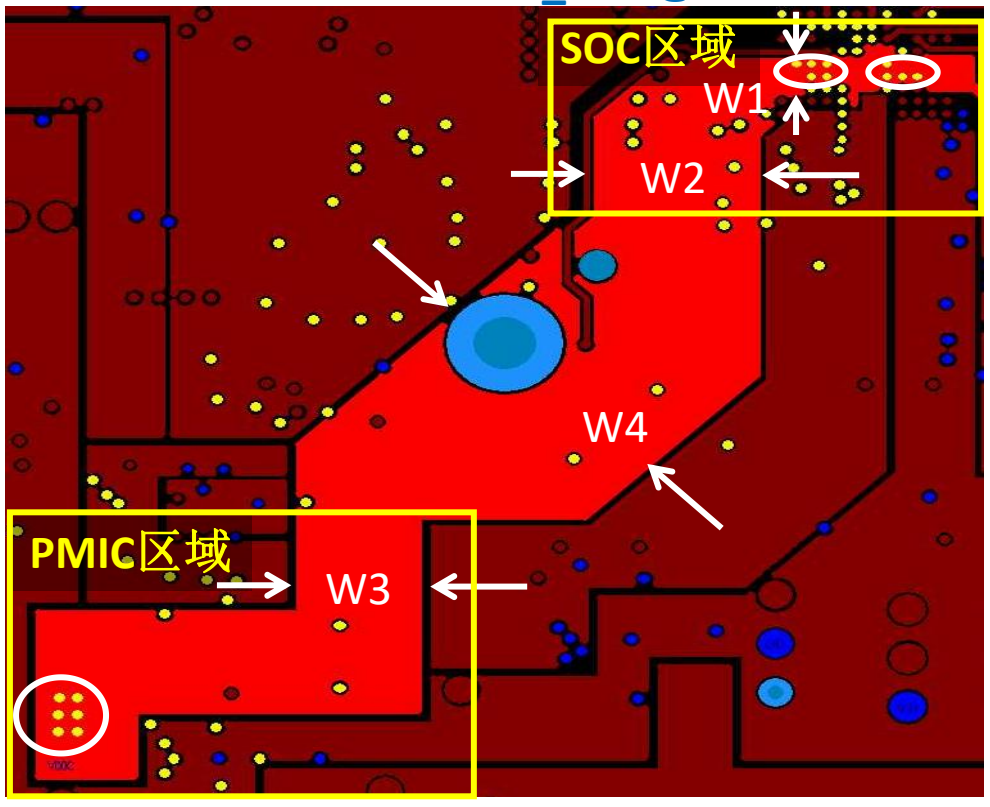
BGA – 4L/6L-PCB – VDDC – Rule 2

Power	Layer	Layout rule
VDDC	VDDC main routing, 4L-PCB: DDR3_1.5V@L3 6L-PCB: DDR3_1.5V@L4	DDR3_1.5V 内层绕线; (1) 确认SOC处9颗VIA, PMIC处6颗VIA (2) **SOC区域,扣除破孔有效宽度: W1>=1mm (SOC ball 正下方),** W2>=1.5mm (进入SOC 区域) (3) PMIC区域, 扣除破孔有效宽度: W3>=1.5mm (4) Main route, , 扣除破孔有效宽度: W4>=1.5mm

DDR3_1.5V@Top



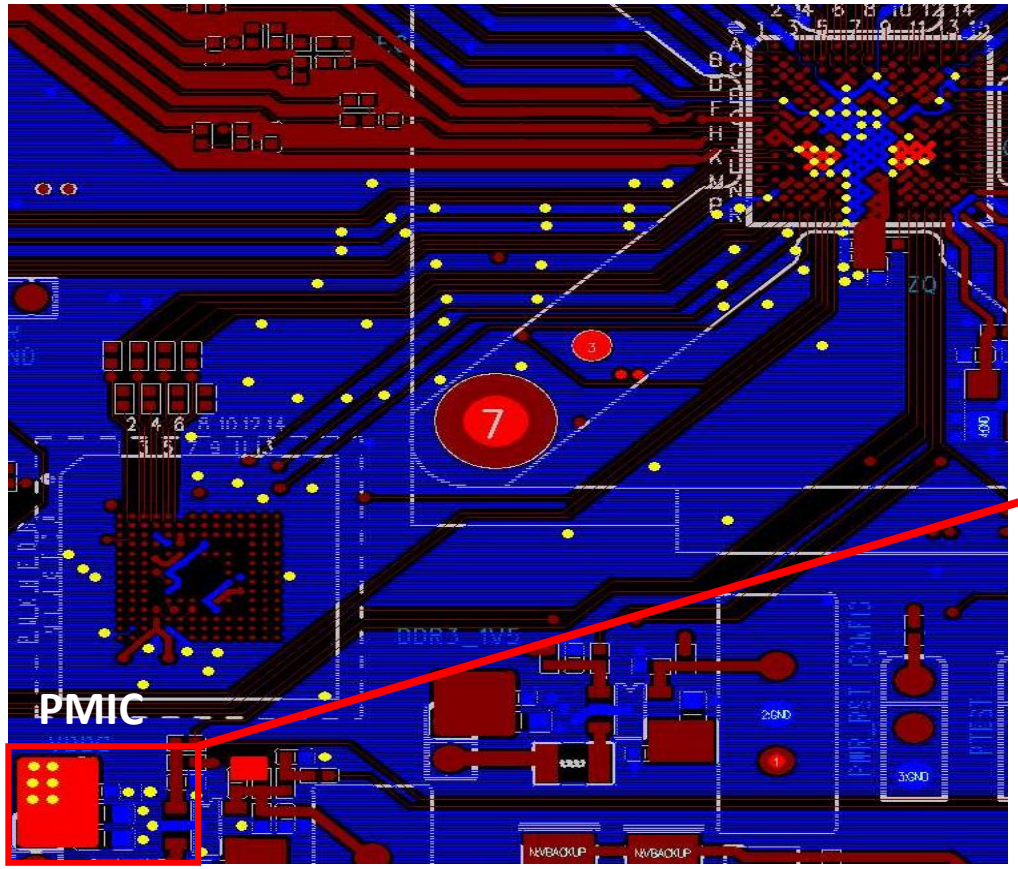
4L-PCB: DDR3_1.5V@L3
6L-PCB: DDR3_1.5V@L4



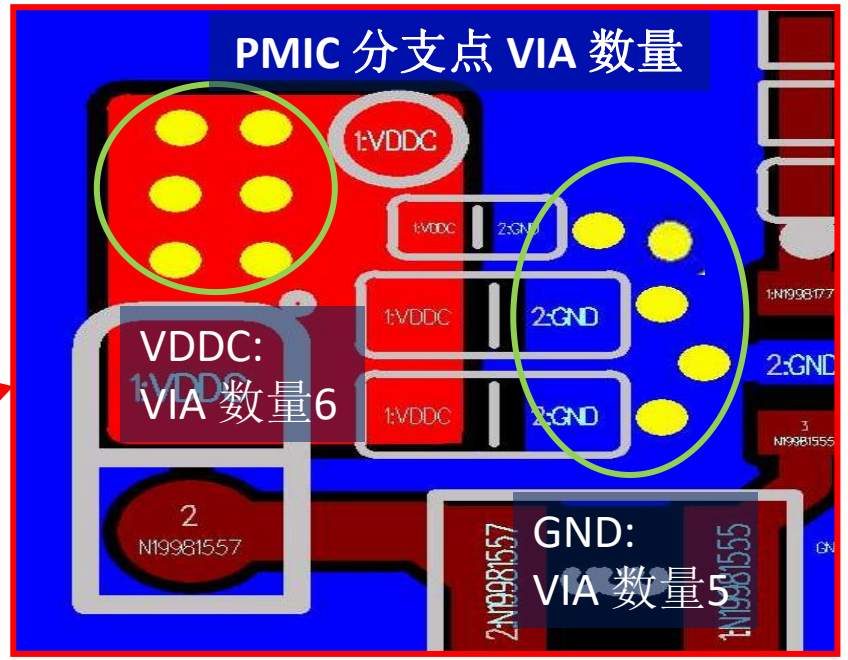
BGA – 4L/6L-PCB – VDDC – Rule 3

Power	PMIC 分支点 VIA 数量
VDDC	(1) VDDC: VIA 数量>=6 (2) GND: VIA 数量>=5

DDR3_1.5V@Top



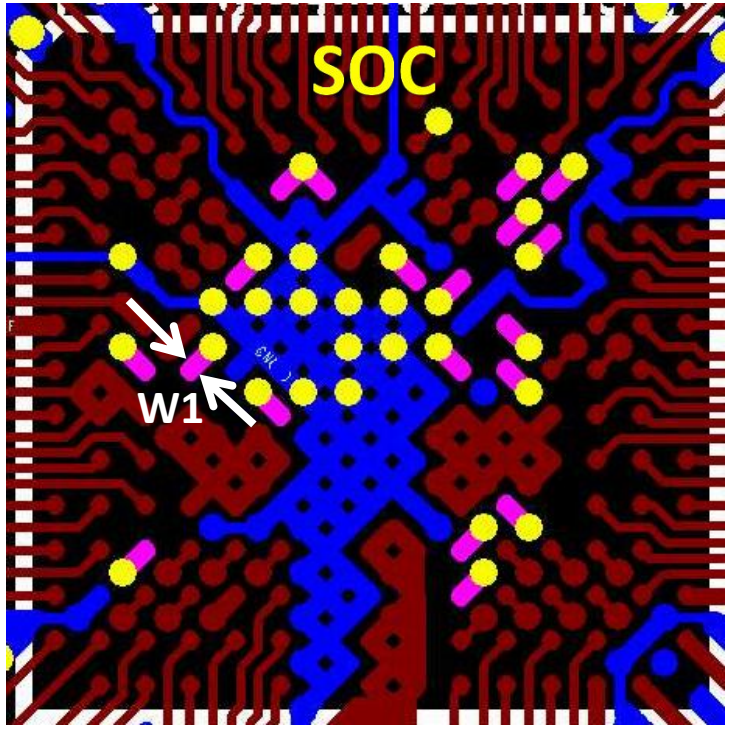
PMIC routing area



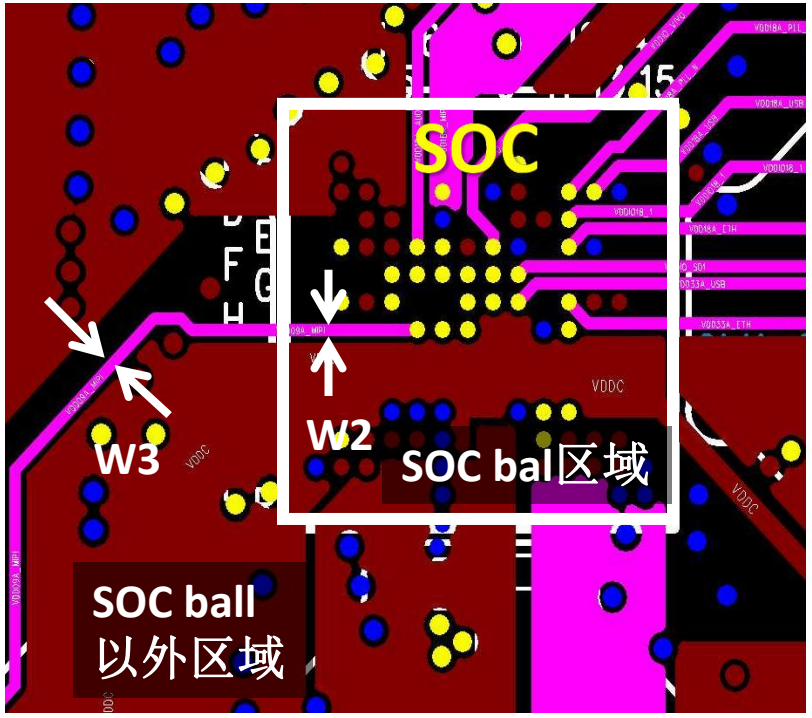
BGA – 4L/6L-PCB – Analog IO Power – Rule 1

Power	Layer	Layout rule
VDDIO_18A/VDDIO18_1 VDD18A_AUD/VDD18A_ETH/VDD_18A_MIPI VDD18A_PLL_N/VDD18A_USB VDD33A_EPHY/VDD33A_ETH VDDIO_EMMC/VDDIO_RTC/VDDIO_VIVO VDDIO_SD0/VDDIO_SD0_A/VDDIO_SD1 VDD09A_EPHY/VDD09A_MIPI VIN3V	4L-PCB: Top/Bottom/L3 6L-PCB: Top/Bottom/L4	@Top: 线宽 W1>=0.3mm (ball与VIA最短距离连线) @内层 : (1) SOC ball 区域: 线宽 W2>=0.3mm (2) SOC ball 以外区域: 线宽 W3>0.5mm @Bottom: (1) SOC ball 区域: 线宽 W4>=0.3mm (2) SOC ball 以外区域: 线宽 W5>0.5mm

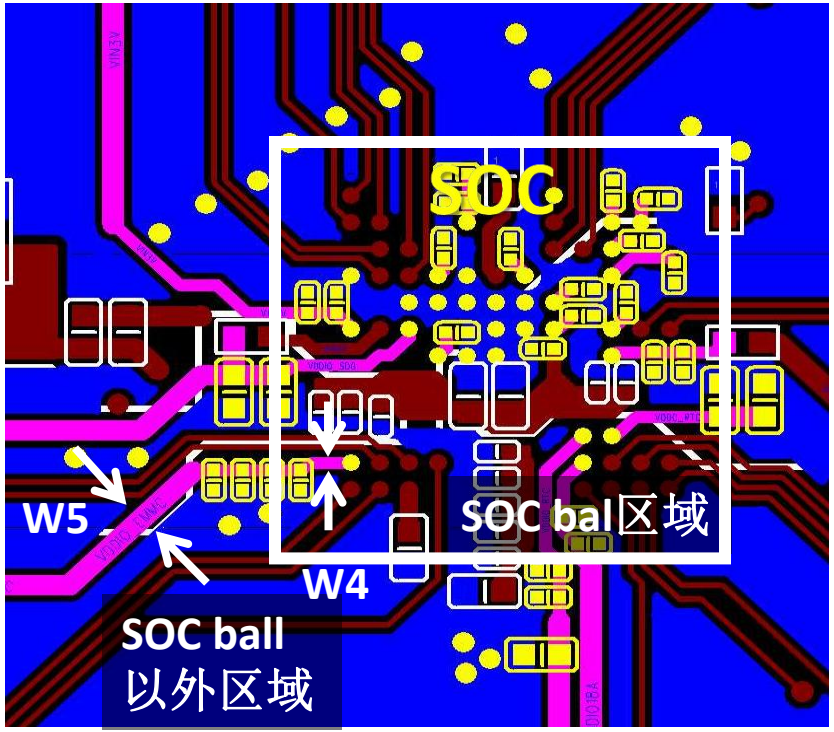
Analog IO power@Top



Analog IO power@内层



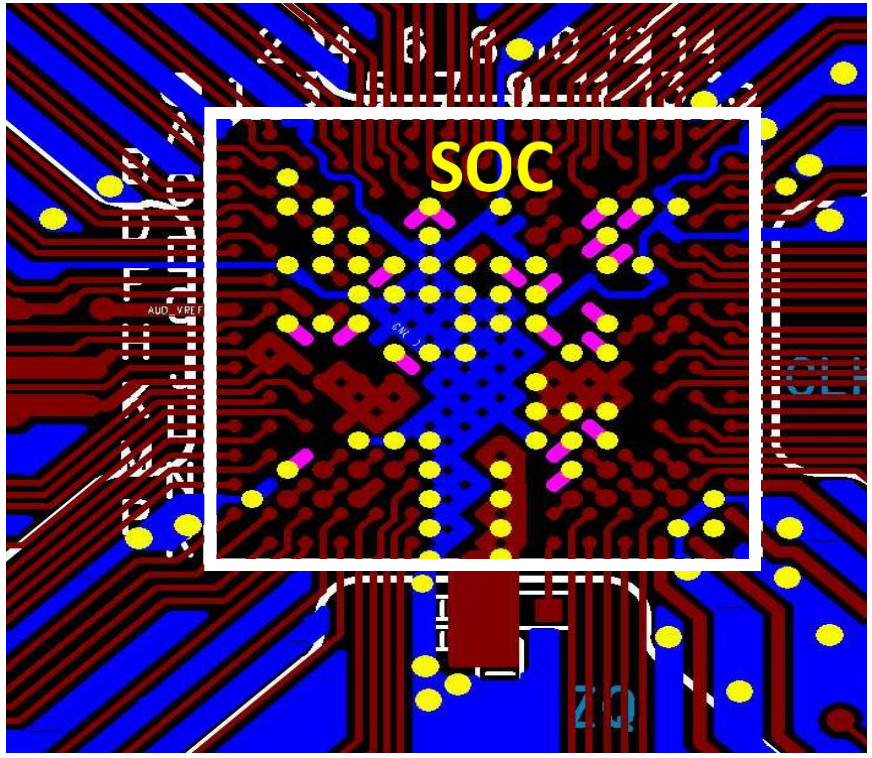
Analog IO power@Bottom



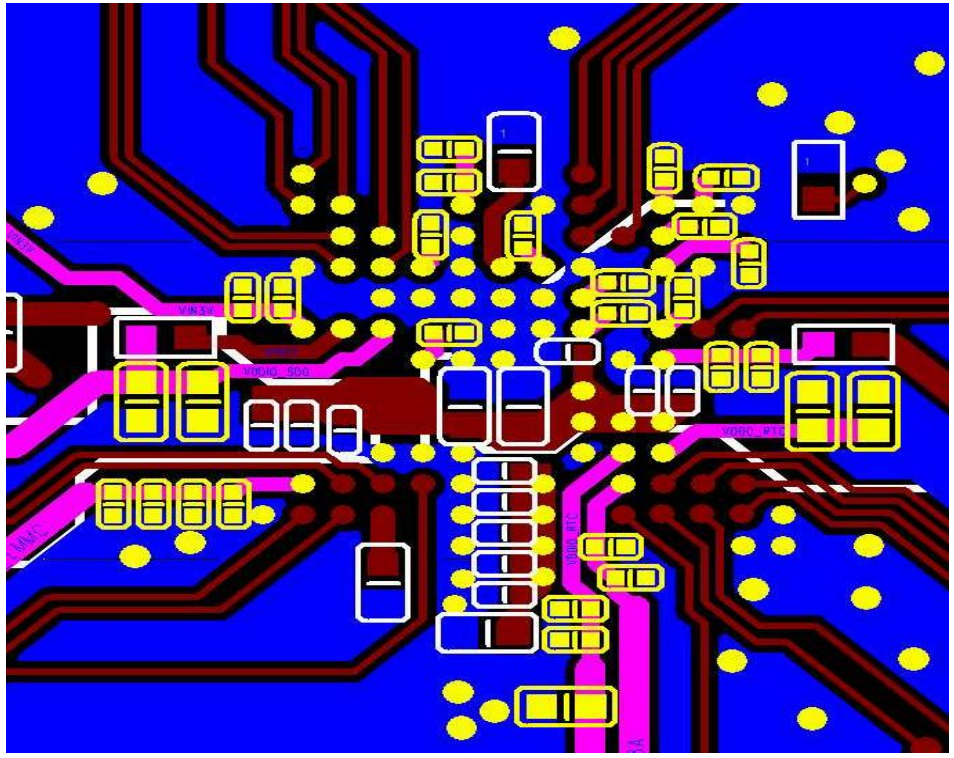
BGA – 4L/6L-PCB – Analog IO Power – Rule 2

Power	Layer	Layout rule
VDDIO_18A/VDDIO18_1 **VDD18A_AUD/VDD18A_ETH/VDD_18A_MIPI** **VDD18A_PLL_N/VDD18A_USB** **VDD33A_EPHY/VDD33A_ETH** **VDDIO_EMMC/VDDIO_RTC/VDDIO_VIVO** **VDDIO_SD0/VDDIO_SD0_A/VDDIO_SD1** **VDD09A_EPHY/VDD09A_MIPI** **VIN3V**	Top/Bottom	(1) Analog IO power VIA rule 确认每颗Cap旁至少1颗analog IO power via (2) GND VIA rule 确认每颗Cap旁至少1颗GND via

Analog IO power@Top



Analog IO power@Bottom



Appendix

MIPI/EPHY/USB/Antenna 阻抗控制

4-layer PCB

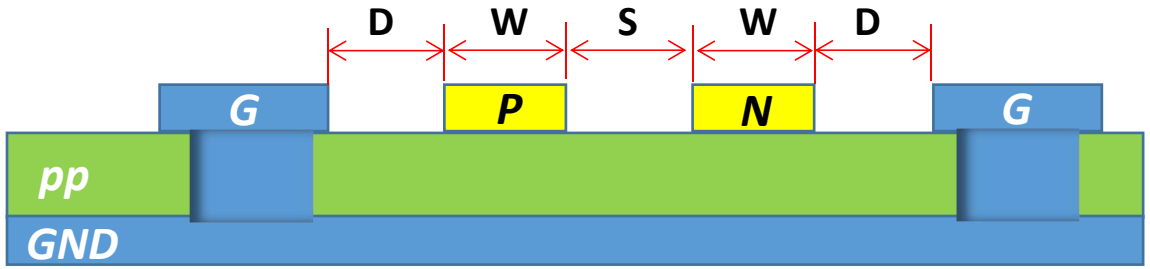
MIPI/EPHY/USB 阻抗控制 –表层走线 Option1

Layer	Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
Top/Bottom	100	5	5	6	97.99
	90	5	4	6	92.48

Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

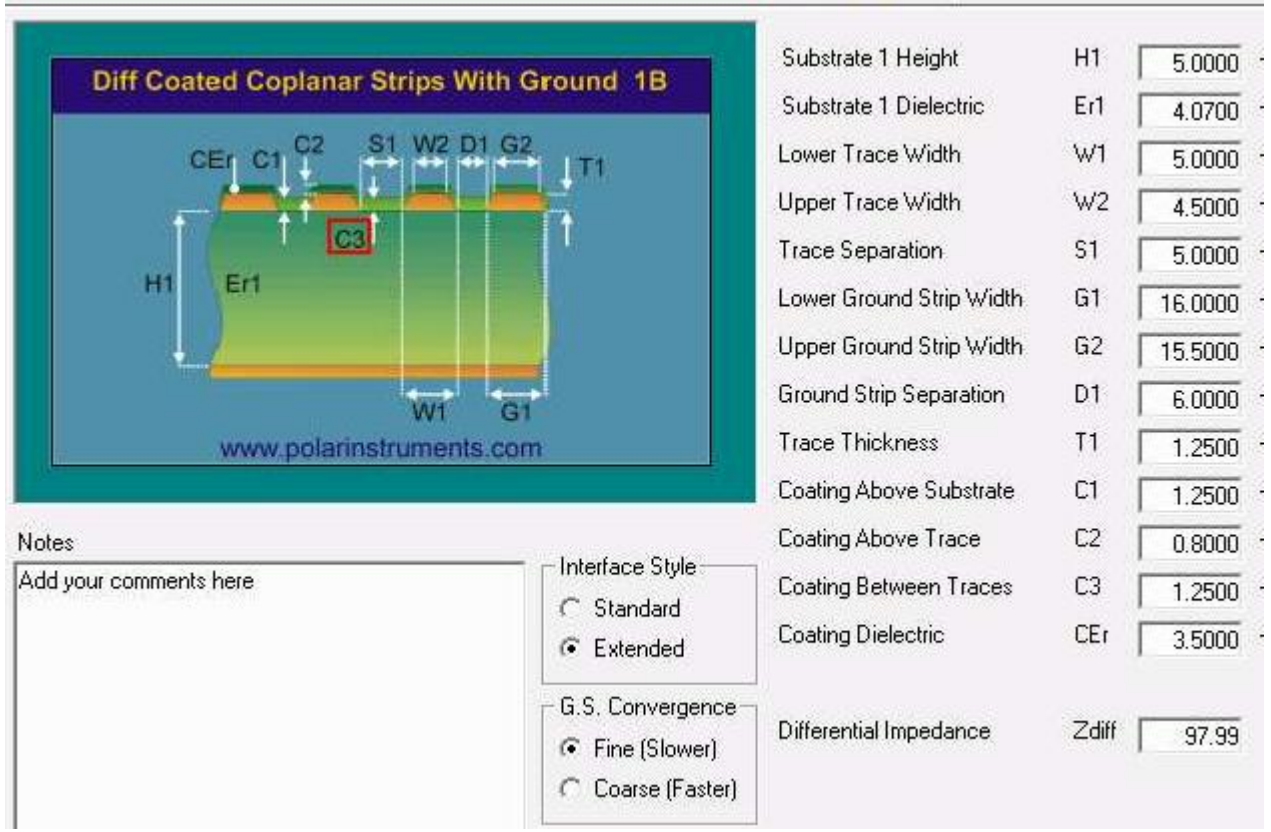
- MIPI/USB differential signals are required impedance control
  - Target impedance:
  (1) MIPI- CSI/DSI: 100ohm
  (2)USB: 90ohm

- Differential signals shielding rule:
  - pair to pair GND shielding

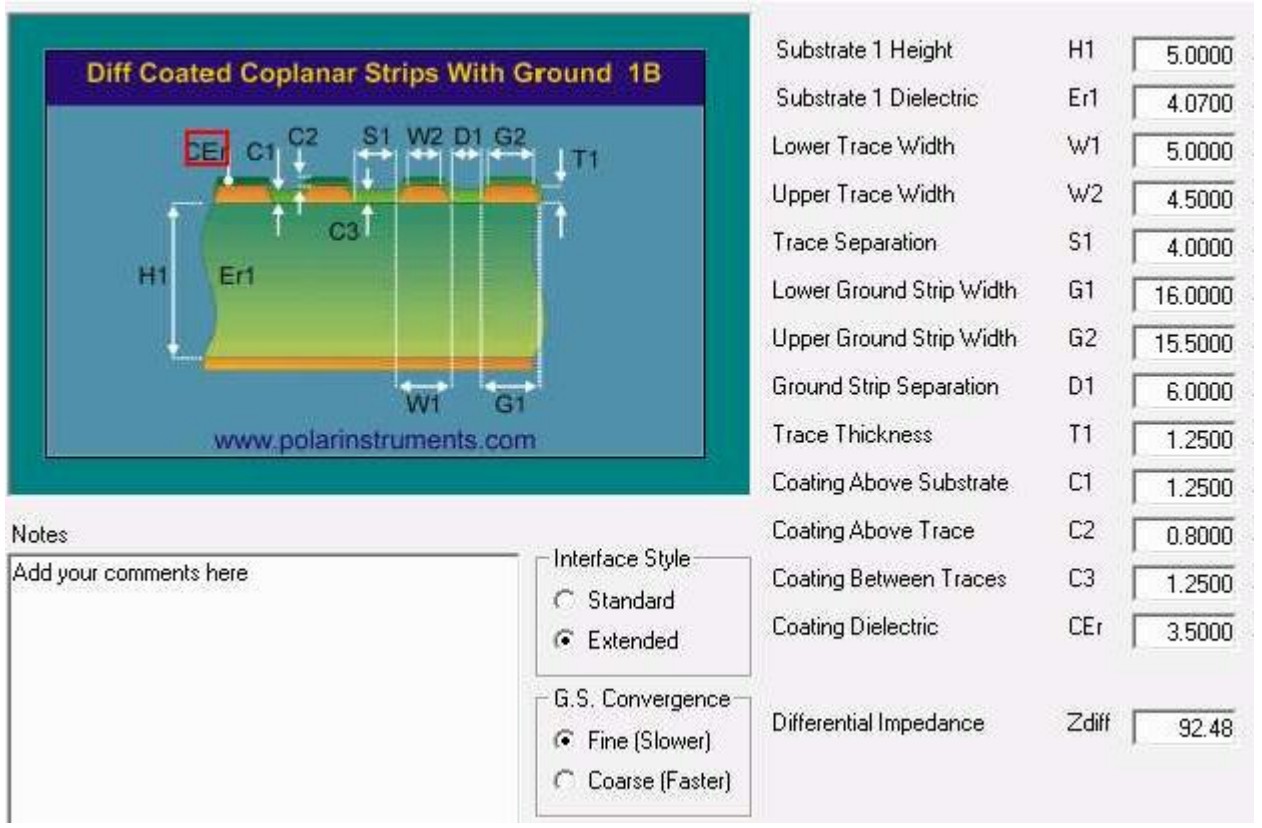


MIPI/EPHY/USB 阻抗控制 –表层走线 Option1

Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
100 +/- 5%	5	5	6	97.99



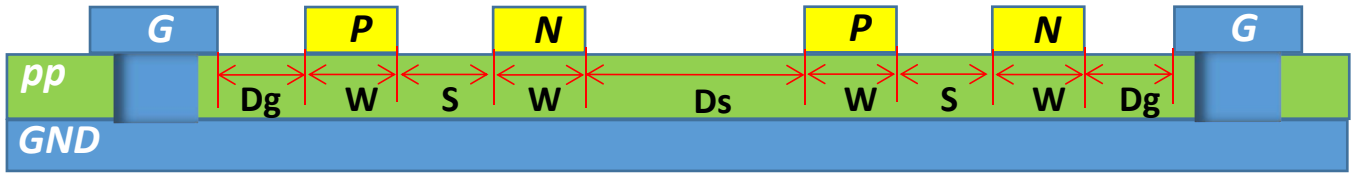
Target Z	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
90 +/- 5%	5	4	6	92.48



MIPI 阻抗控制 – 表层走线 Option2

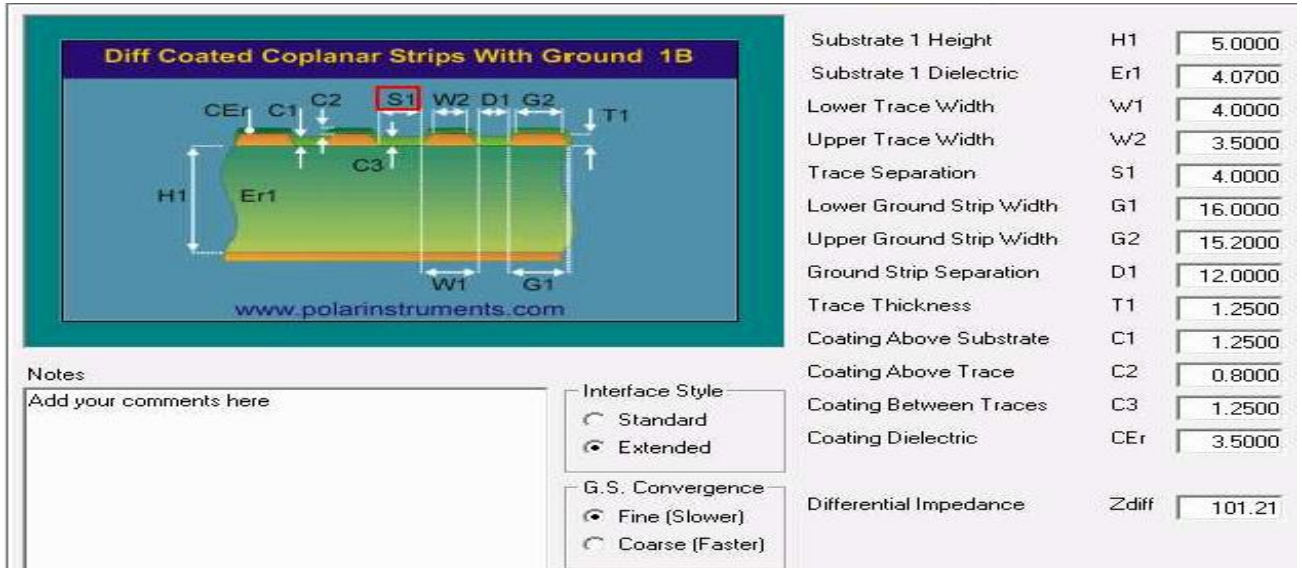
Layer	Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)	Rule
Top/Bottom	100	5	5	12	12	99.96	Ds=3W, Dg=3W

Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

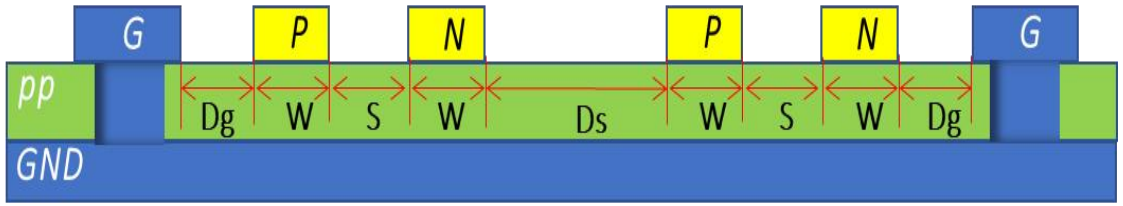


MIPI 阻抗控制 – 表层走线 Option2

Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
100 +/- 5%	5	5	12	12	99.96
	4	4	12	12	101.21



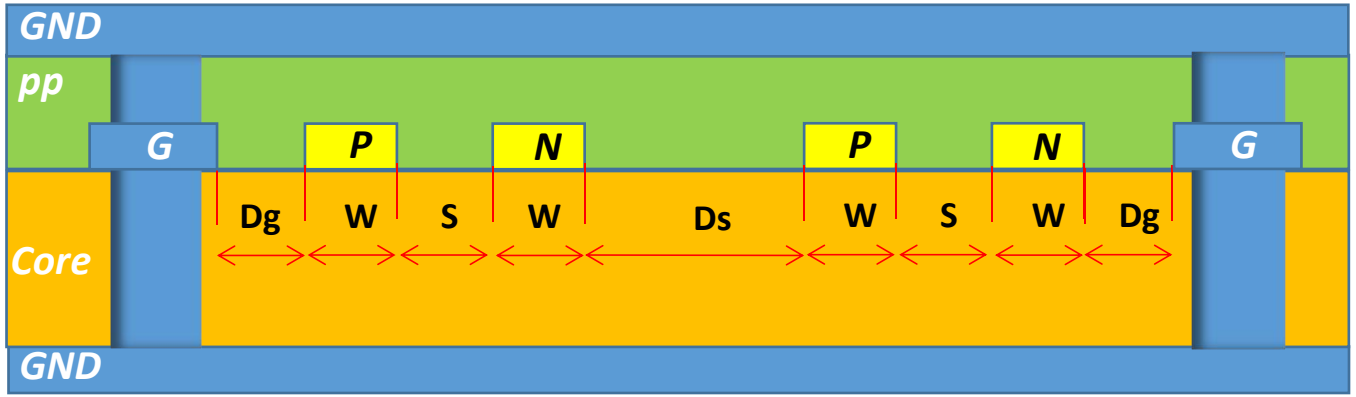
Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	



MIPI 阻抗控制 – 内层走线

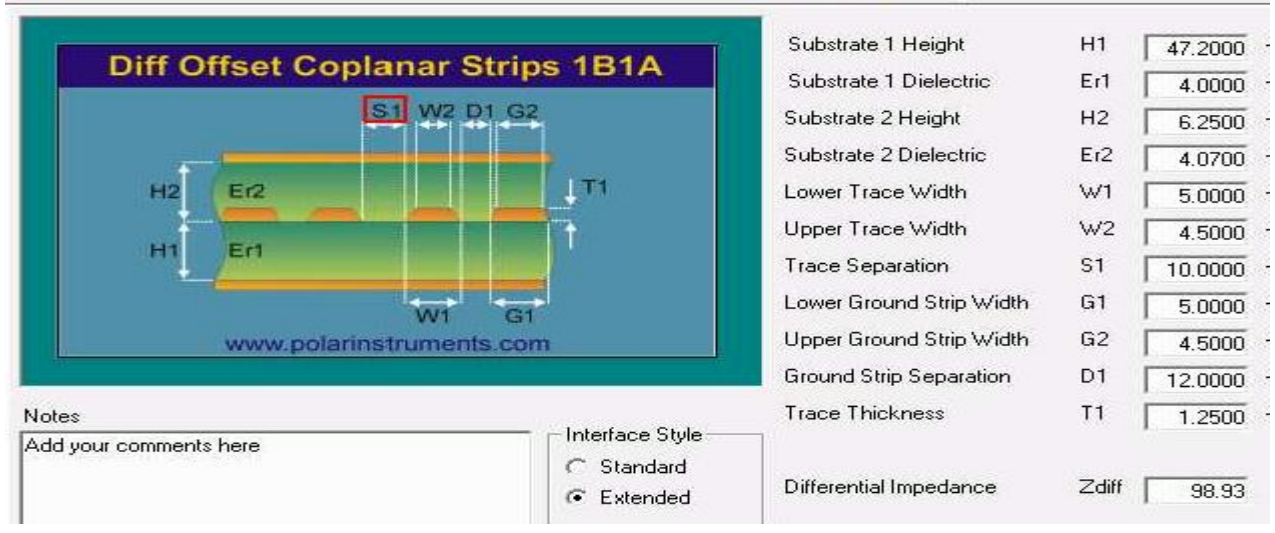
Layer	Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
L2/L3	100	5	10	12	12	98.93

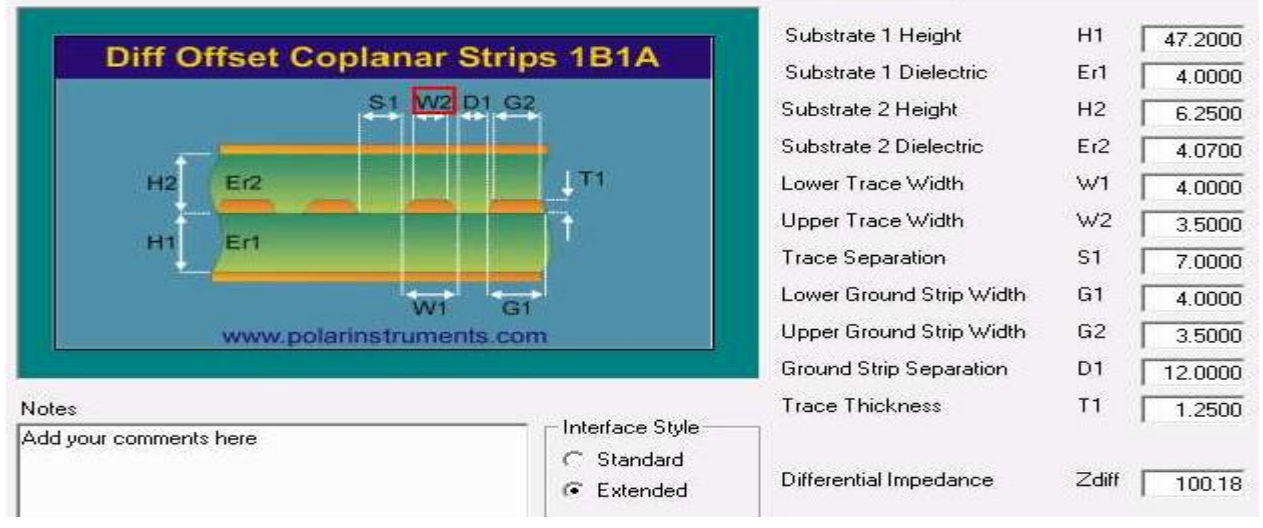
Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	



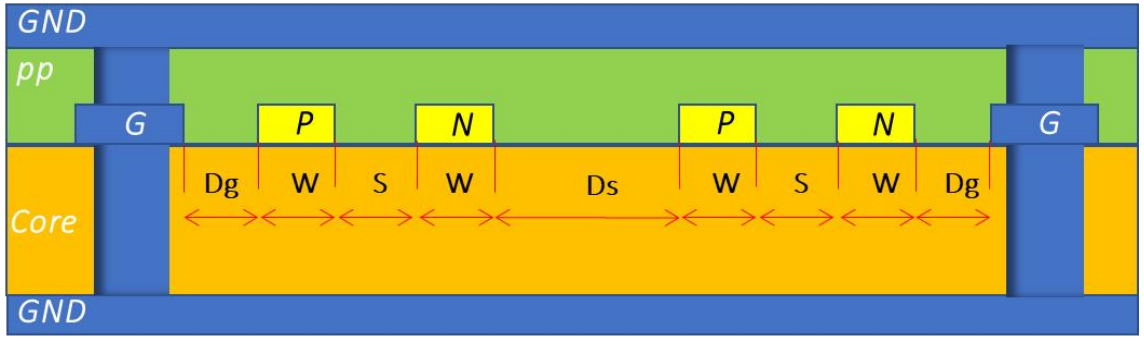
MIPI 阻抗控制 – 内层走线

Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
100 +/- 5%	5	10	12	12	98.93
	4	7	12	12	100.18





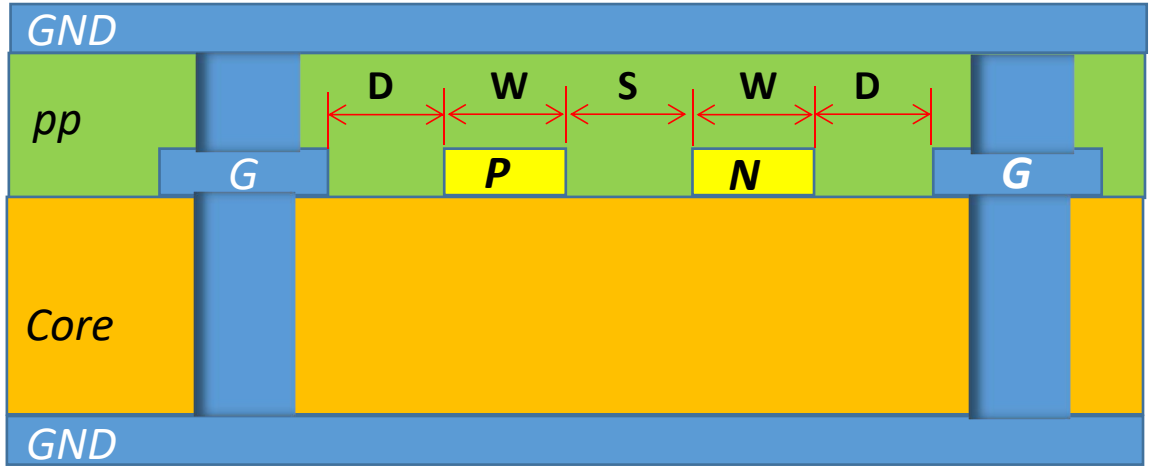
Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	



EPHY/USB 阻抗控制 – 内层走线

Layer	Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
L2/L3	100	5	10	12	98.92
	90	5	7	6	90.33

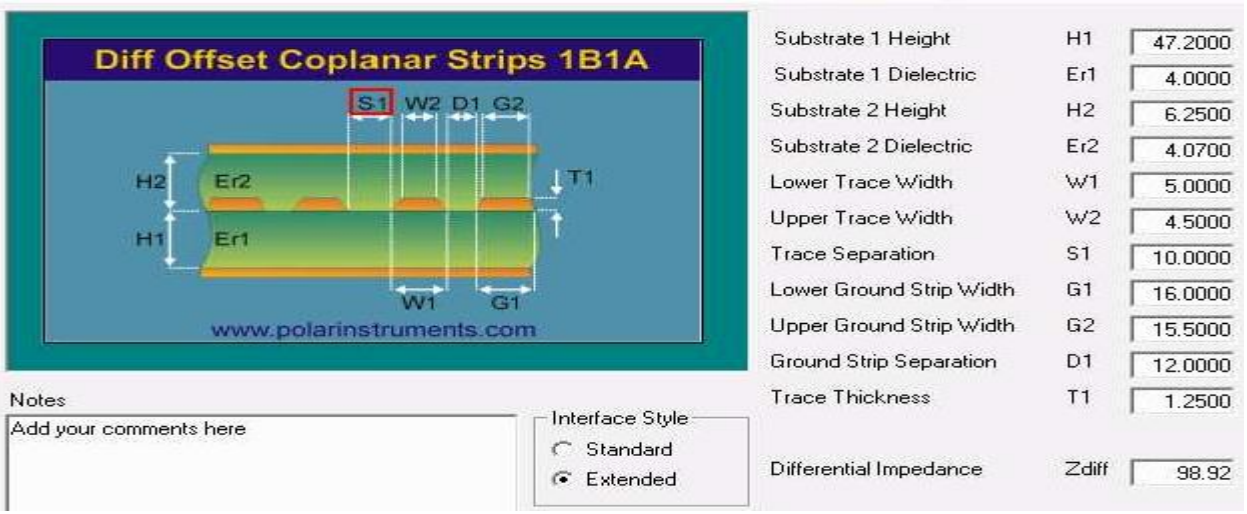
Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

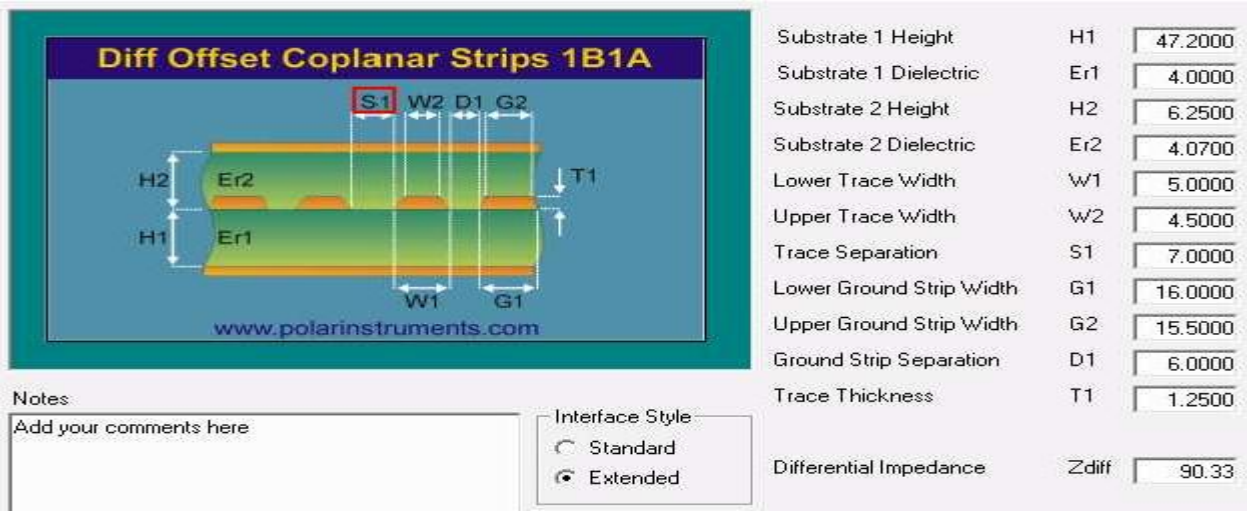


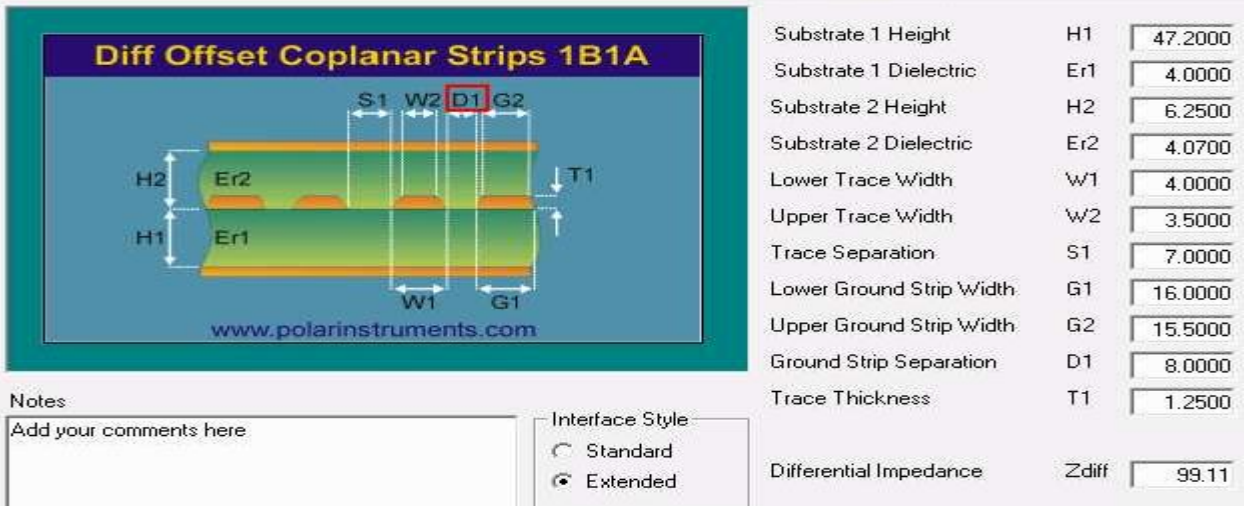
EPHY/USB 阻抗控制 – 内层走线

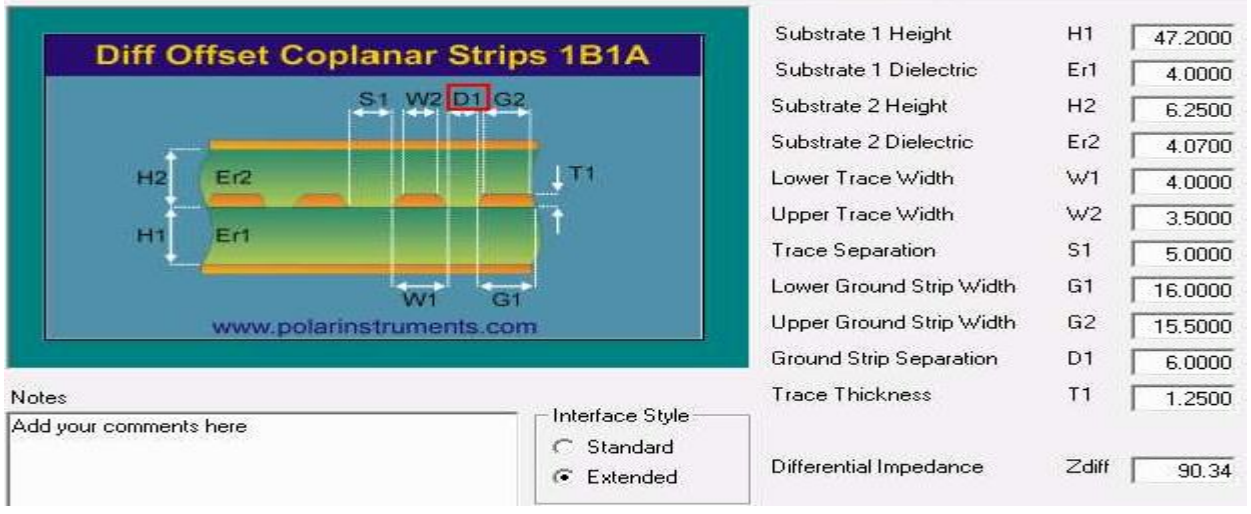
Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
100 +/- 5%	5	10	12	98.92
	4	7	8	99.11

Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
90 +/- 5%	5	7	6	90.33
	4	5	6	90.34





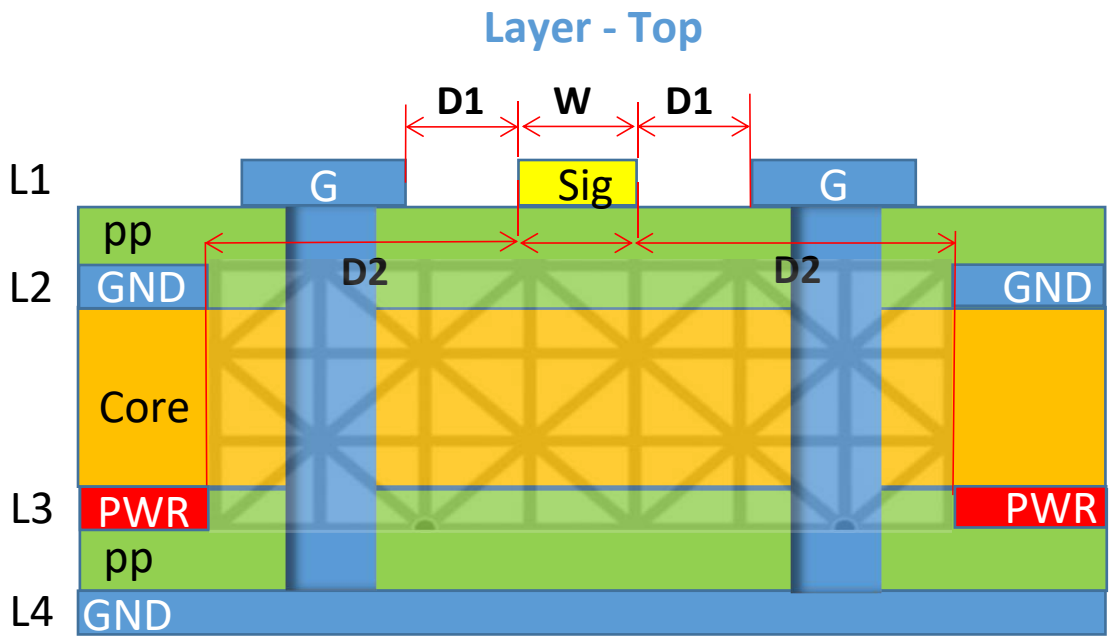




Antenna 50ohm 阻抗控制

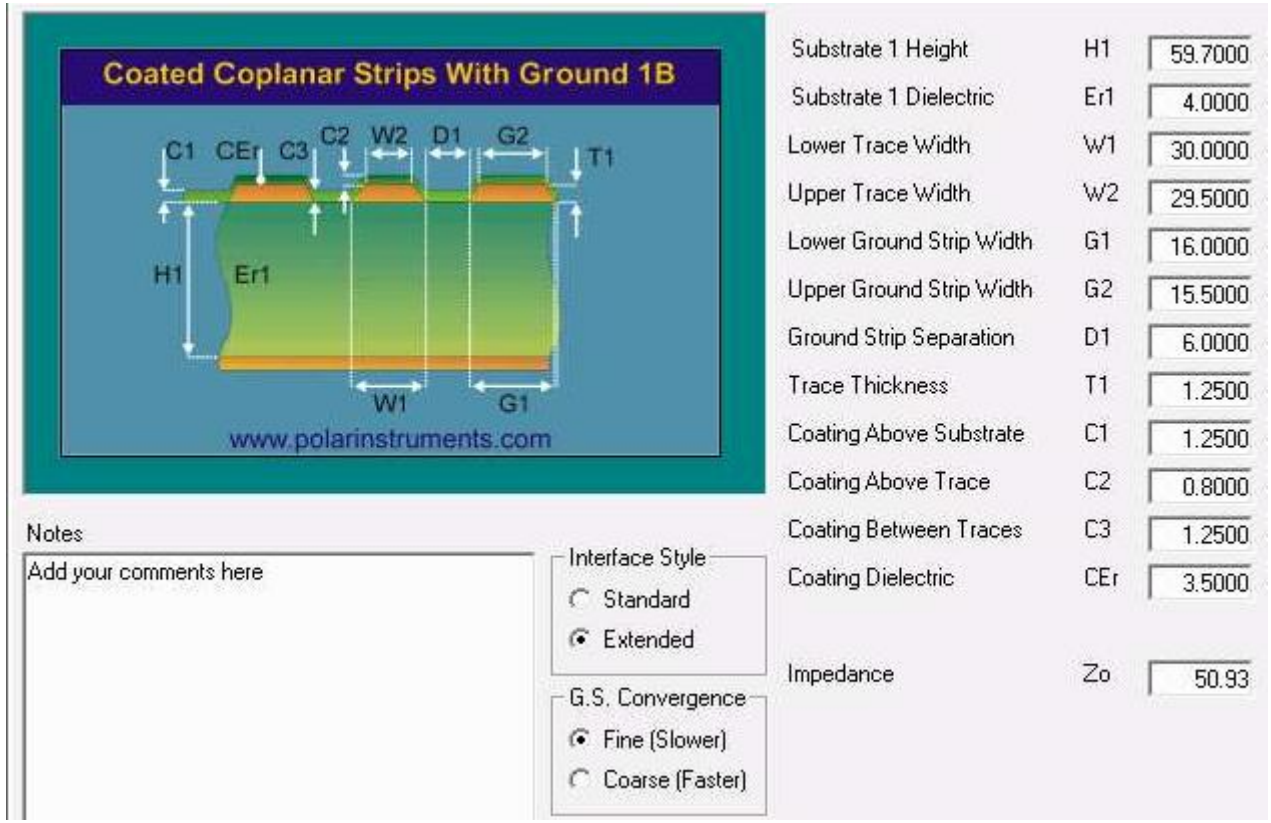
Layer	Target Z (ohm)	W (mils)	D1 (mils)	D2(mils)	Estimated Z (ohm)	Note
Top	50	30	6	12	50.93	Ref layer L4

Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	

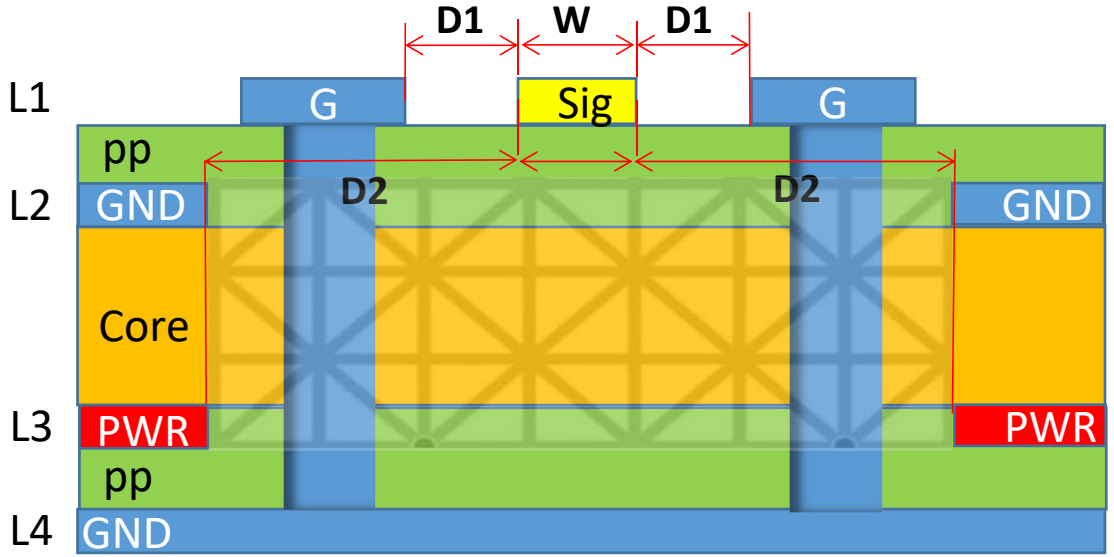


Antenna 50ohm 阻抗控制

Target Z (ohm)	W (mils)	D1 (mils)	D2(mils)	Estimated Z (ohm)
50 +/- 5%	30	6	12	50.93



Stackup	Layer	Material	Thickness (mil)	DK
		Solder Mask	0.8	3.5
L1	Top	copper+plating H+plating	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	1oz (foil)	1.25	
Core		Core	47.2	4
L3	Inner 2	1oz (foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Bottom	copper+plating H+plating	1.25	
		Solder Mask	0.8	3.5
		Total thickness (Suggested)	63.8	



MIPI/EPHY/USB/Antenna 阻抗控制

真6层, 6-layer PCB

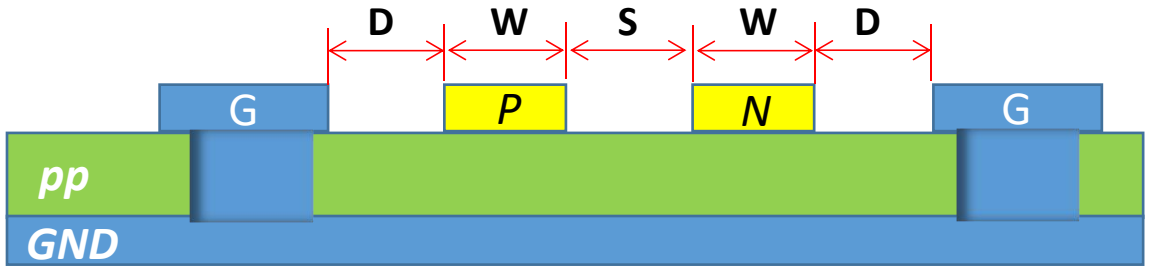
MIPI/EPHY/USB 阻抗控制 –表层走线 Option1

Layer	Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
Top/Bottom	100	5	5	6	97.99
	90	5	4	6	92.48

Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48	

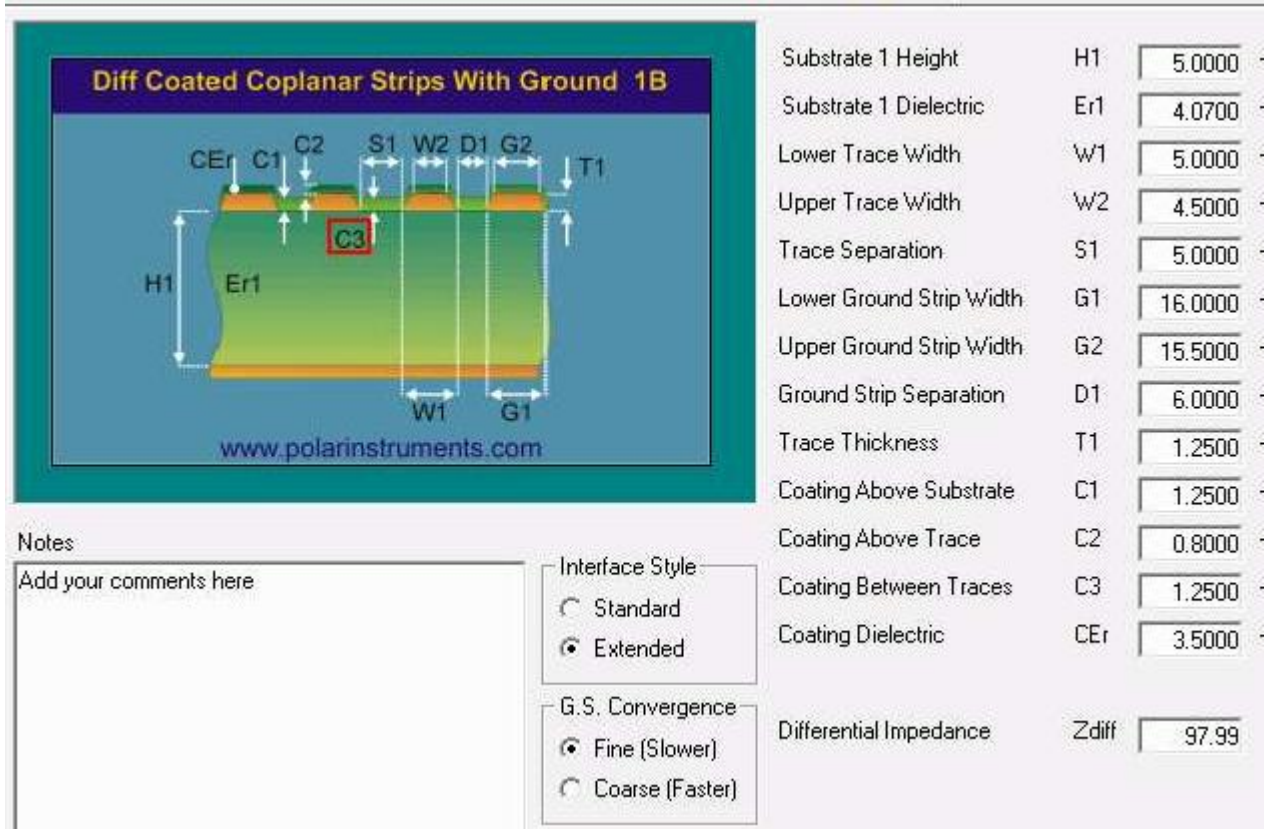
- MIPI/USB differential signals are required impedance control
  - Target impedance:
  (1) MIPI- CSI/DSI: 100ohm
  (2)USB: 90ohm

- Differential signals shielding rule:
  - pair to pair GND shielding

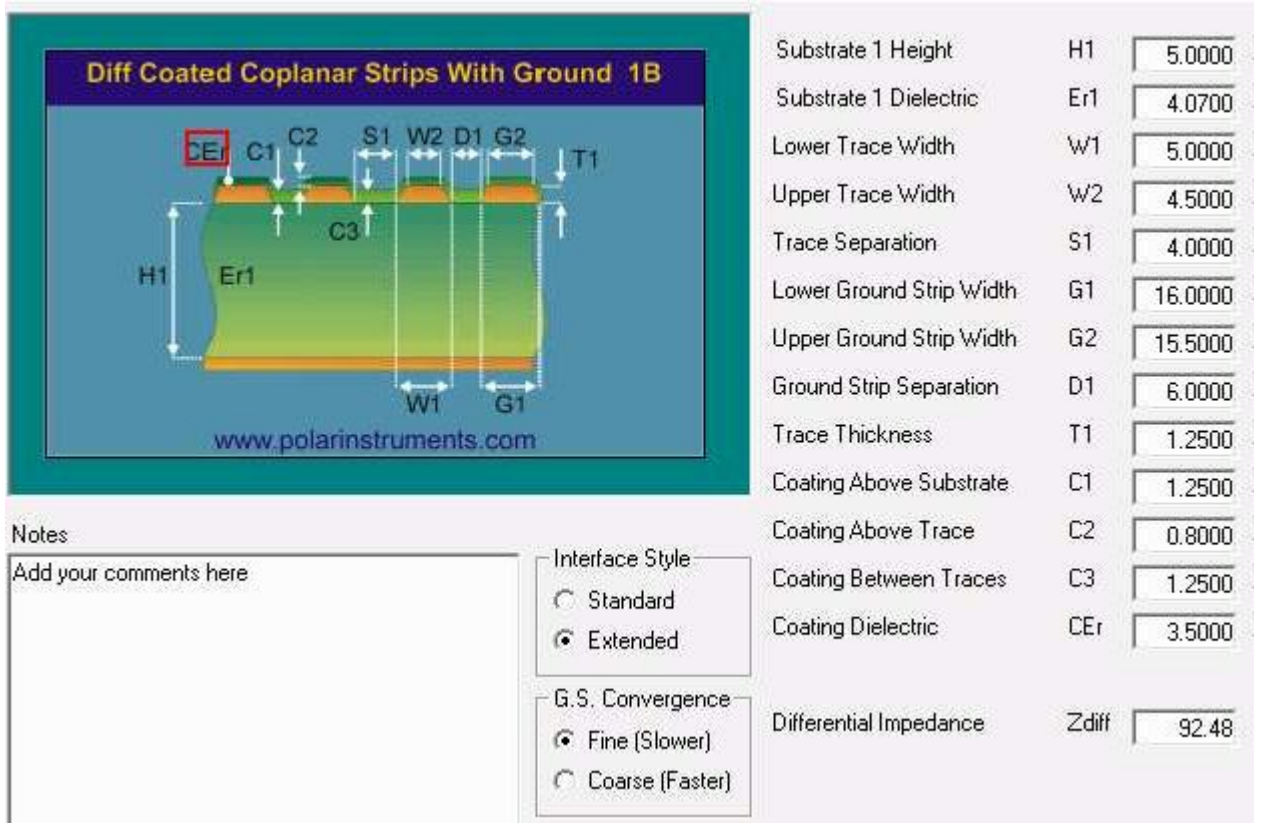


MIPI/EPHY/USB 阻抗控制 –表层走线 Option1

Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
100 +/- 5%	5	5	6	97.99



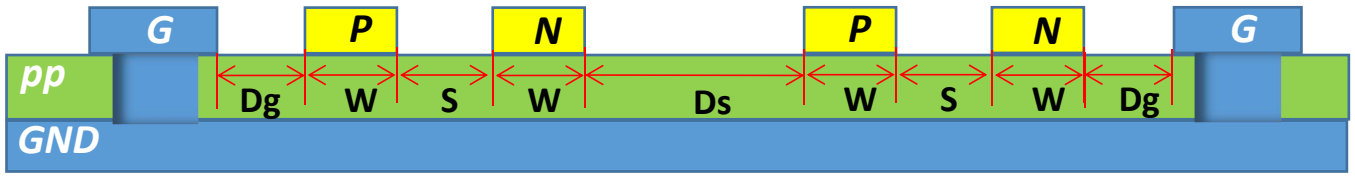
Target Z	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
90 +/- 5%	5	4	6	92.48



MIPI 阻抗控制 – 表层走线 Option2

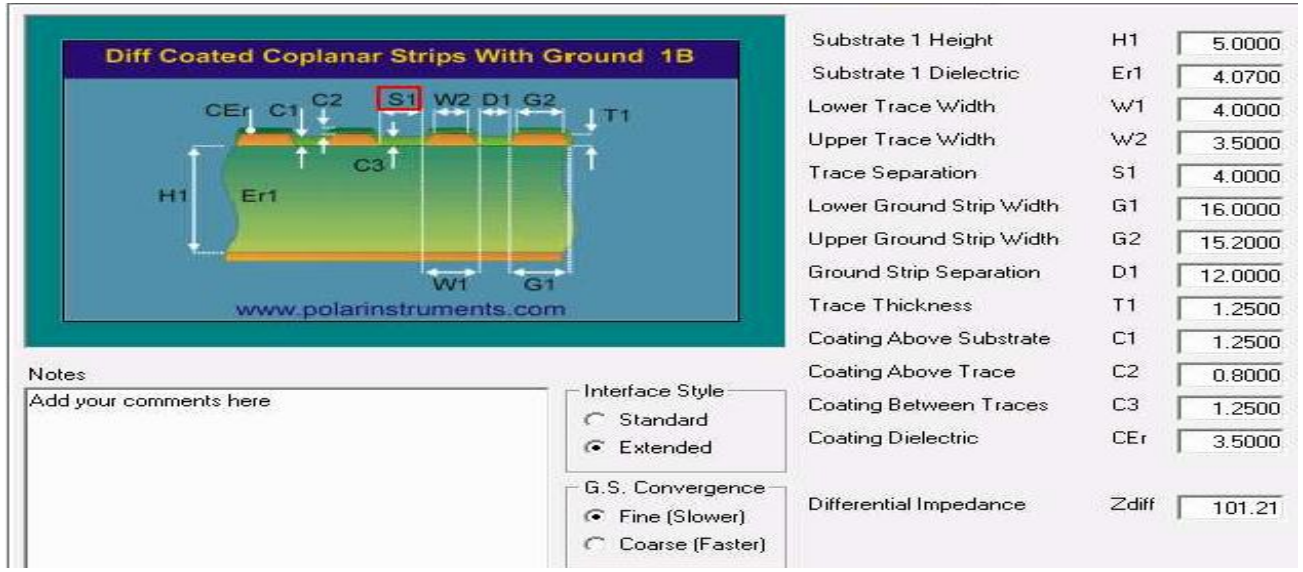
Layer	Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)	Rule
Top/Bottom	100	5	5	12	12	99.96	Ds=3W, Dg=3W

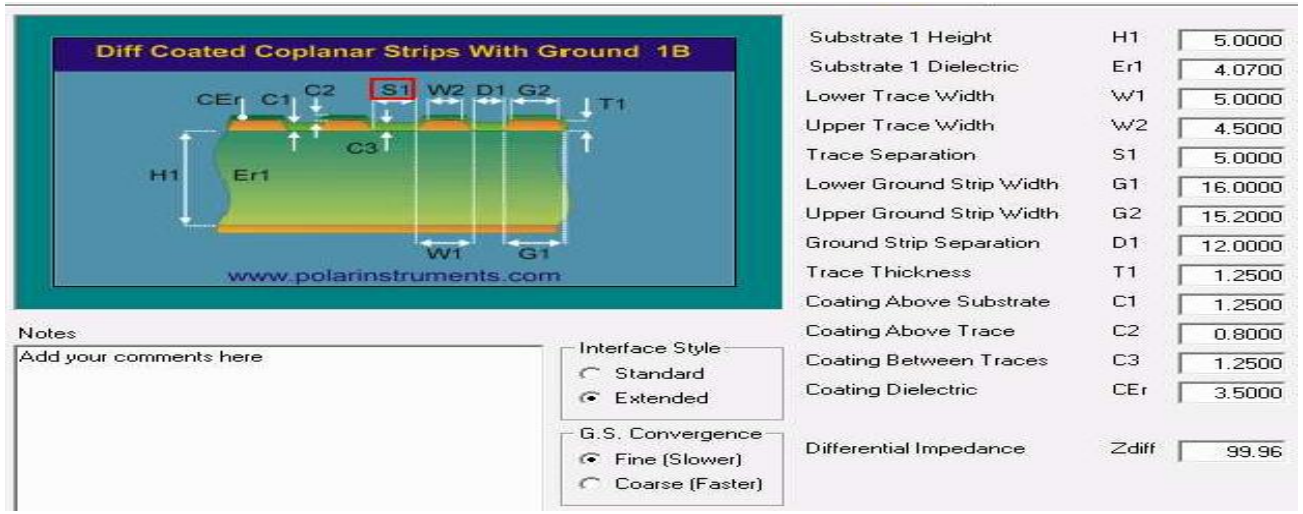
Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48	



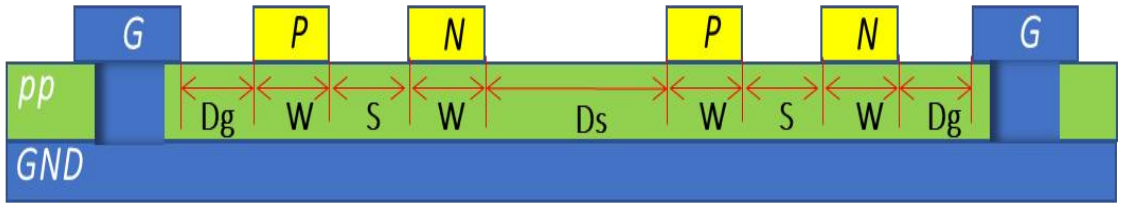
MIPI 阻抗控制 – 表层走线 Option2

Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
100 +/- 5%	5	5	12	12	99.96
	4	4	12	12	101.21





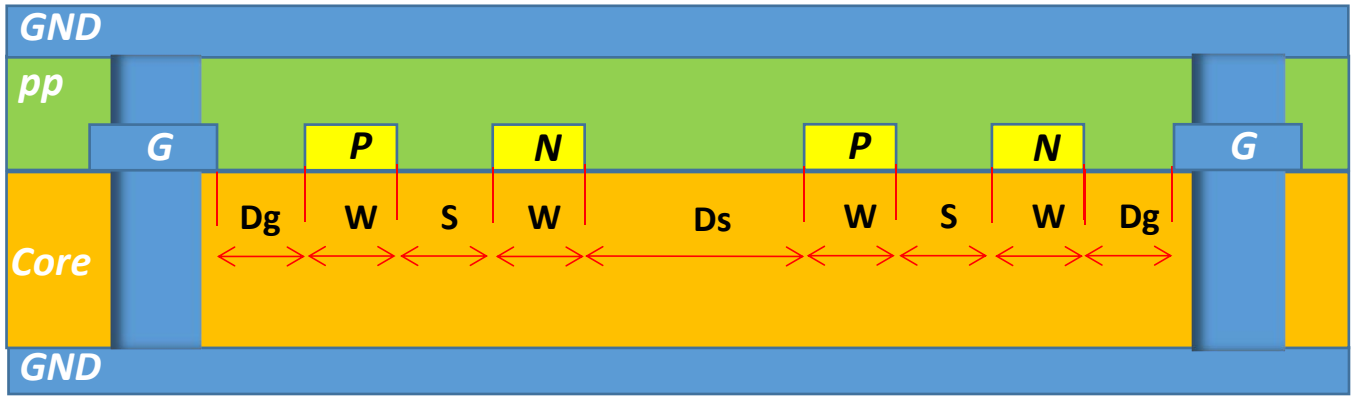
Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48	



MIPI 阻抗控制 – 内层走线

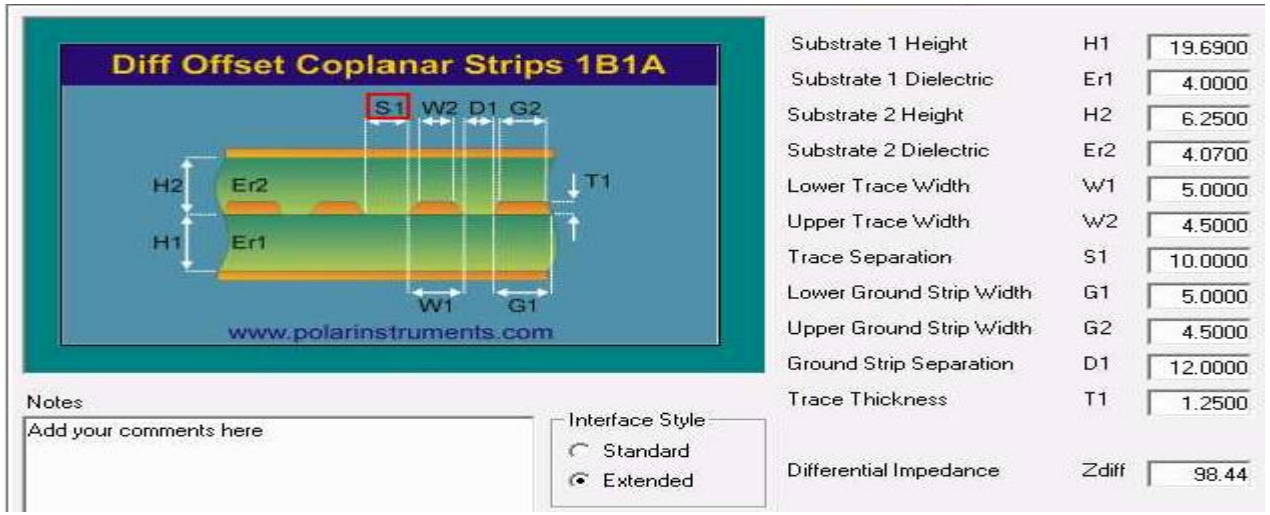
Layer	Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
L2/L3	100	5	10	12	12	98.44

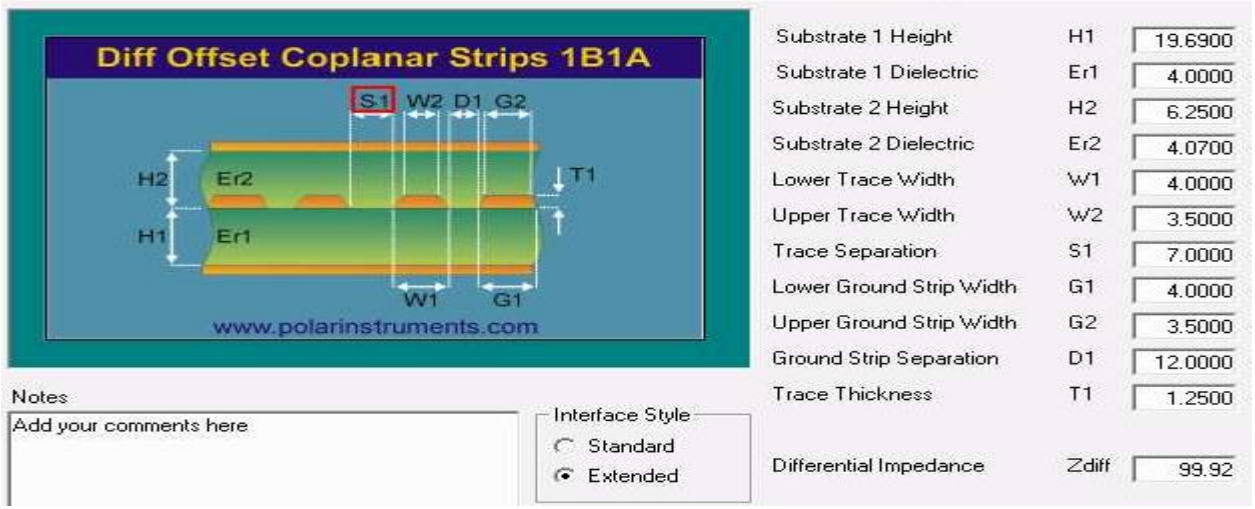
Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48	



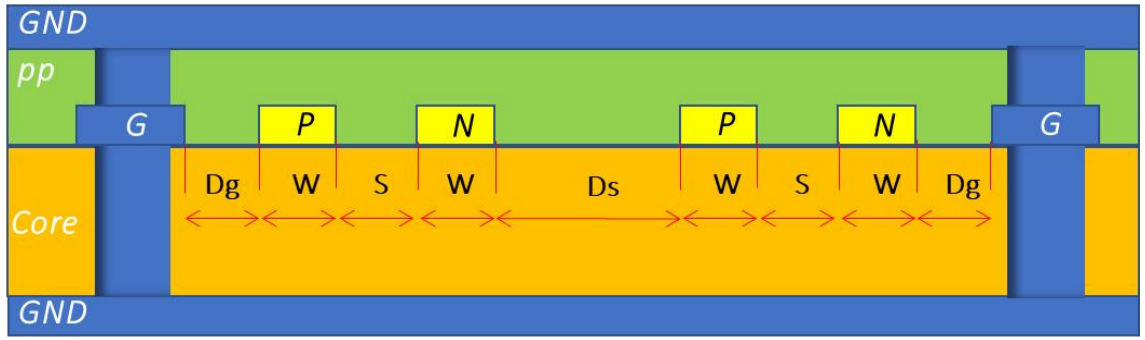
MIPI 阻抗控制 – 内层走线

Target Z (ohm)	W (mils)	S (mils)	Ds (mils)	Dg (mils)	Estimated Z (ohm)
100 +/- 5%	5	10	12	12	98.44
	4	7	12	12	99.92





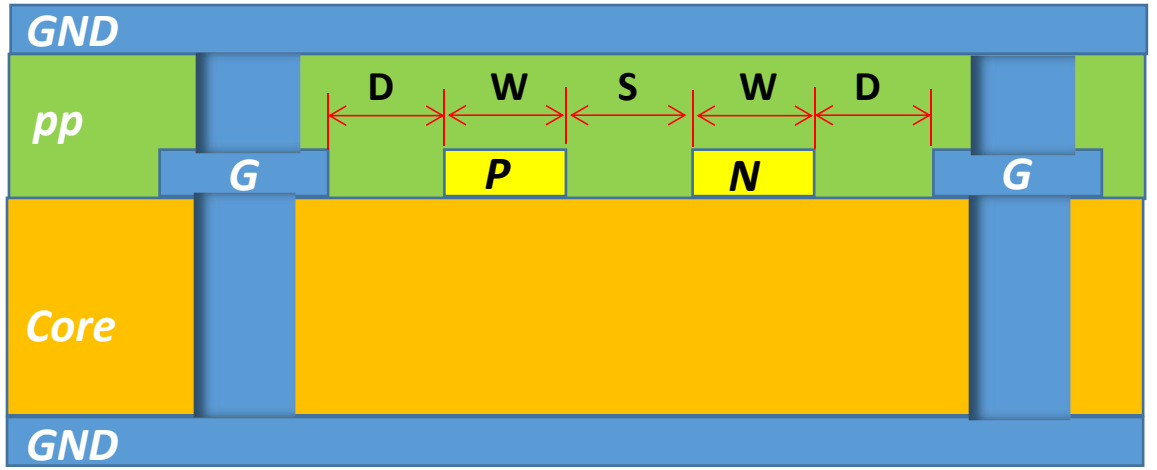
Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48	



EPHY/USB 阻抗控制 – 内层走线

Layer	Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
L2/L3	100	5	10	12	98.44
	90	5	7	6	90.14

Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48	



EPHY/USB 阻抗控制 – 内层走线

Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
100 +/- 5%	5	10	12	98.44
	4	7	8	98.92

Target Z (ohm)	W (mils)	S (mils)	D (mils)	Estimated Z (ohm)
90 +/- 5%	5	7	6	90.14
	4	5	6	90.24

Substrate 1 Height	H1	19.6900
Substrate 1 Dielectric	Er1	4.0000
Substrate 2 Height	H2	6.2500
Substrate 2 Dielectric	Er2	4.0700
Lower Trace Width	W1	5.0000
Upper Trace Width	W2	4.5000
Trace Separation	S1	10.0000
Lower Ground Strip Width	G1	16.0000
Upper Ground Strip Width	G2	15.5000
Ground Strip Separation	D1	12.0000
Trace Thickness	T1	1.2500
Differential Impedance	Zdiff	98.44

Notes: Add your comments here

Interface Style: Standard / Extended

Substrate 1 Height	H1	19.6900
Substrate 1 Dielectric	Er1	4.0000
Substrate 2 Height	H2	6.2500
Substrate 2 Dielectric	Er2	4.0700
Lower Trace Width	W1	5.0000
Upper Trace Width	W2	4.5000
Trace Separation	S1	7.0000
Lower Ground Strip Width	G1	16.0000
Upper Ground Strip Width	G2	15.5000
Ground Strip Separation	D1	6.0000
Trace Thickness	T1	1.2500
Differential Impedance	Zdiff	90.14

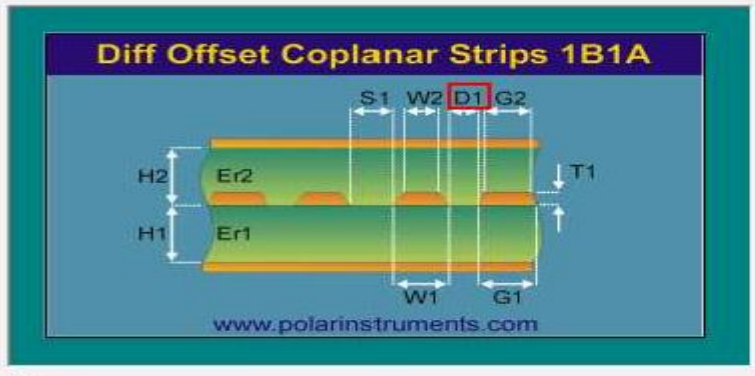
Notes: Add your comments here

Interface Style: Standard / Extended

Substrate 1 Height	H1	19.6900
Substrate 1 Dielectric	Er1	4.0000
Substrate 2 Height	H2	6.2500
Substrate 2 Dielectric	Er2	4.0700
Lower Trace Width	W1	4.0000
Upper Trace Width	W2	3.5000
Trace Separation	S1	7.0000
Lower Ground Strip Width	G1	16.0000
Upper Ground Strip Width	G2	15.5000
Ground Strip Separation	D1	8.0000
Trace Thickness	T1	1.2500
Differential Impedance	Zdiff	98.92

Notes: Add your comments here

Interface Style: Standard / Extended



Substrate 1 Height	H1	19.6900
Substrate 1 Dielectric	Er1	4.0000
Substrate 2 Height	H2	6.2500
Substrate 2 Dielectric	Er2	4.0700
Lower Trace Width	W1	4.0000
Upper Trace Width	W2	3.5000
Trace Separation	S1	5.0000
Lower Ground Strip Width	G1	16.0000
Upper Ground Strip Width	G2	15.5000
Ground Strip Separation	D1	6.0000
Trace Thickness	T1	1.2500
Differential Impedance	Zdiff	90.24

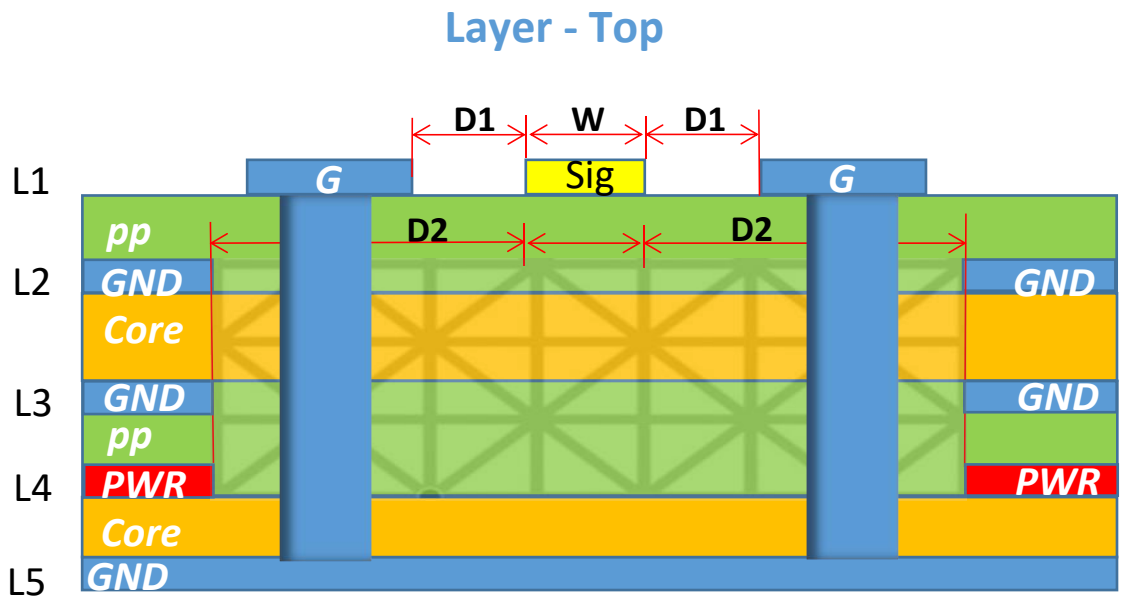
Notes: Add your comments here

Interface Style: Standard / Extended

Antenna 50ohm 阻抗控制

Layer	Target Z (ohm)	W (mils)	D1 (mils)	D2(mils)	Estimated Z (ohm)	Note
Top	50	30	6	12	50.55	Ref layer L5

Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48	



Antenna 50ohm 阻抗控制

Target Z (ohm)	W (mils)	D1 (mils)	D2(mils)	Estimated Z (ohm)
50 +/- 5%	30	6	12	50.55

Stack up	Layer	Material	Thickness (mil)	DK
		soldermask	0.8	
L1	TOP	copper+plating H+Planting	1.25	
Prepreg		Prepreg	5	4.07
L2	Inner 1	copper(foil)	1.25	
Core		Core	19.69	4
L3	Inner 2	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L4	Inner 3	copper(foil)	1.25	
Core		Core	19.69	4
L5	Inner 4	copper(foil)	1.25	
Prepreg		Prepreg	5	4.07
L6	BOT	copper+plating H+Planting	1.25	
		soldermask	0.8	
		Total thickness (suggested)	63.48