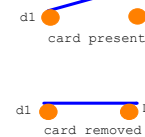
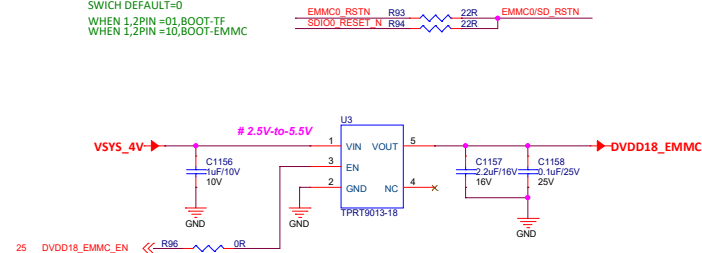
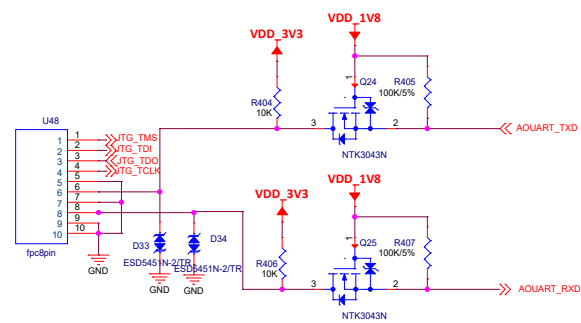
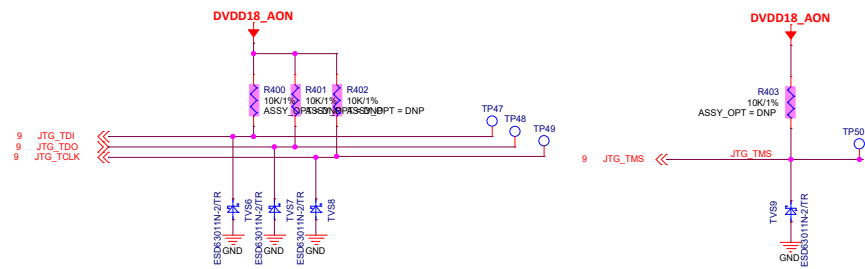


[illegible][illegible]

```
SWICH DEFAULT=0
WHEN 1,2PIN =01,BOOT-TF
WHEN 1,2PIN =10,BOOT-EMMC
```

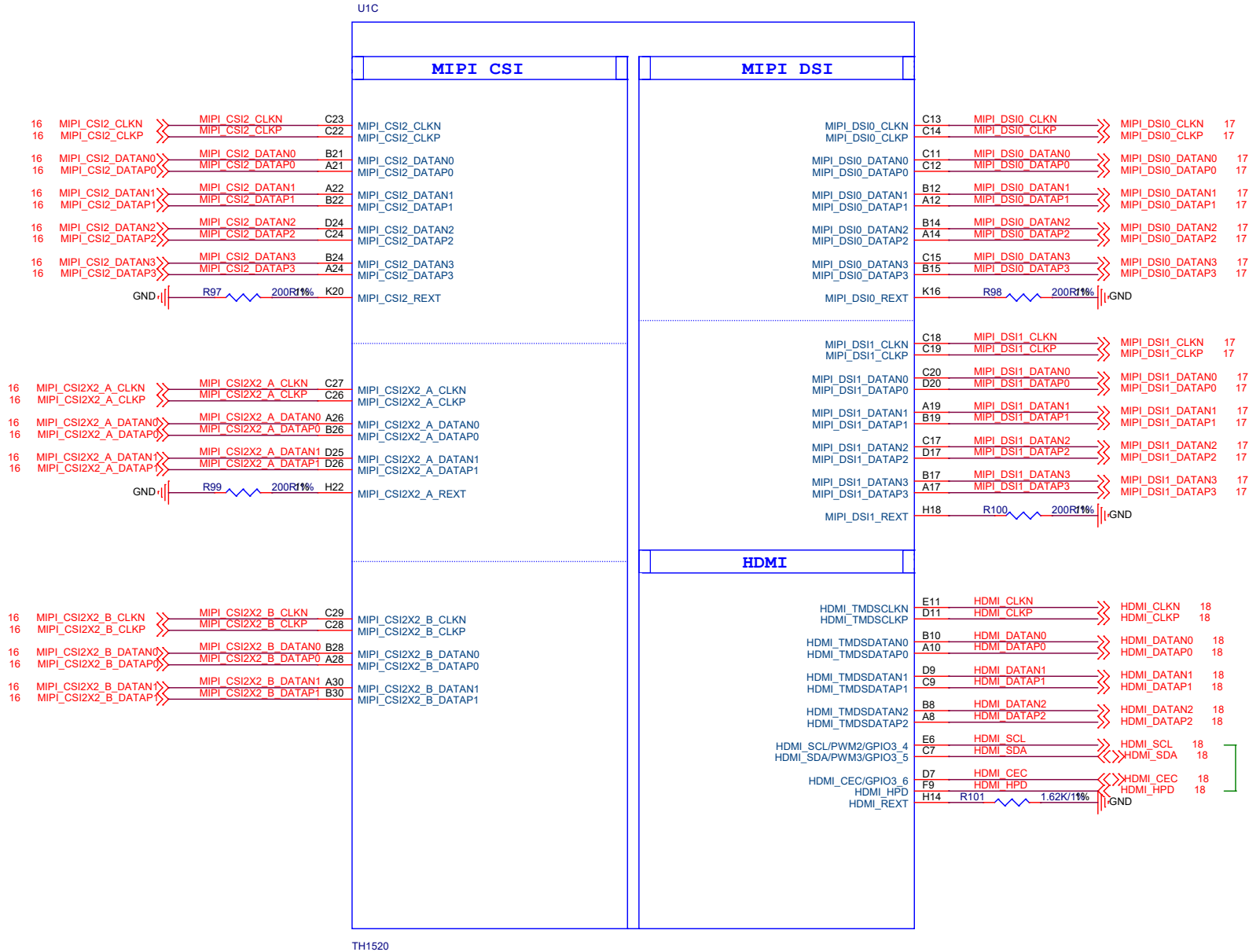


CPU JTAG

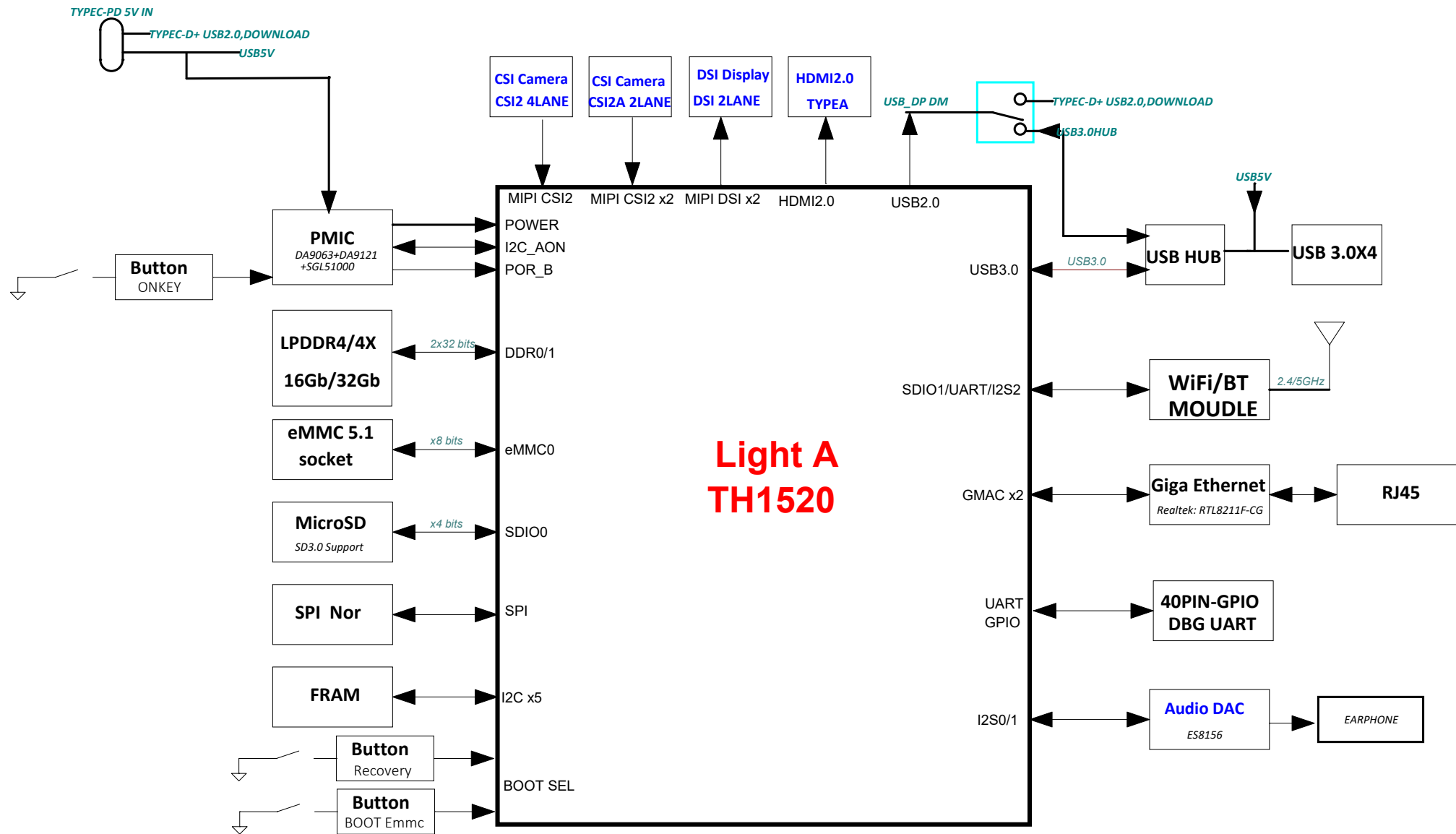


E902 Debug port

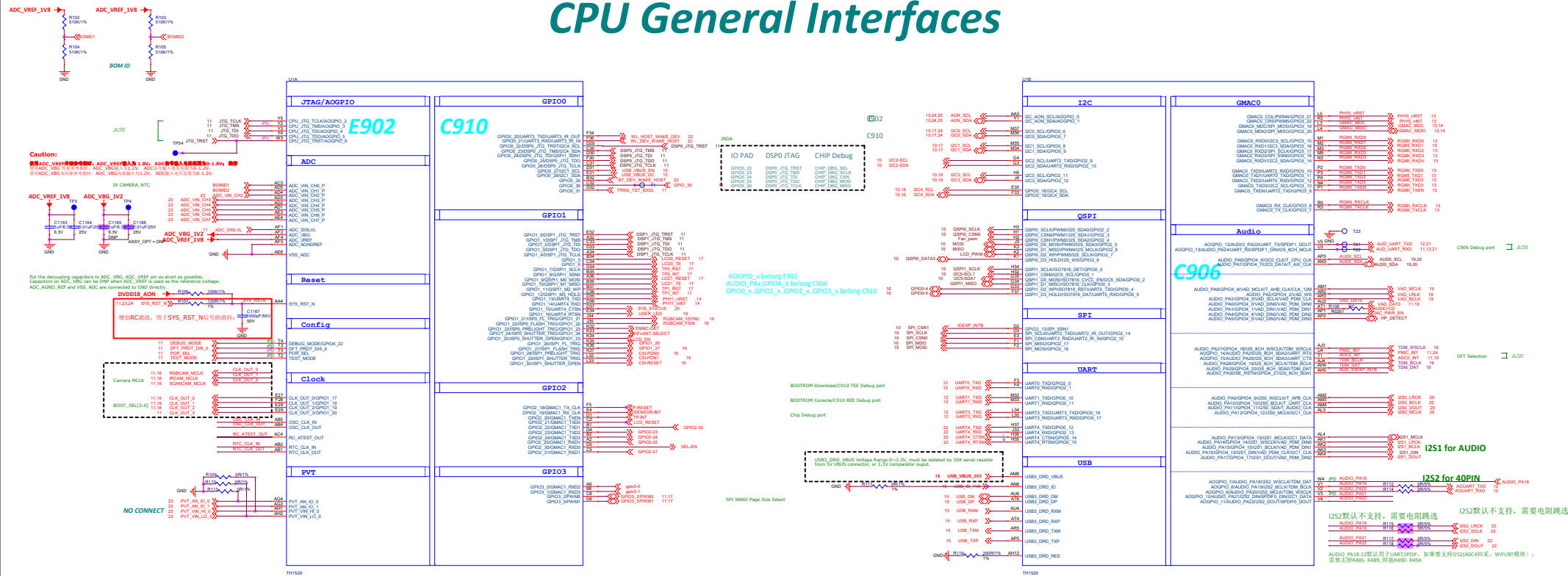
CPU Video Interface



Board Block Diagram

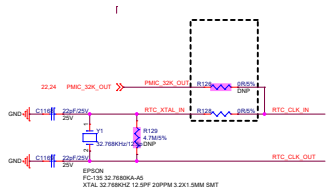


CPU General Interfaces



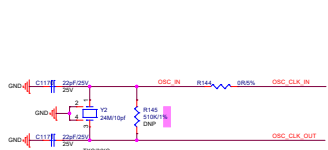
32K RTC Clock

焊盘堆叠放置，根据需要选焊电阻
验证外部有源时钟输入时， 焊接R53，去掉R48, Y1, C336



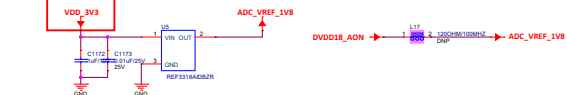
24M Clock

焊盘堆叠放置，根据需要选焊电阻
验证外部有源时钟输入时，焊接R34，去掉R33, Y2, C338



RC_ATEST_OUT

ADC Reference




模拟输出引脚，用于RC 测试

U32靠近CPU放置。
ADC_VREF使用外部供电时，ADC_VREF_V18不能早于AVDD18_ADC（DVDD18_AON）上电，否则有漏电流。
ADC_VREF可使用电源基准源供电，也可以使用普通LDO供电。

I2C Address Table:

I2C Port	Interface	Device	I2C Address
AON_I2C1	PMIC	DA9063	0x5A[10111010]
		DA9121	0x68[11010000]
	RTC	SG1S3000	0x75[11101010]
AUD_I2C0	ADC0-3	PC98063	0x51[080010]
		ES7210	0x40[10000000]
		ES7210	0x41[10000010]
	DAC0	ES7210	0x43[10000010]
		ES8156	0x08[00001000]
		PA1	0x58[10110000]
AUD_I2C1	PA2	AW87519	0x5B[10111110]
	IO EXP	PCA16080AHK	0x20[01000000]
	ADC4	ES7210	0x40[10000000]
	DAC1	ES8156	0x08[00001000]
	PA3	AW87519	0x5B[10110000]
	PA4	AW87519	0x5B[10111110]
I2C0	FRAM	MB85RC1MT	0x50[10100000]
	TOUCH0	GT911	0x5D[10111010]
	LCD BIAS0	SGM3804	0x3E[01111110]
	FRAM	MB85RC1MT	0x50[10100000]
I2C1	TOUCH1	GT911	0x5D[10111010]
			0x14[00101000]
			0x3E[01111110]
I2C2	LCD BIAS1	SGM3804	0x3E[01111110]
	FRAM	MB85RC1MT	0x50[10000000]
	CS12X2A	SC13163	0x65[11001000]
I2C3	FRAM	IOV13371	0x6C[11011000]
		MB85RC1MT	0x50[10100000]
		UV12870	0x20[01000000]
	CS12	SSK4H7	0x20[01000000]
I2C4	FRAM	IOV5693	0x6C[11011000]
		MB85RC1MT	0x50[10100000]
		GC5031	0x65[11011110]
	IO EXP	PTNS150A	0x3A[01100000]
	USB	PCA164080AHK	0x20[01000000]

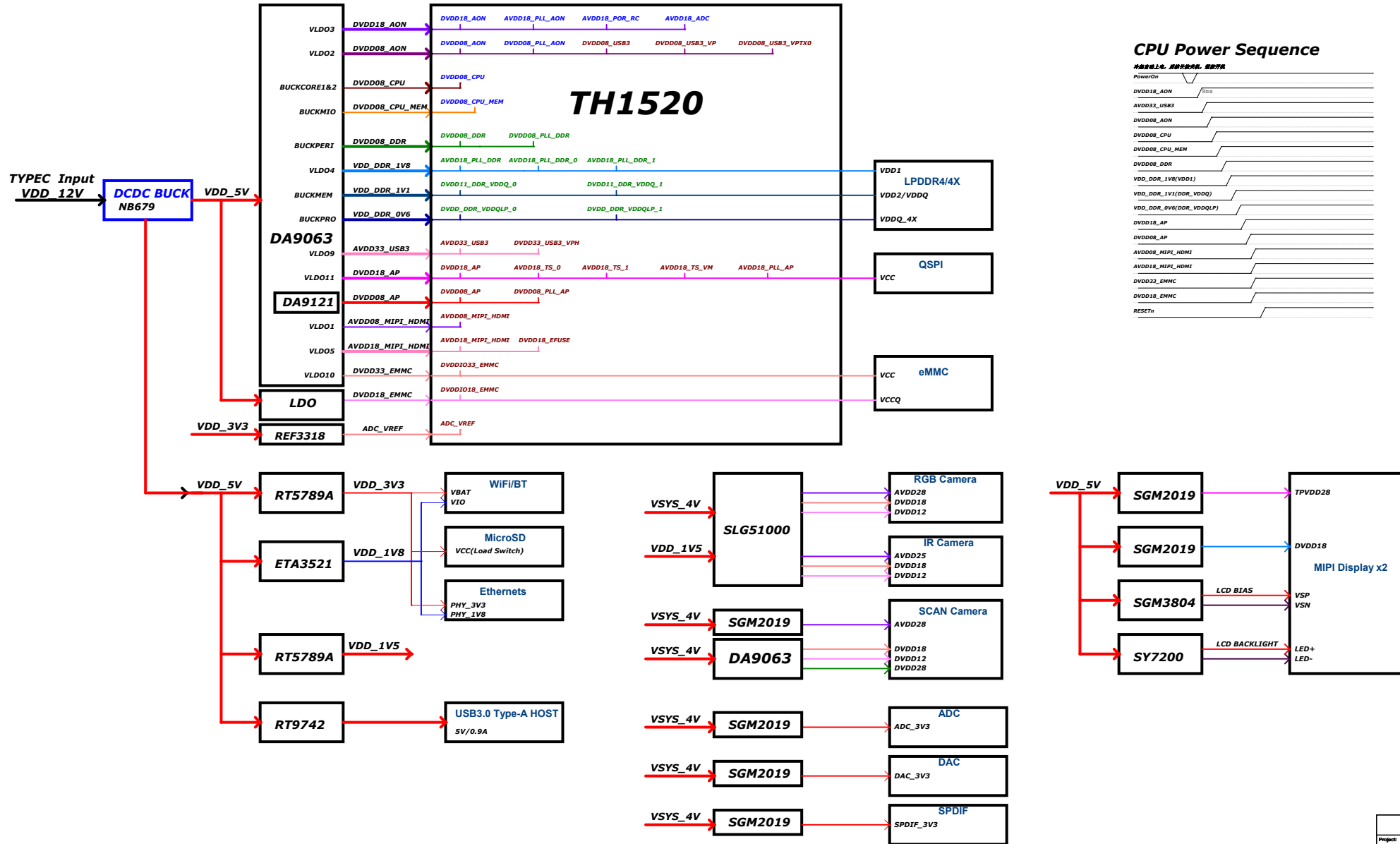
AUDIO PAD 分配情况:

Port	Option1 (Default)	Option1 Device	Option2	Option2 Device
TDI	✓	ES7210	✓	ES7210
VAD_PDM	✓	ES7210	✓	ES7210
I2S0	✓	HT4344	✓	HT4344
I2S1	✓	HT4344	✓	HT4344
I2S2	✗	HT4344	✓	ES7210B1 
SPDIF0	✓	Connector	✗	
SPDIF1	✗		✓	Connector
AUD_I2C0	✓	ES7210,AW87519	✓	ES7210,AW87519
AUD_I2C1	✓	ES7210,AW87519	✓	ES7210,AW87519
AQUART	✗	Connector	✗	
AUDUART	✓	Connector	✗	

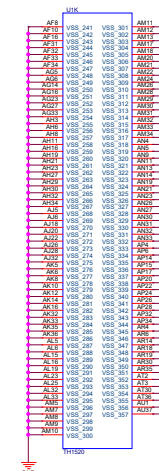
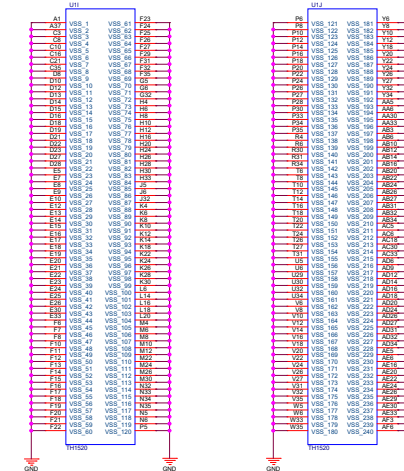
10 PU/PD:

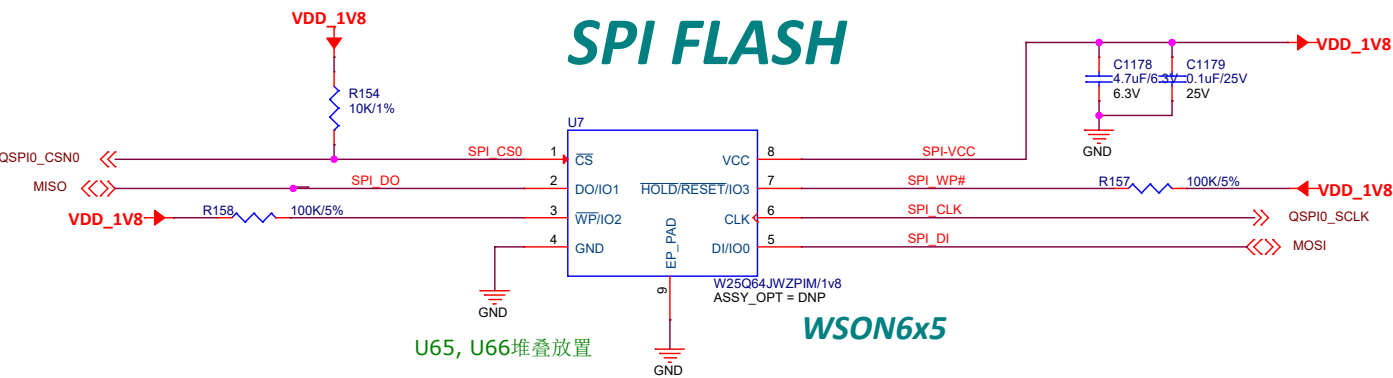
Parameter	Min	Typ	Max
RSPU(Strong)	1.6K	2.1K	3K
RPU	32K	48K	79K
RPD	30K	44K	65K

Power Diagram and Sequence



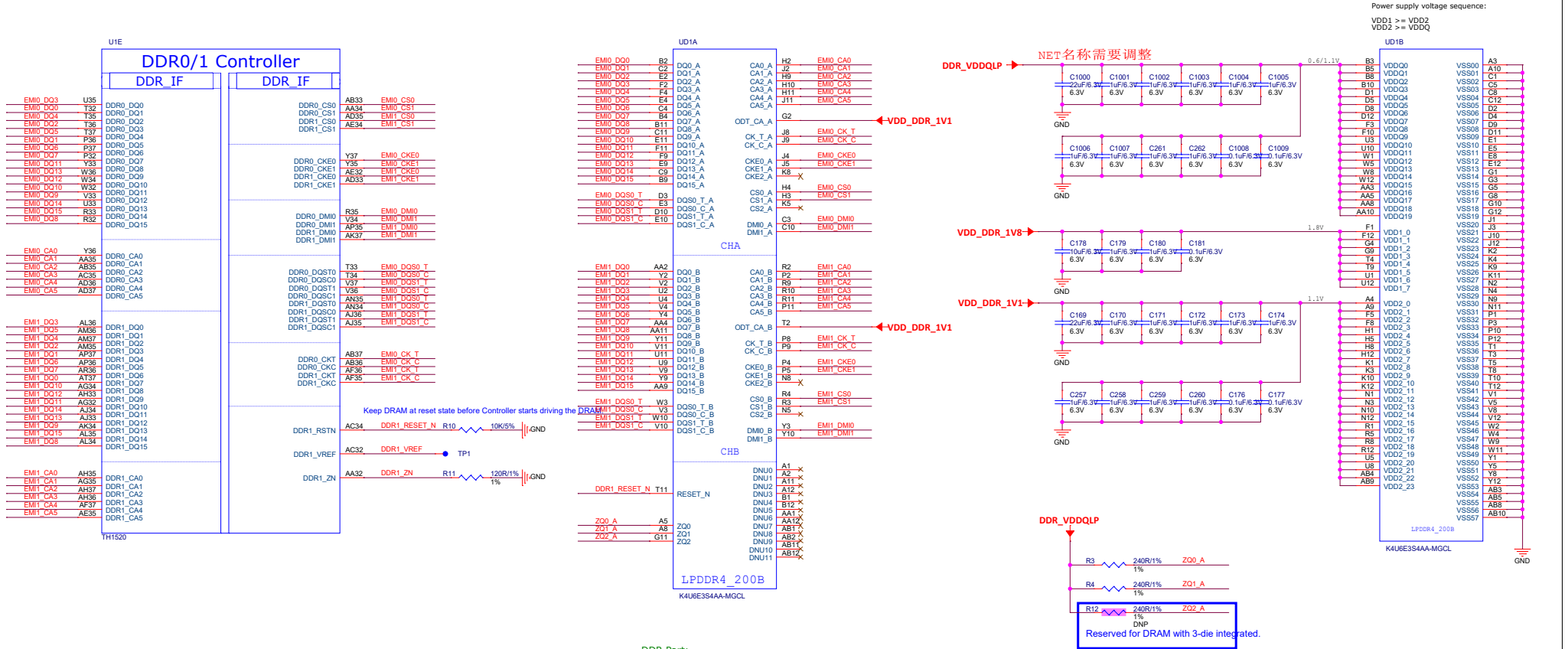
GND

[illegible]



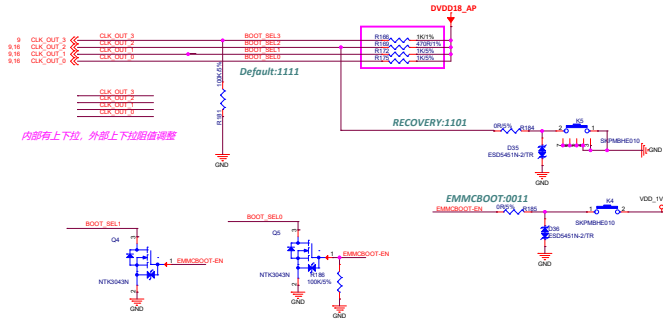
Project:	MV051		
File:	SPI Flash and RTC		
Date:	Monday, February 26, 2024	Rev:	X1.0
Designed by:	<designer>	Sheet:	4 of 24

LPDDR4/4X-1



BOOT Switch and JTAG Debug

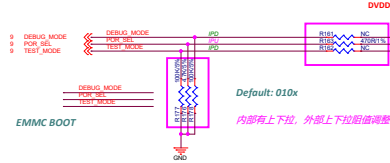
Boot Switch



Boot Mode Setting

BOOT_SEL3 SW1 [1]	BOOT_SEL2 SW1 [2]	BOOT_SEL1 SW1 [3]	BOOT_SEL0 SW1 [4]	Boot Mode Setting SW1 [1-4]
X	0	X	X	USB Download
X	1	0	0	eMMC Boot
X	1	0	1	SD Boot, SDIO0
X	1	1	0	SPI NAND boot, QSPI0, CS0
X	1	1	1	SPI NOR Boot, QSPI0, CS0

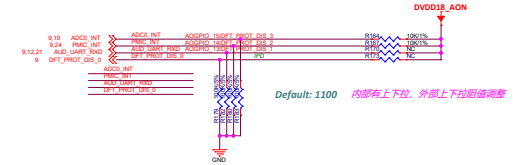
Debug Switch



Debug Setting Table

Signal	Setting	Description
DEBUG_MODE	0	默认低电平，正常工作模式
SW2 [1]	1	高电平，使能芯片测试模式
POR_SEL	0	低电平，选择内部POR
SW2 [2]	1	默认高电平，选择外部POR
TEST_MODE	0	默认低电平，正常工作模式
SW2 [3]	1	高电平，使能芯片测试模式

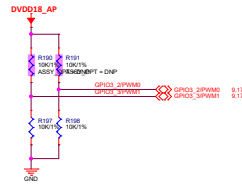
BSCAN Switch



BSCAN Requirement

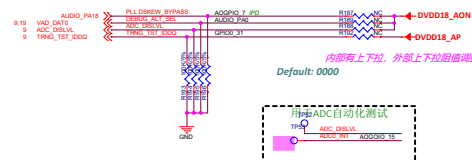
PAD	Signal	PD/PU	SWITCH	Switch Setting
AOGPIO_15	DFT_PROT_DIS_3	PD	SW4 [1]	0
AOGPIO_14	DFT_PROT_DIS_2	PU	SW4 [2]	1
AOGPIO_13	DFT_PROT_DIS_1	PD	SW4 [3]	1
DFT_PROT_DIS_0	DFT_PROT_DIS_0	PU	SW4 [4]	1
TEST_MODE	TEST_MODE	PU	SW2 [3]	1

SPI NAND Page Setting



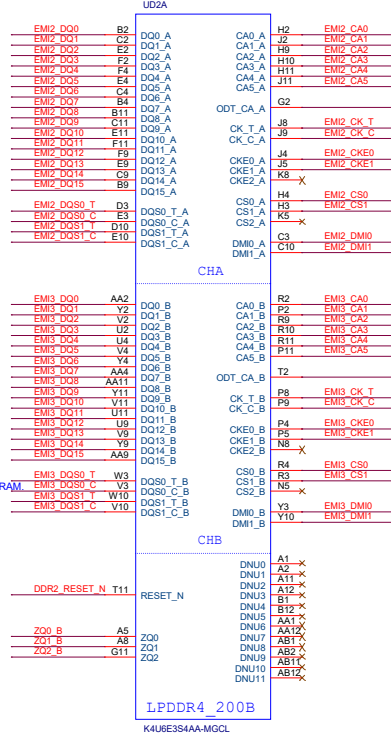
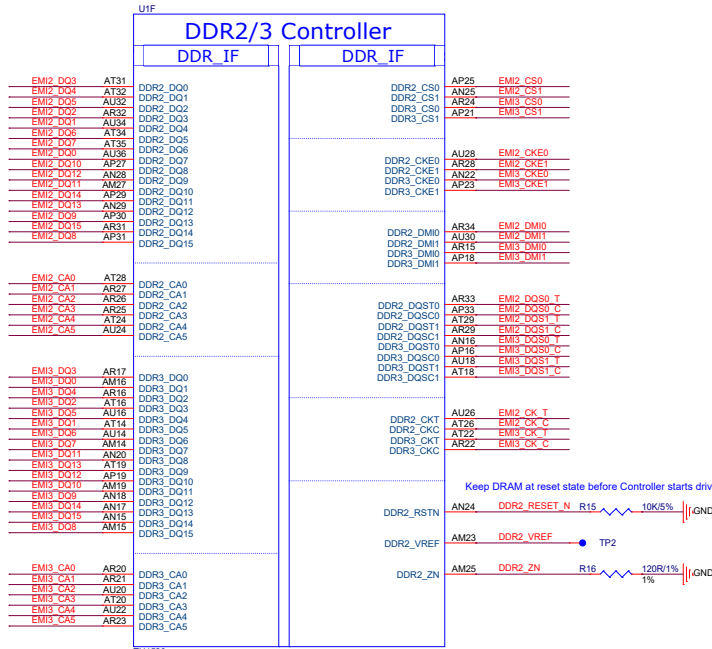
GPIO3_3 HARPS A10	GPIO3_2 HARPS A9	SPI NAND Page Size Setting
0	0	Page size=2K
0	1	Page size=4K
1	0	Page size=8K
1	1	Page size=16K

Misc Switch



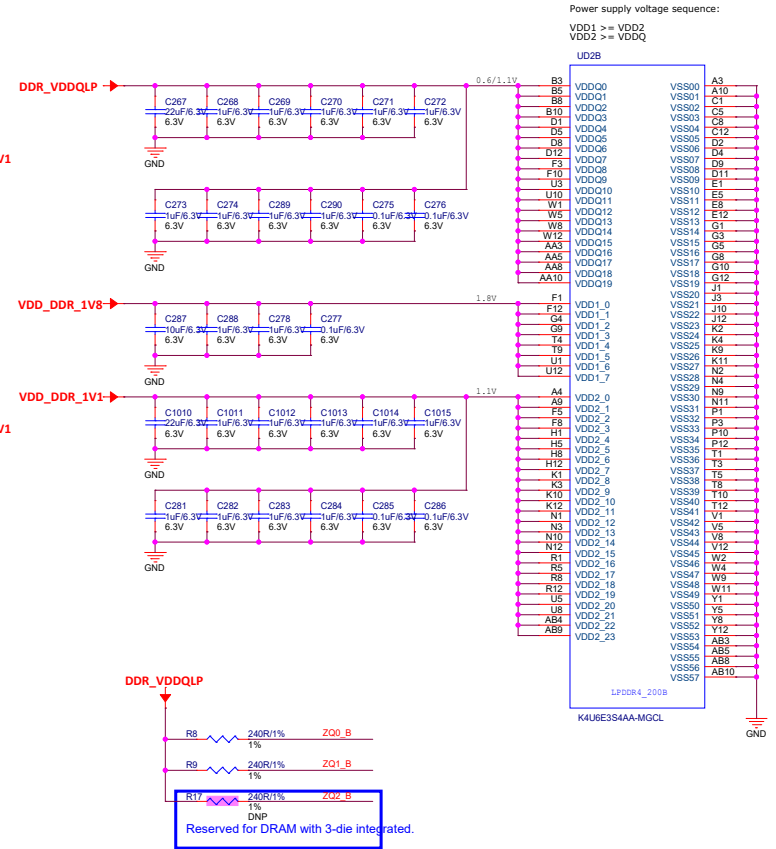
Pad	Signal	Switch	Setting	Description
AOGPIO_7	PLL_DSKEW_BYPASS	SW3 [1]	0	默认低电平，使能PLL校准电路
AUDIO_PA0	DEBUG_ALT_SEL	SW3 [2]	0	高电平，PLL校准电路进入Bypass Mode
ADC_DISLVL	ADC_DISLVL	SW3 [3]	1	默认低电平，正常工作模式
GPIO3_31	TRNG_TST_IDDQ	SW3 [4]	0	默认低电平，正常工作模式
			1	Debug Mode下，作为TRNG_TST_IDDQ功能

LPDDR4/4X-2



DDR Part:

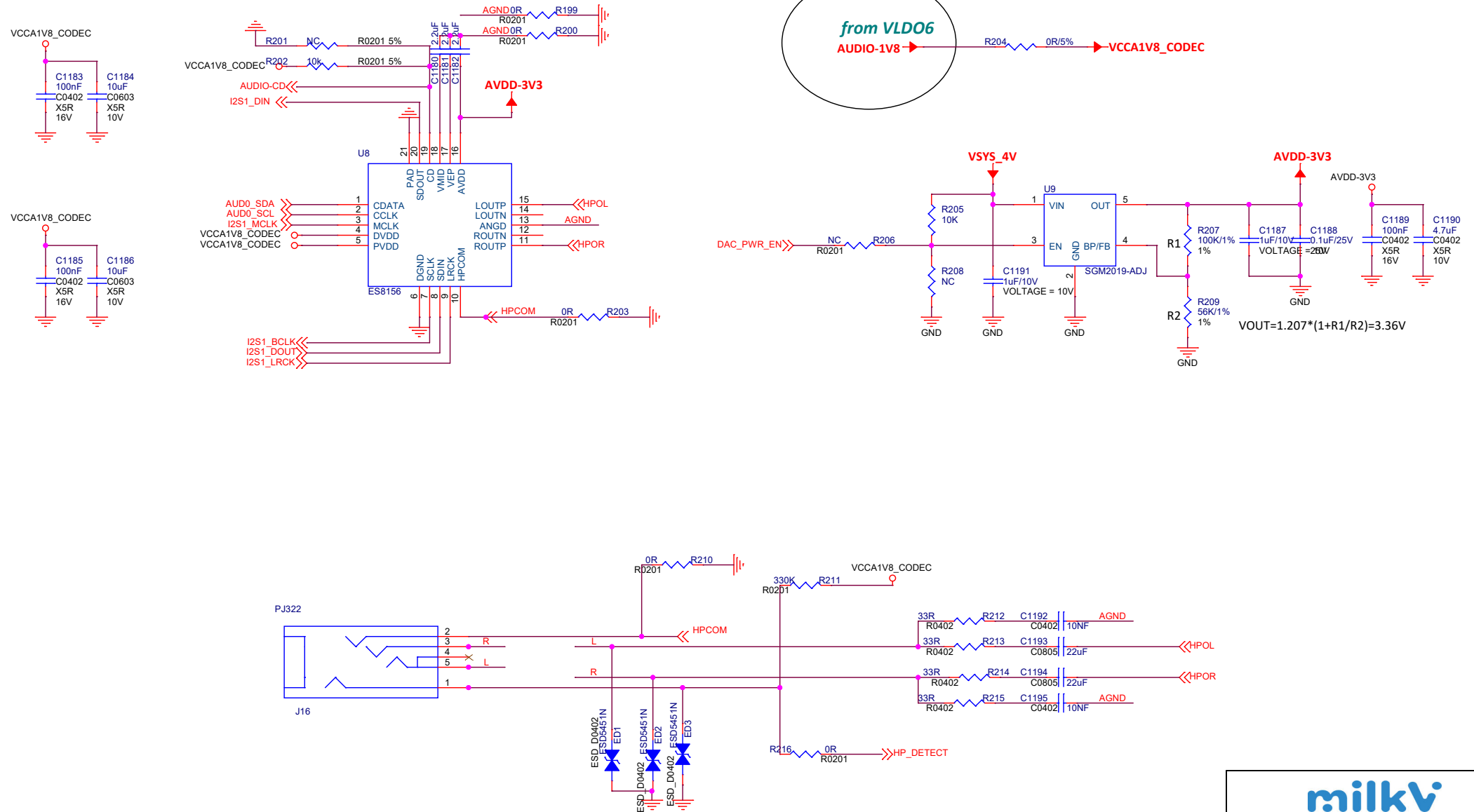
K4UE3S4AA-MGCL	Samsung	LPDDR4X	2GB
K4UE3D4AA-MGCL	Samsung	LPDDR4X	4GB
K4FBE3D4HM-SGCL	Samsung	LPDDR4	4GB
MT53D512M32D2D5-046 WT:D	Micron	LPDDR4/4X	2GB
MT53D1024M32D4DT-046 WT:D	Micron	LPDDR4/4X	4GB




milkv

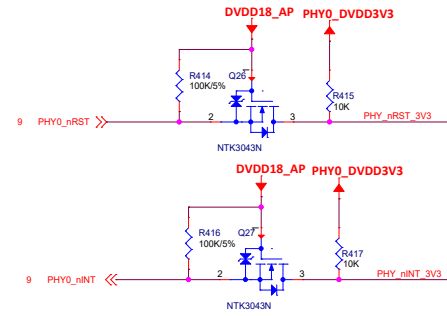
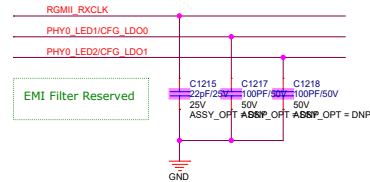
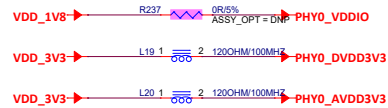
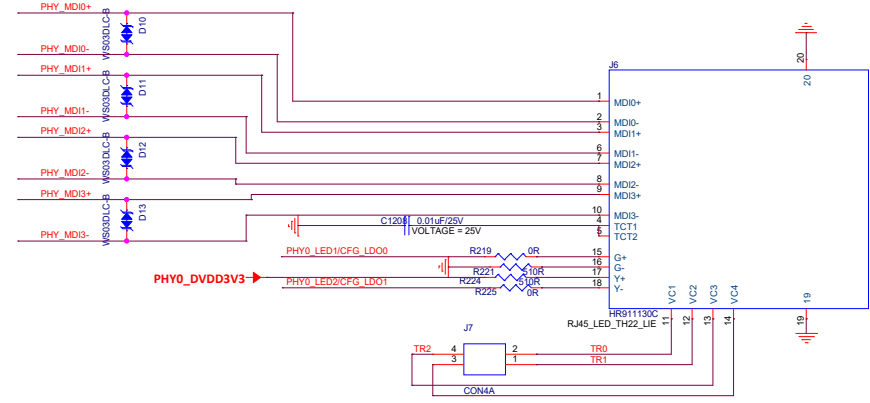
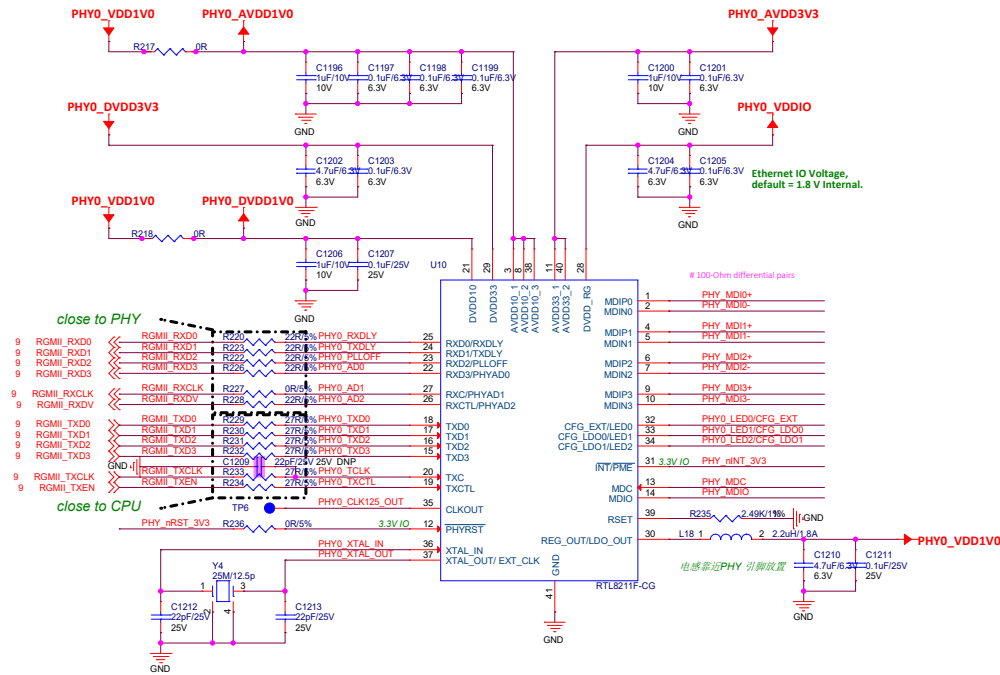
Project:	MV051
File:	LPDDR4/4X-2
Date:	Monday, February 26, 2024
Designed by:	<designer>
Rev:	X1.0
Sheet:	6 of 24

AUDIO DAC

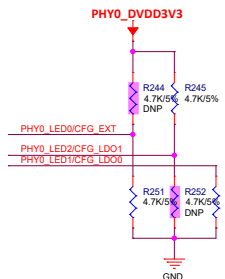


			
Project:		MV051	
File:		Audio DAC	
Date:	Monday, February 26, 2024	Rev:	X1.0
Designed by:	<designer>	Sheet:	6 of 24

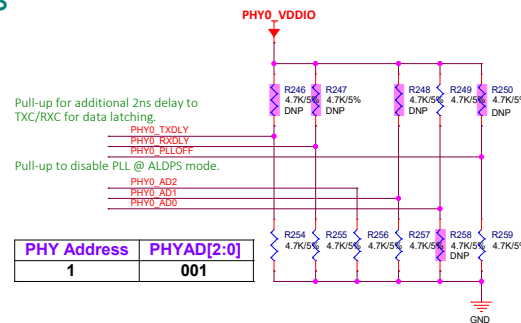
GMAC Ethernet0



Power-on Strapping Pins CFG



RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(Default)	0	10
Internal 1.5V	0	11

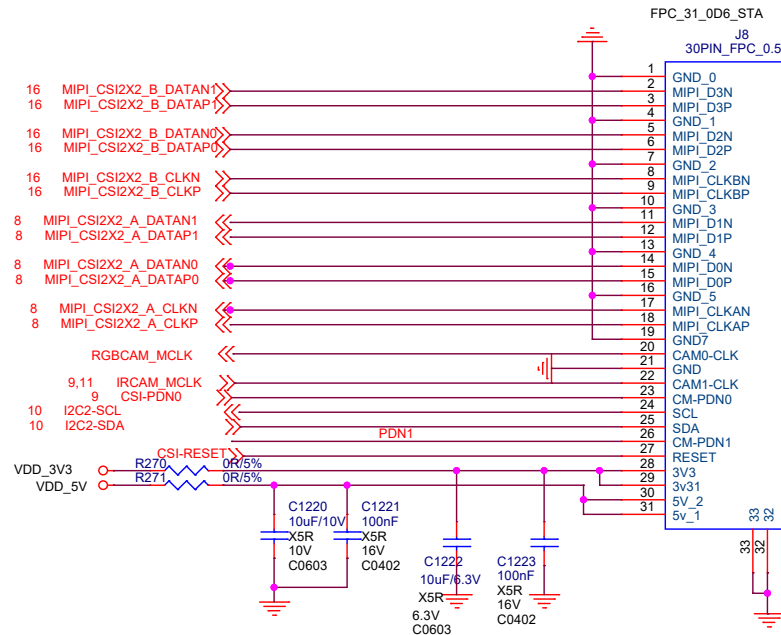
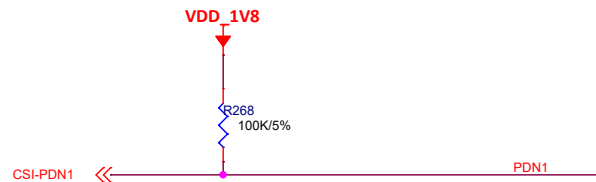


Pull-up for additional 2ns delay to TXC/RXC for data latching.

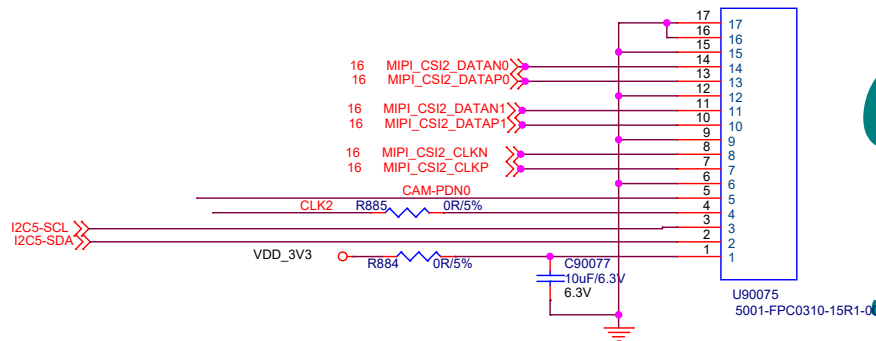
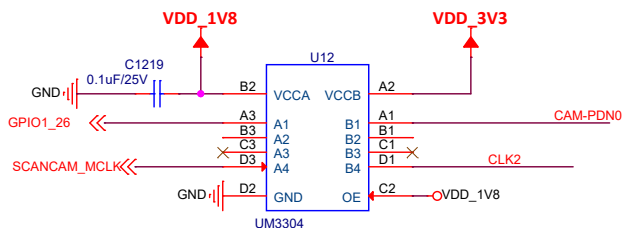
Pull-up to disable PLL @ ALDPS mode.

PHY Address	PHYAD[2:0]
1	001


Project: MV051	
File: Ethernet0	
Date: Monday, February 26, 2024	Rev: X1.0
Designed by: <designer>	Sheet: 7 of 24

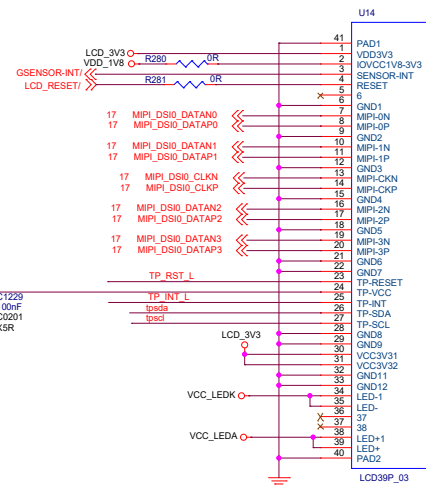
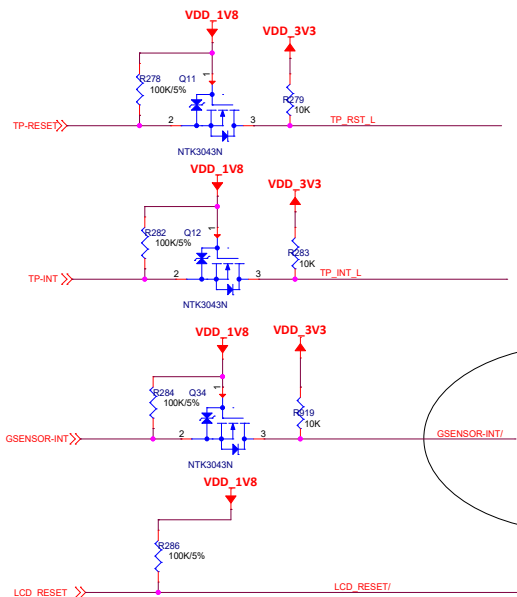
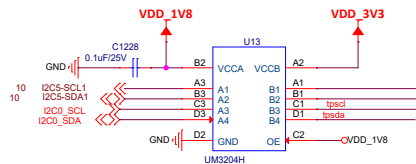


CSI2
1.8V

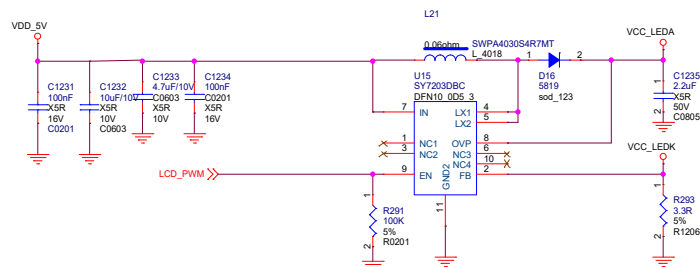
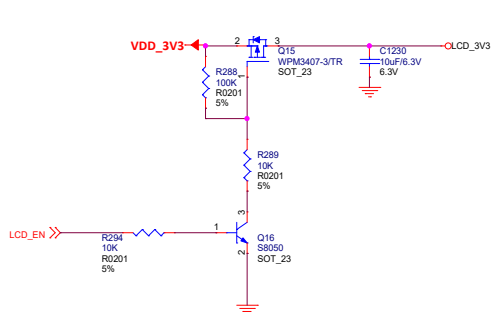


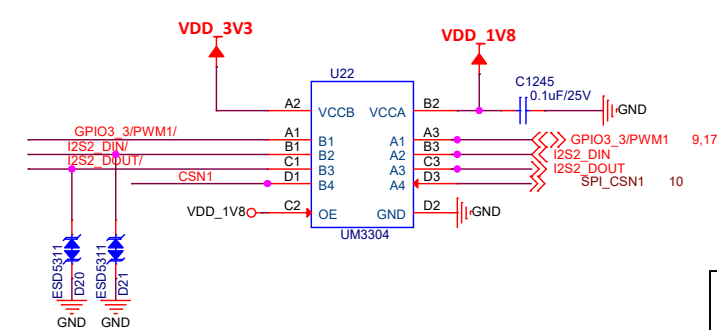
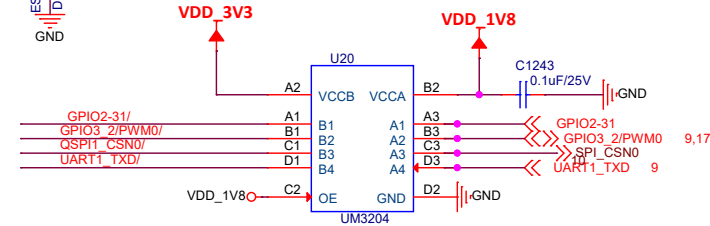
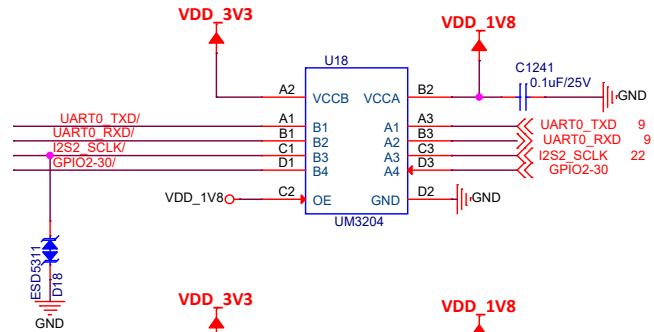
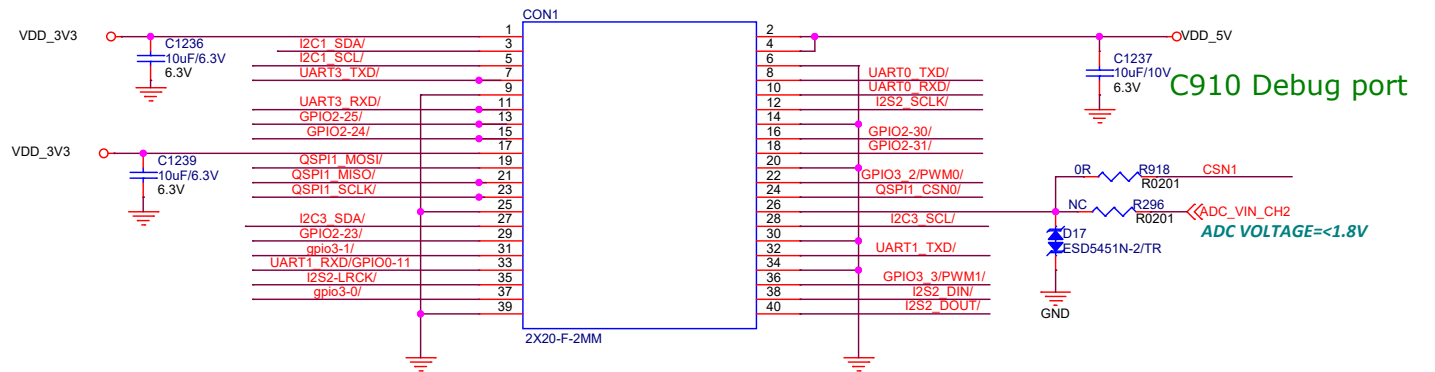
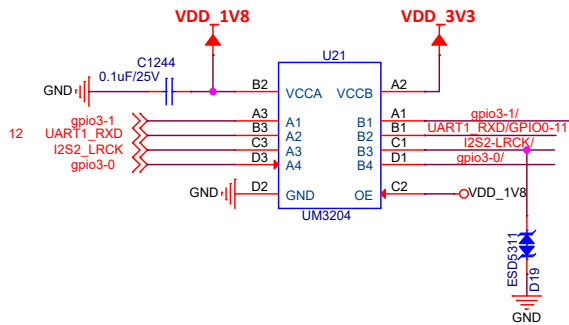
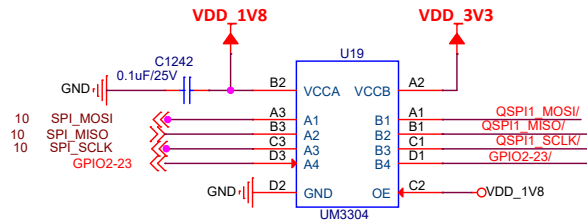
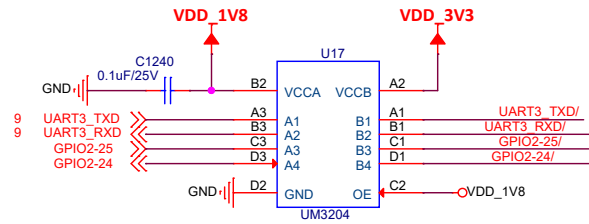
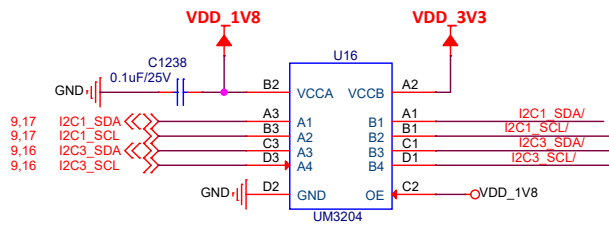
CSI1
3.3V

			
Project:	MV051		
File:	Camera		
Date:	Monday, February 26, 2024	Rev:	X1.0
Designed by:	<designer>	Sheet:	9 of 24



LCD



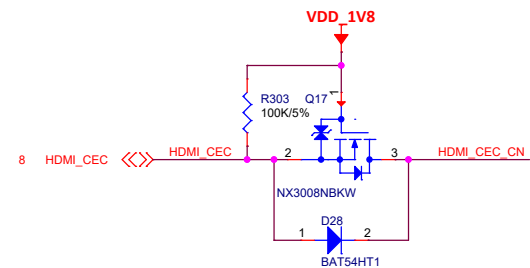
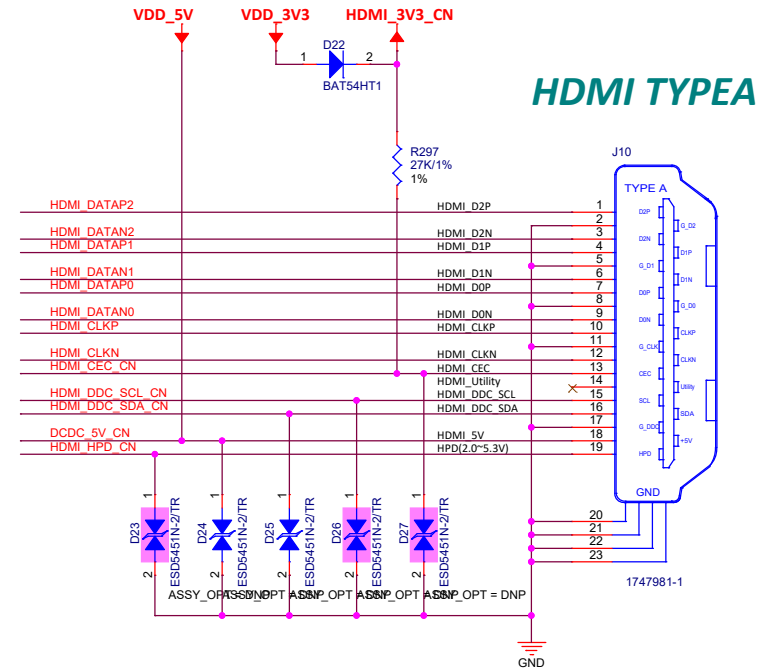
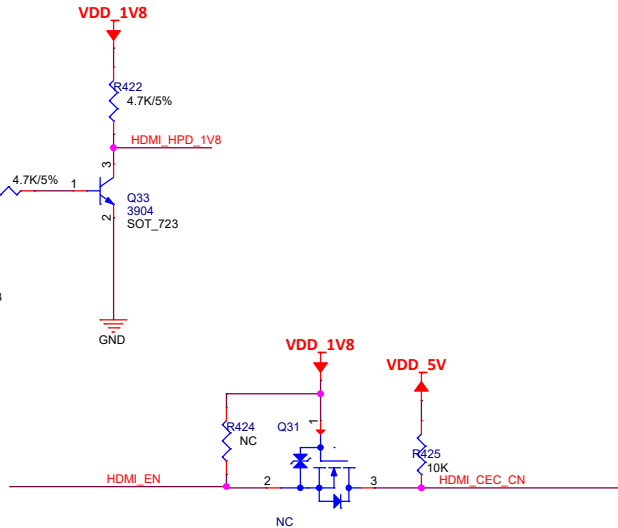
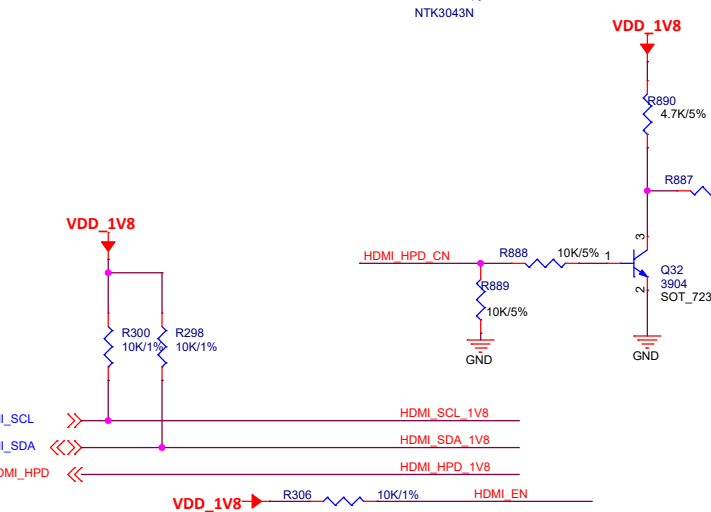
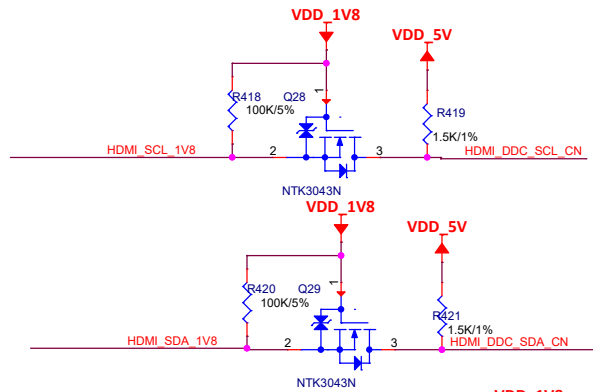
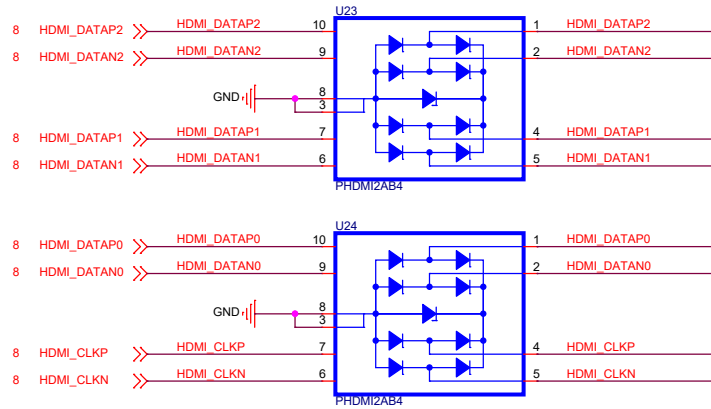


40PIN

			
Project:	MV051		
File:	CONNECTOR		
Date:	Monday, February 26, 2024	Rev:	X1.0
Designed by:	<designer>	Sheet:	11 of 24

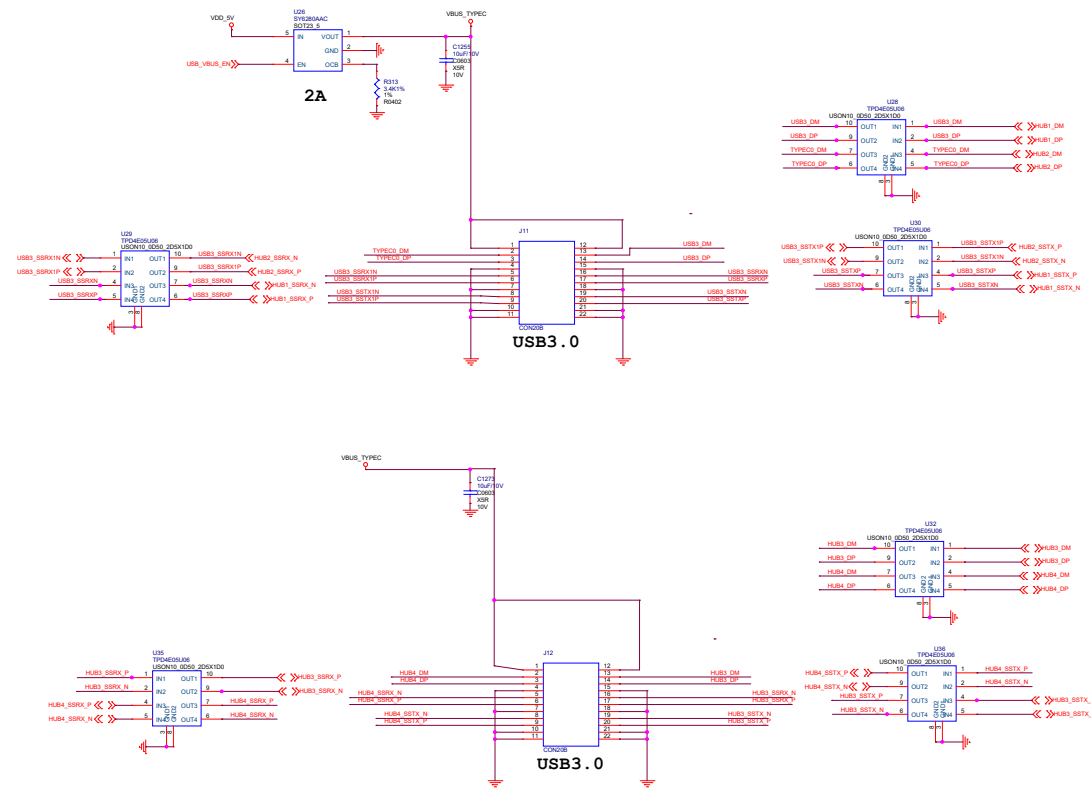
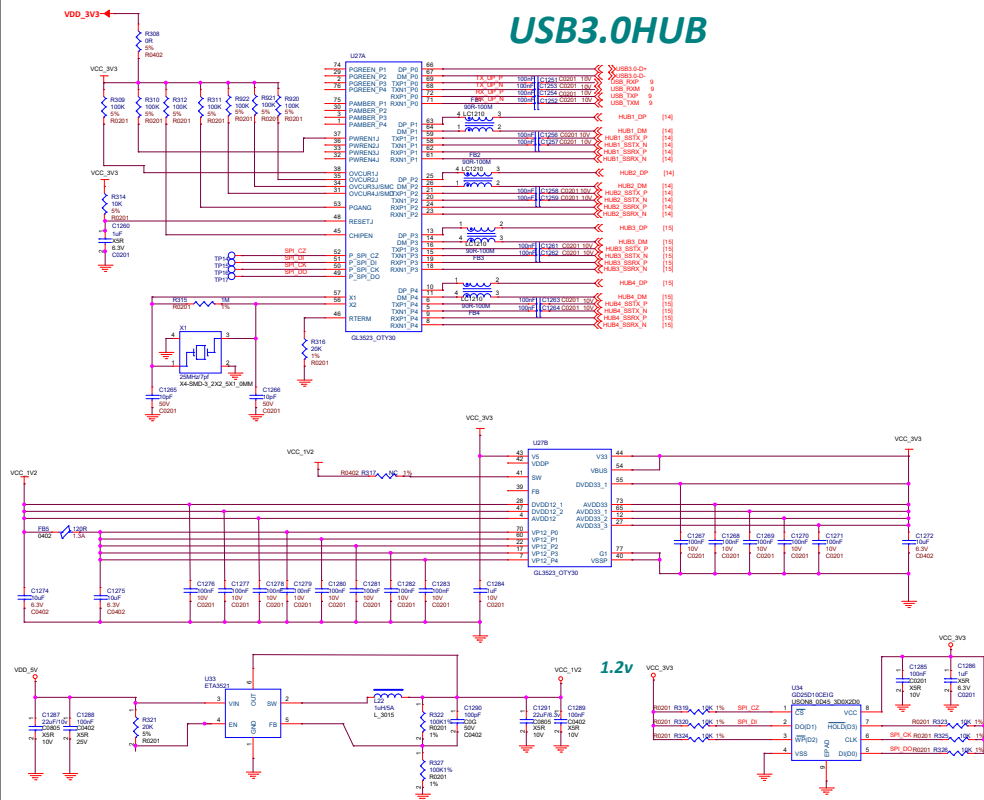
ESD Protection

HDMI Display

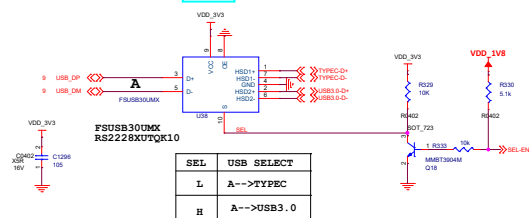


Project: MV051			
File: HDMI Display			
Date: Monday, February 26, 2024	Rev: X1.0		
Designed by: <designer>	Sheet: 12 of 24		

USB3.0HUB

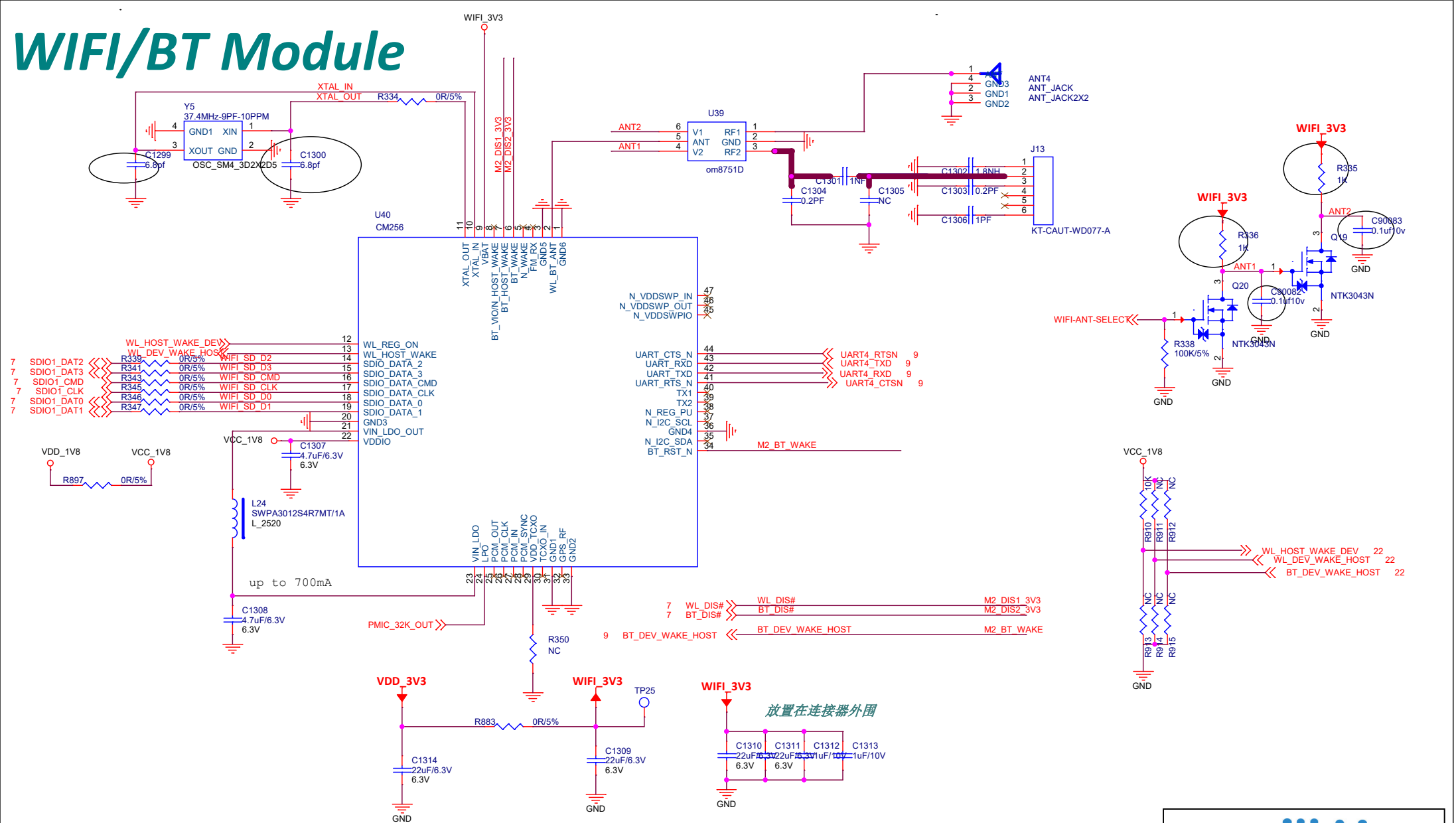


USB_DP DM TYPEC-D+ USB2.0,DOWNLOAD USB3.0HUB

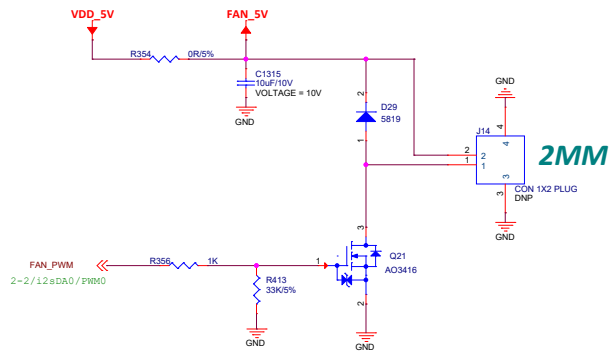


SEL	USB SELECT
L	A-->TYPEC
H	A-->USB3.0

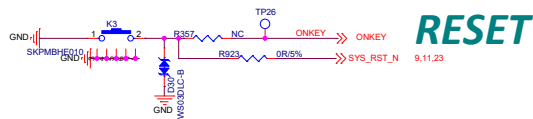
WIFI/BT Module



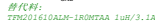
FAN Power Control



BUTTON



FB1P/N should be routed from CPU area. P connects to power, N connects to GND.

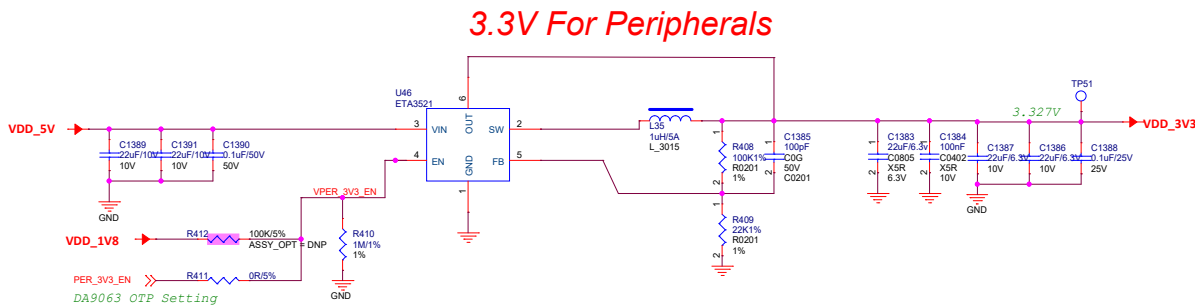
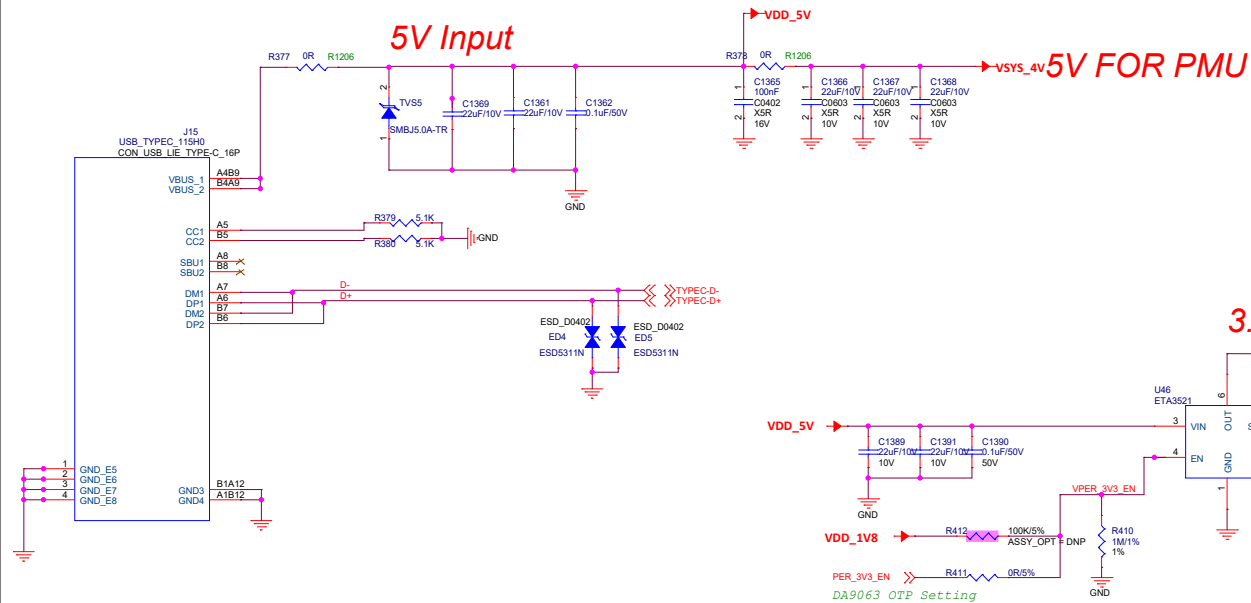


冲程启动上电，屏按长键关机，短键开机

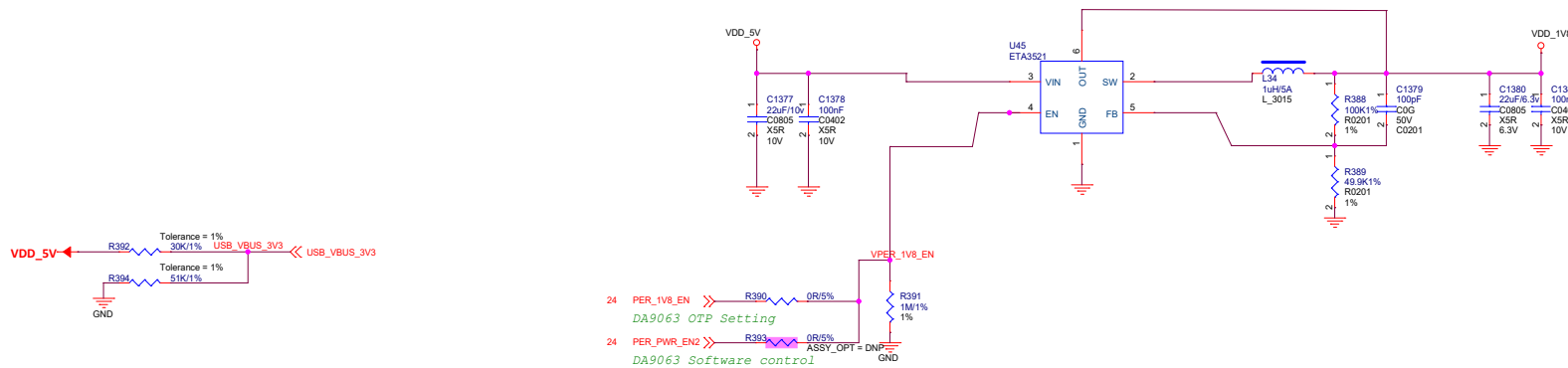
Timing diagram for the DVDD08 power rail. The diagram shows the relationship between the DVDD08_AON, DVDD08_CPU, DVDD08_CPU_MEM, DVDD08_DDR, and DVDD08_DDR_1V8 (VDDQ) signals. The signals are shown as horizontal lines with varying widths and positions, indicating their relative timing and levels. The signals are labeled on the left: PWRon, DVDD08_AON, AVDD03_USB3, DVDD08_AON, DVDD08_CPU, DVDD08_CPU_MEM, DVDD08_DDR, VDDQ_D0R_1V8(VDDQ1), VDDQ_D0R_1V1(DDR_VDDQ), VDDQ_D0R_0V6(DDR_VDDQLP), DVDD08_AP, DVDD08_AP, AVDD08_MIF2_HDMI, DVDD08_MIF2_HDMI, DVDD033_ENMC, DVDD08_ENMC, and RESETn. A 5ms scale bar is shown at the top right.

Time Slot	PMEC Signal	Net Name	Power Supply Name	Default Voltage	Work Status	Standby Status
8	GP10P	VDD_DDR_DV1_EN	VDD_DDR_DV1	1.1V	ON	ON
10	GP1011	PER_V3V_EN	VDD_V3V/VDD_V18	3.18V	ON	ON/OFF
12	GP102	DAP121_EX	DDVD08_AP	0.8V	ON	OFF
13	GP107	DVDD18_EMMC_EN	DVDD18_EMMC	1.8V	ON	ON
NC	GP103	PER_PWR_EN2 (Optional)	VDD_V3V/VDD_V18	3.18V	ON	ON/OFF
NC	GP104	AVDD28_SCAN_EN	AVDD28_SCAN	2.8V	ON/OFF	ON/OFF

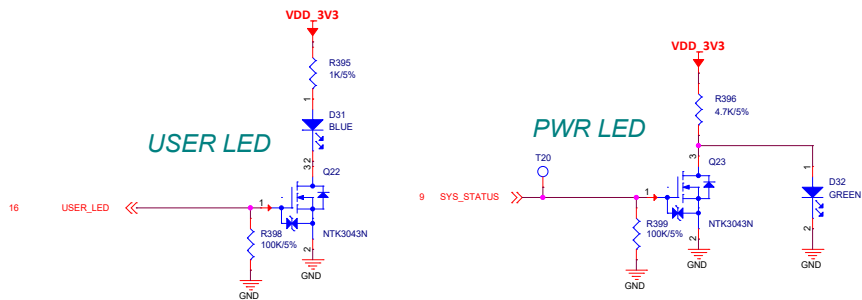
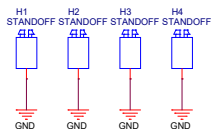
Power Input



1.8V For Peripherals



安装螺柱



Project: MV051	
File: Power Input	
Date: Monday, February 26, 2024	Rev: X1.0
Designed by: <designer>	Sheet: 17 of 24

PINMUX Table

AUDIO PAD SUBSYS PINMUX

PAD NAME	Power Domain	Default	ALT1	ALT2	ALT3	ALT4	ALT5	DEBUG Default	DEBUG ALT1	Reset Condition IN/OUT	Pu/PD	Unused Pin Recommendation
OSC_CLK_IN	DW018_A0M	OSC_CLK_IN								I	N.A.	
OSC_CLK_OUT	DW018_A0M	OSC_CLK_OUT								I	N.A.	
SYS_RST_N	DW018_A0M	SYS_RST_N								I	N.A.	
RTC_CLK_IN	DW018_A0M	RTC_CLK_IN								I	N.A.	
RTC_CLK_OUT	DW018_A0M	RTC_CLK_OUT								I	N.A.	
TEST_MODE	DW018_A0M	TEST_MODE								I	N.A.	
DFT_PROT_DIS_0	DW018_A0M	DFT_PROT_DIS_0								I	N.A.	
DEBUG_MODE	DW018_A0M	DEBUG_MODE								I	N.A.	
I2C_A0N_SCL	DW018_A0M	I2C_A0N_SCL								I	N.A.	
I2C_A0N_SDA	DW018_A0M	I2C_A0N_SDA								I	N.A.	
CRU_JTG_TCLK	DW018_A0M	CRU_JTG_TCLK								I	N.A.	
CRU_JTG_TMS	DW018_A0M	CRU_JTG_TMS								I	N.A.	
CRU_JTG_TDI	DW018_A0M	CRU_JTG_TDI								I	N.A.	
CRU_JTG_TDO	DW018_A0M	CRU_JTG_TDO								I	N.A.	
CRU_JTG_TRST	DW018_A0M	CRU_JTG_TRST								I	N.A.	
ADGMP0_0	DW018_A0M	ADGMP0_0								I	N.A.	
ADGMP0_1	DW018_A0M	ADGMP0_1								I	N.A.	
ADGMP0_2	DW018_A0M	ADGMP0_2								I	N.A.	
ADGMP0_3	DW018_A0M	ADGMP0_3								I	N.A.	
ADGMP0_4	DW018_A0M	ADGMP0_4								I	N.A.	
ADGMP0_5	DW018_A0M	ADGMP0_5								I	N.A.	
ADGMP0_6	DW018_A0M	ADGMP0_6								I	N.A.	
ADGMP0_7	DW018_A0M	ADGMP0_7								I	N.A.	
ADGMP0_8	DW018_A0M	ADGMP0_8								I	N.A.	
ADGMP0_9	DW018_A0M	ADGMP0_9								I	N.A.	
ADGMP0_10	DW018_A0M	ADGMP0_10								I	N.A.	
ADGMP0_11	DW018_A0M	ADGMP0_11								I	N.A.	
ADGMP0_12	DW018_A0M	ADGMP0_12								I	N.A.	
ADGMP0_13	DW018_A0M	ADGMP0_13								I	N.A.	
ADGMP0_14	DW018_A0M	ADGMP0_14								I	N.A.	
ADGMP0_15	DW018_A0M	ADGMP0_15								I	N.A.	
AUDIO_PA0	DW018_A0M	AUDIO_PA0								I	N.A.	
AUDIO_PA1	DW018_A0M	AUDIO_PA1								I	N.A.	
AUDIO_PA2	DW018_A0M	AUDIO_PA2								I	N.A.	
AUDIO_PA3	DW018_A0M	AUDIO_PA3								I	N.A.	
AUDIO_PA4	DW018_A0M	AUDIO_PA4								I	N.A.	
AUDIO_PA5	DW018_A0M	AUDIO_PA5								I	N.A.	
AUDIO_PA6	DW018_A0M	AUDIO_PA6								I	N.A.	
AUDIO_PA7	DW018_A0M	AUDIO_PA7								I	N.A.	
AUDIO_PA8	DW018_A0M	AUDIO_PA8								I	N.A.	
AUDIO_PA9	DW018_A0M	AUDIO_PA9								I	N.A.	
AUDIO_PA10	DW018_A0M	AUDIO_PA10								I	N.A.	
AUDIO_PA11	DW018_A0M	AUDIO_PA11								I	N.A.	
AUDIO_PA12	DW018_A0M	AUDIO_PA12								I	N.A.	
AUDIO_PA13	DW018_A0M	AUDIO_PA13								I	N.A.	
AUDIO_PA14	DW018_A0M	AUDIO_PA14								I	N.A.	
AUDIO_PA15	DW018_A0M	AUDIO_PA15								I	N.A.	
AUDIO_PA16	DW018_A0M	AUDIO_PA16								I	N.A.	
AUDIO_PA17	DW018_A0M	AUDIO_PA17								I	N.A.	
AUDIO_PA18	DW018_A0M	AUDIO_PA18								I	N.A.	
AUDIO_PA19	DW018_A0M	AUDIO_PA19								I	N.A.	
AUDIO_PA20	DW018_A0M	AUDIO_PA20								I	N.A.	
AUDIO_PA21	DW018_A0M	AUDIO_PA21								I	N.A.	
AUDIO_PA22	DW018_A0M	AUDIO_PA22								I	N.A.	
AUDIO_PA23	DW018_A0M	AUDIO_PA23								I	N.A.	
AUDIO_PA24	DW018_A0M	AUDIO_PA24								I	N.A.	
AUDIO_PA25	DW018_A0M	AUDIO_PA25								I	N.A.	
AUDIO_PA26	DW018_A0M	AUDIO_PA26								I	N.A.	
AUDIO_PA27	DW018_A0M	AUDIO_PA27								I	N.A.	
AUDIO_PA28	DW018_A0M	AUDIO_PA28								I	N.A.	
AUDIO_PA29	DW018_A0M	AUDIO_PA29								I	N.A.	
AUDIO_PA30	DW018_A0M	AUDIO_PA30								I	N.A.	
AUDIO_PA31	DW018_A0M	AUDIO_PA31								I	N.A.	
AUDIO_PA32	DW018_A0M	AUDIO_PA32								I	N.A.	
AUDIO_PA33	DW018_A0M	AUDIO_PA33								I	N.A.	
AUDIO_PA34	DW018_A0M	AUDIO_PA34								I	N.A.	
AUDIO_PA35	DW018_A0M	AUDIO_PA35								I	N.A.	
AUDIO_PA36	DW018_A0M	AUDIO_PA36								I	N.A.	
AUDIO_PA37	DW018_A0M	AUDIO_PA37								I	N.A.	
AUDIO_PA38	DW018_A0M	AUDIO_PA38								I	N.A.	
AUDIO_PA39	DW018_A0M	AUDIO_PA39								I	N.A.	
AUDIO_PA40	DW018_A0M	AUDIO_PA40								I	N.A.	
AUDIO_PA41	DW018_A0M	AUDIO_PA41								I	N.A.	
AUDIO_PA42	DW018_A0M	AUDIO_PA42								I	N.A.	
AUDIO_PA43	DW018_A0M	AUDIO_PA43								I	N.A.	
AUDIO_PA44	DW018_A0M	AUDIO_PA44								I	N.A.	
AUDIO_PA45	DW018_A0M	AUDIO_PA45								I	N.A.	
AUDIO_PA46	DW018_A0M	AUDIO_PA46								I	N.A.	
AUDIO_PA47	DW018_A0M	AUDIO_PA47								I	N.A.	
AUDIO_PA48	DW018_A0M	AUDIO_PA48								I	N.A.	
AUDIO_PA49	DW018_A0M	AUDIO_PA49								I	N.A.	
AUDIO_PA50	DW018_A0M	AUDIO_PA50								I	N.A.	
AUDIO_PA51	DW018_A0M	AUDIO_PA51								I	N.A.	
AUDIO_PA52	DW018_A0M	AUDIO_PA52								I	N.A.	
AUDIO_PA53	DW018_A0M	AUDIO_PA53								I	N.A.	
AUDIO_PA54	DW018_A0M	AUDIO_PA54								I	N.A.	
AUDIO_PA55	DW018_A0M	AUDIO_PA55								I	N.A.	
AUDIO_PA56	DW018_A0M	AUDIO_PA56								I	N.A.	
AUDIO_PA57	DW018_A0M	AUDIO_PA57								I	N.A.	
AUDIO_PA58	DW018_A0M	AUDIO_PA58								I	N.A.	
AUDIO_PA59	DW018_A0M	AUDIO_PA59								I	N.A.	
AUDIO_PA60	DW018_A0M	AUDIO_PA60								I	N.A.	
AUDIO_PA61	DW018_A0M	AUDIO_PA61								I	N.A.	
AUDIO_PA62	DW018_A0M	AUDIO_PA62								I	N.A.	
AUDIO_PA63	DW018_A0M	AUDIO_PA63								I	N.A.	
AUDIO_PA64	DW018_A0M	AUDIO_PA64								I	N.A.	
AUDIO_PA65	DW018_A0M	AUDIO_PA65								I	N.A.	
AUDIO_PA66	DW018_A0M	AUDIO_PA66								I	N.A.	
AUDIO_PA67	DW018_A0M	AUDIO_PA67								I	N.A.	
AUDIO_PA68	DW018_A0M	AUDIO_PA68								I	N.A.	
AUDIO_PA69	DW018_A0M	AUDIO_PA69								I	N.A.	
AUDIO_PA70	DW018_A0M	AUDIO_PA70								I	N.A.	
AUDIO_PA71	DW018_A0M	AUDIO_PA71								I	N.A.	
AUDIO_PA72	DW018_A0M	AUDIO_PA72								I	N.A.	
AUDIO_PA73	DW018_A0M	AUDIO_PA73								I	N.A.	
AUDIO_PA74	DW018_A0M	AUDIO_PA74								I	N.A.	
AUDIO_PA75	DW018_A0M	AUDIO_PA75								I	N.A.	
AUDIO_PA76	DW018_A0M	AUDIO_PA76								I	N.A.	
AUDIO_PA77	DW018_A0M	AUDIO_PA77								I	N.A.	
AUDIO_PA78	DW018_A0M	AUDIO_PA78								I	N.A.	
AUDIO_PA79	DW018_A0M	AUDIO_PA79								I	N.A.	
AUDIO_PA80	DW018_A0M	AUDIO_PA80								I	N.A.	
AUDIO_PA81	DW018_A0M	AUDIO_PA81								I	N.A.	
AUDIO_PA82	DW018_A0M	AUDIO_PA82								I	N.A.	
AUDIO_PA83	DW018_A0M	AUDIO_PA83								I	N.A.	
AUDIO_PA84	DW018_A0M	AUDIO_PA84								I	N.A.	
AUDIO_PA85	DW018_A0M	AUDIO_PA85								I	N.A.	
AUDIO_PA86	DW018_A0M	AUDIO_PA86								I	N.A.	
AUDIO_PA87	DW018_A0M	AUDIO_PA87								I	N.A.	
AUDIO_PA88	DW018_A0M	AUDIO_PA88								I	N.A.	
AUDIO_PA89	DW018_A0M	AUDIO_PA89								I	N.A.	
AUDIO_PA90	DW018_A0M	AUDIO_PA90								I	N.A.	
AUDIO_PA91	DW018_A0M	AUDIO_PA91								I	N.A.	
AUDIO_PA92	DW018_A0M	AUDIO_PA92								I	N.A.	
AUDIO_PA93	DW018_A0M	AUDIO_PA93								I	N.A.	
AUDIO_PA94	DW018_A0M	AUDIO_PA94								I	N.A.	
AUDIO_PA95	DW018_A0M	AUDIO_PA95								I	N.A.	
AUDIO_PA96	DW018_A0M	AUDIO_PA96								I	N.A.	
AUDIO_PA97	DW018_A0M	AUDIO_PA97								I	N.A.	
AUDIO_PA98	DW018_A0M	AUDIO_PA98								I	N.A.	
AUDIO_PA99	DW018_A0M	AUDIO_PA99								I	N.A.	
AUDIO_PA100	DW018_A0M	AUDIO_PA100								I	N.A.	
AUDIO_PA101	DW018_A0M	AUDIO_PA101								I	N.A.	
AUDIO_PA102	DW018_A0M	AUDIO_PA102								I	N.A.	
AUDIO_PA103	DW018_A0M	AUDIO_PA103								I	N.A.	
AUDIO_PA104	DW018_A0M	AUDIO_PA104								I	N.A.	
AUDIO_PA105	DW018_A0M	AUDIO_PA105								I	N.A.	
AUDIO_PA106	DW018_A0M	AUDIO_PA106								I	N.A.	
AUDIO_PA107	DW018_A0M	AUDIO_PA107								I	N.A.	
AUDIO_PA108	DW018_A0M	AUDIO_PA108								I	N.A.	
AUDIO_PA109	DW018_A0M	AUDIO_PA109								I	N.A.	
AUDIO_PA110	DW018_A0M	AUDIO_PA110								I	N.A.	
AUDIO_PA111	DW018_A0M	AUDIO_PA111								I	N.A.	
AUDIO_PA112	DW018_A0M	AUDIO_PA112								I	N.A.	
AUDIO_PA113	DW018_A0M	AUDIO_PA113								I	N.A.	
AUDIO_PA114	DW018_A0M	AUDIO_PA114								I	N.A.	
AUDIO_PA115	DW018_A0M	AUDIO_PA115								I	N.A.	
AUDIO_PA116	DW018_A0M	AUDIO_PA116								I	N.A.	
AUDIO_PA117	DW018_A0M	AUDIO_PA117								I	N.A.	
AUDIO_PA118	DW018_A0M	AUDIO_PA118								I	N.A.	
AUDIO_PA119	DW018_A0M	AUDIO_PA119								I	N.A.	
AUDIO_PA120	DW018_A0M	AUDIO_PA120								I	N.A.	
AUDIO_PA121	DW018_A0M	AUDIO_PA121								I	N.A.	
AUDIO_PA122	DW018_A0M	AUDIO_PA122								I	N.A.	
AUDIO_PA123	DW018_A0M	AUDIO_PA123								I	N.A.	
AUDIO_PA124	DW018_A0M	AUDIO_PA124								I	N.A.	
AUDIO_PA125	DW018_A0M	AUDIO_PA125								I	N.A.	
AUDIO_PA126	DW018_A0M	AUDIO_PA126								I		

Audio PAD	ALT1	ALT2	ALT3	ALT4
AUDIO_P0	VAD_DIN0	VAD_PDM_DIN0	SFPOD_DOUT	I2S_RCH_SDA2
AUDIO_P01	VAD_DIN1	VAD_PDM_DIN1	SFPOD_DIN	I2S_RCH_SDA1
AUDIO_P02	VAD_DIN2	VAD_PDM_DIN2	SFPOD_DIN	I2S_RCH_WSCLK
AUDIO_P03	VAD_SCLK	VAD_PDM_CLK	SFPOD_DIN	I2S_RCH_BCLK
AUDIO_P04	VAD_DIN3	VAD_PDM_DIN3	UART_TX	I2S_RCH_SDA2
AUDIO_P05	VAD_DIN4	VAD_PDM_DIN4	UART_RX	I2S_RCH_SDA1
AUDIO_P06	I2C0_DATA	T_AH1_CLK	I2C1_DATA	UART_TX
AUDIO_P07	CLK_WSCLK	T_AH2_CLK	I2S_RCH_MCLK	I2S_RCH_SDA2
AUDIO_P08	I2S0_SCLK	T_AH3_CLK	I2S1_BCLK	I2S1_SDA1
AUDIO_P09	I2S0_MCLK	T_AH4_CLK	TDM_BCLK	I2S1_SDA2
AUDIO_P10	I2S0_MCLK	T_AH5_CLK	UART_TX	I2S1_SDA1
AUDIO_P11	I2S0_MCLK	I2C1_CLK	UART_TX	I2S1_DOUT
AUDIO_P12	I2S0_MCLK	VAD_PDM_DIN0	VAD_DIN0	I2S0_WSCLK
AUDIO_P13	I2S0_MCLK	VAD_PDM_DIN1	VAD_DIN1	I2S0_WSCLK
AUDIO_P14	I2S0_MCLK	VAD_PDM_DIN2	VAD_DIN2	I2S0_WSCLK
AUDIO_P15	I2S1_DIN	VAD_PDM_DIN3	WAD_W5	I2C1_CLK
AUDIO_P16	I2S1_DIN	VAD_PDM_DIN4	WAD_W6	I2C1_CLK
AUDIO_P17	I2S2_WSCLK	TDM_DAT	VAD_DIN2	UART_CTS
AUDIO_P18	I2S2_WSCLK	TDM_DAT	VAD_DIN2	UART_CTS
AUDIO_P19	I2S2_WSCLK	TDM_DAT	TDM_BCLK	UART_CTS
AUDIO_P20	I2S2_MCLK	SFPOD_DIN	SFPOD_DIN	I2C1_DATA
AUDIO_P21	I2S2_MCLK	SFPOD_DIN	SFPOD_DIN	I2C1_CLK
AUDIO_P22	I2S2_DOUT	SFPOD_DOUT	CLK_I2M	
AUDIO_P23	UART_TX	SFPOD_DOUT	SFPOD_DOUT	
AUDIO_P24	UART_RX	SFPOD_DOUT	SFPOD_DOUT	I2S_RCH_MCLK
AUDIO_P25	I2S_RCH_SDA2	SFPOD_DOUT	SFPOD_DOUT	I2C1_DATA
AUDIO_P26	I2S_RCH_SDA1	UART_CTS	SFPOD_DOUT	I2C1_CLK
AUDIO_P27	I2S_RCH_SDA2	SFPOD_DIN	SFPOD_DIN	I2S0_WSCLK
AUDIO_P28	I2S_RCH_BCLK	TDM_BCLK	SFPOD_DOUT	I2S0_BCLK
AUDIO_P29	I2S_RCH_SDA1	TDM_DAT	SFPOD_DOUT	I2S0_BCLK
AUDIO_P30	I2S_RCH_SDA2	I2C0_DATA	I2C0_DATA	I2S0_MCLK