SG2042 Technical Reference Manual

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May 16, 2023

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CHAPTER

ONE

ABSTRACT

SG2042 is server grade chip with high performance, low power consumption and high data throughput

1.1 Key features

- 64 RISC-V cpu cores which implements IMAFDC
- 4 cores per cluster, 16 clusters on chip
- RISC-V vector 0.7
- 2.0GHz CPU frequency
- 64KiB L1 I-Cache and 64KiB L1 D-Cache per core
- 1MiB unified L2 cache per cluster
- 64MiB system level L3 cache
- 512G ops/s for 8bit integer and 256G ops/s for 16bit floating point
- TDP 120W
- 4 DRAM controller, support DDR4 UDIMM/SODIMM/RDIMM up to 3200MT/s with ECC byte
- Max 256GiB DRAM with single chip, 256GiB with dual chips system
- 2 PCIe controller, support PCIe gen4 up to 16GT/s/lan. 32 lans in total.
- 1 1Gbps ethernet RGMII
- 2 eMMC/SDIO, support eMMC 5.1 or SDIO 3.0. 4bit data width
- 2 SPI flash interface
- 1 LPC
- 4 UART
- 4 I2C, support 100K/400K/1M clock frequency
- 2 general SPI controller
- 4 PWM generator for fan control
- 4 Fan speed counter
- 32 GPIO pins
- FCBGA, ball pitch 1mm, package size 57mm x 57mm

CHAPTER

TWO

SYSTEM

2.1 System architecture

SG2042 is a typical NoC(network-on-chip) architecture. All transactions are routed by the router in network. SoC architecture is shown in figure *Mesh architecture*

As you have seen, four CPUs are partitioned into one cluster, totally 16 clusters are connected into the mesh network. Each SLC(System Level Cache) is 4MiB in size totally 16 SLCs are connected. They are shared by all CPUs. Four DRAM controllers locate on the left and right side respectively. They can be accessed by all masters connected on the network.

SG2042 support 2 socket mode through CCIX ports on mesh. Each CCIX port bind to a PCIe controller. CCIX0 bind to PCIe0, CCIX1 bind to PCIe1. Customers can pick each of them for dual socket connection.

PCI device maps bars of PCI devices into SoC address space. PCI master nodes handle requests from PCI devices, like DMA transactions.

SCP(System CoProcessor) is a "out of mesh" CPU subsystem. it has no cache coherence with other CPUs in mesh network. Its responsibility is initilazing basic platform specific devices. Mesh network, DRAM controller, PCIe controller and so on.

2.2 Memory organization

SG2042 implements RISC-V Sv39 virtual address scheme with 40bits physicall addressing ability.

Program memory, data memory, registers and I/O ports are organized within the same linear 1TiB address space.

The bytes are coded in memory in Little Endian format. The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte the most significant.

As SG2042 supports two way CPU technolog. When working at two way mode, the first CPU we naming it as CHIP0, the second CPU we naming it as CHIP1. All resources in CHIP0 are organized within the 512GiB address space(low 39bits). Resources in CHIP1 are organized from 512GiB to 1TiB address space(the most significiant bit of address is 1).

For example, CHIP0 PCIe0 Link0 slave address is located from 0x40_0000_0000 to 0x40_3000_0000. CHIP1 PCIe0 Link0 slave address is located from 0xc0_0000_0000 to 0xc0_3000_0000.

Detailed memory layout is show in table *Memory map*

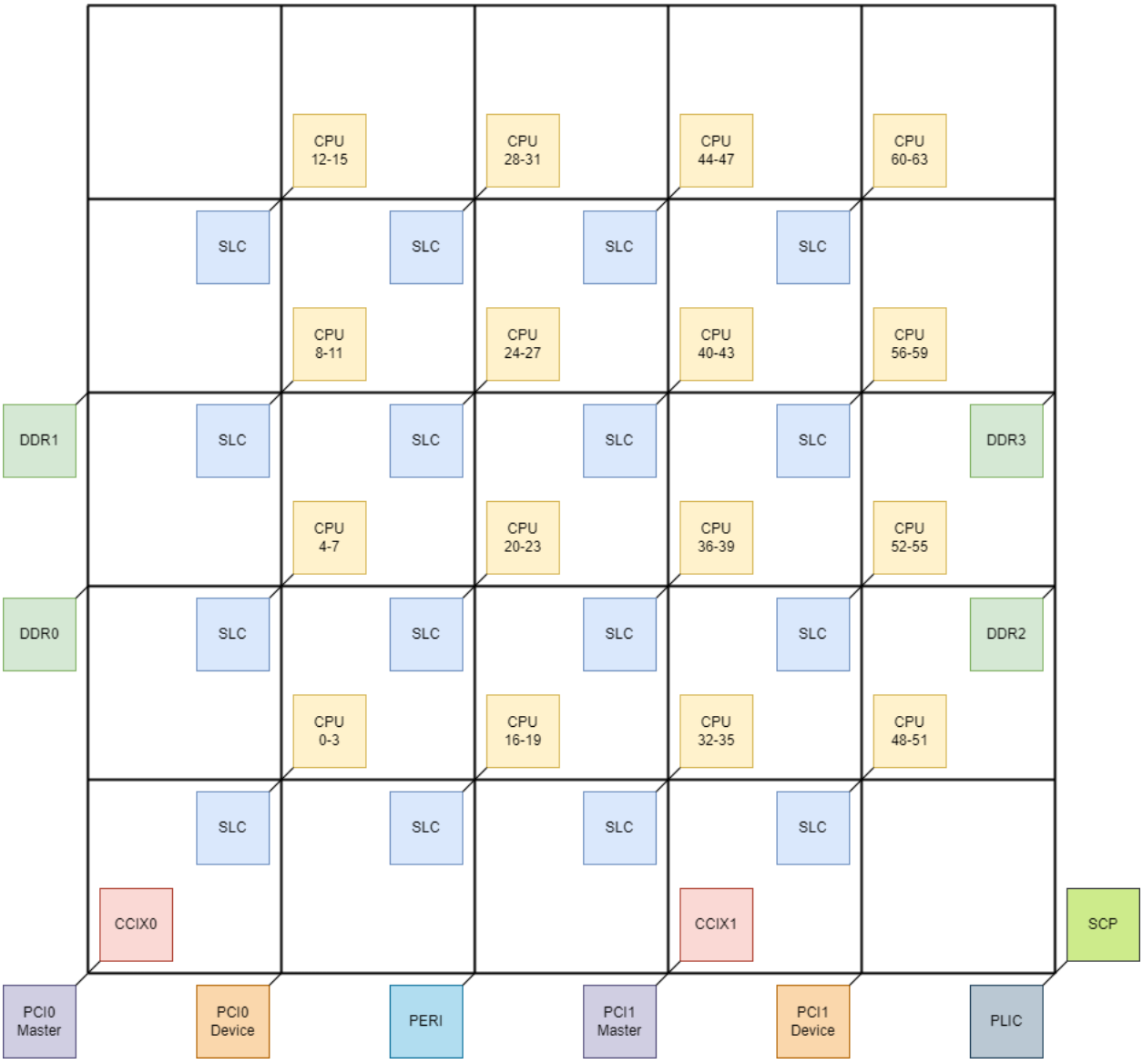

Fig. 1: Mesh architecture

Table 1: Memory map

Start Address	End Address	Devices	Memory Size
000:0000:0000	00F:FFFF:FFFF	DDR0	64G
010:0000:0000	01F:FFFF:FFFF	DDR1	64G
020:0000:0000	02F:FFFF:FFFF	DDR2	64G
030:0000:0000	03F:FFFF:FFFF	DDR3	64G
040:0000:0000	043:FFFF:FFFF	PCIE0_LINK0_SLAVE	16G
044:0000:0000	047:FFFF:FFFF	PCIE0_LINK1_SLAVE	16G
048:0000:0000	04B:FFFF:FFFF	PCIE1_LINK0_SLAVE	16G
04C:0000:0000	04F:FFFF:FFFF	PCIE1_LINK1_SLAVE	16G
070:0014:0000	070:0014:FFFF	SCP_ROM	64K
070:0018:0000	070:0117:FFFF	Serial_Flash0	16M
070:0218:0000	070:0317:FFFF	Serial_Flash1	16M
070:0800:0000	070:0FFF:FFFF	LPC	128M
070:1000:0000	070:100F:FFFF	SRAM0	1M
070:1010:0000	070:101F:FFFF	SRAM1	1M
070:3000:0000	070:3000:0FFF	EFUSE0	4K
070:3000:1000	070:3000:1FFF	EFUSE1	4K
070:3000:2000	070:3000:2FFF	RTC	4K
070:3000:3000	070:3000:3FFF	TIMER	4K
070:3000:4000	070:3000:4FFF	WDT	4K
070:3000:5000	070:3000:5FFF	I2C0	4K
070:3000:6000	070:3000:6FFF	I2C1	4K
070:3000:7000	070:3000:7FFF	I2C2	4K
070:3000:8000	070:3000:8FFF	I2C3	4K
070:3000:9000	070:3000:9FFF	GPIO0	4K
070:3000:A000	070:3000:AFFF	GPIO1	4K
070:3000:B000	070:3000:BFFF	GPIO2	4K
070:3000:C000	070:3000:CFFF	PWM	4K
070:3001:0000	070:3001:7FFF	SYS_CTRL	32K
070:4000:0000	070:4000:0FFF	UART0	4K
070:4000:1000	070:4000:1FFF	UART1	4K
070:4000:2000	070:4000:2FFF	UART2	4K
070:4000:3000	070:4000:3FFF	UART3	4K
070:4000:4000	070:4000:4FFF	SPI0	4K
070:4000:5000	070:4000:5FFF	SPI1	4K
070:4000:6000	070:4001:5FFF	SYS_DMA	64K
070:4001:6000	070:4002:5FFF	HS_DMA	64K
070:4002:6000	070:4002:9FFF	ETH0	16K
070:4002:A000	070:4002:AFFF	EMMC0	4K
070:4002:B000	070:4002:BFFF	EMMC1	4K
070:400A:0000	070:4029:FFFF	TOP_Monitor	2M
070:402A:0000	070:4049:FFFF	HSPERI_Monitor	2M
070:5000:0000	070:51FF:FFFF	DDR0_CFG	32M
070:5200:0000	070:53FF:FFFF	DDR1_CFG	32M
070:5400:0000	070:55FF:FFFF	DDR2_CFG	32M
070:5600:0000	070:57FF:FFFF	DDR3_CFG	32M
070:6000:0000	070:61FF:FFFF	PCIE0_CFG	32M
070:6200:0000	070:63FF:FFFF	PCIE1_CFG	32M
070:7000:0000	070:7FFF:FFFF	MESH	256M
070:9000:0000	070:93FF:FFFF	PLIC	64M

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Table 1 – continued from previous page

Start Address	End Address	Devices	Memory Size
070:9400:0000	070:97FF:FFFF	CLINT_IPI	64M
070:AC00:0000	070:AFFF:FFFF	CLINT_TIMER	64M

2.3 System coprocessor

SG2042 has two CPU subsystem, one is the main 64 cores RISC-V subsystem and the other is system coprocessor(SCP).

After chip power on, system boots from SCP. All RISC-V cores are stay in reset status. SCP will do some platform initialization, then release all 64 RISC-V cores. These platform initializations including:

- Setup PCIe topology. Set PCIe controll to a given mode. Link with PCIe devices.
- Setup DRAM by reading SPD through I2C bus.
- Setup mesh.
- Setup chip to chip CCIX link if dual socket mode is enabled.
- Load RISC-V zero stage bootloader(zsbl.bin)
- Setup RISC-V CPU reset address to where zsbl.bin is loaded.
- Release all RISC-V CPUs, now all CPUs run from zero stage bootloader.

So, RISC-V CPUs donot have a so called bootrom. Zero stage bootloader(zsbl.bin) is the first boot stage of RISC-V CPUs.

2.4 Boot

Boot sequency is controlled by both hardware and software

2.4.1 Power on reset

After power-on reset sequence, SCP reset will be automatically de-asserted by hardware. Customers can select boot devices by pull BOOT_SEL[1] up or down. RISC-V CPUs are asserted remain.

SG2042 provides 8-bit boot strap pins BOOT_SEL[7:0], the usage is shown as table *Boot select*

Table 2: Boot select

Pin	Detect by	Value	Description
BOOT_SEL0	Software	Recommend to 1	0: Disable SD card boot. 1: Try SD card boot first, then try SPI flash boot
BOOT_SEL1	Hard-ware	Recommend to 0	0: Boot from on-chip bootrom. 1: Bootrom from external SPI flash
BOOT_SEL2	Software	Recommend to 0	Eanble SCP console
BOOT_SEL3	Software	Must be 0	Enter system level test mode
BOOT_SEL4-7	Reserved	Must be 0	Reserved, but must be pulled down

When boot from SPI Flash, IO SPIF*_CLK_SEL1 and SPIF*_CLK_SEL0 are used to determine the clock frequency of SPI interface as shown in table *SPI flash clock selection*

Table 3: SPI flash clock selection

SPIx_CLK_SEL1	SPIx_CLK_SEL0	SPI clock frequency
0	0	2.5MHz
0	1	0.5MHz
1	0	10MHz
1	1	25MHz

For SPIx_CLK_SELy, x stands for SPI0 or SPI1, y stands for SEL0 and SEL1.

2.4.2 Bootrom

Bootrom supports loading SCP firmware from SPI flash or SD card.

When booting from SPI flash, bootrom loads SCP firmware from a given offset in flash. When booting from SD card, some restrictions are listed below:

- SD card MUST contain a partition table MBR format.
- The first partition MUST be formated with FAT32 file system.
- SCP firmware MUST be named fip.bin.
- fip.bin MUST be put into the first partition.

Suggest partitioning and formating SD card on linux based PC for compatible considerations. You can do it by following commands (assume your SD card's device file is /dev/sda):

```
$ sudo parted -s /dev/sda -- mklabel msdos mkpart primary fat32 1MiB -1s
$ sudo mkfs.vfat -F32 /dev/sda1
```

2.4.3 SCP firmware

SCP firmware loads RISC-V zero stage bootloader zsbl.bin from SPI or SD card.

SPI flash layout

TODO: add SPI flash layout

SCP firmware load zsbl.bin from the first partition of SD card. zsbl.bin should locate at the root of this partition.

CHAPTER

THREE

PIN MUX

SG2042 pins consist of digital pins, analog pins and power supply pins

3.1 Digital pins

3.1.1 Pin list

Digital pins Digital pins are listed in table *Digital pins*

Table 1: Digital pins

Signal Name	I/O	Voltage	Description	Speed MHz
LPC_LCLK	I	1.8	LPC Host Clock	50
LPC_LFRAME	I	1.8	LPC LFRAME	50
LPC_LAD0	I	1.8	LPC LAD	50
LPC_LAD1	I	1.8	LPC LAD	50
LPC_LAD2	I	1.8	LPC LAD	50
LPC_LAD3	I	1.8	LPC LAD	50
LPC_LDRQ0	I	1.8	LPC Encoded DMA/Bus Master Request	50
LPC_LDRQ1	I	1.8	LPC Encoded DMA/Bus Master Request	50
LPC_SERIRQ	I	1.8	LPC Serialized IRQ	50
LPC_CLKRUN	I	1.8	LPC CLKRUN	50
LPC_LPME	I	1.8	LPC LPME	50
LPC_LPCPD	I	1.8	LPC LPCPD	50
LPC_LSMI	I	1.8	LPC LSMI	50
PCIE0_L0_RESET_X	O	1.8	PCIe0 Link0 Reset	10
PCIE0_L1_RESET_X	O	1.8	PCIE0 Link1 Reset	10
PCIE0_L0_WAKEUP_X	O	1.8	PCIE0 Link0 Wakeup	10
PCIE0_L1_WAKEUP_X	O	1.8	PCIE0 Link1 Wakeup	10
PCIE0_L0_CLKREQ_IN_X	O	1.8	PCIE0 Link0 Clock Req	10
PCIE0_L1_CLKREQ_IN_X	O	1.8	PCIE0 Link1 Clock Req	10
PCIE1_L0_RESET_X	O	1.8	PCIE1 Link0 Reset	10
PCIE1_L1_RESET_X	O	1.8	PCIE1 Link1 Reset	10
PCIE1_L0_WAKEUP_X	O	1.8	PCIE1 Link0 Wakeup	10
PCIE1_L1_WAKEUP_X	O	1.8	PCIE1 Link1 Wakeup	10
PCIE1_L0_CLKREQ_IN_X	O	1.8	PCIE1 Link0 Clock Req	10
PCIE1_L1_CLKREQ_IN_X	O	1.8	PCIE1 Link1 Clock Req	10
SPIF0_CLK_SEL1	I	1.8	SPI0 flash clock select	50
SPIF0_CLK_SEL0	I	1.8	SPI0 flash clock select	50

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Table 1 – continued from previous page

Signal Name	I/O	Voltage	Description	Speed MHz
SPIF0_WP_X	IO	1.8	SPI0 flash Write Protect	50
SPIF0_HOLD_X	IO	1.8	SPI0 flash Hold	50
SPIF0_SDI	IO	1.8	SPI0 flash data input	50
SPIF0_CS_X	O	1.8	SPI0 flash chip select	50
SPIF0_SCK	O	1.8	SPI0 flash clock	50
SPIF0_SDO	IO	1.8	SPI0 flash data output	50
SPIF1_CLK_SEL1	I	1.8	SPI1 flash clock select	50
SPIF1_CLK_SEL0	I	1.8	SPI1 flash clock select	50
SPIF1_WP_X	IO	1.8	SPI1 flash Write Protect	50
SPIF1_HOLD_X	IO	1.8	SPI1 flash Hold	50
SPIF1_SDI	IO	1.8	SPI1 flash data input	50
SPIF1_CS_X	O	1.8	SPI1 flash chip select	50
SPIF1_SCK	O	1.8	SPI1 flash clock	50
SPIF1_SDO	IO	1.8	SPI1 flash data output	50
EMMC_WP	IO	1.8	eMMC write protect signal	50
EMMC_CD_X	IO	1.8	eMMC card detect signal, low active	50
EMMC_RST_X	O	1.8	eMMC card reset signal	50
EMMC_PWR_EN	O	1.8	eMMC card power enable signal	50
SDIO_CD_X	I	1.8	SDIO card detect signal, low active	50
SDIO_WP	I	1.8	SDIO write protect signal	50
SDIO_RST_X	O	1.8	SDIO card reset signal	50
SDIO_PWR_EN	O	1.8	SDIO card power enable signal	50
RGMII0_TXD0	O	1.8	RGMII transmit data	250
RGMII0_TXD1	O	1.8	RGMII transmit data	250
RGMII0_TXD2	O	1.8	RGMII transmit data	250
RGMII0_TXD3	O	1.8	RGMII transmit data	250
RGMII0_TXCTRL	O	1.8	RGMII transmit control	250
RGMII0_RXD0	I	1.8	RGMII receive data	250
RGMII0_RXD1	I	1.8	RGMII receive data	250
RGMII0_RXD2	I	1.8	RGMII receive data	250
RGMII0_RXD3	I	1.8	RGMII receive data	250
RGMII0_RXCTRL	I	1.8	RGMII receive control	250
RGMII0_TXC	O	1.8	RGMII transmit clock	250
RGMII0_RXC	I	1.8	RGMII receive clock	250
RGMII0_REFCLKO	O	1.8	Reference clock output	250
RGMII0_IRQ	I	1.8	Interrupt request from PHY	250
RGMII0_MDC	O	1.8	RGMII management clock	250
RGMII0_MDIO	IO	1.8	RGMII management data IO	250
PWM0	O	1.8	Outputs of PWM0	10
PWM1	O	1.8	Outputs of PWM1	10
PWM2	O	1.8	Outputs of PWM2	10
PWM3	O	1.8	Outputs of PWM3	10
FAN0	IO	1.8	Outputs of FAN0	10
FAN1	IO	1.8	Outputs of FAN1	10
FAN2	IO	1.8	Outputs of FAN2	10
FAN3	IO	1.8	Outputs of FAN3	10
IIC0_SDA	IO	1.8	IIC0 SDA	10
IIC0_SCL	IO	1.8	IIC0 SCL	10
IIC1_SDA	IO	1.8	IIC1 SDA	10

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Table 1 – continued from previous page

Signal Name	I/O	Voltage	Description	Speed MHz
IIC1_SCL	IO	1.8	IIC1 SCL	10
IIC2_SDA	IO	1.8	IIC2 SDA	10
IIC2_SCL	IO	1.8	IIC2 SCL	10
IIC3_SDA	IO	1.8	IIC3 SDA	10
IIC3_SCL	IO	1.8	IIC3 SCL	10
UART0_TX	O	1.8	UART0 transmit data	10
UART0_RX	I	1.8	UART0 receive data	10
UART0_RTS	O	1.8	UART0 RTS	10
UART0_CTS	I	1.8	UART0 CTS	10
UART1_TX	O	1.8	UART1 transmit data	10
UART1_RX	I	1.8	UART1 receive data	10
UART1_RTS	O	1.8	UART1 RTS	10
UART1_CTS	I	1.8	UART1 CTS	10
UART2_TX	IO	1.8	UART2 transmit data	10
UART2_RX	IO	1.8	UART2 receive data	10
UART2_RTS	O	1.8	UART2 RTS	10
UART2_CTS	I	1.8	UART2 CTS	10
UART3_TX	IO	1.8	UART3 transmit data	10
UART3_RX	IO	1.8	UART3 receive data	10
UART3_RTS	O	1.8	UART3 RTS	10
UART3_CTS	I	1.8	UART3 CTS	10
SPI0_CS0_X	O	1.8	SPI0 CS0	50
SPI0_CS1_X	O	1.8	SPI0 CS1	50
SPI0_SDI	I	1.8	SPI0 SDI	50
SPI0_SDO	IO	1.8	SPI0 SDO	50
SPI0_SCK	O	1.8	SPI0 SCK	50
SPI1_CS0_X	O	1.8	SPI1 CS0	50
SPI1_CS1_X	O	1.8	SPI1 CS1	50
SPI1_SDI	I	1.8	SPI1 SDI	50
SPI1_SDO	IO	1.8	SPI1 SDO	50
SPI1_SCK	O	1.8	SPI1 SCK	50
JTAG0_TDO	IO	1.8	JTAG0 TDO	50
JTAG0_TCK	IO	1.8	JTAG0 TCK	50
JTAG0_TDI	IO	1.8	JTAG0 TDI	50
JTAG0_TMS	IO	1.8	JTAG0 TMS	50
JTAG0_TRST_X	IO	1.8	JTAG0 TRST	50
JTAG0_SRST_X	IO	1.8	JTAG0 SRST	50
JTAG1_TDO	IO	1.8	JTAG1 TDO	50
JTAG1_TCK	IO	1.8	JTAG1 TCK	50
JTAG1_TDI	IO	1.8	JTAG1 TDI	50
JTAG1_TMS	IO	1.8	JTAG1 TMS	50
JTAG1_TRST_X	IO	1.8	JTAG1 TRST	50
JTAG1_SRST_X	IO	1.8	JTAG1 SRST	50
JTAG2_TDO	IO	1.8	JTAG2 TDO (for DFT)	50
JTAG2_TCK	IO	1.8	JTAG2 TCK	50
JTAG2_TDI	IO	1.8	JTAG2 TDI	50
JTAG2_TMS	IO	1.8	JTAG2 TMS	50
JTAG2_TRST_X	IO	1.8	JTAG2 TRST	50
JTAG2_SRST_X	IO	1.8	JTAG2 SRST	50

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Table 1 – continued from previous page

Signal Name	I/O	Voltage	Description	Speed MHz
GPIO0	IO	1.8	GPIO0	10
GPIO1	IO	1.8	GPIO1	10
GPIO2	IO	1.8	GPIO2	10
GPIO3	IO	1.8	GPIO3	10
GPIO4	IO	1.8	GPIO4	10
GPIO5	IO	1.8	GPIO5	10
GPIO6	IO	1.8	GPIO6	10
GPIO7	IO	1.8	GPIO7	10
GPIO8	IO	1.8	GPIO8	10
GPIO9	IO	1.8	GPIO9	10
GPIO10	IO	1.8	GPIO10	10
GPIO11	IO	1.8	GPIO11	10
GPIO12	IO	1.8	GPIO12	10
GPIO13	IO	1.8	GPIO13	10
GPIO14	IO	1.8	GPIO14	10
GPIO15	IO	1.8	GPIO15	10
GPIO16	IO	1.8	GPIO16	10
GPIO17	IO	1.8	GPIO17	50
GPIO18	IO	1.8	GPIO18	50
GPIO19	IO	1.8	GPIO19	50
GPIO20	IO	1.8	GPIO20	50
GPIO21	IO	1.8	GPIO21	50
GPIO22	IO	1.8	GPIO22	50
GPIO23	IO	1.8	GPIO23	10
GPIO24	IO	1.8	GPIO24	10
GPIO25	IO	1.8	GPIO25	10
GPIO26	IO	1.8	GPIO26	10
GPIO27	IO	1.8	GPIO27	10
GPIO28	IO	1.8	GPIO28	10
GPIO29	IO	1.8	GPIO29	10
GPIO30	IO	1.8	GPIO30	10
GPIO31	IO	1.8	GPIO31	10
MODE_SEL0	I	1.8	Mode Select0	10
MODE_SEL1	I	1.8	Mode Select1	10
MODE_SEL2	I	1.8	Mode Select2	10
BOOT_SEL0	I	1.8	Boot Select0	10
BOOT_SEL1	I	1.8	Boot Select1	10
BOOT_SEL2	I	1.8	Boot Select2	10
BOOT_SEL3	I	1.8	Boot Select3	10
BOOT_SEL4	I	1.8	Boot Select4	10
BOOT_SEL5	I	1.8	Boot Select5	10
BOOT_SEL6	I	1.8	Boot Select6	10
BOOT_SEL7	I	1.8	Boot Select7	10
MULTI_SCKT	I	1.8	Multi-socket Enable	10
SCKT_ID0	I	1.8	Socket ID0	10
SCKT_ID1	I	1.8	Socket ID1	10
PLL_CLK_IN_MAIN	I	1.8	PLL reference clock input	50
PLL_CLK_IN_DDR_L	I	1.8	DPLL (Left) reference clock input	50
PLL_CLK_IN_DDR_R	I	1.8	DPLL (right) reference clock input	50

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Table 1 – continued from previous page

Signal Name	I/O	Voltage	Description	Speed MHz
XTAL_32K	I	1.8	XTAL 32K clock input	10
SYS_RST_X	I	1.8	System Reset, active-low	10
PWR_BUTTON	I	1.8	System Reset, active-low	10
TEST_EN	I	1.8	TEST Mode Enable	10
TEST_MODE_MBIST	I	1.8	TEST MBIST Mode	10
TEST_MODE_SCAN	I	1.8	TEST Scan Mode	10
TEST_MODE_BSD	I	1.8	TEST BSD Mode	10
BISR_BYP	I	1.8	BISR Bypass	10

3.1.2 Pin function

Most digital pins have multiple functions. Each digital pin can have at most four functions. Pins and functions are listed in table *Digital pin functions*

Table 2: Digital pin functions

Signal Name	Function0	Function1	Function2	Function3
LPC_LCLK	LPC_LCLK(O)	GPIO32(IO)<0>		
LPC_LFRAME	LPC_LFRAME(O)	GPIO33(IO)<0>		
LPC_LAD0	LPC_LAD0(IO)<0>	GPIO34(IO)<0>		
LPC_LAD1	LPC_LAD1(IO)<0>	GPIO35(IO)<0>		
LPC_LAD2	LPC_LAD2(IO)<0>	GPIO36(IO)<0>		
LPC_LAD3	LPC_LAD3(IO)<0>	GPIO37(IO)<0>		
LPC_LDRQ0	LPC_DRQ0(I)<0>	GPIO38(IO)<0>		
LPC_LDRQ1	LPC_DRQ1(I)<0>	GPIO39(IO)<0>		
LPC_SERIRQ	LPC_SERIRQ(IO)<0>	GPIO40(IO)<0>		
LPC_CLKRUN	LPC_CLKRUN(IO)<0>	GPIO41(IO)<0>		
LPC_LPME	LPC_LPME(IO)<0>	GPIO42(IO)<0>		
LPC_LPCPD	LPC_LPCPD(O)	GPIO43(IO)<0>		
LPC_LSMI	LPC_LSMI(I)<0>	GPIO44(IO)<0>		
PCIE0_L0_RESET_X	PCIE0_L0_RESET_X(I)<0>			
PCIE0_L1_RESET_X	PCIE0_L1_RESET_X(I)<0>			
PCIE0_L0_WAKEUP_X	PCIE0_L0_WAKEUP_X(IO)<1>			
PCIE0_L1_WAKEUP_X	PCIE0_L1_WAKEUP_X(IO)<1>			
PCIE0_L0_CLKREQ_IN_X	PCIE0_L0_CLKREQ_IN_X(IO)<1>			
PCIE0_L1_CLKREQ_IN_X	PCIE0_L1_CLKREQ_IN_X(IO)<1>			
PCIE1_L0_RESET_X	PCIE1_L0_RESET_X(I)<0>			
PCIE1_L1_RESET_X	PCIE1_L1_RESET_X(I)<0>			
PCIE1_L0_WAKEUP_X	PCIE1_L0_WAKEUP_X(IO)<1>			
PCIE1_L1_WAKEUP_X	PCIE1_L1_WAKEUP_X(IO)<1>			
PCIE1_L0_CLKREQ_IN_X	PCIE1_L0_CLKREQ_IN_X(IO)<1>			
PCIE1_L1_CLKREQ_IN_X	PCIE1_L1_CLKREQ_IN_X(IO)<1>			
SPIF0_CLK_SEL1	SPIF0_CLK_SEL1(I)<0>			
SPIF0_CLK_SEL0	SPIF0_CLK_SEL0(I)<0>			
SPIF0_WP_X	SPIF0_WP_X(IO)<0>			
SPIF0_HOLD_X	SPIF0_HOLD_X(IO)<0>			
SPIF0_SDI	SPIF0_SDI(IO)<0>			
SPIF0_CS_X	SPIF0_CS_X(O)			
SPIF0_SCK	SPIF0_SCK(O)			

continues on next page

Table 2 – continued from previous page

Signal Name	Function0	Function1	Function2	Function3
SPIF0_SDO	SPIF0_SDO(IO)<0>			
SPIF1_CLK_SEL1	SPIF1_CLK_SEL1(I)<0>			
SPIF1_CLK_SEL0	SPIF1_CLK_SEL0(I)<0>			
SPIF1_WP_X	SPIF1_WP_X(IO)<0>			
SPIF1_HOLD_X	SPIF1_HOLD_X(IO)<0>			
SPIF1_SDI	SPIF1_SDI(IO)<0>			
SPIF1_CS_X	SPIF1_CS_X(O)			
SPIF1_SCK	SPIF1_SCK(O)			
SPIF1_SDO	SPIF1_SDO(IO)<0>			
EMMC_WP	EMMC_WP(I)<1>			
EMMC_CD_X	EMMC_CD_X(I)<1>			
EMMC_RST_X	EMMC_RST_X(O)			
EMMC_PWR_EN	EMMC_PWR_EN(O)			
SDIO_CD_X	SDIO_CD_X(I)<0>			
SDIO_WP	SDIO_WP(I)<0>			
SDIO_RST_X	SDIO_RST_X(O)			
SDIO_PWR_EN	SDIO_PWR_EN(O)			
RGMII0_TXD0	RGMII0_TXD0(O)			
RGMII0_TXD1	RGMII0_TXD1(O)			
RGMII0_TXD2	RGMII0_TXD2(O)			
RGMII0_TXD3	RGMII0_TXD3(O)			
RGMII0_TXCTRL	RGMII0_TXCTRL(O)			
RGMII0_RXD0	RGMII0_RXD0(I)<0>			
RGMII0_RXD1	RGMII0_RXD1(I)<0>			
RGMII0_RXD2	RGMII0_RXD2(I)<0>			
RGMII0_RXD3	RGMII0_RXD3(I)<0>			
RGMII0_RXCTRL	RGMII0_RXCTRL(I)<0>			
RGMII0_TXC	RGMII0_TXC(O)			
RGMII0_RXC	RGMII0_RXC(I)<0>			
RGMII0_REFCLKO	RGMII0_REFCLKO(O)			
RGMII0_IRQ	RGMII0_IRQ(I)<0>			
RGMII0_MDC	RGMII0_MDC(O)			
RGMII0_MDIO	RGMII0_MDIO(IO)<0>			
PWM0	PWM0(O)			
PWM1	PWM1(O)			
PWM2	PWM2(O)	GPIO45(IO)<0>		
PWM3	PWM3(O)	GPIO46(IO)<0>		
FAN0	FAN0(I)<0>			
FAN1	FAN1(I)<0>			
FAN2	FAN2(I)<0>	GPIO47(IO)<0>		
FAN3	FAN3(I)<0>	GPIO48(IO)<0>		
IIC0_SDA	IIC0_SDA(OD)<1>	GPIO49(IO)<0>		
IIC0_SCL	IIC0_SCL(OD)<1>	GPIO50(IO)<0>		
IIC1_SDA	IIC1_SDA(OD)<1>	GPIO51(IO)<0>		
IIC1_SCL	IIC1_SCL(OD)<1>	GPIO52(IO)<0>		
IIC2_SDA	IIC2_SDA(OD)<1>	GPIO53(IO)<0>		
IIC2_SCL	IIC2_SCL(OD)<1>	GPIO54(IO)<0>		
IIC3_SDA	IIC3_SDA(OD)<1>	GPIO55(IO)<0>		
IIC3_SCL	IIC3_SCL(OD)<1>	GPIO56(IO)<0>		

continues on next page

Table 2 – continued from previous page

Signal Name	Function0	Function1	Function2	Function3
UART0_TX	UART0_TX(O)			
UART0_RX	UART0_RX(I)<1>			
UART0_RTS	UART0_RTS(O)	GPIO57(IO)<0>		
UART0_CTS	UART0_CTS(I)<1>	GPIO58(IO)<0>		
UART1_TX	UART1_TX(O)			
UART1_RX	UART1_RX(I)<1>			
UART1_RTS	UART1_RTS(O)	GPIO59(IO)<0>		
UART1_CTS	UART1_CTS(I)<1>	GPIO60(IO)<0>		
UART2_TX	UART2_TX(O)			
UART2_RX	UART2_RX(I)<1>			
UART2_RTS	UART2_RTS(O)	GPIO61(IO)<0>		
UART2_CTS	UART2_CTS(I)<1>	GPIO62(IO)<0>		
UART3_TX	UART3_TX(O)			
UART3_RX	UART3_RX(I)<1>			
UART3_RTS	UART3_RTS(O)	GPIO63(IO)<0>		
UART3_CTS	UART3_CTS(I)<1>	GPIO64(IO)<0>		
SPI0_CS0_X	SPI0_CS0_X(O)	GPIO65(IO)<0>		
SPI0_CS1_X	SPI0_CS1_X(O)	GPIO66(IO)<0>		
SPI0_SDI	SPI0_SDI(I)<0>	GPIO67(IO)<0>		
SPI0_SDO	SPI0_SDO(IO)<0>	GPIO68(IO)<0>		
SPI0_SCK	SPI0_SCK(O)	GPIO69(IO)<0>		
SPI1_CS0_X	SPI1_CS0_X(O)	GPIO70(IO)<0>		
SPI1_CS1_X	SPI1_CS1_X(O)	GPIO71(IO)<0>		
SPI1_SDI	SPI1_SDI(I)<0>	GPIO72(IO)<0>		
SPI1_SDO	SPI1_SDO(IO)<0>	GPIO73(IO)<0>		
SPI1_SCK	SPI1_SCK(O)	GPIO74(IO)<0>		
JTAG0_TDO	JTAG0_TDO(IO)<0>	GPIO75(IO)<0>		
JTAG0_TCK	JTAG0_TCK(I)<0>	GPIO76(IO)<0>		
JTAG0_TDI	JTAG0_TDI(I)<0>	GPIO77(IO)<0>		
JTAG0_TMS	JTAG0_TMS(I)<0>	GPIO78(IO)<0>		
JTAG0_TRST_X	JTAG0_TRST_X(I)<1>	GPIO79(IO)<0>		
JTAG0_SRST_X	JTAG0_SRST_X(I)<1>	GPIO80(IO)<0>		
JTAG1_TDO	JTAG1_TDO(O)	GPIO81(IO)<0>		
JTAG1_TCK	JTAG1_TCK(I)<0>	GPIO82(IO)<0>		
JTAG1_TDI	JTAG1_TDI(I)<0>	GPIO83(IO)<0>		
JTAG1_TMS	JTAG1_TMS(I)<0>	GPIO84(IO)<0>		
JTAG1_TRST_X	JTAG1_TRST_X(I)<1>	GPIO85(IO)<0>		
JTAG1_SRST_X	JTAG1_SRST_X(I)<1>	GPIO86(IO)<0>		
JTAG2_TDO	JTAG2_TDO(O)	GPIO87(IO)<0>		
JTAG2_TCK	JTAG2_TCK(I)<0>	GPIO88(IO)<0>		
JTAG2_TDI	JTAG2_TDI(I)<0>	GPIO89(IO)<0>		
JTAG2_TMS	JTAG2_TMS(I)<0>	GPIO90(IO)<0>		
JTAG2_TRST_X	JTAG2_TRST_X(I)<1>	GPIO91(IO)<0>		
JTAG2_SRST_X	JTAG2_SRST_X(I)<1>	GPIO92(IO)<0>		
GPIO0	GPIO0(IO)<0>		DEBUG_0(O)	
GPIO1	GPIO1(IO)<0>		DEBUG_1(O)	
GPIO2	GPIO2(IO)<0>		DEBUG_2(O)	
GPIO3	GPIO3(IO)<0>		DEBUG_3(O)	
GPIO4	PLL_LOCKO(O)	GPIO4(IO)<0>	DEBUG_4(O)	

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Table 2 – continued from previous page

Signal Name	Function0	Function1	Function2	Function3
GPIO5	GPIO5(IO)<0>		DEBUG_5(O)	
GPIO6	GPIO6(IO)<0>		DEBUG_6(O)	
GPIO7	GPIO7(IO)<0>		DEBUG_7(O)	
GPIO8	GPIO8(IO)<0>		DEBUG_8(O)	
GPIO9	GPIO9(IO)<0>		DEBUG_9(O)	
GPIO10	GPIO10(IO)<0>		DEBUG_10(O)	
GPIO11	GPIO11(IO)<0>		DEBUG_11(O)	
GPIO12	GPIO12(IO)<0>		DEBUG_12(O)	
GPIO13	GPIO13(IO)<0>		DEBUG_13(O)	
GPIO14	GPIO14(IO)<0>		DEBUG_14(O)	
GPIO15	GPIO15(IO)<0>		DEBUG_15(O)	
GPIO16	GPIO16(IO)<0>		DEBUG_16(O)	
GPIO17	GPIO17(IO)<0>		DEBUG_17(O)	
GPIO18	GPIO18(IO)<0>		DEBUG_18(O)	
GPIO19	GPIO19(IO)<0>		DEBUG_19(O)	
GPIO20	GPIO20(IO)<0>		DEBUG_20(O)	
GPIO21	GPIO21(IO)<0>		DEBUG_21(O)	
GPIO22	GPIO22(IO)<0>		DEBUG_22(O)	
GPIO23	GPIO23(IO)<0>		DEBUG_23(O)	
GPIO24	GPIO24(IO)<0>		DEBUG_24(O)	
GPIO25	GPIO25(IO)<0>		DEBUG_25(O)	
GPIO26	GPIO26(IO)<0>		DEBUG_26(O)	
GPIO27	GPIO27(IO)<0>		DEBUG_27(O)	
GPIO28	GPIO28(IO)<0>		DEBUG_28(O)	
GPIO29	DBG_I2C_SCL(OD)<1>	GPIO29(IO)<0>	DEBUG_29(O)	
GPIO30	DBG_I2C_SDA(OD)<1>	GPIO30(IO)<0>	DEBUG_30(O)	
GPIO31	DBG_I2C_SDA_OE(O)	GPIO31(IO)<0>	DEBUG_31(O)	
MODE_SEL0	MODE_SEL0(I)<0>			
MODE_SEL1	MODE_SEL1(I)<0>			
MODE_SEL2	MODE_SEL2(I)<0>			
BOOT_SEL0	BOOT_SEL0(I)<0>			
BOOT_SEL1	BOOT_SEL1(I)<0>			
BOOT_SEL2	BOOT_SEL2(I)<0>			
BOOT_SEL3	BOOT_SEL3(I)<0>			
BOOT_SEL4	BOOT_SEL4(I)<0>			
BOOT_SEL5	BOOT_SEL5(I)<0>			
BOOT_SEL6	BOOT_SEL6(I)<0>			
BOOT_SEL7	BOOT_SEL7(I)<0>			
MULTI_SCKT	MULTI_SCKT(I)<0>			
SCKT_ID0	SCKT_ID0(I)<0>			
SCKT_ID1	SCKT_ID1(I)<0>			
PLL_CLK_IN_MAIN	PLL_CLK_IN_MAIN(I)<0>			
PLL_CLK_IN_DDR_L	PLL_CLK_IN_DDR_L(I)<0>			
PLL_CLK_IN_DDR_R	PLL_CLK_IN_DDR_R(I)<0>			
XTAL_32K	XTAL_32K(I)<0>			
SYS_RST_X	SYS_RST_X(I)<0>			
PWR_BUTTON	PWR_BUTTON(I)<0>			
TEST_EN	TEST_EN(I)<0>			
TEST_MODE_MBIST	TEST_MODE_MBIST(I)<0>			

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Table 2 – continued from previous page

Signal Name	Function0	Function1	Function2	Function3
TEST_MODE_SCAN	TEST_MODE_SCAN(I)<0>			
TEST_MODE_BSD	TEST_MODE_BSD(I)<0>			
BISR_BYP	BISR_BYP(I)<0>			

3.1.3 Registers

Pinmux module controls attributes of pins. These attributes including function, pull up, pull down or no pull, if schmitt trigger is enabled and driving strength.

REG00: offset 0x0000

Table 3: LPC_LCLK and LPC_LFRAME

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for LPC_LFRAME. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for LPC_LFRAME. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for LPC_LFRAME
21:20	RW	0x0	Pin Mux Selector for LPC_LFRAME
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for LPC_LFRAME. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for LPC_LFRAME.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for LPC_LCLK. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for LPC_LCLK. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for LPC_LCLK
5:4	RW	0x0	Pin Mux Selector for LPC_LCLK
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for LPC_LCLK. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for LPC_LCLK.

REG01: offset 0x0004

Table 4: LPC_LAD0 and LPC_LAD1

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for LPC_LAD1. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for LPC_LAD1. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for LPC_LAD1
21:20	RW	0x0	Pin Mux Selector for LPC_LAD1
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for LPC_LAD1. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for LPC_LAD1.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for LPC_LAD0. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for LPC_LAD0. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for LPC_LAD0
5:4	RW	0x0	Pin Mux Selector for LPC_LAD0
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for LPC_LAD0. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for LPC_LAD0.

REG02: offset 0x0008

Table 5: LPC_LAD2 and LPC_LAD3

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for LPC_LAD3. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for LPC_LAD3. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for LPC_LAD3
21:20	RW	0x0	Pin Mux Selector for LPC_LAD3
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for LPC_LAD3. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for LPC_LAD3.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for LPC_LAD2. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for LPC_LAD2. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for LPC_LAD2
5:4	RW	0x0	Pin Mux Selector for LPC_LAD2
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for LPC_LAD2. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for LPC_LAD2.

REG03: offset 0x000c

Table 6: LPC_LDRQ0 and LPC_LDRQ1

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for LPC_LDRQ1. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for LPC_LDRQ1. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for LPC_LDRQ1
21:20	RW	0x0	Pin Mux Selector for LPC_LDRQ1
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for LPC_LDRQ1. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for LPC_LDRQ1.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for LPC_LDRQ0. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for LPC_LDRQ0. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for LPC_LDRQ0
5:4	RW	0x0	Pin Mux Selector for LPC_LDRQ0
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for LPC_LDRQ0. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for LPC_LDRQ0.

REG04: offset 0x0010

Table 7: LPC_SERIRQ and LPC_CLKRUN

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for LPC_CLKRUN. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for LPC_CLKRUN. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for LPC_CLKRUN
21:20	RW	0x0	Pin Mux Selector for LPC_CLKRUN
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for LPC_CLKRUN. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for LPC_CLKRUN.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for LPC_SERIRQ. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for LPC_SERIRQ. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for LPC_SERIRQ
5:4	RW	0x0	Pin Mux Selector for LPC_SERIRQ
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for LPC_SERIRQ. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for LPC_SERIRQ.

REG05: offset 0x0014

Table 8: LPC_LPME and LPC_LPCPD

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for LPC_LPCPD. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for LPC_LPCPD. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for LPC_LPCPD
21:20	RW	0x0	Pin Mux Selector for LPC_LPCPD
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for LPC_LPCPD. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for LPC_LPCPD.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for LPC_LPME. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for LPC_LPME. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for LPC_LPME
5:4	RW	0x0	Pin Mux Selector for LPC_LPME
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for LPC_LPME. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for LPC_LPME.

REG06: offset 0x0018

Table 9: LPC_LSMI and PCIE0_L0_RESET_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for PCIE0_L0_RESET_X. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for PCIE0_L0_RESET_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for PCIE0_L0_RESET_X
21:20	RW	0x0	Pin Mux Selector for PCIE0_L0_RESET_X
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for PCIE0_L0_RESET_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for PCIE0_L0_RESET_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for LPC_LSMI. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for LPC_LSMI. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for LPC_LSMI
5:4	RW	0x0	Pin Mux Selector for LPC_LSMI
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for LPC_LSMI. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for LPC_LSMI.

REG07: offset 0x001c

Table 10: PCIE0_L1_RESET_X and PCIE0_L0_WAKEUP_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for PCIE0_L0_WAKEUP_X. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for PCIE0_L0_WAKEUP_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for PCIE0_L0_WAKEUP_X
21:20	RW	0x0	Pin Mux Selector for PCIE0_L0_WAKEUP_X
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for PCIE0_L0_WAKEUP_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for PCIE0_L0_WAKEUP_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for PCIE0_L1_RESET_X. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for PCIE0_L1_RESET_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for PCIE0_L1_RESET_X
5:4	RW	0x0	Pin Mux Selector for PCIE0_L1_RESET_X
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for PCIE0_L1_RESET_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for PCIE0_L1_RESET_X.

REG08: offset 0x0020

Table 11: PCIE0_L1_WAKEUP_X and PCIE0_L0_CLKREQ_IN_X

Fields	Type	De-fault	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for PCIE0_L0_CLKREQ_IN_X. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for PCIE0_L0_CLKREQ_IN_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for PCIE0_L0_CLKREQ_IN_X
21:20	RW	0x0	Pin Mux Selector for PCIE0_L0_CLKREQ_IN_X
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for PCIE0_L0_CLKREQ_IN_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for PCIE0_L0_CLKREQ_IN_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for PCIE0_L1_WAKEUP_X. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for PCIE0_L1_WAKEUP_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for PCIE0_L1_WAKEUP_X
5:4	RW	0x0	Pin Mux Selector for PCIE0_L1_WAKEUP_X
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for PCIE0_L1_WAKEUP_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for PCIE0_L1_WAKEUP_X.

REG09: offset 0x0024

Table 12: PCIE0_L1_CLKREQ_IN_X and PCIE1_L0_RESET_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for PCIE1_L0_RESET_X. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for PCIE1_L0_RESET_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for PCIE1_L0_RESET_X
21:20	RW	0x0	Pin Mux Selector for PCIE1_L0_RESET_X
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for PCIE1_L0_RESET_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for PCIE1_L0_RESET_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for PCIE0_L1_CLKREQ_IN_X. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for PCIE0_L1_CLKREQ_IN_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for PCIE0_L1_CLKREQ_IN_X
5:4	RW	0x0	Pin Mux Selector for PCIE0_L1_CLKREQ_IN_X
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for PCIE0_L1_CLKREQ_IN_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for PCIE0_L1_CLKREQ_IN_X.

REG0a: offset 0x0028

Table 13: PCIE1_L1_RESET_X and PCIE1_L0_WAKEUP_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for PCIE1_L0_WAKEUP_X. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for PCIE1_L0_WAKEUP_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for PCIE1_L0_WAKEUP_X
21:20	RW	0x0	Pin Mux Selector for PCIE1_L0_WAKEUP_X
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for PCIE1_L0_WAKEUP_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for PCIE1_L0_WAKEUP_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for PCIE1_L1_RESET_X. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for PCIE1_L1_RESET_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for PCIE1_L1_RESET_X
5:4	RW	0x0	Pin Mux Selector for PCIE1_L1_RESET_X
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for PCIE1_L1_RESET_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for PCIE1_L1_RESET_X.

REG0b: offset 0x002c

Table 14: PCIE1_L1_WAKEUP_X and PCIE1_L0_CLKREQ_IN_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for PCIE1_L0_CLKREQ_IN_X. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for PCIE1_L0_CLKREQ_IN_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for PCIE1_L0_CLKREQ_IN_X
21:20	RW	0x0	Pin Mux Selector for PCIE1_L0_CLKREQ_IN_X
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for PCIE1_L0_CLKREQ_IN_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for PCIE1_L0_CLKREQ_IN_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for PCIE1_L1_WAKEUP_X. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for PCIE1_L1_WAKEUP_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for PCIE1_L1_WAKEUP_X
5:4	RW	0x0	Pin Mux Selector for PCIE1_L1_WAKEUP_X
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for PCIE1_L1_WAKEUP_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for PCIE1_L1_WAKEUP_X.

REG0c: offset 0x0030

Table 15: PCIE1_L1_CLKREQ_IN_X and SPIF0_CLK_SEL1

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPIF0_CLK_SEL1. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPIF0_CLK_SEL1. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPIF0_CLK_SEL1
21:20	RW	0x0	Pin Mux Selector for SPIF0_CLK_SEL1
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPIF0_CLK_SEL1. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPIF0_CLK_SEL1.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for PCIE1_L1_CLKREQ_IN_X. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for PCIE1_L1_CLKREQ_IN_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for PCIE1_L1_CLKREQ_IN_X
5:4	RW	0x0	Pin Mux Selector for PCIE1_L1_CLKREQ_IN_X
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for PCIE1_L1_CLKREQ_IN_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for PCIE1_L1_CLKREQ_IN_X.

REG0d: offset 0x0034

Table 16: SPIF0_CLK_SEL0 and SPIF0_WP_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPIF0_WP_X. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPIF0_WP_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPIF0_WP_X
21:20	RW	0x0	Pin Mux Selector for SPIF0_WP_X
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPIF0_WP_X. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPIF0_WP_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPIF0_CLK_SEL0. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPIF0_CLK_SEL0. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPIF0_CLK_SEL0
5:4	RW	0x0	Pin Mux Selector for SPIF0_CLK_SEL0
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPIF0_CLK_SEL0. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPIF0_CLK_SEL0.

REG0e: offset 0x0038

Table 17: SPIF0_HOLD_X and SPIF0_SDI

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPIF0_SDI. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPIF0_SDI. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPIF0_SDI
21:20	RW	0x0	Pin Mux Selector for SPIF0_SDI
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPIF0_SDI. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPIF0_SDI.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPIF0_HOLD_X. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPIF0_HOLD_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPIF0_HOLD_X
5:4	RW	0x0	Pin Mux Selector for SPIF0_HOLD_X
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPIF0_HOLD_X. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPIF0_HOLD_X.

REG0f: offset 0x003c

Table 18: SPIF0_CS_X and SPIF0_SCK

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPIF0_SCK. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPIF0_SCK. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPIF0_SCK
21:20	RW	0x0	Pin Mux Selector for SPIF0_SCK
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPIF0_SCK. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPIF0_SCK.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPIF0_CS_X. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPIF0_CS_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPIF0_CS_X
5:4	RW	0x0	Pin Mux Selector for SPIF0_CS_X
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPIF0_CS_X. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPIF0_CS_X.

REG10: offset 0x0040

Table 19: SPIF0_SDO and SPIF1_CLK_SEL1

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPIF1_CLK_SEL1. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPIF1_CLK_SEL1. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPIF1_CLK_SEL1
21:20	RW	0x0	Pin Mux Selector for SPIF1_CLK_SEL1
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPIF1_CLK_SEL1. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPIF1_CLK_SEL1.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPIF0_SDO. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPIF0_SDO. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPIF0_SDO
5:4	RW	0x0	Pin Mux Selector for SPIF0_SDO
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPIF0_SDO. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPIF0_SDO.

REG11: offset 0x0044

Table 20: SPIF1_CLK_SEL0 and SPIF1_WP_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPIF1_WP_X. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPIF1_WP_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPIF1_WP_X
21:20	RW	0x0	Pin Mux Selector for SPIF1_WP_X
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPIF1_WP_X. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPIF1_WP_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPIF1_CLK_SEL0. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPIF1_CLK_SEL0. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPIF1_CLK_SEL0
5:4	RW	0x0	Pin Mux Selector for SPIF1_CLK_SEL0
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPIF1_CLK_SEL0. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPIF1_CLK_SEL0.

REG12: offset 0x0048

Table 21: SPIF1_HOLD_X and SPIF1_SDI

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPIF1_SDI. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPIF1_SDI. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPIF1_SDI
21:20	RW	0x0	Pin Mux Selector for SPIF1_SDI
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPIF1_SDI. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPIF1_SDI.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPIF1_HOLD_X. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPIF1_HOLD_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPIF1_HOLD_X
5:4	RW	0x0	Pin Mux Selector for SPIF1_HOLD_X
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPIF1_HOLD_X. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPIF1_HOLD_X.

REG13: offset 0x004c

Table 22: SPIF1_CS_X and SPIF1_SCK

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPIF1_SCK. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPIF1_SCK. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPIF1_SCK
21:20	RW	0x0	Pin Mux Selector for SPIF1_SCK
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPIF1_SCK. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPIF1_SCK.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPIF1_CS_X. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPIF1_CS_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPIF1_CS_X
5:4	RW	0x0	Pin Mux Selector for SPIF1_CS_X
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPIF1_CS_X. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPIF1_CS_X.

REG14: offset 0x0050

Table 23: SPIF1_SDO and EMMC_WP

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for EMMC_WP. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for EMMC_WP. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for EMMC_WP
21:20	RW	0x0	Pin Mux Selector for EMMC_WP
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for EMMC_WP. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for EMMC_WP.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPIF1_SDO. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPIF1_SDO. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPIF1_SDO
5:4	RW	0x0	Pin Mux Selector for SPIF1_SDO
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPIF1_SDO. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPIF1_SDO.

REG15: offset 0x0054

Table 24: EMMC_CD_X and EMMC_RST_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for EMMC_RST_X. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for EMMC_RST_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for EMMC_RST_X
21:20	RW	0x0	Pin Mux Selector for EMMC_RST_X
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for EMMC_RST_X. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for EMMC_RST_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for EMMC_CD_X. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for EMMC_CD_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for EMMC_CD_X
5:4	RW	0x0	Pin Mux Selector for EMMC_CD_X
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for EMMC_CD_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for EMMC_CD_X.

REG16: offset 0x0058

Table 25: EMMC_PWR_EN and SDIO_CD_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SDIO_CD_X. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for SDIO_CD_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SDIO_CD_X
21:20	RW	0x0	Pin Mux Selector for SDIO_CD_X
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for SDIO_CD_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for SDIO_CD_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for EMMC_PWR_EN. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for EMMC_PWR_EN. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for EMMC_PWR_EN
5:4	RW	0x0	Pin Mux Selector for EMMC_PWR_EN
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for EMMC_PWR_EN. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for EMMC_PWR_EN.

REG17: offset 0x005c

Table 26: SDIO_WP and SDIO_RST_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SDIO_RST_X. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SDIO_RST_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SDIO_RST_X
21:20	RW	0x0	Pin Mux Selector for SDIO_RST_X
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SDIO_RST_X. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SDIO_RST_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SDIO_WP. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for SDIO_WP. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SDIO_WP
5:4	RW	0x0	Pin Mux Selector for SDIO_WP
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SDIO_WP. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SDIO_WP.

REG18: offset 0x0060

Table 27: SDIO_PWR_EN and RGMII0_TXD0

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for RGMII0_TXD0. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for RGMII0_TXD0. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for RGMII0_TXD0
21:20	RW	0x0	Pin Mux Selector for RGMII0_TXD0
19	RW	0x0	Pull Down Enable for RGMII0_TXD0
18	RW	0x0	Pull Up Enable for RGMII0_TXD0
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SDIO_PWR_EN. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SDIO_PWR_EN. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SDIO_PWR_EN
5:4	RW	0x0	Pin Mux Selector for SDIO_PWR_EN
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SDIO_PWR_EN. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SDIO_PWR_EN.

REG19: offset 0x0064

Table 28: RGMII0_TXD1 and RGMII0_TXD2

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for RGMII0_TXD2. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for RGMII0_TXD2. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for RGMII0_TXD2
21:20	RW	0x0	Pin Mux Selector for RGMII0_TXD2
19	RW	0x0	Pull Down Enable for RGMII0_TXD2
18	RW	0x0	Pull Up Enable for RGMII0_TXD2
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for RGMII0_TXD1. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for RGMII0_TXD1. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for RGMII0_TXD1
5:4	RW	0x0	Pin Mux Selector for RGMII0_TXD1
3	RW	0x0	Pull Down Enable for RGMII0_TXD1
2	RW	0x0	Pull Up Enable for RGMII0_TXD1
1:0	RW	NA	Reserved

REG1a: offset 0x0068

Table 29: RGMII0_TXD3 and RGMII0_TXCTRL

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for RGMII0_TXCTRL. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for RGMII0_TXCTRL. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for RGMII0_TXCTRL
21:20	RW	0x0	Pin Mux Selector for RGMII0_TXCTRL
19	RW	0x0	Pull Down Enable for RGMII0_TXCTRL
18	RW	0x0	Pull Up Enable for RGMII0_TXCTRL
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for RGMII0_TXD3. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for RGMII0_TXD3. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for RGMII0_TXD3
5:4	RW	0x0	Pin Mux Selector for RGMII0_TXD3
3	RW	0x0	Pull Down Enable for RGMII0_TXD3
2	RW	0x0	Pull Up Enable for RGMII0_TXD3
1:0	RW	NA	Reserved

REG1b: offset 0x006c

Table 30: RGMII0_RXD0 and RGMII0_RXD1

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for RGMII0_RXD1. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for RGMII0_RXD1. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for RGMII0_RXD1
21:20	RW	0x0	Pin Mux Selector for RGMII0_RXD1
19	RW	0x0	Pull Down Enable for RGMII0_RXD1
18	RW	0x0	Pull Up Enable for RGMII0_RXD1
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for RGMII0_RXD0. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for RGMII0_RXD0. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for RGMII0_RXD0
5:4	RW	0x0	Pin Mux Selector for RGMII0_RXD0
3	RW	0x0	Pull Down Enable for RGMII0_RXD0
2	RW	0x0	Pull Up Enable for RGMII0_RXD0
1:0	RW	NA	Reserved

REG1c: offset 0x0070

Table 31: RGMII0_RXD2 and RGMII0_RXD3

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for RGMII0_RXD3. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for RGMII0_RXD3. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for RGMII0_RXD3
21:20	RW	0x0	Pin Mux Selector for RGMII0_RXD3
19	RW	0x0	Pull Down Enable for RGMII0_RXD3
18	RW	0x0	Pull Up Enable for RGMII0_RXD3
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for RGMII0_RXD2. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for RGMII0_RXD2. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for RGMII0_RXD2
5:4	RW	0x0	Pin Mux Selector for RGMII0_RXD2
3	RW	0x0	Pull Down Enable for RGMII0_RXD2
2	RW	0x0	Pull Up Enable for RGMII0_RXD2
1:0	RW	NA	Reserved

REG1d: offset 0x0074

Table 32: RGMII0_RXCTRL and RGMII0_TXC

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for RGMII0_TXC. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for RGMII0_TXC. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for RGMII0_TXC
21:20	RW	0x0	Pin Mux Selector for RGMII0_TXC
19	RW	0x0	Pull Down Enable for RGMII0_TXC
18	RW	0x0	Pull Up Enable for RGMII0_TXC
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for RGMII0_RXCTRL. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for RGMII0_RXCTRL. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for RGMII0_RXCTRL
5:4	RW	0x0	Pin Mux Selector for RGMII0_RXCTRL
3	RW	0x0	Pull Down Enable for RGMII0_RXCTRL
2	RW	0x0	Pull Up Enable for RGMII0_RXCTRL
1:0	RW	NA	Reserved

REG1e: offset 0x0078

Table 33: RGMII0_RXC and RGMII0_REFCLKO

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for RGMII0_REFCLKO. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for RGMII0_REFCLKO. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for RGMII0_REFCLKO
21:20	RW	0x0	Pin Mux Selector for RGMII0_REFCLKO
19	RW	0x0	Pull Down Enable for RGMII0_REFCLKO
18	RW	0x0	Pull Up Enable for RGMII0_REFCLKO
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for RGMII0_RXC. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for RGMII0_RXC. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for RGMII0_RXC
5:4	RW	0x0	Pin Mux Selector for RGMII0_RXC
3	RW	0x0	Pull Down Enable for RGMII0_RXC
2	RW	0x0	Pull Up Enable for RGMII0_RXC
1:0	RW	NA	Reserved

REG1f: offset 0x007c

Table 34: RGMII0_IRQ and RGMII0_MDC

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for RGMII0_MDC. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for RGMII0_MDC. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for RGMII0_MDC
21:20	RW	0x0	Pin Mux Selector for RGMII0_MDC
19	RW	0x0	Pull Down Enable for RGMII0_MDC
18	RW	0x0	Pull Up Enable for RGMII0_MDC
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for RGMII0_IRQ. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for RGMII0_IRQ. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for RGMII0_IRQ
5:4	RW	0x0	Pin Mux Selector for RGMII0_IRQ
3	RW	0x0	Pull Down Enable for RGMII0_IRQ
2	RW	0x0	Pull Up Enable for RGMII0_IRQ
1:0	RW	NA	Reserved

REG20: offset 0x0080

Table 35: RGMII0_MDIO and PWM0

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for PWM0. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for PWM0. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for PWM0
21:20	RW	0x0	Pin Mux Selector for PWM0
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for PWM0. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for PWM0.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for RGMII0_MDIO. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for RGMII0_MDIO. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for RGMII0_MDIO
5:4	RW	0x0	Pin Mux Selector for RGMII0_MDIO
3	RW	0x0	Pull Down Enable for RGMII0_MDIO
2	RW	0x0	Pull Up Enable for RGMII0_MDIO
1:0	RW	NA	Reserved

REG21: offset 0x0084

Table 36: PWM1 and PWM2

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for PWM2. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for PWM2. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for PWM2
21:20	RW	0x0	Pin Mux Selector for PWM2
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for PWM2. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for PWM2.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for PWM1. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for PWM1. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for PWM1
5:4	RW	0x0	Pin Mux Selector for PWM1
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for PWM1. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for PWM1.

REG22: offset 0x0088

Table 37: PWM3 and FAN0

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for FAN0. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for FAN0. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for FAN0
21:20	RW	0x0	Pin Mux Selector for FAN0
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for FAN0. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for FAN0.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for PWM3. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for PWM3. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for PWM3
5:4	RW	0x0	Pin Mux Selector for PWM3
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for PWM3. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for PWM3.

REG23: offset 0x008c

Table 38: FAN1 and FAN2

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for FAN2. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for FAN2. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for FAN2
21:20	RW	0x0	Pin Mux Selector for FAN2
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for FAN2. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for FAN2.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for FAN1. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for FAN1. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for FAN1
5:4	RW	0x0	Pin Mux Selector for FAN1
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for FAN1. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for FAN1.

REG24: offset 0x0090

Table 39: FAN3 and IIC0_SDA

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for IIC0_SDA. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for IIC0_SDA. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for IIC0_SDA
21:20	RW	0x0	Pin Mux Selector for IIC0_SDA
19	RW	0x0	Pull Down Enable for IIC0_SDA
18	RW	0x0	Pull Up Enable for IIC0_SDA
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for FAN3. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for FAN3. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for FAN3
5:4	RW	0x0	Pin Mux Selector for FAN3
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for FAN3. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for FAN3.

REG25: offset 0x0094

Table 40: IIC0_SCL and IIC1_SDA

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for IIC1_SDA. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for IIC1_SDA. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for IIC1_SDA
21:20	RW	0x0	Pin Mux Selector for IIC1_SDA
19	RW	0x0	Pull Down Enable for IIC1_SDA
18	RW	0x0	Pull Up Enable for IIC1_SDA
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for IIC0_SCL. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for IIC0_SCL. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for IIC0_SCL
5:4	RW	0x0	Pin Mux Selector for IIC0_SCL
3	RW	0x0	Pull Down Enable for IIC0_SCL
2	RW	0x0	Pull Up Enable for IIC0_SCL
1:0	RW	NA	Reserved

REG26: offset 0x0098

Table 41: IIC1_SCL and IIC2_SDA

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for IIC2_SDA. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for IIC2_SDA. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for IIC2_SDA
21:20	RW	0x0	Pin Mux Selector for IIC2_SDA
19	RW	0x0	Pull Down Enable for IIC2_SDA
18	RW	0x0	Pull Up Enable for IIC2_SDA
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for IIC1_SCL. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for IIC1_SCL. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for IIC1_SCL
5:4	RW	0x0	Pin Mux Selector for IIC1_SCL
3	RW	0x0	Pull Down Enable for IIC1_SCL
2	RW	0x0	Pull Up Enable for IIC1_SCL
1:0	RW	NA	Reserved

REG27: offset 0x009c

Table 42: IIC2_SCL and IIC3_SDA

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for IIC3_SDA. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for IIC3_SDA. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for IIC3_SDA
21:20	RW	0x0	Pin Mux Selector for IIC3_SDA
19	RW	0x0	Pull Down Enable for IIC3_SDA
18	RW	0x0	Pull Up Enable for IIC3_SDA
17:16	RW	NA	Reserved
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for IIC2_SCL. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for IIC2_SCL. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for IIC2_SCL
5:4	RW	0x0	Pin Mux Selector for IIC2_SCL
3	RW	0x0	Pull Down Enable for IIC2_SCL
2	RW	0x0	Pull Up Enable for IIC2_SCL
1:0	RW	NA	Reserved

REG28: offset 0x00a0

Table 43: IIC3_SCL and UART0_TX

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for UART0_TX. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for UART0_TX. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for UART0_TX
21:20	RW	0x0	Pin Mux Selector for UART0_TX
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for UART0_TX. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for UART0_TX.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for IIC3_SCL. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for IIC3_SCL. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for IIC3_SCL
5:4	RW	0x0	Pin Mux Selector for IIC3_SCL
3	RW	0x0	Pull Down Enable for IIC3_SCL
2	RW	0x0	Pull Up Enable for IIC3_SCL
1:0	RW	NA	Reserved

REG29: offset 0x00a4

Table 44: UART0_RX and UART0_RTS

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for UART0_RTS. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for UART0_RTS. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for UART0_RTS
21:20	RW	0x0	Pin Mux Selector for UART0_RTS
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for UART0_RTS. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for UART0_RTS.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for UART0_RX. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for UART0_RX. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for UART0_RX
5:4	RW	0x0	Pin Mux Selector for UART0_RX
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for UART0_RX. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for UART0_RX.

REG2a: offset 0x00a8

Table 45: UART0_CTS and UART1_TX

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for UART1_TX. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for UART1_TX. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for UART1_TX
21:20	RW	0x0	Pin Mux Selector for UART1_TX
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for UART1_TX. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for UART1_TX.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for UART0_CTS. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for UART0_CTS. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for UART0_CTS
5:4	RW	0x0	Pin Mux Selector for UART0_CTS
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for UART0_CTS. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for UART0_CTS.

REG2b: offset 0x00ac

Table 46: UART1_RX and UART1_RTS

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for UART1_RTS. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for UART1_RTS. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for UART1_RTS
21:20	RW	0x0	Pin Mux Selector for UART1_RTS
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for UART1_RTS. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for UART1_RTS.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for UART1_RX. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for UART1_RX. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for UART1_RX
5:4	RW	0x0	Pin Mux Selector for UART1_RX
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for UART1_RX. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for UART1_RX.

REG2c: offset 0x00b0

Table 47: UART1_CTS and UART2_TX

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for UART2_TX. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for UART2_TX. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for UART2_TX
21:20	RW	0x0	Pin Mux Selector for UART2_TX
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for UART2_TX. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for UART2_TX.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for UART1_CTS. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for UART1_CTS. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for UART1_CTS
5:4	RW	0x0	Pin Mux Selector for UART1_CTS
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for UART1_CTS. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for UART1_CTS.

REG2d: offset 0x00b4

Table 48: UART2_RX and UART2_RTS

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for UART2_RTS. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for UART2_RTS. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for UART2_RTS
21:20	RW	0x0	Pin Mux Selector for UART2_RTS
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for UART2_RTS. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for UART2_RTS.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for UART2_RX. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for UART2_RX. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for UART2_RX
5:4	RW	0x0	Pin Mux Selector for UART2_RX
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for UART2_RX. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for UART2_RX.

REG2e: offset 0x00b8

Table 49: UART2_CTS and UART3_TX

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for UART3_TX. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for UART3_TX. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for UART3_TX
21:20	RW	0x0	Pin Mux Selector for UART3_TX
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for UART3_TX. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for UART3_TX.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for UART2_CTS. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for UART2_CTS. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for UART2_CTS
5:4	RW	0x0	Pin Mux Selector for UART2_CTS
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for UART2_CTS. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for UART2_CTS.

REG2f: offset 0x00bc

Table 50: UART3_RX and UART3_RTS

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for UART3_RTS. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for UART3_RTS. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for UART3_RTS
21:20	RW	0x0	Pin Mux Selector for UART3_RTS
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for UART3_RTS. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for UART3_RTS.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for UART3_RX. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for UART3_RX. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for UART3_RX
5:4	RW	0x0	Pin Mux Selector for UART3_RX
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for UART3_RX. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for UART3_RX.

REG30: offset 0x00c0

Table 51: UART3_CTS and SPI0_CS0_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPI0_CS0_X. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPI0_CS0_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPI0_CS0_X
21:20	RW	0x0	Pin Mux Selector for SPI0_CS0_X
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPI0_CS0_X. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPI0_CS0_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for UART3_CTS. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for UART3_CTS. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for UART3_CTS
5:4	RW	0x0	Pin Mux Selector for UART3_CTS
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for UART3_CTS. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for UART3_CTS.

REG31: offset 0x00c4

Table 52: SPI0_CS1_X and SPI0_SDI

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPI0_SDI. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for SPI0_SDI. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPI0_SDI
21:20	RW	0x0	Pin Mux Selector for SPI0_SDI
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPI0_SDI. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPI0_SDI.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPI0_CS1_X. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for SPI0_CS1_X. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPI0_CS1_X
5:4	RW	0x0	Pin Mux Selector for SPI0_CS1_X
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPI0_CS1_X. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPI0_CS1_X.

REG32: offset 0x00c8

Table 53: SPI0_SDO and SPI0_SCK

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPI0_SCK. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for SPI0_SCK. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPI0_SCK
21:20	RW	0x0	Pin Mux Selector for SPI0_SCK
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPI0_SCK. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPI0_SCK.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPI0_SDO. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for SPI0_SDO. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPI0_SDO
5:4	RW	0x0	Pin Mux Selector for SPI0_SDO
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPI0_SDO. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPI0_SDO.

REG33: offset 0x00cc

Table 54: SPI1_CS0_X and SPI1_CS1_X

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPI1_CS1_X. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPI1_CS1_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPI1_CS1_X
21:20	RW	0x0	Pin Mux Selector for SPI1_CS1_X
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPI1_CS1_X. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPI1_CS1_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPI1_CS0_X. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPI1_CS0_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPI1_CS0_X
5:4	RW	0x0	Pin Mux Selector for SPI1_CS0_X
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPI1_CS0_X. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPI1_CS0_X.

REG34: offset 0x00d0

Table 55: SPI1_SDI and SPI1_SDO

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for SPI1_SDO. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for SPI1_SDO. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for SPI1_SDO
21:20	RW	0x0	Pin Mux Selector for SPI1_SDO
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SPI1_SDO. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for SPI1_SDO.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPI1_SDI. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for SPI1_SDI. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPI1_SDI
5:4	RW	0x0	Pin Mux Selector for SPI1_SDI
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPI1_SDI. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPI1_SDI.

REG35: offset 0x00d4

Table 56: SPI1_SCK and JTAG0_TDO

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG0_TDO. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for JTAG0_TDO. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG0_TDO
21:20	RW	0x0	Pin Mux Selector for JTAG0_TDO
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for JTAG0_TDO. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG0_TDO.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for SPI1_SCK. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for SPI1_SCK. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for SPI1_SCK
5:4	RW	0x0	Pin Mux Selector for SPI1_SCK
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SPI1_SCK. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for SPI1_SCK.

REG36: offset 0x00d8

Table 57: JTAG0_TCK and JTAG0_TDI

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG0_TDI. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for JTAG0_TDI. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG0_TDI
21:20	RW	0x0	Pin Mux Selector for JTAG0_TDI
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for JTAG0_TDI. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG0_TDI.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG0_TCK. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for JTAG0_TCK. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG0_TCK
5:4	RW	0x0	Pin Mux Selector for JTAG0_TCK
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for JTAG0_TCK. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG0_TCK.

REG37: offset 0x00dc

Table 58: JTAG0_TMS and JTAG0_TRST_X

Fields	Type	De-fault	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG0_TRST_X. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for JTAG0_TRST_X. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG0_TRST_X
21:20	RW	0x0	Pin Mux Selector for JTAG0_TRST_X
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for JTAG0_TRST_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG0_TRST_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG0_TMS. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for JTAG0_TMS. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG0_TMS
5:4	RW	0x0	Pin Mux Selector for JTAG0_TMS
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for JTAG0_TMS. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG0_TMS.

REG38: offset 0x00e0

Table 59: JTAG0_SRST_X and JTAG1_TDO

Fields	Type	De-fault	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG1_TDO. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for JTAG1_TDO. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG1_TDO
21:20	RW	0x0	Pin Mux Selector for JTAG1_TDO
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for JTAG1_TDO. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG1_TDO.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG0_SRST_X. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for JTAG0_SRST_X. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG0_SRST_X
5:4	RW	0x0	Pin Mux Selector for JTAG0_SRST_X
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for JTAG0_SRST_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG0_SRST_X.

REG39: offset 0x00e4

Table 60: JTAG1_TCK and JTAG1_TDI

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG1_TDI. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for JTAG1_TDI. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG1_TDI
21:20	RW	0x0	Pin Mux Selector for JTAG1_TDI
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for JTAG1_TDI. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG1_TDI.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG1_TCK. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for JTAG1_TCK. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG1_TCK
5:4	RW	0x0	Pin Mux Selector for JTAG1_TCK
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for JTAG1_TCK. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG1_TCK.

REG3a: offset 0x00e8

Table 61: JTAG1_TMS and JTAG1_TRST_X

Fields	Type	De-fault	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG1_TRST_X. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for JTAG1_TRST_X. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG1_TRST_X
21:20	RW	0x0	Pin Mux Selector for JTAG1_TRST_X
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for JTAG1_TRST_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG1_TRST_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG1_TMS. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for JTAG1_TMS. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG1_TMS
5:4	RW	0x0	Pin Mux Selector for JTAG1_TMS
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for JTAG1_TMS. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG1_TMS.

REG3b: offset 0x00ec

Table 62: JTAG1_SRST_X and JTAG2_TDO

Fields	Type	De-fault	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG2_TDO. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for JTAG2_TDO. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG2_TDO
21:20	RW	0x0	Pin Mux Selector for JTAG2_TDO
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for JTAG2_TDO. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG2_TDO.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG1_SRST_X. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for JTAG1_SRST_X. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG1_SRST_X
5:4	RW	0x0	Pin Mux Selector for JTAG1_SRST_X
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for JTAG1_SRST_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG1_SRST_X.

REG3c: offset 0x00f0

Table 63: JTAG2_TCK and JTAG2_TDI

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG2_TDI. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for JTAG2_TDI. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG2_TDI
21:20	RW	0x0	Pin Mux Selector for JTAG2_TDI
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for JTAG2_TDI. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG2_TDI.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG2_TCK. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for JTAG2_TCK. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG2_TCK
5:4	RW	0x0	Pin Mux Selector for JTAG2_TCK
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for JTAG2_TCK. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG2_TCK.

REG3d: offset 0x00f4

Table 64: JTAG2_TMS and JTAG2_TRST_X

Fields	Type	De-fault	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for JTAG2_TRST_X. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for JTAG2_TRST_X. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for JTAG2_TRST_X
21:20	RW	0x0	Pin Mux Selector for JTAG2_TRST_X
19:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for JTAG2_TRST_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for JTAG2_TRST_X.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG2_TMS. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for JTAG2_TMS. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG2_TMS
5:4	RW	0x0	Pin Mux Selector for JTAG2_TMS
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for JTAG2_TMS. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG2_TMS.

REG3e: offset 0x00f8

Table 65: JTAG2_SRST_X and GPIO0

Fields	Type	De-fault	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO0. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for GPIO0. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO0
21:20	RW	0x0	Pin Mux Selector for GPIO0
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO0. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO0.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for JTAG2_SRST_X. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for JTAG2_SRST_X. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for JTAG2_SRST_X
5:4	RW	0x0	Pin Mux Selector for JTAG2_SRST_X
3:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for JTAG2_SRST_X. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for JTAG2_SRST_X.

REG3f: offset 0x00fc

Table 66: GPIO1 and GPIO2

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO2. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for GPIO2. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO2
21:20	RW	0x0	Pin Mux Selector for GPIO2
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO2. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO2.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO1. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for GPIO1. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO1
5:4	RW	0x0	Pin Mux Selector for GPIO1
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO1. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO1.

REG40: offset 0x0100

Table 67: GPIO3 and GPIO4

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO4. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for GPIO4. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO4
21:20	RW	0x0	Pin Mux Selector for GPIO4
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO4. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO4.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO3. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for GPIO3. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO3
5:4	RW	0x0	Pin Mux Selector for GPIO3
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO3. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO3.

REG41: offset 0x0104

Table 68: GPIO5 and GPIO6

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO6. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for GPIO6. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO6
21:20	RW	0x0	Pin Mux Selector for GPIO6
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO6. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO6.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO5. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for GPIO5. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO5
5:4	RW	0x0	Pin Mux Selector for GPIO5
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO5. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO5.

REG42: offset 0x0108

Table 69: GPIO7 and GPIO8

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO8. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for GPIO8. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO8
21:20	RW	0x0	Pin Mux Selector for GPIO8
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO8. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO8.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO7. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for GPIO7. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO7
5:4	RW	0x0	Pin Mux Selector for GPIO7
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO7. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO7.

REG43: offset 0x010c

Table 70: GPIO9 and GPIO10

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO10. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for GPIO10. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO10
21:20	RW	0x0	Pin Mux Selector for GPIO10
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO10. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO10.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO9. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for GPIO9. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO9
5:4	RW	0x0	Pin Mux Selector for GPIO9
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO9. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO9.

REG44: offset 0x0110

Table 71: GPIO11 and GPIO12

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO12. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for GPIO12. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO12
21:20	RW	0x0	Pin Mux Selector for GPIO12
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO12. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO12.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO11. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for GPIO11. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO11
5:4	RW	0x0	Pin Mux Selector for GPIO11
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO11. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO11.

REG45: offset 0x0114

Table 72: GPIO13 and GPIO14

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO14. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for GPIO14. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO14
21:20	RW	0x0	Pin Mux Selector for GPIO14
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO14. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO14.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO13. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for GPIO13. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO13
5:4	RW	0x0	Pin Mux Selector for GPIO13
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO13. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO13.

REG46: offset 0x0118

Table 73: GPIO15 and GPIO16

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO16. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for GPIO16. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO16
21:20	RW	0x0	Pin Mux Selector for GPIO16
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO16. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO16.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO15. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for GPIO15. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO15
5:4	RW	0x0	Pin Mux Selector for GPIO15
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO15. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO15.

REG47: offset 0x011c

Table 74: GPIO17 and GPIO18

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO18. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for GPIO18. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO18
21:20	RW	0x0	Pin Mux Selector for GPIO18
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO18. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO18.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO17. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for GPIO17. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO17
5:4	RW	0x0	Pin Mux Selector for GPIO17
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO17. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO17.

REG48: offset 0x0120

Table 75: GPIO19 and GPIO20

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO20. '1' enables PAD output mode under IP's drive
26	RW	0x0	Schmitt trigger enable for GPIO20. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO20
21:20	RW	0x0	Pin Mux Selector for GPIO20
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO20. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO20.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO19. '1' enables PAD output mode under IP's drive
10	RW	0x0	Schmitt trigger enable for GPIO19. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO19
5:4	RW	0x0	Pin Mux Selector for GPIO19
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO19. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO19.

REG49: offset 0x0124

Table 76: GPIO21 and GPIO22

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO22. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x0	Schmitt trigger enable for GPIO22. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO22
21:20	RW	0x0	Pin Mux Selector for GPIO22
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO22. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO22.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO21. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x0	Schmitt trigger enable for GPIO21. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO21
5:4	RW	0x0	Pin Mux Selector for GPIO21
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO21. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO21.

REG4a: offset 0x0128

Table 77: GPIO23 and GPIO24

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO24. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for GPIO24. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO24
21:20	RW	0x0	Pin Mux Selector for GPIO24
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO24. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO24.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO23. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for GPIO23. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO23
5:4	RW	0x0	Pin Mux Selector for GPIO23
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO23. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO23.

REG4b: offset 0x012c

Table 78: GPIO25 and GPIO26

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO26. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for GPIO26. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO26
21:20	RW	0x0	Pin Mux Selector for GPIO26
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO26. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO26.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO25. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for GPIO25. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO25
5:4	RW	0x0	Pin Mux Selector for GPIO25
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO25. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO25.

REG4c: offset 0x0130

Table 79: GPIO27 and GPIO28

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO28. '1' enables PAD output mode under IP's drive
26	RW	0x1	Schmitt trigger enable for GPIO28. '1' enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO28
21:20	RW	0x0	Pin Mux Selector for GPIO28
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO28. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for GPIO28.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO27. '1' enables PAD output mode under IP's drive
10	RW	0x1	Schmitt trigger enable for GPIO27. '1' enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO27
5:4	RW	0x0	Pin Mux Selector for GPIO27
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO27. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for GPIO27.

REG4d: offset 0x0134

Table 80: GPIO29 and GPIO30

Fields	Type	Default	Function
31:28	RO	NA	Reserved
27	RW	0x1	PAD OEX enable for GPIO30. ‘1’ enables PAD output mode under IP’s drive
26	RW	0x1	Schmitt trigger enable for GPIO30. ‘1’ enables Schmitt trigger input function
25:22	RW	0x8	Driving Selector for GPIO30
21:20	RW	0x0	Pin Mux Selector for GPIO30
19:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for GPIO30. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for GPIO30.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO29. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for GPIO29. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO29
5:4	RW	0x0	Pin Mux Selector for GPIO29
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO29. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for GPIO29.

REG4e: offset 0x0138

Table 81: GPIO31 and MODE_SEL0

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for MODE_SEL0. ‘1’ enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for MODE_SEL0. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for MODE_SEL0.
15:12	RO	NA	Reserved
11	RW	0x1	PAD OEX enable for GPIO31. ‘1’ enables PAD output mode under IP’s drive
10	RW	0x1	Schmitt trigger enable for GPIO31. ‘1’ enables Schmitt trigger input function
9:6	RW	0x8	Driving Selector for GPIO31
5:4	RW	0x0	Pin Mux Selector for GPIO31
3:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for GPIO31. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for GPIO31.

REG4f: offset 0x013c

Table 82: MODE_SEL1 and MODE_SEL2

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for MODE_SEL2. '1' enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for MODE_SEL2. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for MODE_SEL2.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for MODE_SEL1. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for MODE_SEL1. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for MODE_SEL1.

REG50: offset 0x0140

Table 83: BOOT_SEL0 and BOOT_SEL1

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for BOOT_SEL1. '1' enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for BOOT_SEL1. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for BOOT_SEL1.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for BOOT_SEL0. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for BOOT_SEL0. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for BOOT_SEL0.

REG51: offset 0x0144

Table 84: BOOT_SEL2 and BOOT_SEL3

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for BOOT_SEL3. '1' enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for BOOT_SEL3. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for BOOT_SEL3.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for BOOT_SEL2. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for BOOT_SEL2. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for BOOT_SEL2.

REG52: offset 0x0148

Table 85: BOOT_SEL4 and BOOT_SEL5

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for BOOT_SEL5. ‘1’ enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for BOOT_SEL5. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for BOOT_SEL5.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for BOOT_SEL4. ‘1’ enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for BOOT_SEL4. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for BOOT_SEL4.

REG53: offset 0x014c

Table 86: BOOT_SEL6 and BOOT_SEL7

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for BOOT_SEL7. ‘1’ enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for BOOT_SEL7. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for BOOT_SEL7.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for BOOT_SEL6. ‘1’ enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for BOOT_SEL6. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for BOOT_SEL6.

REG54: offset 0x0150

Table 87: MULTI_SCKT and SCKT_ID0

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for SCKT_ID0. ‘1’ enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for SCKT_ID0. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for SCKT_ID0.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for MULTI_SCKT. ‘1’ enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for MULTI_SCKT. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for MULTI_SCKT.

REG55: offset 0x0154

Table 88: SCKT_ID1 and PLL_CLK_IN_MAIN

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x0	Schmitt trigger enable for PLL_CLK_IN_MAIN. '1' enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for PLL_CLK_IN_MAIN. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for PLL_CLK_IN_MAIN.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for SCKT_ID1. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for SCKT_ID1. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for SCKT_ID1.

REG56: offset 0x0158

Table 89: PLL_CLK_IN_DDR_L and PLL_CLK_IN_DDR_R

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x0	Schmitt trigger enable for PLL_CLK_IN_DDR_R. '1' enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for PLL_CLK_IN_DDR_R. (0:pull down; 1:pull up)
16	RW	0x0	Pull Enable for PLL_CLK_IN_DDR_R.
15:11	RO	NA	Reserved
10	RW	0x0	Schmitt trigger enable for PLL_CLK_IN_DDR_L. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for PLL_CLK_IN_DDR_L. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for PLL_CLK_IN_DDR_L.

REG57: offset 0x015c

Table 90: XTAL_32K and SYS_RST_X

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for SYS_RST_X. '1' enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x1	Pull Selector for SYS_RST_X. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for SYS_RST_X.
15:11	RO	NA	Reserved
10	RW	0x0	Schmitt trigger enable for XTAL_32K. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for XTAL_32K. (0:pull down; 1:pull up)
0	RW	0x0	Pull Enable for XTAL_32K.

REG58: offset 0x0160

Table 91: PWR_BUTTON and TEST_EN

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RO	0x1	Schmitt trigger enable for TEST_EN. '1' enables Schmitt trigger input function
25:18	RO	NA	Reserved
17	RO	0x0	Pull Selector for TEST_EN. (0:pull down; 1:pull up)
16	RO	0x1	Pull Enable for TEST_EN.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for PWR_BUTTON. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x1	Pull Selector for PWR_BUTTON. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for PWR_BUTTON.

REG59: offset 0x0164

Table 92: TEST_MODE_MBIST and TEST_MODE_SCAN

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for TEST_MODE_SCAN. '1' enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for TEST_MODE_SCAN. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for TEST_MODE_SCAN.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for TEST_MODE_MBIST. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for TEST_MODE_MBIST. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for TEST_MODE_MBIST.

REG5a: offset 0x0168

Table 93: TEST_MODE_BSD and BISR_BYP

Fields	Type	Default	Function
31:27	RO	NA	Reserved
26	RW	0x1	Schmitt trigger enable for BISR_BYP. '1' enables Schmitt trigger input function
25:18	RW	NA	Reserved
17	RW	0x0	Pull Selector for BISR_BYP. (0:pull down; 1:pull up)
16	RW	0x1	Pull Enable for BISR_BYP.
15:11	RO	NA	Reserved
10	RW	0x1	Schmitt trigger enable for TEST_MODE_BSD. '1' enables Schmitt trigger input function
9:2	RW	NA	Reserved
1	RW	0x0	Pull Selector for TEST_MODE_BSD. (0:pull down; 1:pull up)
0	RW	0x1	Pull Enable for TEST_MODE_BSD.

3.2 Analog pins

TODO

CHAPTER

FOUR

CLOCK

4.1 Clock sources

Three 25MHz clock generation chips are required to provide reference clocks for SG2042.

Clock gen chips are the only option for reference clock input and they should be connected to PLL_CLK_IN_MAIN, PLL_CLK_IN_DPLL_L and PLL_CLK_IN_DPLL_R.

External clock sources are listed in table *External clock sources*

Table 1: External clock sources

Clock Name	Frequency	Description
PLL_CLK_IN_MAIN	25MHz	Main clock
PLL_CLK_IN_DPLL_L	25MHz	DDR0 and DDR1
PLL_CLK_IN_DPLL_R	25MHz	DDR2 and DDR3
PCIE0_REFCLK_M	100MHz	PCIe0 reference clock
PCIE0_REFCLK_P	100MHz	PCIe0 reference clock
PCIE1_REFCLK_M	100MHz	PCIe1 reference clock
PCIE1_REFCLK_P	100MHz	PCIe1 reference clock

4.2 PLL

Different parts inside the chip works on different frequencies. As there is no "one-size-fits-all" PLL, SG2042 instantiates 4 PLLs to satisfy logic's clock requirements.

- **MPLL: the name is short for Main PLL.**
  The output clocks of this PLL are mainly used in RP subsystem and AP subsystem.
- **FPLL: the name is shoft for Fixed PLL.**
  This PLL generates fixed frequency clock, with output clock at 1.0 GHz. The output clocks of this PLL are mainly used in data and configuraiton bus.
- **DPLL0/1: the name is short for DDR PLL.**
  The output clocks of thes PLLs are mainly used in DDR subsystem.

And in order to reconfigure PLL clock frequency on the fly, MPLL and DPLL0/1 use FPLL as a backup.

The micro architecture of a pll cell looks like figure *PLL micro architecture*

The output clock frequency is influenced by:

- FREF: Reference Clock Input (10MHz to 800MHz). SG2042 uses 25MHz reference clock.

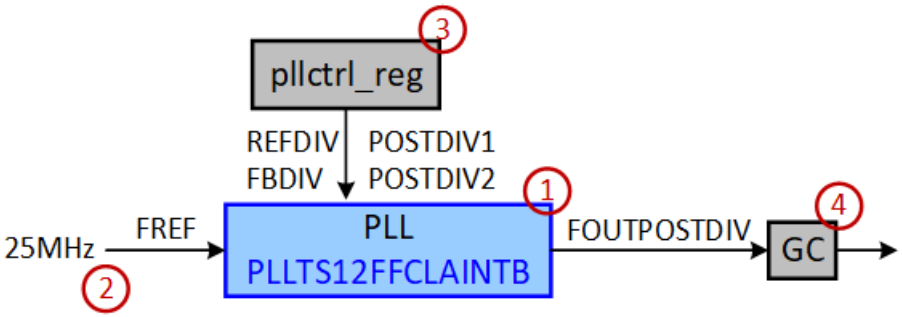

Fig. 1: PLL micro architecture

- FOUTPOSTDIV: Output Clock (16MHz to 3200MHz)
- REFDIV: Reference divide value (1 to 63)
- FBDIV: Feedback divide value (16 to 320)
- POSTDIV1: Post Divide 1 setting (1 to 7)
- POSTDIV2: Post Divide 2 setting (1 to 7)

The output clock frequency is calculated as:

$$FOUTPOSTDIV = FREF * FBDIV/REFDIV/(POSTDIV1 * POSTDIV2)$$

For reference clock, it is used in reset sequence. Only after certain reset sequence (1.5ms), PLL starts to work.

Software together with a dedicated hardware module are in charge of the PLL control, especially the modification of PLL DIV values (REFDIV, FBDIV, POSTDIV1, POSTDIV2).

After Power-On Reset, embedded hardware is able to select the proper initial REFDIV, FBDIV, POSTDIV1 and POSTDIV2 values so that each PLL will generated clocks with expected frequency based on current chip mode.

During runtime, user can alter PLL's output by progamming DIV values inside PLL Control Registers.

Take DPLL0 configuration as an example:

1. Gate PLL output by clearing PLL Clock Enable Control Reg (0x300100C4) bit[4]
2. Modify DPLL0 Control Register (0x300100F8)
3. Polling PLL Status Register (0x300100C0) until: (1). PLL is locked again (bit[12] == 1) and (2). Updating sequence is finished (bit[4] == 0)
4. Un-gate PLL output clock by SettingPLL Clock Enable Control Reg (0x300100C4) bit[4]

When user programs the PLL Control Registers, internal hardware sequence is as figure *PLL hardware sequence*

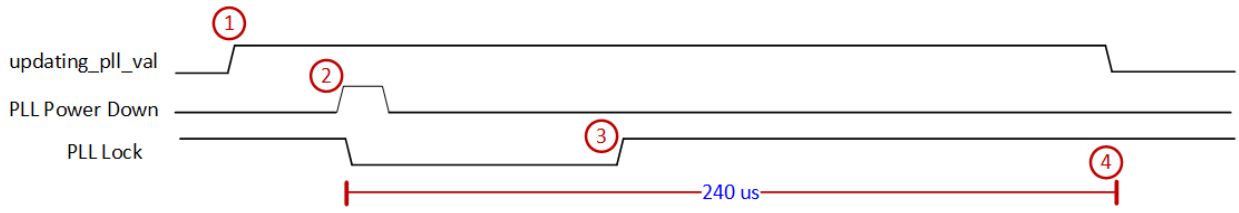

Fig. 2: PLL hardware sequence

- **The updating_pll_val bit is asserted immediately after user writes to PLL Control Registers, and user can check the value of this bit in PLL status**
  register.
- **After hardware logic prepares the new DIV value for PLL, PLL's PD (Global Power Down) signal will be toggled so that PLL will work on**
  the updated value.
- PLL Lock goes high again when PLL's output is stable on new frequency.
- Besides LOCK signal from PLL, internal logic will also wait for 240us then determine the modification sequence is finished and de-assert "updating_pll_val" bit.

User should keep polling PLL Status Register so as to ensure "updating_pll_val" bit field is de-asserted and whole sequece is finished. When the sequence is ongoing, internal logic will prevent initiating another modification.

4.3 Clock gate

When users modify the frequency of a PLL, the output frequency may overshoot/exceed the expected frequency before PLL finally gets stable. This will lead to unwanted behavior or errors.

So output clock of PLL should be gated during configuration.

The generation of clock enable signal is shown as figure *Clock gate*

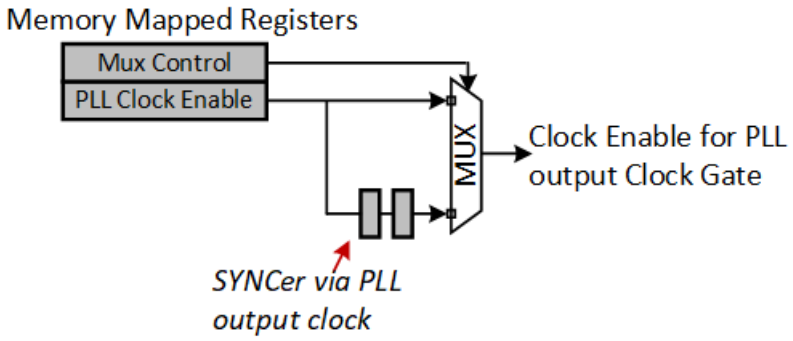

Fig. 3: Clock gate

User is able to control the above logic (Enable/MUX) by programming PLL Clock Enable Control Register (0x3001_00C4).

Both original PLL Clock Enable register and its synced version can be selected as Clock Enable PLL. This is because when PLL's frequency overshoots, the synchonizer may fail to work. There has to be a backup path.

Note that the address of register for controlling PLL Gating shall not be the same as those mentioned in previous section. Cos, once you touch the DIV related register, PLL will be powered-down.

4.4 Clock tree

SG2042 TOP level clock structure is shown as figure *Clock tree*

4.5 Default clock frequency

There three clock modes controlled by clock mode pins. They are safe, normal and fast modes. The tree mode select pins are listed in table *Digital pin functions*

The status of mode select pins is show in table *Mode select*

Table 2: Mode select

MODE_SEL2	MODE_SEL1	MODE_SEL0	MODE
x	0	0	Normal
x	0	1	Fast
x	1	0	Safe
x	1	1	Bypass

MODE_SEL2 pin is no used.

The default clock frequency is show as table *Default clock frequency*

Table 3: Default clock frequency

Clock	NORMAL(MHz)	FAST(MHz)	SAFE(MHz)	BYPASS(MHz)
MPLL	1600	2000	1000	25
FPLL	1000	1000	1000	25
DPLL0	1200	1600	800	25
DPLL1	1200	1600	800	25
RISC-V CPU	1600	2000	1000	25
RISC-V Timer	50	50	50	25
SLC	800	1000	500	25
SYSDMA	250	250	250	25
UART SCLK	500	500	250	25
UART PCLK	250	250	250	25
DBG_I2C	250	250	250	25
LPC	200	200	200	25
BOOTROM	100	100	100	25
SPI Flash	100	100	100	25
BOOTRAM	100	100	100	25
TIMER PCLK	100	100	100	25
TIMER1	50	50	50	25
TIMER2	50	50	50	25
TIMER3	50	50	50	25
TIMER4	50	50	50	25
TIMER5	50	50	50	25
TIMER6	50	50	50	25
TIMER7	50	50	50	25
TIMER8	50	50	50	25
EFUSE CLK	25	25	25	25

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Table 3 – continued from previous page

Clock	NORMAL(MHz)	FAST(MHz)	SAFE(MHz)	BYPASS(MHz)
EFUSE PCLK	100	100	100	25
GPIO PCLK	100	100	100	25
GPIO INTR CLK	100	100	100	25
GPIO DBCLK	0.1	0.1	0.1	0.1
SPI SSI	250	250	250	25
SPI PCLK	250	250	250	25
IIC ICCLK	100	100	100	25
IIC PCLK	100	100	100	25
WDT	100	100	100	25
PWM	100	100	100	25
RTC	100	100	100	25
PCIE0/1/2/3	800	1000	500	25
HSDMA	800	1000	500	25
DDR0/1/2/3	1200	1600	800	25

4.6 Registers

There a set of controll register to controll SoC clocks, including clock gate, divider, mux and pll.

PLL controll registers are located in *Platform control*.

4.6.1 CLKENREG0: offset 0x0000

Table 4: Clock enable register 0

Bits	Attribute	Default	Description
31	RW	0x1	Clock Enable for clk_axi_eth0 (1: Enable; 0: Gate)
30	RW	0x1	Clock Enable for clk_tx_eth0 (1: Enable; 0: Gate)
29	RW	0x1	Clock Enable for clk_apb_rtc (1: Enable; 0: Gate)
28	RW	0x1	Clock Enable for clk_apb_pwm (1: Enable; 0: Gate)
27	RW	0x1	Clock Enable for clk_apb_wdt (1: Enable; 0: Gate)
26	RW	0x1	Clock Enable for clk_apb_i2c (1: Enable; 0: Gate)
25	RW	0x1	Clock Enable for clk_apb_spi (1: Enable; 0: Gate)
24	RW	0x1	Clock Enable for clk_gpio_db (1: Enable; 0: Gate)
23	RW	0x1	Clock Enable for clk_apb_gpio_intr (1: Enable; 0: Gate)
22	RW	0x1	Clock Enable for clk_apb_gpio (1: Enable; 0: Gate)
21	RW	0x1	Clock Enable for clk_apb_efuse (1: Enable; 0: Gate)
20	RW	0x1	Clock Enable for clk_efuse (1: Enable; 0: Gate)
19	RW	0x1	Clock Enable for clk_timer_8 (1: Enable; 0: Gate)
18	RW	0x1	Clock Enable for clk_timer_7 (1: Enable; 0: Gate)
17	RW	0x1	Clock Enable for clk_timer_6 (1: Enable; 0: Gate)
16	RW	0x1	Clock Enable for clk_timer_5 (1: Enable; 0: Gate)
15	RW	0x1	Clock Enable for clk_timer_4 (1: Enable; 0: Gate)
14	RW	0x1	Clock Enable for clk_timer_3 (1: Enable; 0: Gate)
13	RW	0x1	Clock Enable for clk_timer_2 (1: Enable; 0: Gate)
12	RW	0x1	Clock Enable for clk_timer_1 (1: Enable; 0: Gate)
11	RW	0x1	Clock Enable for clk_apb_timer (1: Enable; 0: Gate)

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Table 4 – continued from previous page

Bits	Attribute	Default	Description
10	RW	0x1	Clock Enable for clk_axi_sram (1: Enable; 0: Gate)
9	RW	0x1	Clock Enable for clk_ahb_sf (1: Enable; 0: Gate)
8	RW	0x1	Clock Enable for clk_ahb_rom (1: Enable; 0: Gate)
7	RW	0x1	Clock Enable for clk_ahb_lpc (1: Enable; 0: Gate)
6	RW	0x1	Clock Enable for clk_axi_dbg_i2c (1: Enable; 0: Gate)
5	RW	0x1	Clock Enable for clk_apb_uart (1: Enable; 0: Gate)
4	RW	0x1	Clock Enable for clk_uart_500m (1: Enable; 0: Gate)
3	RW	0x1	Clock Enable for clk_sysdma_axi (1: Enable; 0: Gate)
2	RW	0x1	Clock Enable for clk_slc (1: Enable; 0: Gate)
1	RW	0x1	Clock Enable for clk_scp_timer (1: Enable; 0: Gate)
0	RW	0x1	Clock Enable for clk_rp_cpu_normal (1: Enable; 0: Gate)

4.6.2 CLKENREG1: offset 0x0004

Table 5: Clock enable register 1

Bits	Attribute	Default	Description
31:16	RW	NA	Reserved
15	RW	0x1	Clock Enable for clk_ddr23 (1: Enable; 0: Gate)
14	RW	0x1	Clock Enable for clk_ddr01 (1: Enable; 0: Gate)
13	RW	0x1	Clock Enable for clk_axi_ddr (1: Enable; 0: Gate)
12	RW	0x1	Clock Enable for clk_top_axi_hsperi (1: Enable; 0: Gate)
11	RW	0x1	Clock Enable for clk_top_axi0 (1: Enable; 0: Gate)
10	RW	0x1	Clock Enable for clk_hsdma (1: Enable; 0: Gate)
9	RW	0x1	Clock Enable for clk_axi_pcie1 (1: Enable; 0: Gate)
8	RW	0x1	Clock Enable for clk_axi_pcie0 (1: Enable; 0: Gate)
7	RW	0x1	Clock Enable for clk_100k_sd (1: Enable; 0: Gate)
6	RW	0x1	Clock Enable for clk_sd (1: Enable; 0: Gate)
5	RW	0x1	Clock Enable for clk_axi_sd (1: Enable; 0: Gate)
4	RW	0x1	Clock Enable for clk_100k_emmc (1: Enable; 0: Gate)
3	RW	0x1	Clock Enable for clk_emmc (1: Enable; 0: Gate)
2	RW	0x1	Clock Enable for clk_axi_emmc (1: Enable; 0: Gate)
1	RW	0x1	Clock Enable for clk_ref_eth0 (1: Enable; 0: Gate)
0	RW	0x1	Clock Enable for clk_ptp_ref_i_eth0 (1: Enable; 0: Gate)

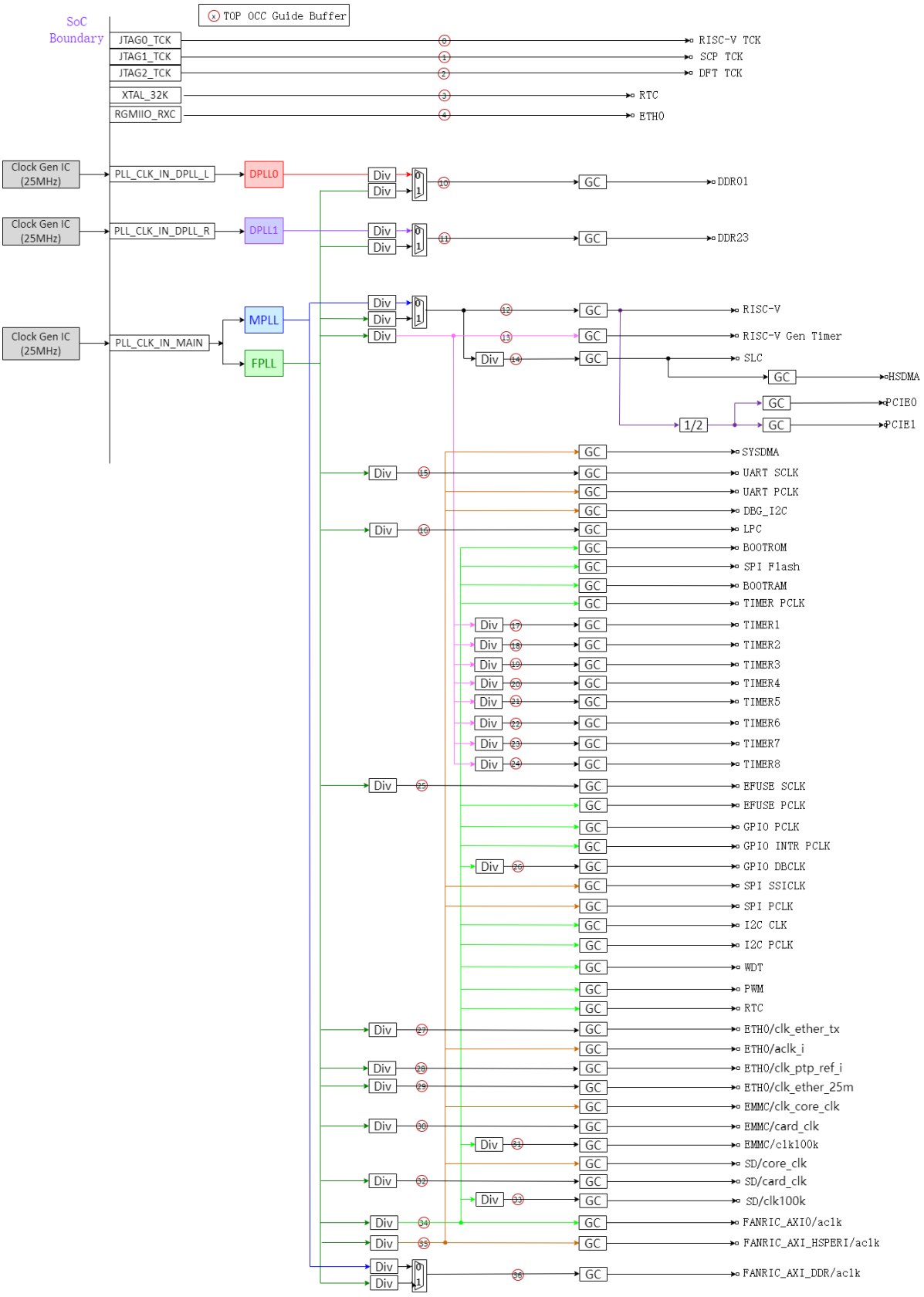

Fig. 4: Clock tree

4.6.3 CLKSELREG0: offset 0x0020

Table 6: Clock select register 0

Bits	Attribute	Default	Description
31:4	RW	NA	Reserved
3	RW	0x1	Clock Select for DDR23's clock core_ddrc_core_clk (aka clk_ddr23) 1: Select in_dpll1_clk as clock source 0: Select in_fpll_clk as clock source
2	RW	0x1	Clock Select for DDR01's clock core_ddrc_core_clk (aka clk_ddr01) 1: Select in_dpll0_clk as clock source 0: Select in_fpll_clk as clock source
1	RW	0x1	Clock Select for FABRIC_AXI_DDR's clock aclk (aka clk_axi_ddr) 1: Select in_mpll_clk as clock source 0: Select in_fpll_clk as clock source
0	RW	0x1	Clock Select for RP's clock top_rp_cpu_clk_normal (aka clk_rp_cpu_normal) 1: Select in_mpll_clk as clock source 0: Select in_fpll_clk as clock source

4.6.4 CLKDIVREG0: offset 0x0040

Table 7: Clock divider 0 control of RISC-V core

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:5	RW	NA	Reserved
4	RW	0x0	Clock Enable for this Branch Divider 0: Gate this Branch Divider 1: Enable this Branch Divider
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.5 CLKDIVREG1: offset 0x0044

Table 8: Clock divider 1 control of RISC-V core

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:5	RW	NA	Reserved
4	RW	0x0	Clock Enable for this Branch Divider 0: Gate this Branch Divider 1: Enable this Branch Divider
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.6 CLKDIVREG2: offset 0x0048

Table 9: Clock divider control of SCP timer

Bits	Attribute	Default	Description
31:24	RW	NA	Reserved
23:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.7 CLKDIVREG3: offset 0x004c

Table 10: Clock divider control of SLC

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.8 CLKDIVREG4: offset 0x0050

Table 11: Clock divider control of UART

Bits	Attribute	Default	Description
31:23	RW	NA	Reserved
22:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.9 CLKDIVREG5: offset 0x0054

Table 12: Clock divider control of LPC

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.10 CLKDIVREG6: offset 0x0058

Table 13: Clock divider control of TIMER1

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.11 CLKDIVREG7: offset 0x005c

Table 14: Clock divider control of TIMER2

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.12 CLKDIVREG8: offset 0x0060

Table 15: Clock divider control of TIMER3

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.13 CLKDIVREG9: offset 0x0064

Table 16: Clock divider control of TIMER4

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.14 CLKDIVREG10: offset 0x0068

Table 17: Clock divider control of TIMER5

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.15 CLKDIVREG11: offset 0x006c

Table 18: Clock divider control of TIMER6

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.16 CLKDIVREG11: offset 0x0070

Table 19: Clock divider control of TIMER7

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.17 CLKDIVREG12: offset 0x0074

Table 20: Clock divider control of TIMER8

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.18 CLKDIVREG13: offset 0x0078

Table 21: Clock divider control of eFuse

Bits	Attribute	Default	Description
31:23	RW	NA	Reserved
22:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.19 CLKDIVREG14: offset 0x007c

Table 22: Clock divider control of GPIO DB

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.20 CLKDIVREG15: offset 0x0080

Table 23: Clock divider control of ETH TX

Bits	Attribute	Default	Description
31:27	RW	NA	Reserved
26:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.21 CLKDIVREG16: offset 0x0084

Table 24: Clock divider control of ETH PTP

Bits	Attribute	Default	Description
31:24	RW	NA	Reserved
23:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.22 CLKDIVREG17: offset 0x0088

Table 25: Clock divider control of ETH

Bits	Attribute	Default	Description
31:24	RW	NA	Reserved
23:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.23 CLKDIVREG18: offset 0x008c

Table 26: Clock divider control of eMMC

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.24 CLKDIVREG18: offset 0x0090

Table 27: Clock divider control of eMMC 100k

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.25 CLKDIVREG19: offset 0x0094

Table 28: Clock divider control of SDIO

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.26 CLKDIVREG20: offset 0x0098

Table 29: Clock divider control of SDIO 100k

Bits	Attribute	Default	Description
31:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.27 CLKDIVREG21: offset 0x009c

Table 30: Clock divider control of TOP AXI0

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RO	0x0	Select Divide Factor from Register This bit is reserved for this divider.
2	RO	0x0	Select High Wide Control from Register This bit is reserved for this divider.
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RO	0x1	Divider Reset Control This bit is reserved for this divider.

4.6.28 CLKDIVREG22: offset 0x00a0

Table 31: Clock divider control of TOP AXI0

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:4	RW	NA	Reserved
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.29 CLKDIVREG23: offset 0x00a4

Table 32: Clock divider 0 control of AXI DDR

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:5	RW	NA	Reserved
4	RW	0x0	Clock Enable for this Branch Divider 0: Gate this Branch Divider 1: Enable this Branch Divider
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.30 CLKDIVREG24: offset 0x00a8

Table 33: Clock divider 1 control of AXI DDR

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:5	RW	NA	Reserved
4	RW	0x0	Clock Enable for this Branch Divider 0: Gate this Branch Divider 1: Enable this Branch Divider
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.31 CLKDIVREG25: offset 0x00ac

Table 34: Clock divider 0 control of DDR01

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:5	RW	NA	Reserved
4	RW	0x0	Clock Enable for this Branch Divider 0: Gate this Branch Divider 1: Enable this Branch Divider
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.32 CLKDIVREG26: offset 0x00b0

Table 35: Clock divider 1 control of DDR01

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:5	RW	NA	Reserved
4	RW	0x0	Clock Enable for this Branch Divider 0: Gate this Branch Divider 1: Enable this Branch Divider
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.33 CLKDIVREG27: offset 0x00b4

Table 36: Clock divider 0 control of DDR23

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:5	RW	NA	Reserved
4	RW	0x0	Clock Enable for this Branch Divider 0: Gate this Branch Divider 1: Enable this Branch Divider
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

4.6.34 CLKDIVREG28: offset 0x00b8

Table 37: Clock divider 1 control of DDR23

Bits	Attribute	Default	Description
31:21	RW	NA	Reserved
20:16	RW	0x0	Clock Divider Factor
15:5	RW	NA	Reserved
4	RW	0x0	Clock Enable for this Branch Divider 0: Gate this Branch Divider 1: Enable this Branch Divider
3	RW	0x0	Select Divide Factor from Register 0: Select initial value 1: Select Divide Factor from this register
2	RW	0x0	Select High Wide Control from Register 0: Select initial value 1: Select High Wide from this register
1	RW	0x0	High Wide Control (when Divider Factor is odd) 0: Low level of the clock is wider 1: High level of the clock is wider
0	RW	0x1	Divider Reset Control 0: Assert Reset 1: De-assert Reset

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