DDR4 32GB 3200MT/s 2Rank x 8 RDIMM

RER432A032G7-WFS100

Version: 1.1

Revision History

Rev.	Date	Mark
1.0	2022/4	Preliminary
1.1	2022/7	Product Brand and PN Change, Add IDD specifications and Product Certifications, update the Module Dimensions.

Contents

1. INTRODUCTION

1.1. General Description

This document describes DDR4 2048M x 72 two ranks 32GB DDR4-3200 CL22 1.2V Registered DIMM product.

The product is based on 16C+2C 1024M x8-bit DDR4 FBGA components (2C DRAM for ECC function).The SPD is programmed follow JEDEC standard for 3200MT/s timing of 22-22-22 at 1.2V low power.

This product design specification reference JEDEC standard (N.O. 21C) DDR4 Registered DIMM Design raw-card E3.

This 288-pin RDIMM requires +1.2V VDD and VDDQ power supply.

1.2. Ordering Information

[Table 1] Ordering Information

Part Number	Memory Type	Density	Organization	Component Composition	#of Ranks
RER432A032G7-WFS100	DDR4 RDIMM	32GB	2048Mx72bit per Rank	DDR4 2048M*8 18C	2

1.3. Features

•Power Supply: VDD=1.2V (1.14V to 1.26V)
•VDDQ = 1.2V (1.14V to 1.26V)
•VPP=2.5V (2.375V to 2.75V)
•VDDSPD=2.25V to 2.75V
•Functionality and operations comply with the DDR4 SDRAM datasheet
•16 internal banks
•Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
•Bi-Directional Differential Data Strobe
•8 bit pre-fetch

•Average Refresh Cycle (Normal Operating Temperature Range 0℃ ~ 85℃ Extended Temperature Range:85℃~95℃)
•Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
•Supports ECC error correction and detection
•On-Die Termination (ODT)
• SPD with integrated temperature sensor
•This product is in compliance with the RoHS directive.
•Per DRAM Addressability is supported
•Internal Vref DQ level generation is available
•Write CRC is supported at all speed grades
•DBI (Data Bus Inversion) is supported(x8)

2. Key Parameters

Speed Grade	Data Rate (MT/s)	Target CL- tRCD-tRP	CL (ns)	tRCD (ns)	tRP (ns)
2933	2933	21-21-21	14.32	14.32	14.32
3200	3200	22-22-22	13.75	13.75	13.75

2.1. Addressing

Parameter	2048Meg x 8bit
Number of bank groups	4
Bank group address	BG[1:0]
Bank address in bank group	BA[1:0]
Row addressing	A[15:0]
Column addressing	A[9:0]
Page size	1KB

2.2. Pin Assignments

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
1	12V	145	12V	74	CK0_t	218	CK1_t
2	VSS	146	VREFCA	75	CK0_c	219	CK1_c
3	DQ4	147	VSS	76	VDD	220	VDD
4	VSS	148	DQ5	77	VTT	221	VTT
5	DQ0	149	VSS				
6	VSS	150	DQ1				
7	DQS9_t, DM0_n, DBI0_n, TDQS9_t	151	VSS	78	EVENT_n	222	PARITY
8	DQS9_c, TDQS9_c	152	DQS0_c	79	A0	223	VDD
9	VSS	153	DQS0_t	80	VDD	224	BA1
10	DQ6	154	VSS	81	BA0	225	A10/AP
11	VSS	155	DQ7	82	RAS_n/A16	226	VDD
12	DQ2	156	VSS	83	VDD	227	RFU
13	VSS	157	DQ3	84	S0_n	228	WE_n/A14
14	DQ12	158	VSS	85	VDD	229	VDD
15	VSS	159	DQ13	86	CAS_n/A15	230	Save_n,NC
16	DQ8	160	VSS	87	ODT0	231	VDD
17	VSS	161	DQ9	88	VDD	232	A13
18	DQS10_t, DM1_n, DBI1_n, TDQS10_t	162	VSS	89	S1_n	233	VDD
19	DQS10_c, TDQS10_c	163	DQS1_c	90	VDD	234	A17, NC
20	VSS	164	DQS1_t	91	ODT1	235	C[2], NC
21	DQ14	165	VSS	92	VDD	236	VDD
22	VSS	166	DQ15	93	S2_n, C[0]	237	S3_n, C[1]
23	DQ10	167	VSS	94	VSS	238	SA2
24	VSS	168	DQ11	95	DQ36	239	VSS
25	DQ20	169	VSS	96	VSS	240	DQ37
26	VSS	170	DQ21	97	DQ32	241	VSS
27	DQ16	171	VSS	98	VSS	242	DQ33
28	VSS	172	DQ17	99	DQS13_t, DM4_n, DBI4_n, TDQS13_t	243	VSS
29	DQS11_t, DM2_n, DBI2_n, TDQS11_t	173	VSS	100	DQS13_c, TDQS13_c	244	DQS4_c

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
30	DQS11_c,TDQS11_c	174	DQS2_c	101	VSS	245	DQS4_t
31	VSS	175	DQS2_t	102	DQ38	246	VSS
32	DQ22	176	VSS	103	VSS	247	DQ39
33	VSS	177	DQ23	104	DQ34	248	VSS
34	DQ18	178	VSS	105	VSS	249	DQ35
35	VSS	179	DQ19	106	DQ44	250	VSS
36	DQ28	180	VSS	107	VSS	251	DQ45
37	VSS	181	DQ29	108	DQ40	252	VSS
38	DQ24	182	VSS	109	VSS	253	DQ41
39	VSS	183	DQ25	110	DQS14_t, DM5_n, DBI5_n, TDQS14_t	254	VSS
40	DQS12_t, DM3_n, DBI3_n, TDQS12_t	184	VSS	111	DQS14_c, TDQS14_c	255	DQS5_C
41	DQS12_c, TDQS12_c	185	DQS3_c	112	VSS	256	DQS5_t
42	VSS	186	DQS3_t	113	DQ46	257	VSS
43	DQ30	187	VSS	114	VSS	258	DQ47
44	VSS	188	DQ31	115	DQ42	259	VSS
45	DQ26	189	VSS	116	VSS	260	DQ43
46	VSS	190	DQ27	117	DQ52	261	VSS
47	CB4,NC	191	VSS	118	VSS	262	DQ53
48	VSS	192	CB5,NC	119	DQ48	263	VSS
49	CB0,NC	193	VSS	120	VSS	264	DQ49
50	VSS	194	CB1,NC	121	DQS15_t, DM6_n, DBI6_n, TDQS15_t	265	VSS
51	DQS17_t, DM8_n, DBI8_n, TDQS17_t	195	VSS	122	DQS15_c, TDQS15_c	266	DQS6_c
52	DQS17_c, TDQS17_c	196	DQS8_c	123	VSS	267	DQS6_t
53	VSS	197	DQS8_t	124	DQ54	268	VSS

Pin	Front Side Pin Label	Pin	Back Side Pin Label	Pin	Front Side Pin Label	Pin	Back Side Pin Label
54	CB6,NC	198	VSS	125	VSS	269	DQ55
55	VSS	199	CB7,NC	126	DQ50	270	VSS
56	CB2,NC	200	VSS	127	VSS	271	DQ51
57	VSS	201	CB3,NC	128	DQ60	272	VSS
58	RESET_n	202	VSS	129	VSS	273	DQ61
59	VDD	203	CKE1	130	DQ56	274	VSS
60	CKE0	204	VDD	131	VSS	275	DQ57
61	VDD	205	RFU	132	DQS16_t, DM7_n, DBI7_n, TDQS16_t	276	VSS
62	ACT_n	206	VDD	133	DQS16_c, TDQS16_c	277	DQS7_c
63	BG0	207	BG1	134	VSS	278	DQS7_t
64	VDD	208	ALERT_n	135	DQ62	279	VSS
65	A12	209	VDD	136	VSS	280	DQ63
66	A9	210	A11	137	DQ58	281	VSS
67	VDD	211	A7	138	VSS	282	DQ59
68	A8	212	VDD	139	SA0	283	VSS
69	A6	213	A5	140	SA1	284	VDDSPD
70	VDD	214	A4	141	SCL	285	SDA
71	A3	215	VDD	142	VPP	286	VPP
72	A1	216	A2	143	VPP	287	VPP
73	VDD	217	VDD	144	RFU	288	VPP

2.3. Pin Descriptions

Pin Name	Description	Pin Name	Description
A0–A17[1]	SDRAM address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	SDRAM bank select input	SDA	I2C serial data line for SPD/TS and register
BG0, BG1	Register Bank Group Inputs	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power
WE_n[4]	Register write enable input	12 V	Optional Power Supply on socket but not used on RDIMM
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	VPP	SDRAM Supply
CB0–CB7	DIMM ECC check bits	RESET_n	Set Register and SDRAMs to a Known State
TDQS9_t-TDQS17_t TDQS9_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs.	EVENT_n	SPD signals a thermal event has occurred
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DBI0_n-DBI8_n	Data Bus Inversion	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clock input (negative line of differential pair)		

Notes：

1. Address A17 is only valid for 16Gbx4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

2.4. Input/Output Pin Functional Descriptions

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On-Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t, and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 will be considered as Row Address A16, A15, and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command being entered. Those pins are multi-function. For example, for activation with ACT_n Low, these are Addresses like A16, A15, and A14, but for non-activation command with ACT_n High, these are Command pins for Read, Write, and other commands defined in command truth table.

BG0, BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write, or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0, BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS9_t-TDQS17_t, TDQS9_c-TDQS17_c	Output	Provides a dummy load for x8 based RDIMMs where mixed populations of x4 and x8 based RDIMMs are present.

DBI0_n-DBI8_n	Input/ Output	Provides for data bus inversion. Only possible for x8 based RDIMMs and where only x8 based RDIMMs are on a channel.
DM0_n-DM8_n	Input	Provides for masking of a byte on WRITE commands to the SDRAMs. Only Possible x8 based RDIMMs and where only x8 based RDIMMs are on a channel.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time as command & address, with CS_n LOW.
ALERT_n	Output (Input)	Alert: Is multi functions, such as CRC error flag or Command and Address Parity error flag, as on Output signal. If there is an error in the CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is an error in the Command Address Parity Check, then ALERT_n goes LOW for a relatively long period until on going SDRAM internal recovery transaction is complete. During Connectivity Test mode, this pin functions as an input. Using this signal or not is dependent on the system.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.
NC		No Connect: No on DIMM electrical connection is present.
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VTT	Supply	Power Supply for termination of Address, Command and Control, VDD/2.
12V	Supply	12V supply not used on RDIMMs.
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VDDSPD	Supply	Power supply used to power the I2C bus on the SPD-TSE.
VREFCA	Supply	Reference voltage for CA

2.5. AC & DC Operating Conditions

Recommended DC Operating Conditions –DDR4 (1.2V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Supply Voltage for DRAM Activating	2.375	2.5	2.75	V	3

Notes:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

2.6. DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
	Normal Operating Temperature Range	0 to 85	°C	1,2
T_{OPER}	Extended Temperature Range	85 to 95	°C	1,3

Notes

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 -85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range.
   Please refer to the DIMM SPD for option availability
   If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

2.7. IDD Specifications

IDD and IPP Current Limits; Die Rev. F

Symbol	DDR4-2933	DDR4-3200	Unit
I_{DD0}:One bank ACTIVATE-to-PRECHARGE current	59	60	mA
I_{PP0}:One bank ACTIVATE-to-PRECHARGE Ipp current	3	3	mA
I_{DD1}:One bank ACTIVATE-to-READ-to- PRECHARGE current	70	71	mA
I_{DD2N}:Precharge standby current	44	45	mA
I_{DD2NT}:Precharge standby ODT current	50	51	mA
I_{DD2P}:Precharge power-down current	38	38	mA
I_{DD2Q}: Precharge quiet standby current	42	42	mA
I_{DD3N}: Active standby current	60	61	mA
I_{PP3N}:Active standby I_{pp} current	2	2	mA
I_{DD3P}:Active power-down current	49	50	mA
I_{DD4R}:Burst read current	132	140	mA
I_{DD4W}:Burst write current	107	112	mA
I_{DD5R}:Distributed refresh current (1× REF)	68	68	mA
I_{PP5R}:Distributed refresh I_{pp} current (1× REF)	4	4	mA
I_{DD6N}:Self refresh current;-40-85℃[1]	53	53	mA
I_{DD6E}:Self refresh current;-40-95℃[2,4]	90	90	mA
I_{DD6R}:Self refresh current;-40-45℃[3,4]	20	20	mA
I_{DD6A}:Auto self refresh current(25℃)[4]	11	11	mA
I_{DD6A}:Auto self refresh current (45℃)[4]	20	20	mA
I_{DD6A}:Auto self refresh current (75℃)[4]	51	51	mA
I_{DD6A}:Auto self refresh current(95℃)[4]	90	90	mA

I_{PP6X}:Auto self refresh Ipp current;-40-95℃[5]	6	6	mA
I_{DD7}:Bank interleave read current	165	167	mA
I_{PP7}:Bank interleave read Ipp current	8	8	mA
I_{DD8}:Maximum power-down current	36	36	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation(-40-85℃).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation(-40-95℃).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation(-40-45℃).
4. IDD6R, IDD6A, and IDD6E values are verified by design and characterization, and may not be subject to production test.
5. IPP6X is applicable to IDD6N, IDD6E, IDD6R and IDD6A conditions.

2.8. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.3V~1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3V~1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3V~3.0	V	4
V_{IN},V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3V~1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	℃	1,2

Notes:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times
5. Overshoot area above 1.5V is specified in DDR4 Device Operation.

3. Function Related

3.1. Registering Clock Driver Operation

Registering clock driver device consisting of a register and a phase-lock loop (PLL). The device compliant with the JEDEC DDR4RCD02 specification. Registering clock driver (RCD) used to reduce the electrical load on the host memory controller's command, address, and control bus.

Registering Clock Driver Timing

Symbol	Parameter	Conditions	DDR4-2933/3200		Units
			Min	Max	
f_{clock}	Input clock frequency	Application frequency	625	1620	MHz
t_{CH}/t_{CL}	Pulse duration, CK_t/CK_c HIGH or LOW	--	0.4	--	tCK
$t_{jit\_inp(p\text{-}p)}$	Accumulated input phase jitter at CK_t/CK_c	--	0	50	ps

t_{ACT}	Inputs active time before DRST_n is taken HIGH	DCKE0/1=LOW and DCS0/1_n=HIGH	16	--	tCK
t_{MRD}	Control word to control word delay	Number of clock cycles between two control word accesses, MRS accesses, or any DRAM commands	8	--	tCK
t_{MRC}	Register command word to CW or DRAM command delay	Number of clock cycles between register command word (F0RC06) and CW or any DRAM command	16	--	tCK
t_{PDM}	Propagation delay, single bit switching; CK_t/CK_c cross point to output	1.2 V Operation	1	1.3	ns
t_{DIS}	Output disable time	Rising edge of Yn_t to output float	0.5*tCK + tQSK1(min)	--	ps
t_{EN}	Output disable time	Output valid to rising edge of Yn_t	0.5*tCK - tQSK1(max)	--	ps

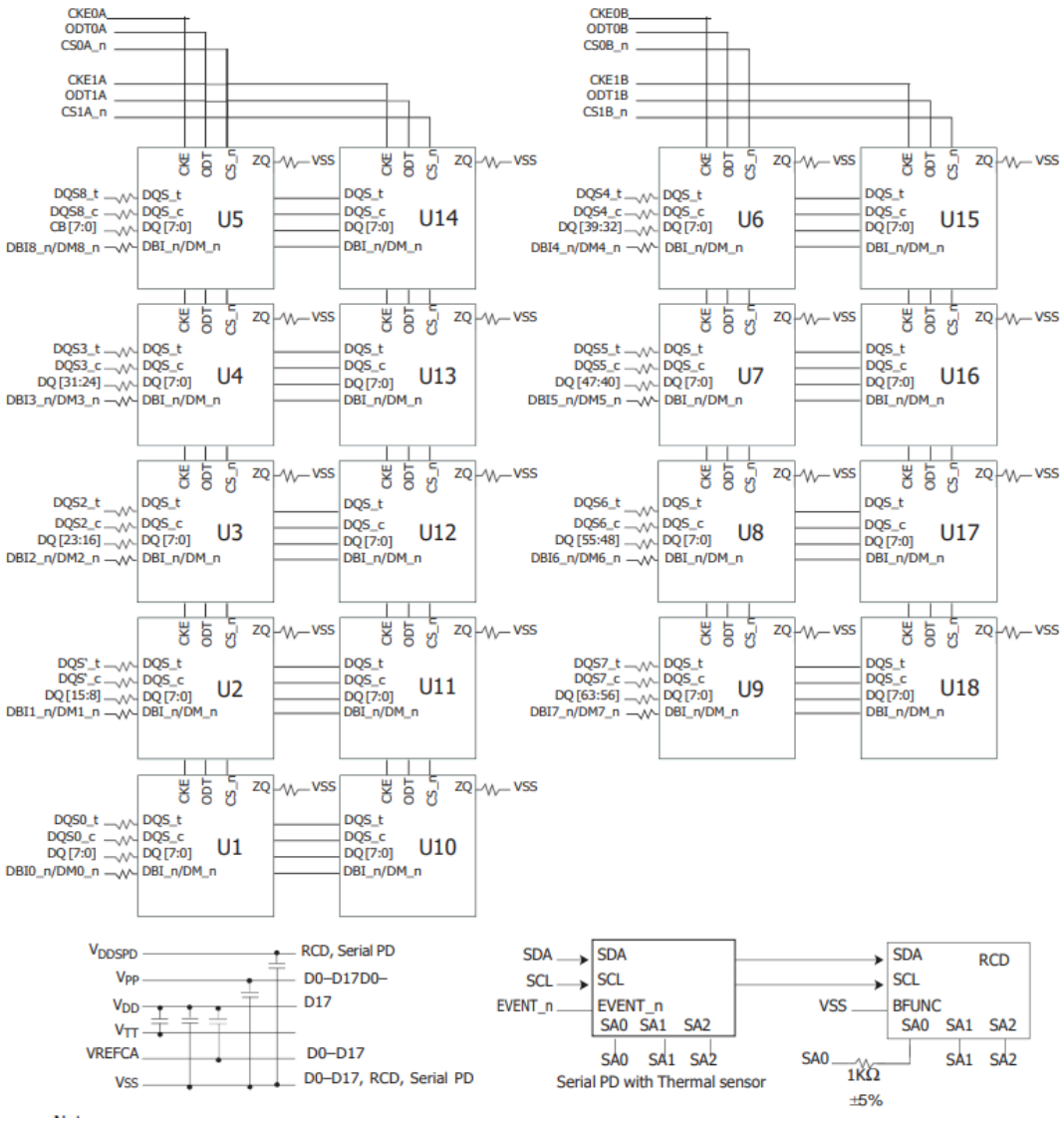
Notes:
1. This parameter compliant with the JEDEC DDR4RCD02 specification.

Registering Clock Driver Operating Electrical Characteristics

Symbol	Parameter	Applicable Signals	Min	Nom	Max	Unit
V_{DD} PV_{DD}	DC Supply voltage	--	1.14	1.2	1.26	V
AV_{DD}	DC Supply voltage before fiter	--	1.13	1.2	1.26	V
V_{TT}	DC Termination voltage	--	V_{DDnom}/2-45	V_{DDnom}/2	V_{DDnom}/2+45	mV
V_{REF}	DC Reference voltage	VrefCA	0.49xV_{DD}	0.5xV_{DD}	0.51xV_{DD}	mV
$V_{IH.CMOS}$	HIGH-level input voltage	DRST_n	0.65xV_{DD}	--	V_{DD}	V
$V_{IL.CMOS}$	LOW-level input voltage		V_{SS}	--	0.35xV_{DD}	V
$V_{OH(AC)}$	AC output high level	All outputs except ALERT_n	V_{TT} + 0.15xV_{DD}	--	--	V
$V_{OL(AC)}$	AC output low level		--	--	V_{TT} - 0.15xV_{DD}	V
$V_{oHdiff(AC)}$	AC differential output high measurement level (for output SR)	Y_{n_t}/Y_{n_c}, BCK_t/BCK_c	--	+ 0.3 x V_{DD}	--	V
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)		--	-0.3 x V_{DD}	--	V

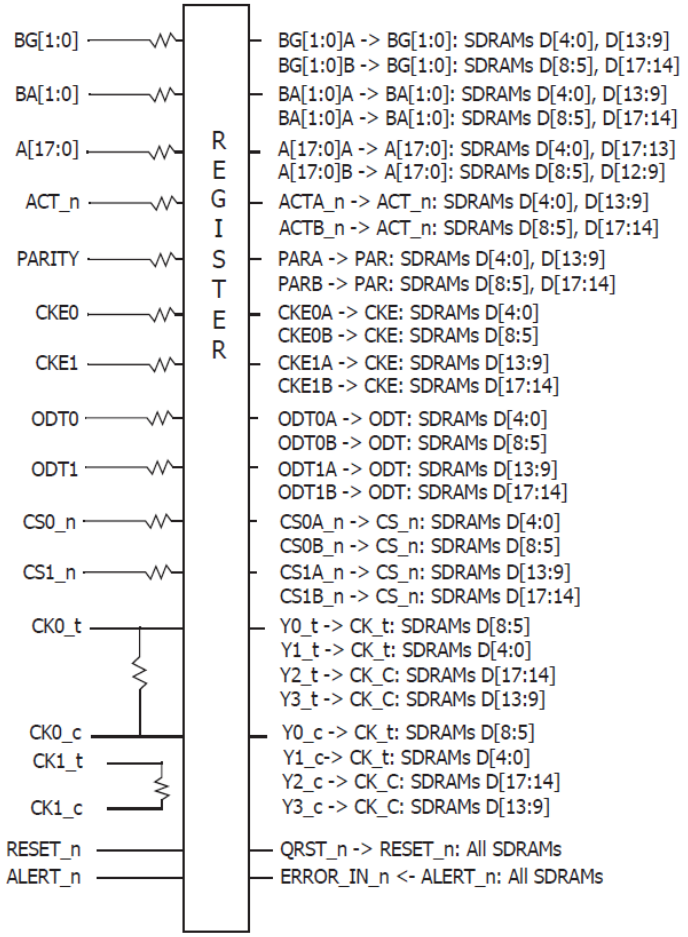
Notes:
1. Table is provided as a general reference. Consult JEDEC DDR4RCD02 for complete details.

3.2. Functional Block Diagram



Notes:

1. Unless otherwise noted, resistors values are 15Ω+/-5%;
2. See the Net Structure diagrams for all resistors associated with the command , address and control bus；
3. ZQ resistors are 240Ω+/-1%;
4. The TEN Pin on the SDRAMS are tied to VSS；
5. VDD and VDDSPD also connected to the RCD。



Notes:

1. CK0_t， CK0_c terminated with 120Ω+/- 5% resistor;
2. CK1_t, CK1_c terminated with 120Ω+/- 5% resistor but not used;
3. Unless otherwise noted resistors are 22Ω+/- 5%.

3.3. Thermal Sensor with SPD EEPROM Operation

3.3.1 Thermal Sensor Operations

The thermal sensor continuously monitors the temperature of the module, Temperature data can be read from the I2C bus at any time, which provide the host real-time feedback of the module's temperature.

The Temperature Register Set stores the temperature data, limits, and configuration values. All registers in the address space from 0x00 through 0x08 are 16-bit registers (shown in the table below), accessed through block rea d and write commands.

Temperature Register Addresses

ADDR	R/W	NAME	FUNCTION	DEFAULT
NA	W	Address Pointer	Address storage for subsequent operations	undefined
00	R	Capabilities	Indicates the functions and capabilities of the temperature sensor	00EFh
01	R/W	Configuration	Controls the operation of the temperature monitor	0000
02	R/W	High Limit	Temperature High Limit	0000
03	R/W	Low Limit	Temperature Low Limit	0000
04	R/W	TCRIT Limit	Critical Temperature	0000
05	R	Ambient Temperature	Current Ambient temperature	NA
06	R	Manufacturer ID	PCI-SIG manufacturer ID	Contact FAE for more information
07	R	Device/Revision	Device ID and Revision number	Contact FAE for more information
08-0F	R/W	Vendor-defined	Vendor specific information	NA

Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 TSE2004 for complete details.

Thermal sensor DC parameters

Symbol	Parameter	Min	Max	Units
V_{DDSPD}	Supply Voltage	2.25	2.75	V
I_{LI}	Input leakage current (SCL, SDA)	--	±5	μA
I_{LO}	Output leakage current	--	±5	μA
I_{DDR}	Supply current, read operation	--	2	mA
I_{DDW}	Supply current, write operation	--	3	mA
I_{DDI}	Standby Supply current	--	100	μA
V_{IL}	Input low voltage (SCL, SDA)	-0.5	$0.3xV_{DDSPD}$	V
V_{IH}	Input high voltage (SCL, SDA)	$0.7xV_{DDSPD}$	V_{DDSPD} + 0.5	V
V_{OL1}	Output low voltage1 open-drain or open-collector	--	0.4	V
V_{OL2}		--	$0.2xV_{DDPSD}$	V

Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 TSE2004 for complete details.

Thermal sensor and EEPROM serial interface timing

		$V_{DDSPD} \geq 2.2$ V				
		400 KHz		1000 KHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{SCL}	Clock frequency	10	400	10	1000	kHz
t_{HIGH}	Clock pulse width HIGH time	600	-	260	--	ns
t_{LOW}	Clock pulse width LOW time	1300	-	500	--	ns
$t_{TIMEOUT}$	Detect clock LOW timeout	25	35	25	35	ms
t_R	SDA rise time	20	300	--	120	ns
t_F	SDA fall time	20	300	--	120	ns
$t_{SU:DAT}$	Data-in setup time	100	-	50	--	ns
$t_{HD:DI}$	Data-in hold time	0	-	0	--	ns
$t_{HD:DAT}$	Data out hold time	200	900	0	350	ns
$t_{SU:STA}$	Start condition setup time	600	--	260	--	ns
$t_{HD:STA}$	Start condition hold time	600	--	260	--	ns
$t_{SU:STO}$	Stop condition setup time	600	--	260	--	ns
t_{BUF}	Time the bus must be free before a new transi- tion can start	1300	--	500	--	ns
t_W	Write time	--	5	--	5	ms
t_{POFF}	Warm power cycle time off	1	--	1	--	ms
t_{INIT}	Time from power on to first command	10	--	10	--	ms

Notes:
Table is provided as a general reference. Consult JEDEC JC-42.4 TSE2004 for complete details.

3.3.2 EVENT_n Pin

The EVENT_n pin is an open drain output that requires a pull-up to VDDSPD on the system motherboard or integrated into the master controller. EVENT_n has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

In Interrupt Mode the EVENT_n pin will remain asserted until it is released by writing a '1' to the "Clear Event" bit in the Status Register. The value to write is independent of the EVENT_n polarity bit.

In Comparator Mode the EVENT_n pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Finally, in the TCRIT Only Mode the EVENT_n pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. Figure 5 illustrates the operation of the different modes over time and temperature

3.3.3 Address Mirroring

DDR4 RDIMMs will use address mirroring. Where possible SDRAMs for even ranks will be placed on the front side of the module. SDRAMs for odd ranks will be placed on the back side of the module. Wiring of the address bus will be as defined in Table.

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR4 SPD-TSE specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the odd ranks.

Signal Name	SDRAM Ball Label		Comment
Connector	Even Rank	Odd Rank	
A0	A0	A0	
A1	A1	A1	
A2	A2	A2	
A3	A3	A4	
A4	A4	A3	
A5	A5	A6	
A6	A6	A5	
A7	A7	A8	
A8	A8	A7	

A9	A9	Ag	
A10/AP	A10/AP	A10/AP	
A11	A11	A13	
A12/BC_n	A12/BC_n	A12/BC_n	
A13	A13	A11	
A14/WE_n	A14/WE_n	A14/WE_n	
A15/CAS_n	A15/CAS_n	A15/CAS_n	
A16/RAS_n	A16/RAS_n	A16/RAS_n	
A17	A17	A17	Only valid for x4 based DIMMs with SDRAMs components above 8 Gb.
BAO	BAO	BA1	
BA1	BA1	BA0	
BG0	BG0	BG1	
BG1	BG1	BG0	

3.3.4 SPD EEPROM Operation

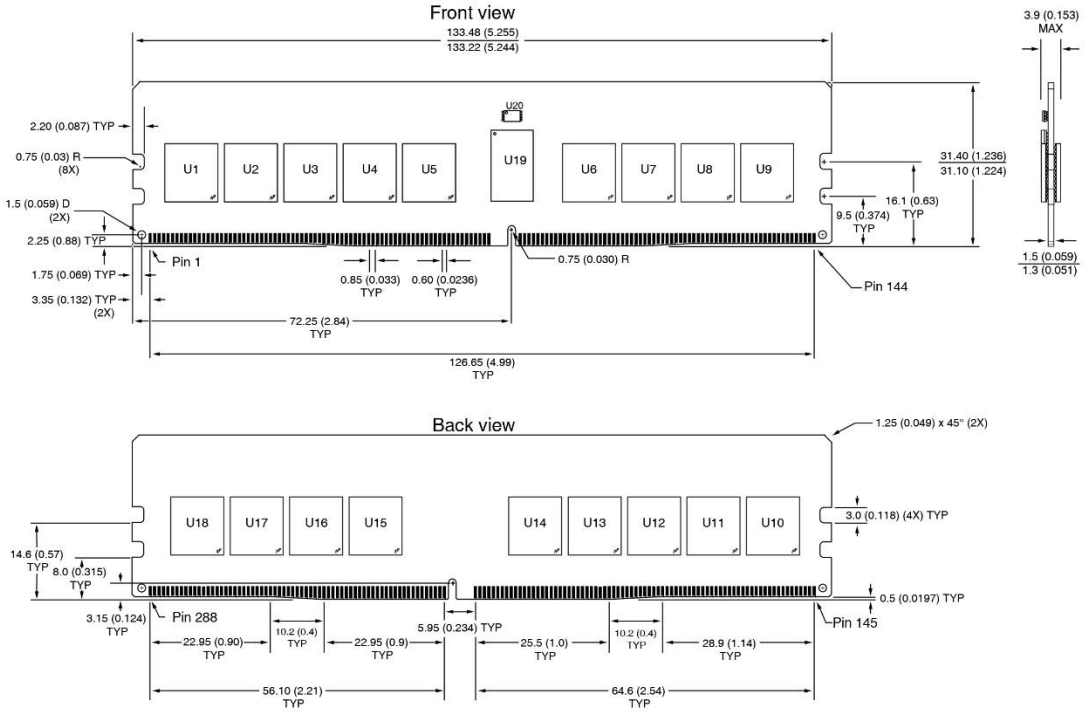
Consistent with the definition of DDR4 generation SPD devices (EE1004 and TSE2004) which have four individual write protection blocks of 128 bytes in length each, the SPD contents are aligned with these blocks as shown in the table below.

Block	Range		Description
0	0~127	0x000~0x07F	Base Configuration and DRAM Parameters
1	128~191	0x080~0x0BF	RDIMM Memory Module Type
	192~255	0x0C0~0x0FF	Unused
2	256~319	0x100~0x13F	Reserved
	320~383	0x140~0x17F	Module Supplier's Data
3	384~511	0x180~0x1FF	End User Programmable

Notes:

1. Table is provided as a general reference. Consult JEDEC JC-45 TSE2004 for complete detail

3.4. Module Dimensions



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.
3. Tolerance on all dimensions ±0.15mm unless otherwise specified.

4. Product Certifications

Certification	Logo	Country/Region/Company
RoHS		Europe
REACH		Europe
CE		Europe
WEEE		Europe
HF