Andrew Miller
M10180594
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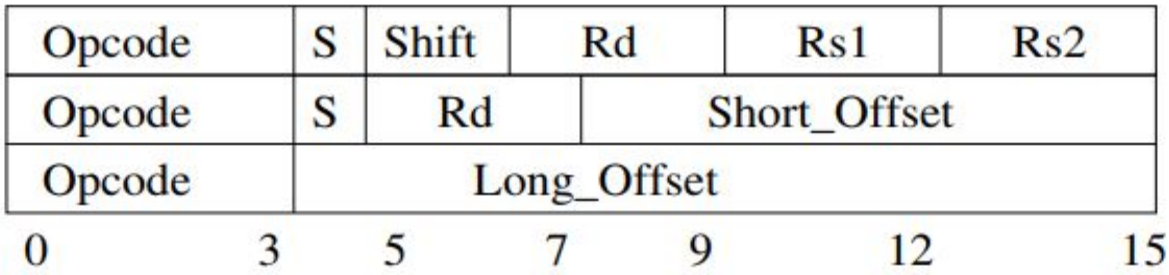
Introduction to Computer Architecture and Organization:
Project 3

The purpose of this project is to gain an understanding of the fundamental function of a control unit inside of a processor. Project 3 required a gate-level single bus implementation of a given instruction set:



Name	Opcode	Description
ADD	0	GPR[Rd] = GPR[Rs1] + left_shifted(GPR[Rs2],IR.Shift)
SUB	1	GPR[Rd] = GPR[Rs1] - left_shifted(GPR[Rs2],IR.Shift)
AND	2	GPR[Rd] = GPR[Rs1] **and** left_shifted(GPR[Rs2],IR.Shift)
SHL	3	GPR[Rd] = shift_left(GPR[Rs1]) by left_shifted(GPR[Rs2],IR.Shift)$_{3-0}$
SHRA	4	GPR[Rd] = shift_right(GPR[Rs1]) by left_shifted(GPR[Rs2],IR.Shift)$_{3-0}$
OR	5	GPR[Rd] = GPR[Rs1] **or** left_shifted(GPR[Rs2],IR.Shift)
NOT	6	GPR[Rd] = **not** MM[PC + Short_Offset]
LD	7	GPR[Rd] = MM[PC + Short_Offset]
ST	8	MM[PC + Short_Offset] = GPR[Rd]
BRN	9	if CC.N then PC = PC + Long_Offset
BRZ	10	if CC.Z then PC = PC + Long_Offset
BR	11	PC = PC + Long_Offset
JSR	12	GPR[Rd] = PC; PC = PC + Short_Offset
RTS	13	PC = GPR[Rd] + Short_Offset
CLK	14	Set timer to MM[PC + Long_Offset]
LPSW	15	PSW = MM[PC + Long_Offset]

The system is defined to have a 16-bit word size, single 16-bit bus, and byte addressable memory. The PSW Register contains two condition codes for use in branching operations, as well as the data that indicates the state of privileged mode or user mode. The General Purpose Registers (8) need to always hold 0 in GPR[0], and GPR[7] is the Program Counter. The control unit needs to respond to a timeout signal if it is not in privileged mode.

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Opcode and Control Signals Changes / Optimizations

Attached before this page are the handwritten control signals for each opcode in the instruction set. Several revisions were made during the process. Before the alteration of the project's constraints, the intent was to keep the shift signal for opcodes 3 and 4 away from the data bus by including a slave register in the implementation of Z and routing it back into the ALU as a shift control. It was determined that this would add too much hardware to the circuit to be worth saving a single clock cycle on the rare occasions that shifting is necessary.

Due to this problem, there are many alterations made to the signals to avoid sending the IR.Shift value onto the bus, which saved the first cycle in many cases. In the case of Long and Short Offset, a similar change was made and then revoked upon new understanding.

The configuration on these papers is not the final configuration of the opcodes, as a couple of them were shifted to be adjacent to similar operations to help ease the design process. Operations 12 and 13, using Short Offset, were relocated to be Op 9 and 10, while the original 9-11 operations translate to 11-13 now.

System Opcodes	
ADD	0000
SUB	0001
AND	0010
OR	0011
SHL	0100
SHRA	0101
NOT	0110
LD	0111
ST	1000
JSR	1001
RTS	1010
BRN	1011
BRZ	1100
BR	1101
CLK	1110
LPSW	1111

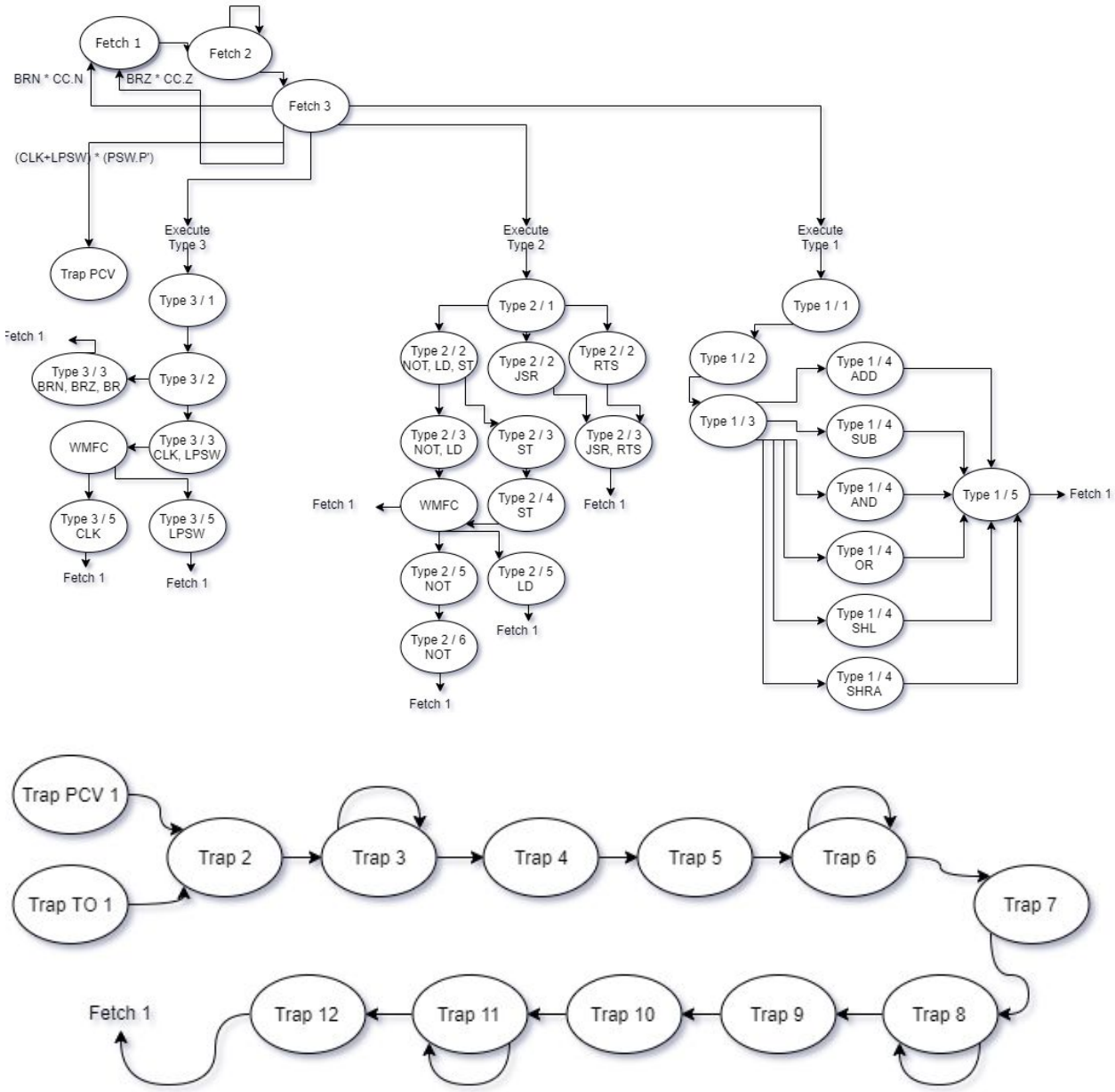
During the construction of the ALU, opcodes were created to note the operation for the ALU to execute. Originally, 8 operations were included for three instruction bits, but the design process revealed that an 9th operation (increment by 2) would be helpful, so it was added.

ALU Opcodes	
Operation	Code
inc	0000
inc2	0001
add	0010
sub	0011
and	0100
or	0101
not	0110
left_shift	0111
right_shift_A	1000

The Control Signals needed to be assigned a code to be represented with flip flops in the control unit. Because there were greater than 32 states, this called for six flip flops ($2^6 = 64$). Each unique set of signals was provided with a code, prioritizing the more common signal sets with the flip flop codes that include the least number of logical high bits.

Control Signals		
State Code	Control Signal	Diagram Representation
000000	PCOUT, MARIN, ALU/inc, Read_MM, ZIN	Fetch 1
000001	WFMC	WMFC
000010	ZOUT, GPR[IR.Rd]IN	T1/5, T2/6 NOT
000100	ZOUT, PCIN	T2/3 JRS RTS, T3/3 BRN BRZ BR
001000	PSWOUT, MDRIN, Write_MM	Trap 2
010000	WMFC, ZOUT, PCIN	Fetch 2
100000	MDROUT, IRIN	Fetch 3
000011	IR.Shift/out, GPR[IR.Rs2]OUT, ALU/left_shift, ZIN	T1/2
000101	ZOUT, YIN	T1/3
001001	GPR[IR.Rs1]OUT, ALU/add, ZIN	T1/4 ADD
010001	GPR[IR.Rs1]OUT, ALU/sub, ZIN	T1/4 SUB
100001	GPR[IR.Rs1]OUT, ALU/and, ZIN	T1/4 AND
000110	GPR[IR.Rs1]OUT, ALU/or, ZIN	T1/4 OR
001010	GPR[IR.Rs1]OUT, ALU/shift_left, ZIN	T1/4 SHL
010010	GPR[IR.Rs1]OUT, ALU/shift_right_A, ZIN	T1/4 SHRA
100010	IR.Short_OffsetOUT, YIN	T2/1
001100	PCOUT, ALU/add, ZIN	T2/2 NOT LD ST
010100	IR.Long_OffsetOUT, YIN	T3/1
100100	PCOUT, ALU/add, ZIN	T3/2
011000	ZOUT, MARIN, Read_MM	T2/3 NOT LD, T3/3 CLK LPSW
101000	ZOUT, MARIN	T2/3 ST
110000	MDROUT, ALU/not, ZIN	T2/5 NOT
000111	MDROUT, GPR[IR.Rd]IN	T2/5 LD
001011	MDRIN, GPR[IR.Rd]OUT, Write_MM	T2/4 ST
010011	PCOUT, GPR[IR.Rd]IN, ALU/add, ZIN	T2/2 JSR
100011	GPR[IR.Rd]OUT, ALU/add, ZIN	T2/2 RST
001101	MDROUT, TimerIN	T3/5 CLK
010101	MDROUT, PSWIN	T3/5 LPSW
100101	ROM[0]OUT, MARIN, ALU/inc2, ZIN	Trap PCV
011001	ROM[8]OUT, MARIN, ALU/inc2, ZIN	Trap TO
101001	PSWOUT, MDRIN, Write_MM	Tr2
110001	WMFC, ZOUT, PSWIN	Tr3
001110	PSWOUT, MARIN, ALU/inc2, ZIN	Tr4
010110	PCOUT, MDRIN, Write_MM	Tr5
100110	WMFC, ZOUT, PSWIN	Tr6
011010	PSWOUT, MARIN, Read_MM, ALU/inc2, ZIN	Tr7
101010	WMFC, ZOUT, PCIN	Tr8
110010	MDROUT, PSWIN	Tr9
011100	PCOUT, MARIN, Read_MM	Tr10
101100	WMFC	Tr11
110100	MDROUT, PCIN	Tr12

State Diagram:



Constructed with the use of the handwritten control signals, and used in construction of the current / next state table. Fetch 2 and trap states that loop back to themselves contain WMFC.

Current / Next State Table (V2)

Current/Next State Table	Current State						Inputs					Next State					
Notes	Q5	Q4	Q3	Q2	Q1	Q0	Opcode	N	Z	P	MFC	Q5	Q4	Q3	Q2	Q1	Q0
F1 -> F2	0	0	0	0	0	0	x	x	x	x	x	0	1	0	0	0	0
F2 -> F2	0	1	0	0	0	0	x	x	x	x	0	0	1	0	0	0	0
F2 -> F3	0	1	0	0	0	0	x	x	x	x	1	1	0	0	0	0	0
F3 -> T1/2	1	0	0	0	0	0	0-5	x	x	x	x	0	0	0	0	1	1
T1/2 -> T1/3	0	0	0	0	1	1	x	x	x	x	x	0	0	0	1	0	1
T1/3 -> T1/4 ADD	0	0	0	1	0	1	0	x	x	x	x	0	0	1	0	0	1
T1/3 -> T1/4 SUB	0	0	0	1	0	1	1	x	x	x	x	0	1	0	0	0	1
T1/3 -> T1/4 AND	0	0	0	1	0	1	2	x	x	x	x	1	0	0	0	0	1
T1/3 -> T1/4 OR	0	0	0	1	0	1	3	x	x	x	x	0	0	0	1	1	0
T1/3 -> T1/4 SHL	0	0	0	1	0	1	4	x	x	x	x	0	0	1	0	1	0
T1/3 -> T1/4 SHRA	0	0	0	1	0	1	5	x	x	x	x	0	1	0	0	1	0
T1/4 ADD -> T1/5	0	0	1	0	0	1	x	x	x	x	x	0	0	0	0	1	0
T1/4 SUB -> T1/5	0	1	0	0	0	1	x	x	x	x	x	0	0	0	0	1	0
T1/4 AND -> T1/5	1	0	0	0	0	1	x	x	x	x	x	0	0	0	0	1	0
T1/4 OR -> T1/5	0	0	0	1	1	0	x	x	x	x	x	0	0	0	0	1	0
T1/4 SHL -> T1/5	0	0	1	0	1	0	x	x	x	x	x	0	0	0	0	1	0
T1/4 SHRA -> T1/5	0	1	0	0	1	0	x	x	x	x	x	0	0	0	0	1	0
T1/5 -> F1	0	0	0	0	1	0	x	x	x	x	x	0	0	0	0	0	0
F3 -> T2/1	1	0	0	0	0	0	6-10	x	x	x	x	1	0	0	0	1	0
T2/1 -> T2/2 Op6-8	1	0	0	0	1	0	6-8	x	x	x	x	0	0	1	1	0	0
T2/1 -> T2/2 Op9	1	0	0	0	1	0	9	x	x	x	x	0	1	0	0	1	1
T2/1 -> T2/2 Op10	1	0	0	0	1	0	10	x	x	x	x	1	0	0	0	1	1
T2/2 Op6-8 -> T2/3 Op6-7	0	0	1	1	0	0	6-7	x	x	x	x	0	1	1	0	0	0
T2/2 Op6-8 -> T2/3 Op8	0	0	1	1	0	0	8	x	x	x	x	1	0	1	0	0	0
T2/2 Op9 -> T2/3 Op9-10	0	1	0	0	1	1	x	x	x	x	x	0	0	0	1	0	0
T2/2 Op10 -> T2/3 Op9-10	1	0	0	0	1	1	x	x	x	x	x	0	0	0	1	0	0
T2/3 Op6-7 -> WMFC	0	1	1	0	0	0	x	x	x	x	x	0	0	0	0	0	1
T2/3 Op8 -> T2/4 Op8	1	0	1	0	0	0	x	x	x	x	x	0	0	1	0	1	1
T2/3 Op9-10 -> F1	0	0	0	1	0	0	x	x	x	x	x	0	0	0	0	0	0
T2/4 Op8 -> WMFC	0	0	1	0	1	1	x	x	x	x	x	0	0	0	0	0	1
WMFC -> F1	0	0	0	0	0	1	8	x	x	x	1	0	0	0	0	0	0
WMFC -> T2/5 Op6	0	0	0	0	0	1	6	x	x	x	1	1	1	0	0	0	0
WMFC -> T2/5 Op7	0	0	0	0	0	1	7	x	x	x	1	0	0	0	1	1	1
WMFC -> WMFC	0	0	0	0	0	1	x	x	x	x	0	0	0	0	0	0	1

T2/5 Op6 -> T2/6	1	1	0	0	0	0	x	x	x	x	x	0	0	0	0	1	0
T2/5 Op7 -> F1	0	0	0	1	1	1	x	x	x	x	x	0	0	0	0	0	0
T2/6 -> F1	0	0	0	0	1	0	x	x	x	x	x	0	0	0	0	0	0
F3 -> T3/1	1	0	0	0	0	0	11	1	x	x	x	0	1	0	1	0	0
F3 -> T3/1	1	0	0	0	0	0	12	x	1	x	x	0	1	0	1	0	0
F3 -> T3/1	1	0	0	0	0	0	13	x	x	x	x	0	1	0	1	0	0
F3 -> T3/1	1	0	0	0	0	0	14-15	x	x	1	x	0	1	0	1	0	0
F3 -> Trap PCV 1	1	0	0	0	0	0	14-15	x	x	0	x	1	0	0	1	0	1
F3 -> F1	1	0	0	0	0	0	11	0	x	x	x	0	0	0	0	0	0
F3 -> F1	1	0	0	0	0	0	12	x	0	x	x	0	0	0	0	0	0
T3/1 -> T3/2	0	1	0	1	0	0	x	x	x	x	x	1	0	0	1	0	0
T3/2 -> T3/3 Op11-13	1	0	0	1	0	0	11-13	x	x	x	x	0	0	0	1	0	0
T3/2 -> T3/3 Op14-15	1	0	0	1	0	0	14-15	x	x	x	x	0	1	1	0	0	0
T3/3 Op11-13 -> F1	0	0	0	1	0	0	x	x	x	x	x	0	0	0	0	0	0
T3/3 Op14-15 -> WMFC	0	1	1	0	0	0	x	x	x	x	x	0	0	0	0	0	1
WMFC -> T3/5 Op14	0	0	0	0	0	1	14	x	x	x	1	0	0	1	1	0	1
WMFC -> T3/5 Op15	0	0	0	0	0	1	15	x	x	x	1	0	1	0	1	0	1
T3/5 Op14 -> F1	0	0	1	1	0	1	x	x	x	x	x	0	0	0	0	0	0
T3/5 Op15 -> F1	0	1	0	1	0	1	x	x	x	x	x	0	0	0	0	0	0
Trap PCV 1 -> Tr2	1	0	0	1	0	1	x	x	x	x	x	1	0	1	0	0	1
Trap TO 1 -> Tr2	0	1	1	0	0	1	x	x	x	x	x	1	0	1	0	0	1
Tr2 -> Tr3	1	0	1	0	0	1	x	x	x	x	x	1	1	0	0	0	1
Tr3 -> Tr3	1	1	0	0	0	1	x	x	x	x	0	1	1	0	0	0	1
Tr3 -> Tr4	1	1	0	0	0	1	x	x	x	x	1	0	0	1	1	1	0
Tr4 -> Tr5	0	0	1	1	1	0	x	x	x	x	x	0	1	0	1	1	0
Tr5 -> Tr6	0	1	0	1	1	0	x	x	x	x	x	1	0	0	1	1	0
Tr6 -> Tr6	1	0	0	1	1	0	x	x	x	x	0	1	0	0	1	1	0
Tr6 -> Tr7	1	0	0	1	1	0	x	x	x	x	1	0	1	1	0	1	0
Tr7 -> Tr8	0	1	1	0	1	0	x	x	x	x	x	1	0	1	0	1	0
Tr8 -> Tr8	1	0	1	0	1	0	x	x	x	x	0	1	0	1	0	1	0
Tr8 -> Tr9	1	0	1	0	1	0	x	x	x	x	1	1	1	0	0	1	0
Tr9 -> Tr10	1	1	0	0	1	0	x	x	x	x	x	0	1	1	1	0	0
Tr10 -> Tr11	0	1	1	1	0	0	x	x	x	x	x	1	0	1	1	0	0
Tr11 -> Tr11	1	0	1	1	0	0	x	x	x	x	0	1	0	1	1	0	0
Tr11 -> Tr12	1	0	1	1	0	0	x	x	x	x	1	1	1	0	1	0	0
Tr12 -> F1	1	1	0	1	0	0	x	x	x	x	x	0	0	0	0	0	0
ANYTHING -> Trap TO 1	x	x	x	x	x	x	Timer counts to zero					0	1	1	0	0	1

Trap states are unique from non-traps because they can occur with any opcode 0-13.

Simplification of Input Equations

Flip Flop Input D0:

	Original Terms	Simplification Process---->				
Equation Age	Generation 1	Generation 2 (Group by Q5 + Q5')	Generation 3 (Group by Q4 + Q4')	Generation 4 (Group by Q3 + Q3')	Generation 5 (Group by Q2 + Q2')	Generation 6 (Small groups)
Term 1	Q5Q4'Q3'Q2'Q1'Q0'Op0-5	Q4'Q3'Q2'Q1Q0	Q3'Q2'Q1Q0	Q2'Q1Q0	Q1Q0	
Term 2	Q5'Q4'Q3'Q2'Q1Q0	Q4'Q3'Q2Q1'Q0Op0-2	Q3'Q2Q1'Q0Op0-2	Q2Q1'Q0Op0-2	Q1'Q0Op7 MFC	
Term 3	Q5'Q4'Q3'Q2Q1'Q0Op0-2	Q4Q3Q2'Q1'Q0'	Q3Q2'Q1Q0	Q2'Q1'Q0Op7 MFC	Q1'Q0 MFC'	
Term 4	Q5Q4'Q3'Q2'Q1Q0'Op9-10	Q4'Q3Q2'Q1Q0	Q3'Q2'Q1'Q0Op7 MFC	Q2'Q1'Q0 MFC'	Q1'Q0Op14-15 MFC	Q0(Q1 + MFC' + Op7+14+15)
Term 5	Q5'Q4Q3Q2'Q1'Q0'	Q4'Q3'Q2'Q1'Q0Op7 MFC	Q3'Q2'Q1'Q0 MFC'	Q2'Q1'Q0Op14-15 MFC	Q1'Q0Op0-2	Q1'Q0Op0+1+2
Term 6	Q5Q4'Q3Q2'Q1'Q0'	Q4'Q3'Q2'Q1'Q0 MFC'	Q3'Q2'Q1'Q0Op14-15 MFC	Q2'Q1Q0	Q1Q0	Q1Q0
Term 7	Q5'Q4'Q3Q2'Q1Q0	Q4Q3Q2'Q1'Q0'	Q3Q2'Q1'Q0'	Q2'Q1'Q0'	Q1'Q0'	
Term 8	Q5'Q4'Q3'Q2'Q1'Q0Op7 MFC	Q4'Q3'Q2'Q1'Q0Op14-15 MFC	Q3Q2'Q1'Q0'	Q2'Q1'Q0'	Q1'Q0'	
Term 9	Q5'Q4'Q3'Q2'Q1'Q0 MFC'	Q4Q3Q2'Q1'Q0	Q3Q2'Q1'Q0	Q2'Q1'Q0	Q1'Q0	Q1'
Term 10	Q5Q4'Q3'Q2'Q1'Q0'Op14-15 P'	Q4'Q3'Q2'Q1'Q0'Op0-5	Q3'Q2'Q1'Q0'Op0-5	Q2'Q1'Q0'Op0-5	Q1'Q0'Op0-5	
Term 11	Q5'Q4Q3Q2'Q1'Q0'	Q4'Q3'Q2'Q1Q0'Op9-10	Q3'Q2'Q1Q0'Op9-10	Q2'Q1Q0'Op9-10	Q1Q0'Op9-10	Q0'(Q1Op9+10 + Q1'(Op0-5 + (Op14+15 P')))
Term 12	Q5'Q4'Q3'Q2'Q1'Q0Op14-15 MFC	Q4'Q3Q2'Q1'Q0'	Q3Q2'Q1'Q0'	Q2'Q1'Q0'Op14-15 P'	Q1'Q0'Op14-15 P'	
Term 13	Q5Q4'Q3'Q2Q1'Q0	Q4'Q3'Q2'Q1'Q0'Op14-15 P'	Q3'Q2'Q1'Q0'Op14-15 P'	Q2Q1'Q0	Q1'Q0	Q1'Q0
Term 14	Q5'Q4Q3Q2'Q1'Q0	Q4'Q3'Q2Q1'Q0	Q3'Q2Q1'Q0	Q2'Q1'Q0'	Q1'Q0'	
Term 15	Q5Q4'Q3Q2'Q1'Q0	Q4'Q3Q2'Q1'Q0	Q3Q2'Q1'Q0	Q2'Q1'Q0	Q1'Q0	Q1'
Term 16	Q5Q4Q3'Q2'Q1'Q0 MFC'	Q4Q3'Q2'Q1'Q0 MFC'	Q3'Q2'Q1'Q0 MFC'	Q2'Q1'Q0 MFC'	Q1'Q0 MFC'	Q1'Q0MFC'

Final Equation: D0 = Q5(Q4Q3'Q2'Q1'Q0MFC' + Q4'(Q3Q2'Q1' + Q3'(Q2Q1'Q0 + Q2'(Q0'(Q1Op9+10 + Q1'(Op0-5 + (Op14+15 P')))))) + Q5'(Q4Q3Q2'Q1' + Q4'(Q3Q2'Q1Q0 + Q3'(Q2Q1'Q0Op0+1+2 + Q2'Q0(Q1 + MFC' + Op7+14+15))))

Flip Flop Input D1:

	Original Terms	Simplification Process---->			
Equation Age	Generation 1	Generation 2 (Group by Q5 + Q5')	Generation 3 (Group by Q4 + Q4')	Generation 4 (Group by Q3 + Q3')	Generation 5 (General Simplification)
Term 1	Q5Q4'Q3'Q2'Q1'Q0'Op0-5	Q4'Q3'Q2Q1'Q0Op3-5	Q3'Q2Q1'Q0Op3-5	Q2Q1'Q0Op3-5	
Term 2	Q5'Q4'Q3'Q2Q1'Q0Op3-5	Q4'Q3'Q2'Q1'Q0	Q3'Q2'Q1'Q0	Q2'Q1'Q0	
Term 3	Q5'Q4'Q3'Q2'Q1'Q0	Q4Q3'Q2'Q1'Q0	Q3'Q2Q1Q0'	Q2Q1Q0'	
Term 4	Q5'Q4Q3'Q2'Q1'Q0	Q4'Q3'Q2Q1Q0'	Q3Q2'Q1Q0'	Q2'Q1'Q0Op7 MFC	Q2(Q1'Q0Op3+4+5 + Q1Q0') + Q2'Q1'Q0
Term 5	Q5Q4'Q3'Q2'Q1'Q0	Q4'Q3Q2'Q1Q0'	Q3'Q2'Q1'Q0Op7 MFC	Q2'Q1Q0'	
Term 6	Q5'Q4'Q3'Q2Q1Q0'	Q4Q3'Q2'Q1Q0'	Q3Q2Q1Q0'	Q2Q1Q0'	Q1Q0'
Term 7	Q5'Q4'Q3Q2'Q1Q0'	Q4'Q3'Q2'Q1'Q0Op7 MFC	Q3'Q2'Q1'Q0	Q2'Q1'Q0	
Term 8	Q5'Q4Q3'Q2'Q1Q0'	Q4'Q3Q2Q1Q0'	Q3'Q2'Q1Q0'	Q2'Q1Q0'	
Term 9	Q5Q4'Q3'Q2'Q1'Q0'Op6-10	Q4Q3'Q2Q1Q0'	Q3'Q2Q1Q0'	Q2Q1Q0'	Q2'Q1'Q0 + Q1Q0'
Term 10	Q5Q4'Q3'Q2'Q1Q0'Op9+10	Q4Q3Q2'Q1Q0'	Q3Q2'Q1Q0'	Q2'Q1Q0'	Q2'Q1Q0'
Term 11	Q5Q4'Q3Q2'Q1'Q0'	Q4'Q3'Q2'Q1'Q0'Op0-5	Q3'Q2'Q1'Q0'Op0-5	Q2'Q1'Q0'Op0-5	
Term 12	Q5'Q4'Q3'Q2'Q1'Q0Op7 MFC	Q4'Q3'Q2'Q1'Q0	Q3'Q2'Q1'Q0	Q2'Q1'Q0	
Term 13	Q5Q4Q3'Q2'Q1'Q0'	Q4'Q3'Q2'Q1'Q0'Op6-10	Q3'Q2'Q1'Q0'Op6-10	Q2'Q1'Q0'Op6-10	
Term 14	Q5Q4Q3'Q2'Q1'Q0 MFC	Q4'Q3'Q2'Q1Q0'Op9+10	Q3'Q2'Q1Q0'Op9+10	Q2'Q1Q0'Op9+10	
Term 15	Q5'Q4'Q3Q2Q1Q0'	Q4'Q3Q2'Q1'Q0'	Q3Q2'Q1'Q0'	Q2Q1Q0'	Q2Q1Q0' + Q2'(Q1'Q0 + Q1'Q0'Op0-10 + Q1Q0'Op9+10)
Term 16	Q5'Q4Q3'Q2Q1Q0'	Q4Q3'Q2'Q1'Q0'	Q3'Q2Q1Q0'	Q2'Q1'Q0'	
Term 17	Q5Q4'Q3'Q2Q1Q0'	Q4Q3'Q2'Q1'Q0 MFC	Q3Q2'Q1Q0'	Q2'Q1Q0'	Q2'Q0'
Term 18	Q5'Q4Q3Q2'Q1Q0'	Q4'Q3'Q2Q1Q0'	Q3'Q2'Q1'Q0'	Q2'Q1'Q0'	
Term 19	Q5Q4'Q3Q2'Q1Q0'	Q4'Q3Q2'Q1Q0'	Q3'Q2'Q1'Q0 MFC	Q2'Q1'Q0 MFC	Q2'Q1'(Q0' + MFC)

Final Equation: D1 = Q5(Q4Q3'Q2'Q1'(Q0' + MFC) + Q4'(Q3Q2'Q0' + Q3'(Q2Q1Q0' + Q2'(Q1'Q0 + Q1'Q0'Op0-10 + Q1Q0'Op9+10)))) + Q5'(Q4(Q3Q2'Q1Q0' + Q3'(Q2'Q1'Q0 + Q1Q0')) + Q4'(Q3Q1Q0' + Q3'Q2(Q1'Q0Op3+4+5 + Q1Q0') + Q2'Q1'Q0))

Flip Flop Input D2:

	Original Terms	Simplification Process---->			
Equation Age	Generation 1	Generation 2 (Group by Q5 + Q5')	Generation 3 (Group by Q4 + Q4')	Generation 4 (Group by Q3 + Q3')	Generation 5 (General Simplification)
Term 1	Q5'Q4'Q3'Q2'Q1Q0	Q4'Q3'Q2'Q1Q0	Q3'Q2'Q1Q0	Q2'Q1Q0	
Term 2	Q5'Q4'Q3'Q2Q1'Q0 Op3	Q4'Q3'Q2Q1'Q0 Op3	Q3'Q2Q1'Q0 Op3	Q2Q1'Q0 Op3	
Term 3	Q5Q4'Q3'Q2'Q1Q0' Op6-8	Q4Q3'Q2'Q1Q0	Q3'Q2'Q1'Q0Op7 MFC	Q2'Q1'Q0Op7 MFC	
Term 4	Q5'Q4Q3'Q2'Q1Q0	Q4'Q3'Q2'Q1'Q0Op7 MFC	Q3'Q2'Q1'Q0 Op14+15 MFC	Q2'Q1'Q0 Op14+15 MFC	Q2'(Q1Q0 + Q0MFC(Op7 + Op14+15)) + Q2Q1'Q0Op3
Term 5	Q5Q4'Q3'Q2'Q1Q0	Q4Q3'Q2Q1'Q0'	Q3Q2Q1Q0'	Q2Q1Q0'	Q2Q1Q0'
Term 6	Q5'Q4'Q3'Q2'Q1'Q0Op7 MFC	Q4'Q3'Q2'Q1'Q0 Op14+15 MFC	Q3'Q2'Q1Q0	Q2'Q1Q0	
Term 7	Q5Q4'Q3'Q2'Q1'Q0' Op11 N	Q4'Q3Q2Q1Q0'	Q3'Q2Q1'Q0'	Q2Q1'Q0'	
Term 8	Q5Q4'Q3'Q2'Q1'Q0' Op12 Z	Q4Q3'Q2Q1Q0'	Q3'Q2Q1Q0'	Q2Q1Q0'	
Term 9	Q5Q4'Q3'Q2'Q1'Q0' Op13-15	Q4Q3Q2Q1'Q0'	Q3Q2Q1'Q0'	Q2Q1'Q0'	Q2Q0' + Q2'Q1Q0
Term 10	Q5'Q4Q3'Q2Q1'Q0'	Q4'Q3'Q2'Q1Q0' Op6-8	Q3'Q2'Q1Q0' Op6-8	Q2Q1'Q0'	Q2Q1'Q0'
Term 11	Q5Q4'Q3'Q2Q1'Q0' Op11-13	Q4'Q3'Q2'Q1Q0	Q3'Q2'Q1Q0	Q2'Q1Q0' Op6-8	
Term 12	Q5'Q4'Q3'Q2'Q1'Q0 Op14+15 MFC	Q4'Q3'Q2'Q1'Q0' Op11 N	Q3'Q2'Q1'Q0' Op11 N	Q2'Q1Q0	
Term 13	Q5Q4Q3'Q2'Q1'Q0 MFC	Q4'Q3'Q2'Q1'Q0' Op12 Z	Q3'Q2'Q1'Q0' Op12 Z	Q2'Q1'Q0' Op11 N	
Term 14	Q5'Q4'Q3Q2Q1Q0'	Q4'Q3'Q2'Q1'Q0' Op13-15	Q3'Q2'Q1'Q0' Op13-15	Q2'Q1'Q0' Op12 Z	
Term 15	Q5'Q4Q3'Q2Q1Q0'	Q4'Q3'Q2Q1'Q0' Op11-13	Q3'Q2Q1'Q0' Op11-13	Q2'Q1'Q0' Op13-15	
Term 16	Q5Q4'Q3'Q2Q1Q0'	Q4Q3'Q2'Q1'Q0 MFC	Q3'Q2Q1Q0'	Q2Q1'Q0' Op11-13	Q2Q0'(Q1 + Op11-13) + Q2'(Q1(Q0 + Op6-8) + Q1'Q0'(Op11 N + Op12 Z + Op13-15))
Term 17	Q5Q4Q3'Q2'Q1Q0'	Q4'Q3'Q2Q1Q0'	Q3Q2Q1'Q0'	Q2Q1Q0'	
Term 18	Q5'Q4Q3Q2Q1'Q0'	Q4Q3'Q2'Q1Q0'	Q3'Q2'Q1'Q0 MFC	Q2'Q1'Q0 MFC	
Term 19	Q5Q4'Q3Q2Q1'Q0'	Q4'Q3Q2Q1'Q0'	Q3'Q2'Q1Q0'	Q2Q1Q0'	Q2'(Q1'Q0MFC + Q1Q0')

Final Equation: D2 = Q5(Q4Q3'Q2'(Q1'Q0MFC + Q1Q0') + Q4'(Q3Q2Q1'Q0' + Q3'(Q2Q0'(Q1 + Op11-13) + Q2'(Q1(Q0 + Op6-8) + Q1'Q0'(Op11 N + Op12 Z + Op13-15))))) + Q5'(Q4Q3'(Q2Q0' + Q2'Q1Q0) + Q4'(Q3Q2Q1Q0' + Q3'(Q2'(Q1Q0 + Q0MFC(Op7 + Op14+15)) + Q2Q1'Q0Op3))

	Flip Flop Input D3:				
	Original Terms	Simplification Process---->			
Equation Age	Generation 1	Generation 2 (Group by Q5 + Q5')	Generation 3 (Group by Q4 + Q4')	Generation 4 (Group by Q3 + Q3')	Generation 5 (General Simplification)
Term 1	Q5'Q4'Q3'Q2'Q1'Q0 Op0+4	Q4'Q3'Q2Q1'Q0 Op0+4	Q3'Q2Q1'Q0 Op0+4	Q2Q1'Q0 Op0+4	
Term 2	Q5Q4'Q3'Q2'Q1Q0' Op6-8	Q4'Q3'Q2'Q1'Q0 Op14 MFC	Q3'Q2'Q1'Q0 Op14 MFC	Q2'Q1'Q0 Op14 MFC	Q1'Q0(Q2Op0+4 + Q2'Op14MFC)
Term 3	Q5Q4'Q3Q2'Q1'Q0'	Q4Q3Q2'Q1'Q0	Q3Q2'Q1'Q0	Q2'Q1'Q0	
Term 4	Q5Q4'Q3'Q2Q1'Q0' Op14-15	Q4Q3Q2'Q1Q0'	Q3Q2'Q1Q0'	Q2'Q1Q0'	
Term 5	Q5'Q4'Q3'Q2'Q1'Q0 Op14 MFC	Q4Q3Q2Q1'Q0'	Q3Q2Q1'Q0'	Q2Q1'Q0'	Q2Q1'Q0' + Q2'(Q1 XOR Q0)
Term 6	Q5Q4'Q3Q2Q1'Q0	Q4'Q3'Q2'Q1Q0' Op6-8	Q3'Q2'Q1Q0' Op6-8	Q2'Q1Q0' Op6-8	
Term 7	Q5'Q4Q3Q2'Q1'Q0	Q4'Q3Q2'Q1'Q0'	Q3Q2'Q1'Q0'	Q2'Q1'Q0'	
Term 8	Q5Q4Q3'Q2'Q1'Q0 MFC	Q4'Q3'Q2Q1'Q0' Op14-15	Q3'Q2Q1'Q0' Op14-15	Q2Q1'Q0' Op14-15	Q0'(Q2'(Q1' + Op6+7+8) + Q2Q1'Op14+15)
Term 9	Q5Q4'Q3'Q2Q1Q0' MFC	Q4'Q3Q2Q1'Q0	Q3Q2Q1'Q0	Q2Q1'Q0	
Term 10	Q5'Q4Q3Q2'Q1Q0'	Q4Q3'Q2'Q1'Q0 MFC	Q3'Q2Q1Q0' MFC	Q2Q1Q0' MFC	
Term 11	Q5Q4'Q3Q2'Q1Q0' MFC'	Q4'Q3'Q2Q1Q0' MFC	Q3Q2'Q1Q0' MFC'	Q2'Q1Q0' MFC'	
Term 12	Q5Q4Q3'Q2'Q1Q0'	Q4'Q3Q2'Q1Q0' MFC'	Q3Q2Q1'Q0' MFC'	Q2Q1'Q0' MFC'	Q2(Q1'(Q0 + MFC') + Q1Q0MFC) + Q2'Q1Q0'MFC'
Term 13	Q5'Q4Q3Q2Q1'Q0'	Q4Q3'Q2'Q1Q0'	Q3'Q2'Q1Q0'	Q2'Q1Q0'	
Term 14	Q5Q4'Q3Q2Q1'Q0' MFC'	Q4'Q3Q2Q1'Q0' MFC'	Q3'Q2'Q1'Q0 MFC	Q2'Q1'Q0 MFC	Q2'(Q1Q0' + Q1'Q0MFC)
Final Equation:	D3 = Q5(Q4Q3'Q2'(Q1Q0' + Q1'Q0MFC) + Q4'(Q3(Q2(Q1'(Q0 + MFC') + Q1Q0MFC) + Q2'Q1Q0'MFC') + Q3'Q0'(Q2'(Q1' + Op6+7+8) + Q2Q1'Op14+15))) + Q5'(Q4Q3(Q2Q1'Q0' + Q2'(Q1 XOR Q0)) + Q4'Q3'Q1'Q0(Q2Op0+4 + Q2'Op14MFC))				

	Flip Flop Input D4:				
	Original Terms	Simplification Process---->			
Equation Age	Generation 1	Generation 2 (Group by Q5 + Q5')	Generation 3 (Group by Q4 + Q4')	Generation 4 (Group by Q3 + Q3')	Generation 5 (General Simplification)
Term 1	Q5'Q4'Q3'Q2'Q1'Q0'	Q4'Q3'Q2'Q1'Q0'	Q3'Q2'Q1'Q0'	Q2'Q1'Q0'	
Term 2	Q5'Q4Q3'Q2'Q1'Q0' MFC'	Q4Q3'Q2'Q1'Q0' MFC'	Q3'Q2Q1'Q0Op1+5	Q2Q1'Q0Op1+5	
Term 3	Q5'Q4'Q3'Q2Q1'Q0Op1+5	Q4'Q3'Q2Q1'Q0Op1+5	Q3Q2Q1'Q0'Op6+7	Q2'Q1'Q0Op6 MFC	
Term 4	Q5Q4'Q3'Q2'Q1Q0'Op9	Q4'Q3Q2Q1'Q0'Op6+7	Q3'Q2'Q1'Q0Op6 MFC	Q2'Q1'Q0Op15 MFC	Q1'(Q2'Q0' + Q2'MFC(Op6+15) + Q2Q0Op1+5)
Term 5	Q5'Q4'Q3Q2Q1'Q0'Op6+7	Q4'Q3'Q2'Q1'Q0Op6 MFC	Q3'Q2'Q1'Q0Op15 MFC	Q2Q1'Q0'Op6+7	
Term 6	Q5'Q4'Q3'Q2'Q1'Q0Op6 MFC	Q4'Q3'Q2'Q1'Q0Op15 MFC	Q3Q2Q1Q0'	Q2Q1Q0'	Q2Q0'(Q1 + (Op6+7))
Term 7	Q5Q4'Q3'Q2'Q1'Q0'Op11 N	Q4'Q3Q2Q1Q0'	Q3'Q2'Q1'Q0' MFC'	Q2'Q1'Q0' MFC'	Q2'Q1'Q0'MFC'
Term 8	Q5Q4'Q3'Q2'Q1'Q0'Op12 Z	Q4'Q3'Q2'Q1Q0'Op9	Q3'Q2'Q1Q0'Op9	Q2'Q1Q0'Op9	
Term 9	Q5Q4'Q3'Q2'Q1'Q0'Op13	Q4'Q3'Q2'Q1'Q0'Op11 N	Q3'Q2'Q1'Q0'Op11 N	Q2'Q1'Q0'Op11 N	
Term 10	Q5Q4'Q3'Q2'Q1'Q0'Op14+15 P	Q4'Q3'Q2'Q1'Q0'Op12 Z	Q3'Q2'Q1'Q0'Op12 Z	Q2'Q1'Q0'Op12 Z	
Term 11	Q5Q4'Q3'Q2Q1'Q0'Op14+15	Q4'Q3'Q2'Q1'Q0'Op13	Q3'Q2'Q1'Q0'Op13	Q2'Q1'Q0'Op13	
Term 12	Q5'Q4'Q3'Q2'Q1'Q0Op15 MFC	Q4'Q3'Q2'Q1'Q0'Op14+15 P	Q3'Q2'Q1'Q0'Op14+15 P	Q2'Q1'Q0'Op14+15 P	
Term 13	Q5Q4'Q3Q2'Q1'Q0	Q4'Q3'Q2Q1'Q0'Op14+15	Q3'Q2Q1'Q0'Op14+15	Q2Q1'Q0'Op14+15	Q2Q0'(Q1MFC + Q1'Op14+15) + Q2'Q0'(Q1Op9 + Op11N + Op12Z + Op13 + Op(14+15)P)
Term 14	Q5Q4Q3'Q2'Q1'Q0	Q4'Q3Q2'Q1'Q0	Q3Q2'Q1'Q0	Q2Q1Q0' MFC	
Term 15	Q5'Q4'Q3Q2Q1Q0'	Q4Q3'Q2'Q1'Q0	Q3'Q2Q1Q0' MFC	Q2'Q1'Q0	
Term 16	Q5Q4'Q3'Q2Q1Q0' MFC	Q4'Q3'Q2Q1Q0' MFC	Q3Q2'Q1Q0' MFC	Q2'Q1Q0' MFC	
Term 17	Q5Q4'Q3Q2'Q1Q0' MFC	Q4'Q3Q2'Q1Q0' MFC	Q3Q2Q1'Q0' MFC	Q2Q1'Q0' MFC	Q2'(Q1'Q0 + Q1Q0'MFC) + Q2Q1'Q0'MFC
Term 18	Q5Q4Q3'Q2'Q1Q0'	Q4Q3'Q2'Q1Q0'	Q3'Q2'Q1'Q0	Q2'Q1'Q0	
Term 19	Q5Q4'Q3Q2Q1'Q0' MFC	Q4'Q3Q2Q1'Q0' MFC	Q3'Q2'Q1Q0'	Q2'Q1Q0'	Q2'(Q1 XOR Q0)
Final Equation:	D4 = Q5(Q4Q3'Q2'(Q1 XOR Q0) + Q4'(Q3(Q2'(Q1'Q0 + Q1Q0'MFC) + Q2Q1'Q0'MFC) + Q3'(Q2Q0'(Q1MFC + Q1'Op14+15) + Q2'Q0'(Q1Op9 + Op11N + Op12Z + Op13 + Op(14+15)P)))) + Q5'(Q4Q3'Q2'Q1'Q0'MFC' + Q4'(Q3Q2Q0'(Q1 + (Op6+7)) + Q3'(Q1'(Q2'Q0' + Q2'MFC(Op6+15)) + Q2Q0Op1+5)))				

	Flip Flop Input D5:				
	Original Terms	Simplification Process---->			
Equation Age	Generation 1	Generation 2 (Group by Q5 + Q5')	Generation 3 (Group by Q4 + Q4')	Generation 4 (Group by Q3 + Q3')	Generation 5 (General Simplification)
Term 1	Q5'Q4Q3'Q2'Q1'Q0' MFC	Q4Q3'Q2'Q1'Q0' MFC	Q3'Q2Q1'Q0Op2	Q2'Q1'Q0Op6 MFC	
Term 2	Q5'Q4'Q3'Q2Q1'Q0Op2	Q4'Q3'Q2Q1'Q0Op2	Q3Q2Q1'Q0'Op8	Q2Q1'Q0Op2	Q1'Q0(Q2Op2 + Q2'Op6MFC)
Term 3	Q5Q4'Q3'Q2'Q1'Q0'Op6-10	Q4'Q3Q2Q1'Q0'Op8	Q3'Q2'Q1'Q0Op6 MFC	Q2Q1'Q0'Op8	Q2Q1'Q0'Op8
Term 4	Q5Q4'Q3'Q2'Q1Q0'Op10	Q4'Q3'Q2'Q1'Q0Op6 MFC	Q3'Q2'Q1'Q0' MFC	Q2'Q1'Q0' MFC	
Term 5	Q5'Q4'Q3Q2Q1'Q0'Op8	Q4Q3'Q2Q1'Q0'	Q3'Q2Q1'Q0'	Q2Q1'Q0'	
Term 6	Q5'Q4'Q3'Q2'Q1'Q0Op6 MFC	Q4Q3Q2'Q1'Q0	Q3Q2'Q1'Q0	Q2Q1Q0'	Q0'(Q2 + Q1'MFC)
Term 7	Q5Q4'Q3'Q2'Q1'Q0'Op14+15 P'	Q4Q3'Q2Q1Q0'	Q3'Q2Q1Q0'	Q2'Q1'Q0	
Term 8	Q5'Q4Q3'Q2Q1'Q0'	Q4Q3Q2'Q1Q0'	Q3Q2'Q1Q0'	Q2'Q1Q0'	
Term 9	Q5Q4'Q3'Q2Q1'Q0	Q4Q3Q2Q1'Q0'	Q3Q2Q1'Q0'	Q2Q1'Q0'	Q2'(Q1 XOR Q0) + Q2Q1'Q0'
Term 10	Q5'Q4Q3Q2'Q1'Q0	Q4'Q3'Q2'Q1'Q0'Op6-10	Q3'Q2'Q1'Q0'Op6-10	Q2'Q1'Q0'Op6-10	
Term 11	Q5Q4'Q3Q2'Q1'Q0	Q4'Q3'Q2'Q1Q0'Op10	Q3'Q2'Q1Q0'Op10	Q2'Q1Q0'Op10	
Term 12	Q5Q4Q3'Q2'Q1'Q0 MFC'	Q4'Q3'Q2'Q1'Q0'Op14+15 P'	Q3'Q2'Q1'Q0'Op14+15 P'	Q2'Q1'Q0'Op14+15 P'	
Term 13	Q5Q4'Q3'Q2Q1Q0' MFC'	Q4'Q3'Q2Q1'Q0	Q3'Q2Q1'Q0	Q2Q1'Q0	
Term 14	Q5'Q4Q3'Q2Q1Q0'	Q4'Q3Q2'Q1'Q0	Q3Q2'Q1'Q0	Q2Q1Q0' MFC'	Q2(Q1'Q0 + Q1Q0'MFC') + Q2'(Q1Q0'Op10 + Q1'Q0'(Op(6-10) + Op(14+15)P))
Term 15	Q5'Q4Q3Q2'Q1Q0'	Q4Q3'Q2'Q1'Q0 MFC'	Q3'Q2Q1Q0' MFC'	Q2'Q1'Q0	
Term 16	Q5Q4'Q3Q2'Q1Q0'	Q4'Q3'Q2Q1Q0' MFC'	Q3Q2'Q1Q0'	Q2'Q1Q0'	
Term 17	Q5'Q4Q3Q2Q1'Q0'	Q4'Q3Q2'Q1Q0'	Q3Q2Q1'Q0'	Q2Q1'Q0'	Q2'(Q1 XOR Q0) + Q2Q1'Q0'
Term 18	Q5Q4'Q3Q2Q1'Q0'	Q4'Q3Q2Q1'Q0'	Q3'Q2'Q1'Q0 MFC'	Q2'Q1'Q0 MFC'	Q2'Q1'Q0 MFC'
Final Equation:	D5 = Q5(Q4Q3'Q2'Q1'Q0MFC' + Q4'(Q3(Q2'(Q1 XOR Q0) + Q2Q1'Q0') + Q3'(Q2(Q1'Q0 + Q1Q0'MFC') + Q2'(Q1Q0'Op10 + Q1'Q0'(Op(6-10) + Op(14+15)P))))) + Q5'(Q4(Q3(Q2'(Q1 XOR Q0) + Q2Q1'Q0') + Q3'Q0'(Q2 + Q1'MFC)) + Q4'(Q3Q2Q1'Q0'Op8 + Q3'Q1'Q0(Q2Op2 + Q2'Op6MFC)))				

Next State + Output Table

Next State						Outputs																									
						PC		MAR	MDR		MM		ALU	IR	Shift	GPR[Rs1]	GPR[Rs2]	GPR[Rd]		short	long	Y	Z		PSW		[0]	[8]	WMFC	Timer	Set
Q5	Q4	Q3	Q2	Q1	Q0	in	out	in	in	out	R	W	op	in	out	out	out	in	out	out	out	in	in	out	in	out	out	out		in	CC
0	1	0	0	0	0	1																		1					1		
0	1	0	0	0	0	1																		1					1		
1	0	0	0	0	0					1				1																	
0	0	0	0	1	1								7		1		1						1								
0	0	0	1	0	1																	1		1							
0	0	1	0	0	1								2			1							1								
0	1	0	0	0	1								3			1							1								
1	0	0	0	0	1								4			1							1								
0	0	0	1	1	0								5			1							1								
0	0	1	0	1	0								7			1							1								
0	1	0	0	1	0								8			1							1								
0	0	0	0	1	0													1						1							1
0	0	0	0	1	0													1						1							1
0	0	0	0	1	0													1						1							1
0	0	0	0	1	0													1						1							1
0	0	0	0	1	0													1						1							1
0	0	0	0	1	0													1						1							1
0	0	0	0	0	0		1	1			1		0										1								
1	0	0	0	1	0															1		1									
0	0	1	1	0	0		1						2										1								
0	1	0	0	1	1		1						2					1					1								
1	0	0	0	1	1								2						1				1								
0	1	1	0	0	0			1			1													1							
1	0	1	0	0	0			1																1							
0	0	0	1	0	0	1																		1							1
0	0	0	1	0	0	1																		1							1
0	0	0	0	0	1																								1		
0	0	1	0	1	1				1			1							1												
0	0	0	0	0	0		1	1			1		0										1								
0	0	0	0	0	1																								1		
0	0	0	0	0	0		1	1			1		0										1								
1	1	0	0	0	0					1			6										1								
0	0	0	1	1	1					1								1													1

0	0	0	0	0	1																							1		
0	0	0	0	1	0													1						1							1
0	0	0	0	0	0		1	1			1		0										1								
0	0	0	0	0	0		1	1			1		0										1								
0	1	0	1	0	0																1	1									
0	1	0	1	0	0																1	1									
0	1	0	1	0	0																1	1									
0	1	0	1	0	0																1	1									
1	0	0	1	0	1			1					1										1				1				
0	0	0	0	0	0		1	1			1		0										1								
0	0	0	0	0	0		1	1			1		0										1								
1	0	0	1	0	0		1						2										1								
0	0	0	1	0	0	1																		1							
0	1	1	0	0	0			1			1													1							
0	0	0	0	0	0		1	1			1		0										1								
0	0	0	0	0	1																								1		
0	0	1	1	0	1					1																				1	
0	1	0	1	0	1					1															1						
0	0	0	0	0	0		1	1			1		0										1								
0	0	0	0	0	0		1	1			1		0										1								
1	0	1	0	0	1				1			1														1					
1	0	1	0	0	1				1			1														1					
1	1	0	0	0	1																			1	1				1		
1	1	0	0	0	1																			1	1				1		
0	0	1	1	1	0			1					1										1			1					
0	1	0	1	1	0		1		1			1																			
1	0	0	1	1	0																			1	1				1		
1	0	0	1	1	0																			1	1				1		
0	1	1	0	1	0			1			1		1										1			1					
1	0	1	0	1	0	1																		1					1		
1	0	1	0	1	0	1																		1					1		
1	1	0	0	1	0					1															1						
0	1	1	1	0	0		1	1			1																				
1	0	1	1	0	0																								1		
1	0	1	1	0	0																								1		
1	1	0	1	0	0	1				1																					
0	0	0	0	0	0		1	1			1		0										1								
0	1	1	0	0	1			1					1										1					1			

Output Simplification Table

Outputs:			
PC in	Original Terms	Decimal Representation of Terms	Final Equation
Term 1	010000	16	Q0'(Q5(Q4'Q3Q2'Q1 + Q4Q3'Q2Q1') + Q5'Q3'Q1'(Q4 XOR Q2))
Term 2	000100	4	
Term 3	101010	42	
Term 4	110100	52	
PC out	Original Terms		Final Equation
Term 1	000000	0	Q5Q4'Q3'Q2Q1'Q0' + Q5'(Q4(Q3Q2Q1'Q0' + Q3'Q1(Q2 XOR Q0)) + Q4'Q1'Q0'(Q3 XNOR Q2))
Term 2	001100	12	
Term 3	010011	19	
Term 4	100100	36	
Term 5	010110	22	
Term 6	011100	28	
MAR in	Original Terms		Final Equation
Term 1	101000	40	Q5Q4'Q1'(Q3Q2'Q0' + Q3'Q2Q0) + Q5'(Q4'Q0'(Q3'Q2'Q1' + Q3Q2Q1) + Q4Q3(Q2'Q1' + Q0'(Q2 XOR Q1))))
Term 2	100101	37	
Term 3	000000	0	
Term 4	011000	24	
Term 5	001110	14	
Term 6	011010	26	
Term 7	011100	28	
Term 8	011001	25	
MDR in	Original Terms		Final Equation

Term 1	001011	11	Q5'Q1(Q4'Q3Q2'Q0 + Q4Q3'Q2Q0') + Q5Q4'Q3Q2'Q1'Q0
Term 2	101001	41	
Term 3	010110	22	
MDR out	Original Terms		Final Equation
Term 1	100000	32	Q5Q3'Q0'(Q4(Q2'+Q1') + Q4'Q2'Q1') + Q5'Q0Q2(Q4'(Q3 XOR Q1) + Q4Q3'Q1')
Term 2	110000	48	
Term 3	110010	50	
Term 4	110100	52	
Term 5	000111	7	
Term 6	001101	13	
Term 7	010101	21	
Read_MM	Original Terms		Final Equation
Term 1	000000	0	Q5'Q0'(Q4'Q3'Q2'Q1' + Q4Q3(Q2'+Q1'))
Term 2	011000	24	
Term 3	011010	26	
Term 4	011100	28	
Write_MM	Original Terms		Final Equation
Term 1	001011	11	Q4'Q3Q2'Q0(Q5 XOR Q1) + Q5'Q4Q3'Q2Q1Q0'
Term 2	101001	41	
Term 3	010110	22	
ALU 0	Original Terms		Final Equation
Term 1	000000	0	Q5'Q4'Q3'Q2'Q1'Q0'

ALU 1	Original Terms		Final Equation
Term 1	100101	37	Q5'Q4Q3Q2'(Q1 XOR Q0) + Q4'Q2(Q5Q3'Q1'Q0 + Q5'Q3Q1Q0')
Term 2	011010	26	
Term 3	011001	25	
Term 4	001110	14	
ALU 2	Original Terms		Final Equation
Term 1	001001	9	Q5'(Q4'Q3Q1'(Q2 XOR Q0) + Q4Q3'Q2'Q1Q0) + Q5Q4'Q3'(Q2'Q1Q0 + Q2Q1'Q0')
Term 2	001100	12	
Term 3	010011	19	
Term 4	100011	35	
Term 5	100100	36	
ALU 3	Original Terms		Final Equation
Term 1	010001	17	Q5'Q4Q3'Q2'Q1'Q0
ALU 4	Original Terms		Final Equation
Term 1	100001	33	Q5Q4'Q3'Q2'Q1'Q0
ALU 5	Original Terms		Final Equation
Term 1	000110	6	Q5'Q4'Q3'Q2Q1Q0'
ALU 6	Original Terms		Final Equation
Term 1	110000	48	Q5Q4Q3'Q2'Q1'Q0'
ALU 7	Original Terms		Final Equation

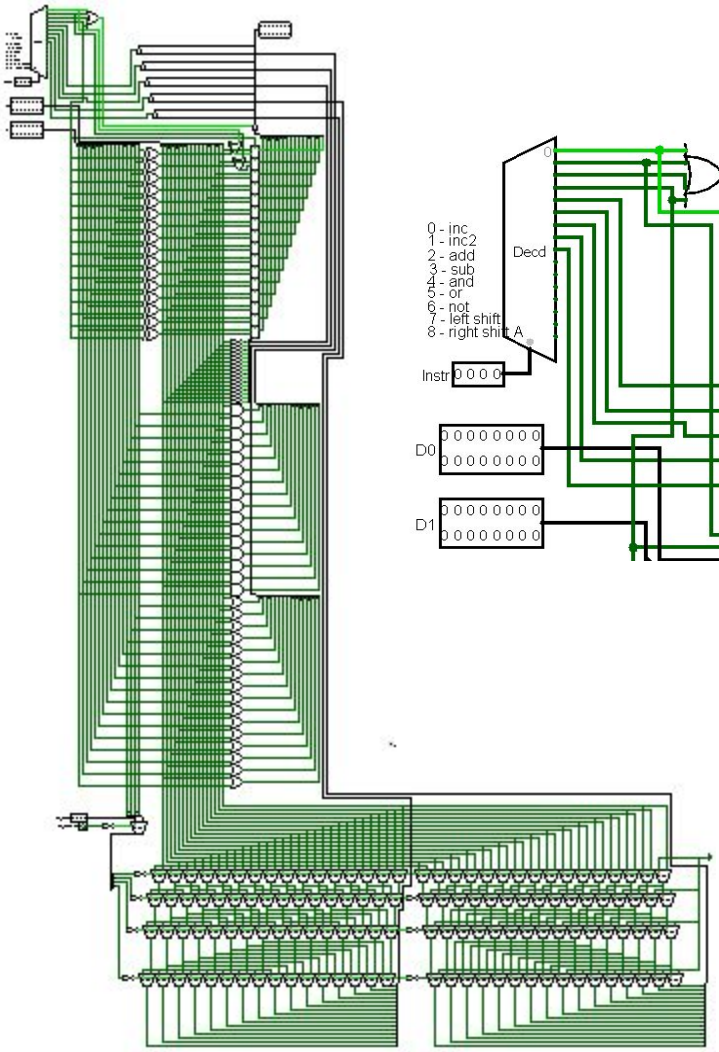
Term 1	000011	3	Q5'Q4'Q2'Q1(Q3 XOR Q0)
Term 2	001010	10	
ALU 8	Original Terms		Final Equation
Term 1	010010	18	Q5'Q4Q3'Q2'Q1Q0'
IR in	Original Terms		Final Equation
Term 1	100000	32	Q5Q4'Q3'Q2'Q1'Q0'
IR.Shift/out	Original Terms		Final Equation
Term 1	000011	3	Q5'Q4'Q3'Q2'Q1Q0
GPR[IR.Rs1] out	Original Terms		Final Equation
Term 1	001001	9	Q2'Q1'Q0(Q5'Q4'Q3 + Q5Q4'Q3' + Q5'Q4Q3') + Q5'Q1Q0'(Q4'Q3'Q2 + Q4'Q3Q2' + Q4Q3'Q2')
Term 2	010001	17	
Term 3	100001	33	
Term 4	000110	6	
Term 5	001010	10	
Term 6	010010	18	
GPR[IR.Rs2] out	Original Terms		Final Equation
Term 1	000011	3	Q5'Q4'Q3'Q2'Q1Q0
GPR[IR.Rd] in	Original Terms		Final Equation
Term 1	000010	2	Q5'Q3'(Q4'Q2'Q1Q0' + Q4Q2'Q1Q0 + Q4'Q2Q1Q0)
Term 2	010011	19	

Term 3	000111	7	
GPR[IR.Rd] out	Original Terms		Final Equation
Term 1	100011	35	Q4'Q2'Q1Q0(Q5 XOR Q3)
Term 2	001011	11	
IR.Short_Offset/out	Original Terms		Final Equation
Term 1	100010	34	Q5Q4'Q3'Q2'Q1Q0'
IR.Long_Offset/out	Original Terms		Final Equation
Term 1	010100	20	Q5'Q4Q3'Q2Q1'Q0'
Y in	Original Terms		Final Equation
Term 1	000101	5	Q3'(Q5'Q4'Q2Q1'Q0 + Q5Q4'Q2'Q1Q0' + Q5'Q4Q2Q1'Q0')
Term 2	100010	34	
Term 3	010100	20	
Z in	Original Terms		Final Equation
Term 1	000011	3	Q5'(Q4'(Q3'(Q2'Q1'Q0' + Q1(Q2 XOR Q0)) + Q3(Q0'(Q2 + Q1) + Q2'Q1'Q0)) + Q4(Q3'Q2'(Q1 + Q0) + Q3Q2'(Q1 XOR Q0))) + Q5Q3'(Q4'(Q2'Q0 + Q2Q1') + Q4Q2'Q1'Q0')
Term 2	001001	9	
Term 3	010001	17	
Term 4	100001	33	
Term 5	000110	6	
Term 6	001010	10	
Term 7	010010	18	
Term 8	000000	0	
Term 9	001100	12	

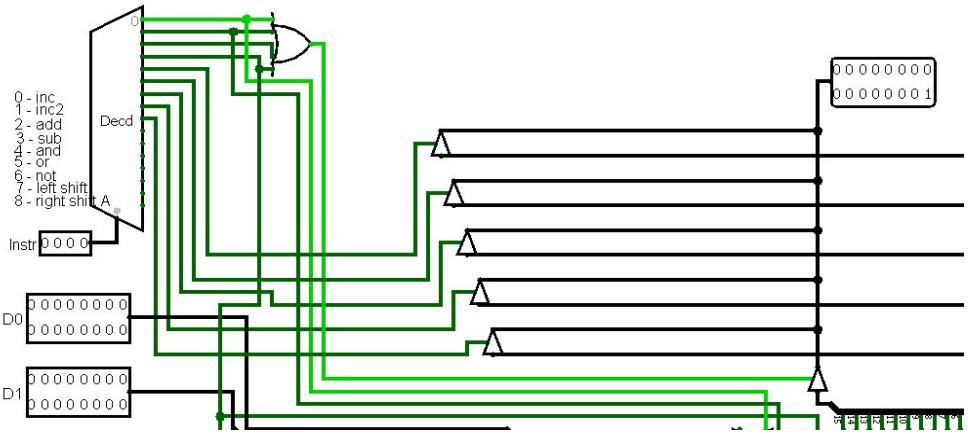
Term 10	010011	19	
Term 11	100011	35	
Term 12	110000	48	
Term 13	100101	37	
Term 14	100100	36	
Term 15	001110	14	
Term 16	011010	26	
Term 17	011001	25	
Z out	Original Terms		Final Equation
Term 1	010000	16	Q5'(Q4'Q3'(Q2Q1' + Q2'Q1Q0') + Q4Q2'Q1'Q0') + Q5(Q4'Q0'(Q3Q2'Q1' + Q1(Q3 XOR Q2)) + Q4Q3'Q2'Q1'Q0)
Term 2	000101	5	
Term 3	000010	2	
Term 4	011000	24	
Term 5	101000	40	
Term 6	000100	4	
Term 7	110001	49	
Term 8	100110	38	
Term 9	101010	42	
PSW in	Original Terms		Final Equation
Term 1	010101	21	Q4Q3'Q1'Q0(Q5 XOR Q2) + Q5Q3'Q1Q0'(Q4 XOR Q2)
Term 2	110001	49	
Term 3	100110	38	
Term 4	110010	50	
PSW out	Original Terms		Final Equation
Term 1	101001	41	Q3(Q5Q4'Q2'Q1'Q0 + Q5'Q1Q0'(Q4 XOR Q2))
Term 2	001110	14	

Term 3	011010	26	
GPR[0] out	Original Terms		Final Equation
Term 1	100101	37	Q5Q4'Q3'Q2Q1'Q0
ROM[8] out	Original Terms		Final Equation
Term 1	011001	25	Q5'Q4Q3Q2'Q1'Q0
WMFC	Original Terms		Final Equation
Term 1	010000	16	Q5'Q3'Q2'Q1'(Q4 XOR Q0) + Q5(Q4Q3'Q2'Q1'Q0 + Q4'Q0'(Q3'Q2Q1 + Q3Q2'Q1 + Q3Q2Q1'))
Term 2	000001	1	
Term 3	110001	49	
Term 4	100110	38	
Term 5	101010	42	
Term 6	101100	44	
Timer in	Original Terms		Final Equation
Term 1	001101	13	Q5'Q4'Q3Q2Q1'Q0
Set_CC	Original Terms		Final Equation
Term 1	000010	2	Q5'Q4'Q3'(Q2Q1Q0 + Q0'(Q2 XOR Q1))
Term 2	000100	4	
Term 3	000111	7	

ALU

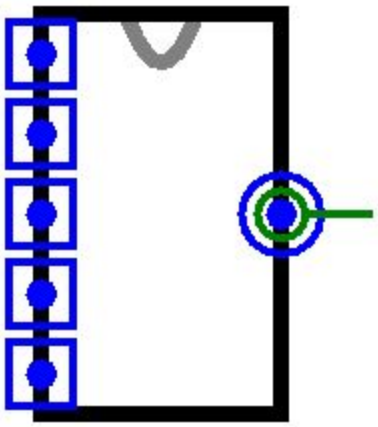


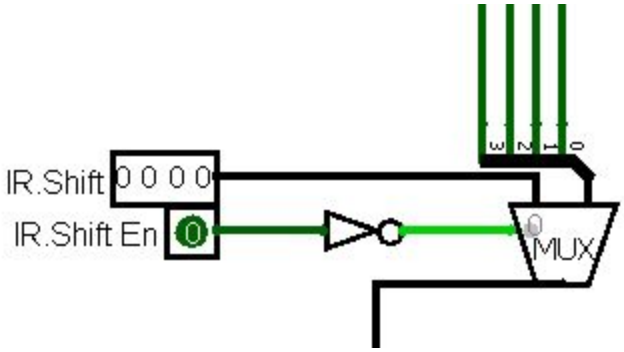
The ALU for this project contains 9 operations which are decoded from 4 bit instructions here:



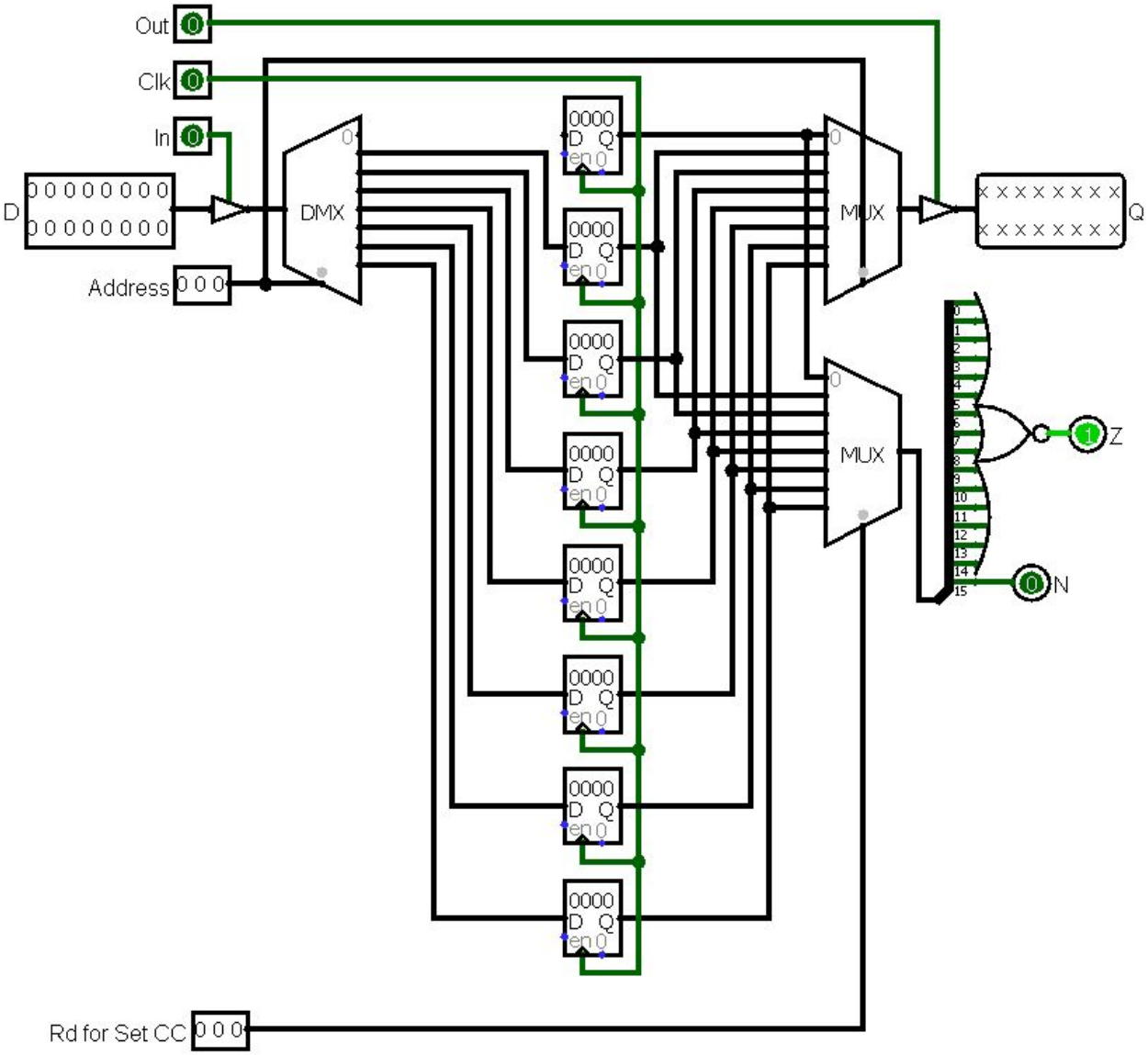
The increment, increment by 2, add, and subtract operations all utilize an array of 16 full adders. NOT, AND, and OR operations are executed with their respective logic gate. Left and Right Arithmetic Shift operations utilize Multiplexer-based barrel shifters.

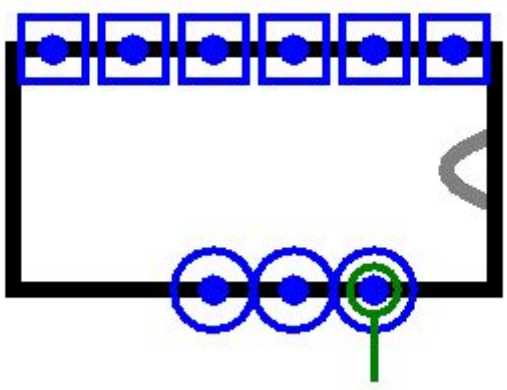
The shift bits to the shifters can come from the first four bits of the Y register, or the two (extended to four) bits from the IR, seen here:





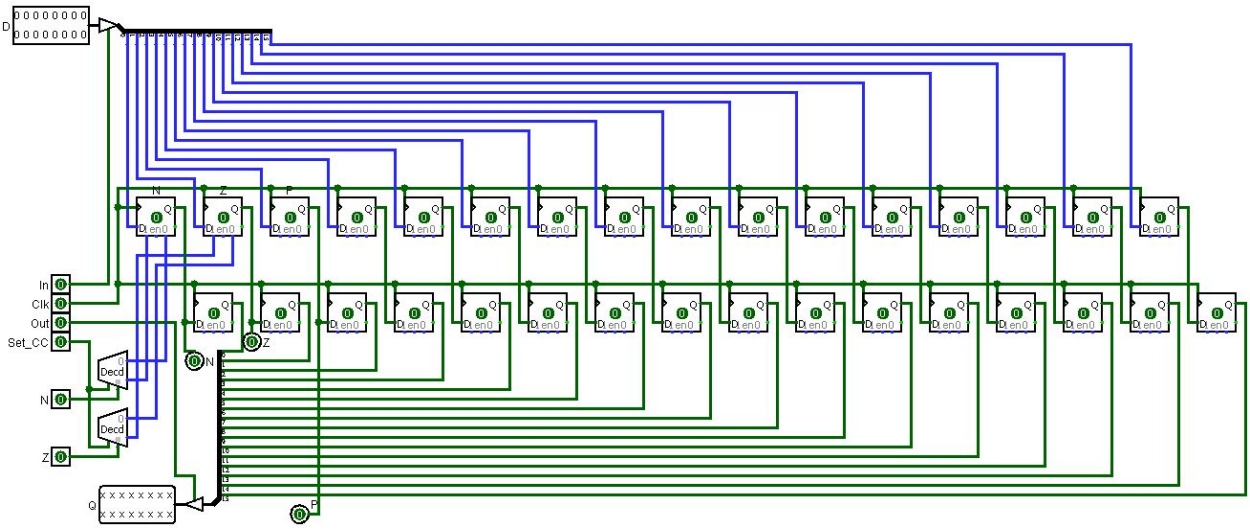
GPR



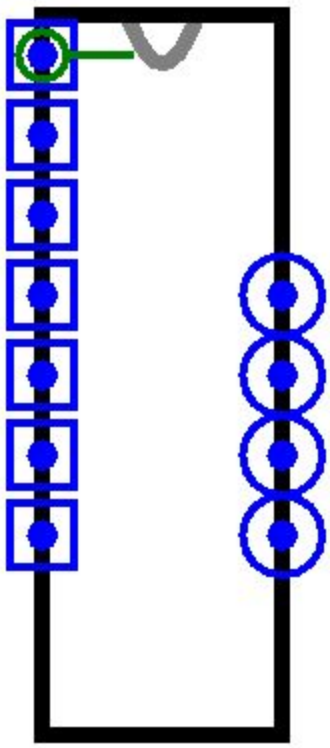


The GPR contains 8 registers, where the 0th register is not able to have its default value of zero altered. Outside of the GPR is a multiplexer for the address signals from the IR, and the control signals from the control unit are encoded and used to select from the aforementioned multiplexer.

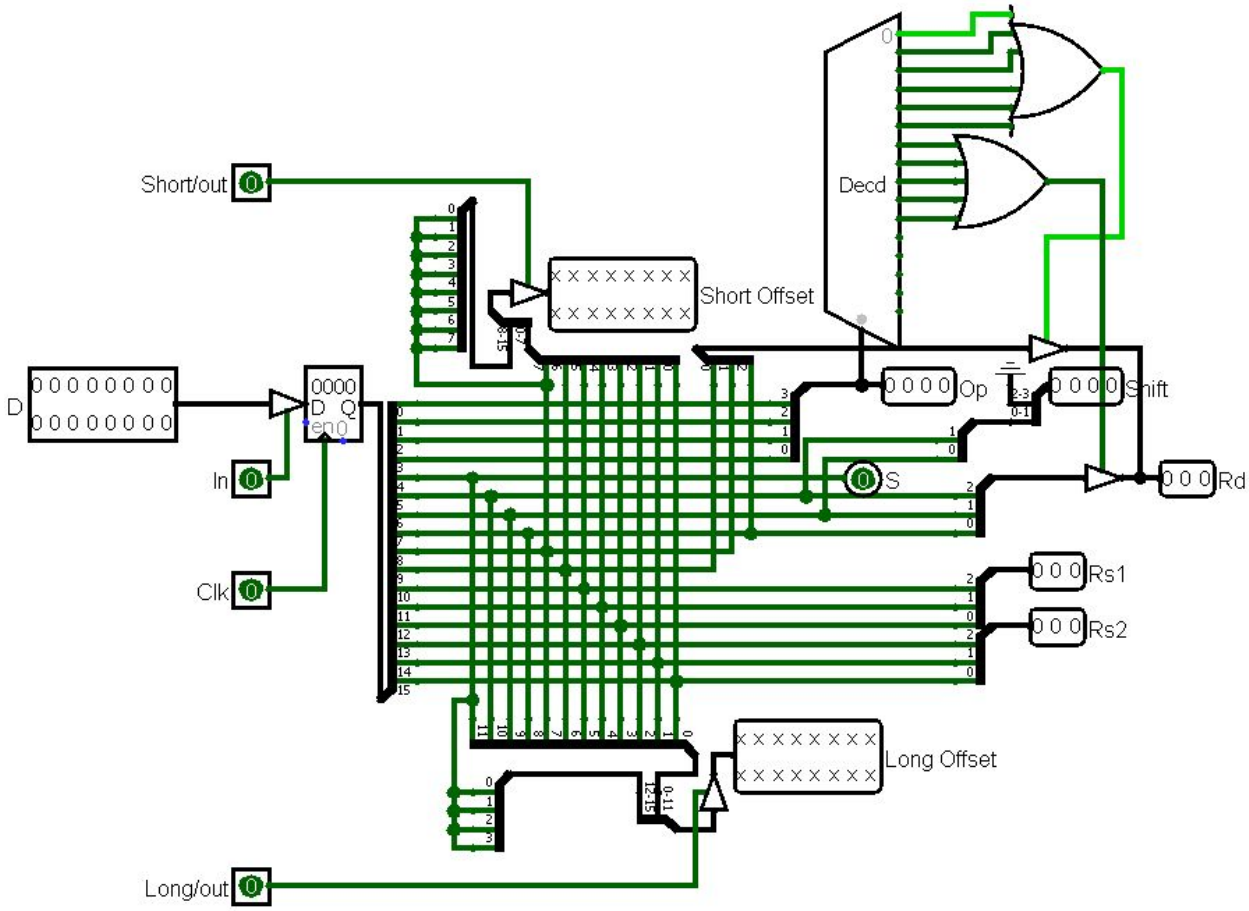
PSW



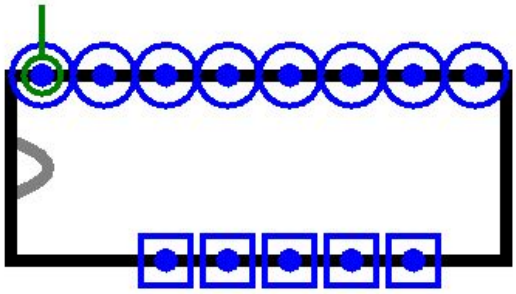
The Program Status Word has a special control input for when the condition codes are to be set, and when they are set N and Z are decoded to either the asynchronous set 1 or set 0 for their respective locations in the register. The bit that stores privileged mode is the third bit of the register, which is output and sent straight to the control unit.



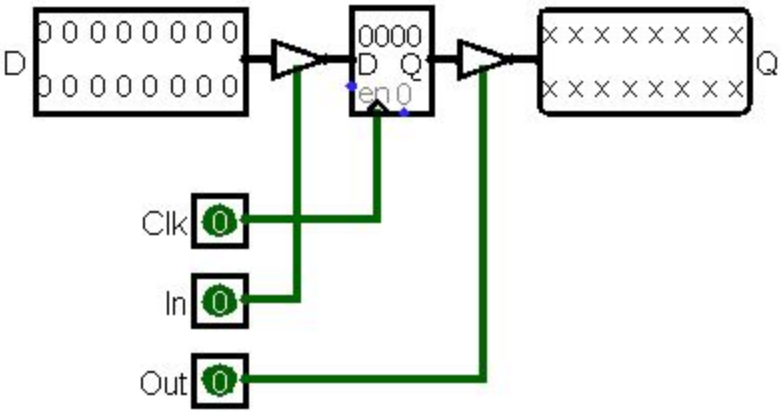
IR



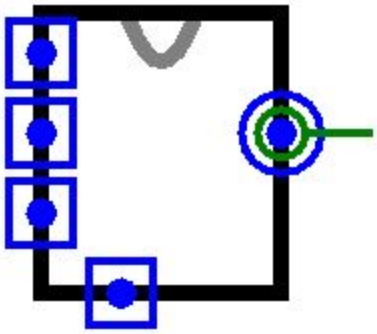
The Instruction Register has no output for all 16 bits to the bus. Short and Long Offsets are sign-extended and put out to the bus. Rd, Rs1, and Rs2 are all sent to a multiplexer to the GPR, and the mux is selected by the control unit. The Shift bits are extended to a width of 4 and sent to the ALU. The opcode goes straight to the control unit. The S bit goes to a tri-state buffer controlling the Set_CC signal that goes from the control unit to the PSW.



Generic Register

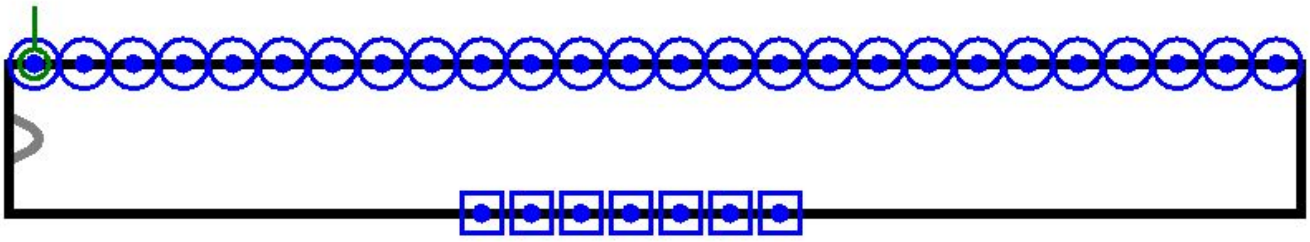


The Z, Y, Memory Data, Memory Address and ROM registers are all a generic form used to store a 16-bit word. The ROM register's input signal is always powered, and the Y register's output signal is always powered as it attaches to the ALU.

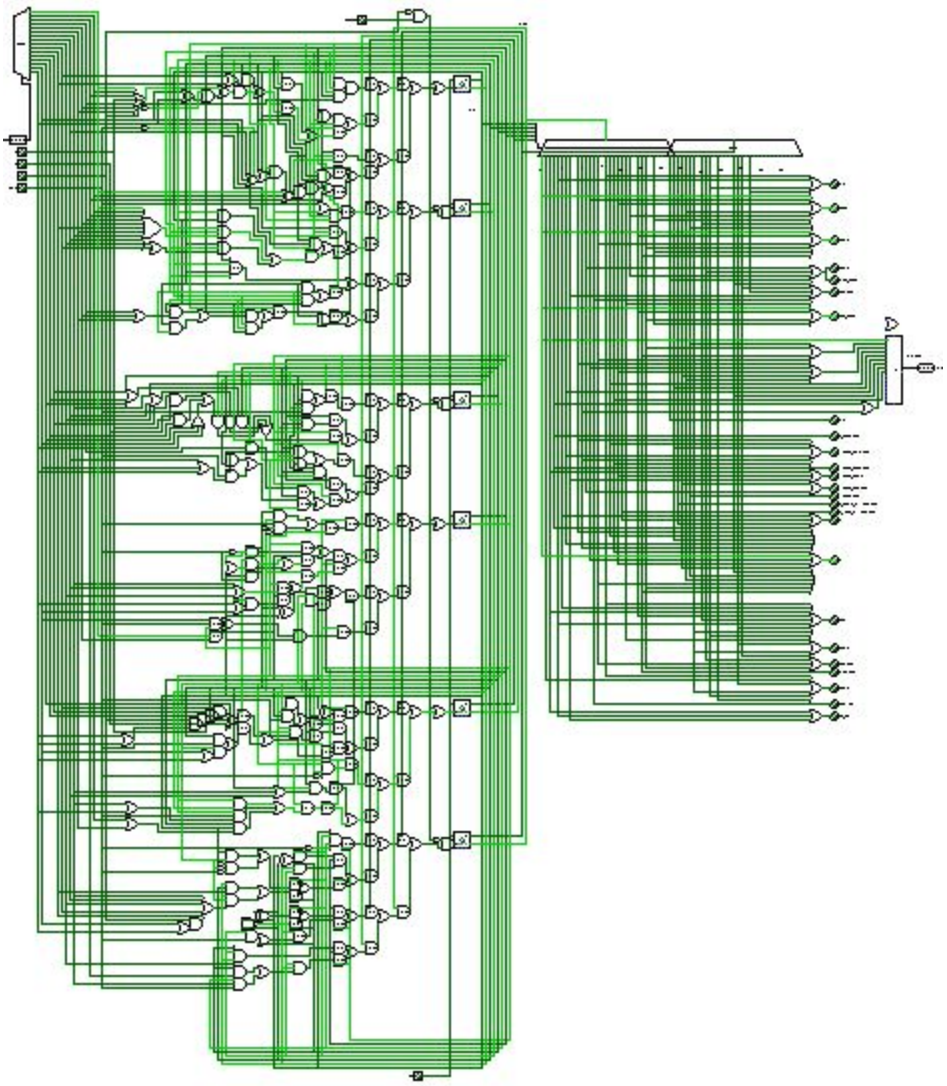


Control Unit

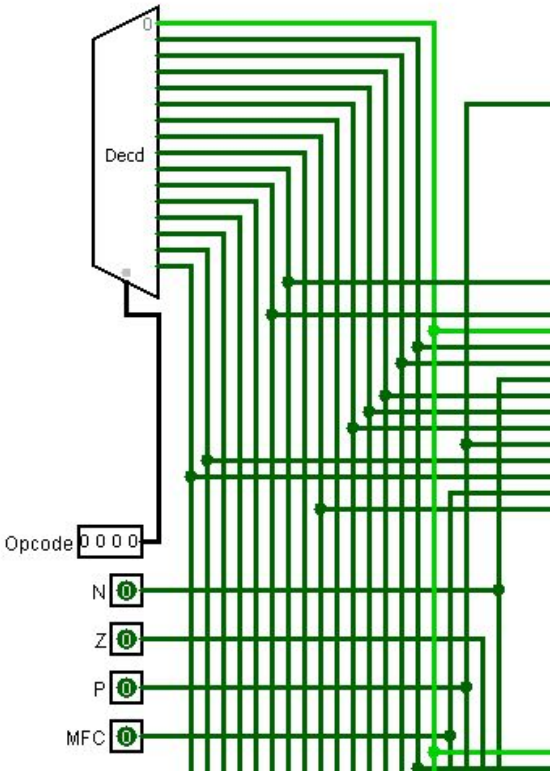
The pin description of the Control Unit is below due to space concerns with the size of the control unit wiring.



Control Unit Design

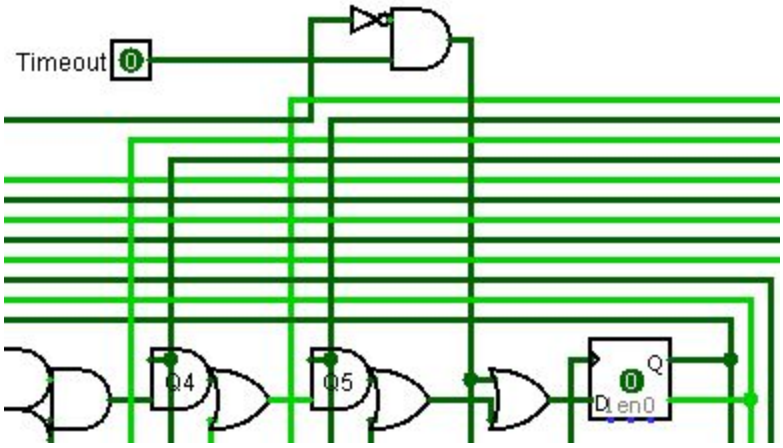


The inputs to the control unit are decoded and strewn along the left of the circuit, and shown below:



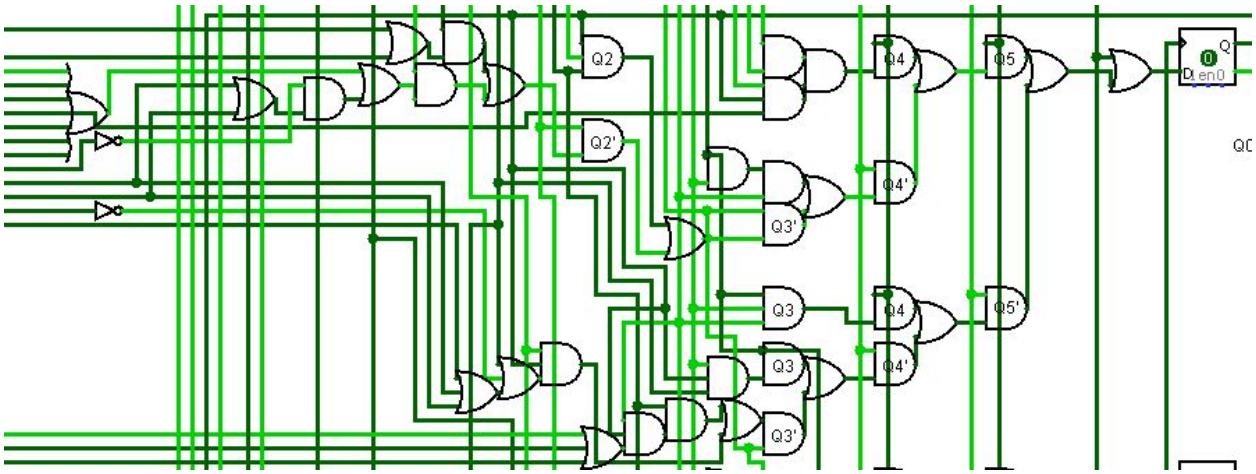
The Timeout override was included at the end of design:

Timeout (right) is designed to force each flip flop to be the proper state for the TO1 trap state. It is AND'ed with the Privileged state bit that is inverted so that timeout cannot trigger if the user is in privileged mode.

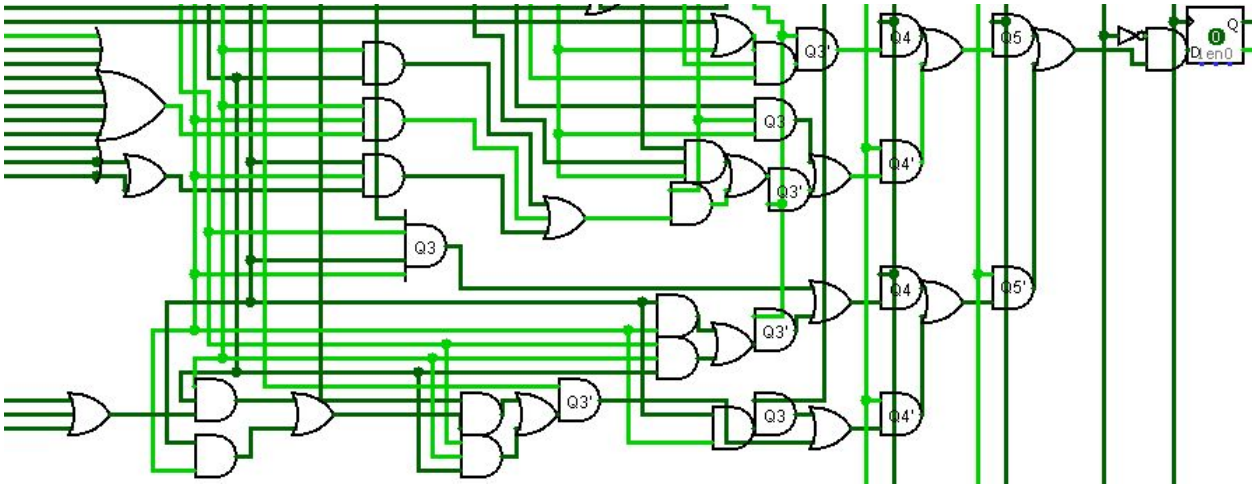


Flip Flop Implementations:

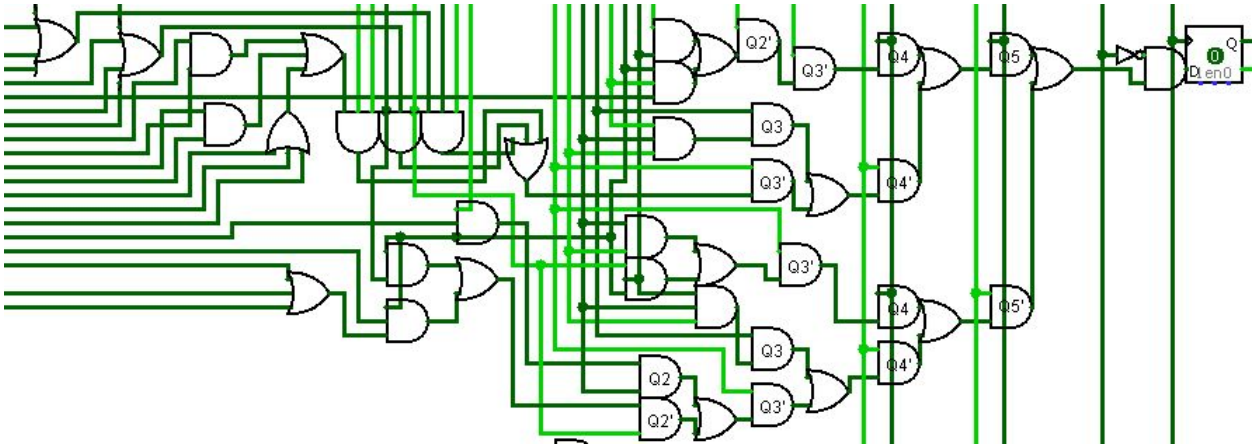
Q0:



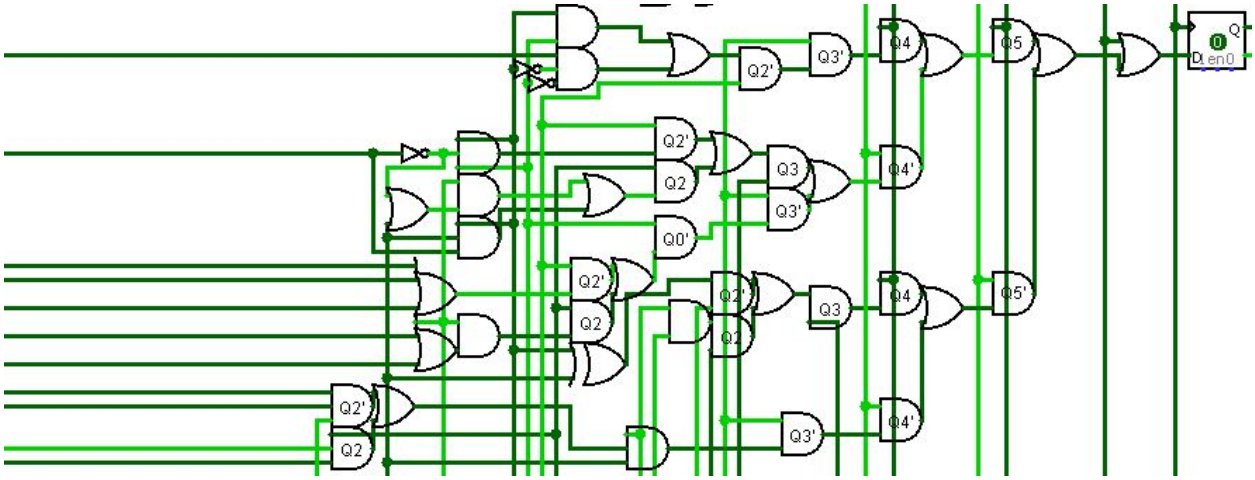
Q1:



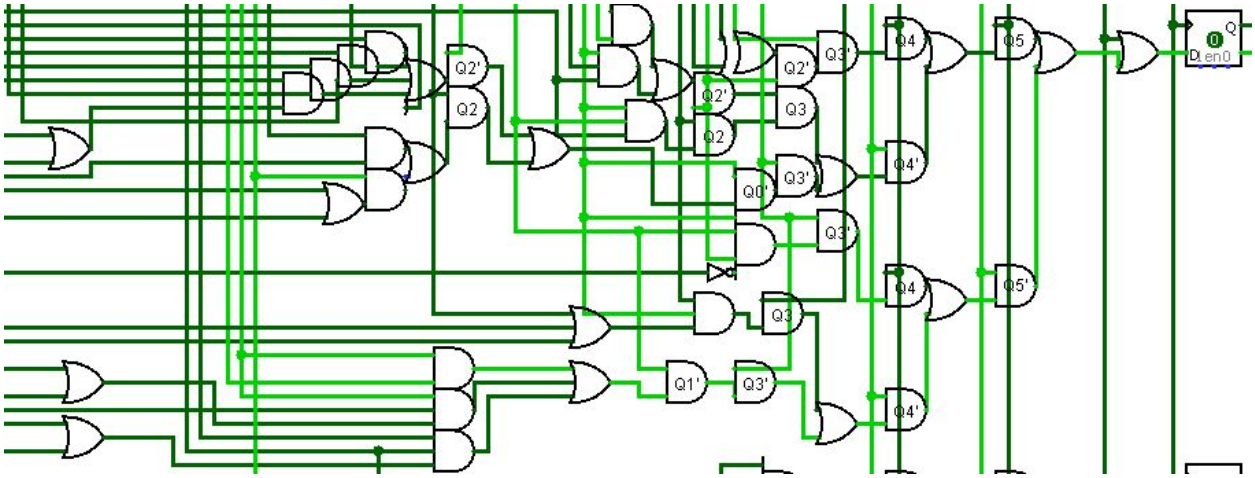
Q2:



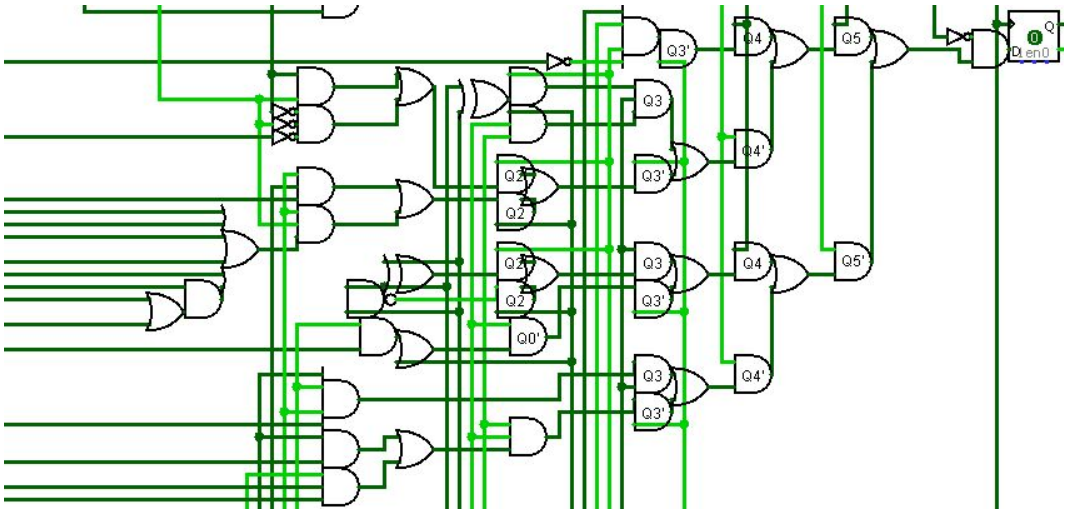
Q3:


Q2'
Q2
Q0'
Q3'
Q4'
Q5'
Q3
Q4
Q5
Q
D
en
0

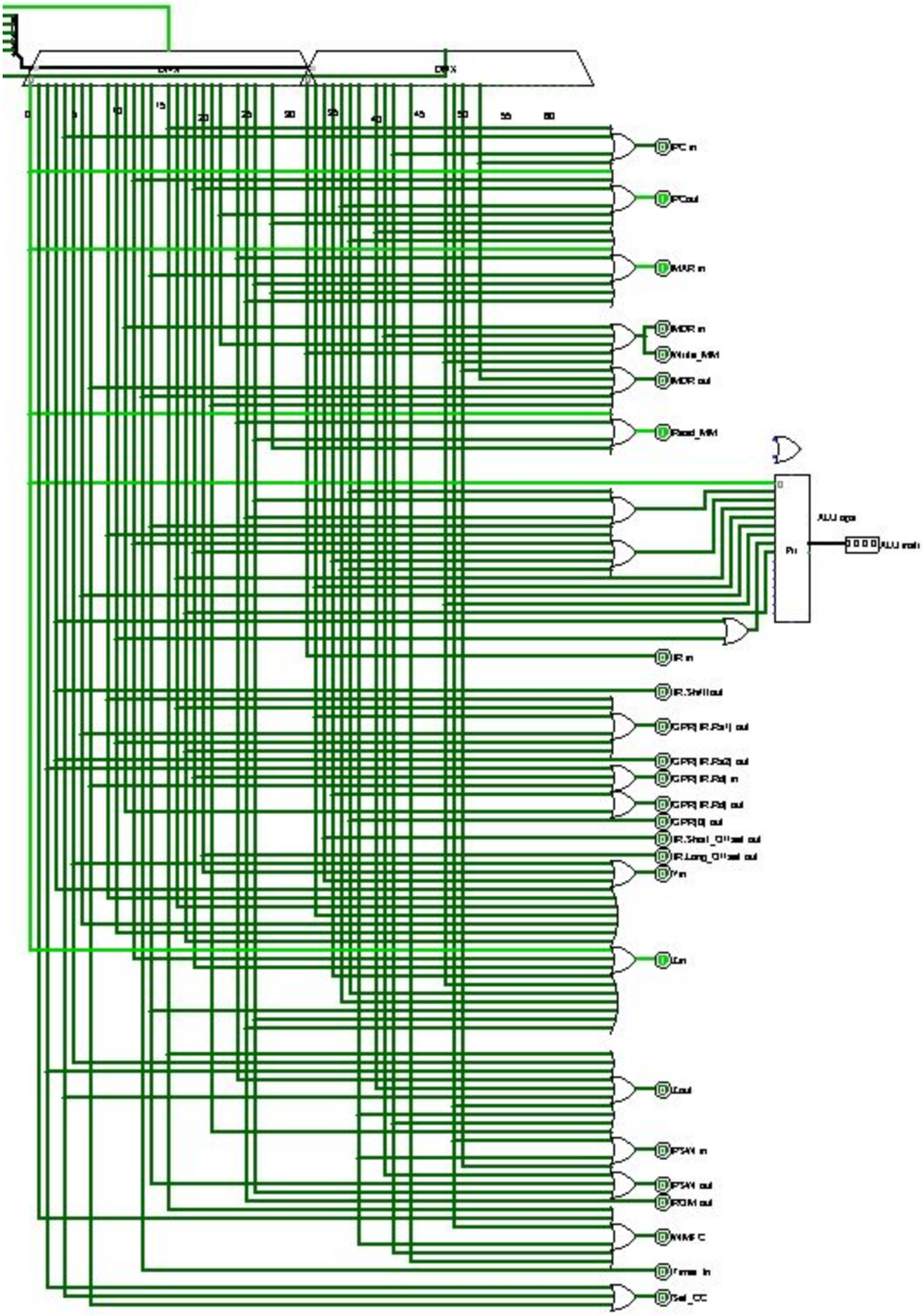
Q4:


Q2'
Q2
Q0'
Q1'
Q3'
Q4'
Q5'
Q3
Q4
Q5
Q
D
en
0

Q5:

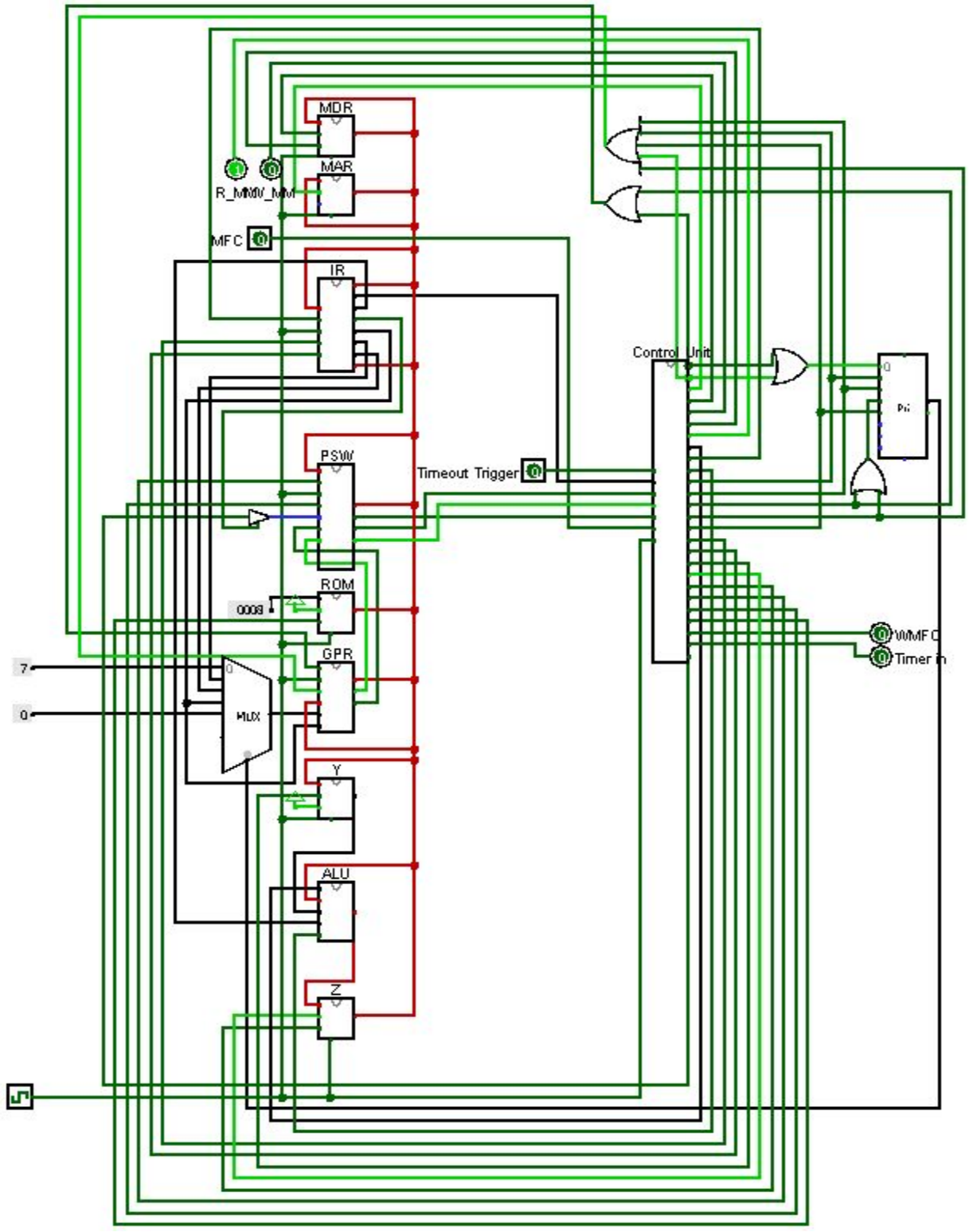

Q2'
Q2
Q0'
Q3'
Q4'
Q5'
Q3
Q4
Q5
Q
D
en
0

Control Unit Outputs



The outputs of the control unit were found by decoding the 6 flip flops into 64 possible states, and wiring each output to the states that it should be 1. The simplified boolean equations for each output signal were available, but this design was opted for due to severe time constraints, as the design process with this method is much faster to implement.

Main Circuit



The Data Bus exhibits a red wire with an “error” value because the tri-states to control register in/out are on the inside of the subcircuits. Due to time constraints, this was not a high priority fix.