

[Year]

SRAM 256x4b BIST Engine

FINAL PROJECT REPORT

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*File/Report included in zip.

Introduction

The aim of the project is to design a Built-In Self-Test for a SRAM array of size 256x4b. The BIST is an essential tool in testing memory devices. It can be used to trace faults along lines, columns or even single bits with more complex patterns (eg. MARCH-LR).

This project is divided into 2 components,

1. BIST Engine: Used to generate and feed address and data signals for test patterns.
2. SRAM Array 256x4b: The SRAM array has a word size of 4b , the memory is word addressable. There are 256 words capacity.

The BIST Engine is further divided into the following modules:

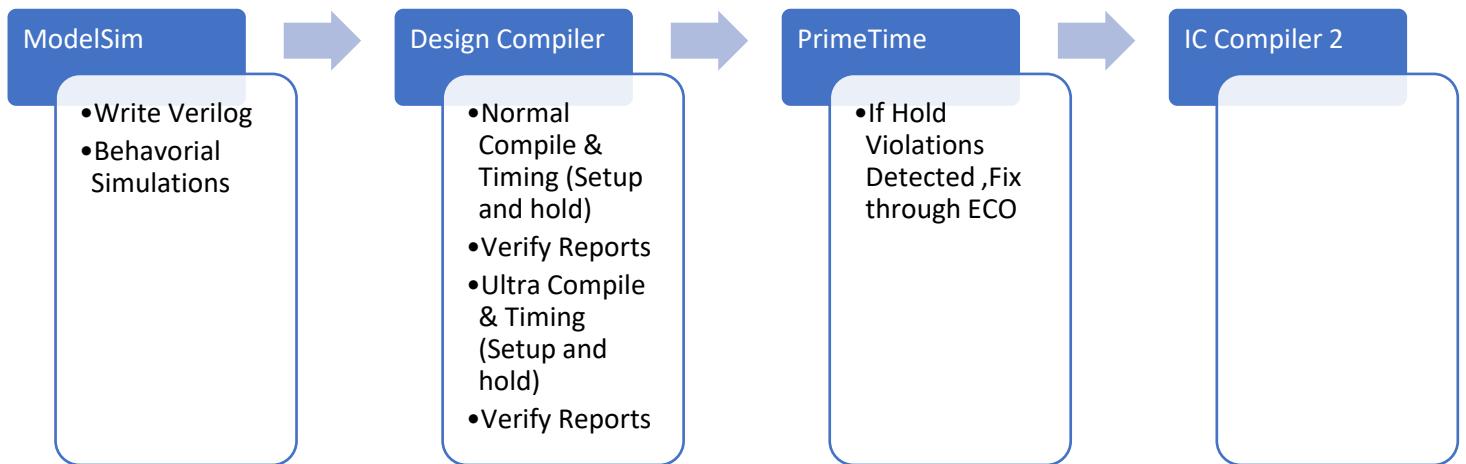
1. Control Unit
2. Blanket Generator
3. Checkerboard Generator
4. March_C Generator
5. March_LR Generator

The components are explained in detail in the report. The design flow followed is also presented in the report. This holds true for most components in the design. Testbenches for each individual component are also included.

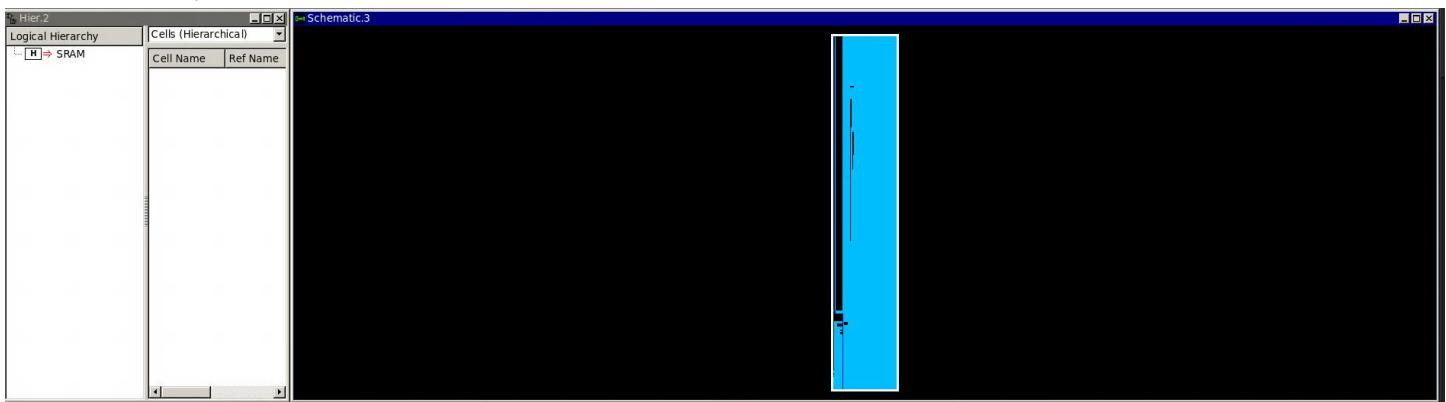
The library used is SAED32_EDK.

*File/Report included in zip.

Design Flow



SRAM Array 256x4b

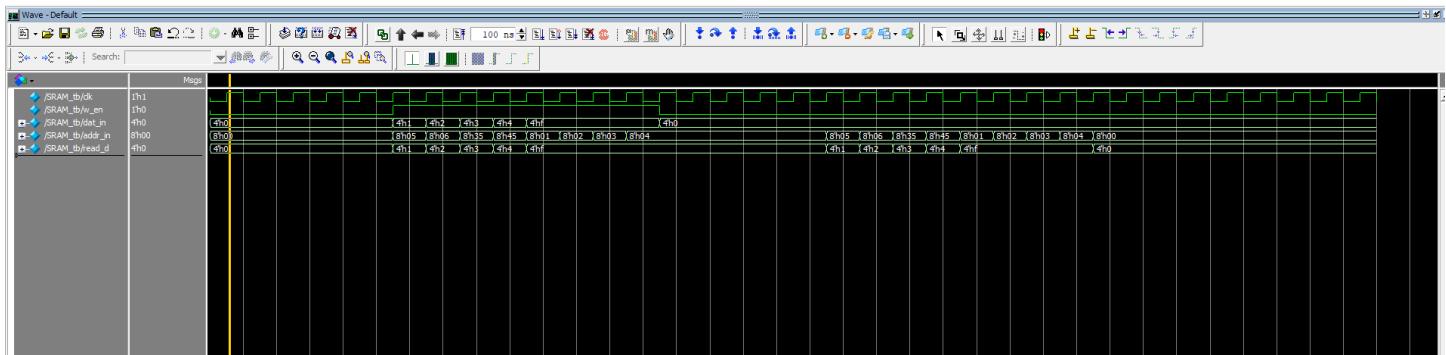


Schematic 1 SRAM Uncompiled

Technical Specifications:

- Word Size = 4 bits
- Total capacity = 256 x4b = 128 bytes
- Target Clock Period = 3 ns
- Achieved Clock Period = 1.1 ns

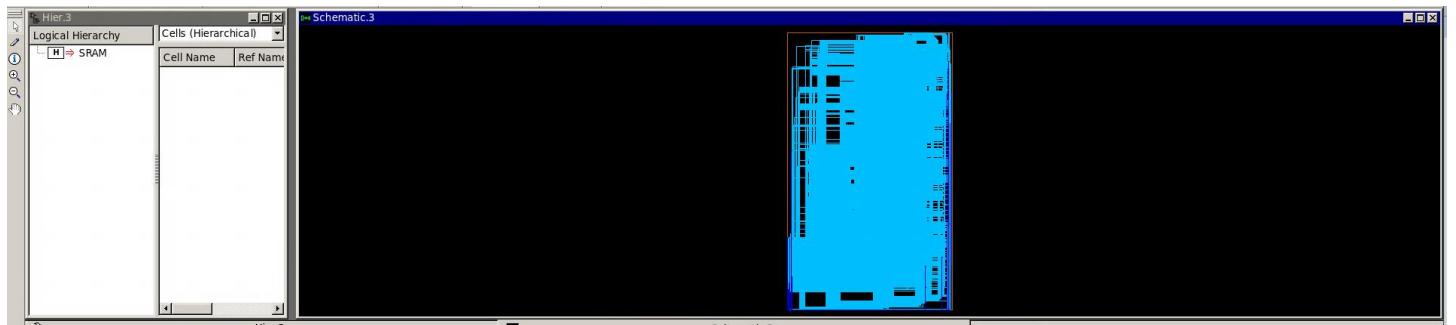
ModelSim (SRAM_tb)



Waveform 1 SRAM Write and then Read testbench

*File/Report included in zip.

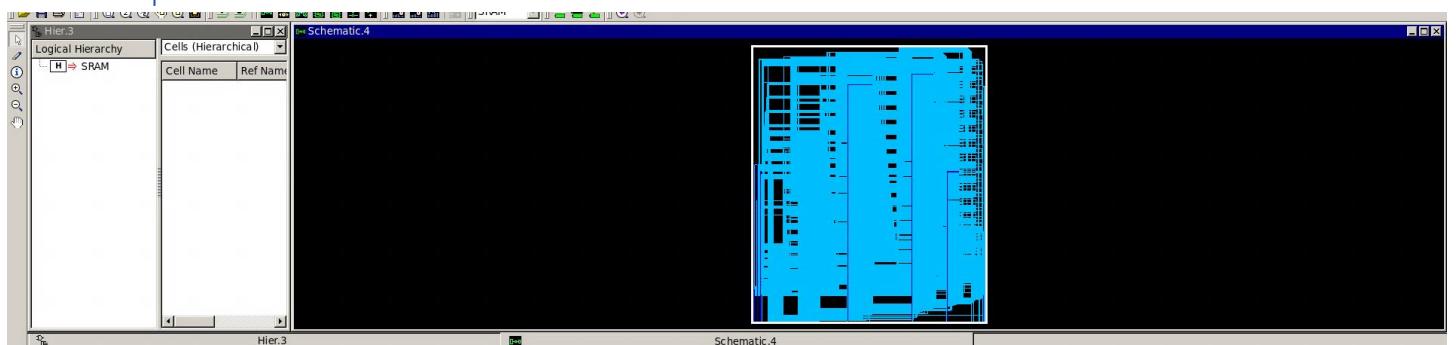
Normal Compile



Schematic 2 Normal Compile SRAM 256x4b

- Min Clock Period Achieved = 1.1 ns
- Reports Included

Ultra-Compile

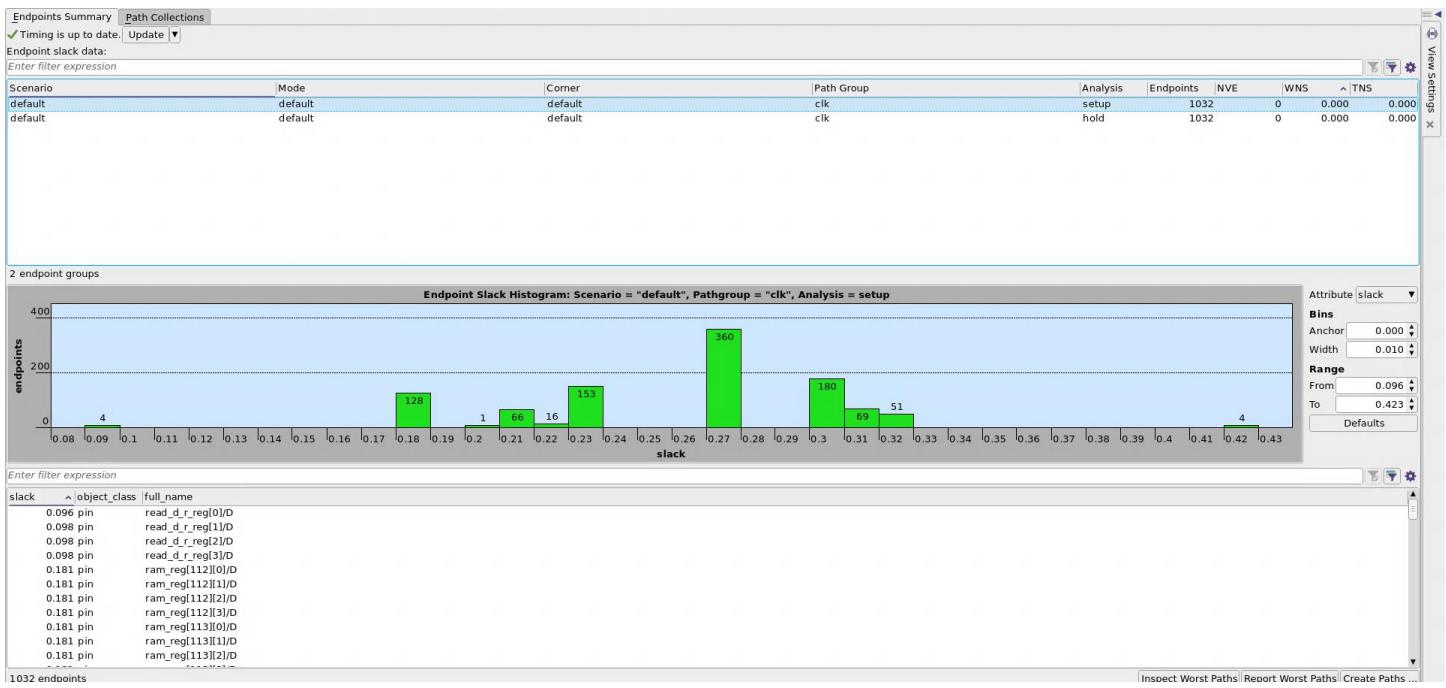


Schematic 3 Ultra Compile SRAM 256x4b

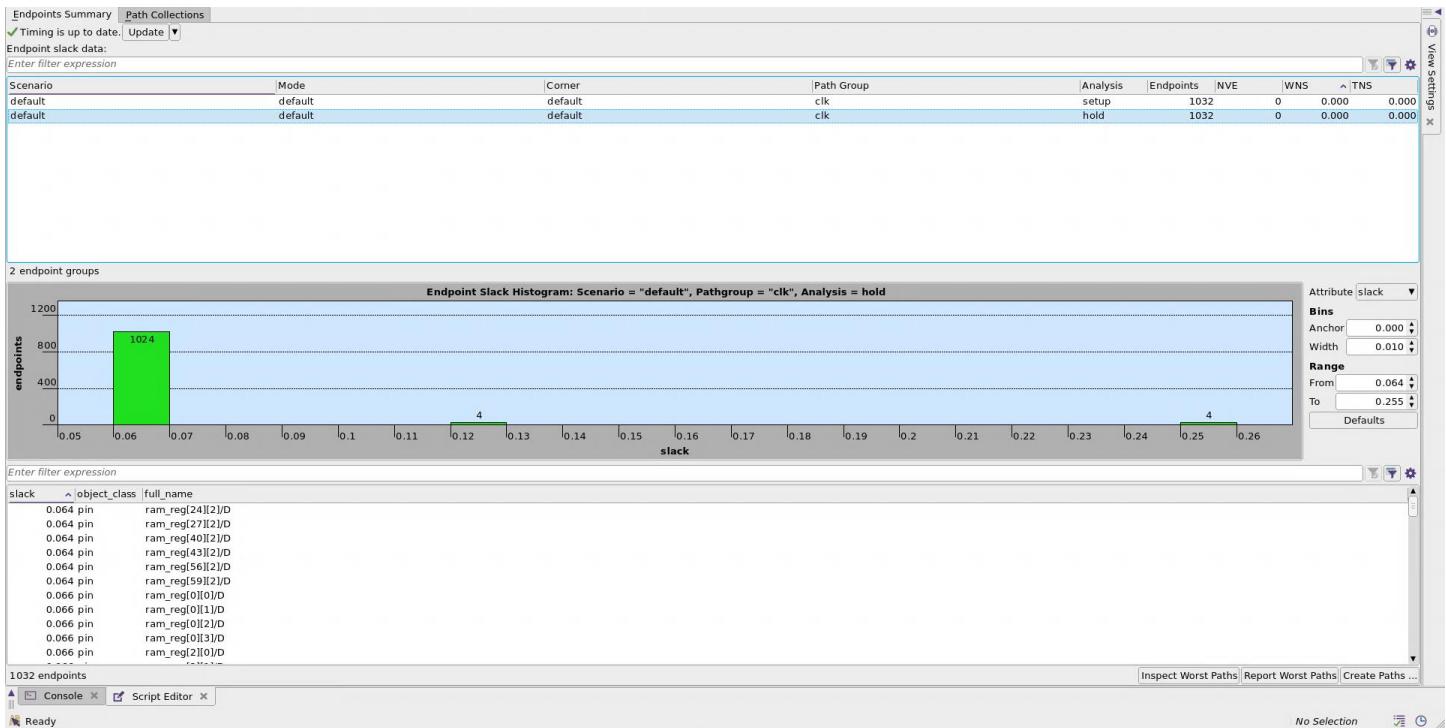
- Min Clock Period Achieved = 1.1.ns
- Reports Included.

*File/Report included in zip.

PrimeTime



Report 1 PrimeTime Setup Violations 1.1ns clk

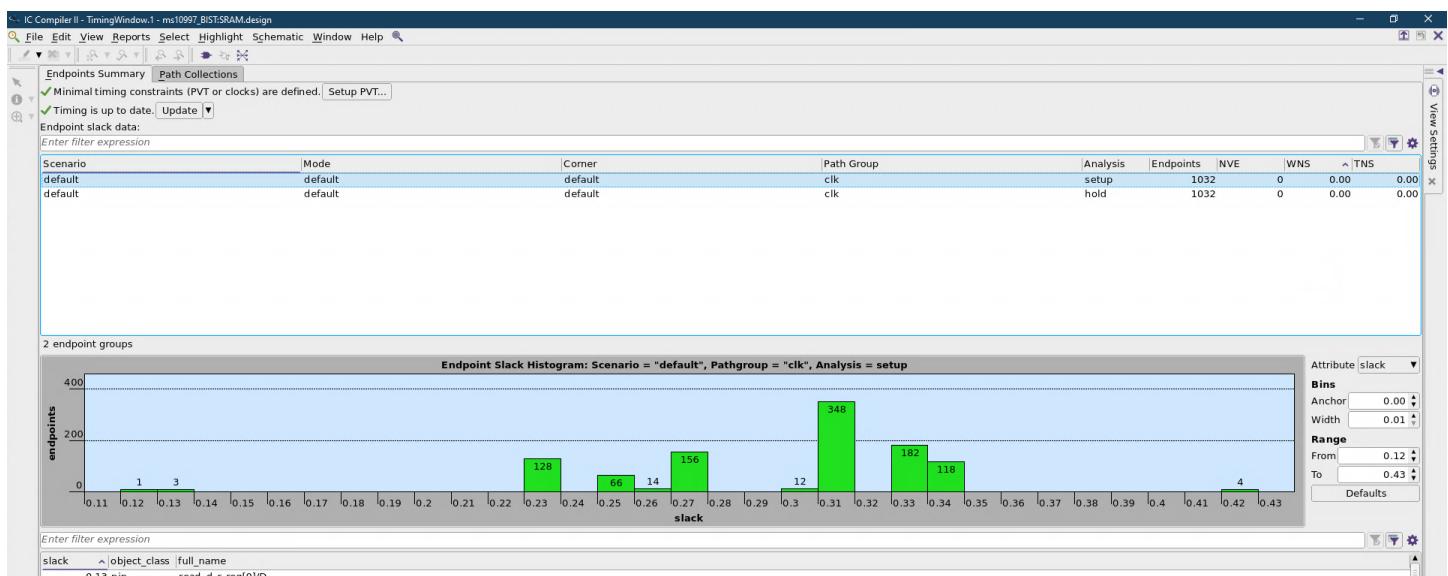


Report 2 PrimeTime Hold Violations 1.1 ns clk

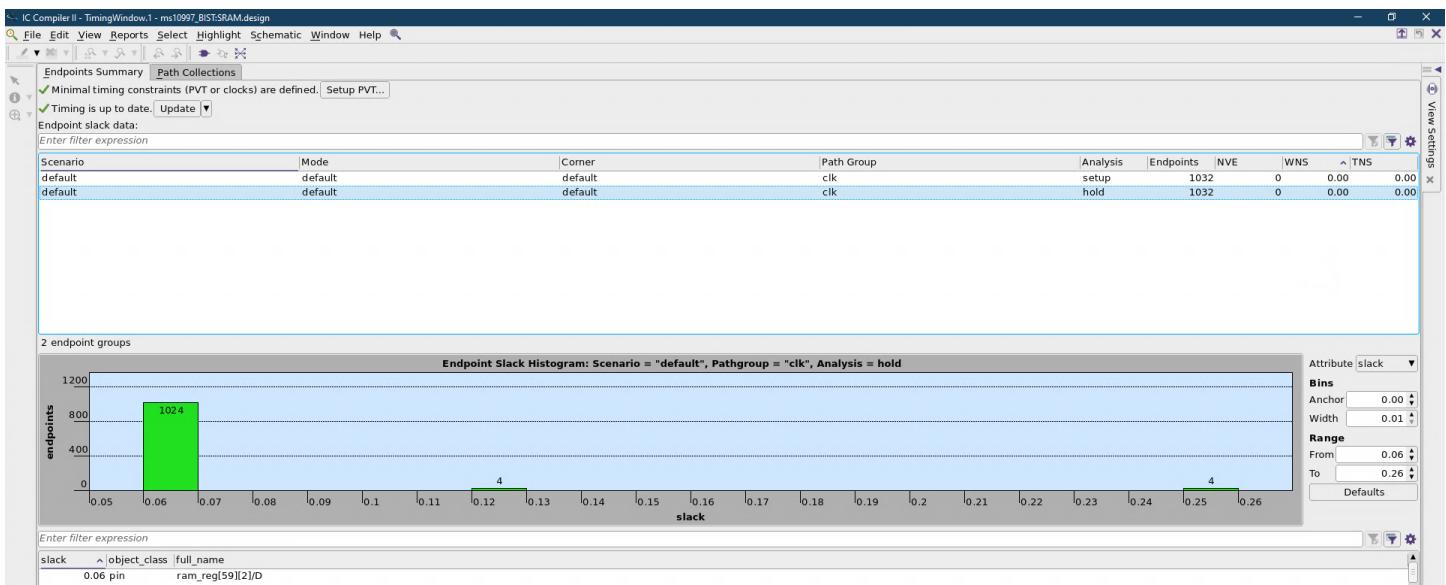
*File/Report included in zip.



Schematic 4 ICC2 Generated Layout



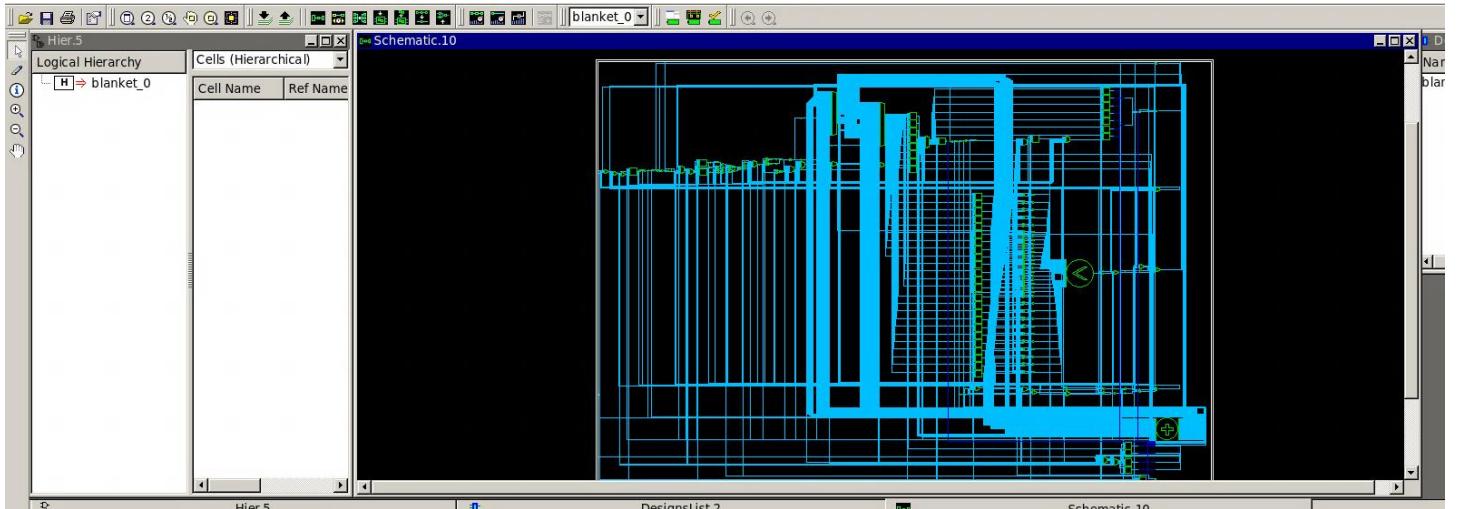
*File/Report included in zip.



Report 4 ICC2 Min Timing Report 1.1ns

*File/Report included in zip.

Blanket Generator Module (bg0)

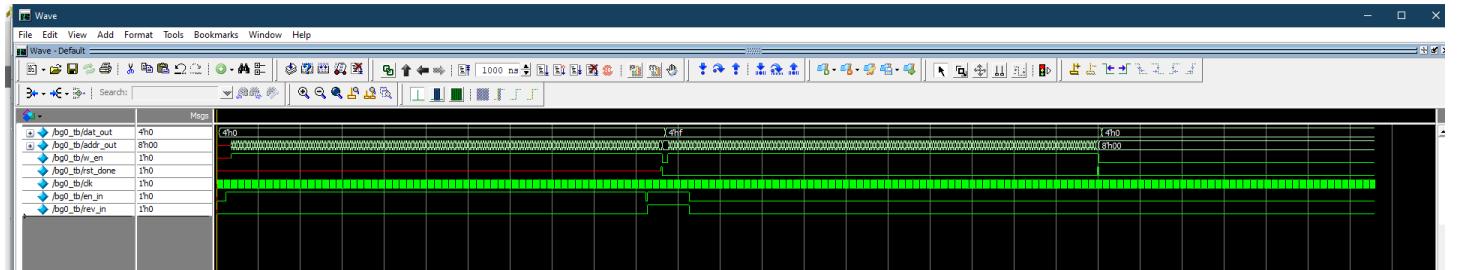


Schematic 5 Blanket Module Uncompiled

Technical Specifications:

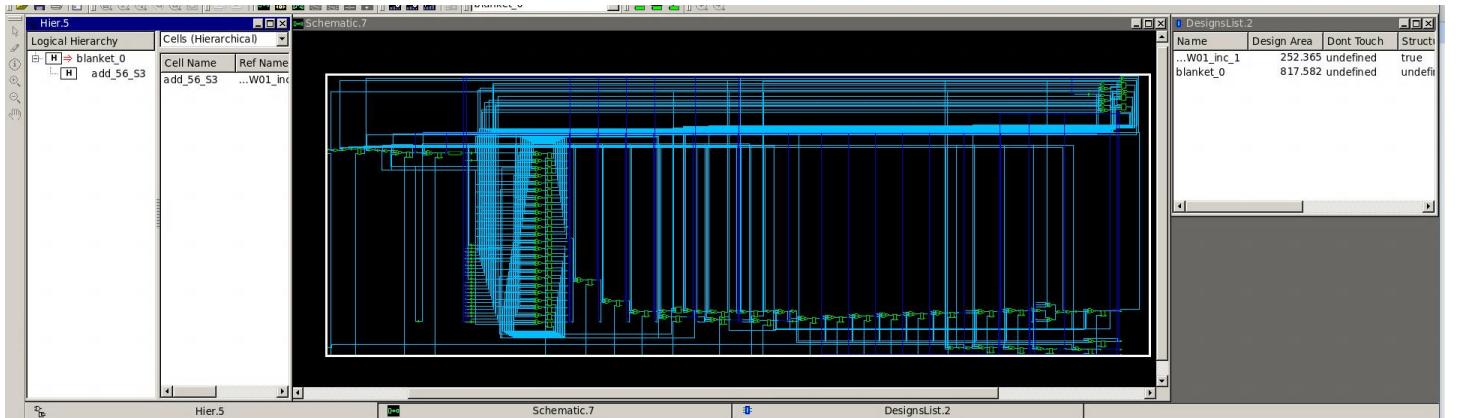
- Select line Rev_in controls Blanket -0 or Blanket-1.
- Rst_done signal indicates that operation is complete.
- Target Clock Period = 3 ns
- Achieved Clock Period = 1 ns

ModelSim (blanket_0)



Waveform 2 blanket_0 then Blanket-1 Write and then Read testbench

Normal Compile



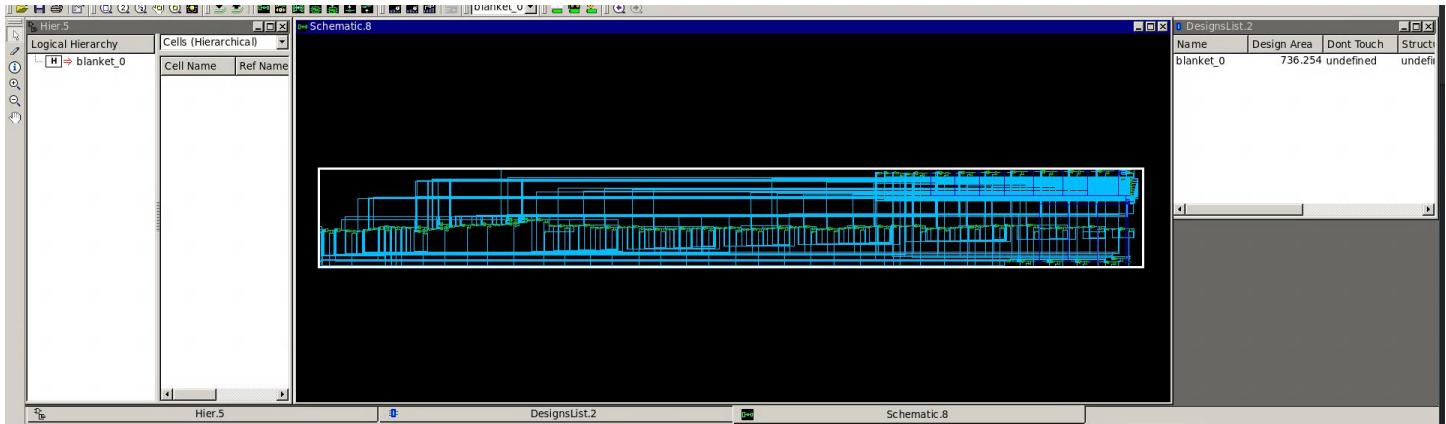
Schematic 6 Normal Compile Blanket Generator

- Min Clock Period Achieved = 1 ns

*File/Report included in zip.

Reports Included

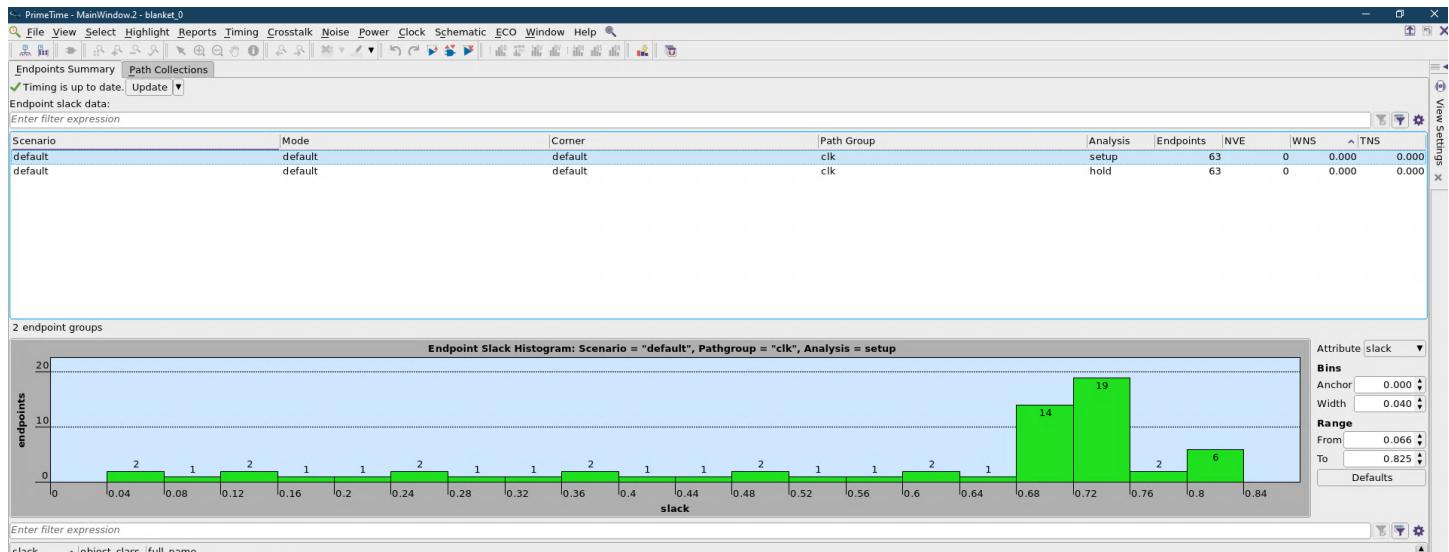
Ultra-Compile



Schematic 7 Ultra Compile Blanket Generator

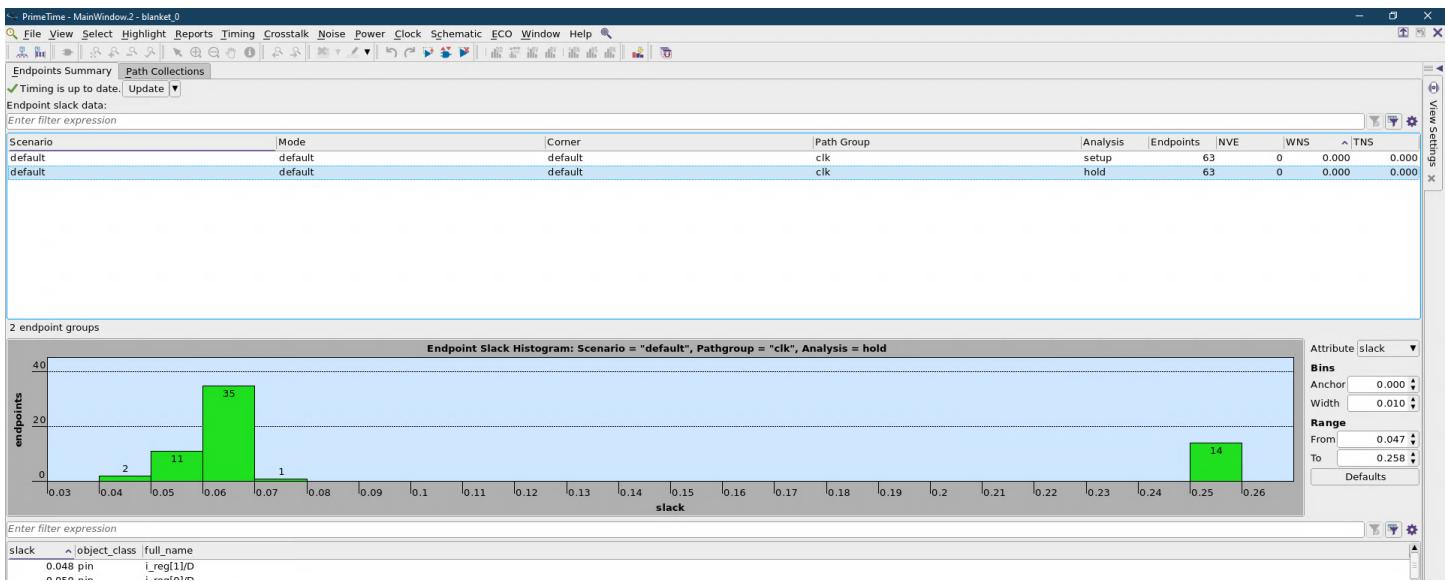
- Min Clock Period Achieved = 1 ns
- Reports Included.

PrimeTime

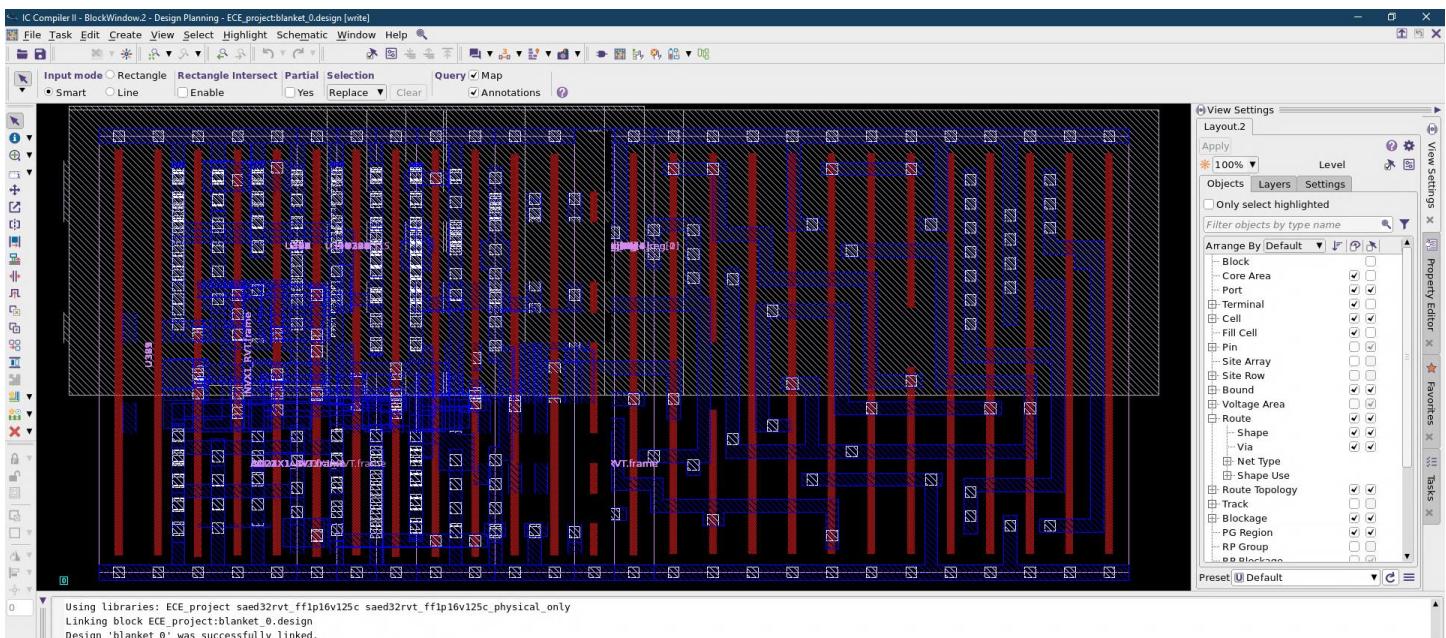


Report 5 PrimeTime Setup Violations 1ns clk

*File/Report included in zip.

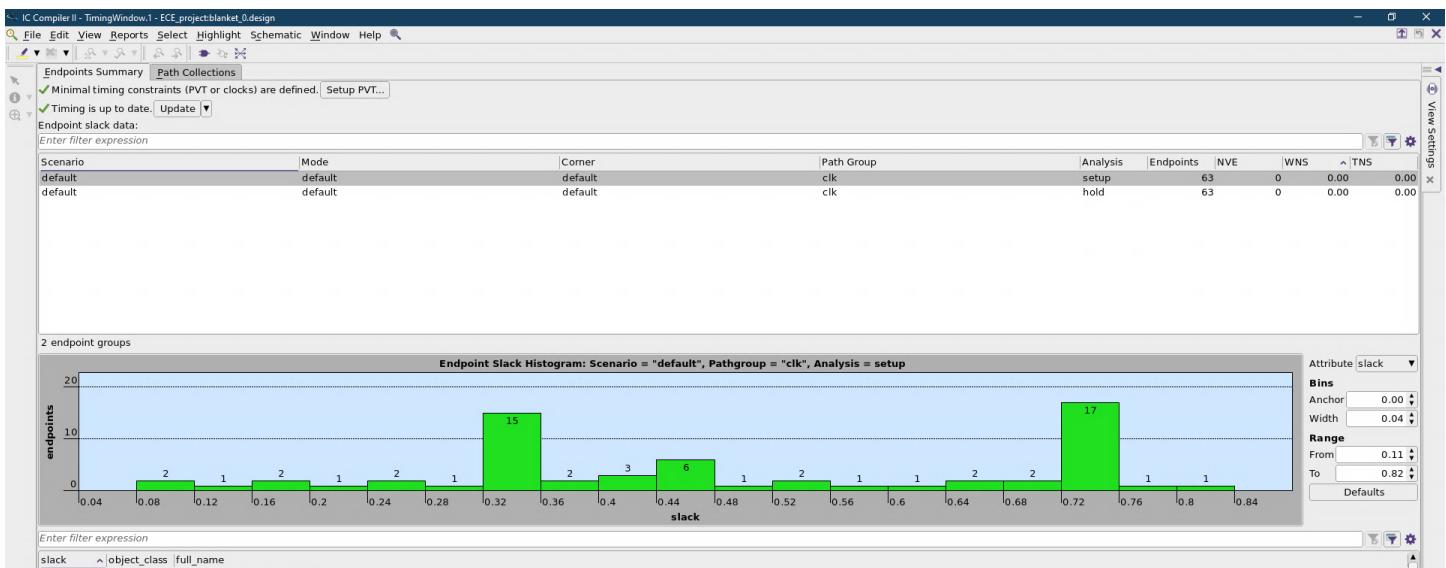


Report 6 PrimeTime Hold Violations 1 ns clk

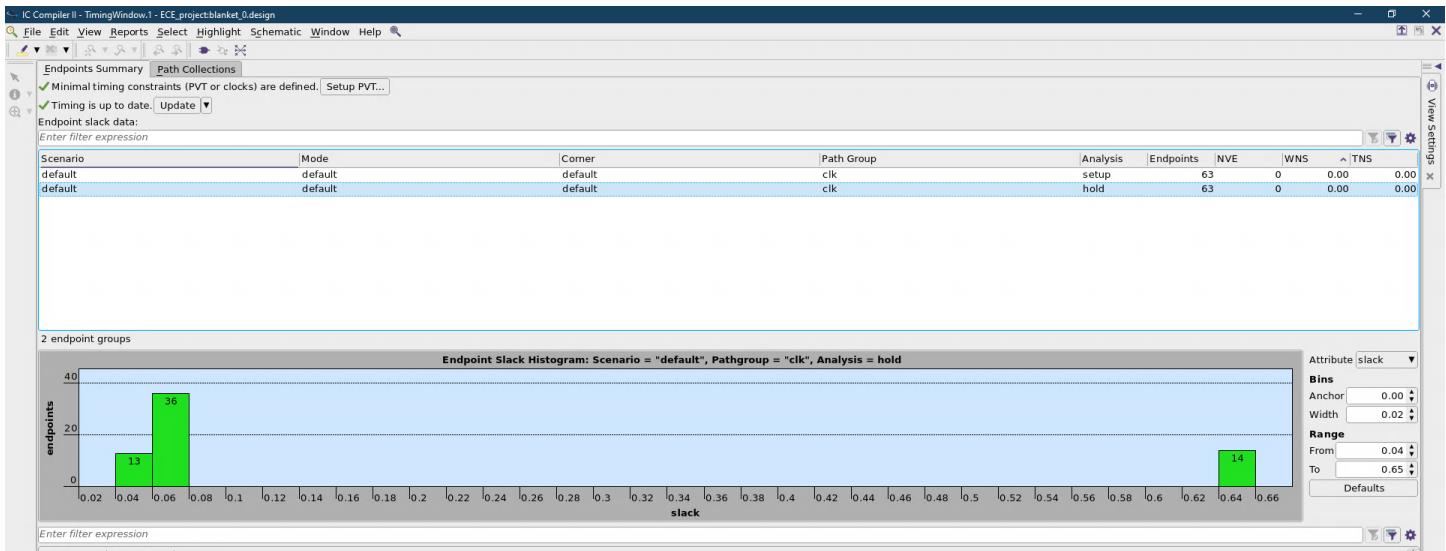


Schematic 8 ICC2 Generated Layout

*File/Report included in zip.



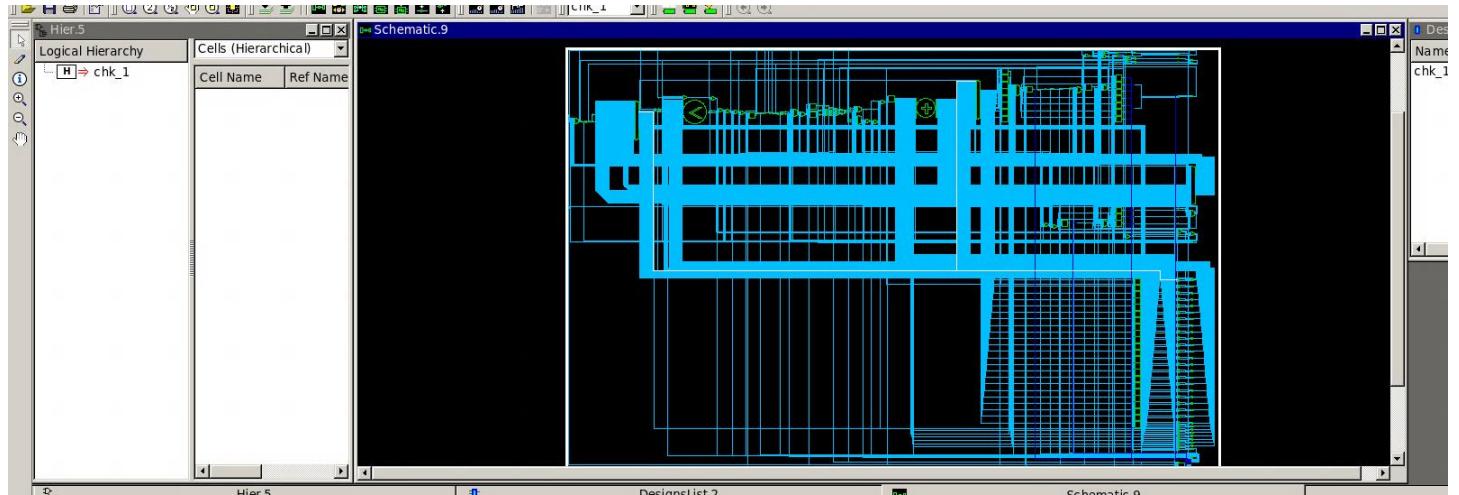
Report 7 ICC2 Max Timing Report 1ns



Report 8 ICC2 Min Timings Report 1ns

*File/Report included in zip.

Checkerboard Generator Module (chk_0)

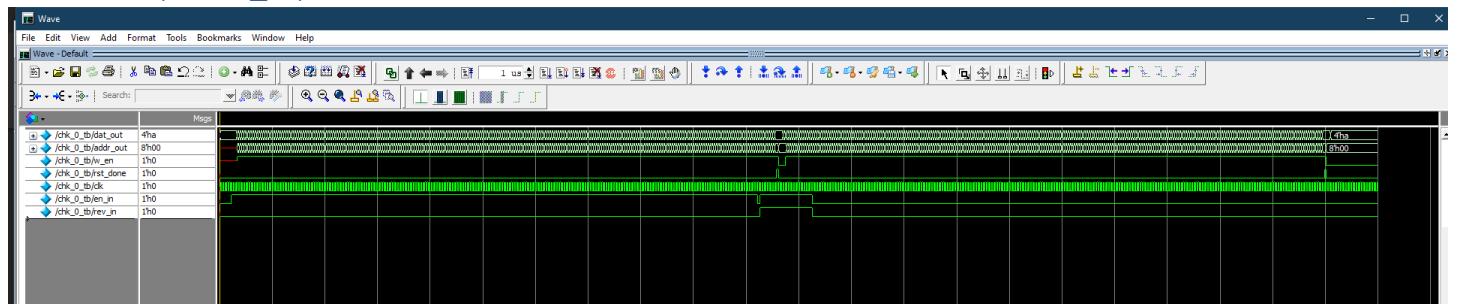


Schematic 9 Checkerboard Module Uncompiled

Technical Specifications:

- Select line Rev_in controls Checkerboard Forward or Reverse.
- En_in Signal activates the pattern generation
- Rst_done signal indicates that operation is complete.
- Target Clock Period = 3 ns
- Achieved Clock Period = 1 ns

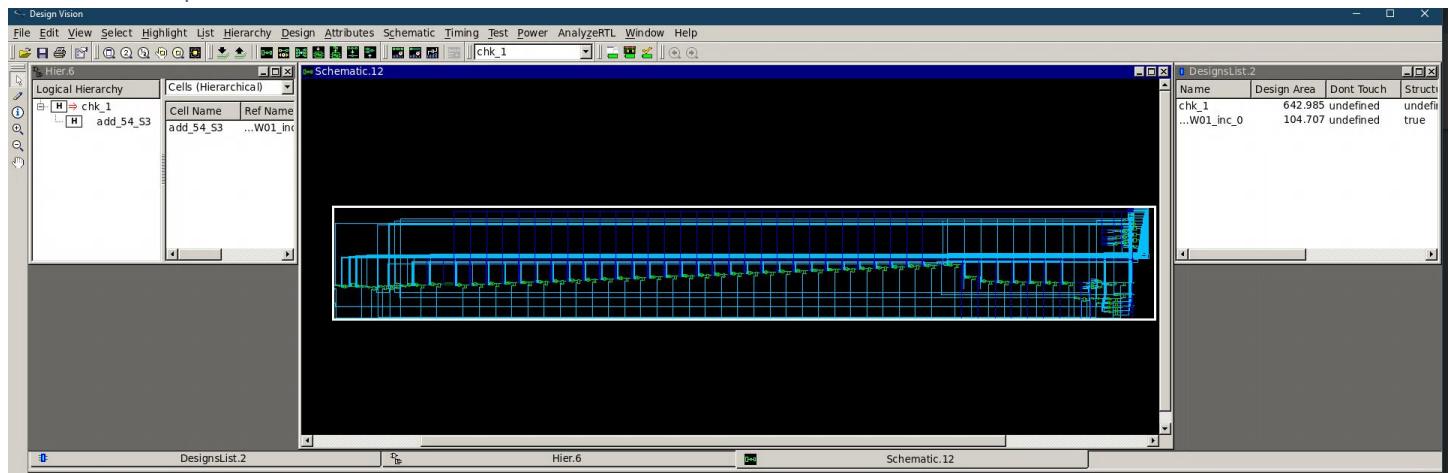
ModelSim (SRAM_tb)



Waveform 3 Checkerboard Write and then Read testbench

*File/Report included in zip.

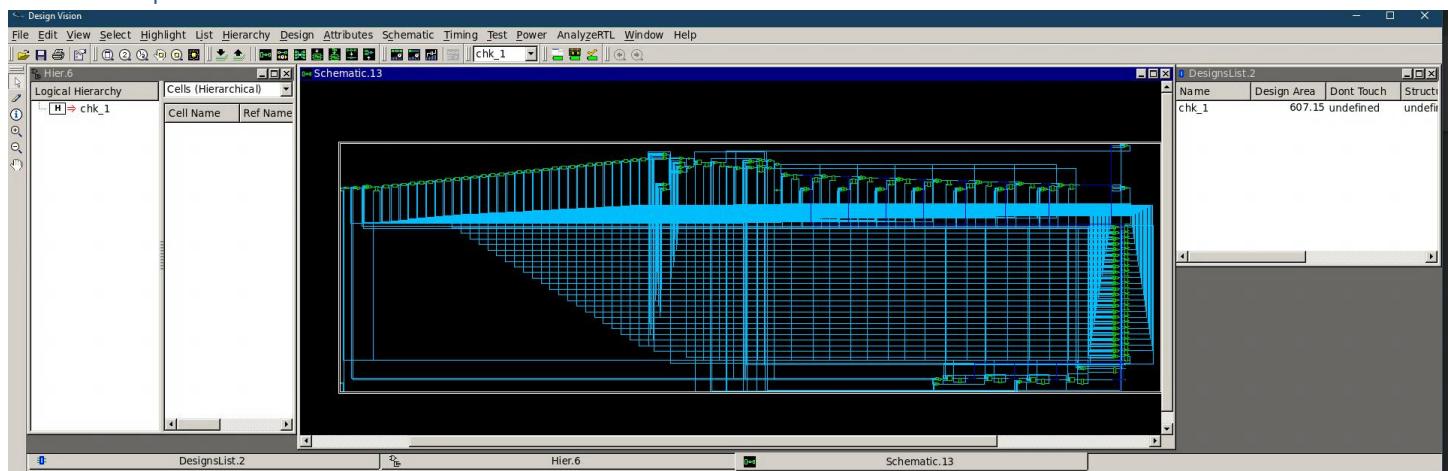
Normal Compile



Schematic 10 Normal Compile Checkerboard Generator

- Min Clock Period Achieved = 1 ns
- Reports Included

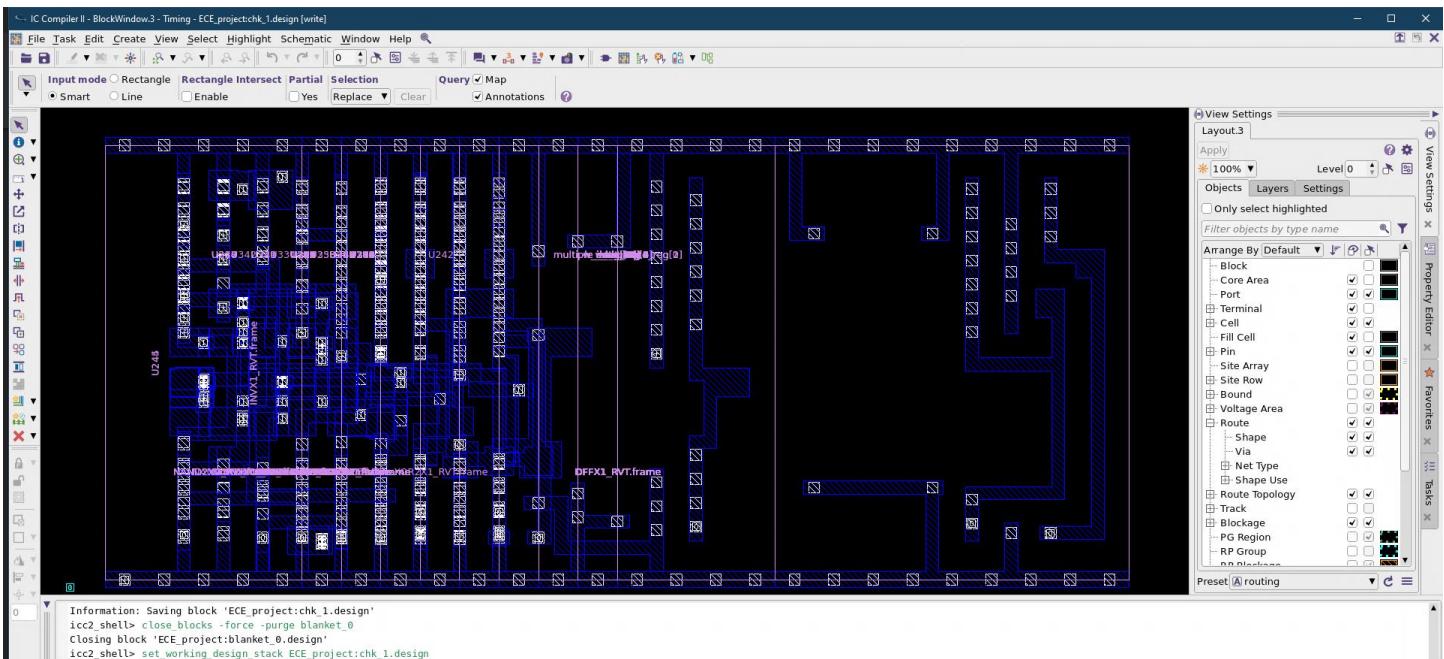
Ultra-Compile



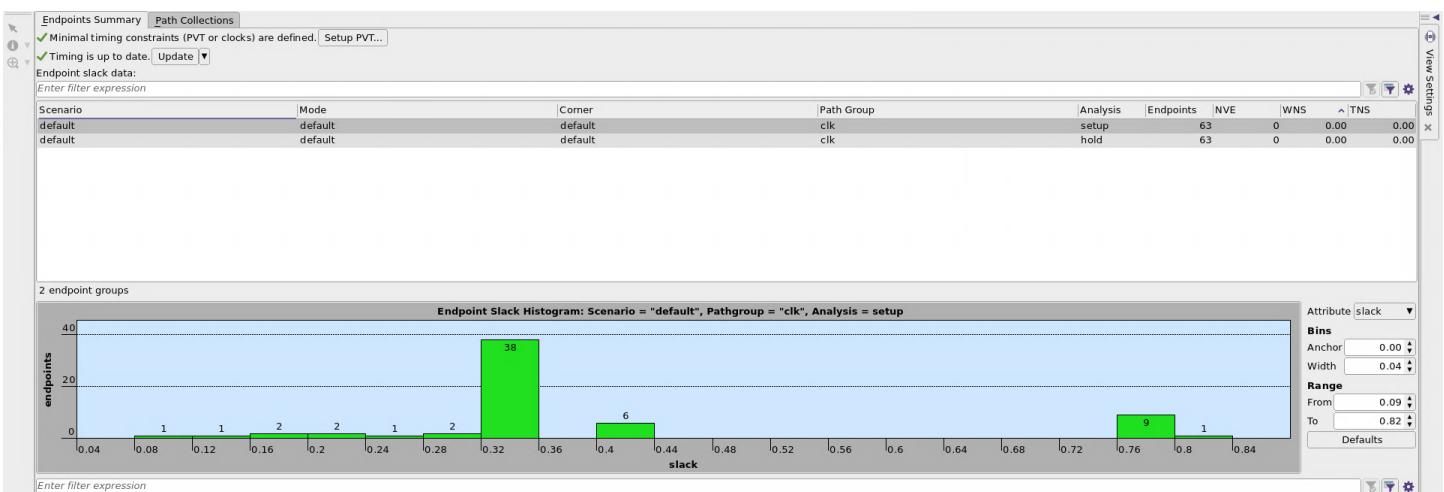
Schematic 11 Ultra Compile Checkerboard Generator

- Min Clock Period Achieved = 1 ns
- Reports Included.
- PrimeTime Analysis Passed.

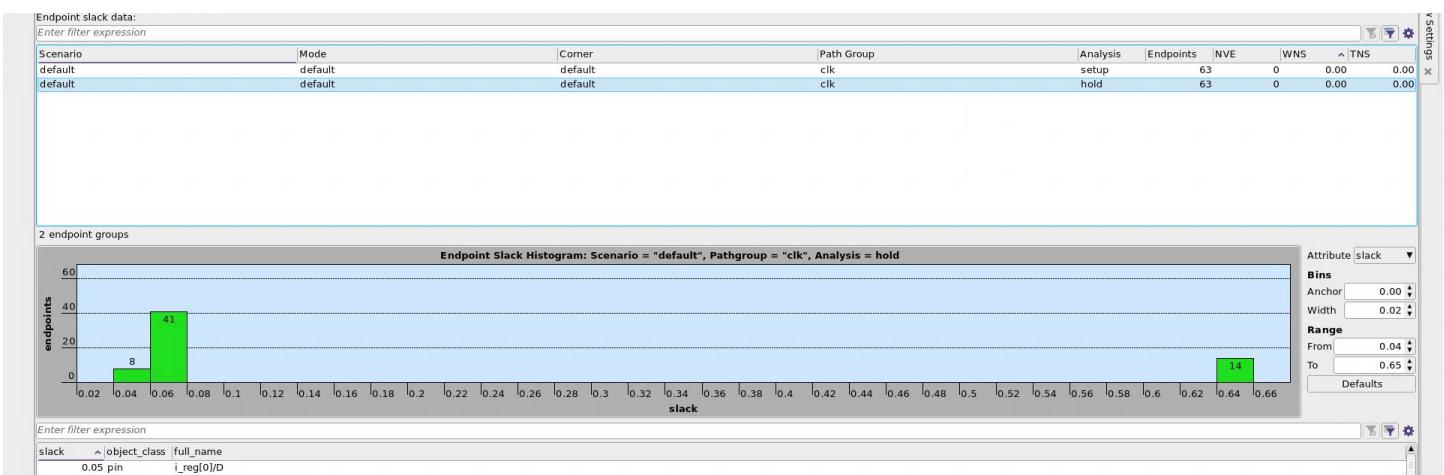
*File/Report included in zip.



Schematic 12 ICC2 Generated Layout



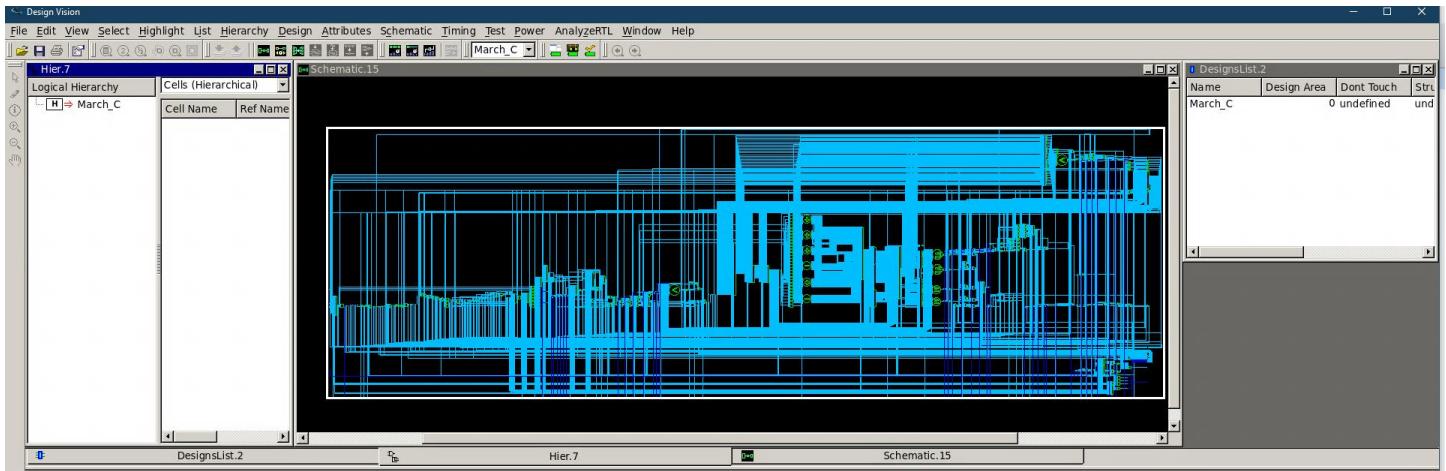
Report 9 ICC2/PrimeTime Max Timing Report 1ns



Report 10 ICC2/PrimeTime2 Min Timings Report 1ns

*File/Report included in zip.

March_C Module (mar_c)

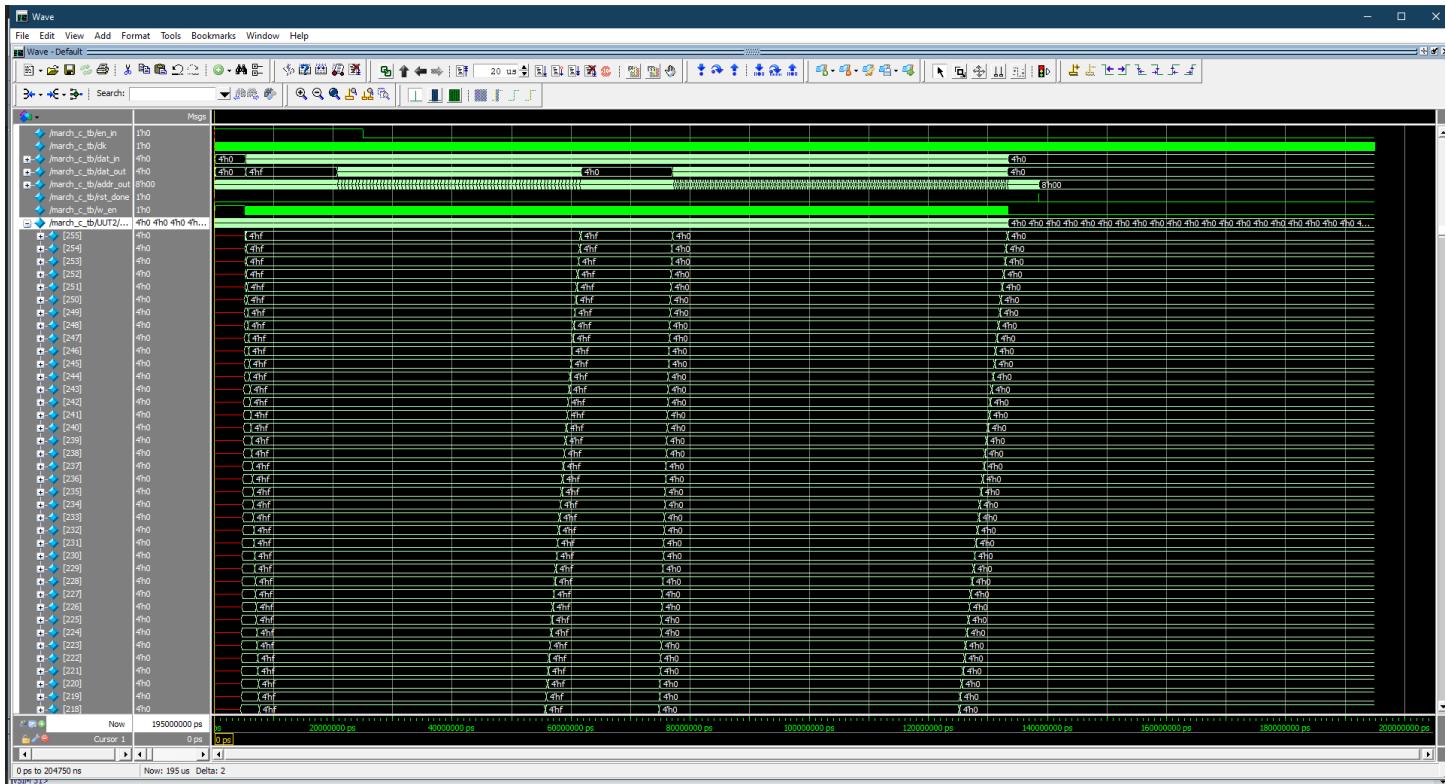


Schematic 13 March_C Module Uncompiled

Technical Specifications:

- Select line Rev_in controls Checkerboard Forward or Reverse.
- Rst_done signal indicates that operation is complete.
- Target Clock Period = 3 ns
- Achieved Clock Period = 1.8 ns

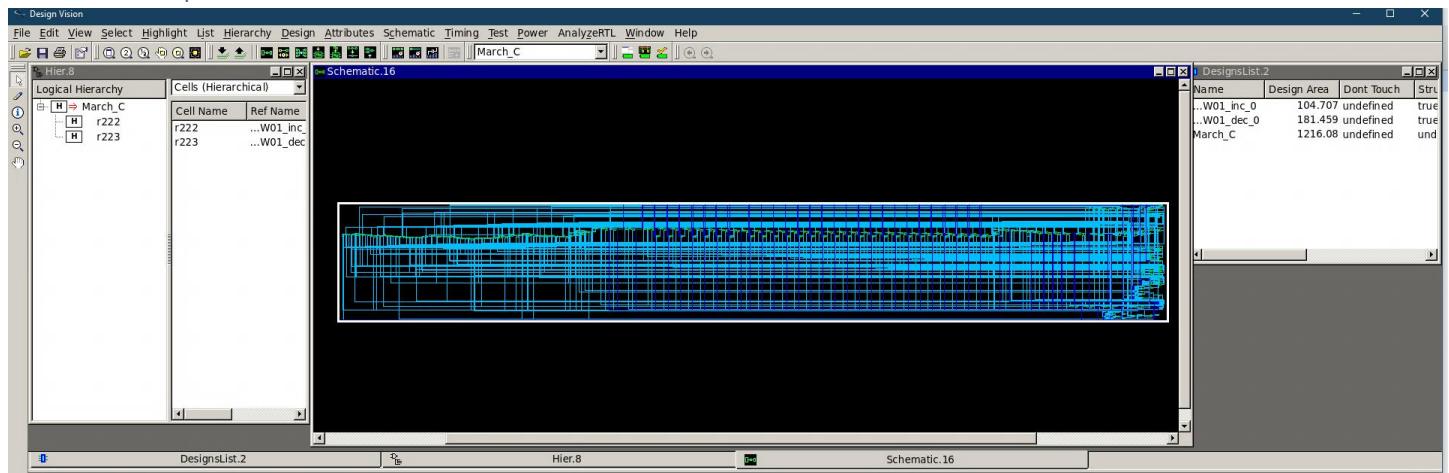
ModelSim (mar_c_tb)



Waveform 4 March_C Write and then Read testbench

*File/Report included in zip.

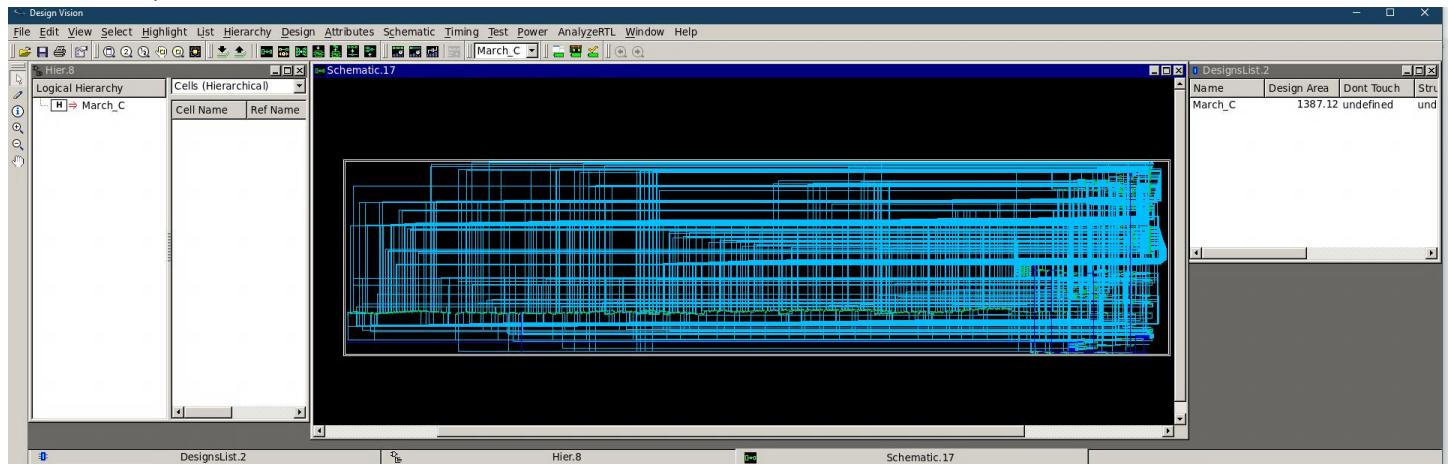
Normal Compile



Schematic 14 Normal Compile Checkerboard Generator

- Min Clock Period Achieved = 1.8 ns
- Reports Included

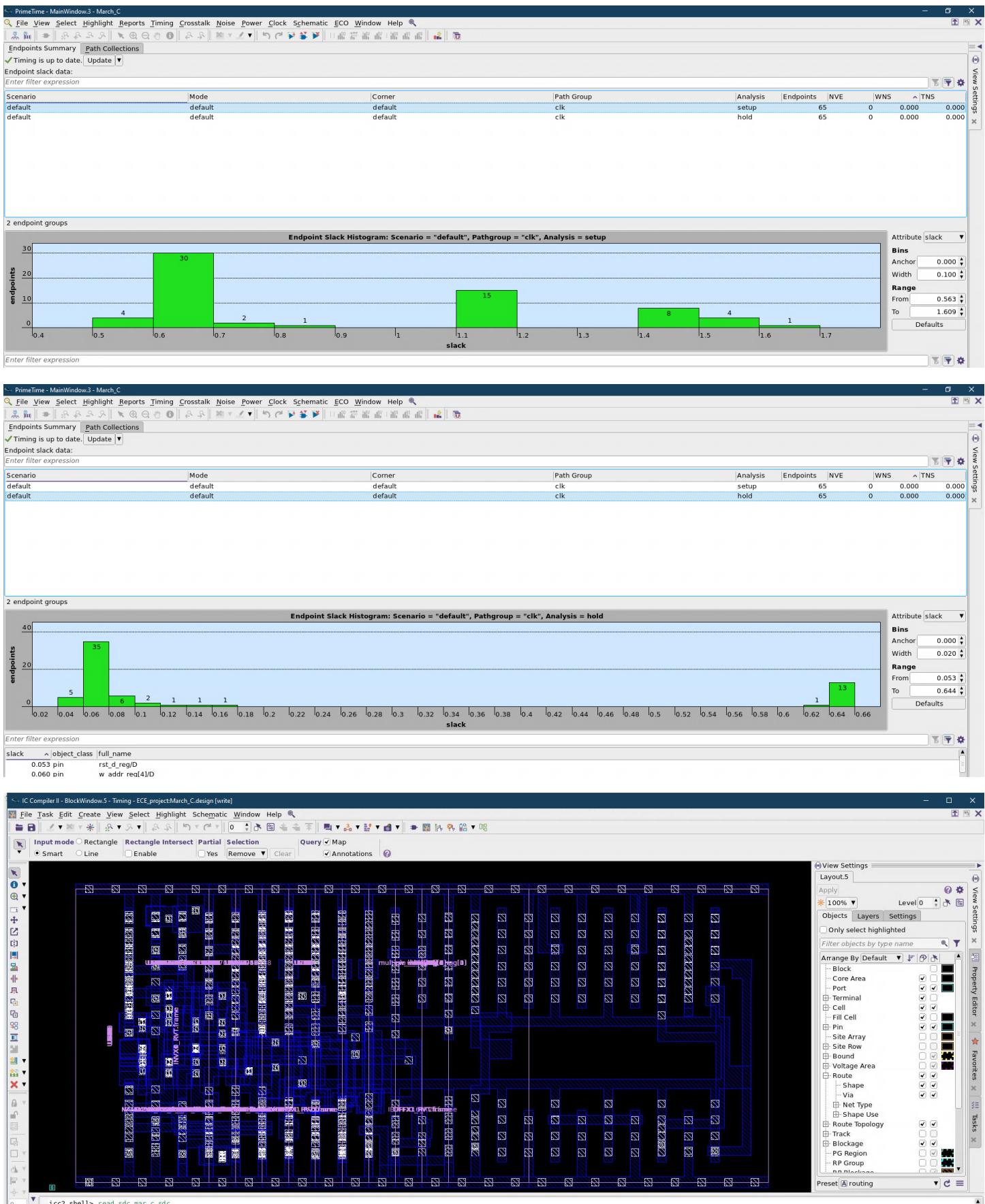
Ultra-Compile



Schematic 15 Ultra Compile Checkerboard Generator

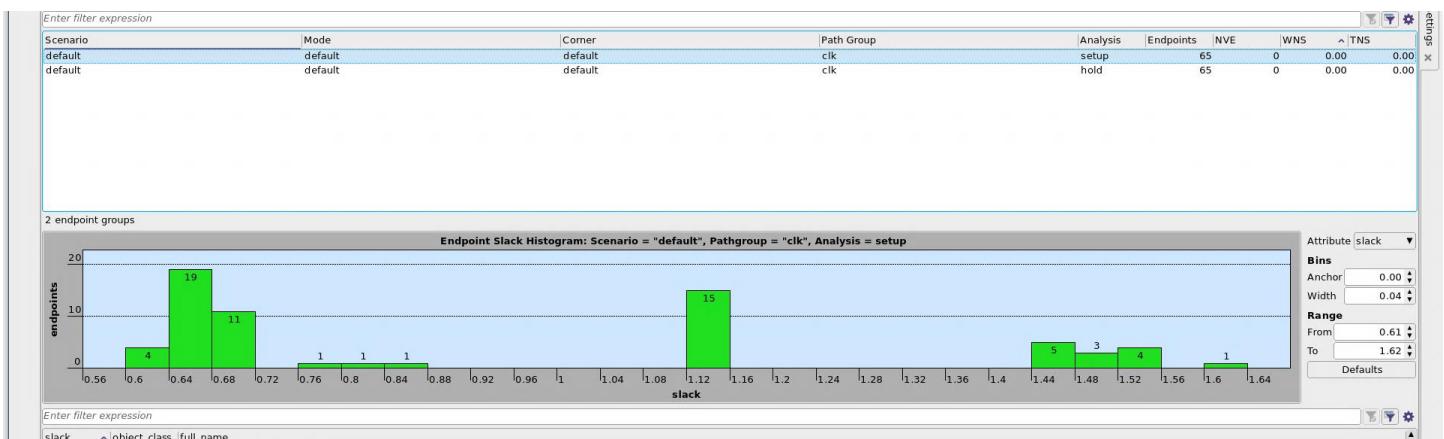
- Min Clock Period Achieved = 1.8 ns
- Reports Included.

*File/Report included in zip.

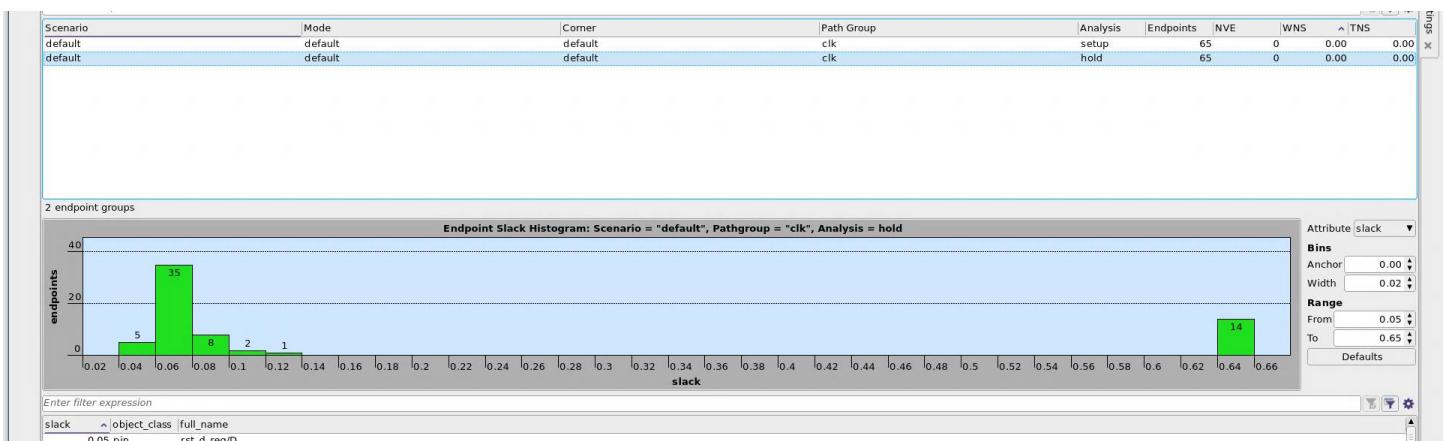


Schematic 16 ICC2 Generated Layout

*File/Report included in zip.



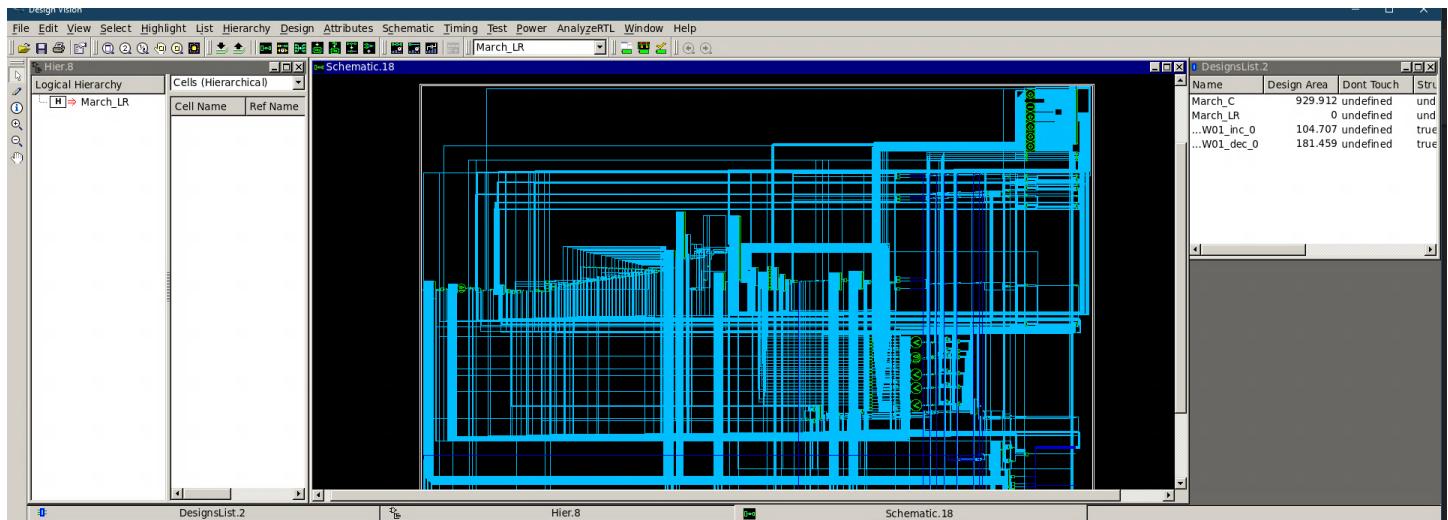
Report 11 ICC2 Max Timing Report 1.8ns



Report 12 ICC2 Min Timings Report 1.8ns

*File/Report included in zip.

March_LR Module (mar_lr)



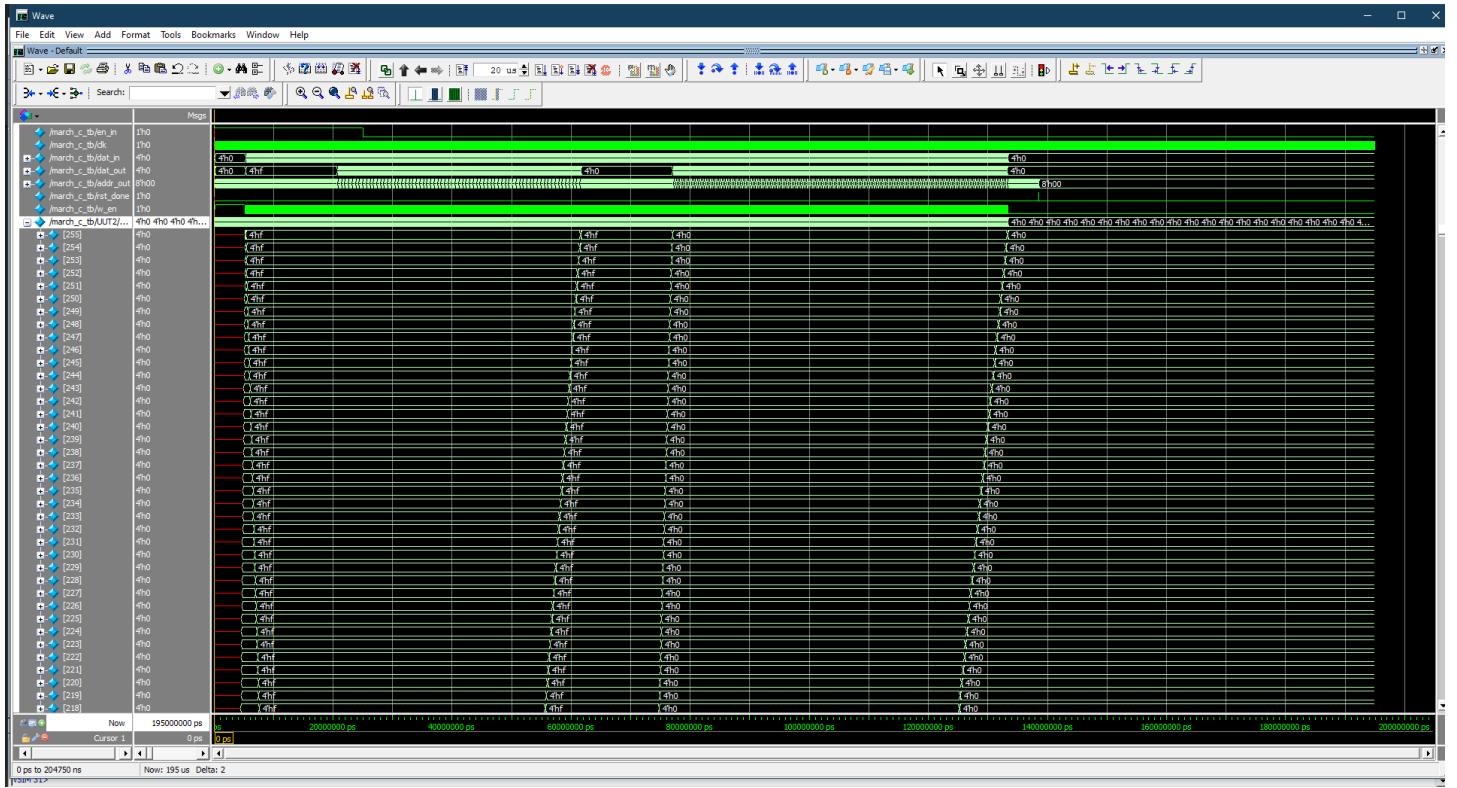
Schematic 17 March_C Module Uncompiled

Technical Specifications:

- Select line Rev_in controls Checkerboard Forward or Reverse.
- Rst_done signal indicates that operation is complete.
- Target Clock Period = 3 ns
- Achieved Clock Period = 2.2 ns

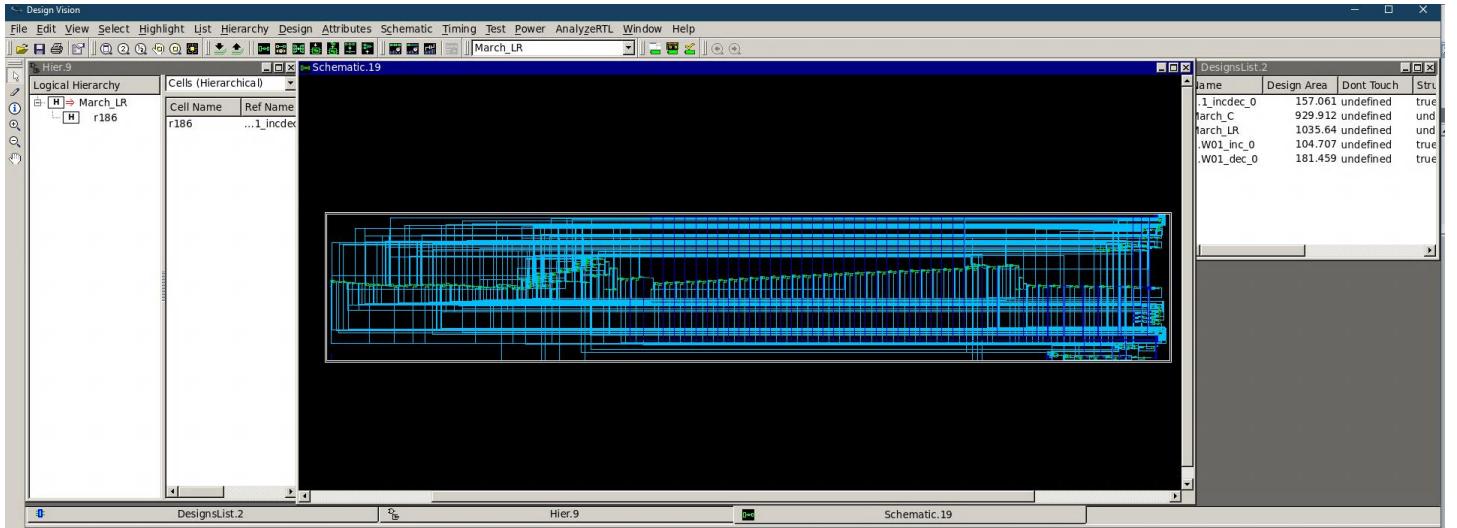
*File/Report included in zip.

ModelSim (mar_c_tb)



Waveform 5 March_C Write and then Read testbench

Normal Compile

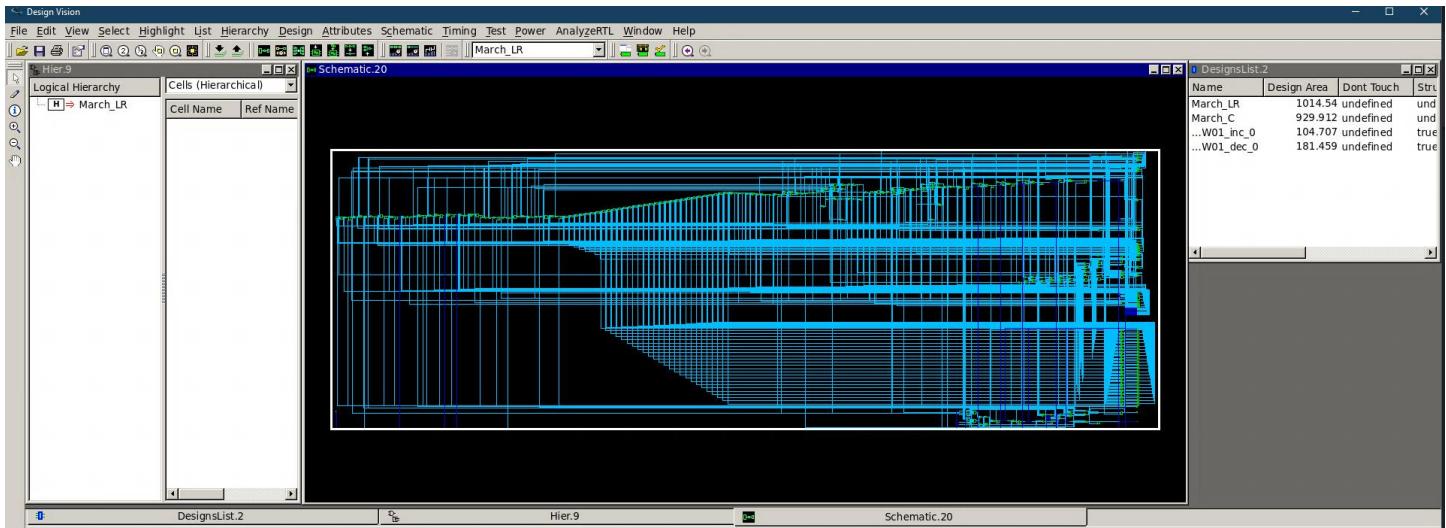


Schematic 18 Normal Compile March_C

- Min Clock Period Achieved = 2.2 ns
- Reports Included

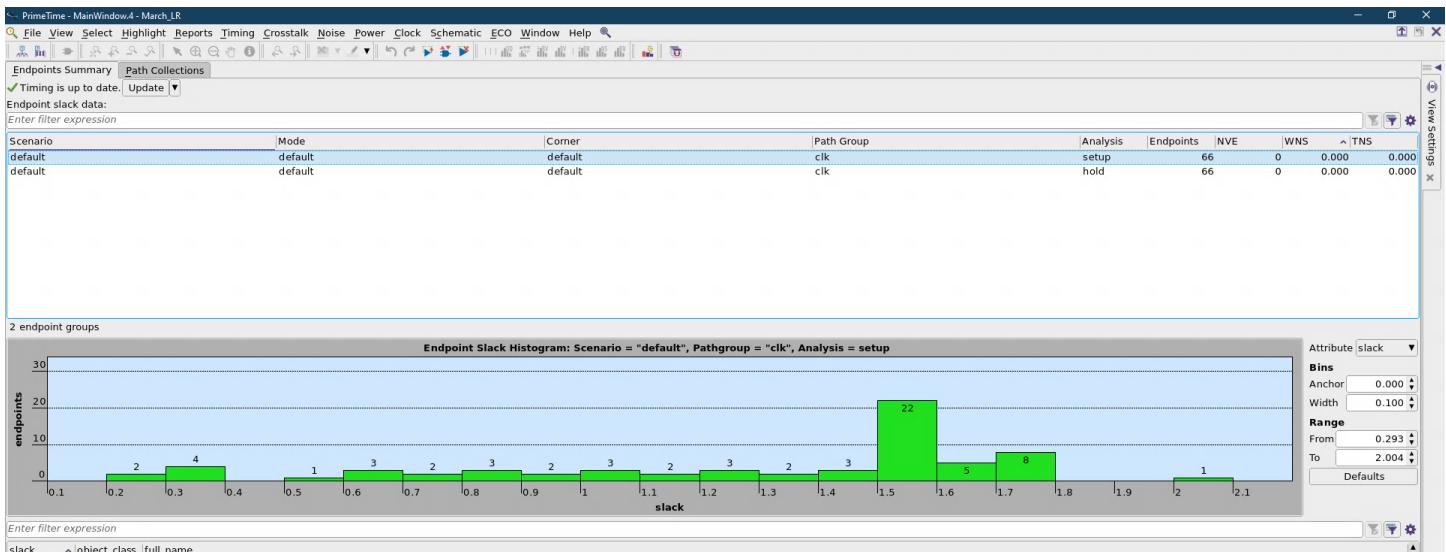
*File/Report included in zip.

Ultra-Compile



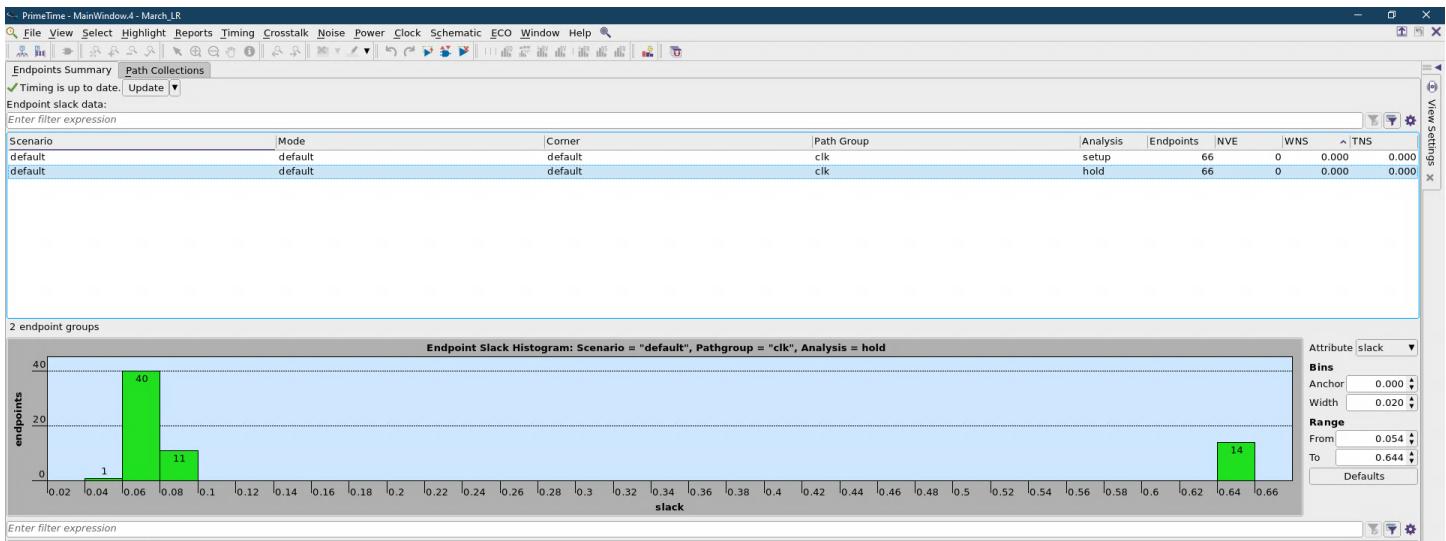
Schematic 19 Ultra Compile March_C

- Min Clock Period Achieved = 2.2 ns
- Reports Included.

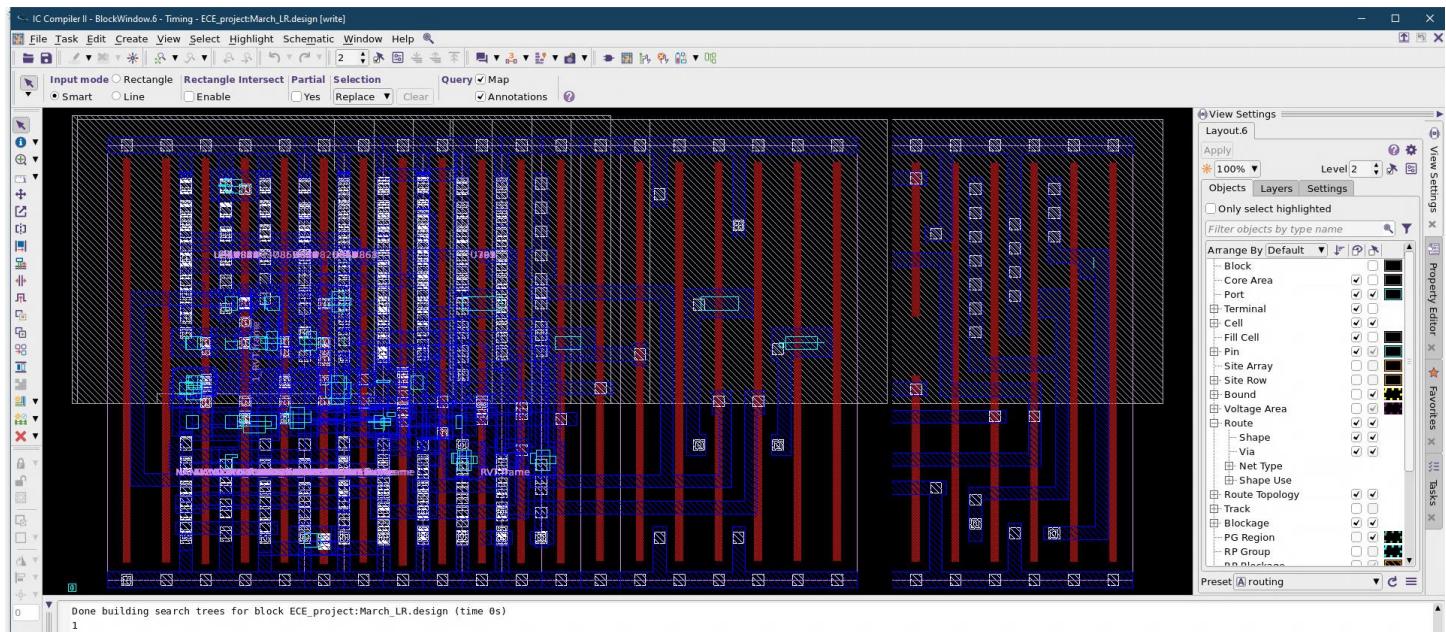


Report 13 PrimeTime Max Delays 2.2ns

*File/Report included in zip.

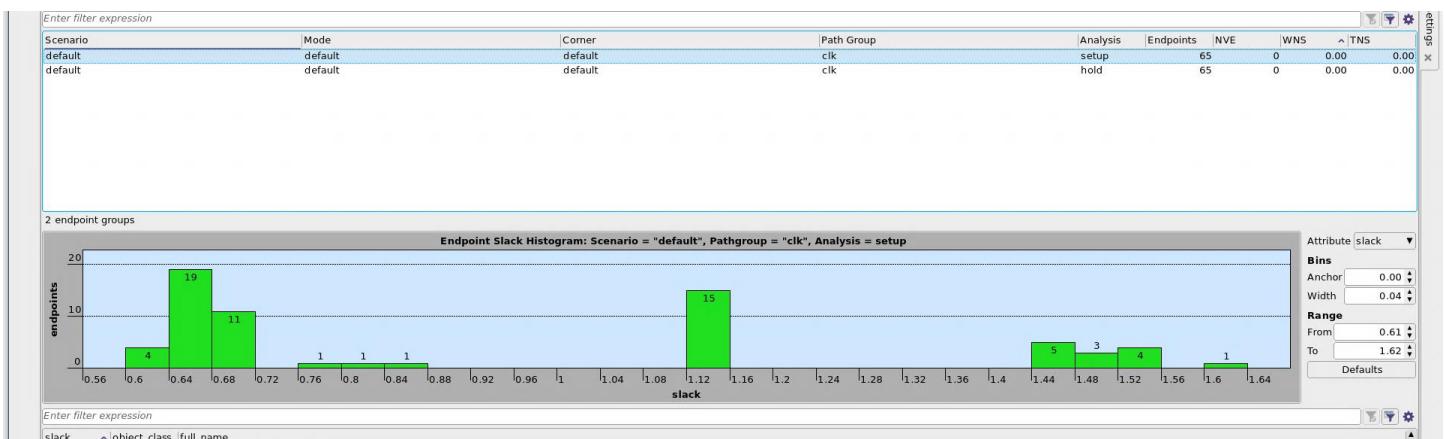


Report 14 Primetime Min Delays 2.2ns

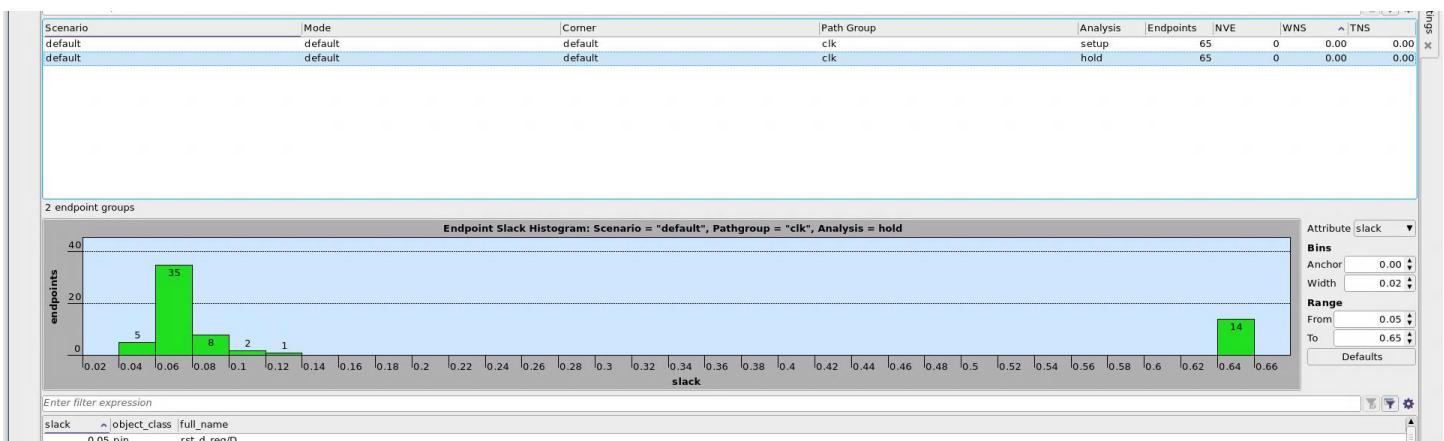


Schematic 20 ICC2 Generated Layout

*File/Report included in zip.



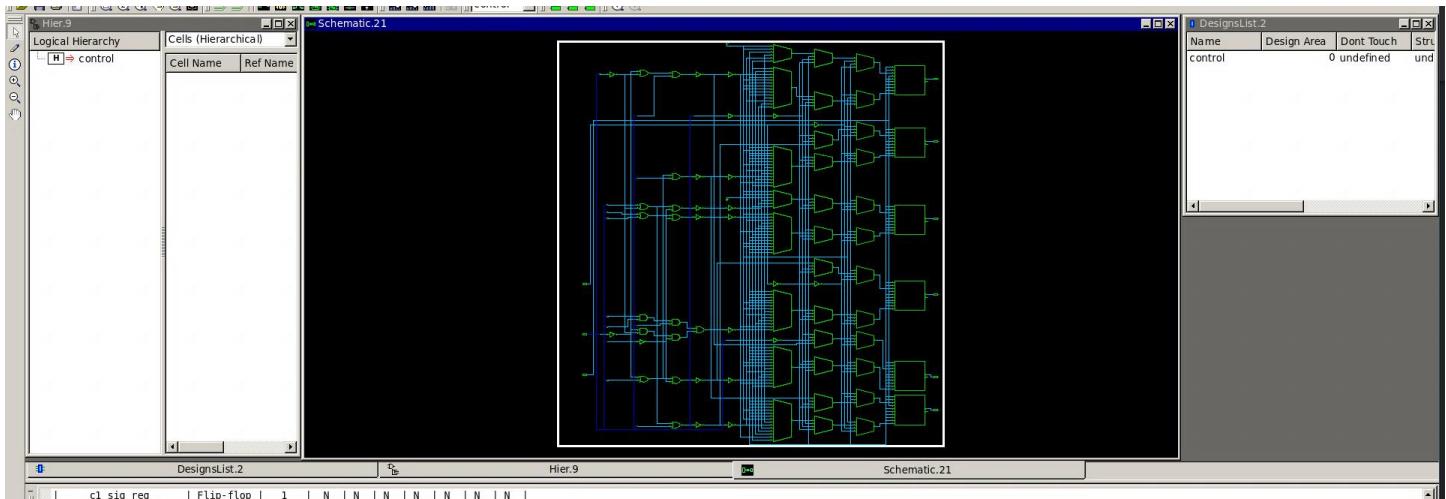
Report 15 ICC2 Max Timing Report 2.2ns



Report 16 ICC2 Min Timings Report 2.2ns

*File/Report included in zip.

Control Unit (Control_unit)

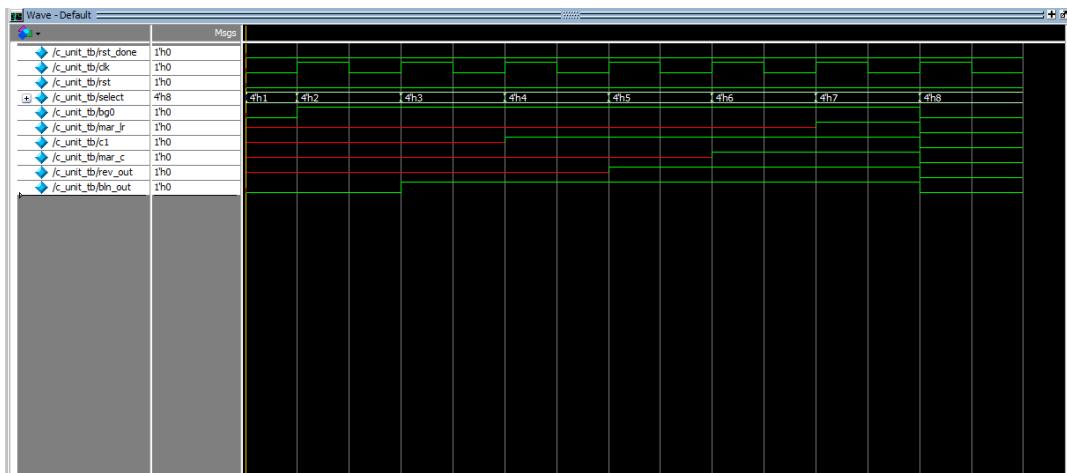


Schematic 21 Control Unit Module Uncompiled

Technical Specifications:

- Select lines act as Mode bits
 1. Blanket -0
 2. Blanket -1
 3. Checkerboard Forward
 4. Checkerboard Reverse
 5. March_C
 6. March_LR
 0. NO Operation (Normal SRAM Operation)

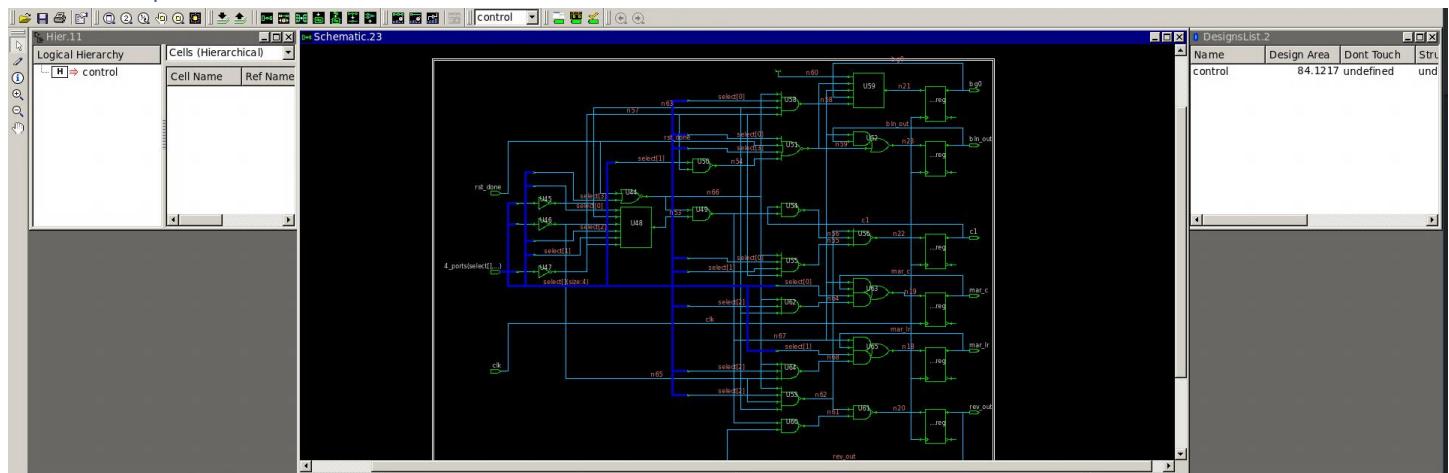
ModelSim (c_unit_tb)



Waveform 6 c_unit Write and then Read testbench

*File/Report included in zip.

Ultra-Compile

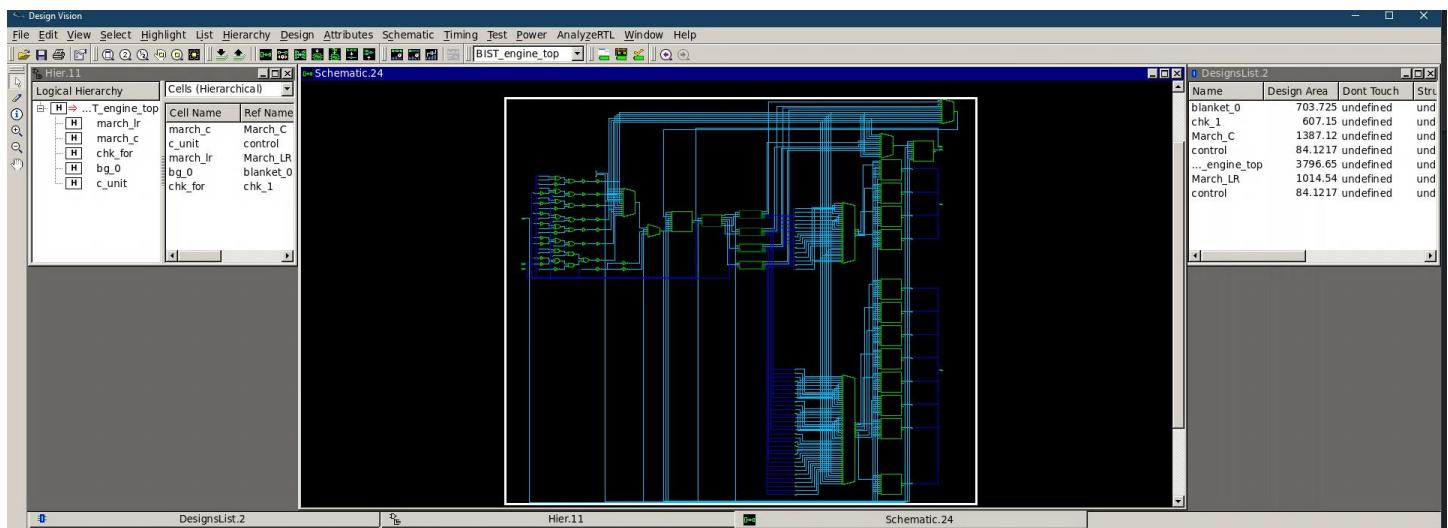


Schematic 22 Ultra Compile Control Unit

- Min Clock Period Achieved = 1 ns
 - Reports Included.

*File/Report included in zip.

BIST ENGINE Top Module (mar_lr)



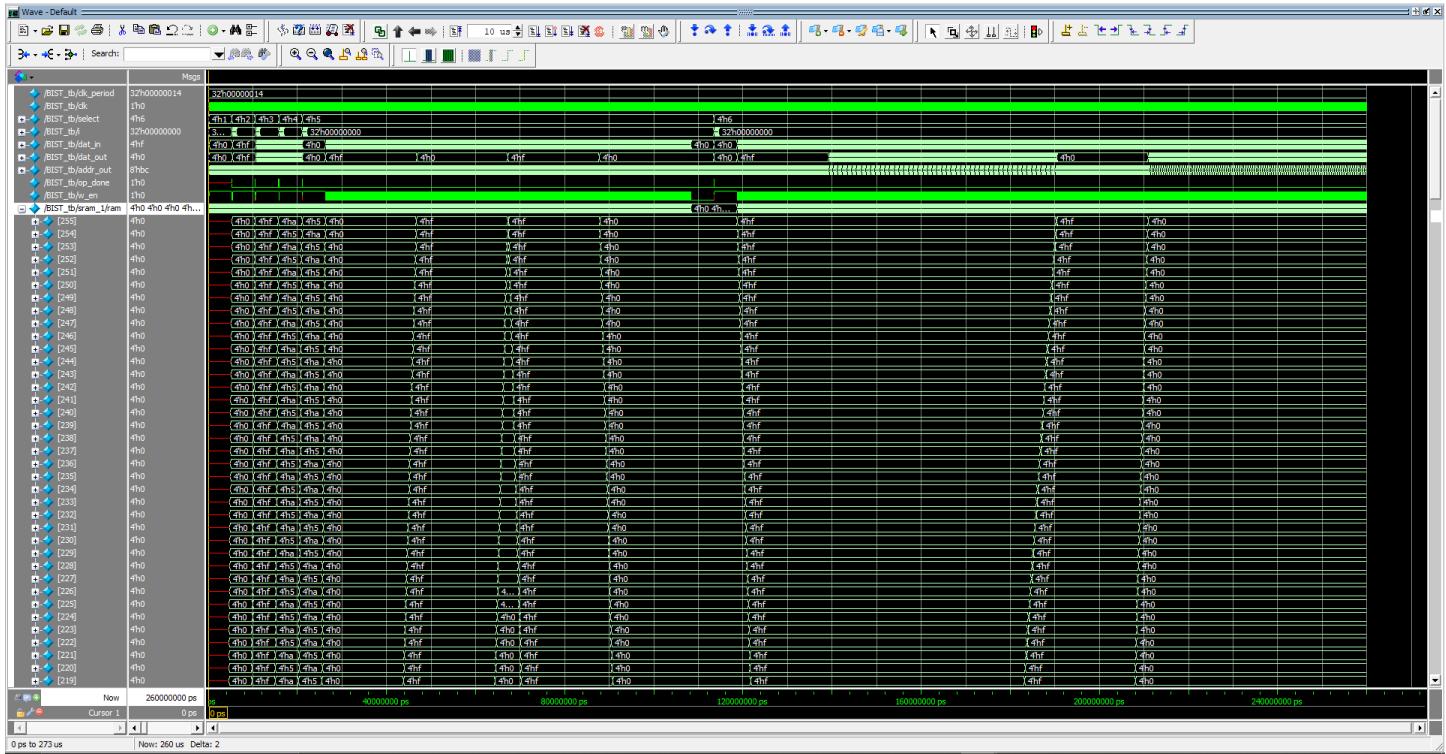
Schematic 23 BIST Engine Top Module Uncompiled

Technical Specifications:

- BIST Engine consists of 5 modules
 1. Blanket Generator
 2. Checkerboard Generator
 3. March_C
 4. March_LR
 5. Control Unit
- The testbench is configured to automatically switch between all possible patterns, the patterns being tested are controlled by mode bits (select[3:0]) , currently select1-6 is mapped to patterns as described in the control unit section.
- Select 0 is normal SRAM operation.
- BIST_engine was ungrouped during ultra-compile for better results. No cells were lost.

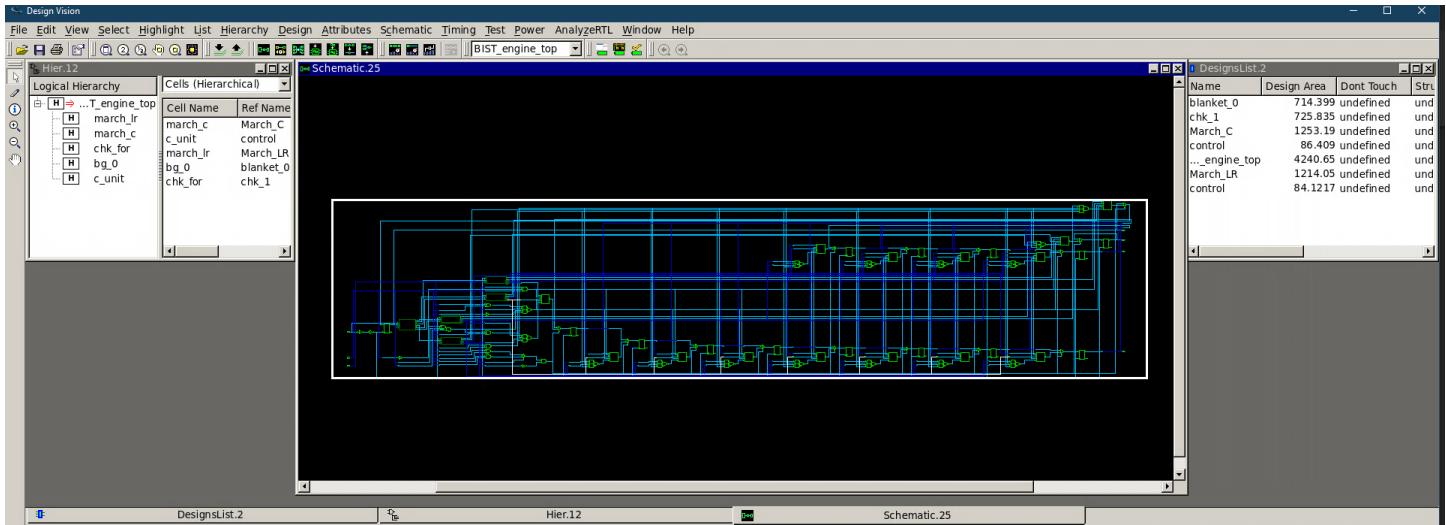
*File/Report included in zip.

ModelSim (BIST_Engine_tb)



Waveform 7 BIST_Engine Waveform

Normal Compile

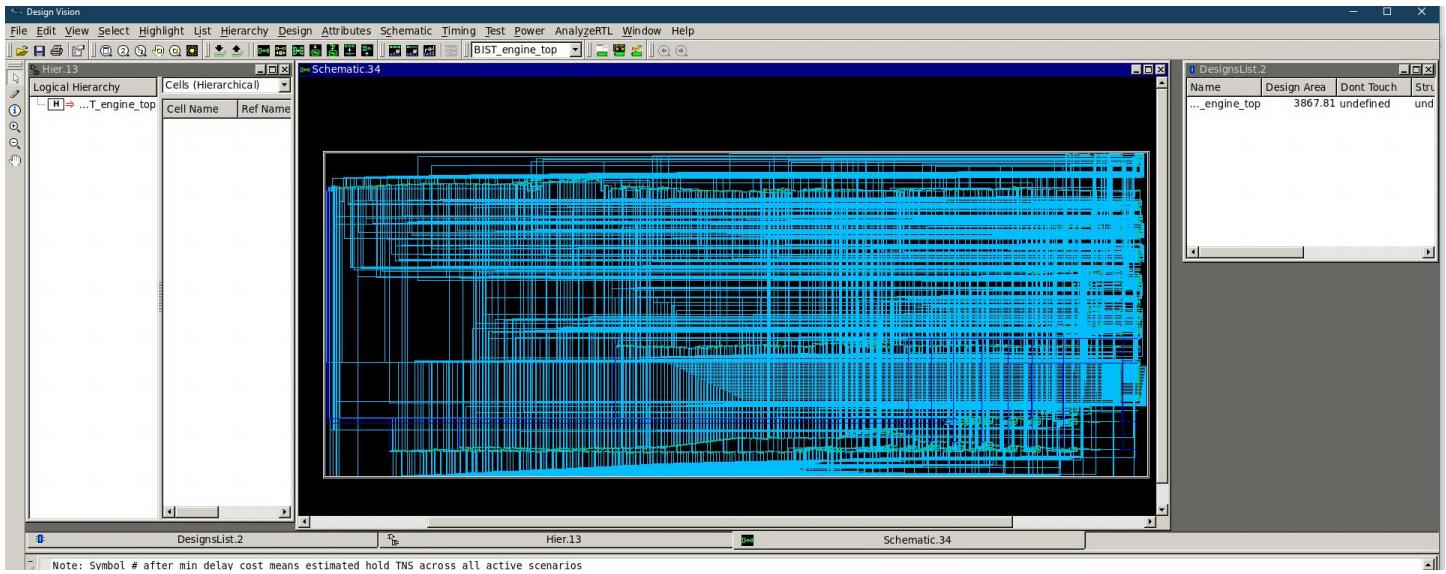


Schematic 24 Normal Compile BIST_Engine

- Min Clock Period Achieved = 2.2 ns
- Reports Included

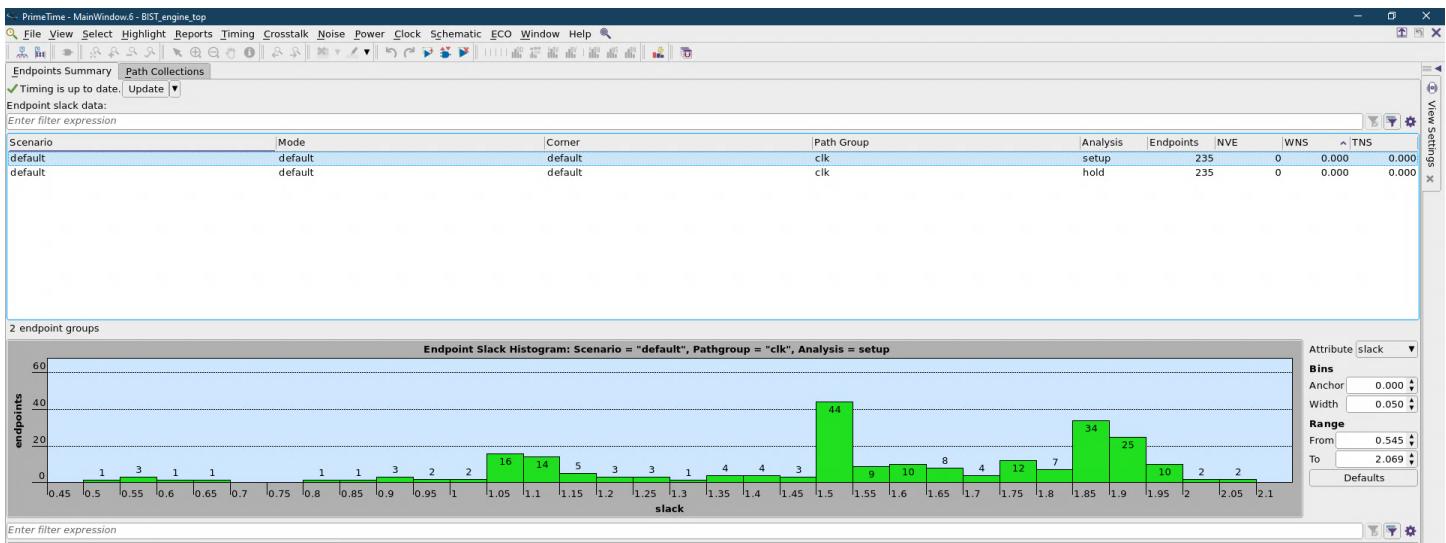
*File/Report included in zip.

Ultra-Compile



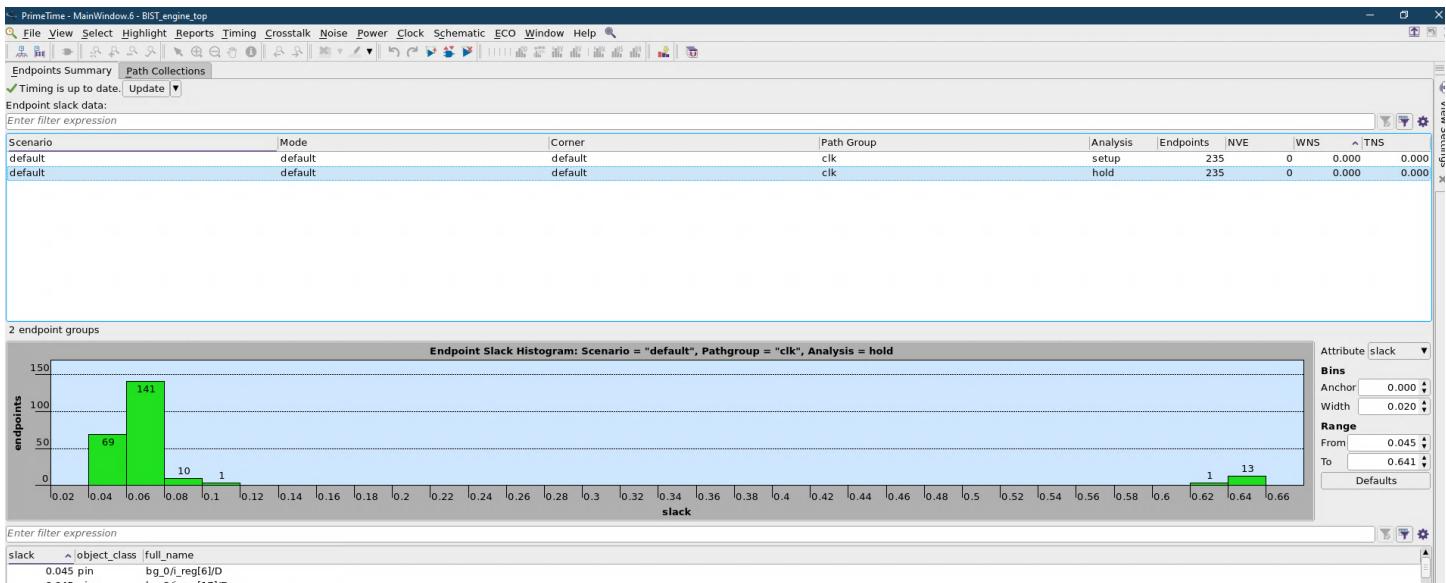
- Schematic 25 Ultra Compile BIST_Engine

- Min Clock Period Achieved = 2.2 ns
- Reports Included.

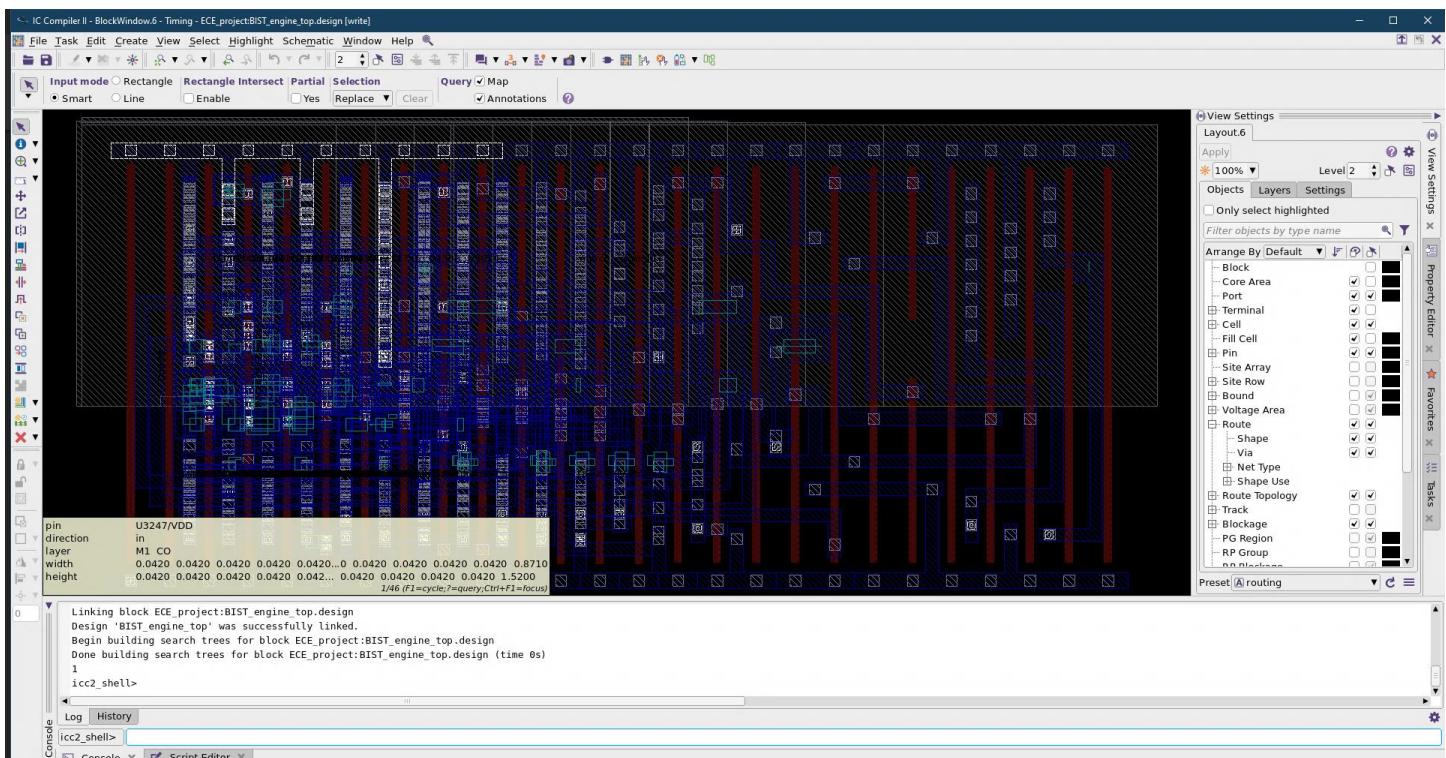


Report 17 PrimeTime Max Delays 2.2ns

*File/Report included in zip.

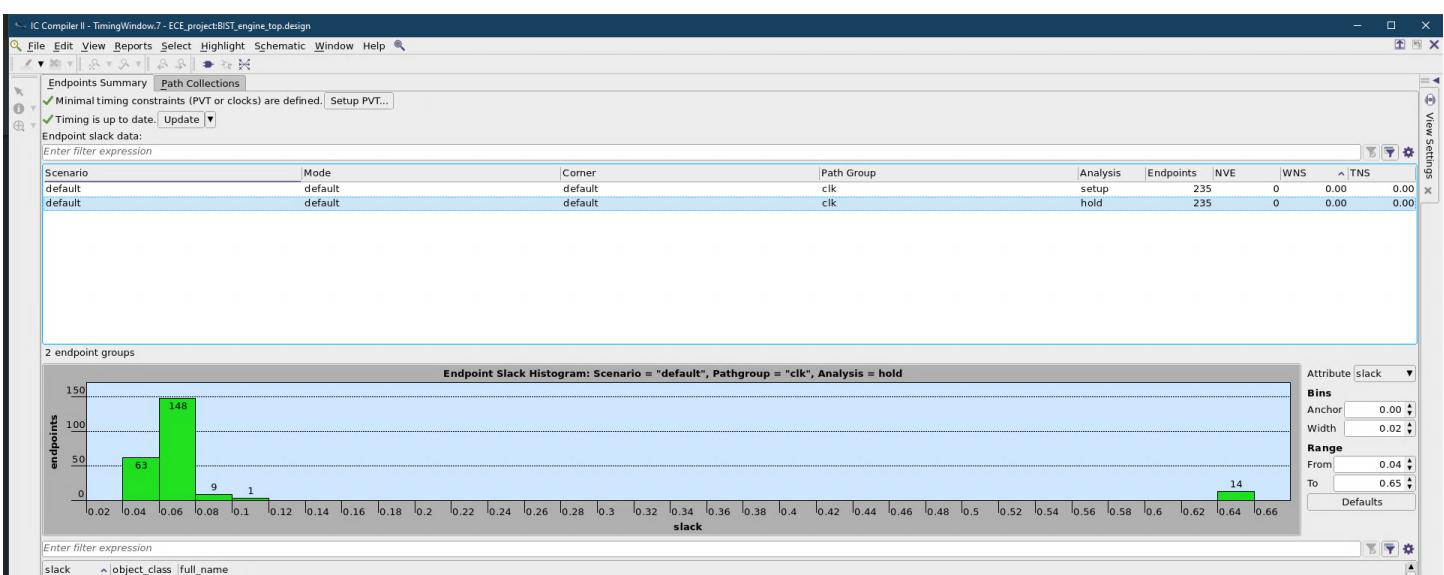
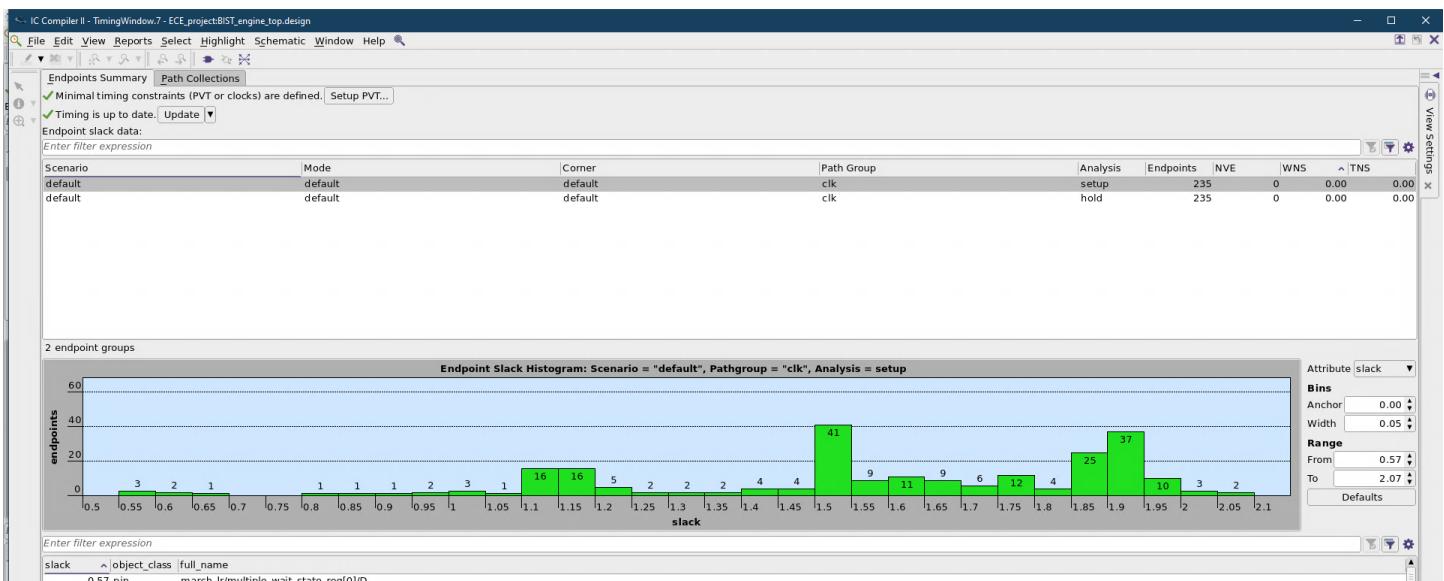


Report 18 Primetime Min Delays 2.2ns



Schematic 26 ICC2 Generated Layout

*File/Report included in zip.



*File/Report included in zip.