

Lab0: Icarus Verilog Installation Tutorial



Download under Windows system

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ICARUS VERILOG

Icarus Verilog for Windows

Icarus Verilog is a free compiler implementation for the IEEE-1364 Verilog hardware description language. Icarus is maintained by Stephen Williams and it is released under the [GNU GPL license](#).

In this page you will find easy to install Icarus Verilog packages compiled with the [MinGW](#) toolchain for the Windows environment. [GTKWave for Win32](#) is also included in the latest releases. The installers have been created with Jordan Russell's [Inno Setup](#) free installer utility.

Download

You can find Icarus Verilog sources and binaries for most platforms at the [Icarus site FTP](#). The sources available here have been compressed with 7-zip.

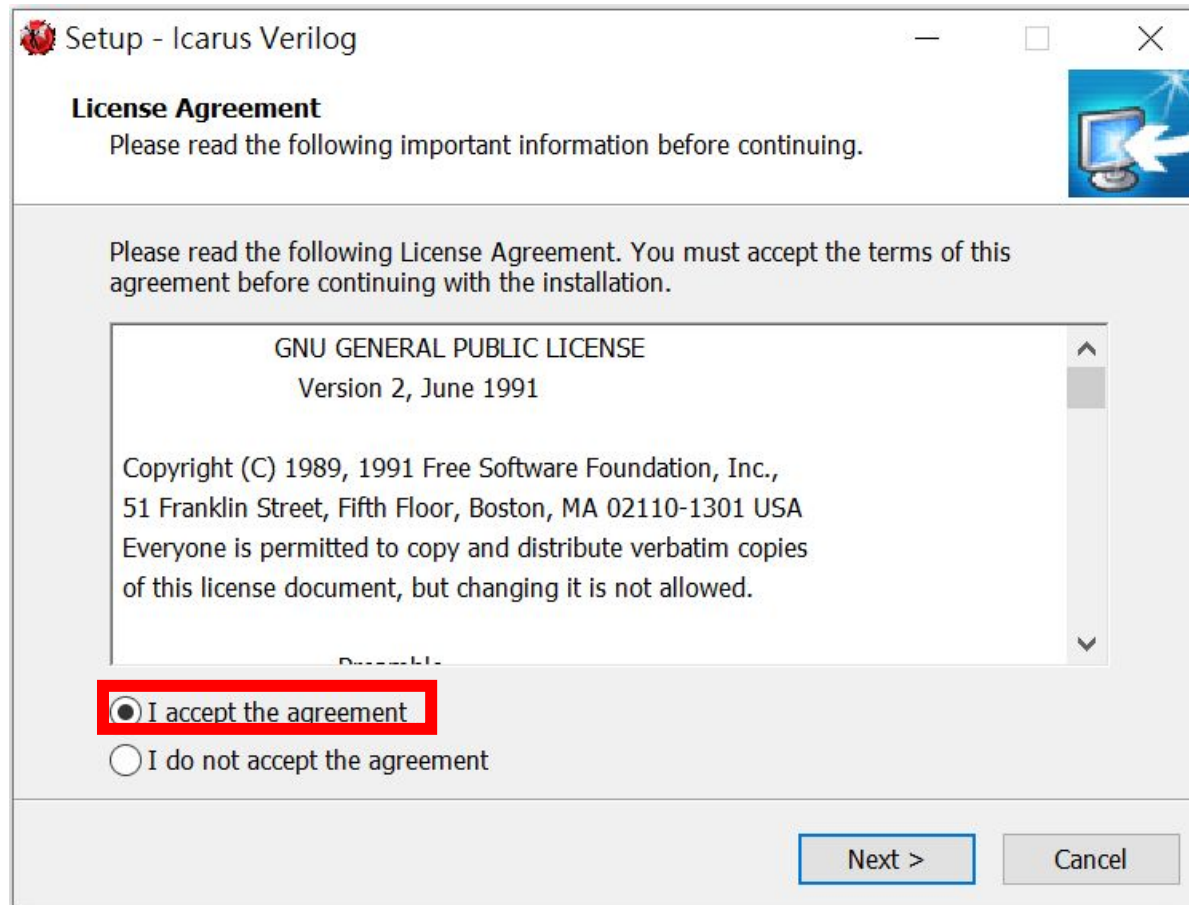
- iverilog-v12-20220611-x64_setup [18.2MB]
- iverilog-v11-20210204-x64_setup.exe [44.1MB]
- iverilog-10.1.1-x64_setup.exe [9.77MB]
- iverilog-10.0-x86_setup.exe [11.1MB]
- iverilog-10.0-x86_setup.exe (development snapshot) [11.2MB]
- iverilog-0.9.7_setup.exe (latest stable release) [10.5MB]
- iverilog-0.9.6_setup.exe [10.4MB]
- iverilog-0.8.6_setup.exe (latest release 0.8 series) [1.29MB] iverilog-0.8.6.7z [800kB]
- iverilog-0.7-20040706_setup.exe [1.09MB] iverilog-0.7-20040706.7z [588kB]

Download: <https://bleyer.org/icarus/>

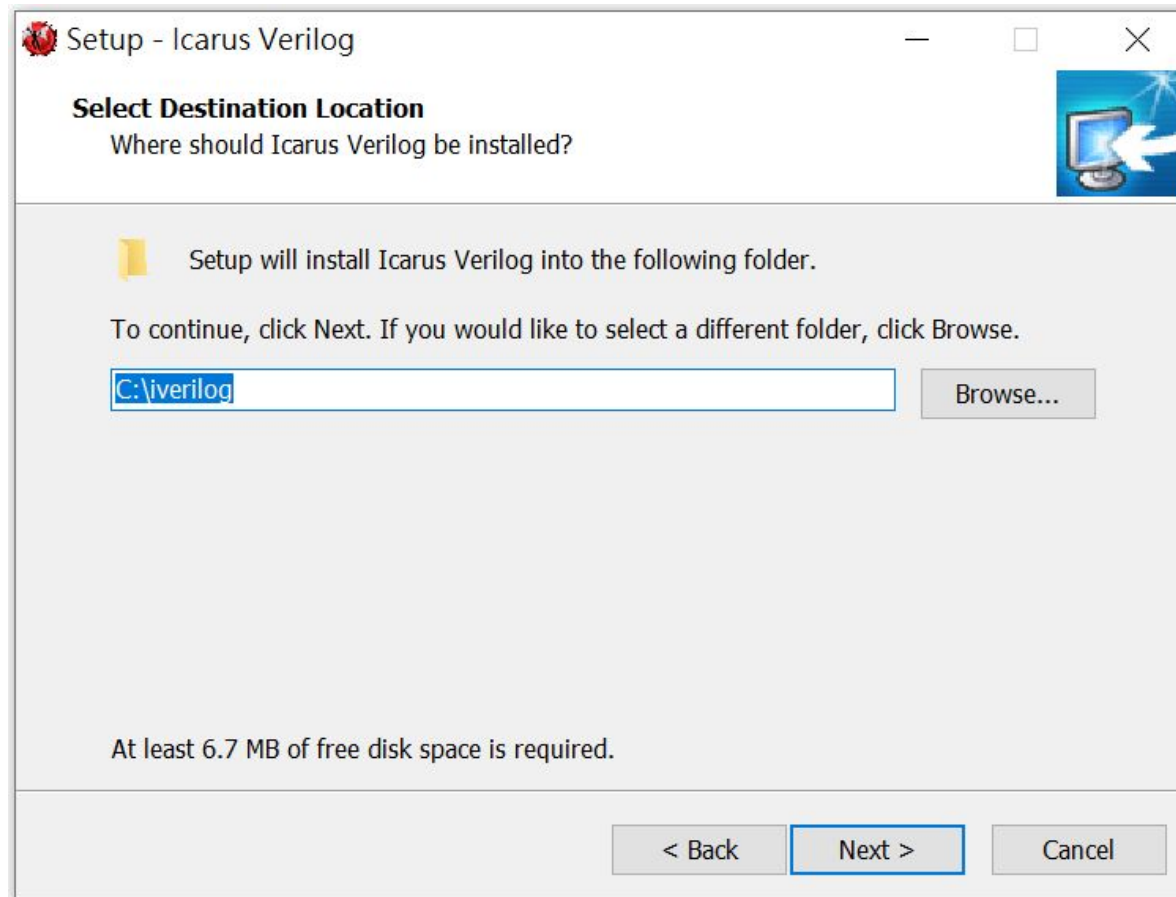
64 bit : iverilog-10.1.1-x64_setup.exe [9.77MB]

32 bit : iverilog-10.0-x86_setup.exe [11.1MB]

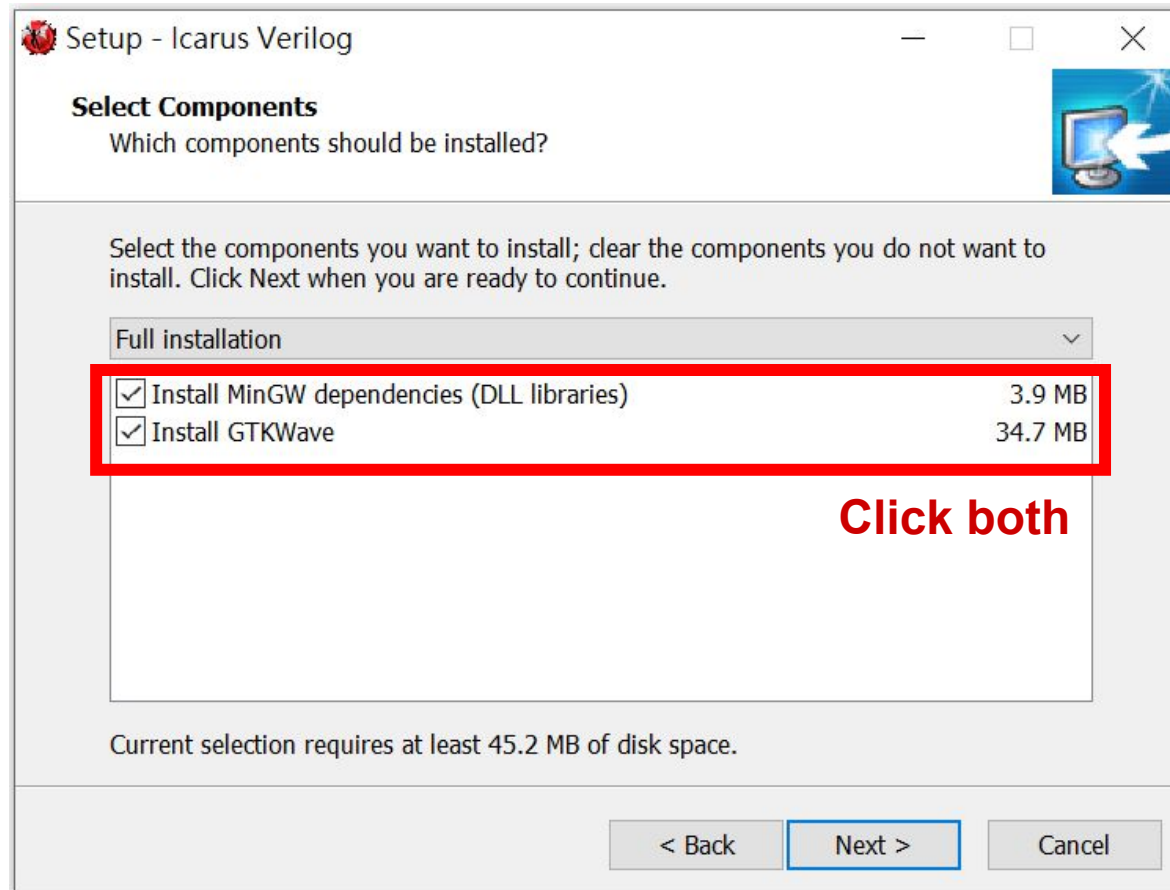
Installation



Installation



Installation



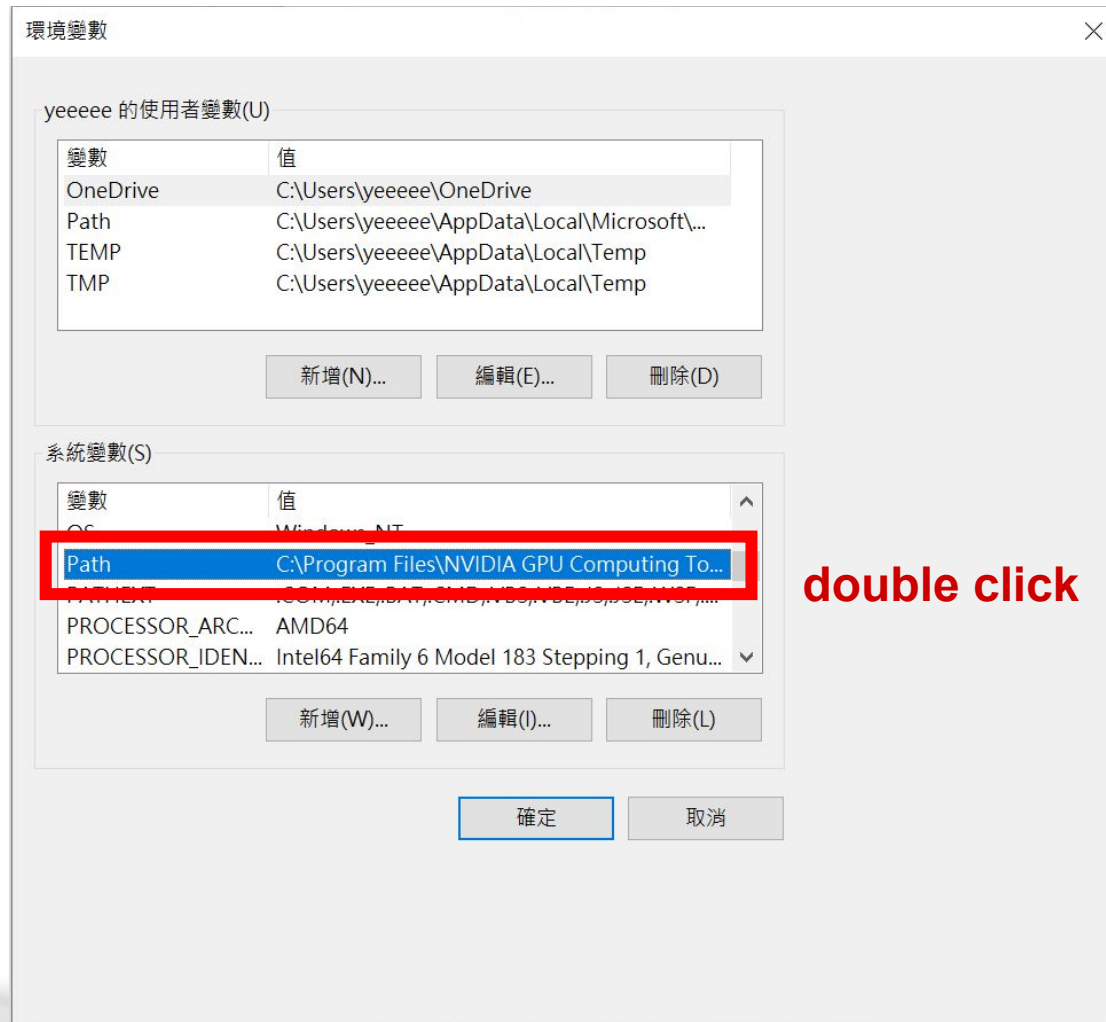
Add Environment Variable



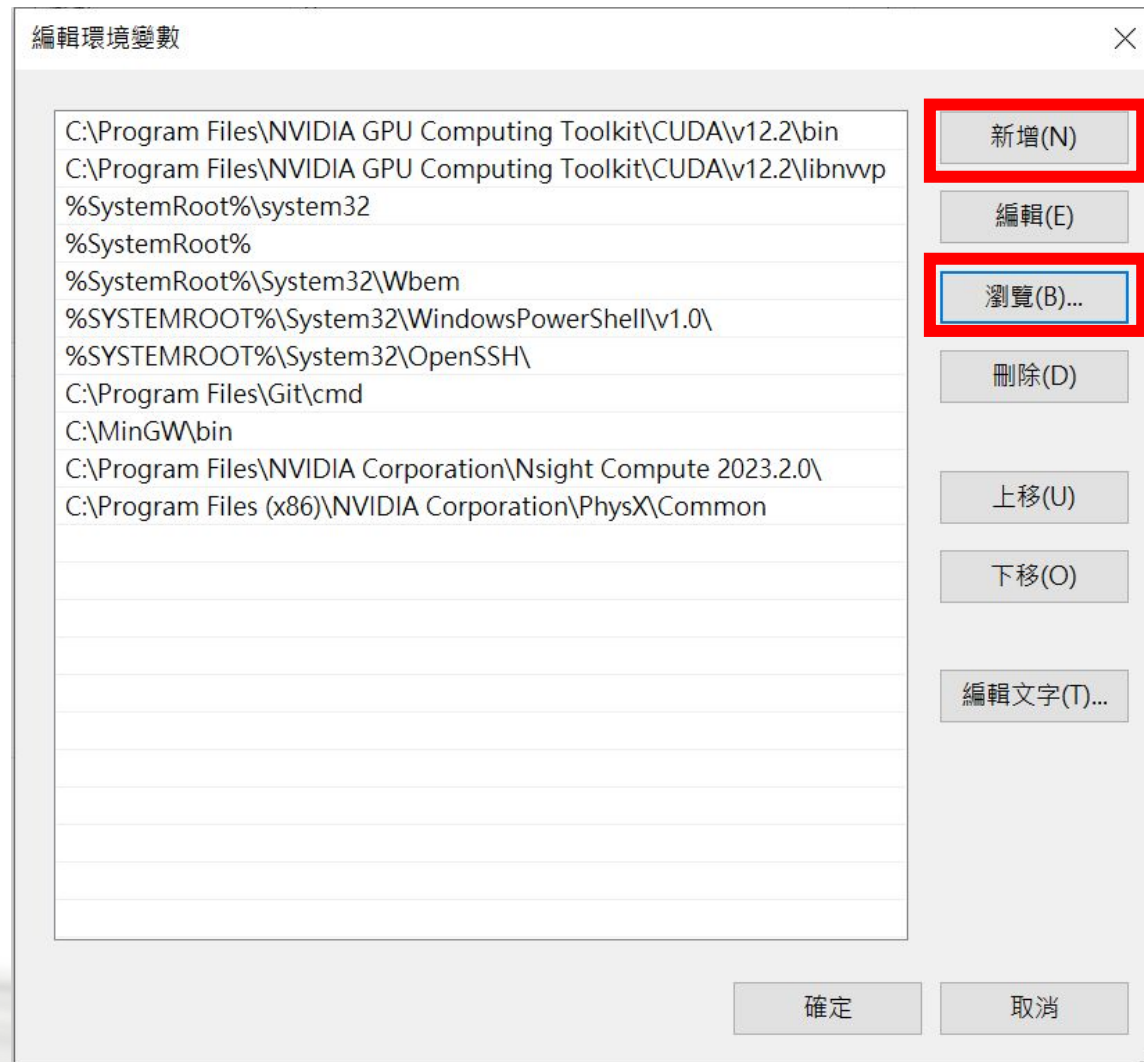
控制台 \ 系統及安全性 \ 系統 \ 進階系統
設定 \ 系統內容

Control Panel \ System and Security \
System \ Advanced system settings \
System Properties

Add Environment Variable



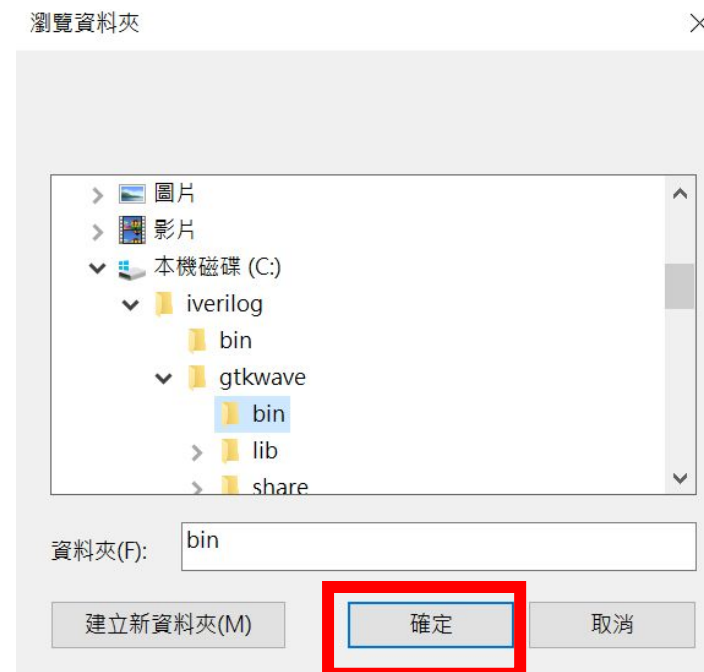
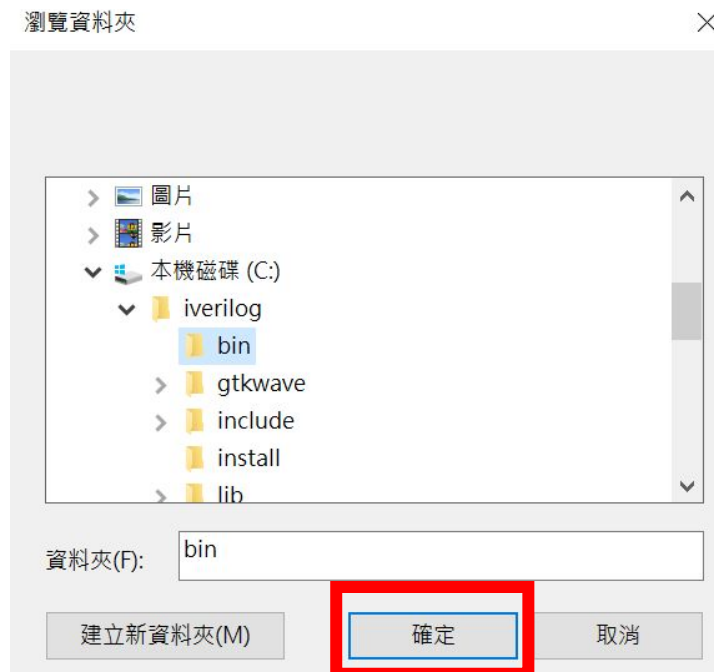
Add Environment Variable



Step 1

Step 2

Add Environment Variable



Add **two** paths!(“iverilog/bin” & “iverilog/gtkwave/bin”)

Add Environment Variable

編輯環境變數



C:\Program Files\NVIDIA GPU Computing Toolkit\CUDA\v12.2\bin
C:\Program Files\NVIDIA GPU Computing Toolkit\CUDA\v12.2\libnvp
%SystemRoot%\system32
%SystemRoot%
%SystemRoot%\System32\Wbem
%SYSTEMROOT%\System32\WindowsPowerShell\v1.0\
%SYSTEMROOT%\System32\OpenSSH\
C:\Program Files\Git\cmd
C:\MinGW\bin
C:\Program Files\NVIDIA Corporation\Nsight Compute 2023.2.0\
C:\Program Files (x86)\NVIDIA Corporation\PhysX\Common
C:\iverilog\bin
C:\iverilog\gtkwave\bin

新增(N)

編輯(E)

瀏覽(B)...

刪除(D)

上移(U)

下移(O)

編輯文字(T)...

確定

取消

After clicking OK, **restart the computer!**



Download under MacOS system

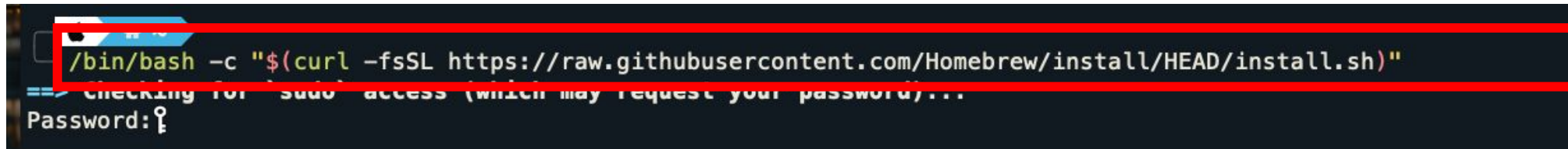
Open terminal



Download Iverilog

Install Homebrew

```
/bin/bash -c "$(curl -fsSL  
https://raw.githubusercontent.com/Homebrew/install/HEAD/install.sh)"
```

A terminal window with a dark background. The command `/bin/bash -c "$(curl -fsSL https://raw.githubusercontent.com/Homebrew/install/HEAD/install.sh)"` is entered and highlighted with a red rectangular box. Below the command, the text `==> Checking for 'sudo' access (which may request your password)...` is visible. At the bottom, the prompt `Password: ?` is shown, with a cursor at the end of the question mark.

```
/bin/bash -c "$(curl -fsSL https://raw.githubusercontent.com/Homebrew/install/HEAD/install.sh)"  
==> Checking for 'sudo' access (which may request your password)...  
Password: ?
```


Download Iverilog

Install icarus-Verilog

brew install icarus-Verilog

```
└─ brew install icarus-Verilog
warning: icarus-verilog 12.0 is already installed and up-to-date.
To reinstall 12.0, run:
  brew reinstall icarus-verilog

└─ which iverilog
/opt/homebrew/bin/iverilog
```

Version Error

若安裝過程遇到 CLT (CommandLineTools) 版本過舊的問題, 可以執行下面兩條指令解決

```
sudo rm -rf /Library/Developer/CommandLineTools
```

```
# 刪除原有的 CLT (delete own CLT)
```

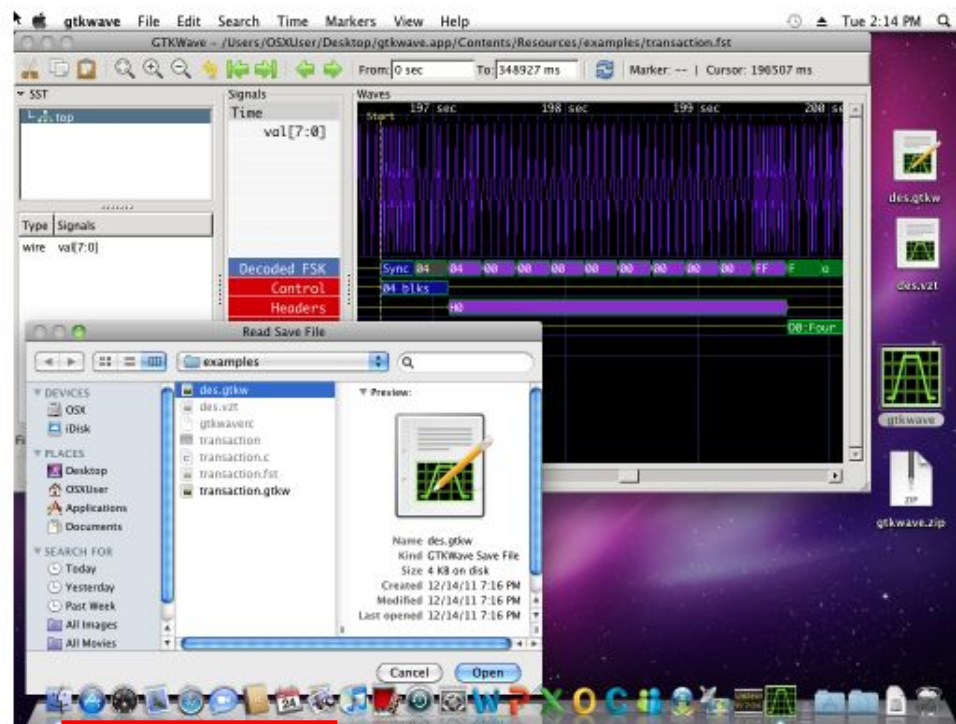
```
sudo xcode-select --install
```

```
# 安裝新的 CLT (Install new CLT)
```

```
Error: Your CLT does not support macOS 11.2.  
It is either outdated or was modified.  
Please update your CLT or delete it if no updates are available.
```

Download gtkwave

Download here: <http://gtkwave.sourceforge.net/>



Simply download, unzip, and it is ready to run on the Mac...

Download gtkwave

解壓縮 gtkwave.zip, 會看到應用程式 gtkwave



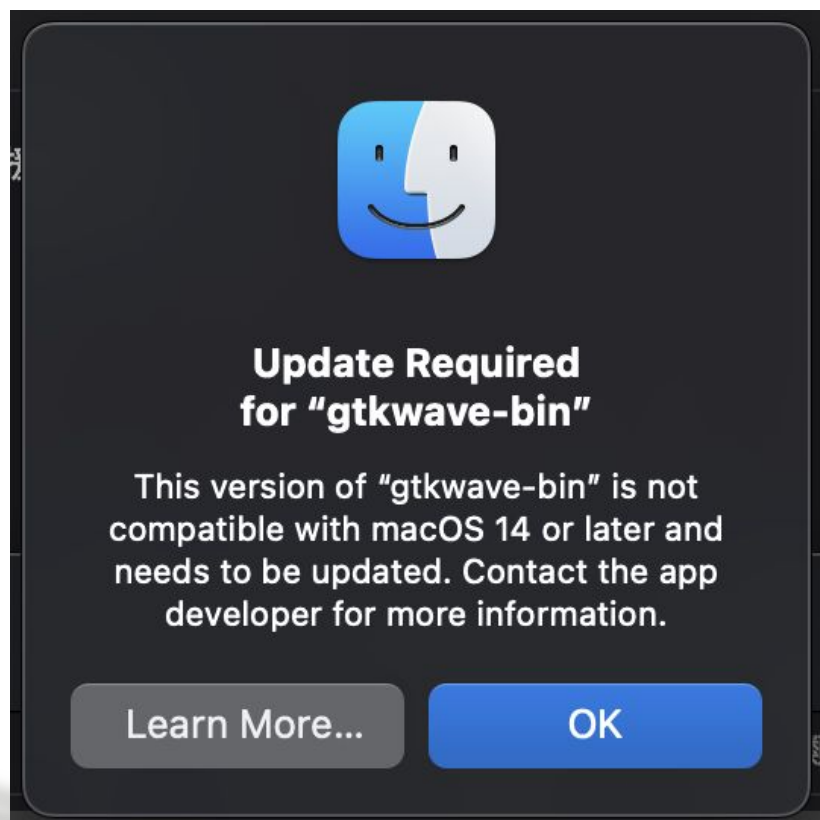
Download gtkwave

接著會跳出警告視窗，點選打開
Click open on the warning window



注意

如果你的 Mac OS version ≥ 14 請使用下面的使令
`brew install --HEAD randomplum/gtkwave/gtkwave`





Compile and Observe the waveform

Compile Verilog code and run

```
命令提示字元 - gtkwave t_Simple_Circuit.vcd
Microsoft Windows [版本 10.0.18363.1379]
(c) 2019 Microsoft Corporation. 著作權所有，並保留一切權利。

C:\Users\user>cd C:\Users\user\Desktop\助教課程\數位電路設計\Lab0

C:\Users\user\Desktop\助教課程\數位電路設計\Lab0>iverilog -o t_Simple_Circuit.vvp t_Simple_Circuit.v Simple_Circuit.v

C:\Users\user\Desktop\助教課程\數位電路設計\Lab0>vvp t_Simple_Circuit.vvp
VCD info: dumpfile t_Simple_Circuit.vcd opened for output.

C:\Users\user\Desktop\助教課程\數位電路設計\Lab0>gtkwave t_Simple_Circuit.vcd

GTKWave Analyzer v3.3.71 (w)1999-2016 BSI

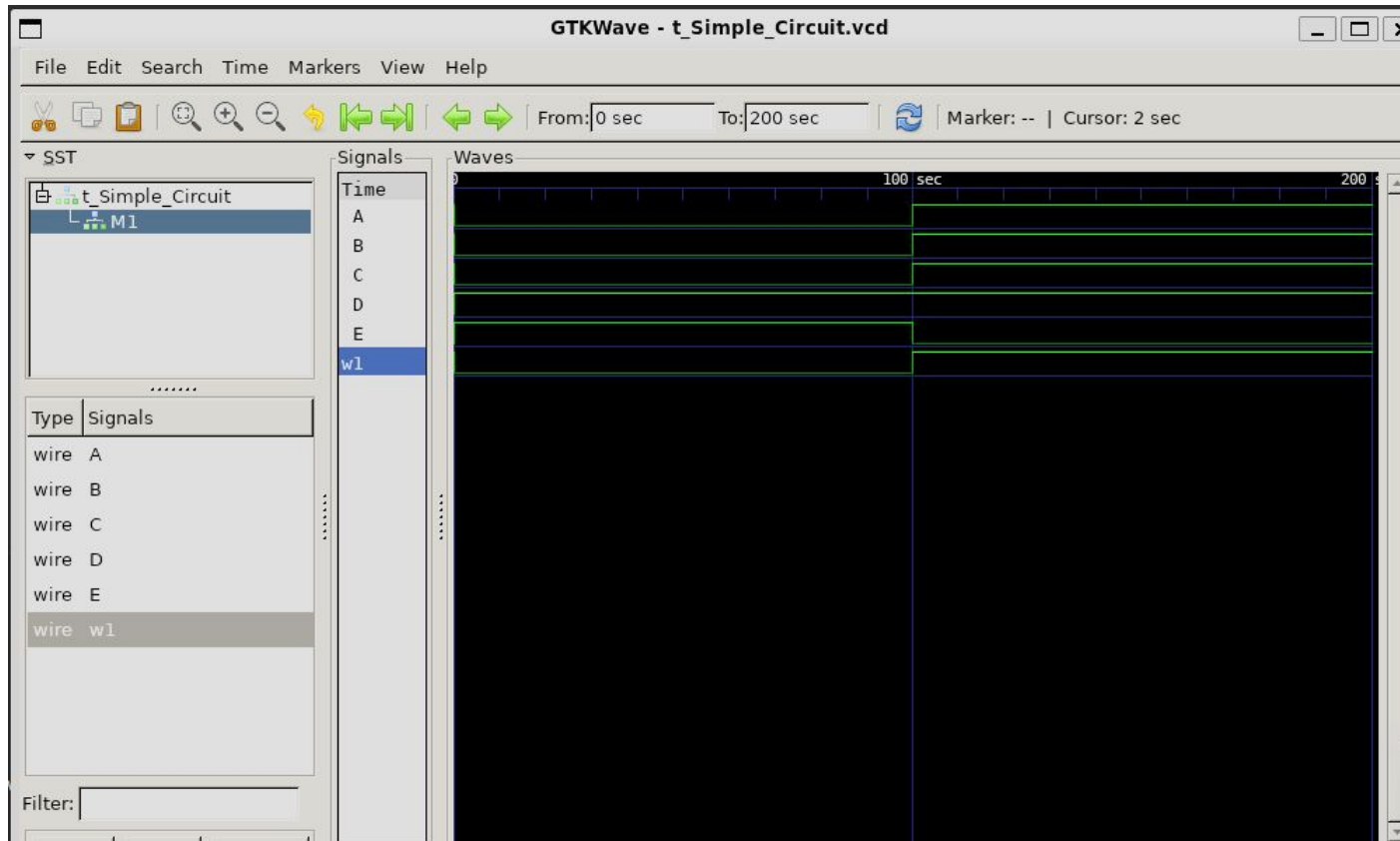
[0] start time.
[200] end time.
```

1. Download files provided on E3 (Simple_Circuit.v & t_Simple_Circuit.v)
2. Open Command Prompt (終端機)
3. Use cd [path] to reach the Simple_Circuit.v and t_Simple_Circuit.v folders.

Compile Verilog code and run

- iverilog -o t_Simple_Circuit.vvp t_Simple_Circuit.v Simple_Circuit.v
 - ◆ iverilog: 編譯 verilog 和 vhd1 檔, 進行語法檢查, 生成可執行檔
- vvp t_Simple_Circuit.vvp
 - ◆ vvp: 根據可執行檔, 生成模擬波形文件
- gtkwave t_Simple_Circuit.vcd
 - ◆ gtkwave: 用於打開模擬波形檔, 圖形化顯示波形

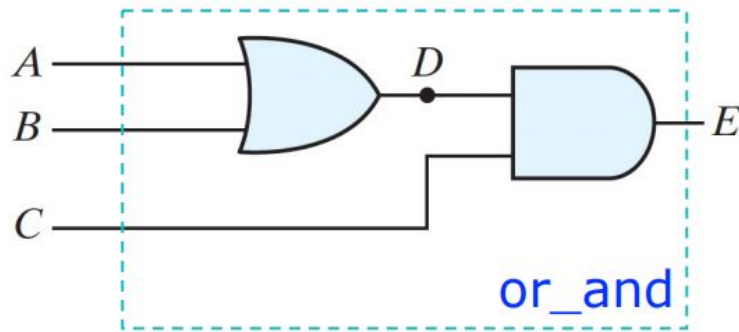
Observe the waveform



1. Click  next to Simple_Circuit and click M1
2. Drag variables below to the Signals section

Sample Assignment

Verilog Example 3.1: $E = (A + B) C$



A	B	C	D	E
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1

Edit module and testbench

```
1 module or_and(  
2     output E,  
3     input A,B,C  
4 );  
5     wire D;  
6     assign D = A||B;  
7     assign E = C&&D;  
8 endmodule
```

Use any text editor to finish
your module and testbench.
(E.g. notepad++、VSCode...)

```
1 module or_and_tb;  
2     reg A,B,C;  
3     wire E;  
4  
5     or_and M1(.E(E),  
6         .A(A),  
7         .B(B),  
8         .C(C));  
9  
10    initial begin  
11        $dumpfile("wave.vcd");  
12        $dumpvars(0, or_and_tb);  
13    end  
14  
15    initial begin  
16        #10 A=1'b0;B=1'b0;C=1'b0;  
17        #20 A=1'b0;B=1'b0;C=1'b1;  
18        #20 A=1'b0;B=1'b1;C=1'b0;  
19        #20 A=1'b0;B=1'b1;C=1'b1;  
20        #20 A=1'b1;B=1'b0;C=1'b0;  
21        #20 A=1'b1;B=1'b0;C=1'b1;  
22        #20 A=1'b1;B=1'b1;C=1'b0;  
23        #20 A=1'b1;B=1'b1;C=1'b1;  
24        #20 $finish;  
25    end  
26 endmodule
```

iverilog 編譯器專用語句

References

- [Icarus Verilog 官方網站](#)
- [Icarus Verilog User Guide](#)

