Tutorial 5
Quiz solution

COMP2120B Computer organization

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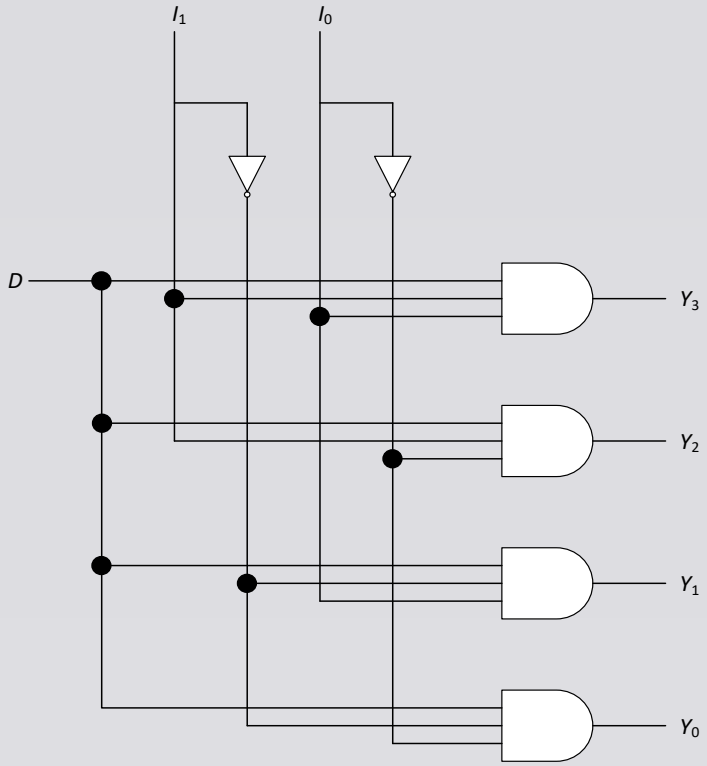
Q1a

- Complete the following truth table for a 1-to-4 demultiplexer.

D	I1	I0	Y3	Y2	Y1	Y0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

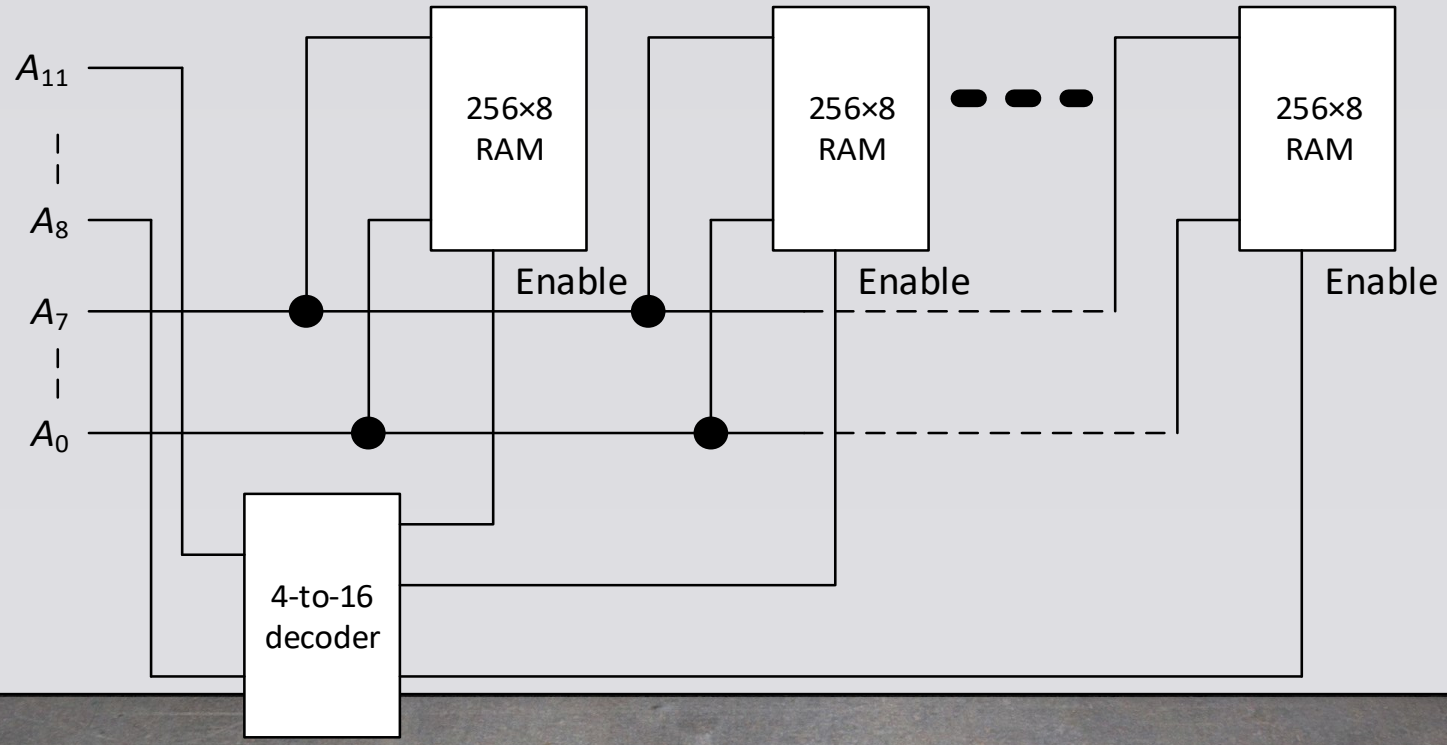
Q1b

- Draw a logic circuit for the 1-to-4 demultiplexer in (a).



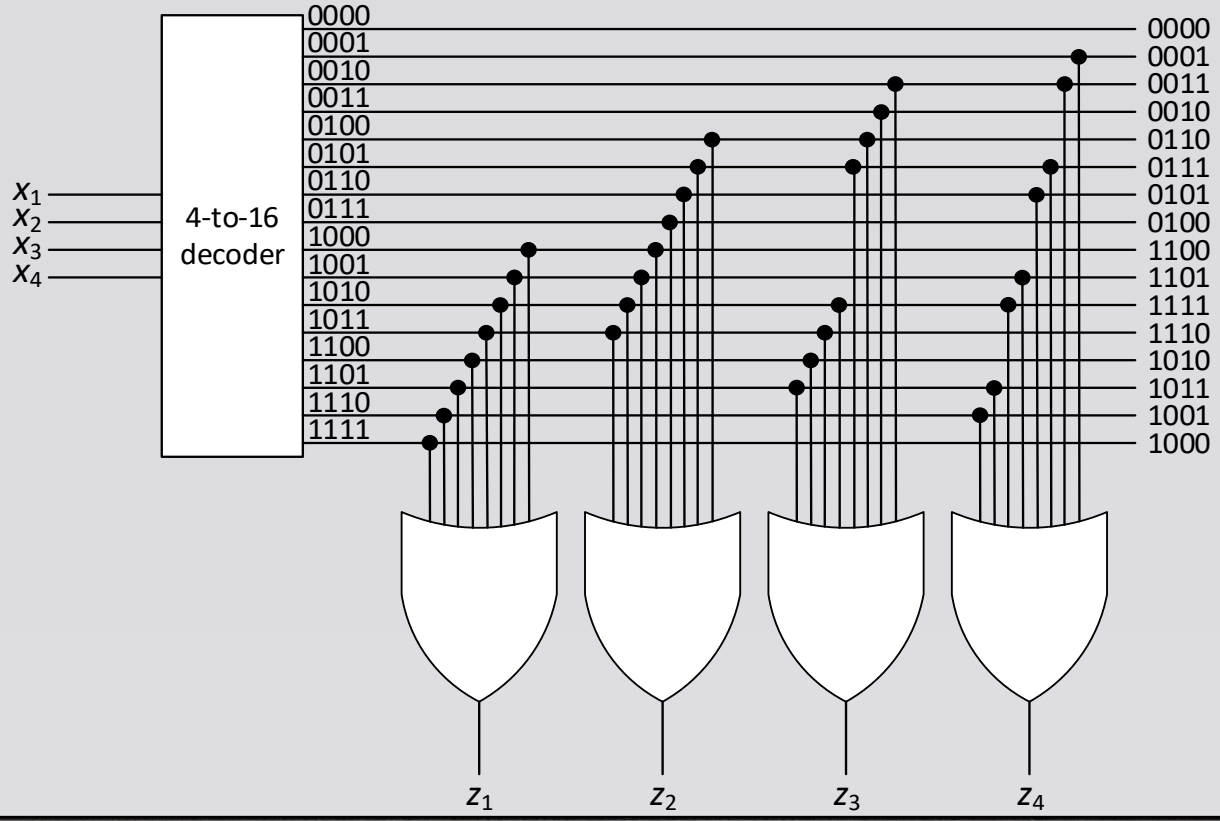
Q1c

- Illustrate how we can use 4-to-16 decoder to construct 4K-byte memory using sixteen 256 x 8 bit RAM chips.



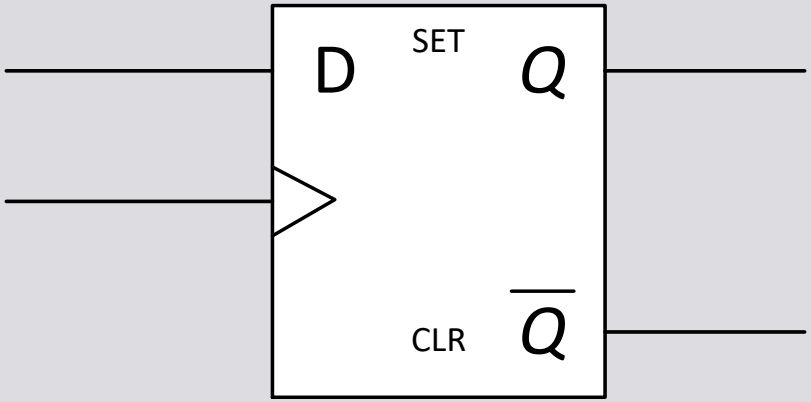
Q1d

- Illustrate how we can use 4-to-16 decoder to construct a 64 bit ROM



Q2a

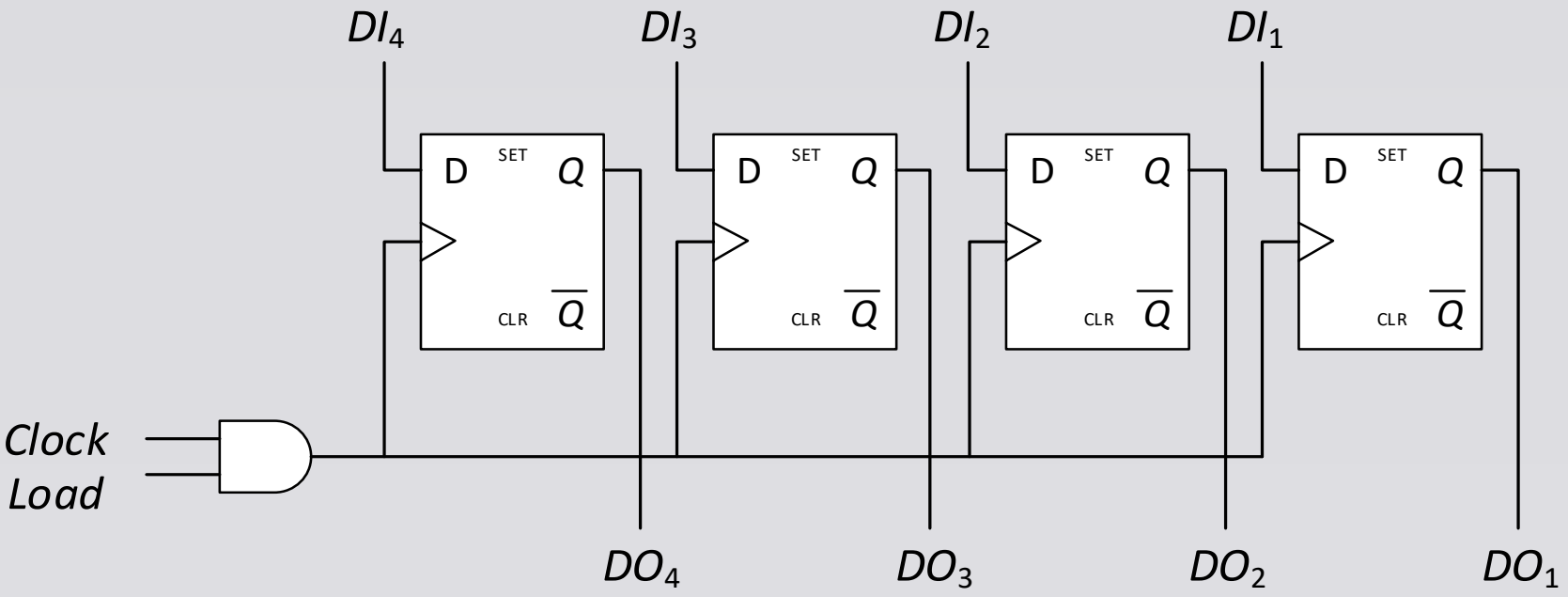
- Write down the Truth Table of a clocked D Flip-Flop.



D	Q_{n+1}
0	0
1	1

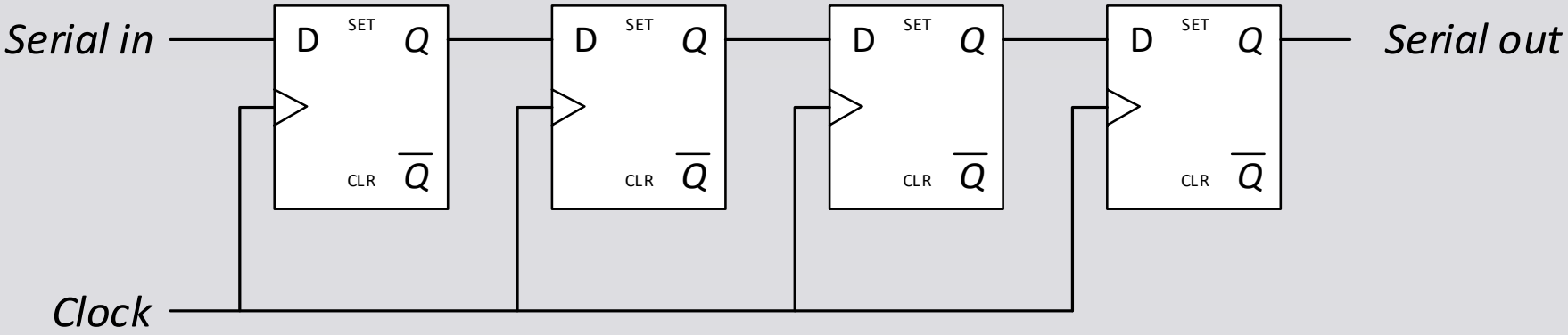
Q2b

- Draw a diagram to illustrate how to use clocked D Flip-Flops to realise 4-bit Parallel Register.



Q2c

- Draw a diagram to illustrate how to use clocked D Flip-Flops to realise 4-bit Shift Register.



Q2d

- Explain the operation differences between the two registers presented in (b) and (c).

	Parallel Register	Serial Register
Transfer of Data Bits	Parallel	Serial/sequential
Clock Cycles to Fetch/Store Bytes	1	Equals to number of bits of the register
Tolerance to interference	More Cross Talk	Less Cross Talk
Transmission Distance	Shorter	Longer