Prelab5

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1.
Design Specification

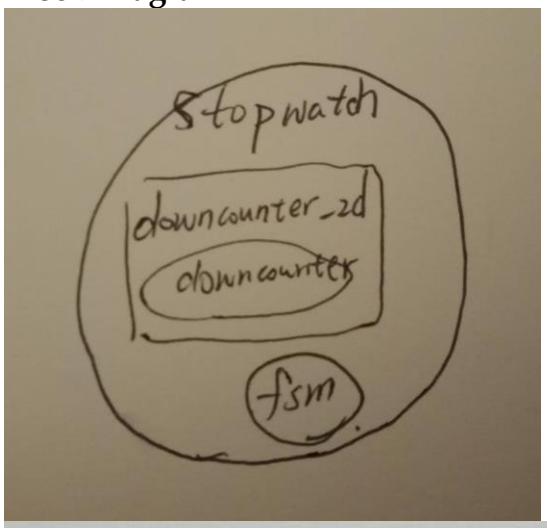
- ✓ **Input / Output**

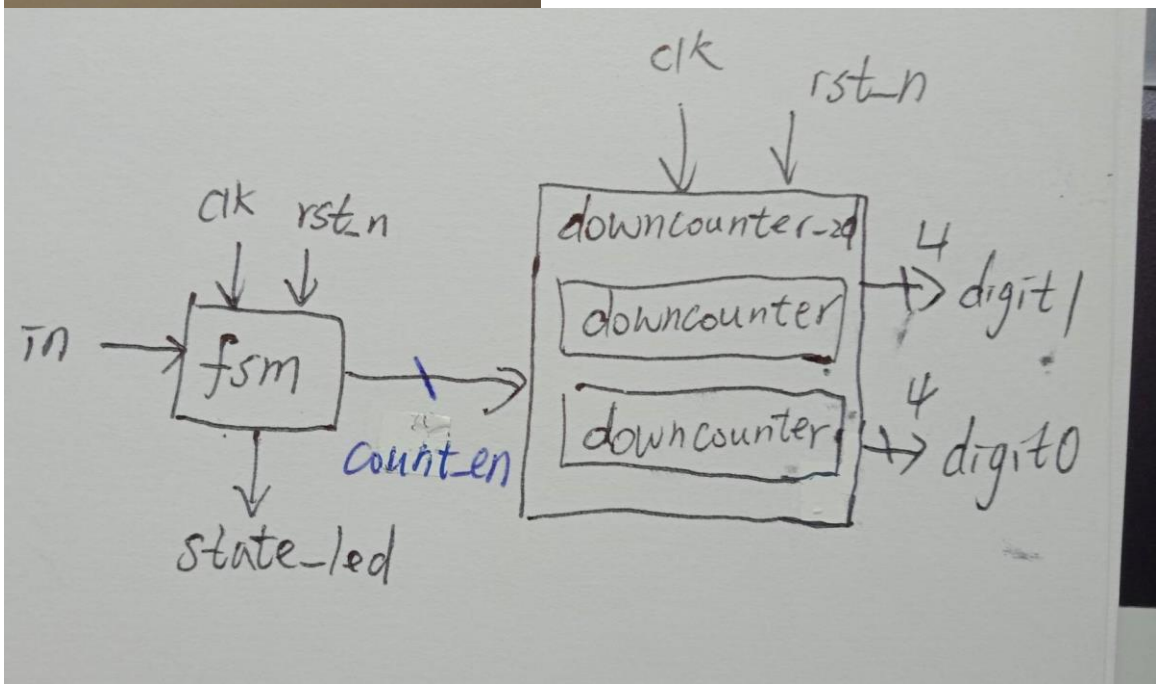
  For a 4-bit synchronous binary up counter:

  input :clk, rst_n, in,

  output: [3:0]digit0, [3:0]digit1, state_led, [14:0]led

- ✓ **Block Diagram**





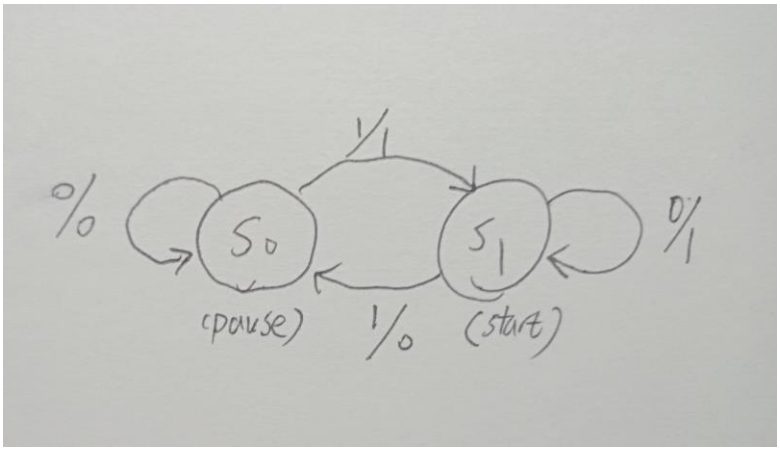
Design Implementation

✓ Function descriptions

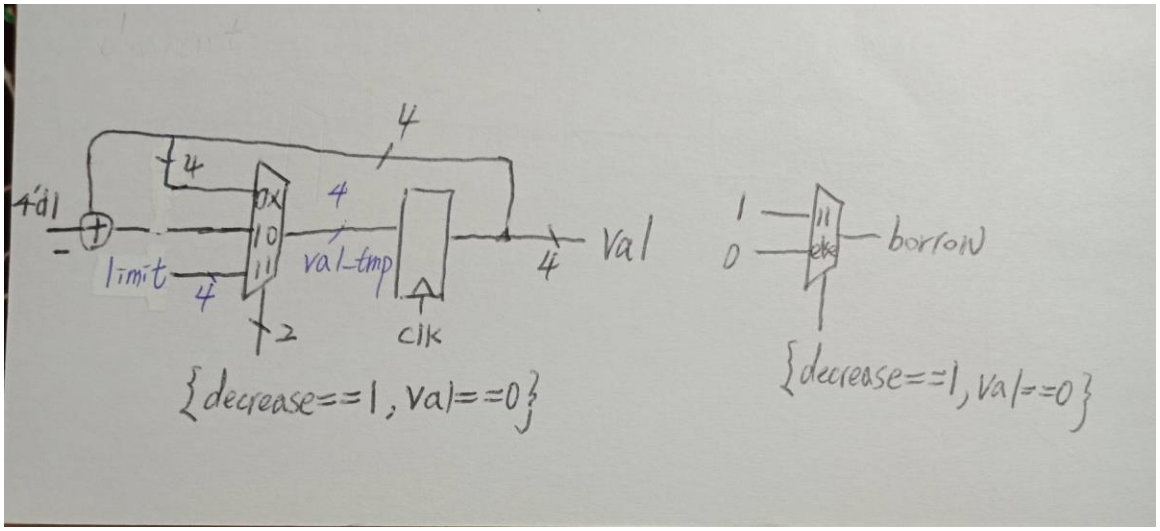
此功能為一個從 30 數到 0(此時 led 全亮)的倒數計時器，並設有暫停開始的功能。因為為 simulation 而已，並不需要除頻器與 debounce, one pulse 跟 display 的功能，這裡只有 finite state machine 跟 downcounter。Push button 的 in 輸進 fsm 裡，fsm 裡有 mux 來做選擇。若現在是 pause 的狀態，in = 1 就讓他開始數(輸入 count_en = 1 到 downcounter)若現在是 start 狀態，in = 1 就讓她暫停(輸入 count_en =0 到 downcounter) 其他種都是狀態維持不改變。輸入的 count_en 會進到 downcounter 的 decrease 當作要不要減的判斷。Downcounter 的作法在前面的實驗已提及。

✓ Logic Diagram

- **fsm**



- **downcounter**



✓ **Logic Functions**

```
if (digit0==4'd0&&digit1==4'd0)
    {led, state_led} = 16'b1111111111111111;
else
    state_led = state;
    led = 15'b000_0000_0000_0000;
```

✓ **Simulation**