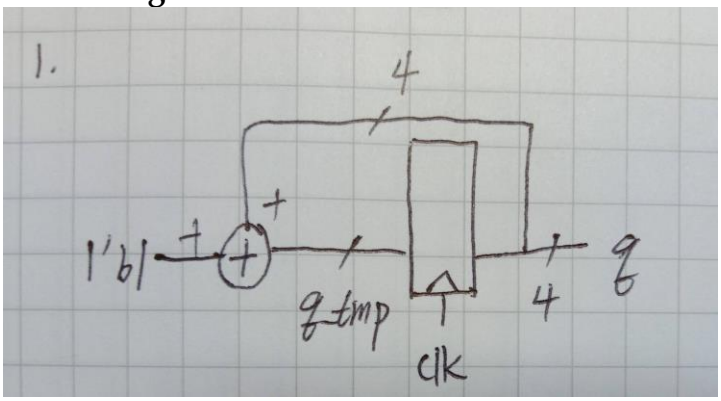
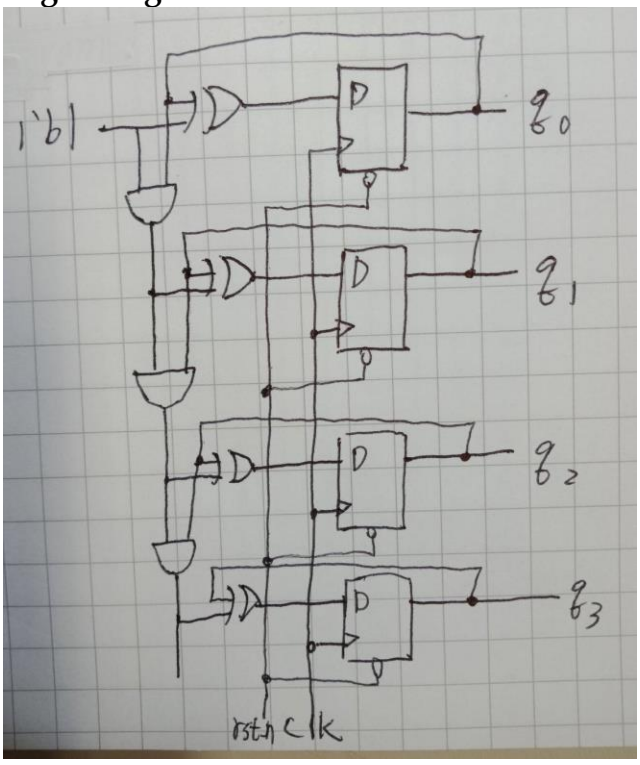
1.
Design Specification

- ✓ **Input / Output**
  For a 4-bit synchronous binary up counter:
  Input: clk, rst_n.
  Output: q[3:0].
- ✓ **Block Diagram**

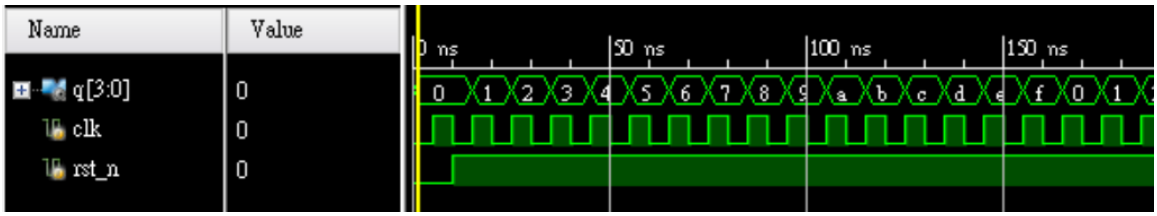


Design Implementation

- ✓ **Logic Diagram**



✓ **Simulation**



2.

Design Specification

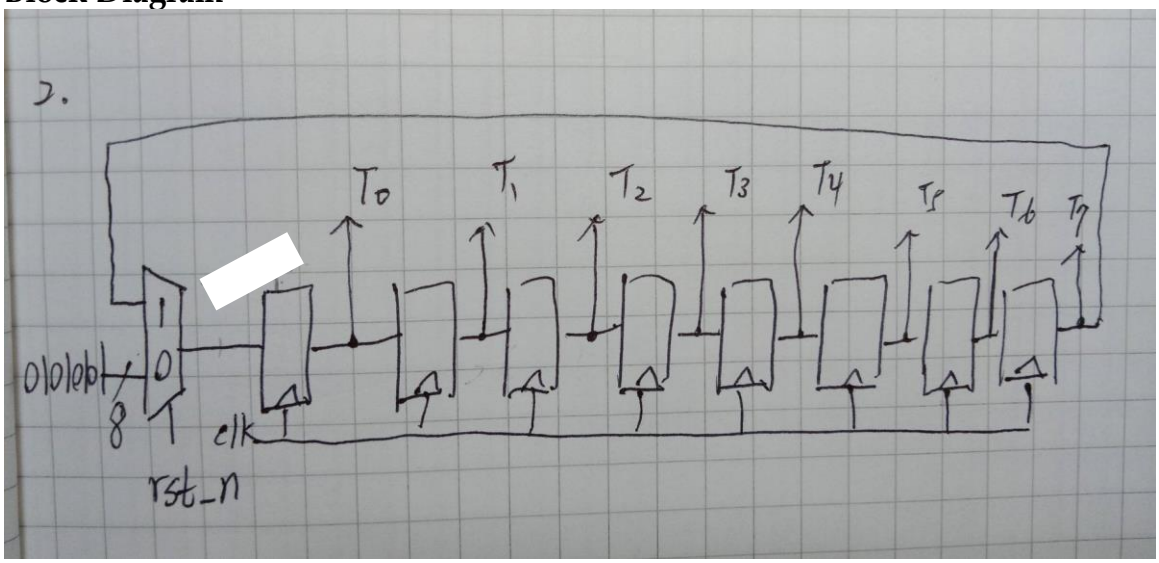
✓ **Input / Output**

For a ringer counter of 8 DFFs:

Input: clk, rst_n.

Output: T[7:0].

✓ **Block Diagram**



Design Implementation

✓ **Simulation**