Sequential Circuit Analysis

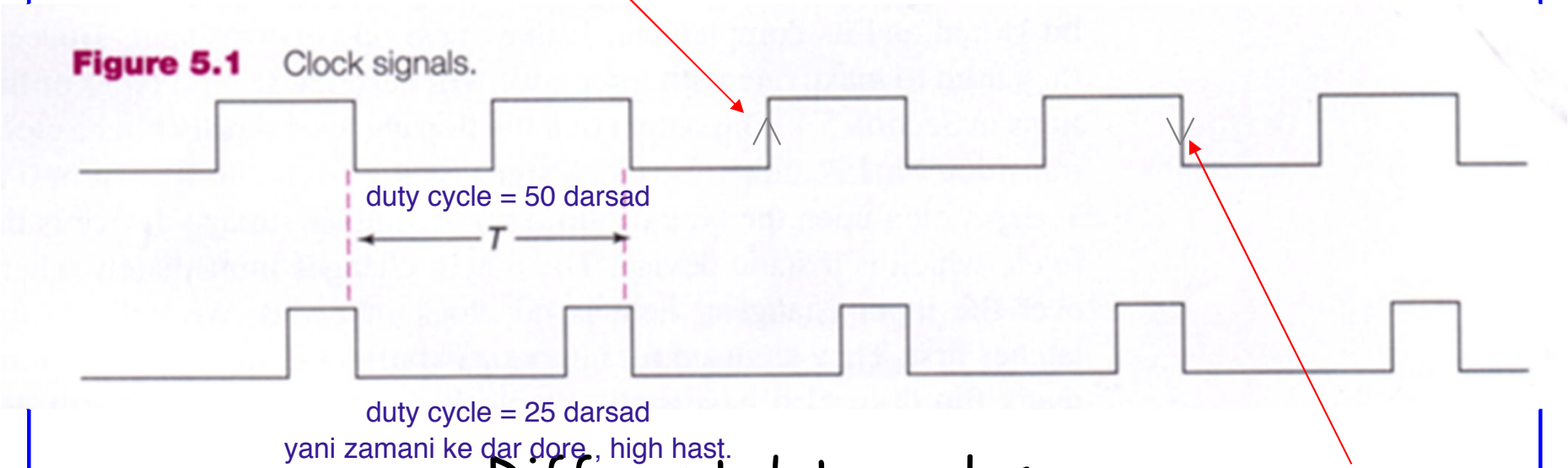
Synchronous vs. Asynch.

- **Synchronous sequential circuit:**
  - Its behavior can be determined knowing its input signals at discrete instants of time.
  - Achieves synchronization among components by using a timing signal called the *clock:*
    - Its outputs change synchronized with the clock
- **Asynchronous sequential circuit:**
  - Its behavior depends on the order of input signals changes over a continuous time
  - There is no need for synchronization:
    - No clock signal
    - Its outputs can change at **any** time

Clock Signal

Rising Clock Edge

Clock generator: Periodic train of clock pulses



Different duty cycles

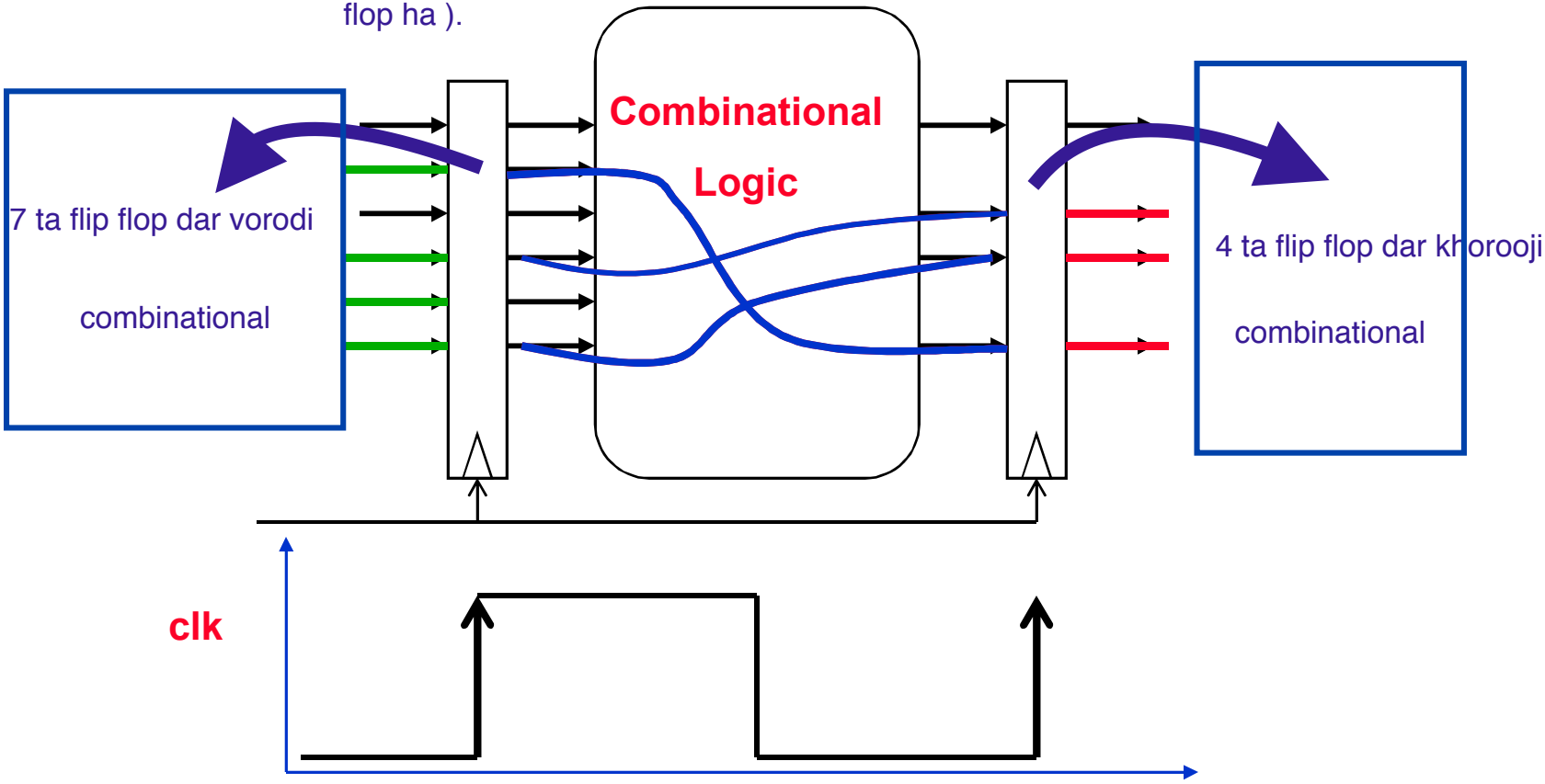
Falling Clock Edge

Clock Signal

- Clock is distributed throughout the entire design
- Each component synchronizes itself with it

Synchronous Circuits

yek madar sancron tashkil mishe az jazire haye combinational ke mahsoor shodan beine register ha (flip flop ha).

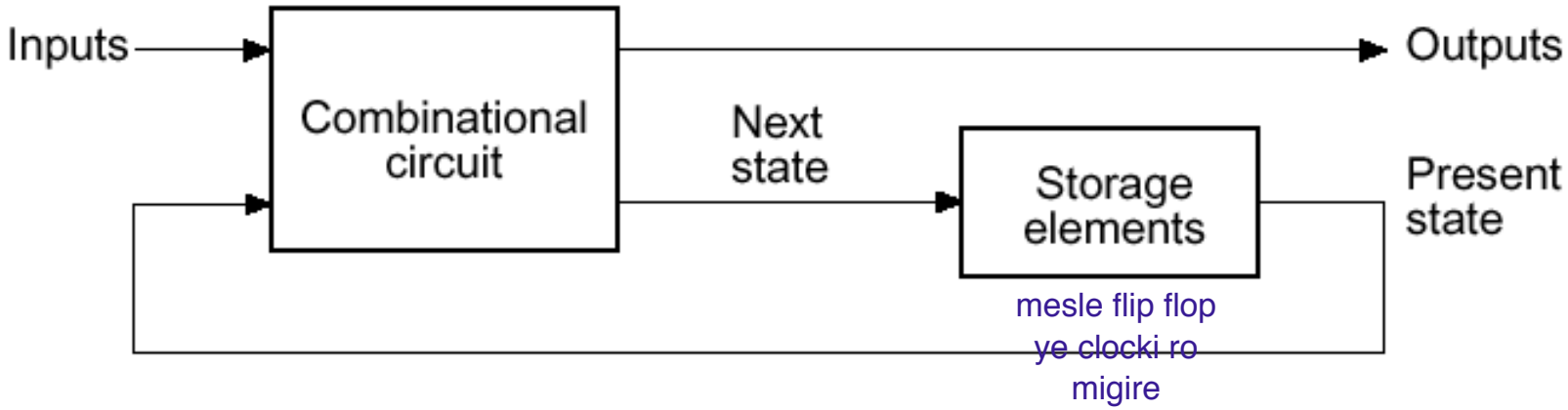


har etefaghi ma beyne clock ha biofte ma nemibinimesh , vaghti clock ha yek beshe , ma signal ro mibinim dar halate dge ma signale ghadimir ro mibinim .

Sequential Circuit Analysis

- **Analysis:**
  - Obtaining a suitable description that demonstrates the time sequence of inputs, outputs, and states

Sequential Circuits



- At each clock edge, the present state of the system is stored in storage elements (FFs)

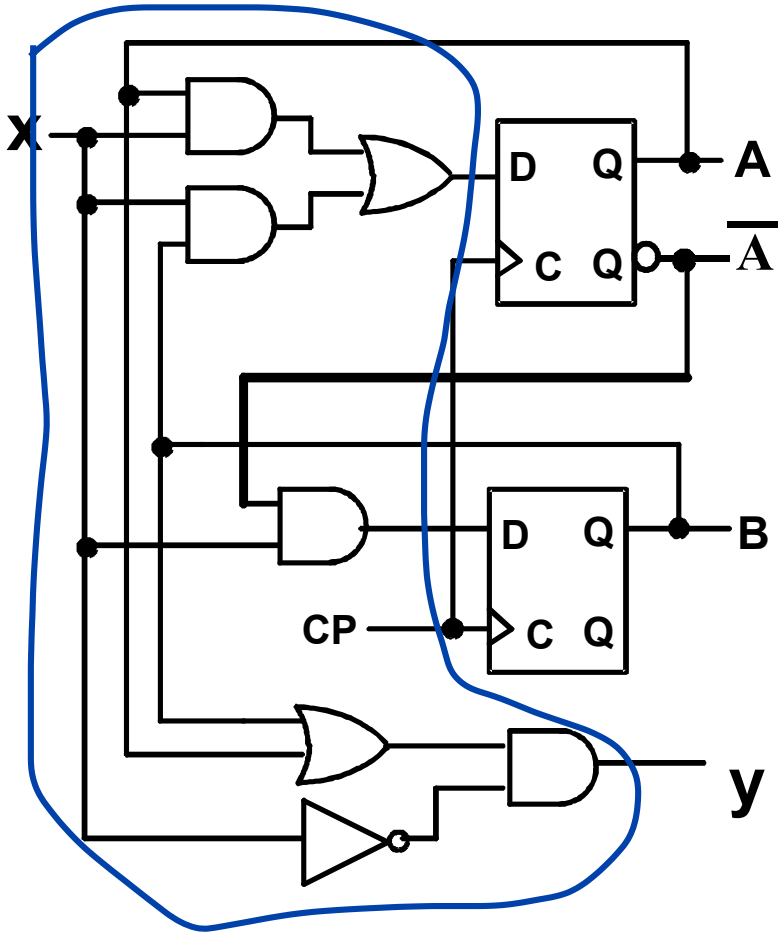
Example 1

ye seri vorodi va khoroji asli darim
va ye seri vorodi ham feedback ha hastan

- **Input:** x(t)
- **Output:** y(t)
- **State:** (A(t), B(t))

tedade state = 2 be tavane tedade flip flop ha , ke inja zoje moratabe

- **What is the Output Function?**
- **What is the Next State Function?**



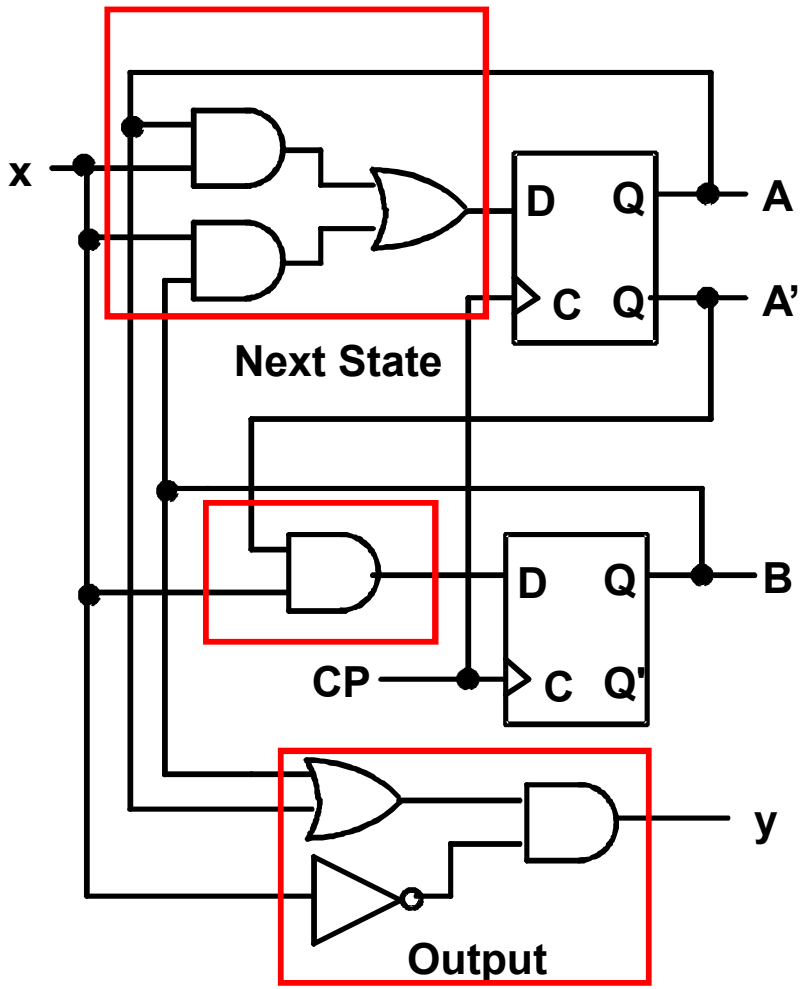
Example 1 (Cont'd)

- **Boolean equations for the functions:**

  - A(t+1) = A(t)x(t) + B(t)x(t)
  - B(t+1) = A'(t)x(t)
  - y(t) = x'(t) [B(t) + A(t)]

inja a va b t+1 hastan vali y t , chon
a va b khoroji haye ff hastan va ta clock nayad
taghiri nemidan .

tebghe shekle slide 7



State Table Definition

- ***State table***
  - A multiple variable table with the following four sections:
  - *Present State*
    - The values of the state variables for each allowed state
  - *Input*
    - The input combinations allowed
  - *Next-state*
    - The value of the state at time (t+1) based on the present state and the input
  - *Output*
    - The value of the output as a function of the present state and (sometimes) the input

State Table Characteristics

- **From the viewpoint of a truth table:**
  - The inputs: Input, Present State
  - The outputs: Output, Next State

State Table

- **Example:**
  - The state table can be filled in using the next state and output equations:

$A(t+1) = A(t)x(t) + B(t)x(t)$

$B(t+1) = \bar{A}(t)x(t)$

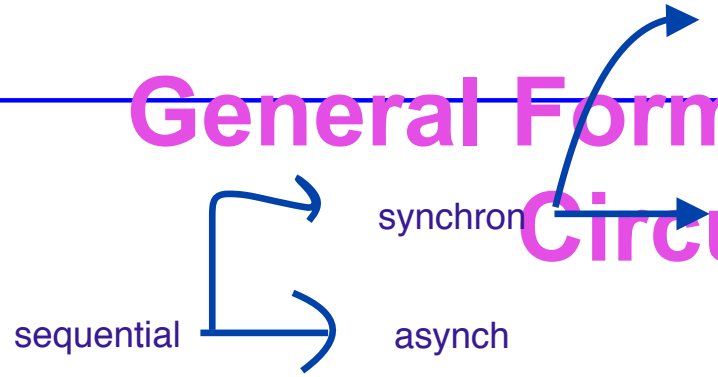
$y(t) = \bar{x}(t)[B(t) + A(t)]$

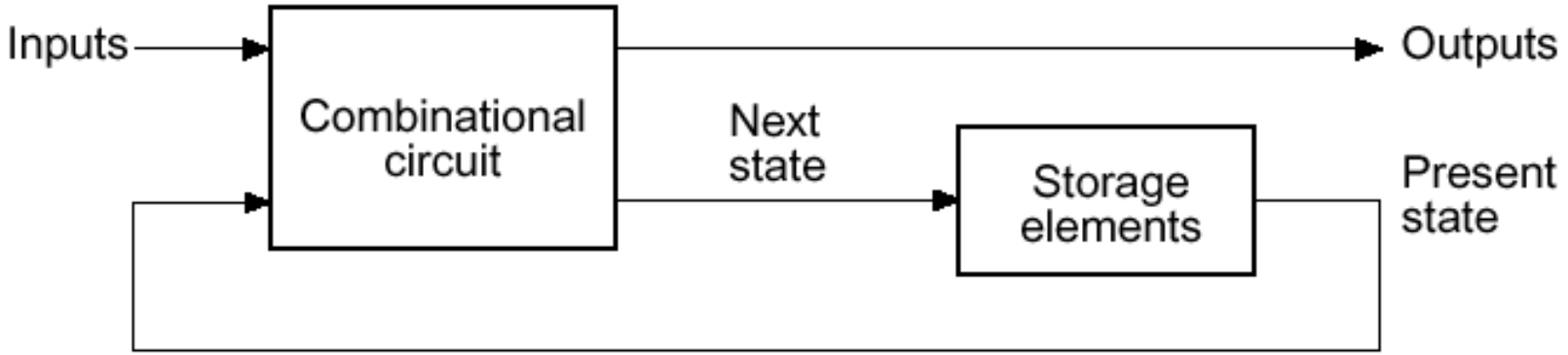
inja meghdare khoroji haro az hamin rabete ha be dast avordim .

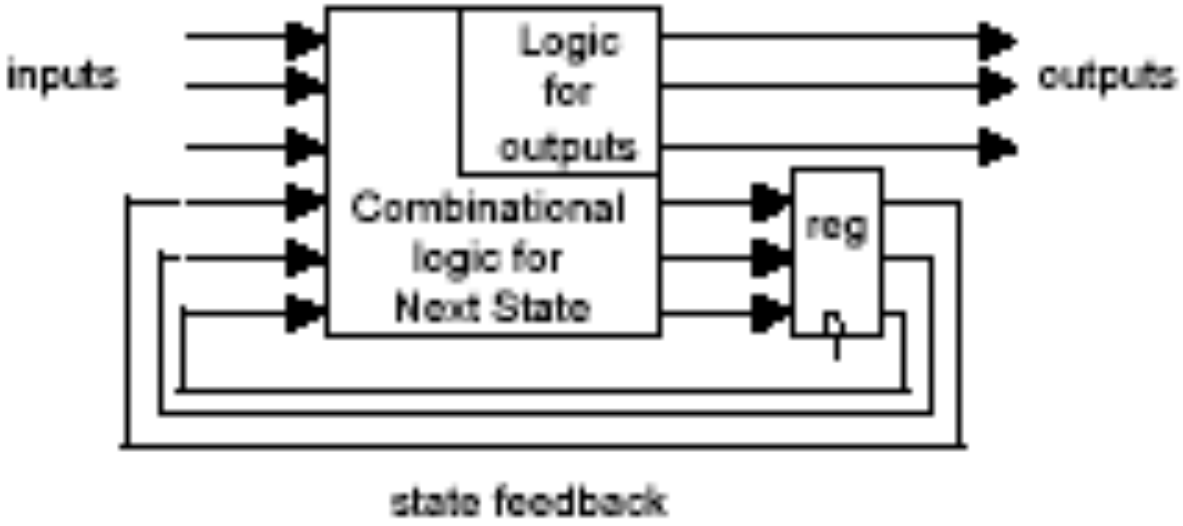
1 + 2 = 3 —> 2 be tavane 3 yani 8 satr niaz darim .

Present State		Input	Next State		Output
A(t)	B(t)	x(t)	A(t+1)	B(t+1)	y(t)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

General Forms of Sequential Circuits (1)

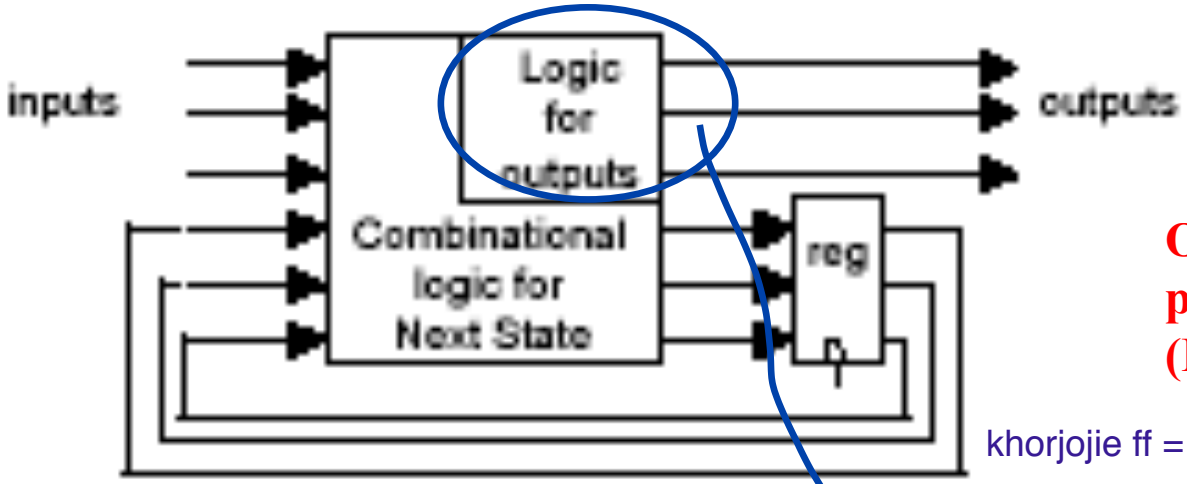






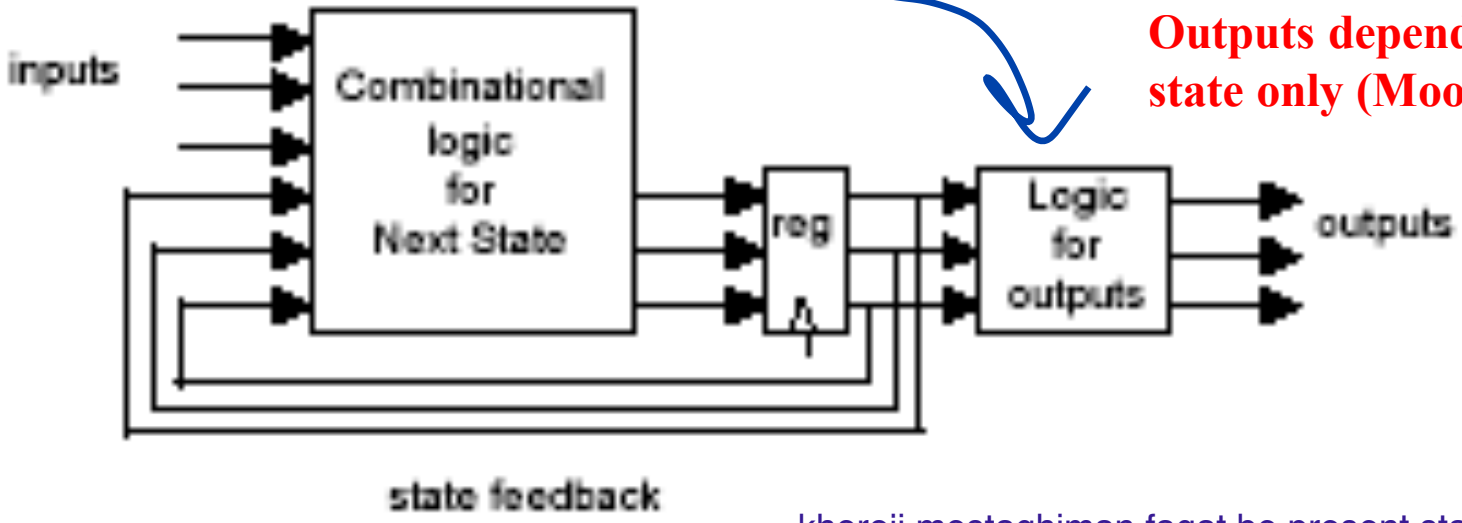
General Forms of Sequential Circuits (2)

khoroji bastegi dare be inputs va present state ha —> mili



Outputs depend on present state and inputs (Mealy machine)

khorjojie ff = present state



Outputs depend on present state only (Moore machine)

khoroji mostaghiman faqat be present state vabastast va gheire mostaghim be inputs vabastast .

Mealy vs. Moore Machines

- **Mealy model:**
  - Both outputs and next state depend on primary inputs AND present state
    - Out = f(inputs, state)
    - Top diagram in the previous slide
- **Moore model:**
  - Only next state depends directly on primary inputs AND present state. Outputs depend only on present state
    - Out = f(state)
    - Bottom diagram in the previous slide

Mealy/Moore Comparison

toye moore khoroji hatman vbyad vaiste clock biad va ff ha taghir bokonan
ta khoroji tashkil behse vali toye mili majboor nistan viastan va soratesh bishtare .

- Mealy machines react faster to inputs
  - React in same cycle – don't need to wait for clock
  - In Moore machines, more logic may be necessary to decode state into outputs – more gate delays after
- Moore machines are easier and safer to use

ehtemle khata toosh kamtare

  - Outputs change at clock edge (always one cycle later)
  - In Mealy machines, input change can cause output change as soon as logic is done – a big problem when two machines are interconnected – asynchronous feedback

tosie baraye ma = moore

State Diagram

- The sequential circuit function can be represented in graphical form as a state diagram with the following components:
  - A circle with the state name in it for each state
  - A directed arc (felesh haye jahaat dar) from the Present State to the Next State (jabeayi halat) for each state transition
  - A label on each directed arc with the Input values which causes the state transition, and
  - A label:
    - In each circle with the output value produced (Moore), or
    - On each directed arc with the output value produced (Mealy).

State Diagram

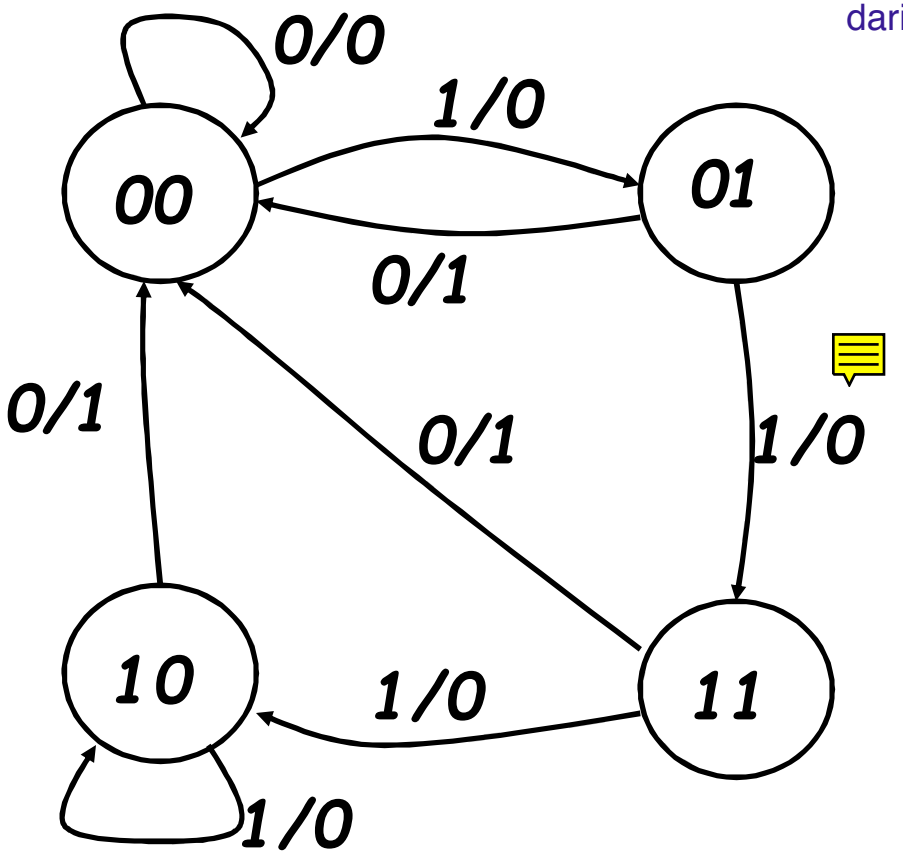
- **Label form:**
  - In circle (for Moore machines):
    - state/output
    - **Moore** type output depends only on state
  - On directed arc (for Mealy machines):
    - input/output
    - **Mealy** type output depends on state and input

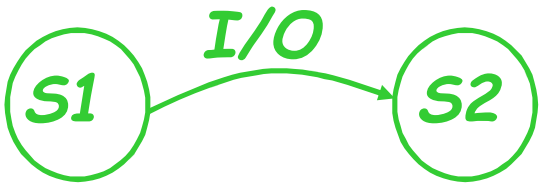
Example: Mealy Model

age dar state 00 basham va vorodie 1 biad , khoroji ma 0 hast (na mimone na taghir mikone chon khoroji ghablie ro nemidonim) va mirim state 01 .

State Diagram

4 halat dare —>chon 4 dayere
pas 2 ta motegahyere halat darim . (2 be tavane 2.)





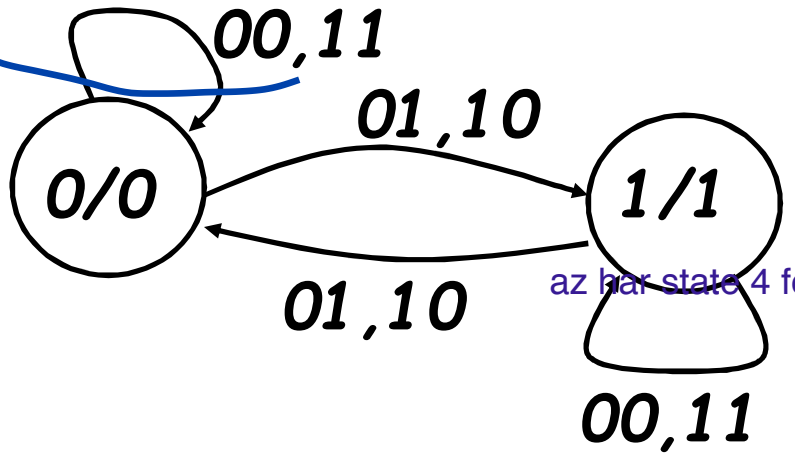
Reads as:
When at state ***s1*** and apply input ***I***, we get output ***O*** and proceed to state ***s2***.

deghat kon ke inja comma hast va slash nist

Example: Moore Model

State Diagram

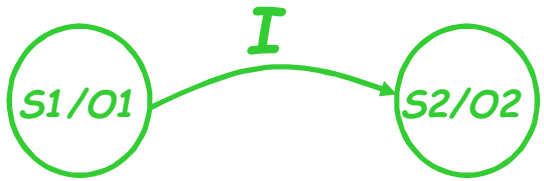
inja dar vaghe baraye kamtar shodane tedad felesh ha inkaro kardim .



az har state 4 felesh kharej mishe pas kamle hast .

inja age state 0 bashe ouput ham 0 va 1 bashe 1 .

chon khoroji faqat be state mostaghim vabastast va be input gheire mostaghim vabastast —> pas baham to ye dayere

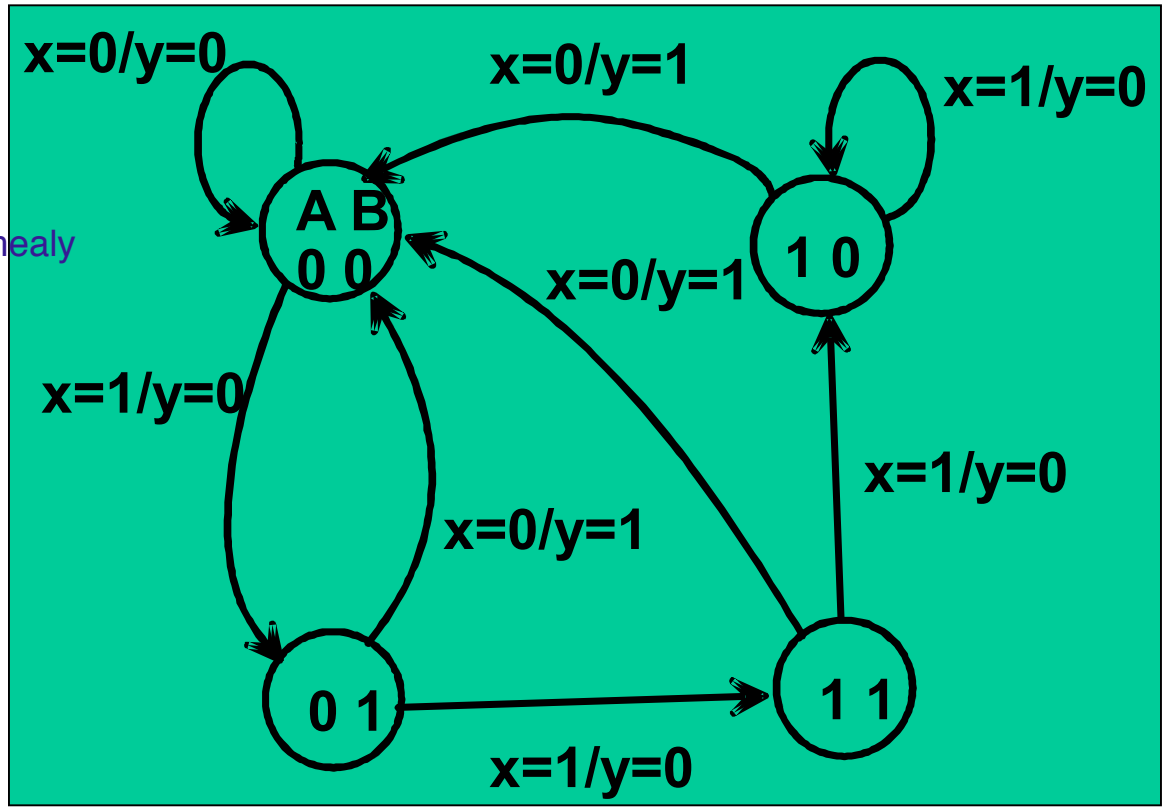


Reads as:
When at state ***s1*** with output ***O1*** and apply input ***I***,
we proceed to state ***s2*** with output ***O2***.

State Diagram Example

- Which type?

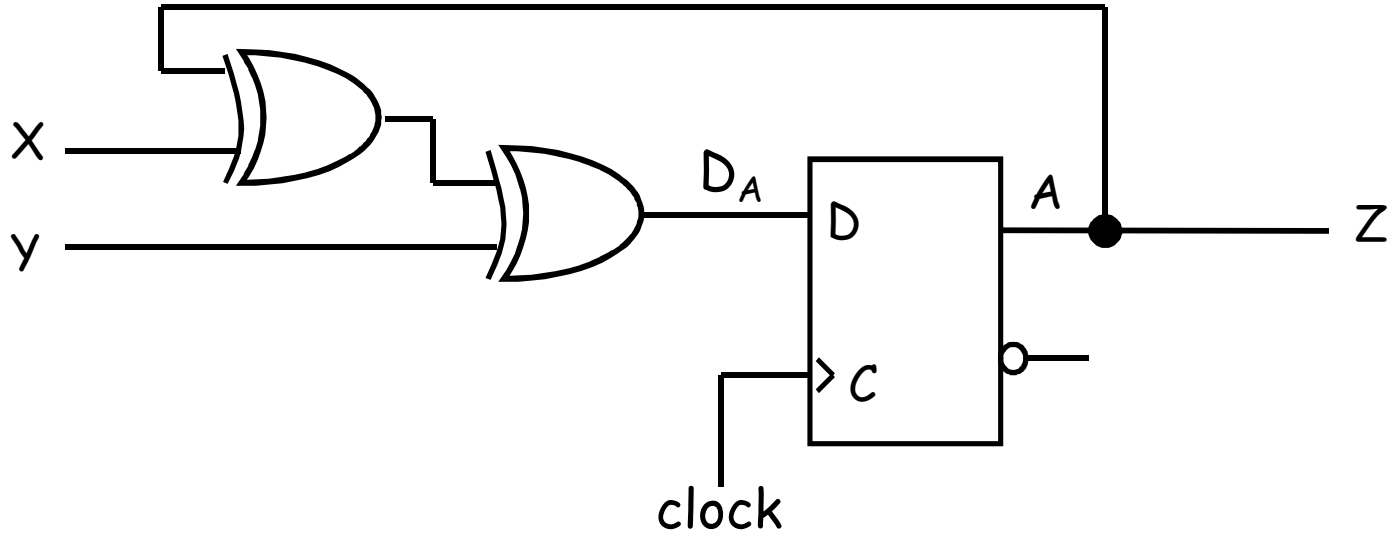
horoji dar dakhele haat nayoomade —> mealy



a va b moteghayer haye halate ma hastan.
kamel hast chon 2 felesh az harkodom kharej mishe.

Example of a M…(?) Machine

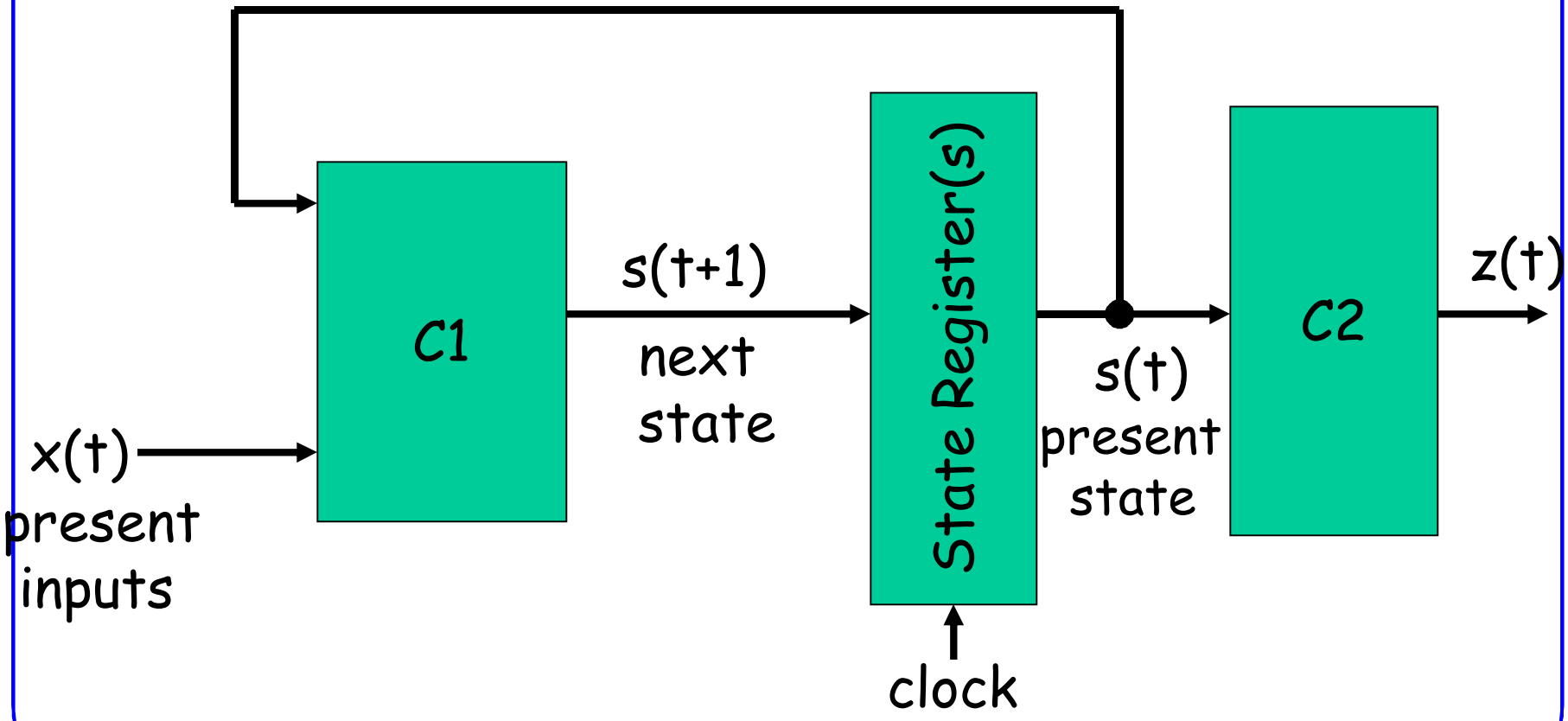
- **Obtain the logic expression and state table for this circuit:**



moore - > chon yek khoroji faqat darim va faqat be state vabastast .
az vorodi man masiri be khorji ke az ff oboor nakone nadarim .

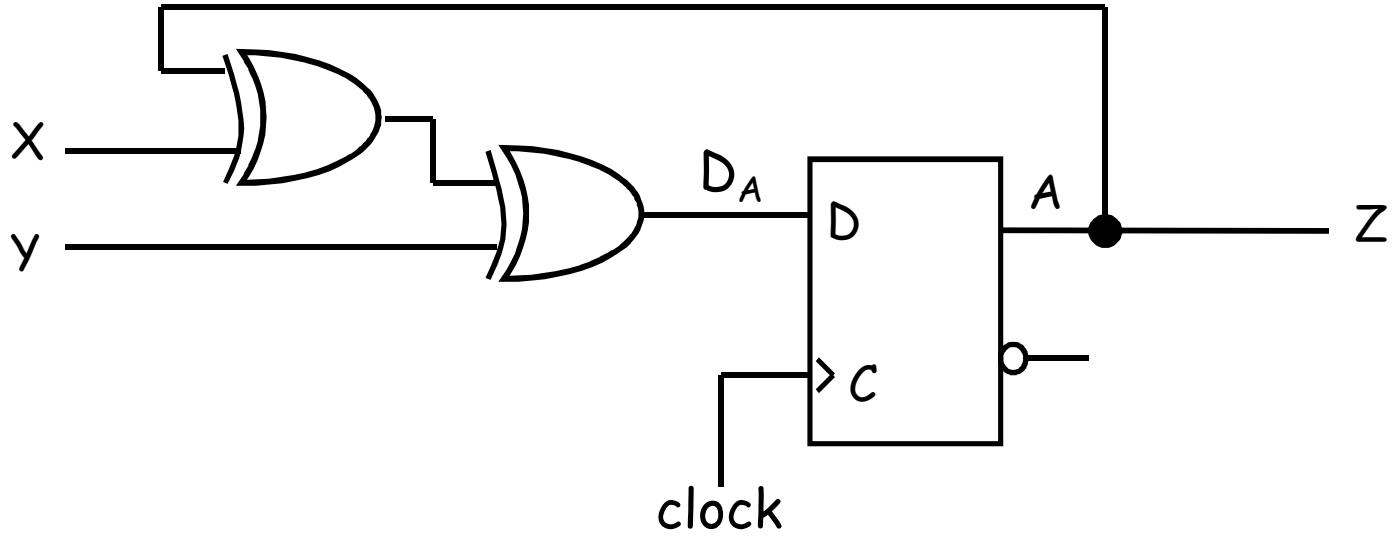
Moore Machine Reminder

to mesal ghabli c2 sime



Example of a Moore Machine

- **Obtain the logic expression and state table for this circuit:**



$D_A = A \oplus X \oplus Y$ hamishe vorodie ff next state hast .

$Z = A$

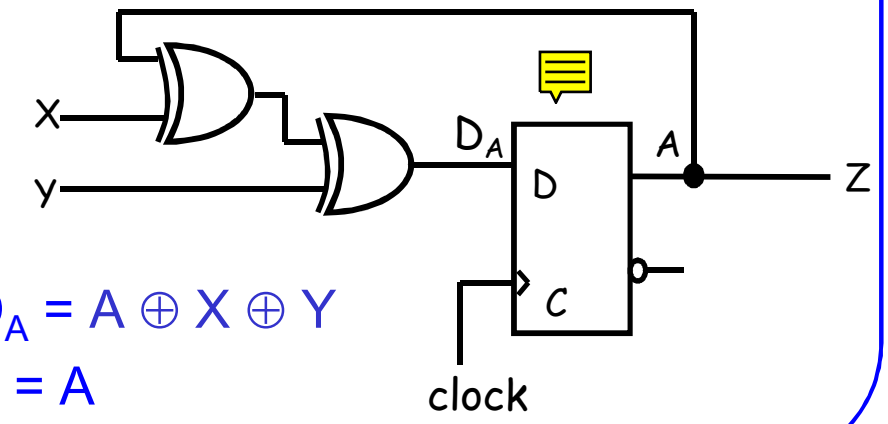
Example of a Moore Machine (cont.)

State Table

Present State	Inputs		Next State	Output
A(t)	X	Y	A(t+1)	Z
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Alternative State Table

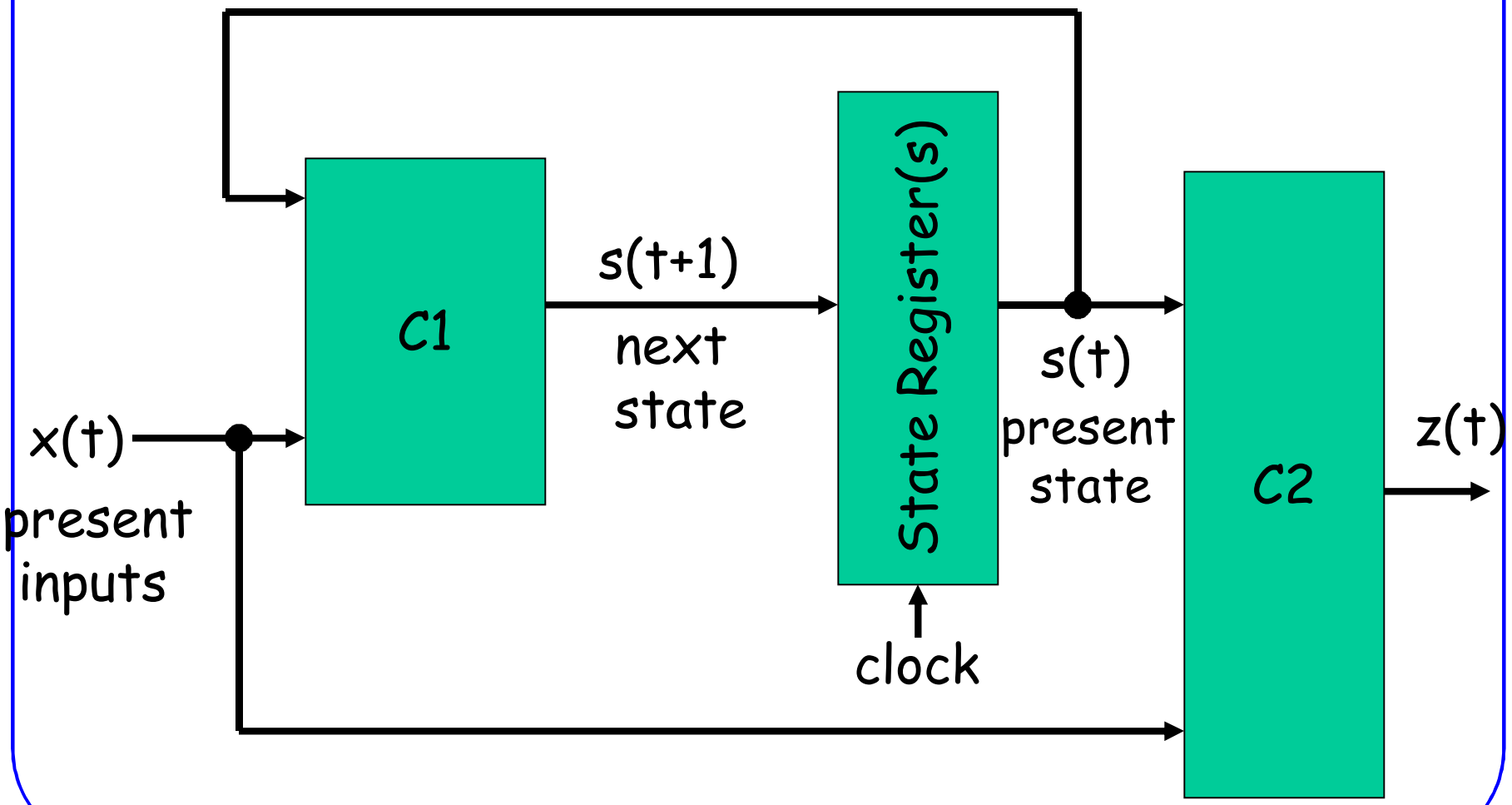
Present State	Next State				Output
	XY=00	XY=01	XY=10	XY=11	
A(t)	A(t+1)	A(t+1)	A(t+1)	A(t+1)	Z
0	0	1	1	0	0
1	1	0	0	1	1



$D_A = A \oplus X \oplus Y$

$Z = A$

Mealy Machine Reminder



Example: Mealy Model

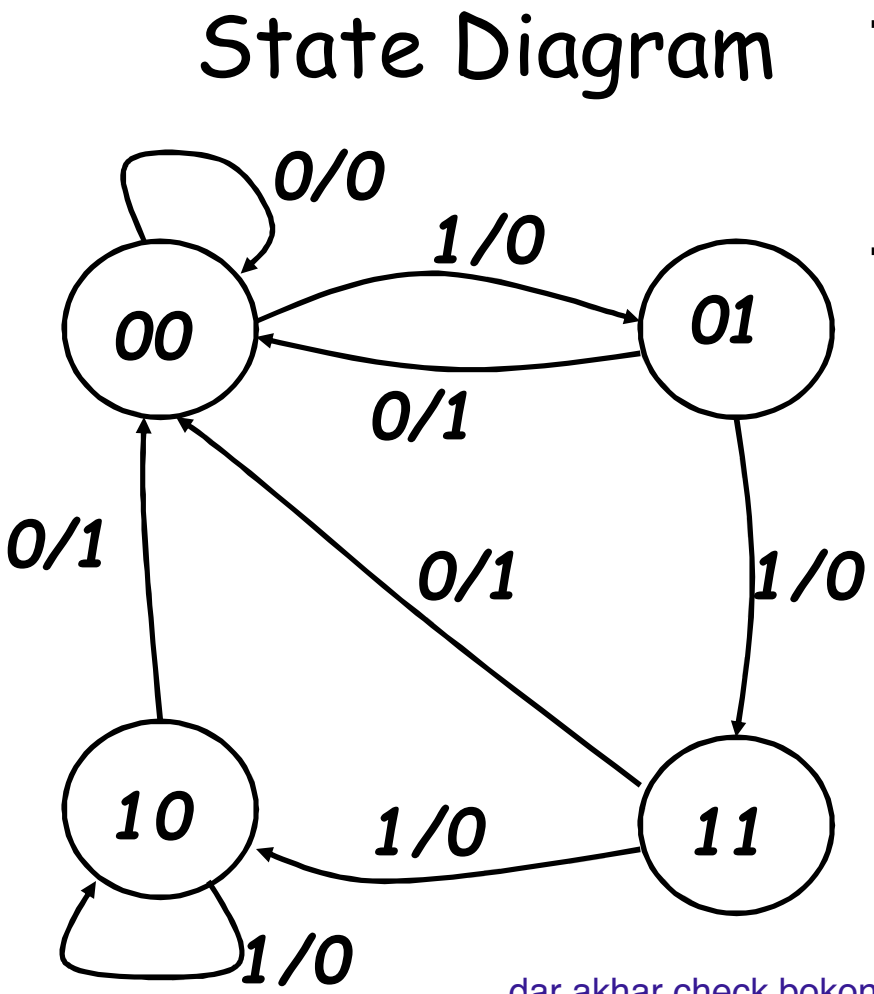
Draw the state diagram of the machine whose state table is like this:

State Table

Present State		Input	Next State		Output
A(t)	B(t)	X	A(t+1)	B(t+1)	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Possible states = {00, 01, 10, 11}
→ 4 nodes in state diagram

Example: Mealy Model (cont.)



Present State		Input	Next State		Output
A(t)	B(t)	X	A(t+1)	B(t+1)	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

dar akhar check bokon ke az har state 2 ta felesh kharej shod e bashe .

Example: Moore Model

State Table

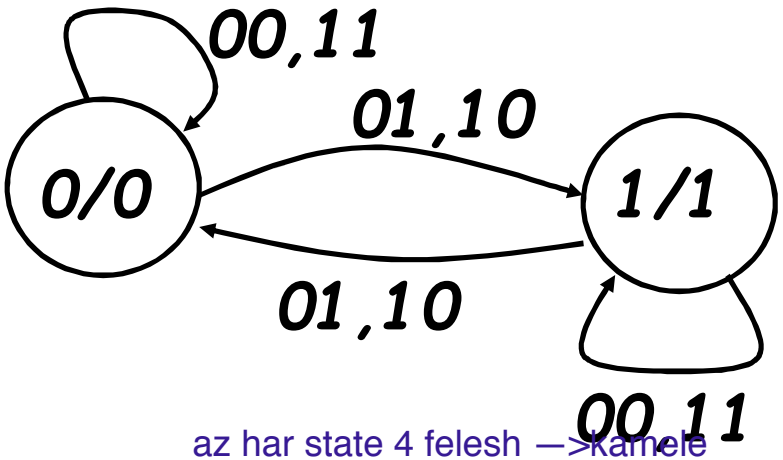
Present State	Inputs		Next State	Output
A(t)	X	Y	A(t+1)	Z
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Possible states = {0, 1} chon yedone moteghayere halat darim

→ 2 nodes in state diagram

Example: Moore Model (cont.)

State Diagram



az har state 4 felesh —>kamele

Present State	Inputs		Next State	Output
A(t)	X	Y	A(t+1)	Z
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

State Tables for JK Flip-Flops

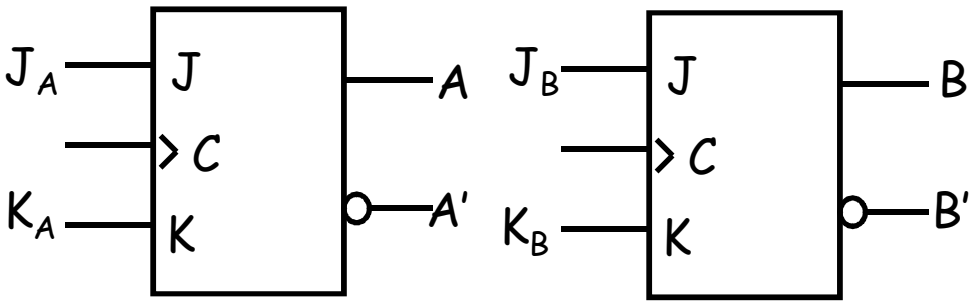
- **Two-step procedure:**
  1. Obtain binary values of each FF input equation in terms of present state and input variables.
  2. Use corresponding FF characteristic table to determine the next state.

Example

$J_A = B, K_A = BX'$

$J_B = X', K_B = AX' + A'X = A \oplus X$

- → **2 JK-FFs:**



JK-FF Characteristic Table

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q(t)'

Example (cont.)

Present State		Input	Next State		FF inputs			
A(t)	B(t)	X	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0			0	0	1	0
0	0	1			0	0	0	1
0	1	0			1	1	1	0
0	1	1			1	0	0	1
1	0	0			0	0	1	1
1	0	1			0	0	0	0
1	1	0			1	1	1	1
1	1	1			1	0	0	0

$J_A = B$, $K_A = BX'$

$J_B = X'$, $K_B = AX' + A'X = A \oplus X$

Step 1:
Use FF input equations

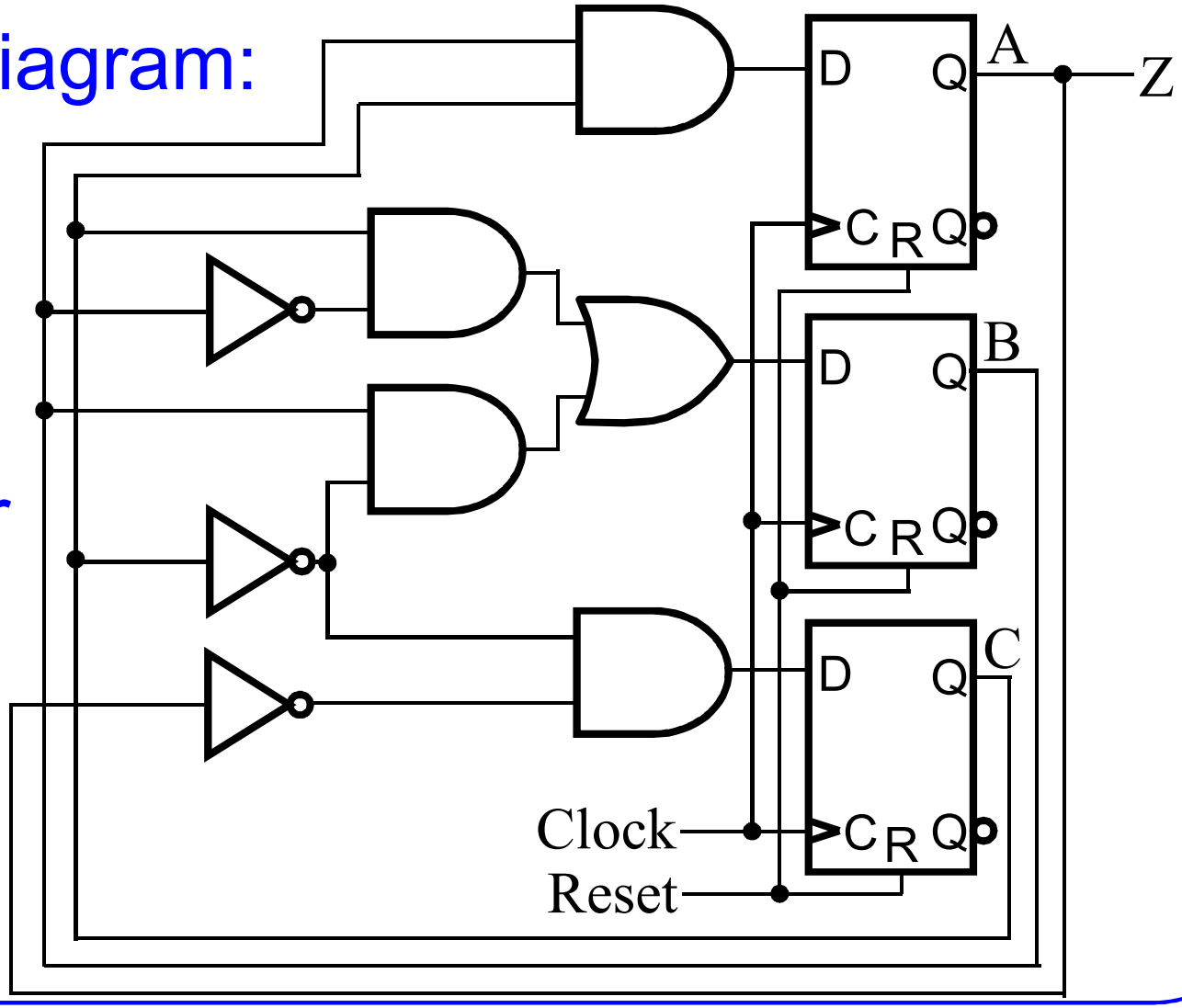
Example (cont.)

Present State		Input	Next State		FF inputs			
A(t)	B(t)	X	A(t+1)	B(t+1)	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

Step 2:
Use FF inputs and JK characteristic table

Example 2: Sequential Circuit Analysis

- Logic Diagram:



- Mealy or Moore?

Example 2: Flip-Flop Input Equations

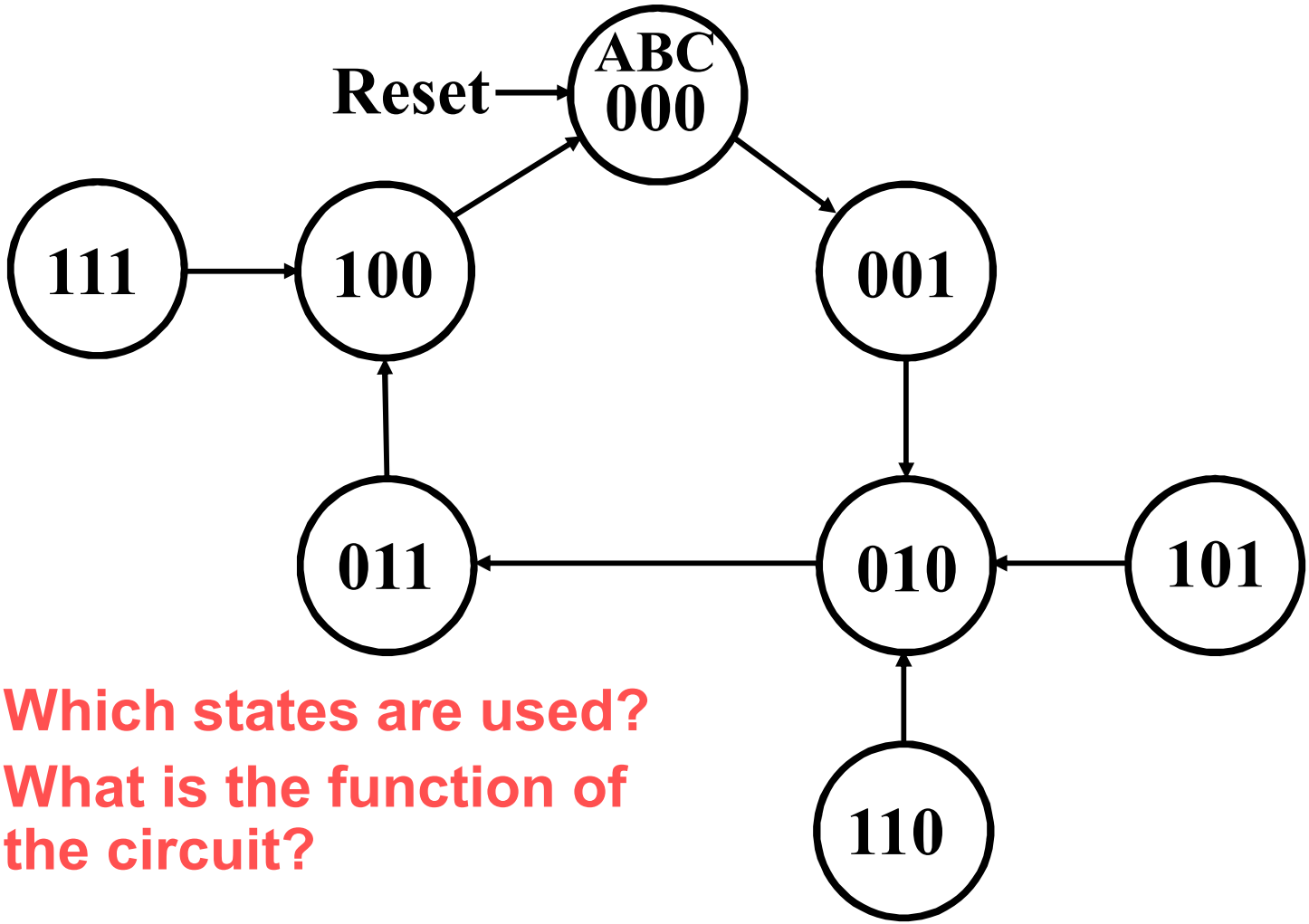
- **Variables**
  - Inputs: None
  - Outputs: Z
  - State Variables: A, B, C
- **Initialization:**
  - Reset to (0,0,0)
- **Equations**
  - A(t+1) = ? BC
  - B(t+1) = ? B'C+BC'
  - C(t+1) = ? A'C'
  - Z = ? A

Example 2: State Table

$S^+=S(t+1)$

A B C	$A^+B^+C^+$	Z
0 0 0		
0 0 1		
0 1 0		
0 1 1		
1 0 0		
1 0 1		
1 1 0		
1 1 1		

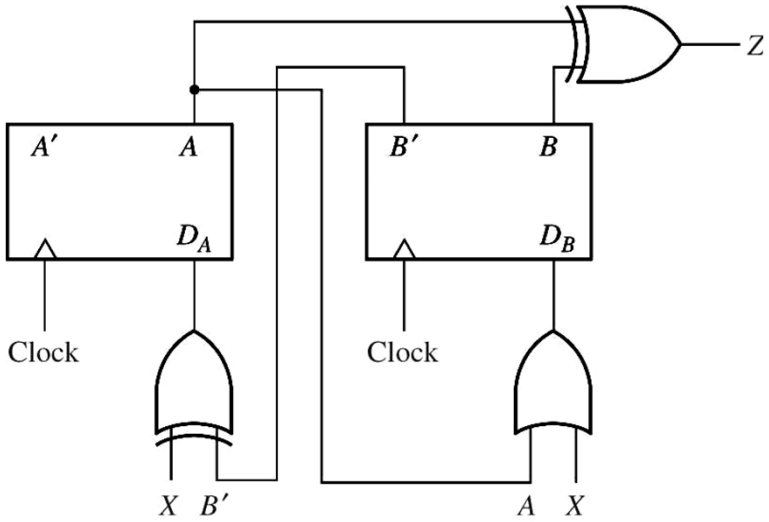
Example 2: State Diagram



- Which states are used?
- What is the function of the circuit?

Example 3

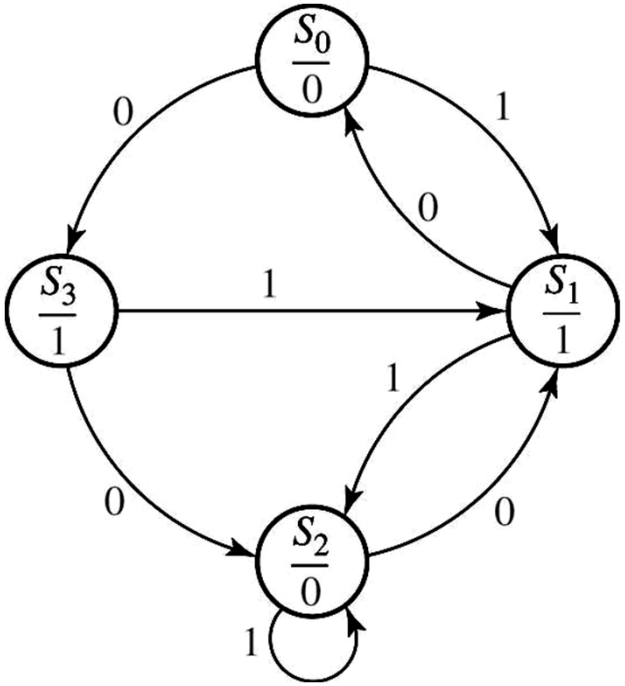
- **Mealy or Moore?**

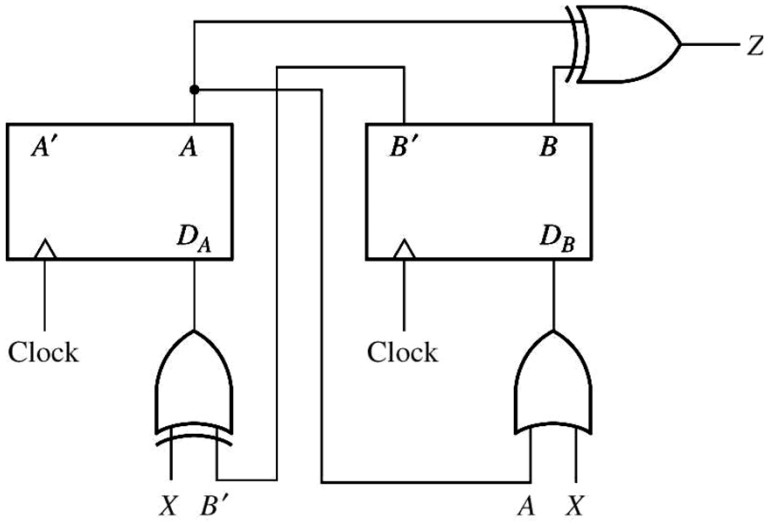


AB	$X=0$ A^+B^+	$X=1$ A^+B^+	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

Present State	Next state $X=0$	Next state $X=1$	Present Output(z)
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

Example 3

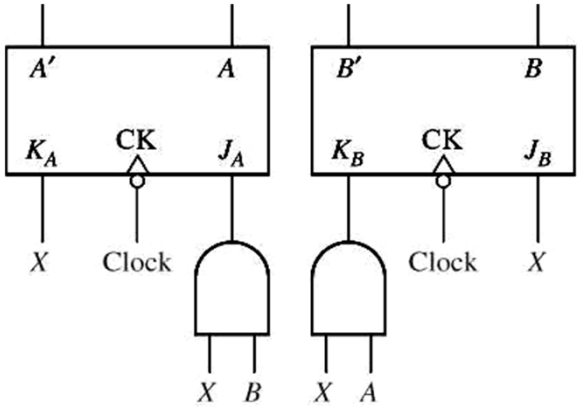


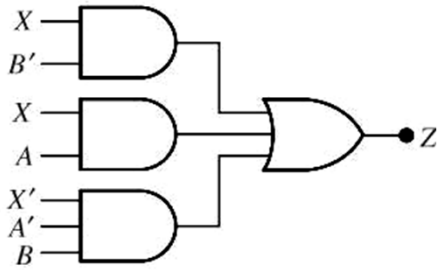


Present State	Next state $X=0$	Next state $X=1$	Present Output(z)
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

Example 4

- Mealy or Moore?

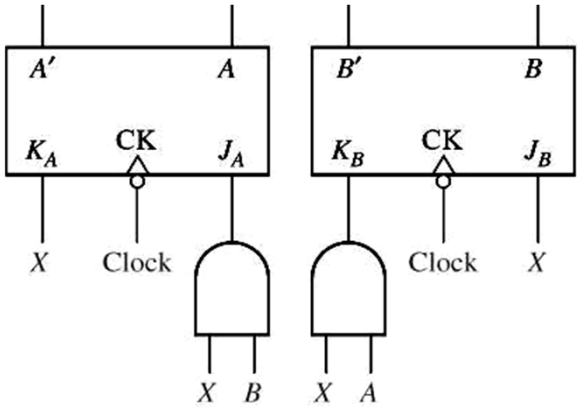


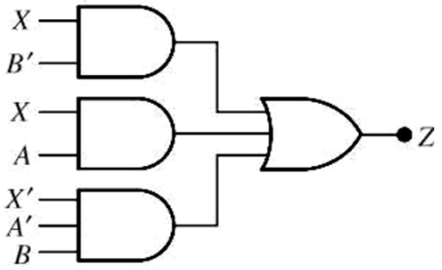


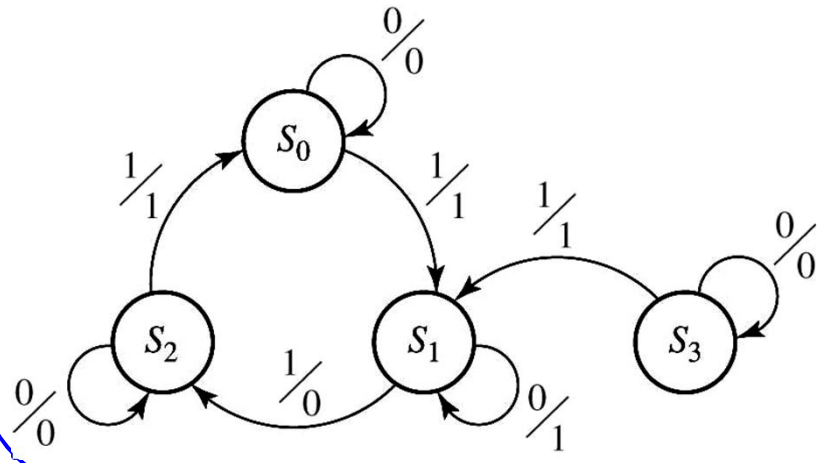
AB	A^+B^+ $X=0$	$X=1$	Z $X=0$	$X=1$
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

Present State	Next state $X=0$	$X=1$	Present Output(z) $X=0$	$X=1$
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

Example 4







Present State	Next state		Present Output(z)	
	$X=0$	$X=1$	$X=0$	$X=1$
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

Circuit Analysis by Signal Tracing

Waveforms

Timing Chart

- **Construction and interpretation of a timing chart:**
  - A state change can only occur after the rising (or falling) edge of the clock.
  - The input will normally be stable immediately before and after the active clock edge.
  - For a Mealy circuit, the output can change when the input changes as well as when the state changes.
    - A false output may occur between the state changes and the time the input changes to its new value.
  - False outputs are difficult to determine from the state diagram, so sometimes have to use signal tracing (timing chart).

State Tables

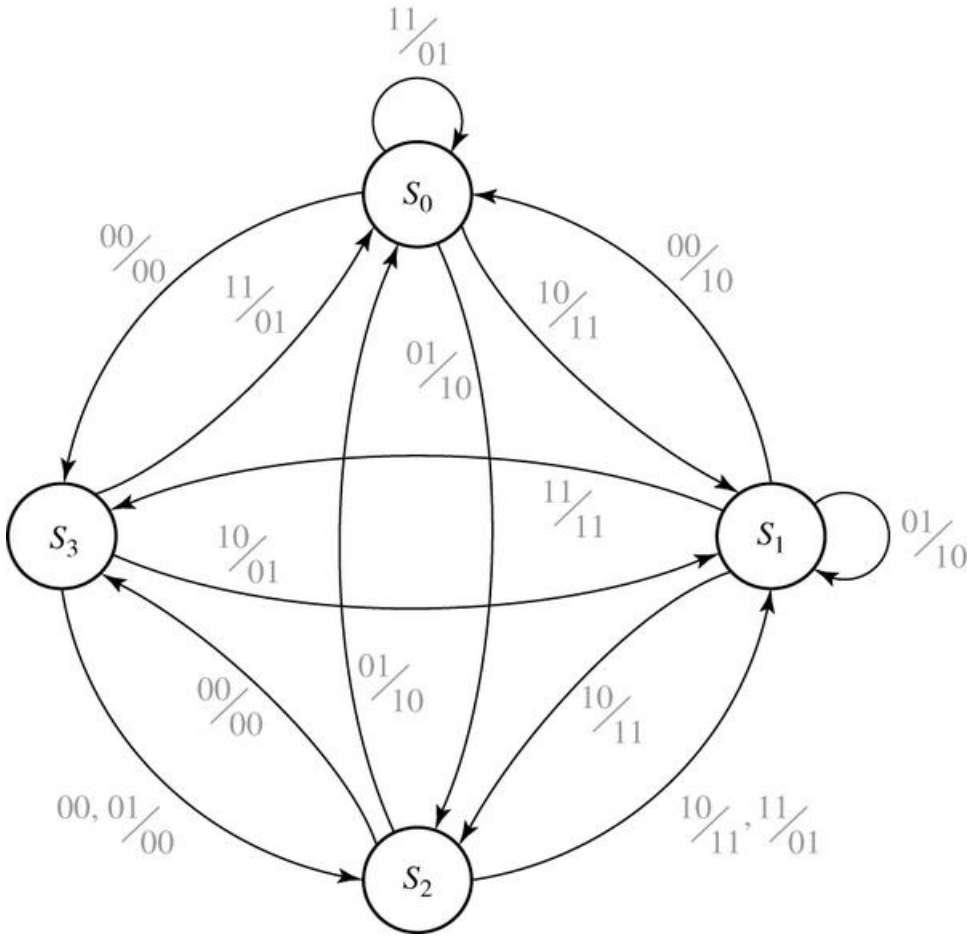
Example of a state table with multiple inputs and outputs:

(2 state variables => 4 states, 2 inputs, 2 outputs)

Present State	Next state				Outputs			
	$X_1X_2 = 00$	01	10	11	$X_1X_2 = 00$	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

State Diagram

The state diagram of the previous example



Mealy Machine State Diagrams

- A CLARIFICATION:
  - The state diagram notation for output values in Mealy machines is a little misleading:
    - You should remember that the listed output value is produced continuously when the machine is in the indicated state and has the indicated input, not just during the transition to the next state.