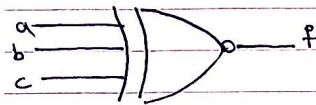


Subject:

1)



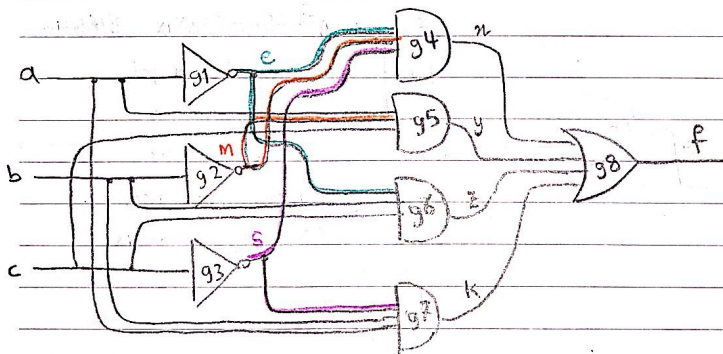
$$f = (a \oplus b \oplus c)'$$

| a | b | c | $a \oplus b$ | $(a \oplus b) \oplus c$ | f |
|---|---|---|--------------|-------------------------|---|
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 |

| c \ ab | 00 | 01 | 11 | 10 |
|--------|----|----|----|----|
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |

$\xrightarrow{SOP} f = a'b'c' + a'bc + abc' + ab'c$

2)



Subject:

```
module xnor_circuit ( a, b, c, f );
```

```
input a, b, c;
```

```
output f;
```

```
wire e, m, s, x, y, z, k;
```

```
not g1(e, a);
```

```
not g2(m, b);
```

```
not g3(s, c);
```

```
and g4(x, e, m, s);
```

```
and g5(y, m, a, c);
```

```
and g6(z, e, b, c);
```

```
and g7(k, s, a, b);
```

```
or g8(f, x, y, z, k);
```

```
endmodule
```