age: Details 🔻		▼ <u>R</u> esult: 5 - 13	36 - prefixSumSca	anKernel	- 7	∇ -	Add Baseline 🔻	Apply <u>R</u> ules	Occupancy Calculator		Save as PDF		
	Result		Time	Cycles	Regs GP	PU		SM Frequency	CC	Process	⊕ ⊝	R	A
Curre	nt 136 - pre	efixSumScanKernel (30.30 usecond	٤٢٠٠٣٣	۱٦ ٥-	NVID	IA GeForce RTX 3090	1.38 cycle/nseco	nd 8.6	[258893] task2	Street Square		
▶ GPU	Speed Of Lig	ght Throughput							All			-	Ω
		of the throughput for co etical maximum. Breakc											
Compute (SM) Throughput [%]					20.	.61	Duration [usecond]					30.	30
Memory Throughput [%]					18.	.13	Elapsed Cycles [cycle]					42,0	33
L1/TEX Cache Throughput [%]					19.	.35	SM Active Cycles [cyc	:le]			39	,321.	55
L2 Cache Throughput [%]				2.	.26	SM Frequency [cycle/	nsecond]				1.	38	
DRAM T	hroughput [%]			0.	.76	DRAM Frequency [cyc	cle/nsecond]				9.	44
	atency Issu	Statistics and D Wa	throughput and/earp State Statistic		y bandwidt ntial reaso		low 60.0% of peak typ	ically indicate laten	cy issues	s. Look at <u>D Sche</u>	duler	€	_
Laun	ch Statistics	;											Ω
		figuration used to laund execute the kernel. Ch							n of the o	grid into blocks, a	and the G	PU	
Grid Size	e				24,0	000	Function Cache Confi	guration		cudaFuncC	achePre	ferNo	ne
Register	rs Per Threa	d [register/thread]				16	Static Shared Memory	y Per Block [Kbyte/b	olock]			8.	19
Block Size						4	Dynamic Shared Mem	nory Per Block [byte	/block]				0
	[thread]				96,0	000	Driver Shared Memory	y Per Block [Kbyte/l	olock]				02
Waves F	Per SM				26.	.61	Shared Memory Confi	iguration Size (Kbyt	e]			102.	40
A E	Block Size	Threads are executed Consequently, some the block to be a multiple thread blocks rather the kernels that frequently	nreads in a warp a of 32 threads. Bet nan one large thre	re maske tween 128 ad block p	d off and to and 256 to per multipre	those thread oces	hardware resources a ds per block is a good sor if latency affects p	are unused. Try char initial range for exp performance. This is	nging the perimenta s particul	number of threa ation. Use smalle arly beneficial to	er	•	2
▶ Occu	pancy												Ω
percenta always re	ge of the ha educes the a	io of the number of act irdware's ability to proc ability to hide latencies, ically indicates highly ir	ess warps that is resulting in overa	actively in Il perform	n use. High	ner oc	cupancy does not alw	ays result in higher	perform	ance, however, lo	ож оссир	ancy	
Theoretical Occupancy [%]				22.	.92	Block Limit Registers	[block]				1	28	
Theoretical Active Warps per SM [warp]						11	Block Limit Shared Me	em [block]					11
Achieved Occupancy [%]				18.	.31	Block Limit Warps [blo	ock]					48	
Achieved Active Warps Per SM [warp]				8.	.79	Block Limit SM [block	[16	
A (Occupancy L	imiters	theoretical occup ails on optimizing			ited b	y the required amount	t of shared memory	See the	CUDA Best Pr			