Page: Details | Result: 0 - 114 - convolution_2D_tiled_kerne | Add Baseline | Apply Rules | Occupancy Calculator | Save as PDF

	Result	Time	Cycles	Regs	GPU	SM Frequency	CC	Process
Current	114 - convolution_2D_tiled_kernel (750, 500, 1)x(8, 8, 1)	767.78 usecond	١٬٠٧٠٬٧٥٣	٢٤	0 - NVIDIA GeForce RTX 3090	1.39 cycle/nsecond	8.6	[256896] task1

GPU Speed Of Light Throughput

High-level overview of the throughput for compute and memory resources of the GPU. For each unit, the throughput reports the achieved percentage of utilization with respect to the theoretical maximum. Breakdowns show the throughput for each individual sub-metric of Compute and Memory to clearly identify the highest contributor.

Compute (SM) Throughput [%]	45.48	Duration [usecond]	767.78
Memory Throughput [%]	40.37	Elapsed Cycles [cycle]	1,070,753
L1/TEX Cache Throughput [%]	44.57	SM Active Cycles [cycle]	1,068,001.29
L2 Cache Throughput [%]	40.37	SM Frequency [cycle/nsecond]	1.39
DRAM Throughput [%]	27.08	DRAM Frequency [cycle/nsecond]	9.49

Latency Issue This kernel exhibits low compute throughput and memory bandwidth utilization relative to the peak performance of this device. Achieved compute throughput and/or memory bandwidth below 60.0% of peak typically indicate latency issues. Look at Scheduler Statistics and Warp State Statistics for potential reasons.

Launch Statistics

Summary of the configuration used to launch the kernel. The launch configuration defines the size of the kernel grid, the division of the grid into blocks, and the GPU resources needed to execute the kernel. Choosing an efficient launch configuration maximizes device utilization.

Grid Size	375,000	Function Cache Configuration	cudaFuncCachePreferNone
Registers Per Thread [register/thread]	24	Static Shared Memory Per Block [byte/block]	256
Block Size	64	Dynamic Shared Memory Per Block [byte/block]	0
Threads [thread]	24,000,000	Driver Shared Memory Per Block [Kbyte/block]	1.02
Waves Per SM	285.82	Shared Memory Configuration Size [Kbyte]	32.77

Occupancy

Occupancy is the ratio of the number of active warps per multiprocessor to the maximum number of possible active warps. Another way to view occupancy is the percentage of the hardware's ability to process warps that is actively in use. Higher occupancy does not always result in higher performance, however, low occupancy always reduces the ability to hide latencies, resulting in overall performance degradation. Large discrepancies between the theoretical and the achieved occupancy during execution typically indicates highly imbalanced workloads.

Theoretical Occupancy [%]	66.67	Block Limit Registers [block]	42
Theoretical Active Warps per SM [warp]	32	Block Limit Shared Mem [block]	25
Achieved Occupancy [%]	56.53	Block Limit Warps [block]	24
Achieved Active Warps Per SM [warp]	27.13	Block Limit SM [block]	16

Occupancy Limiters This kernel's theoretical occupancy (66.7%) is limited by the number of blocks that can fit on the SM The difference between calculated theoretical (66.7%) and measured achieved occupancy (56.5%) can be the result of warp scheduling overheads or workload imbalances during the kernel execution. Load imbalances can occur between warps within a block as well as across blocks of the same kernel. See the CUDA Best Practices Guide for more details on optimizing occupancy.