Latch

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test scenario | D | Clk | Q | Nq |
|  | 1 | 0 | X | X |
| 1 | 1 | 1 | 1 | 0 |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 0 | 0 | 0 | 1 |
| 4 | 1 | 0 | 0 | 1 |

Tff

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test scenario | T | Clk | Clear | Q |
|  | 0 | 0 | 0 | X |
| Clear asynchronously set the output to zero | 0 | 0 | 1 | 0 |
| T change to one, Output does not change | 1 | 0 | 1 | 0 |
| Clear to zero, Output does not change | 1 | 0 | 0 | 0 |
| T at one toggles output from zero to 1 on rising edge clock | 1 | 1 | 0 | 1 |
| Clear asynchronously set the output to zero clearing 1 output | 1 | 1 | 1 | 0 |
| T to zero, Output does not change | 0 | 1 | 1 | 0 |
| Clear to zero, Output does not change | 0 | 1 | 0 | 0 |
| Clock falling edge, Output does not change | 0 | 0 | 0 | 0 |
| T change to one, Output does not change | 1 | 0 | 0 | 0 |
| T at one toggles output from zero to 1 on rising edge clock | 1 | 1 | 0 | 1 |
| Clock falling edge, Output does not change | 1 | 0 | 0 | 1 |
| T at 1 toggles output from 1 to zero on rising edge clock | 1 | 1 | 0 | 0 |

Priority

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Test scenario | Sel0 | Sel1 | Sel2 | Sel4 | Z0 | Z1 | Z2 |
| Out of bounds Input set priority to 111 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Sel is 1000 priority is 000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Sel is 0100  priority is 001 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Out of bounds Input set priority to 111 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| Sel is 0010 priority is 010 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Out of bounds Input set priority to 111 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| Out of bounds Input set priority to 111 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| Out of bounds Input set priority to 111 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| Sel is 0001  Priority is 011 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| Out of bounds Input set priority to 111 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| Out of bounds Input set priority to 111 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| Out of bounds Input set priority to 111 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| Out of bounds Input set priority to 111 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| Out of bounds Input set priority to 111 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| Out of bounds Input set priority to 111 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| Out of bounds Input set priority to 111 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Mux

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Test scenario | S1 | S0 | A | B | C | D | z |
| S is 00 and A (zero) is propagated to output | 0 | 0 | 0 | X | X | X | 0 |
| S is 00 and A (1) is propagated to output | 0 | 0 | 1 | X | X | X | 1 |
| S is 01 and B (zero) is propagated to output | 0 | 1 | 1 | 0 | X | X | 0 |
| S is 0 and B (1) is propagated to output | 0 | 1 | X | 1 | X | X | 1 |
| S is 10 and C (zero) is propagated to output | 1 | 0 | X | 1 | 0 | X | 0 |
| S is 10 and C (1) is propagated to output | 1 | 0 | X | X | 1 | X | 1 |
| S is 11 and D (zero) is propagated to output | 1 | 1 | X | X | 1 | 0 | 0 |
| S is 11 and D (1) is propagated to output | 1 | 1 | X | X | X | 1 | 1 |

Halfadder

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test scenario | a | B | S | c |
| For Zero input sum and carry is zero | 0 | 0 | 0 | 0 |
| Input bit a is one, sum is one and carry is zero | 1 | 0 | 1 | 0 |
| Both inputs are one, both output carry is set and sum is not set | 1 | 1 | 0 | 1 |
| Input bit b is one and the other is zero, sum is one carry is zero | 0 | 1 | 1 | 0 |

fulladder

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Test scenario | a | B | c\_in | S | C\_out |
| For Zero input sum and carry is zero | 0 | 0 | 0 | 0 | 0 |
| Input bit a is one, sum is one and carry is zero | 1 | 0 | 0 | 1 | 0 |
| Both inputs are one and input carry is zero, output carry is set and sum is not set | 1 | 1 | 0 | 0 | 1 |
| Input bit b is one and the other is zero, sum is one carry is zero | 0 | 1 | 0 | 1 | 0 |
| Input bit b is one and input carry is one, only output carry is set | 0 | 1 | 1 | 0 | 1 |
| All inputs are set, all outputs are set as a result | 1 | 1 | 1 | 1 | 1 |
| Only bit a and the input carry are set, only output carry is set | 1 | 0 | 1 | 0 | 1 |
| Only input carry is set, only sum bit is set | 0 | 0 | 1 | 1 | 0 |

Demux

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Test scenario | A1 | A0 | D | Z3 | Z2 | Z1 | Z0 |
| Select first output and input is zero, only first output is zero | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Select first output and input is one, first output is one | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Select second input and input is one, only second output is one | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| Select second output and input is zero, output is zero | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Select fourth output and input is zero, output is zero | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Select fourth output and input is one, only fourth output is one | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| Select third output and input is one, only third output is one | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Select third output and input is zero, output is zero | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Decoder

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Test scenario | Address2 | Address1 | Address0 | Decode7 | Decode6 | Decode5 | Decode4 | Decode3 | Decode2 | Decode1 | Decode0 |
| Default case | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Designed output | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| Default case | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Designed output | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Designed output | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Designed output | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| Designed output | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Default case | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |