Latch

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test scenario | D | Clk | Q | Nq |
|  | 1 | 0 | X | X |
| 1 | 1 | 1 | 1 | 0 |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 0 | 0 | 0 | 1 |
| 4 | 1 | 0 | 0 | 1 |

Tff

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Test scenario | T | Clk | Clear | Q |
|  | 0 | 0 | 0 | X |
| Clear asynchronously set the output to zero | 0 | 0 | 1 | 0 |
| T change to one, Output does not change | 1 | 0 | 1 | 0 |
| Clear to zero, Output does not change | 1 | 0 | 0 | 0 |
| T at one toggles output from zero to 1 on rising edge clock | 1 | 1 | 0 | 1 |
| Clear asynchronously set the output to zero clearing 1 output | 1 | 1 | 1 | 0 |
| T to zero, Output does not change | 0 | 1 | 1 | 0 |
| Clear to zero, Output does not change | 0 | 1 | 0 | 0 |
| Clock falling edge, Output does not change | 0 | 0 | 0 | 0 |
| T change to one, Output does not change | 1 | 0 | 0 | 0 |
| T at one toggles output from zero to 1 on rising edge clock | 1 | 1 | 0 | 1 |
| Clock falling edge, Output does not change | 1 | 0 | 0 | 1 |
| T at 1 toggles output from 1 to zero on rising edge clock | 1 | 1 | 0 | 0 |