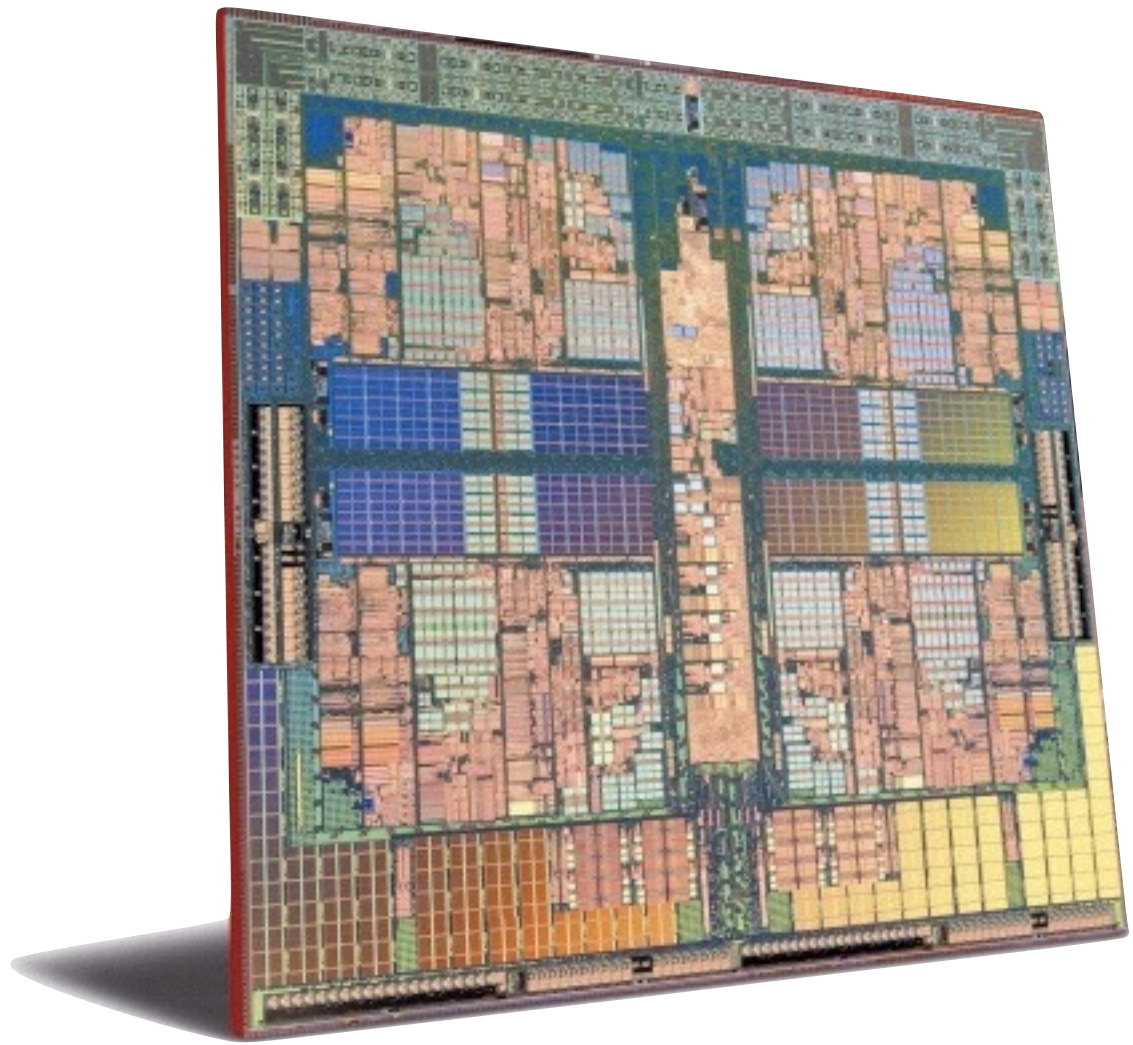

CSE 311: COMPUTER ORGANIZATION (2)

Lecture 1

Dr. Cherif Salama

THE LECTURER

- B.Sc. and M.Sc. from Ain Shams University, Egypt
- Ph.D. from Rice University, TX, USA
- Collaborated with Intel Strategic CAD Labs, OR, USA
- Worked in IBM Austin Research Labs, TX, USA
- Lectured at the EELU, the MIU, and the GUC
- Currently lecturer at ASU
- Other Research Interests
  - CAD Tools
  - GPU Computing
  - Programming Languages
  - Multistage Programming
  - Artificial Intelligence (game playing)

CONTACT INFO

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  - By Email appointment
- Teaching Assistant:
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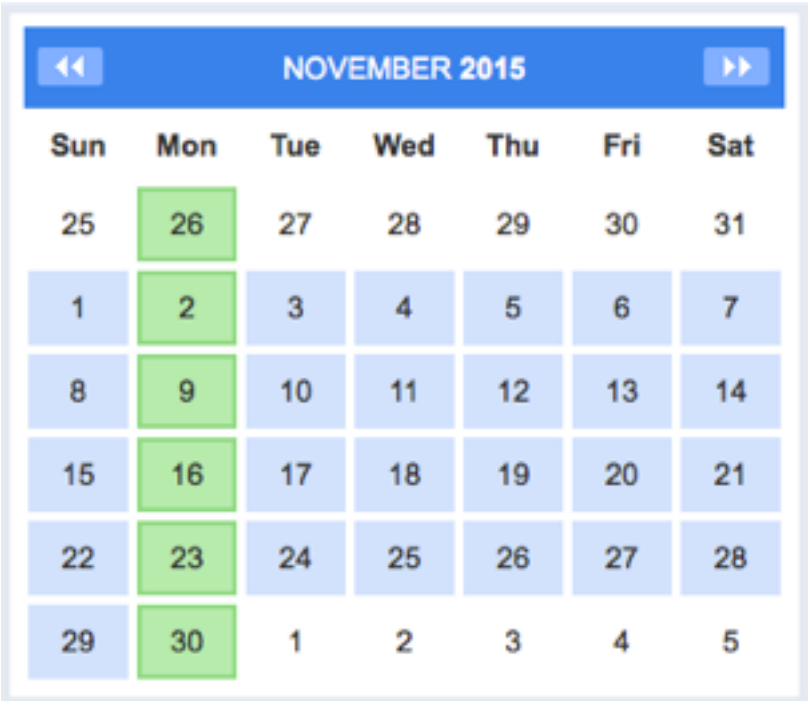
COURSE INFO

- **Lectures**:
  - 2 lectures/week
  - Monday 1st and 2nd slot
  - Location: 319
- **Tutorials**:
  - 1 session per week
  - Starting **third** week
- ***Attendance is of crucial importance***
  - Please be on time



COURSE INFO

- Textbook and reference:
  - David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 5th Edition, 2013
- Course Prerequisites:
  - CSE 211: Computer Organization (1)
- Assessment (150 marks)
  - Course Work: 40
    - Project+Report: 13+7=20
    - Midterm: 20
  - Final: 110

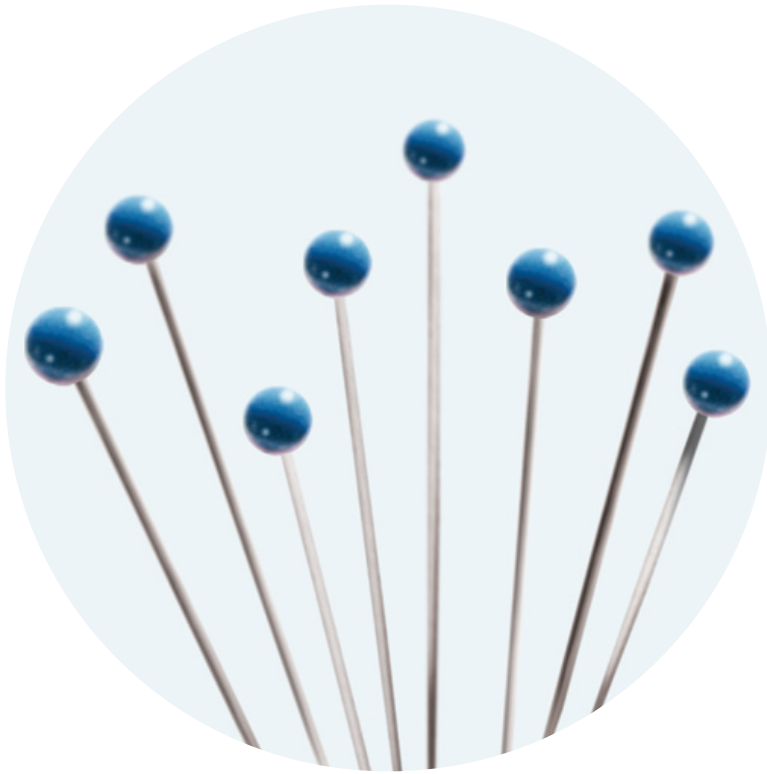
LECTURE RULES

WHY STUDY COMPUTER ORGANIZATION IN DETAILS ?

- Computers are everywhere
- Get a deeper understanding of
  - Computers inner workings
  - Factors affecting computer performance & performance metrics
- Become a better programmer
- Microprocessors architecture is simply beautiful!
- You are an engineering student

MOORE'S LAW

50 years ago (in 1965) Gordon Moore Intel co-founder observed that the number of transistors on a chip was roughly doubling every 2 years and predicted that this trend was going to continue for the 10 following years. His prediction now known as Moore's law is still valid nowadays and is expected to continue till 2025.



On the road to a billion transistors per chip, Intel has developed transistors so small that about 200 million of them could fit on the head of each of these pins.

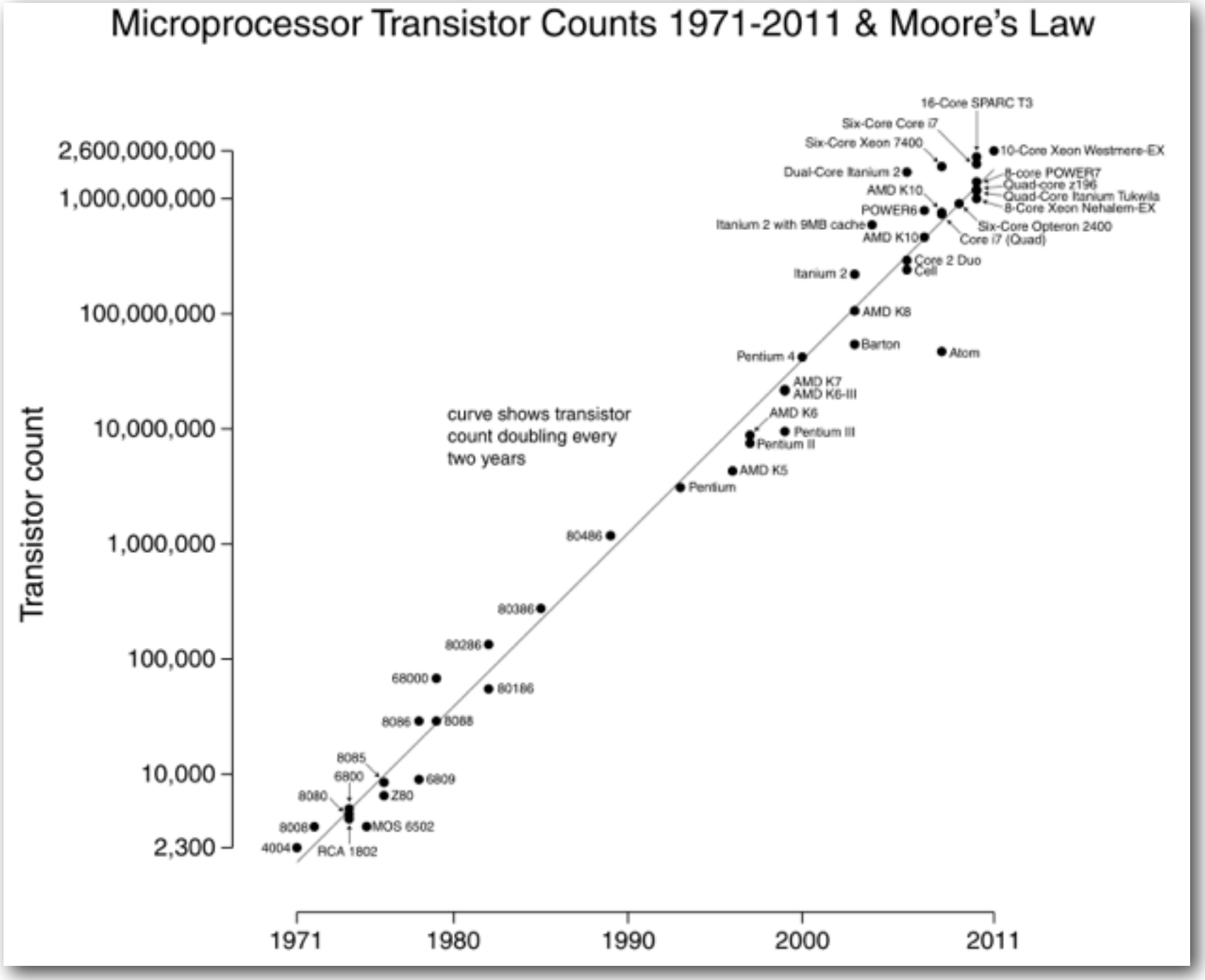
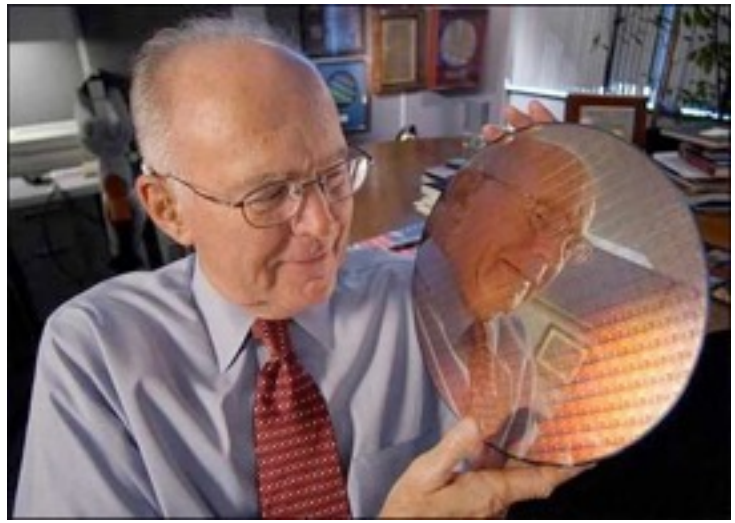


Figure from http://en.wikipedia.org/wiki/Moore's_law

MOORE'S SECOND LAW



The cost of a semiconductor chip fabrication plant doubles every four years. As of 2003, the price had already reached about 3 billion US dollars.

MICROPROCESSOR BUSINESS MODEL

- New generation of silicon technology every 2.5 to 3 years
  - 30% reduction in linear dimensions
  - 30% reduction in device delay
  - Cost reduction and performance improvement
  - Enabling new generation of microprocessors (with wider, more parallel, more functional organization)
- Business growth enables investment in new technology
  - Driven by performance and new applications

Gordon Moore estimated in 2003 that the number of transistors shipped in a year had reached about 10,000,000,000,000,000,000 (10^{18}). That's about 100 times the number of ants estimated to be in the world.

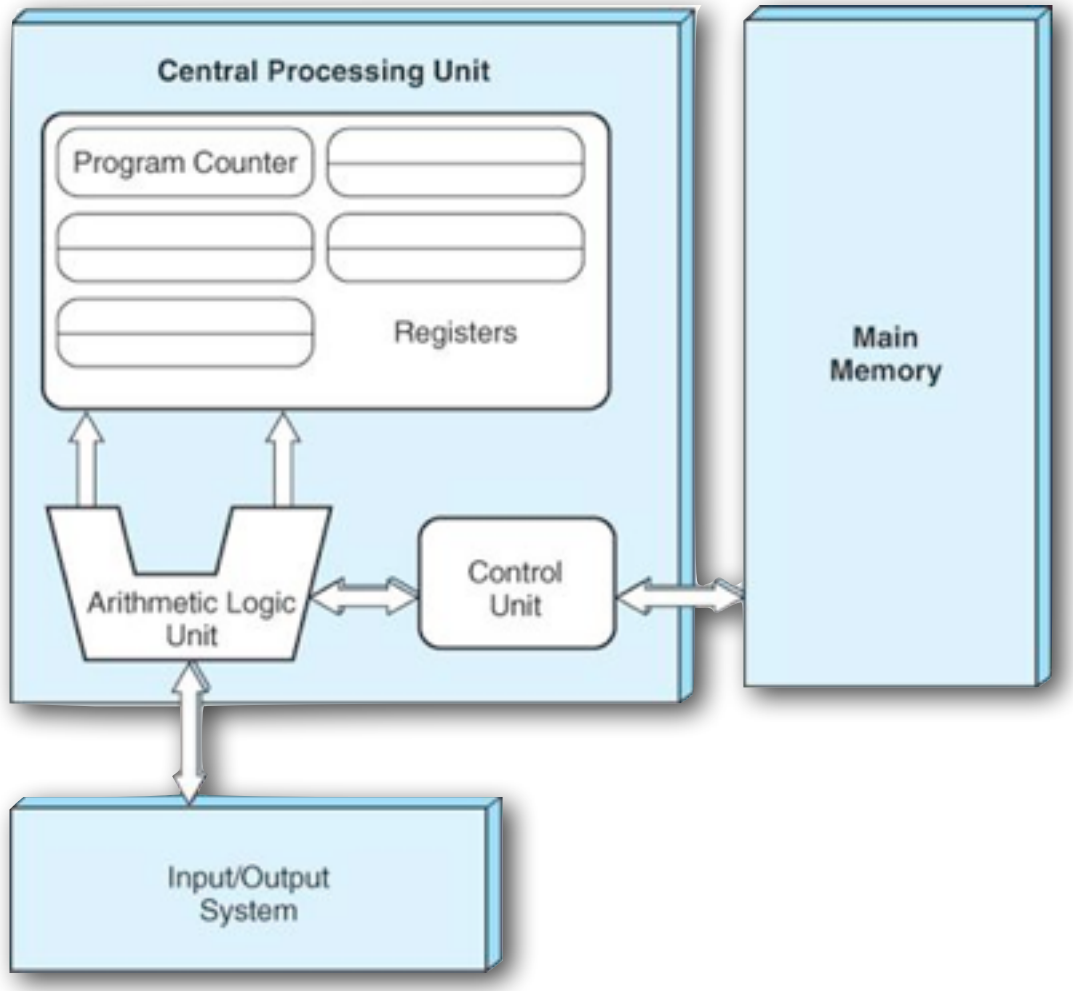
1965	1977	1998	2009
			
IBM System 360/50 0.15 MIPS 64 KB $1M $6.6M per MIPS	DEC VAX11/780 1 MIPS 1 MB $200K $200K per MIPS	Dell Dimension XPS-300 725 MIPS 64 MB $2412 (1/4/98) $3.33 per MIPS	PS3 & GPUs $500 $0.01 per MIPS

SO WHAT?

- Making use of the large number of available transistors and the impressive technological advances is crucial
- This course will show you how to do that in the context of a commercial computer
  - Pipelined MIPS implementation
  - Cache Memory
  - Virtual Memory
  - More advanced implementations (superscalar, VLIW)
  - Multiprocessors
- In addition to
  - Verilog Hardware Description Language

A QUICK REVIEW

- Von-Neumann model
- Performance Evaluation
- MIPS ISA and programming
- Simple MIPS implementation



VON-NEUMANN MODEL OF A COMPUTER

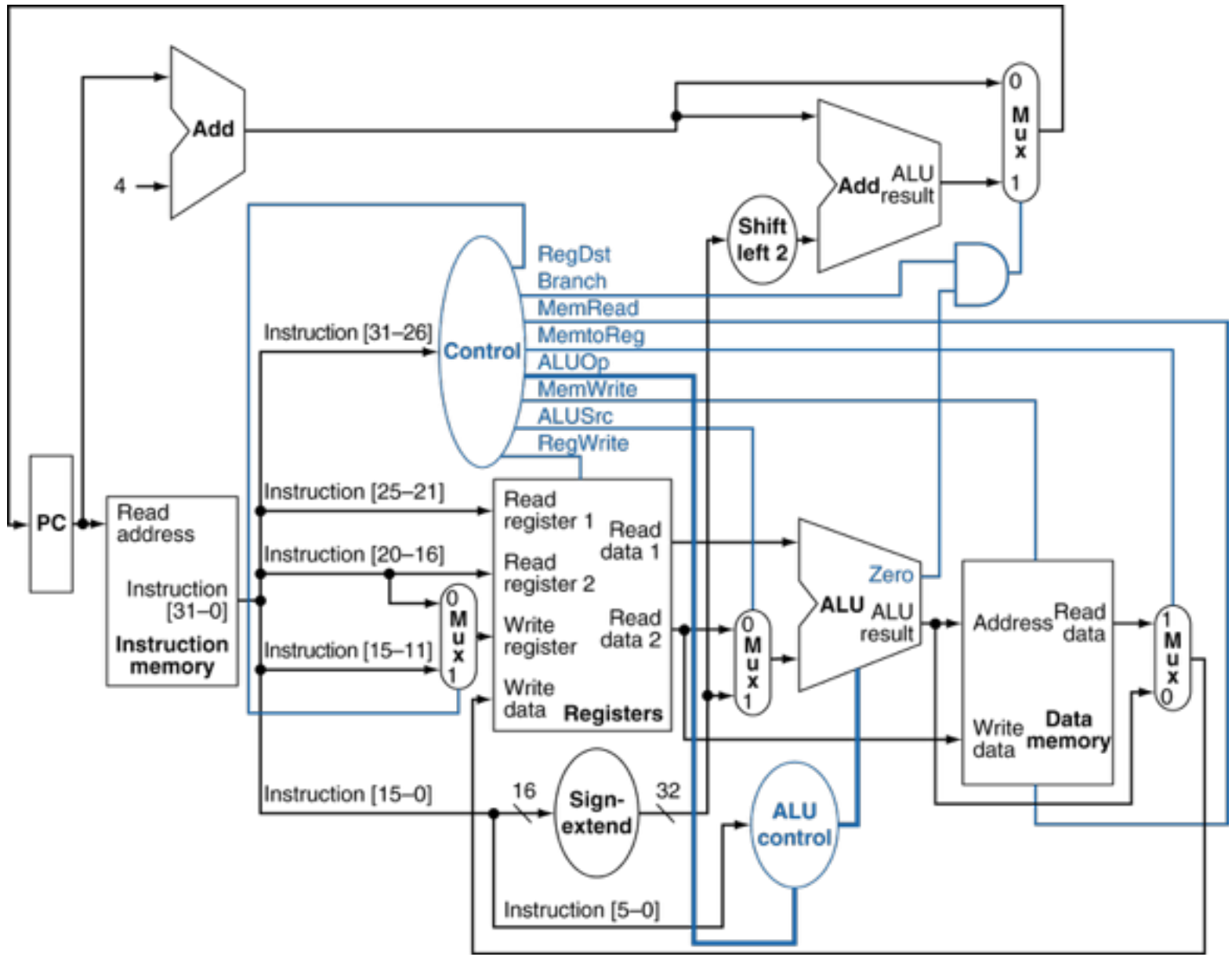
PERFORMANCE EVALUATION

- Various metrics can be used
  - Million Instructions Per Second (MIPS)
  - Clocks Per Instruction (CPI)
- In this course, we will be mostly concerned with CPI (or its reciprocal IPC) as a metric because it depends only the architecture (not the clock speed which mainly depends on the manufacturing technology)

MIPS INSTRUCTIONS

- **Instructions**
  - Arithmetic: `add, addi, sub, mul`
  - Load/Store: `lw, lh, lhu, lb, lbu, sw, sh, sb, lui`
  - Logic: `sll, srl, and, andi, or, ori, nor`
  - Control flow: `beq, bne, j, jal, jr`
  - Comparison: `slt, slti, sltu, sltui`
- **Pseudo-instructions**
  - `move, blt`
- **Registers** (32 in total) listed in numbering order
  - `$zero, $at, $v0-$v1, $a0-$a3, $t0-t7, $s0-s7, $t8-$t9, $k0-$k1, $gp, $sp, $fp, and $ra`
- **Instruction formats**
  - R-Format (`add, sub, mul, sll, srl, and, or, nor, jr, slt, sltu`), I-Format (`addi, lw, lh, lhu, lb, lbu, sw, sh, sb, lui, andi, ori, beq, bne, slti, sltui`), and J-Format (`j, jal`)

MIPS SINGLE CYCLE IMPLEMENTATION



REFERENCES

- Computer Organization and Design: The Hardware/Software Interface, Fifth Edition, Patterson and Hennessy, 2013
- Microprocessor Architecture: From simple pipelines to chip multiprocessors, Jean-Loup Baer, 2010