

## DLD LAB

1/1 अंक

SAP ID: - 60132

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Question 1:-

Design a  $1 \times 4$  and  $1 \times 8$  ....

• Components:-

1 Data Input: D.

2 Select Lines: S1, S0

3 4 outputs, Y0, Y1, Y2, Y3

4 Logic Gates Required: AND, NOT

• Logic:-

The select lines (S1, S0) determine which output

(Y0 to Y3) will receive the input signal

(D). Each output has a combination of

the select lines.

• Boolean Equation for Outputs:-

$$Y_0 = D \cdot \overline{S_1} \cdot \overline{S_0}$$

$$Y_1 = D \cdot \overline{S_1} \cdot S_0$$

$$Y_2 = D \cdot S_1 \cdot \overline{S_0}$$

$$Y_3 = D \cdot S_1 \cdot S_0$$

• Circuit Construction:-

Use NOT gates to create the inverted versions

1 / 1 25

of the select lines  $S_1$  and  $-S_0$ )

- 2- Connect the data input ( $D$ ) to each AND gate
  - 3- Use AND gates to create the conditions for each output.
  - 4- For  $Y_0$ , connect  $D$ ,  $-S_1$ , and  $-S_0$  to an AND gate
  - 5- For  $Y_1$  connect  $D$ ,  $-S_1$  and  $-S_0$  to an AND gate
  - 6- For  $Y_2$ , connect  $D$ ,  $S_1$  and  $-S_0$  to an AND gate
  - 7- For  $Y_3$ , connect  $D$ ,  $S_1$ , and  $S_0$  to one AND gate
- 1 x 8 Demultiplexer Design Components
1. 1 Data Input:  $D$
  2. 3 Select lines  $S_2$ ,  $S_1$ ,  $S_0$
  3. 8 Outputs:  $Y_0$ ,  $Y_1$ ,  $Y_2$ ,  $Y_3$ ,  $Y_4$ ,  $Y_5$ ,  $Y_6$ ,  $Y_7$

## Logic Gates Required AND, OR, NOT.

### Logic:

The select lines ( $S_2, S_1, S_0$ ) decide which output ( $Y_0$  to  $Y_7$ ) will get the input signal ( $D$ ) - Each output has a unique combination of select lines.

### Boolean Equations for Outputs.

$$Y_0 = D \cdot \overline{S_2} \cdot \overline{S_1} \cdot S_0$$

$$Y_1 = D \cdot \overline{S_2} \cdot \overline{S_1} \cdot \overline{S_0}$$

$$Y_2 = D \cdot \overline{S_2} \cdot S_1 \cdot \overline{S_0}$$

$$Y_3 = D \cdot \overline{S_2} \cdot S_1 \cdot S_0$$

$$Y_4 = D \cdot S_2 \cdot \overline{S_1} \cdot \overline{S_0}$$

$$Y_5 = D \cdot S_2 \cdot \overline{S_1} \cdot S_0$$

$$Y_6 = D \cdot S_2 \cdot S_1 \cdot \overline{S_0}$$

$$Y_7 = D \cdot S_2 \cdot S_1 \cdot S_0$$

### Circuit Construction:-

1 Use NOT gates to create the inverted versions of the select lines ( $\overline{S_2}, \overline{S_1}, \overline{S_0}$ ).

2 Connect the data input ( $D$ ) to each AND gate.

3- Use AND gates to create the conditions for each outputs

• 1 x 4 Demultiplexer logic Diagram.

Input:

D

0

1

1

2

1

3

1

D<sub>0</sub>

D<sub>1</sub>

2- Understand the operation of 1x4  
Components

1- 1 Data Input - D (the data that will be  
routed to one of the outputs).

- 2 Select lines :  $S_1$  and  $S_0$  (These determine which output is selected)
  - 3 4 Outputs  $Y_0, Y_1, Y_2, Y_3$  (Only one will be active at a time)
- How it works
- 1 The data input ( $D$ ) is the main signal you want to send to one of the four outputs ( $Y_0$  to  $Y_3$ )
  - 2 The 2 select lines ( $S_1$  and  $S_0$ ) determine which output will receive the data from  $D$  -
  - 3 Depending on the combination of  $S_1$  and  $S_0$ , one of the four outputs ( $Y_0$  to  $Y_3$ ) will be selected, and the data from  $D$  will appear on that output -
  - 4. The rest of the outputs will be 0 (inactive)

1 x 8 Demultiplexer :-

Component :

- 1- 1 Data Input : D (the main input signal)
- 2- 3 Select Lines, S<sub>2</sub>, S<sub>1</sub>, S<sub>0</sub> (used to choose one of the eight outputs)
- 3- 8 outputs : Y<sub>0</sub>, Y<sub>1</sub>, Y<sub>2</sub>, Y<sub>3</sub>, Y<sub>4</sub>, Y<sub>5</sub>, Y<sub>6</sub>, Y<sub>7</sub>  
(only one will be active at a time)

- How It Works:-

- 1- The data input (D) is the signal that you want to send to one of the eight outputs.
- 2- The 3 select lines (S<sub>2</sub>, S<sub>1</sub>, S<sub>0</sub>) are used to select which output will receive the data.
- 3- The output is chosen based on the binary combination of the select lines.
- 4- Only one output will be active and receive the data from D, while the rest will be 0 (inactive).

- Implementing a Boolean Function -----

$$F(A, B) = \sum_m(1, 3)$$

2- Use a 1x4 Demultiplexer

1 Data Input (D) : Set to 1 because the data has to go to all four outputs.

to the correct output.

2 Select Lines (A, B).

These lines will determine which output is activated.

4 Outputs ( $Y_0, Y_1, Y_2, Y_3$ ).

3 - Connect the Select lines:-

A and B will be connected to the select lines of the  $1 \times 4$  demultiplexer.

The demultiplexer will use these select lines to determine which output gets the input signal.

4 Activate Required Outputs:-

The function  $F(A \cdot B) = \sum m(1, 3)$  means

we need outputs  $Y_1$  and  $Y_3$  to be active.

$Y_1$ : Activated when  $A = 0$  and  $B = 1$ .

$Y_3$ : Activated when  $A = 1$  and  $B = 1$

5 Connections:-

Connect Output  $Y_1$  and  $Y_3$  to an OR gate.

• 1x4 Demultiplexer Table:-

A	B	Output Active	$y_0$	$y_1$	$y_2$	$y_3$
0	0	$y_0$	1	0	0	0

1- Tasks.

Boolean Function - - 1x8 - -

A 1x8 demultiplexer has 1 data input.

(D), 3 select lines ( $s_2, s_1, s_0$ ) and 8 outputs

( $y_0$  to  $y_7$ ) -

$$y_0 = D \cdot \overline{s_2} \cdot \overline{s_1} \cdot \overline{s_0}$$

$$y_1 = D \cdot \overline{s_2} \cdot \overline{s_1} \cdot s_0$$

$$y_2 = D \cdot \overline{s_2} \cdot s_1 \cdot \overline{s_0}$$

$$y_3 = D \cdot \overline{s_2} \cdot s_1 \cdot s_0$$

$$y_4 = D \cdot s_2 \cdot \overline{s_1} \cdot \overline{s_0}$$

$$y_5 = D \cdot s_2 \cdot \overline{s_1} \cdot s_0$$

$$y_6 = D \cdot s_2 \cdot \overline{s_1} \cdot \overline{s_0}$$

$$y_7 = D \cdot s_2 \cdot s_1 \cdot \overline{s_0}$$

Each output is combination of the select lines  
and the data input - .

2- Difference b/w Multiplexer - - -

1. Multiplexer (MUX) :-

Combines multiple inputs into a single output.

Uses select lines to choose which input is connected to the output.

2. Demultiplexer (DEMUX) :-

Takes a single input and distributes it to multiple outputs.

Uses select lines to choose which output receives the input.

3- How to find - - -

To find the number of select lines ( $n$ )

For a demultiplexer -

$2^n = \text{number of outputs}$

So,  $n = \log_2 (\text{number of outputs})$

For example, for a  $1 \times 8$  demultiplexer

there are 8 outputs.  $2^n = 8 \rightarrow n=3$ .

Therefore 3 times select lines are needed.

5- Number of AND gates - - -

A  $1 \times 8$  multiplexer needs 8 input lines and

3 select lines.

The total number of AND gates required is 8,

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where each AND gate handles one combination  
of select lines and the data inputs

•  $1 \times 8$  demultiplexer diagram :-

