# [Half Adder]

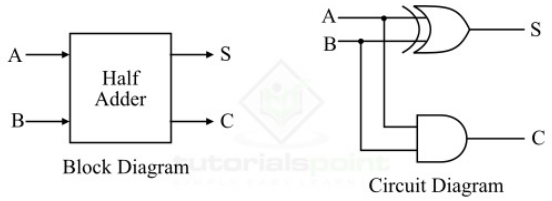



Figure 1 - Half Adder

**RTL**

```
// ================================
// Half Adder Module
// This module performs the basic half-adder logic,
// which computes the sum and carry-out of two 1-bit binary inputs.
// ================================
module half_adder (A, B, S, C);
  input wire A,B;   // A: First input bit, B: Second input bit
  output wire S,C;  // S(sum): XOR of A and B, C(carry): AND of A and B

  // Logic for sum and carry
  // assign {C, S} = A + B;
  // assign {C, S} = {A & B, A ^ B};
  assign S = A ^ B;
  assign C = A & B;
endmodule
```

**TB**

```
// ================================
// Testbench for the half_adder module
// This module applies all possible combinations of 1-bit inputs (a, b)
// and observes the outputs sum and carry.
// ================================
module half_adder_tb;
    reg net_test_a, net_test_b;
    wire net_test_sum, net_test_carry;

    // Instantiate the Device Under Test (DUT)
    half_adder uut (
      .A(net_test_a),
      .B(net_test_b),
      .S(net_test_sum),
      .C(net_test_carry)
    );

    // Initial block to perform test cases
    initial begin
      // Create VCD file for waveform analysis
      $dumpfile("dump.vcd");
      $dumpvars;

      $display("HA - Half Adder Test Results");
      $display("-------------------------------");

      // Display signal values at every change
      $monitor("Time=%0t, a=%b, b=%b, sum=%b, carry=%b", $time, net_test_a, net_test_b, net_test_sum, net_test_carry);

      // Apply 4 input combinations
```

```
    net_test_a = 1'b0; net_test_b = 1'b0; #10;
    net_test_a = 1'b0; net_test_b = 1'b1; #10;
    net_test_a = 1'b1; net_test_b = 1'b0; #10;
    net_test_a = 1'b1; net_test_b = 1'b1; #10;

    // End simulation
    $finish;
  end
endmodule
```

---

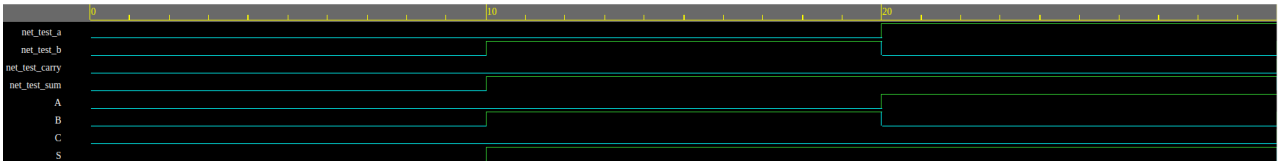
## Simulation Result by EDA playground

Log | Share

```
# run -all
# HA - Half Adder Test Results
# ------------------------------
# Time=0, a=0, b=0, sum=0, carry=0
# Time=10, a=0, b=1, sum=1, carry=0
# Time=20, a=1, b=0, sum=1, carry=0
# Time=30, a=1, b=1, sum=0, carry=1
# ** Note: $finish    : testbench.sv(37)
#    Time: 40 ns  Iteration: 0  Instance: /half_adder_tb
# End time: 09:41:05 on Jun 13,2025, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
End time: 09:41:05 on Jun 13,2025, Elapsed time: 0:00:01
```

Playground | https://edaplayground.com/x/AzPh | From: 0ns | To: 30ns

gnals | Radix | 100% | 30ns

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## Run QuestaSim by Makefile

```
meynchan@MEYNCHAN: ~/Documents/HalfAdder_MakeFile
meynchan@MEYNCHAN: ~/Documents/run_QuestaSim_by_Makefile
meynchan@MEYNCHAN: ~/Documents/HalfAdder_MakeFile
meynchan@MEYNCHAN:~/Documents/HalfAdder_MakeFile$ make all
mkdir -p log
touch run_test.vt
vlib work
** Warning: (vlib-34) Library already exists at "work".
Errors: 0, Warnings: 1
vmap work work
Questa Intel Starter FPGA Edition-64 vmap 2023.4 Lib Mapping Utility 2023.10 Oct  9 2023
vmap work work
Modifying modelsim.ini
vlog -coveropt 3 +cover +acc -f compile.f
Questa Intel Starter FPGA Edition-64 vlog 2023.4 Compiler 2023.10 Oct  9 2023
Start time: 00:59:24 on Jun 17,2025
vlog -coveropt 3 "+cover" "+acc" -f compile.f
-- Compiling module half_adder
-- Compiling module half_adder_tb

Top level modules:
        half_adder_tb
End time: 00:59:25 on Jun 17,2025, Elapsed time: 0:00:01
Errors: 0, Warnings: 0
vlog  -f compile.f
Questa Intel Starter FPGA Edition-64 vlog 2023.4 Compiler 2023.10 Oct  9 2023
Start time: 00:59:25 on Jun 17,2025
vlog -f compile.f
-- Compiling module half_adder
-- Compiling module half_adder_tb

Top level modules:
        half_adder_tb
End time: 00:59:25 on Jun 17,2025, Elapsed time: 0:00:00
Errors: 0, Warnings: 0
vsim -l default_value_test.log -voptargs=+acc -assertdebug -c half_adder_tb -do "log -r /*; run -all;"
Reading pref.tcl

# 2023.4

# vsim -l default_value_test.log -voptargs="+acc" -assertdebug -c half_adder_tb -do "log -r /*; run -all;"
# Start time: 00:59:25 on Jun 17,2025
```

meynchan@MEYNCHAN: ~/Documents/HalfAdder_MakeFile

meynchan@MEYNCHAN: ~/Documents/run_QuestaSim_by_Makefile | meynchan@MEYNCHAN: ~/Documents/HalfAdder_MakeFile

```
# ** Note: (vsim-3812) Design is being optimized...
# ** Warning: (vopt-10587) Some optimizations are turned off because the +acc switch is in effect. This will cause your simulation to run slowly. Please use -access/-debug to maintain needed
 visibility.
# ** Note: (vsim-12126) Error and warning message counts have been restored: Errors=0, Warnings=1.
# //  Questa Intel Starter FPGA Edition-64
# //  Version 2023.4 linux_x86_64 Oct  9 2023
# //
# //  Copyright 1991-2023 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  QuestaSim and its associated documentation contain trade
# //  secrets and commercial or financial information that are the property of
# //  Mentor Graphics Corporation and are privileged, confidential,
# //  and exempt from disclosure under the Freedom of Information Act,
# //  5 U.S.C. Section 552. Furthermore, this information
# //  is prohibited from disclosure under the Trade Secrets Act,
# //  18 U.S.C. Section 1905.
# //
# Loading work.half_adder_tb(fast)
# Loading work.half_adder(fast)
# log -r /*
#  run -all
# HA - Half Adder Test Results
# -------------------------------
# Time=0, a=0, b=0, sum=0, carry=0
# Time=10, a=0, b=1, sum=1, carry=0
# Time=20, a=1, b=0, sum=1, carry=0
# Time=30, a=1, b=1, sum=0, carry=1
# ** Note: $finish    : tb/ha_tb.v(37)
#    Time: 40 ns  Iteration: 0  Instance: /half_adder_tb
# End time: 00:59:25 on Jun 17,2025, Elapsed time: 0:00:00
# Errors: 0, Warnings: 1
mv default_value_test.log ./log
cp -rf vsim.wlf default_value_test.wlf
mv default_value_test.wlf ./log
ln -sf ./log/default_value_test.log sim.log
meynchan@MEYNCHAN:~/Documents/HalfAdder_MakeFile$ make wave
vsim -i -view vsim.wlf -do "add wave vsim:/half_adder_tb/*; radix -hexadecimal"
Reading pref.tcl
```

QuestaIntel Starter FPGA Edition-64 2023.4 (WLF View)