Document Information	
Project Title	SINGLE 8-BIT TIMER (TMR)
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Last Modified	August 1st, 2025
Version	1.0

SINGLE 8-BIT TIMER (TMR)

Synchronous design with APB interface

1. OVERVIEW

1.1. Feature

8-bit Timer is a general-purpose, single-channel module with the following key features:

8-bit Single-Channel Counter Compact timer module featuring one 8-bit counter, suitable for general-purpose timing applications.

Selection of Four external clock sources Offers four external clock inputs derived from the main system clock (PCLK)

CLK_IN [0] (= PCLK/2)
CLK_IN [1] (= PCLK/4)
CLK_IN [2] (= PCLK/8)
CLK_IN [3] (= PCLK/16)

Edge-Triggered Counting Counter increments or decrements on each rising edge of the selected clock source.

Counter Initialization Counter value can be loaded from Timer Data Register (TDR) when TCR[7] = 1 is set.

Counters can operate in different modes

Up Count: Increments by 1 on each clock cycle
Down Count: Decrements by 1 on each clock cycle

Control and Status Registers Configurable through control (TCR) and status (TSR) registers to manage and monitor timer behavior, such as enabling the counter, setting modes, or detecting overflow/underflow.

1.2. Block diagram

A Timer Module in its most basic form is a digital logic circuit that counts up or counts down every clock cycle. This Timer module consists of the following key blocks:

Read/Write Register Control (APB Interface)
Clock Select
Control Logic
Counter Unit
Overflow/Underflow Comparator

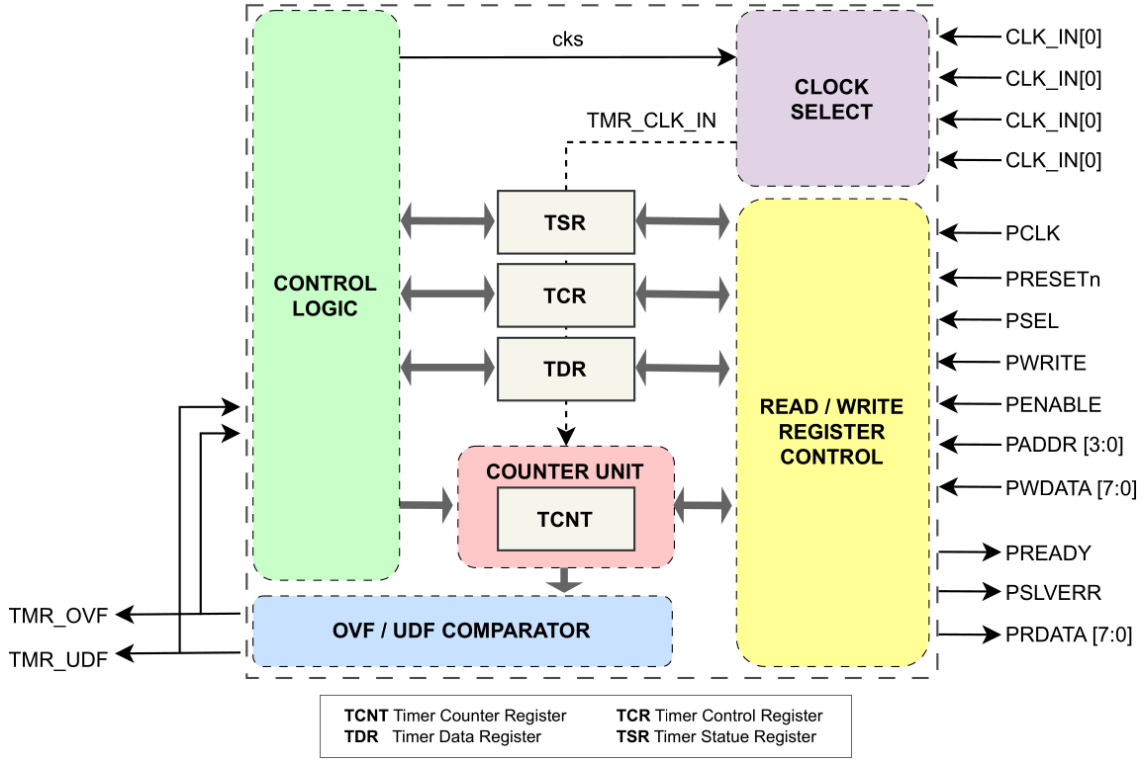


Figure 1.1. 8-bit Timer Block Diagram

1.3. Input/Output Pins

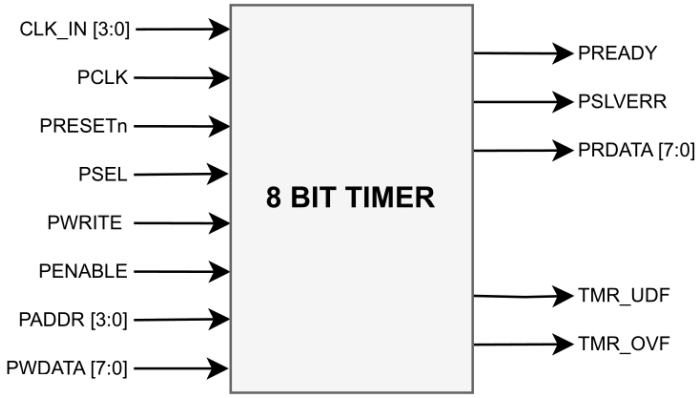


Figure 1.2. 8-bit Timer Input/Output Pin

Below table shows the Input and Output Pins configuration of the TMR.

Table 1.1. TMR Input Pins Configuration

Port Name	Bit Width	I/O	Description
CLK_IN[3:0]	4	Input	Clock for counting
PCLK	1	Input	Provided System clock for APB protocol
PRESETn	1	Input	Asynchronous reset is low active
PSEL	1	Input	Chip select is high active for the transfer
PWRITE	1	Input	PWRITE indicates an APB write access when HIGH

			and an APB read access when LOW.
PENABLE	1	Input	The enable signal is deasserted at the end of the transfer
PADDR	3	Input	Address is used to select the registers
PWDATA	8	Input	Data is used to update selected registers
PRDATA	8	Output	Read bus is used for reading data from register
PREADY	1	Output	PREADY signal from the slave can extend the Transfer
PSLVERR	1	Output	Indicate an error condition on an APB transfer
TMR_OVF	1	Output	Provided timer counter status when counter count up from 8'H00 to 8'HFF (counter reaches 8'HFF)
TMR_UDF	1	Output	Provided timer counter status when counter count down from 8'HFF to 8'H00 (counter reaches 8'H00)

1.4. Register specification

The TMR module has 4 configuration registers.

Table 1.2. Configuration Registers

Offset	Register Name	Description	Bit Width	Access	Reset value
0x0	Timer Data Register **TDR**	Value to load into TCNT	8	R/W	0
0x1	Timer Control Register **TCR**	Control signals	8	R/W	0
0x2	Timer Status Register **TSR**	Status flags	8	R/W	0
0x3	Timer Counter **TCNT**	Current counter value	8	R	0

1.4.1. Timer Counter (TCNT)

TCNT is an 8-bit readable counter that holds the current count value.
Initialized to 8'h00 and cleared by an external reset signal PRESETn.
If TCR[7] = 1, TCNT is loaded with value from TDR; otherwise, normal counting continues.
Up-counting mode: counts up to H'FF, then wraps to H'00; sets TMR_OVF = 1.
Down-counting mode: counts down to H'00, then wraps to H'FF; sets TMR_UDF = 1.

Table 1.3. TCNT - Bit Description

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	|	|	|	|	|	|	|	|
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

1.4.2. Timer Data Register (TDR)

TDR is an 8-bit readable/writable register that holds the initial value to be loaded into TCNT.
Initialized to 8'h00 and cleared by an external reset signal PRESETn.
When bit TCR[7] = 1, the value in TDR is loaded into TCNT at the start of counting.
If the value of this register is changed, its new value is updated to TCNT immediately

Table 1.4. TDR - Bit Description

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	|	|	|	|	|	|	|	|
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1.4.3. Timer Control Register (TCR)

The TCR is an 8-bit read/write register that controls the operation mode of the timer.
Initialized to 8'h00 and cleared by an external reset signal PRESETn.
It allows selection of the internal clock source and controls various operational settings for TCNT, such as count direction, enable/disable, and manual data loading.
Each bit has a specific function, as described in the tables below.

Table 1.5. TCR - Bit Description

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	**Load**	**Reserved**	**Up/Dw**	**En**	**Reserved**	**Reserved**	**cks1**	**cks0**
Initial Value	0	0	0	0	0	0	0	0
R/W	R/W	R	R/W	R/W	R	R	R/W	R/W

Table 1.6. TCR - Bit Description

Bit	**Bit Name**	**R/W**	**Description**
TCR[7]	**Load**	R/W	When set to 1, the value in TDR is immediately loaded into TCNT. When 0, normal counting operation continues.
TCR[6]	**Reserved**	R	Reserved bit. Should be written as 0.
TCR[5]	**Up/Dw**	R/W	Counter direction control: 0: Count up (increment). 1: Count down (decrement).
TCR[4]	**En**	R/W	Timer enable control: 0: Disable the timer. 1: Enable the timer.

TCR[3:2]	**Reserved**	R	Reserved bits. Should be written as 00.
TCR[1:0]	**cks[1:0]**	R/W	These bits select internal clock input for timer: 00 : Tx2 01 : Tx4 10 : Tx8 11 : Tx16

1.4.4. Timer Status Register (TSR)

The TSR is an 8-bit status register that indicates overflow and underflow events of the timer counter (TCNT). Initialized to 8'h00 and cleared by an external reset signal PRESETn.

Table 1.7. TSR - Bit Description

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**TMR_UDF**	**TMR_OVF**
Initial Value	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R/W	R/W

Table 1.8. TSR - Bit Description

Bit	Bit Name	R/W	Description
TSR[7:2]	**Reserved**	R	Reserved bit. Should be written as 0.
TSR[1]	**TMR_UDF**	R/W*	Set to 1 when TCNT underflows from 8'H00 to 8'HFF (down-counting) This bit is only set by hardware, clear by software
TSR[0]	**TMR_OVF**	R/W*	Set to 1 when TCNT overflows from 8'HFF to 8'H00 (up-counting) This bit is only set by hardware, clear by software

2. READ/WRITE REGISTER CONTROL

2.1. Input/Output pin

Table 2.1. Pin Configuration

Port Name	Bit Width	I/O	Description
PCLK	1	Input	Clock. The rising edge of PCLK times all transfers on the APB.
PRESETn	1	Input	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PADDR	3	Input	Address. This is the APB address bus. It is driven by the peripheral bus bridge unit.

PSELx	1	Input	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a PSELx signal for each slave.
PENABLE	1	Input	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	1	Input	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PWDATA	8	Input	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH.
PREADY	1	Output	Ready. The slave uses this signal to extend an APB transfer.
PRDATA	8	Output	Read Data. The selected slave drives this bus during read cycles when PWRITE is LOW.
PSLVERR	1	Output	Slave error. This signal indicates a transfer failure.

2.2. Functional/Protocol

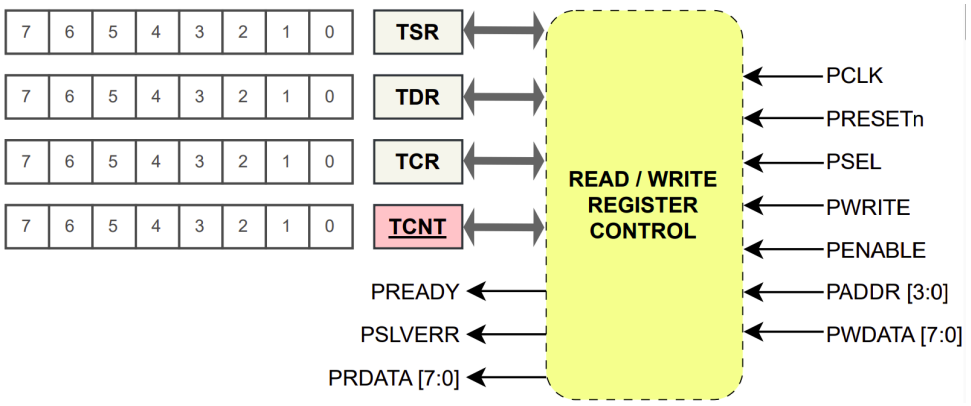


Figure 2.1. State diagram

This module uses the AMBA 3 APB (Advanced Peripheral Bus) protocol to access internal control and status registers such as TCR, TCNT, TDR, and TSR. APB is a low-power, low-complexity bus interface, ideal for simple peripheral register access that does not require high-speed pipelining.

The APB3 interface ensures compatibility with standard AMBA-based systems and allows seamless integration with higher-performance buses like AHB-Lite or AXI via bus bridges. All data transactions occur on the rising edge of the clock, making timing predictable and simplifying integration.

This protocol enables efficient and straightforward communication between the processor and the timer peripheral.

The module supports the following APB3 signals:

PADDR - address bus PWDATA - write data bus PRDATA - read data bus
PWRITE - write enable PSEL- slave select PENABLE - enable transfer
PREADY - slave ready PSLVERR - slave error indicator

2.3. State machine control for APB protocol

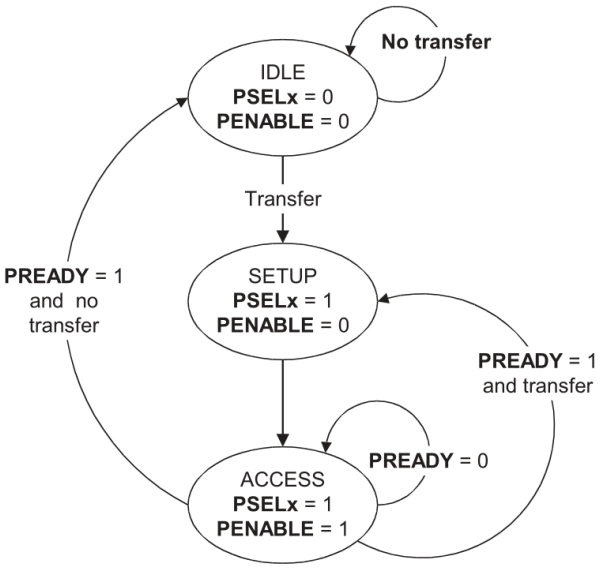


Figure 2.2. State diagram

The state machine operates through the following states:

IDLE	This is the default state of the APB.
SETUP	When a transfer is required, the interface moves into the SETUP state, where the appropriate select signal, PSELx, is asserted. The interface only remains in the SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock.
ACCESS	The enable signal, PENABLE, is asserted in the ACCESS state. The address, write, select, and write data signals must remain stable during the transition from the SETUP to ACCESS state. Exit from the ACCESS state is controlled by the PREADY signal from the slave. If PREADY is held LOW by the slave then the peripheral bus remains in the ACCESS state. If PREADY is driven HIGH by the slave then the ACCESS state is exited and the bus returns to the IDLE state if no more transfers are required. Alternatively, the bus moves directly to the SETUP state if another transfer follows.

2.4. Design circuit

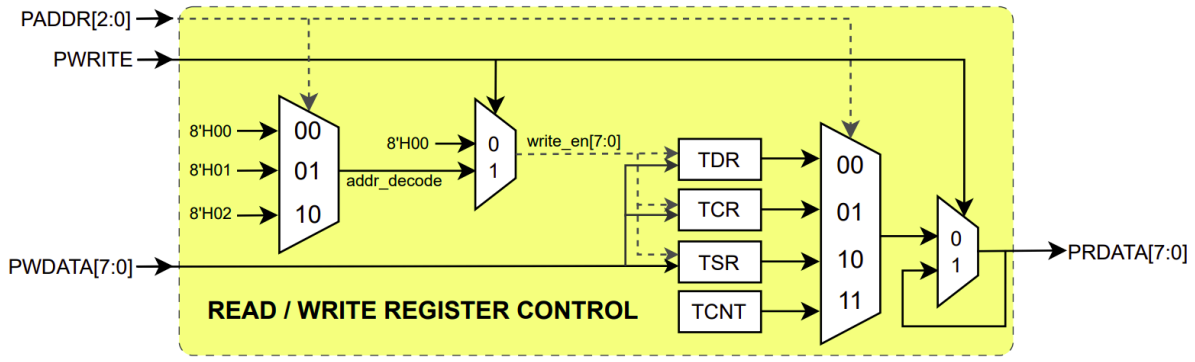


Figure 2.3. READ/WRITE REGISTER CONTROL Circuit

2.5. Timing chart

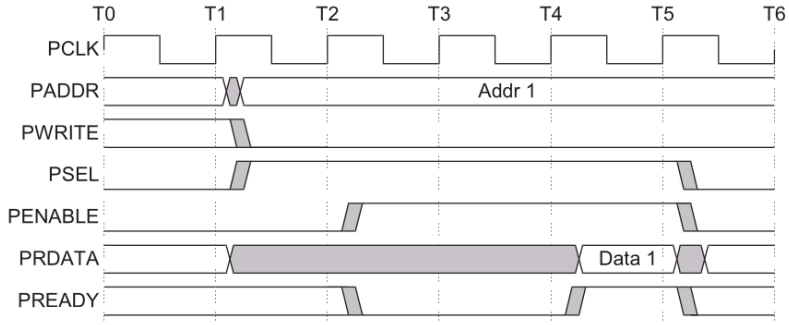


Figure 2.4. Read transaction with wait state

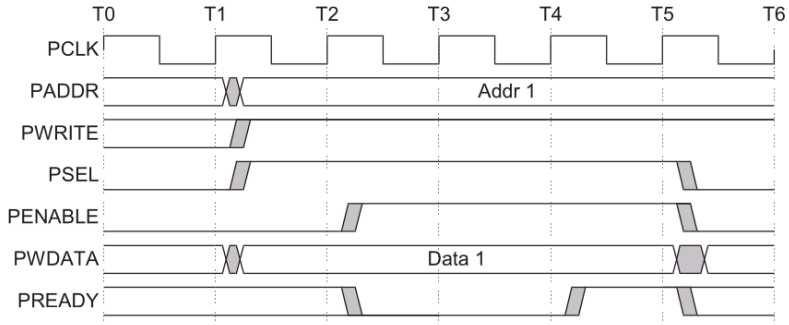


Figure 2.5. Write transaction with wait state

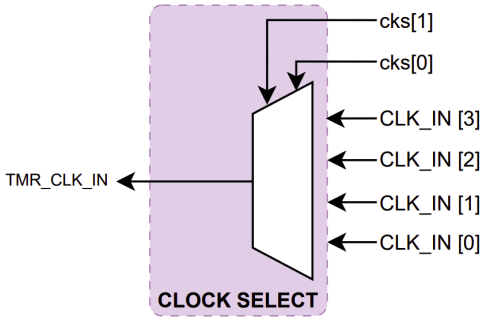
3. CLOCK SELECT

3.1. Input/Output pin

Table 3.1. Pin Configuration

Signal name	I/O	Description
CLK_IN[3:0]	Input	4 external clock sources. The selected clock source depends on the value of TCR[1:0].
cks[1:0]	Input	Clock select bits from the TCR. These two bits determine which one of the CLK_IN[3:0] signals is selected as the input clock (TMR_CLK_IN) for the timer.
TMR_CLK_IN	Output	Selected clock output used as the timer's input clock

3.2. Functional/Protocol



CLOCK SELECT Block diagram

This block selects one clock signal among multiple inputs (CLK_IN[3:0]) based on a 2-bit selector (TCR[1:0]).

Figure 3.2.

3.3. Design circuit

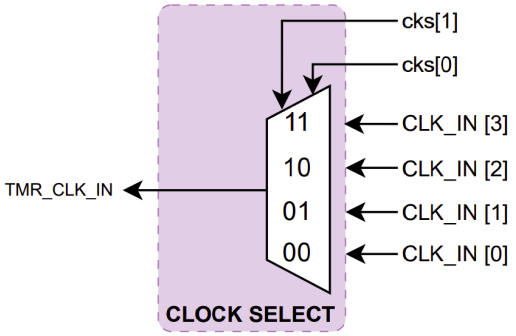


Figure 3.3. CLOCK SELECT Circuit

3.4. Timing chart

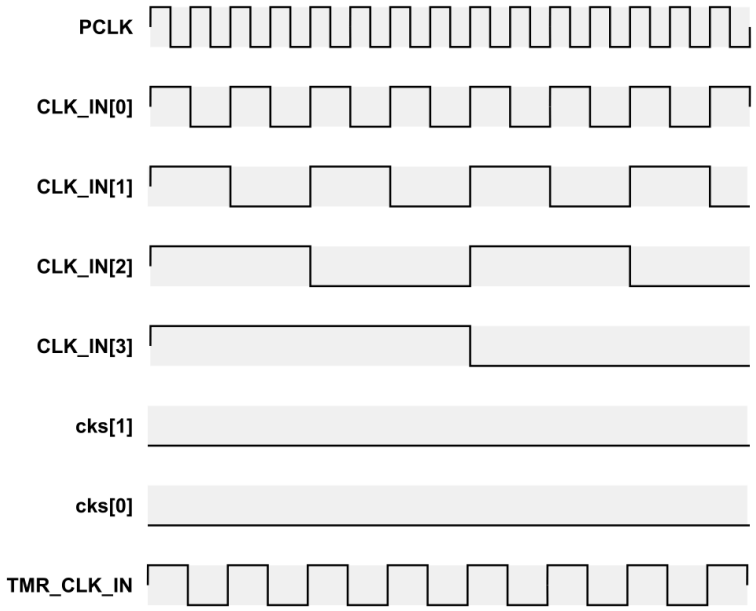


Figure 3.4. CLOCK SELECT Timing chart

4. CONTROL LOGIC

4.1. Input/Output pin

Table 4.1. Pin Configuration

Signal name	I/O	Description
TCR	Input	Timer Control Register – provides control settings such as clock selection, enable bits, etc.
TDR	Input	Timer Data Register – holds the value to compare with the timer counter (for overflow/underflow detection).
count_start_value	Output	Initial value to load into TCNT
count_up_down	Output	Signal indicating count direction: 0 for Count up and 1 for Count down.
count_enable	Output	Signal to enable counting
TMR_OVF	Input	Overflow interrupt/event signal triggered when the counter

		matches overflow condition.
TMR_UDF	Input	Underflow interrupt/event signal triggered when the counter matches underflow condition.
cks[1:0]	Output	Clock select bits from the TCR. These two bits determine which one of the CLK_IN[3:0] signals is selected as the input clock (TMR_CLK_IN) for the timer.

4.2. Functional/Protocol

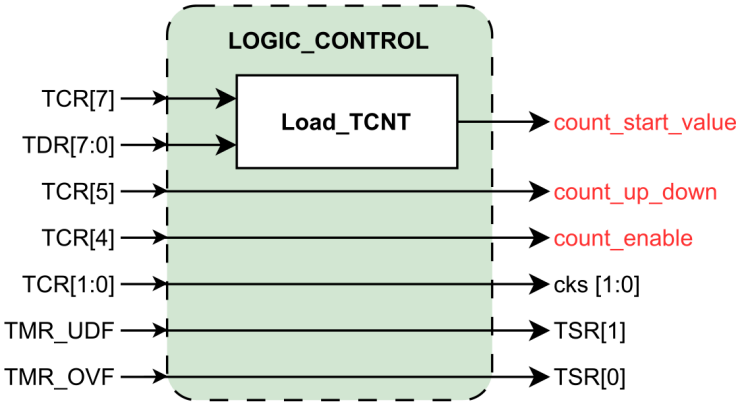


Figure 4.1. CONTROL LOGIC Block diagram

Logic Control Block manages core timer operations based on TCR and TDR inputs.
It handles:
- Counter load from TDR when Load bit in TCR = 1; otherwise, normal counting (up/down).
- Count direction via UpDw bit in TCR: 0 for count up and 1 for count down.
- Enable counter control when the Enable bit in TCR is asserted.
- Overflow/underflow detection, setting TMR_OVF or TMR_UDF, and updating TSR[1:0].
- Clock source selection via cks[1:0] bits from TCR.
- Ensures register synchronization for reliable timer control.

4.3. Design circuit

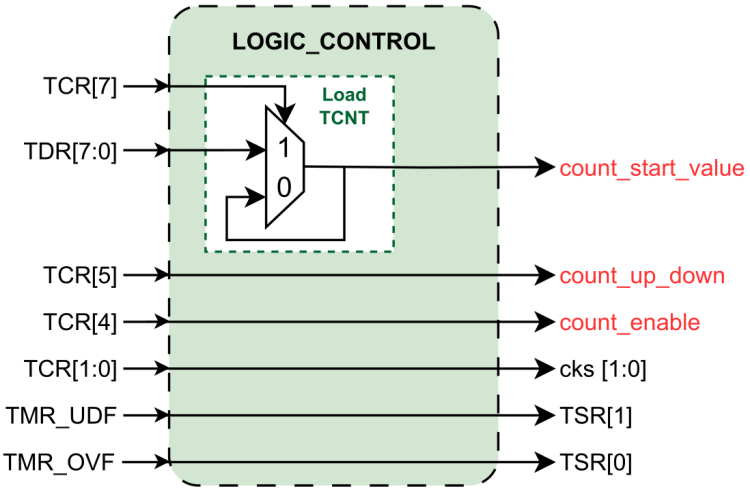


Figure 3.2. LOGIC CONTROL circuit

4.4. Timing chart

A timing diagram is not necessary for the LOGIC_CONTROL block because it operates solely on combinational logic. This means the output signals update instantly in response to input changes, without the need for clock synchronization.

5. COUNTER UNIT

5.1. Input/Output pin

Table 5.1. Pin Configuration

Signal name	I/O	Description
PCLK	Input	System clock
TMR_CLK_IN	Input	Selected clock output used as the timer's input clock.
PRESETn	Input	The reset signal is active LOW.
count_start_value	Input	Input value to initialize the timer counter when loading is requested.
count_load	Input	When set to 1, the value in TDR is immediately loaded into TCNT. When 0, normal counting operation continues.
count_enable	Input	Enables the counting process when asserted.
count_up_down	Input	Selects the counting direction: 0 for Count up and 1 for Count down.
TCNT	Output	Current value of the timer/counter, updated based on clock edges and controls.

5.2. Functional/Protocol

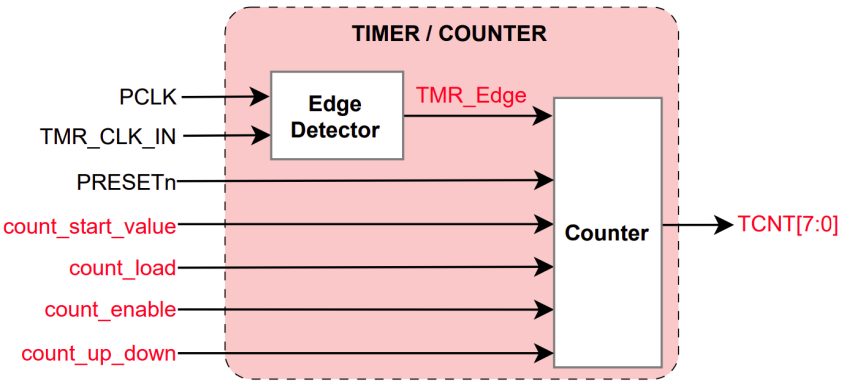


Figure 5.1. COUNTER UNIT Block diagram

The COUNTER UNIT unit performs up/down counting based on control inputs from the Control Logic. It operates synchronously with the TMR_Edge signal, generated from the selected clock via the Clock Select block.

Functional overview:

- TCNT resets to 0 when PRESETn = 0.
- If count_enable = 1, counting begins:

count_up_down = 0: counter increments on each TMR_Edge.
count_up_down = 1: counter decrements on each TMR_Edge

- When count_load = 1, the counter loads count_start_value from TDR.
- Output TCNT[7:0] reflects the current counter value.
- Overflow and underflow events are detected and trigger TMR_OVF or TMR_UDF flags.
- These flags are stored in the Timer Status Register (TSR) for software access.

5.3. Design circuit

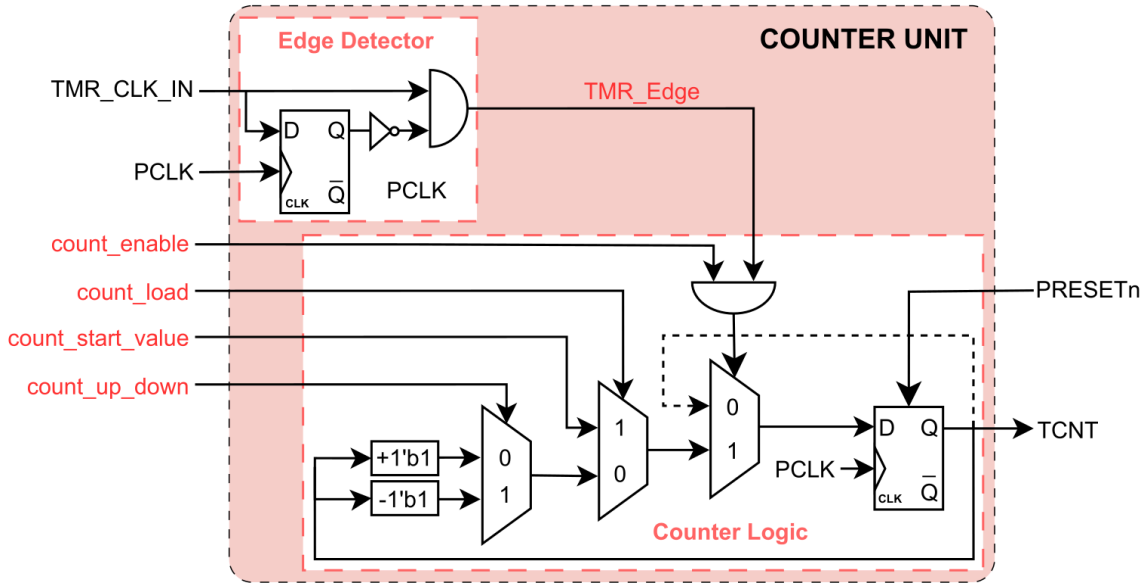


Figure 5.2. COUNTER UNIT circuit

5.4. Timing chart

Detect Rising Edge

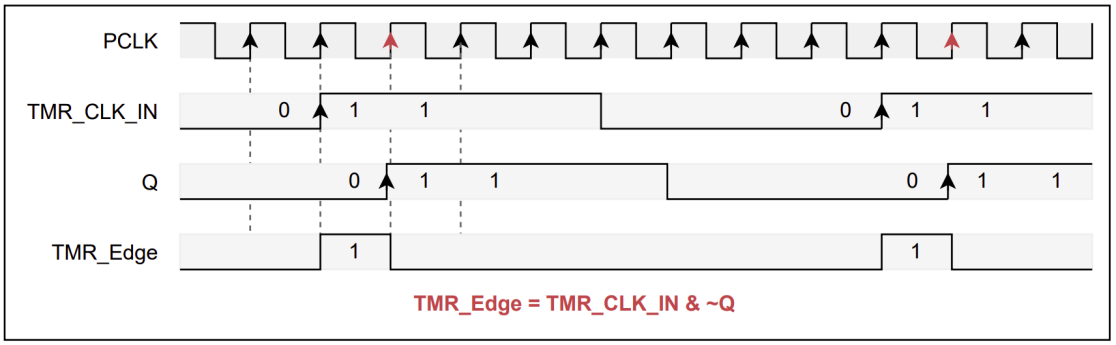


Figure 5.3. Detect Rising Edge Timing chart

TCNT Count up Timing

Figure 6.1. shows the TCNT count up timing for internal clock input.

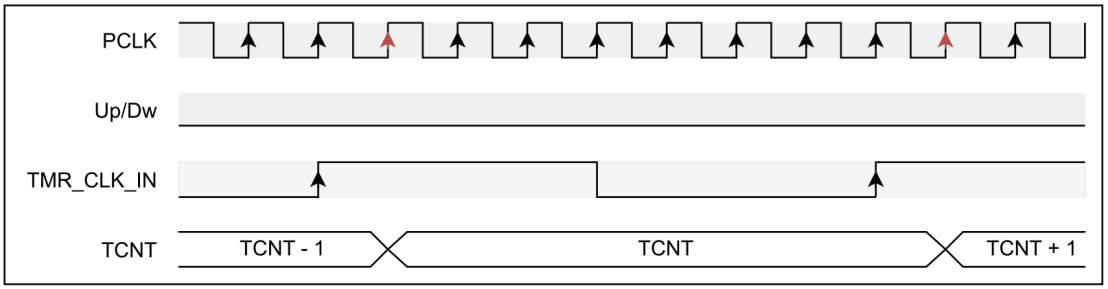


Figure 5.4. TCNT Count up Timing chart (Rising Edge)

TCNT Count down Timing

Figure 6.2. shows the TCNT count down timing for internal clock input.

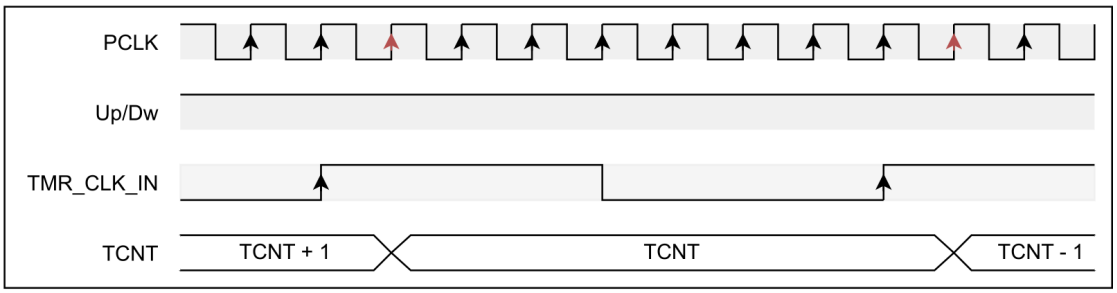


Figure 5.5. TCNT Count down Timing chart (Rising Edge)

6. OVERFLOW/UNDERFLOW COMPARATOR

6.1. Input/Output pin

Table 6.1. Pin Configuration

Signal name	I/O	Description
TCNT	Input	Current value of the timer/counter. This value is continuously monitored to detect overflow (8'hFF) or underflow (8'h00).
count_up_down	Input	Selects the counting direction: 0 for Count up and 1 for Count down
TMR_UDF	Output	Underflow flag. Asserted high for one clock cycle when TCNT == 8'h00 in count-down mode.
TMR_OVF	Output	Overflow flag. Asserted high for one clock cycle when TCNT == 8'hFF in count-up mode.

6.2. Functional/Protocol

Figure 6.1. OVERFLOW/UNDERFLOW COMPARATOR Block diagram

This block monitors the counter value (TCNT) to detect overflow and underflow events:

- Count-up mode (count_up_down = 0): When TCNT reaches 8'hFF+1, the TMR_OVF flag is set high for one clock cycle to indicate an overflow.
- Count-down mode (count_up_down = 1): When TCNT reaches 8'h00+1, the TMR_UDF flag is set high for one clock cycle to indicate an underflow.

6.3. Design circuit

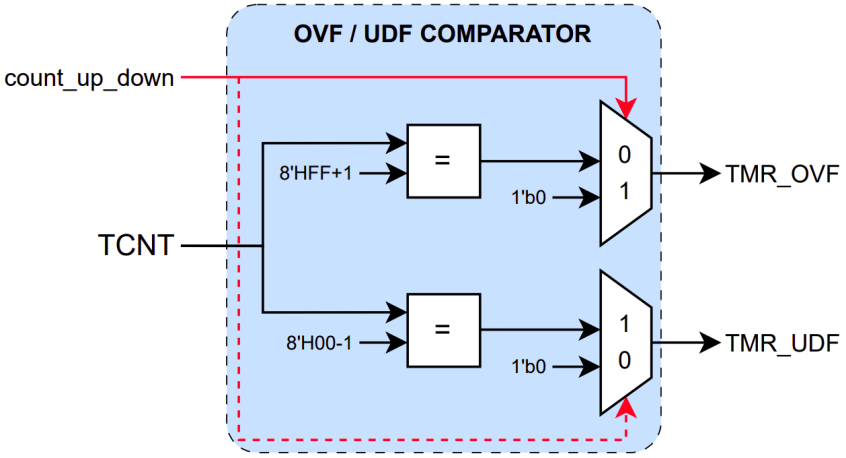


Figure 6.2. OVERFLOW/UNDERFLOW COMPARATOR circuit

6.4. Timing chart

Timing of Overflow Flag (TMR_OVF) Setting The TMR_OVF bit in TCSR is set to 1 when TCNT overflows (changes from H'FF to H'00).

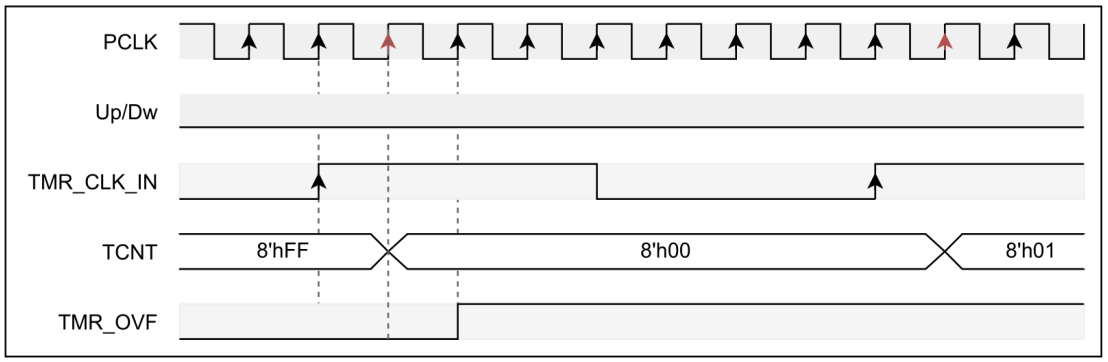


Figure 6.3. Timing of Overflow Flag (TMR_OVF) Setting (Rising Edge)

Timing of Underflow Flag (TMR_UDF) Setting The TMR_UDF bit in TCSR is set to 1 when TCNT underflows (changes from H'00 to H'FF).

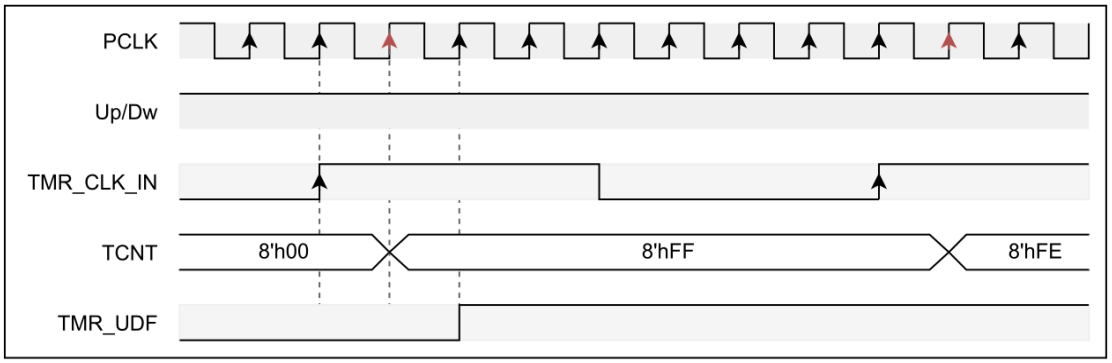


Figure 6.4. Timing of Underflow Flag (TMR_UDF) Setting (Rising Edge)

Note

+ Design Rising Edge Circuit to apply the synchronous design for 8-bit Counter.
+ Status bit TMR_OVF is set to 1 at the final system clock before the counter changes from 8'hFF to 8'h00.
+ Status bit TMR_UDF is set to 1 at the final system clock before the counter changes from 8'h00 to 8'hFF.