1. Description

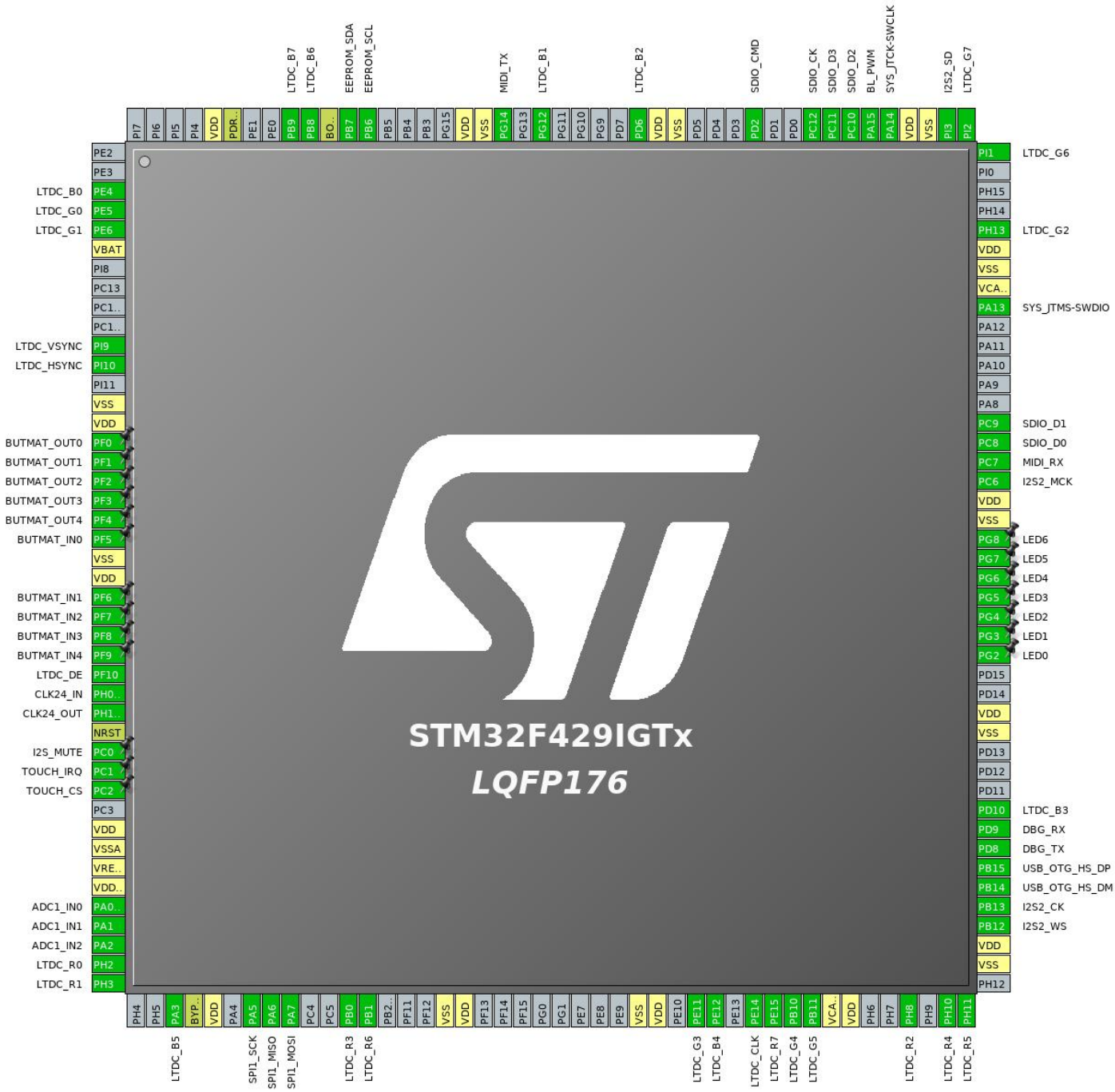
1.1. Project

Project Name	test2
Board Name	custom
Generated with:	STM32CubeMX 5.0.0
Date	12/04/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429IGTx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



3. Pins Configuration

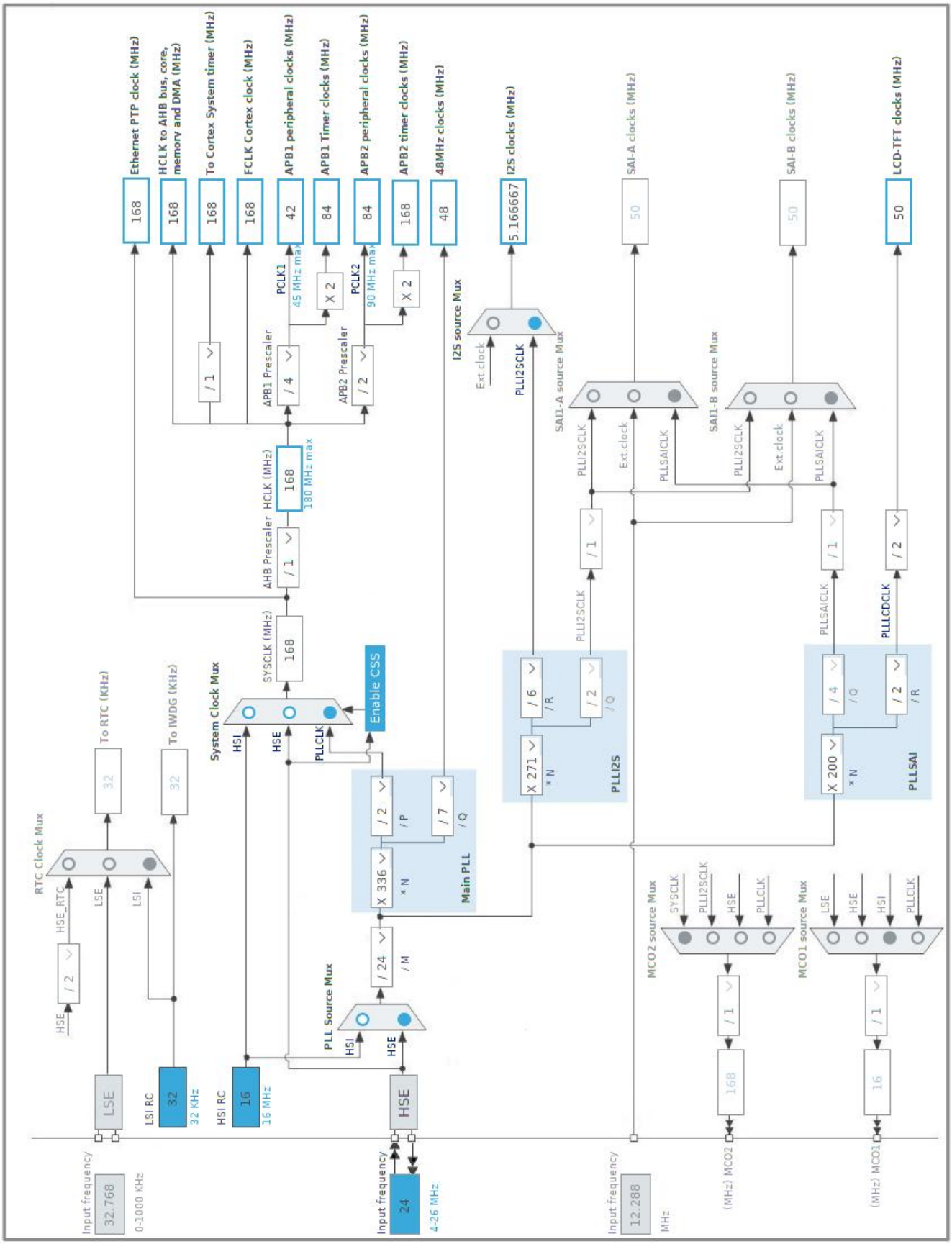
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
3	PE4	I/O	LTDC_B0	
4	PE5	I/O	LTDC_G0	
5	PE6	I/O	LTDC_G1	
6	VBAT	Power		
11	PI9	I/O	LTDC_VSYNC	
12	PI10	I/O	LTDC_HSYNC	
14	VSS	Power		
15	VDD	Power		
16	PF0 *	I/O	GPIO_Output	BUTMAT_OUT0
17	PF1 *	I/O	GPIO_Output	BUTMAT_OUT1
18	PF2 *	I/O	GPIO_Output	BUTMAT_OUT2
19	PF3 *	I/O	GPIO_Output	BUTMAT_OUT3
20	PF4 *	I/O	GPIO_Output	BUTMAT_OUT4
21	PF5 *	I/O	GPIO_Input	BUTMAT_IN0
22	VSS	Power		
23	VDD	Power		
24	PF6 *	I/O	GPIO_Input	BUTMAT_IN1
25	PF7 *	I/O	GPIO_Input	BUTMAT_IN2
26	PF8 *	I/O	GPIO_Input	BUTMAT_IN3
27	PF9 *	I/O	GPIO_Input	BUTMAT_IN4
28	PF10	I/O	LTDC_DE	
29	PH0/OSC_IN	I/O	RCC_OSC_IN	CLK24_IN
30	PH1/OSC_OUT	I/O	RCC_OSC_OUT	CLK24_OUT
31	NRST	Reset		
32	PC0 *	I/O	GPIO_Output	I2S_MUTE
33	PC1 *	I/O	GPIO_Input	TOUCH_IRQ
34	PC2 *	I/O	GPIO_Output	TOUCH_CS
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
40	PA0/WKUP	I/O	ADC1_IN0	
41	PA1	I/O	ADC1_IN1	
42	PA2	I/O	ADC1_IN2	
43	PH2	I/O	LTDC_R0	
44	PH3	I/O	LTDC_R1	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
47	PA3	I/O	LTDC_B5	
48	BYPASS_REG	Reset		
49	VDD	Power		
51	PA5	I/O	SPI1_SCK	
52	PA6	I/O	SPI1_MISO	
53	PA7	I/O	SPI1_MOSI	
56	PB0	I/O	LTDC_R3	
57	PB1	I/O	LTDC_R6	
61	VSS	Power		
62	VDD	Power		
71	VSS	Power		
72	VDD	Power		
74	PE11	I/O	LTDC_G3	
75	PE12	I/O	LTDC_B4	
77	PE14	I/O	LTDC_CLK	
78	PE15	I/O	LTDC_R7	
79	PB10	I/O	LTDC_G4	
80	PB11	I/O	LTDC_G5	
81	VCAP_1	Power		
82	VDD	Power		
85	PH8	I/O	LTDC_R2	
87	PH10	I/O	LTDC_R4	
88	PH11	I/O	LTDC_R5	
90	VSS	Power		
91	VDD	Power		
92	PB12	I/O	I2S2_WS	
93	PB13	I/O	I2S2_CK	
94	PB14	I/O	USB_OTG_HS_DM	
95	PB15	I/O	USB_OTG_HS_DP	
96	PD8	I/O	USART3_TX	DBG_TX
97	PD9	I/O	USART3_RX	DBG_RX
98	PD10	I/O	LTDC_B3	
102	VSS	Power		
103	VDD	Power		
106	PG2 *	I/O	GPIO_Output	LED0
107	PG3 *	I/O	GPIO_Output	LED1
108	PG4 *	I/O	GPIO_Output	LED2
109	PG5 *	I/O	GPIO_Output	LED3
110	PG6 *	I/O	GPIO_Output	LED4

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
111	PG7 *	I/O	GPIO_Output	LED5
112	PG8 *	I/O	GPIO_Output	LED6
113	VSS	Power		
114	VDD	Power		
115	PC6	I/O	I2S2_MCK	
116	PC7	I/O	USART6_RX	MIDI_RX
117	PC8	I/O	SDIO_D0	
118	PC9	I/O	SDIO_D1	
124	PA13	I/O	SYS_JTMS-SWDIO	
125	VCAP_2	Power		
126	VSS	Power		
127	VDD	Power		
128	PH13	I/O	LTDC_G2	
132	PI1	I/O	LTDC_G6	
133	PI2	I/O	LTDC_G7	
134	PI3	I/O	I2S2_SD	
135	VSS	Power		
136	VDD	Power		
137	PA14	I/O	SYS_JTCK-SWCLK	
138	PA15	I/O	TIM2_CH1	BL_PWM
139	PC10	I/O	SDIO_D2	
140	PC11	I/O	SDIO_D3	
141	PC12	I/O	SDIO_CK	
144	PD2	I/O	SDIO_CMD	
148	VSS	Power		
149	VDD	Power		
150	PD6	I/O	LTDC_B2	
155	PG12	I/O	LTDC_B1	
157	PG14	I/O	USART6_TX	MIDI_TX
158	VSS	Power		
159	VDD	Power		
164	PB6	I/O	I2C1_SCL	EEPROM_SCL
165	PB7	I/O	I2C1_SDA	EEPROM_SDA
166	BOOT0	Boot		
167	PB8	I/O	LTDC_B6	
168	PB9	I/O	LTDC_B7	
171	PDR_ON	Reset		
172	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	test2
Project Folder	/home/matthew/test2
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.23.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429IGTx
Datasheet	024030_Rev9

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

mode: IN1

mode: IN2

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**3 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles
Rank	**2 ***
Channel	**Channel 1 ***
Sampling Time	3 Cycles
Rank	**3 ***
Channel	**Channel 2 ***
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. I2C1

I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Timing configuration:

Coefficient of Digital Filter	0
Analog Filter	Enabled

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.3. I2S2

Mode: Half-Duplex Master

mode: Master Clock Output

7.3.1. Parameter Settings:

Generic Parameters:

Transmission Mode	Mode Master Transmit
Communication Standard	I2S Philips
Data and Frame Format	16 Bits Data on 16 Bits Frame
Selected Audio Frequency	**Custom Freq ***
Custom I2S Frequency (Hz)	**44100 ***
Real Audio Frequency	**44.108 KHz ***
Error between Selected and Real	**0.24 % ***

Clock Parameters:

Clock Source	I2S PLL Clock
Clock Polarity	Low

7.4. LTDC

Display Type: RGB888 (24 bits)

7.4.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	**480 ***
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	494
Total Width	500

Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	**272 ***
Vertical Front Porch	2
VSync Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	277
Total Height	279

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

7.4.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0

Layer 1 - Red	0

Number of Layers:

Number of Layers	2 layers

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	0
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

7.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

7.6. RNG

mode: Activated

7.7. SDIO

Mode: SD 4 bits Wide bus

7.7.1. Parameter Settings:

SDIO parameters:

Clock transition on which the bit capture is made	Rising transition
SDIO Clock divider bypass	Disable
SDIO Clock output enable when the bus is idle	Disable the power save for the clock
SDIO hardware flow control	The hardware control flow is disabled
SDIOCLK clock divide factor	0

7.8. SPI1

Mode: Full-Duplex Master

7.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola

Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**42.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.9. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.10. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.11. USART3

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.12. USART6

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	**31250 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.13. USB_OTG_HS

Internal FS Phy: Host_Only

7.13.1. Parameter Settings:

Speed	Host Full Speed 12MBit/s
Enable internal IP DMA	**Enabled ***
Physical interface	Internal Phy
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	EEPROM_SCL
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	EEPROM_SDA
I2S2	PB12	I2S2_WS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	I2S2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	I2S2_MCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI3	I2S2_SD	Alternate Function Push Pull	No pull-up and no pull-down	Low	
LTDC	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH2	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH3	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH8	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH11	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD10	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH13	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	CLK24_IN
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	CLK24_OUT
SDIO	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	BL_PWM
USART3	PD8	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	DBG_TX
	PD9	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	DBG_RX
USART6	PC7	USART6_RX	Alternate Function Push Pull	Pull-up	**Very High ***	MIDI_RX
	PG14	USART6_TX	Alternate Function Push Pull	Pull-up	**Very High ***	MIDI_TX
USB_OTG_HS	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUTMAT_OUT0
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUTMAT_OUT1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUTMAT_OUT2
	PF3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUTMAT_OUT3
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BUTMAT_OUT4
	PF5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTMAT_IN0
	PF6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTMAT_IN1
	PF7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTMAT_IN2
	PF8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTMAT_IN3
	PF9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUTMAT_IN4
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	I2S_MUTE
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	TOUCH_IRQ
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TOUCH_CS
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED4
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED5
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED6

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI2_TX	DMA1_Stream4	Memory To Peripheral	Low

SPI2_TX: DMA1_Stream4 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream4 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM2 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART3 global interrupt	unused		
SDIO global interrupt	unused		
USART6 global interrupt	unused		
USB On The Go HS End Point 1 Out global interrupt	unused		
USB On The Go HS End Point 1 In global interrupt	unused		
USB On The Go HS global interrupt	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		

*** User modified value**

9. Software Pack Report