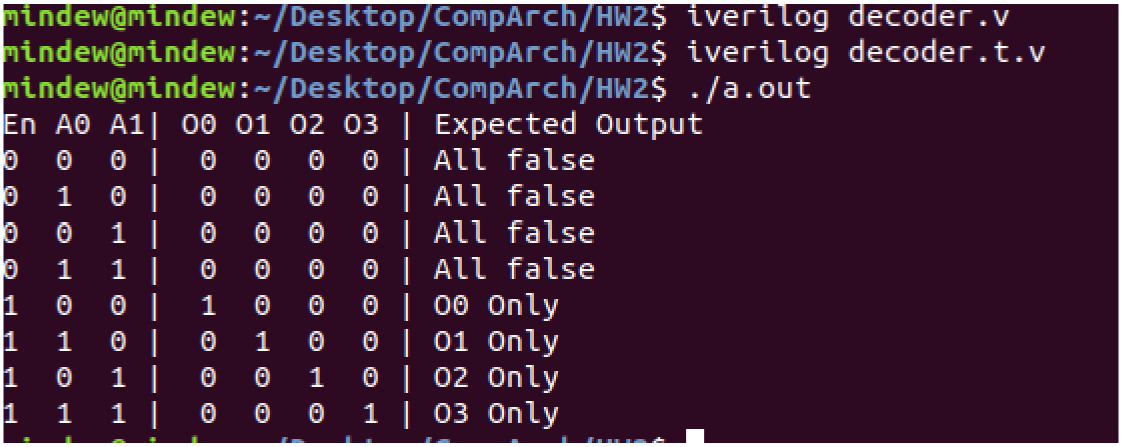
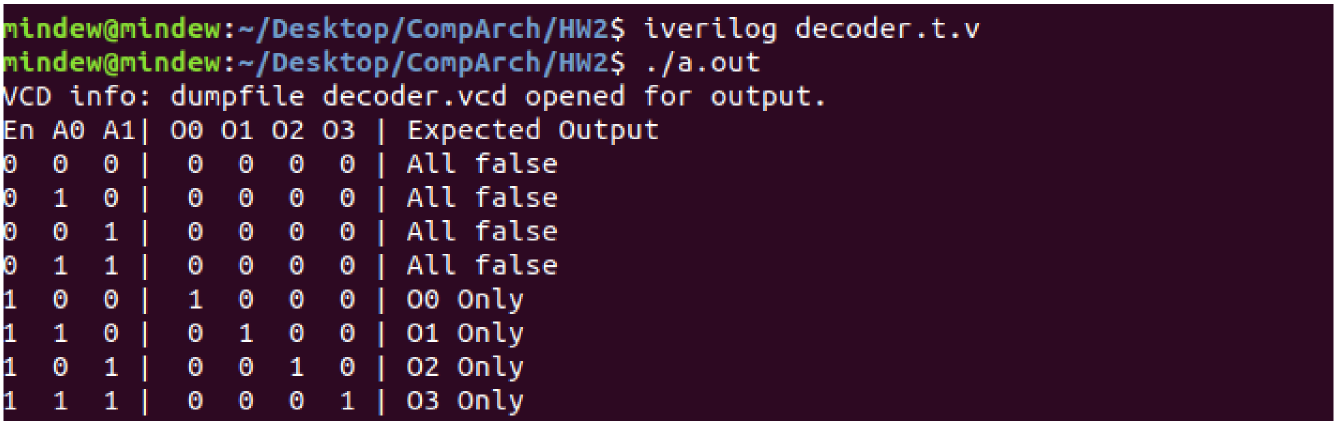
Writeup Minju Kang

First, I started with testing the given test bench with behavioral decoder.
<Behavioral>



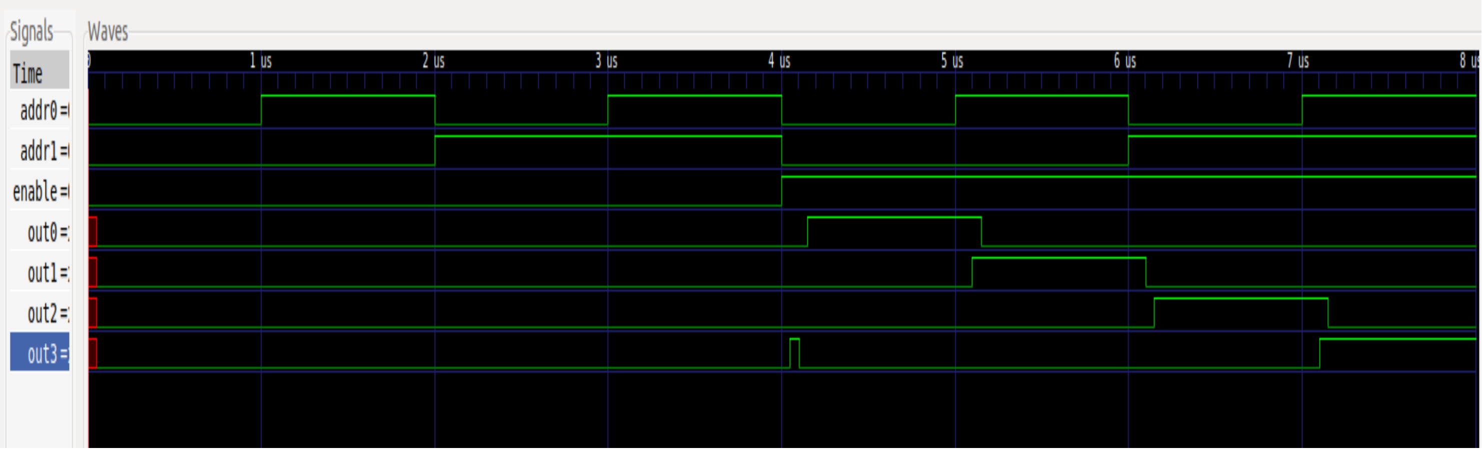
```
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog decoder.v
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog decoder.t.v
mindew@mindew:~/Desktop/CompArch/HW2$ ./a.out
En A0 A1| O0 O1 O2 O3 | Expected Output
0  0  0 |  0  0  0  0 | All false
0  1  0 |  0  0  0  0 | All false
0  0  1 |  0  0  0  0 | All false
0  1  1 |  0  0  0  0 | All false
1  0  0 |  1  0  0  0 | O0 Only
1  1  0 |  0  1  0  0 | O1 Only
1  0  1 |  0  0  1  0 | O2 Only
1  1  1 |  0  0  0  1 | O3 Only
```

Then, I built the structural decoder with 2 NOT gates and 8 AND gates (4 for inputs and 4 for inputs & enable).
<Structural>



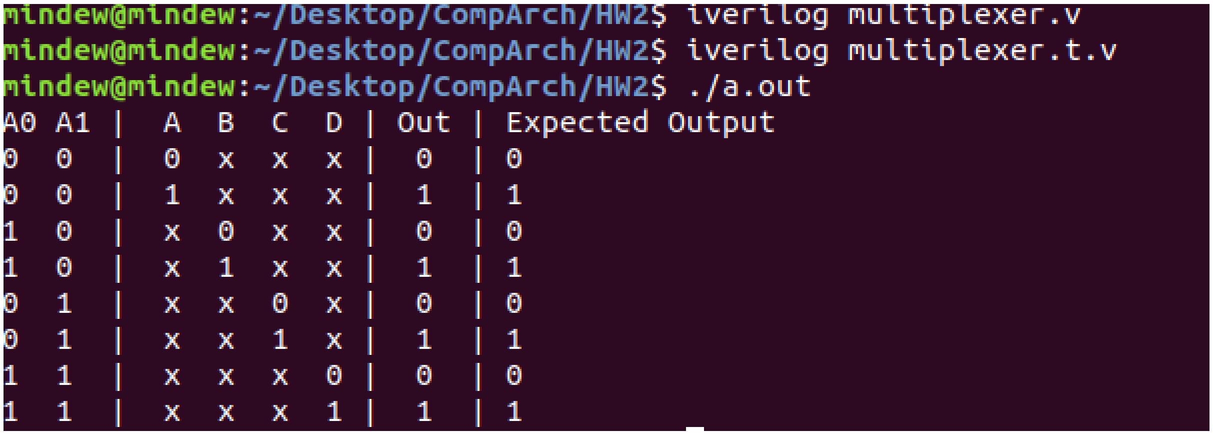
```
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog decoder.t.v
mindew@mindew:~/Desktop/CompArch/HW2$ ./a.out
VCD info: dumpfile decoder.vcd opened for output.
En A0 A1| O0 O1 O2 O3 | Expected Output
0  0  0 |  0  0  0  0 | All false
0  1  0 |  0  0  0  0 | All false
0  0  1 |  0  0  0  0 | All false
0  1  1 |  0  0  0  0 | All false
1  0  0 |  1  0  0  0 | O0 Only
1  1  0 |  0  1  0  0 | O1 Only
1  0  1 |  0  0  1  0 | O2 Only
1  1  1 |  0  0  0  1 | O3 Only
```

With dumped .vcd file, I checked that the structural decoder corresponds with waveform.



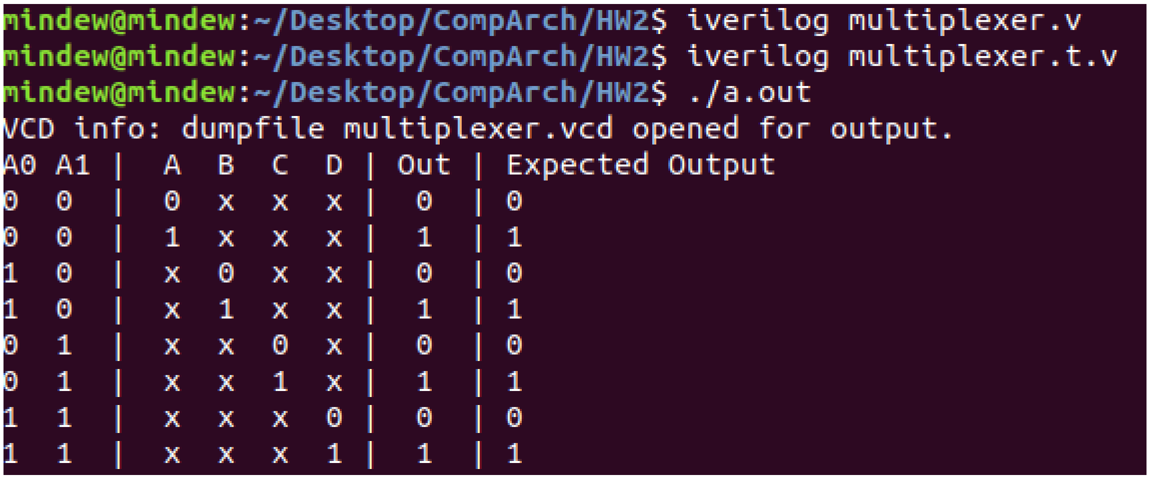
Then, I built 4 input multiplexer with 2 NOT gates and 8 AND gates (4 for addresses and 4 for inputs & addresses), 2 OR gates (1 for in0 and in1, 1 for in2 and in3). Following is truth tables for behavioral and structural multiplexer. Then, I checked gtkwave.

<Behavioral>

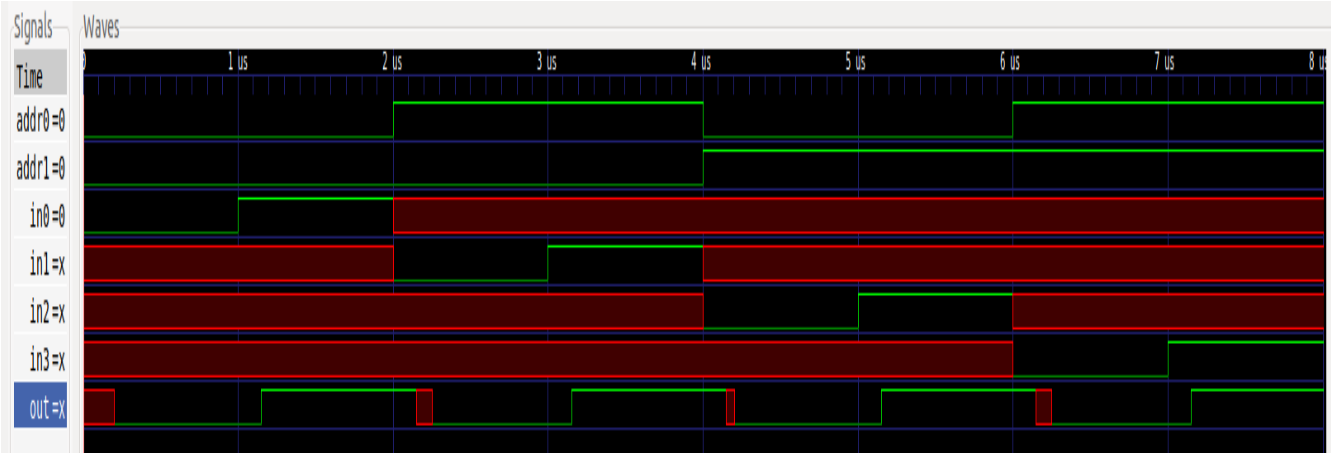


```
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog multiplexer.v
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog multiplexer.t.v
mindew@mindew:~/Desktop/CompArch/HW2$ ./a.out
A0 A1 |  A  B  C  D |  Out  | Expected Output
0  0  |  0  x  x  x |   0   | 0
0  0  |  1  x  x  x |   1   | 1
1  0  |  x  0  x  x |   0   | 0
1  0  |  x  1  x  x |   1   | 1
0  1  |  x  x  0  x |   0   | 0
0  1  |  x  x  1  x |   1   | 1
1  1  |  x  x  x  0 |   0   | 0
1  1  |  x  x  x  1 |   1   | 1
```

<Structural>



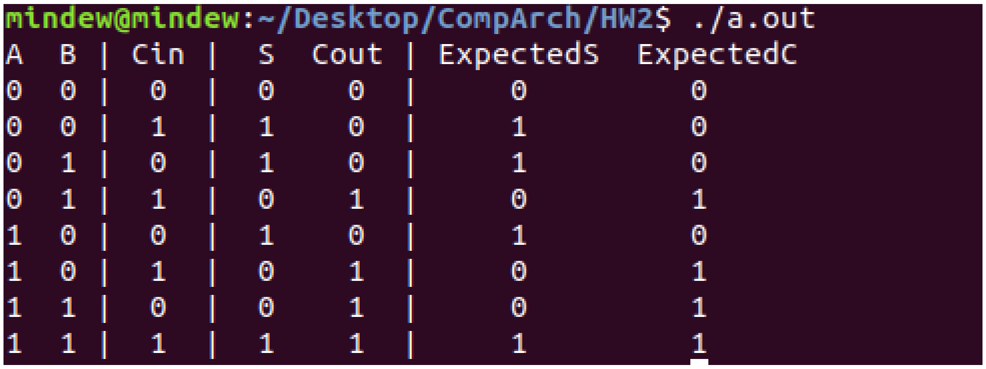
```
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog multiplexer.v
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog multiplexer.t.v
mindew@mindew:~/Desktop/CompArch/HW2$ ./a.out
VCD info: dumpfile multiplexer.vcd opened for output.
A0 A1 |  A  B  C  D |  Out  | Expected Output
0  0  |  0  x  x  x |   0   | 0
0  0  |  1  x  x  x |   1   | 1
1  0  |  x  0  x  x |   0   | 0
1  0  |  x  1  x  x |   1   | 1
0  1  |  x  x  0  x |   0   | 0
0  1  |  x  x  1  x |   1   | 1
1  1  |  x  x  x  0 |   0   | 0
1  1  |  x  x  x  1 |   1   | 1
```



Red sections indicate null part of the logic (X)

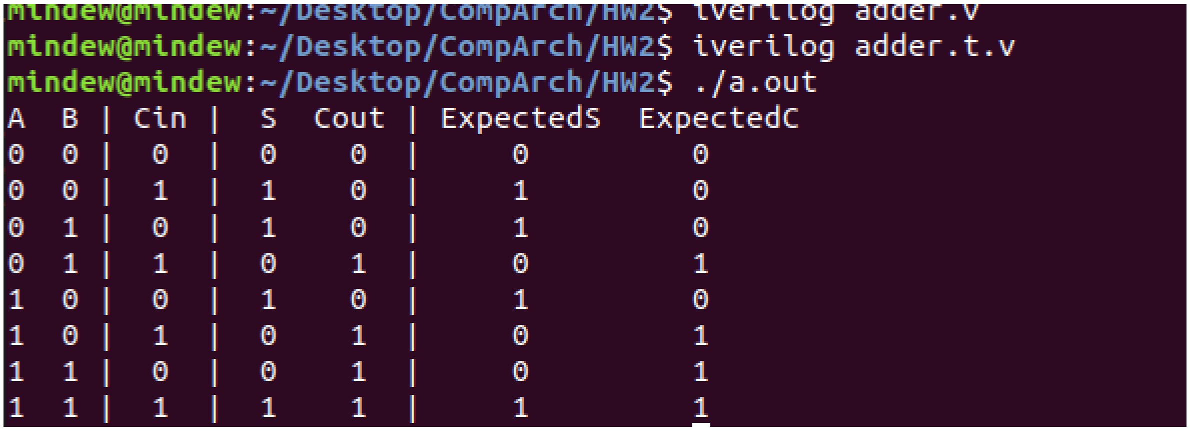
Finally, I built FULL adder with 2 XOR gates, 2 AND gates and 1 OR gate. Followings are truth tables for behavioral and structural adder. Then, gtkwave result is checked with the truth tables.

<Behavioral>

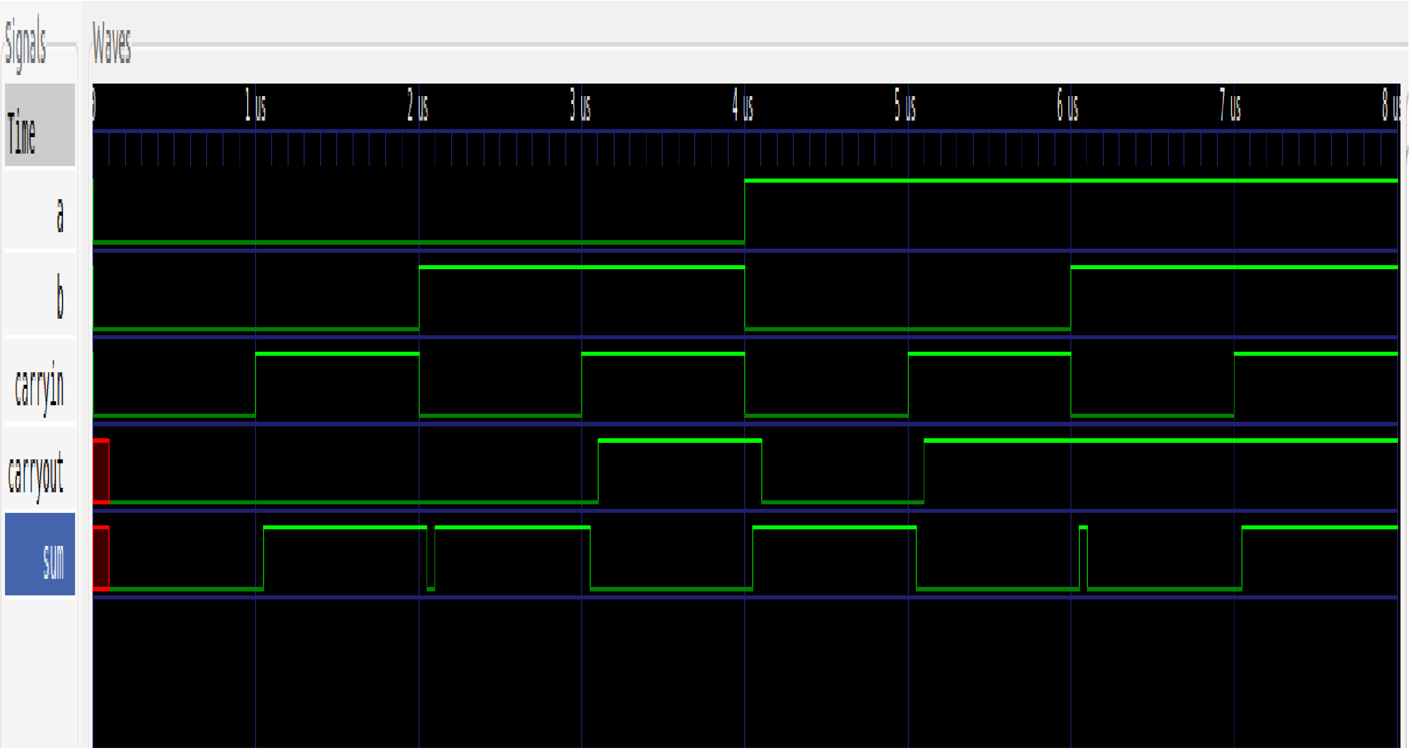


```
mindew@mindew:~/Desktop/CompArch/HW2$ ./a.out
A  B | Cin |  S   Cout | ExpectedS  ExpectedC
0  0 |  0  |  0    0   |     0          0
0  0 |  1  |  1    0   |     1          0
0  1 |  0  |  1    0   |     1          0
0  1 |  1  |  0    1   |     0          1
1  0 |  0  |  1    0   |     1          0
1  0 |  1  |  0    1   |     0          1
1  1 |  0  |  0    1   |     0          1
1  1 |  1  |  1    1   |     1          1
```

<Structural>



```
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog adder.v
mindew@mindew:~/Desktop/CompArch/HW2$ iverilog adder.t.v
mindew@mindew:~/Desktop/CompArch/HW2$ ./a.out
A  B | Cin |  S   Cout | ExpectedS  ExpectedC
0  0 |  0  |  0    0   |     0          0
0  0 |  1  |  1    0   |     1          0
0  1 |  0  |  1    0   |     1          0
0  1 |  1  |  0    1   |     0          1
1  0 |  0  |  1    0   |     1          0
1  0 |  1  |  0    1   |     0          1
1  1 |  0  |  0    1   |     0          1
1  1 |  1  |  1    1   |     1          1
```


Signals
Waves
Time
a
b
carryin
carryout
sum
0
1 us
2 us
3 us
4 us
5 us
6 us
7 us
8 us