
DIGITAL ELECTRONICS

How many 32 K × 1 RAM chips are needed to provide a memory capacity of 256 K-bytes ?

1. 8
2. 128
3. 32
4. 64

Combinational & Sequential Logic Circuits

Sequential Logic Circuits

FLIP-FLOPS

- Both **Latches and flip flops** are circuit elements wherein the output not only depends on the current inputs, but also depends on the previous input and outputs. The main **difference between** the **latch and flip flop** is that a **flip flop** has a clock signal, whereas a **latch** does not.
- A **flip-flop** or **latch** is a circuit that has two stable states and can be used to store state information. A **flip-flop** is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.

Sequential Logic Circuits

FLIP-FLOPS

- Latches and flip-flops are the basic elements for storing information. One latch or **flip-flop can store one bit of information**.

- The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted.

Sequential Logic Circuits

FLIP-FLOPS

- In other words, when they are enabled, their content changes immediately when their inputs change. Flip- flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes.

- There are basically four main types of latches and flip- flops:
- **SR, D, JK, and T**. The major differences in these flip-flop types are the number of **inputs they have and how they change state**. For each type, there are also different variations that enhance their operations.
- Each type can have different variations such as active high or low inputs, whether they change state at the rising or falling edge of the clock signal, and whether they have asynchronous inputs or not.
- The flip-flops can be described fully and uniquely by its logic symbol, characteristic table, characteristic equation, state diagram, or excitation table, and are summarized in Figure below.

- Latches are digital circuits that store a single bit of information and hold its value until it is updated by new input signals. They are used in digital systems as temporary storage elements to store binary information. Latches can be implemented using various digital logic gates, such as AND, OR, NOT, NAND, and NOR gates.

- There are two types of latches:

- S-R (Set-Reset) Latches: S-R latches are the simplest form of latches and are implemented using two inputs: S (Set) and R (Reset). The S input sets the output to 1, while the R input resets the output to 0. When both S and R are at 1, the latch is said to be in an “undefined” state.

- D (Data) Latches: D latches are also known as transparent latches and are implemented using two inputs: D (Data) and a clock signal. The output of the latch follows the input at the D terminal as long as the clock signal is high. When the clock signal goes low, the output of the latch is stored and held until the next rising edge of the clock.

- Latches are widely used in digital systems for various applications, including data storage, control circuits, and flip-flop circuits. They are often used in combination with other digital circuits to implement sequential circuits, such as state machines and memory elements.

- SR (Set-Reset) Latch – They are also known as preset and clear states. The SR latch forms the basic building blocks of all other types of flip-flops.

- SR Latch is a circuit with:

(i) 2 cross-coupled NOR gate or 2 cross-coupled NAND gate.
(ii) 2 input S for SET and R for RESET.
(iii) 2 output Q, Q'.

Flip-Flops : SR, D, JK, and T Flip-Flops

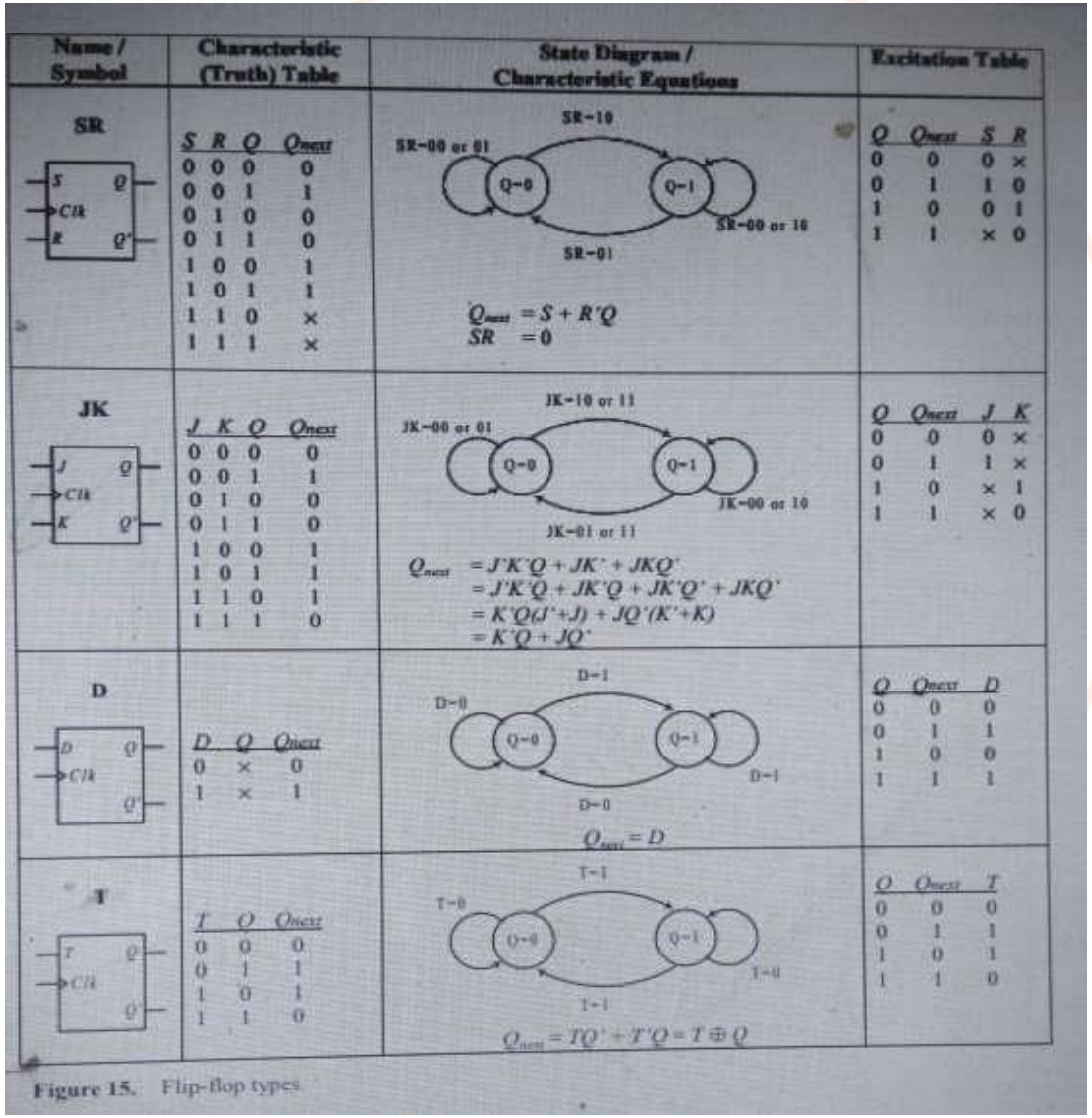


Figure 15. Flip-flop types

- Flip-flop is a circuit that maintains a state until directed by input to change the state. A basic flip-flop can be constructed using four-NAND or four-NOR gates. Flip flop is popularly known as the basic digital memory circuit. It has its two states as logic 1(High) and logic 0(low) states. A flip flop is a sequential circuit which consist of single binary state of information or data. The digital circuit is a flip flop which has two outputs and are of opposite states. It is also known as a Bistable Multivibrator.

- Types of flip-flops:

- SR Flip Flop
- JK Flip Flop
- D Flip Flop
- T Flip Flop

S-R Flip Flop

- This is the most common flip-flop among all. This simple flip-flop circuit has a set input (S) and a reset input (R). Apart from this, you can see the clock at the input end. At the output end, you will find two complementary outputs. The output is also feedback to the input visible in its circuit. Hence Q and Q' are not the actual outputs.

- You can make this simple flip flop either using AND and NOR gates or just NAND gates. We have taken the basic circuit of SR flip flop using AND and NOR gates for better understanding. You can check the logic gate basics.

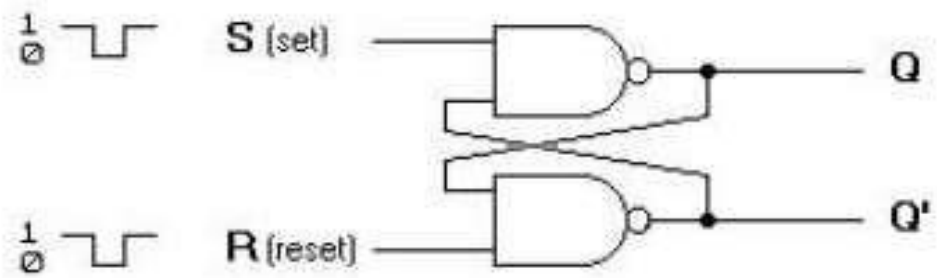
- Figure 4. SR latch: (a) circuit using NAND gates; (b) truth table; (c) logic symbol; (d) timing diagram.

- Figure 4. SR latch: (a) circuit using NAND gates; (b) truth table; (c) logic symbol; (d) timing diagram.

Continued…

- Like the NOR Gate S-R flip flop, this one also has four states. They are
- **S=0, R=1—Q=0, Q'=1**
- This state is also called the **SET** state.
- **S=1, R=0—Q=1, Q'=0**
- This state is known as the **RESET** state.
- In both the states you can see that the outputs are just compliments of each other and that the value of
- Q follows the compliment value of S.
- **S=0, R=0—Q=Q0, & Q' =Q0' No change**
- If both the values of S and R are switched to 0, then the circuit remembers the value of S and R in their previous state.
- **S=1, R=1—Q & Q'= Remember**
- If both the values of S and R are switched to 1 it is an invalid state because the values of both Q and Q' are 1. They are supposed to be compliments of each other. Normally, this state must be avoided.

S-R FLIP FLOP USING NAND GATE



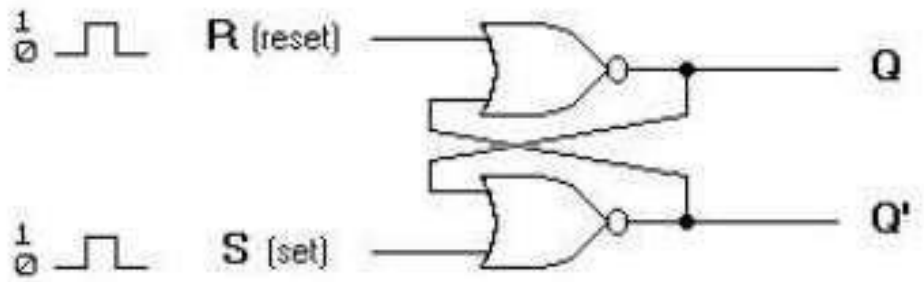
(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after S=1, R=0)
0	1	1	0	
1	1	1	0	(after S=0, R=1)
0	0	1	1	

(b) Truth table

Basic flip-flop circuit with NAND gates

S-R FLIP FLOP USING NOR GATE



(a) Logic diagram

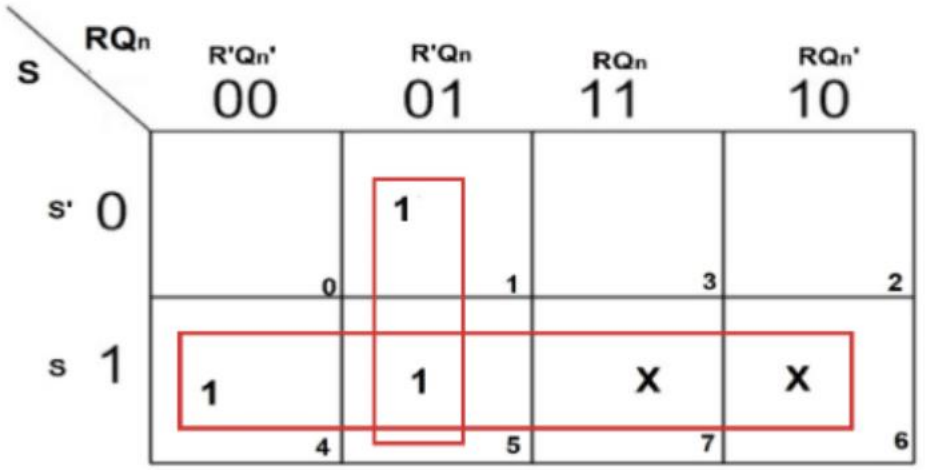
S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after S=1, R=0)
0	1	0	1	
0	0	0	1	(after S=0, R=1)
1	1	0	0	

(b) Truth table

Basic flip-flop circuit with NOR gates

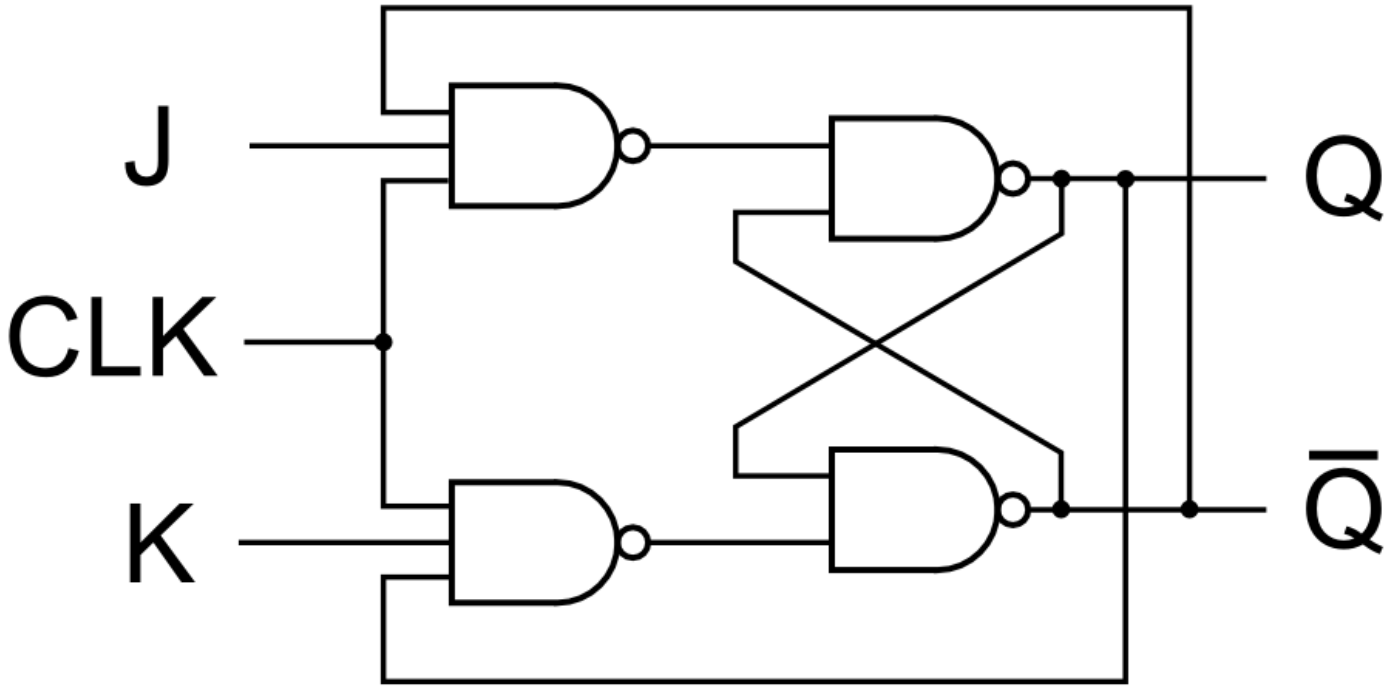
Characteristic Table

S	R	Qn	Q(n+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X



J-K FLIP-FLOP :

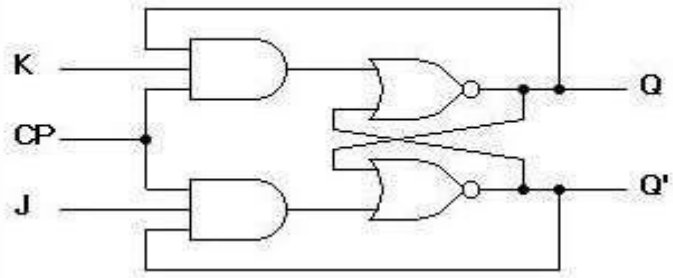
- Due to the undefined state in the SR flip-flops, another flip-flop is required in electronics. The JK flip-flop is an improvement on the SR flip-flop where S=R=1 is not a problem.



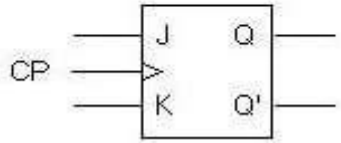
- Figure 17: JK flip-flop: (a) circuit; (b) truth table; (c) logic symbol.

J-K Flip-Flop :

- A J-K flip flop can also be defined as a modification of the S-R flip flop. The only difference is that the intermediate state is more refined and precise than that of a S-R flip flop.
- The behavior of inputs J and K is same as the S and R inputs of the S-R flip flop. The letter J stands for SET and the letter K stands for CLEAR.



(a) Logic diagram



(b) Graphical symbol

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(c) Transition table

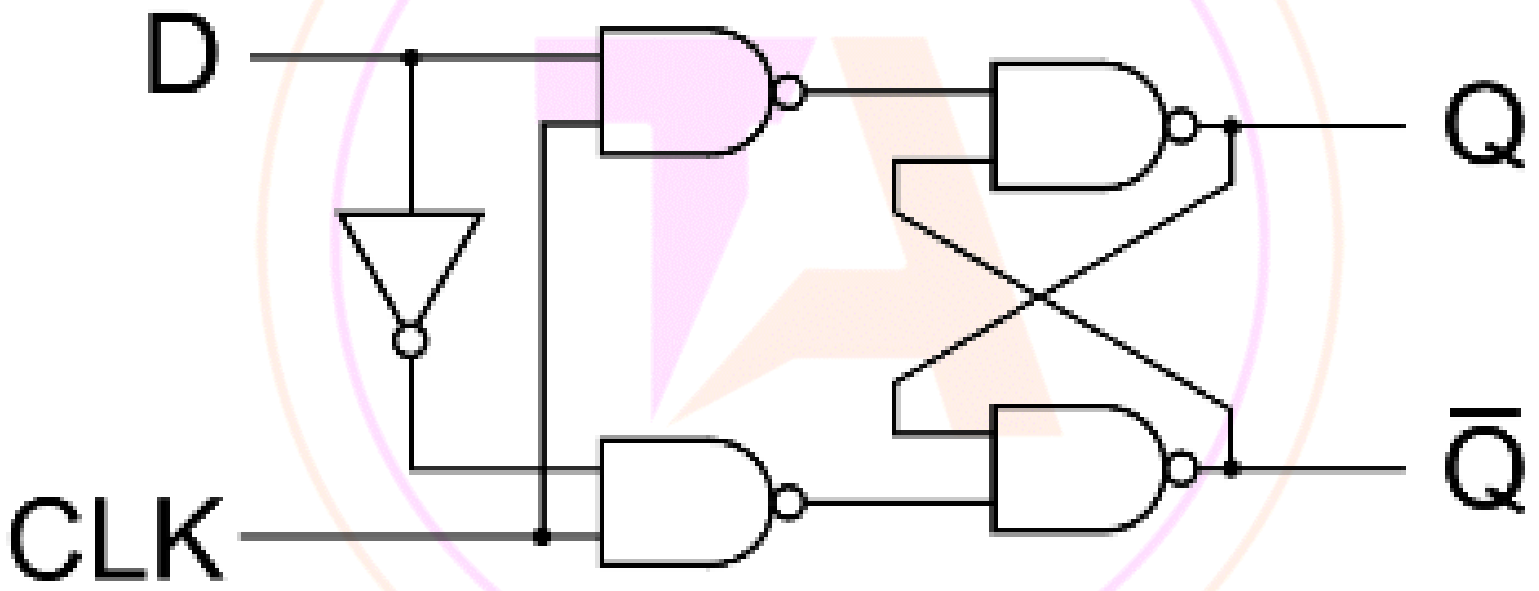
Clocked JK flip-flop

J-K Flip-Flop :

- When both the inputs J and K have a HIGH state, the flip-flop switch to the complement state. So, for a value of Q = 1, it switches to Q=0 and for a value of Q = 0, it switches to Q=1.
- The circuit includes two 3-input AND gates. The output Q of the flip flop is returned back as a feedback to the input of the AND along with other inputs like K and clock pulse [CP]. So, if the value of CP is 1, the flip flop gets a CLEAR signal and with the condition that the value of Q was earlier 1. Similarly output Q' of the flip flop is given as a feedback to the input of the AND along with other inputs like J and clock pulse [CP]. So the output becomes SET when the value of CP is 1 only if the value of Q' was earlier 1.
- **The output may be repeated in transitions once they have been complimented for J=K=1 because of the feedback connection in the JK flip-flop. This can be avoided by setting a time duration lesser than the propagation delay through the flip-flop. The restriction on the pulse width can be eliminated with a master- slave or edge-triggered construction.**

D TYPE FLIP-FLOP :

- D flip-flop is a better alternative that is very popular with digital electronics. They are commonly used for counters and shift registers and input synchronization.

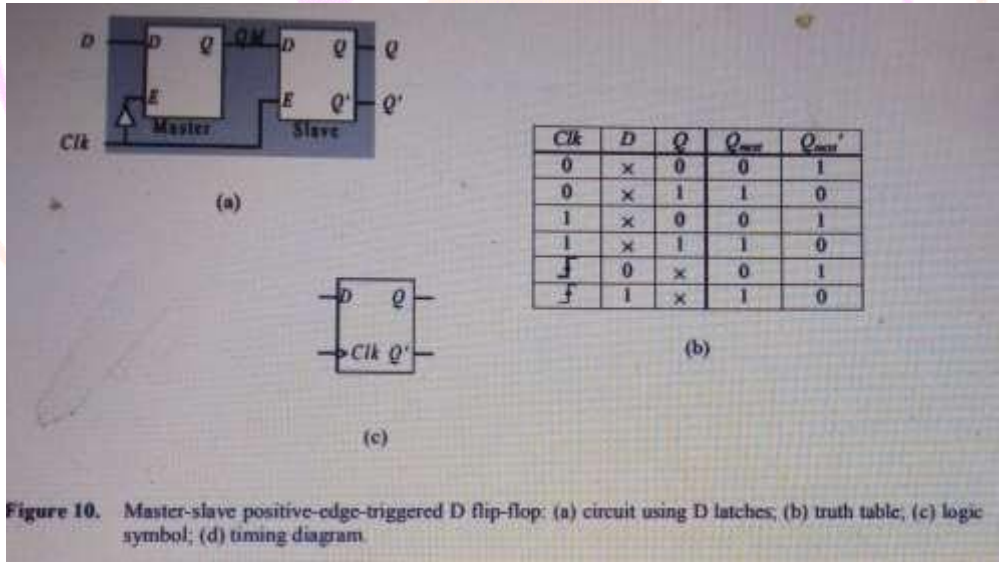


D TYPE FLIP-FLOP :

- Latches are often called level-sensitive because their output follows their inputs as long as they are enabled. They are transparent during this entire time when the enable signal is asserted. There are situations when it is more useful to **have the output change only at the rising or falling edge of the enable signal.** This enable signal is usually the controlling clock signal. Thus, we can have all changes synchronized to the rising or falling edge of the clock. An edge-triggered flip-flop achieves this by combining in series a pair of latches. Figure shows a positive edge-triggered D flip-flop where two D latches are connected in series and a clock signal Clk is connected to the E input of the latches, one directly, and one through an inverter. The first latch is called the master latch. The master latch is enabled when Clk = 0 and follows the primary input D. When Clk is a 1, the master latch is disabled but the second latch, called the slave latch, is enabled so that the output from the master latch is transferred to the slave latch. The slave latch is enabled all the while that Clk = 1, but its content changes only at the beginning of the cycle, that is, only at the rising edge of the signal because once Clk is 1, the master latch is disabled and so the

Continued…

- input to the slave latch will not change. The circuit of Figure 10(a) is called a positive edge-triggered flip-flop because the output Q on the slave latch changes only at the rising edge of the clock. If the slave latch is enabled when the clock is low, then it is referred to as a negative edge-triggered flip-flop. The circuit of Figure 10(a) is also referred to as a masterslave D flip-flop because of the two latches used in the circuit. Figure 10(b) and (c) show the truth table and the logic symbol respectively. Figure 10(d) shows the timing diagram for the D flip-flop.

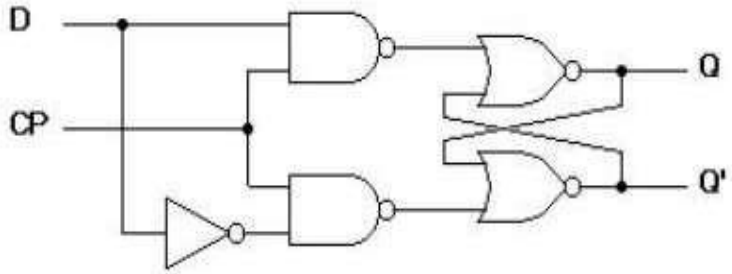


Clk	D	Q	Q_{next}	Q_{next}'
0	×	0	0	1
0	×	1	1	0
1	×	0	0	1
1	×	1	1	0
↓	0	×	0	1
↓	1	×	1	0

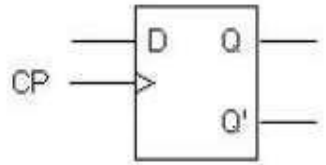
Figure 10. Master-slave positive-edge-triggered D flip-flop: (a) circuit using D latches; (b) truth table; (c) logic symbol; (d) timing diagram

D type Flip-Flop :

- The circuit diagram and truth table is given in figure
- D flip flop is actually a slight modification of the above explained **clocked SR flip-flop**. From the figure you can see that the D input is connected to the S input and the complement of the D input is connected to the R input. The D input is passed on to the flip flop when the value of CP is '1'.
- When CP is HIGH, the flip flop moves to the SET state. If it is '0', the flip flop switches to the CLEAR state.



(a) Logic diagram with NAND gates



(b) Graphical symbol

Q D	Q(t+1)
0 0	0
0 1	1
1 0	0
1 1	1

(c) Transition table

Clocked D flip-flop

T type Flip-Flop

- The T flip-flop has one input in addition to the clock. T stands for **toggle** for the obvious reason. When T is asserted (T = 1), the flip-flop state toggles back and forth, and when T is de-asserted, the flip-flop keeps its current state. The T flip-flop can be constructed using a D flip-flop with the two outputs Q and Q' feedback to the D input through a multiplexer that is controlled by the T input as shown in Figure 18.

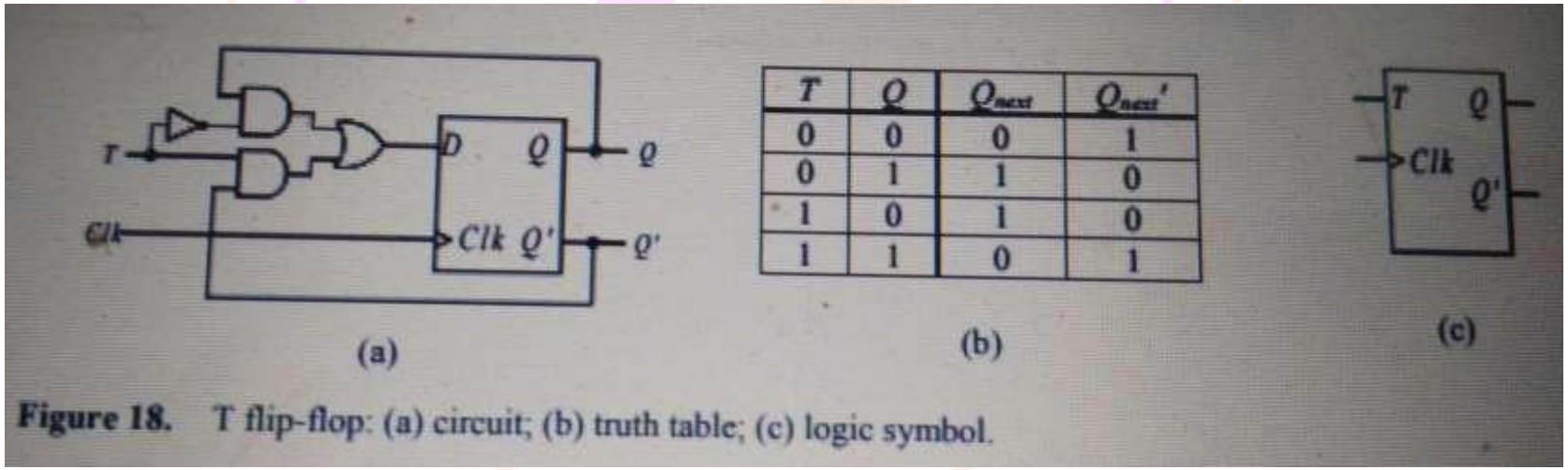
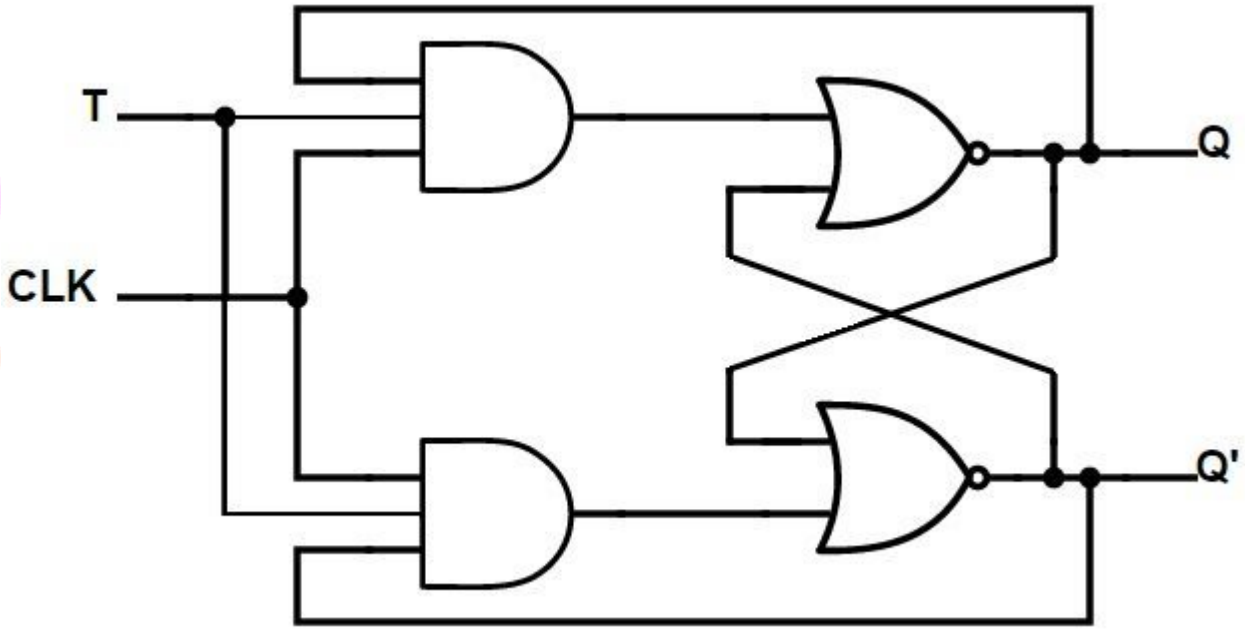


Figure 18. T flip-flop: (a) circuit; (b) truth table; (c) logic symbol.

- Figure 18. T flip-flop: (a) circuit; (b) truth table; (c) logic symbol.

T TYPE FLIP-FLOP :

- A T flip-flop is like a JK flip-flop. These are basically single-input versions of JK flip-flops. This modified form of the JK is obtained by connecting inputs J and K together. It has only one input along with the clock input.

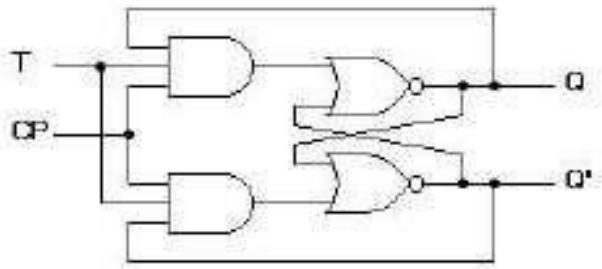


Truth Table:

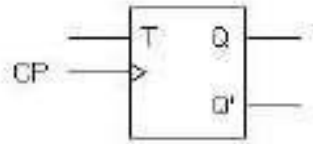
T	Q	Q (t+1)
0	0	0
1	0	1
0	1	1
1	1	0

T TYPE FLIP-FLOP :

- This is a much simpler version of the J-K flip flop. Both the J and K inputs are connected together and thus are also called a single input J-K flip flop. When clock pulse is given to the flip flop, the output begins to toggle. Here also the restriction on the pulse width can be eliminated with a master-slave or edge-triggered construction. Take a look at the circuit and truth table is shown in figure.



(a) Logic diagram



(b) Graphical symbol

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

(c) Transition table

Clocked T flip-flop

Q. A sequential circuit is an interconnection of _____ and _____.

A. flip-flops; gates

B. clocks; flip-flops

C. flip-flops; registers

D. clocks; gates

Q. Which of the following is NOT a way to represent negative fixed-point binary numbers?

A. Unsigned magnitude

B. Signed-1's complement

C. Signed-2's complement

D. Signed magnitude

Q. The multiplexer is also called a_____ since it selects one of many data inputs and steers the binary information to the output.

A. data distributor

B. data constructor

C. data convertor

D. data selector

Q. Which of the following is an application of decoder?

A. Serial-to-parallel conversion

B. Octal-to-binary conversion

C. Binary-to-octal conversion

D. Parallel-to-serial conversion

Q. Which of the following memory access methods in a computer system involves referring to any location that can be selected at random and directly addressed and accessed?

A. Dynamic access

B. Static access

C. Random access

D. Sequential access

Q. The manipulation of binary information in a CPU is done by logic circuits called _____.

A. gates

B. registers

C. flip-flop

D. bus

Q. A Boolean operator Θ is defined as follows:
1 Θ 1 =1, 1 Θ 0 = 0, 0 Θ 1= 0 and 0 Θ 0 =1
What will be the truth value of the expression

(x Θ y) Θ z = x Θ (y Θ z)?

(A) Always false
(B) Always true
(C) Sometimes true
(D) True when x,y,z are all true

Q. A multiplexer is a logic circuit that

(A) accepts one input and gives several output
(B) accepts many inputs and gives many output
(C) accepts many inputs and gives one output
(D) accepts one input and gives one output

Q. The Karnaugh map for a Boolean function is given as

The simplified Boolean equation for the above Karnaugh Map is

(A) AB + CD + AB' + AD
(B) AB + AC + AD + BCD
(C) AB + AD + BC + ACD
(D) AB + AC + BC + BCD

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	0	0	0
$\bar{A}B$	0	0	1	0
AB	1	1	1	1
$A\bar{B}$	0	1	1	1

Q. The Boolean function with the Karnaugh map

CD \ AB	00	01	11	10
00	0	1	1	0
01	0	1	1	1
11	1	1	1	1
10	0	1	1	0

(1) (A + C).D + B
(2) (A + B).C + D
(3) (A + D).C + B
(4) (A + C).B + D

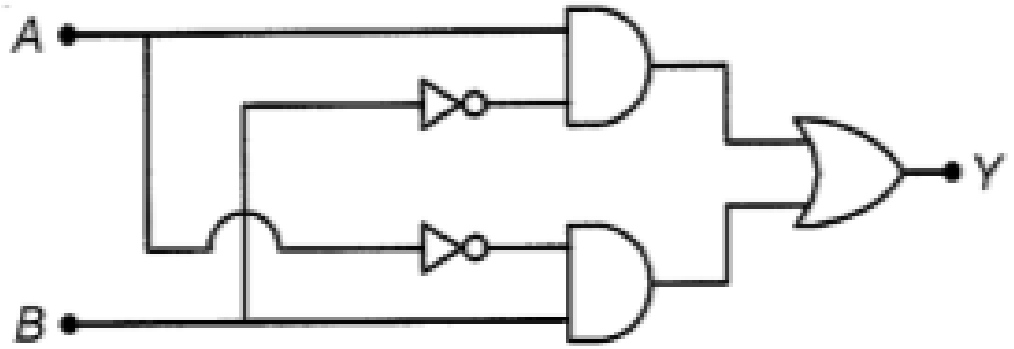
Q. The expression Y=AB+BC+AC shows the _____ operation.

a) EX-OR
b) SOP
c) POS
d) NOR

Q. The expression for Absorption law is given by _____

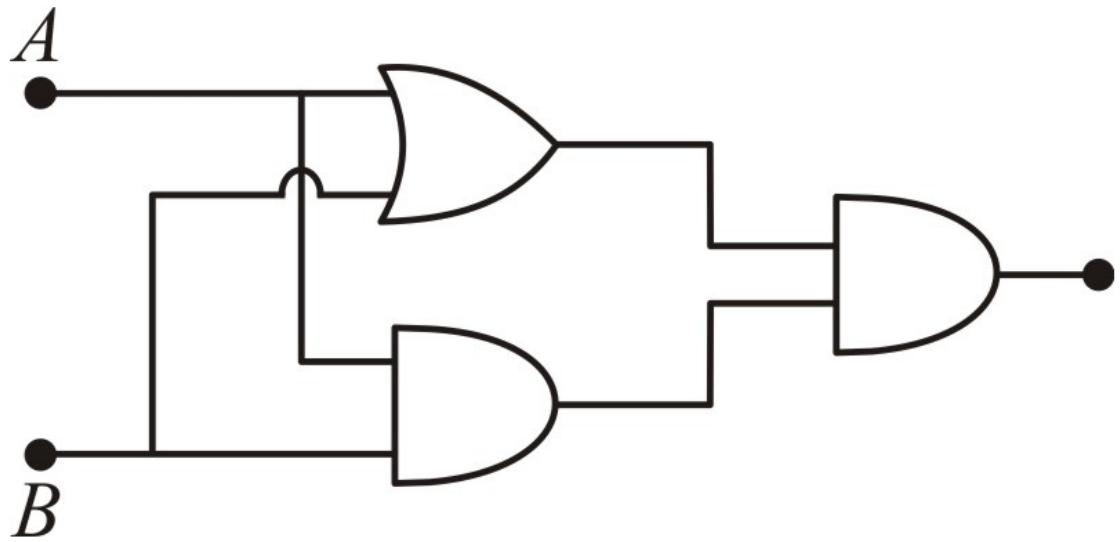
a) A + AB = A
b) A + AB = B
c) AB + AA’ = A
d) A + B = B + A

Q. For the logic circuit given below, the output Y for A=0, B=0 and A=1, B=1 are:



1. 0 and 1
2. 0 and 0
3. 1 and 0
4. 1 and 1

Q. The combination of gates shown in the diagram is equivalent to:



1. OR
2. AND
3. NAND
4. NOT

Q. Complement of the expression A'B + CD' is _____

a) (A' + B)(C' + D)
b) (A + B')(C' + D)
c) (A' + B)(C' + D)
d) (A + B')(C + D')

Q. From the truth table below, determine the standard SOP expression.

$X = \overline{A}\,\overline{B}\,\overline{C} + A\,B\,C + A\,\overline{B}\,C$

$X = A\,B\,C + A\,B\,C + A\,B\,C$

$X = A\,\overline{B}\,C + \overline{A}\,B\,C + A\,B\,\overline{C}$

$X = \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,B\,\overline{C}$

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0