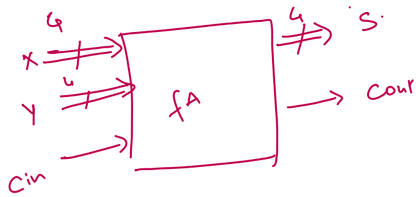
1. VHDL Code Structure

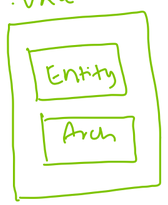


.v

```
module fa(
    input [3:0] x, y,
    input cin,
    output [3:0] s,
    output cout
);
wire [4:0] sum;
assign sum = x+y;
assign s = sum[3:0];
assign cout = sum[4];

endmodule
```

.vhd




```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_signed.all;

entity fa is
    port (
        cin : in std_logic;
        x,y : in std_logic_vector (3 downto 0);
        s : out std_logic_vector (3 downto 0);
        cout : out std_logic
    );
end fa;

architecture behav of fa is
    signal sum : std_logic_vector (4 downto 0);
begin
    sum <= ('0' & x) + y + cin;
           -- {1'b0, x}
           -- concat
    s <= sum (3 downto 0);
    c <= sum(4);

end behav;
```