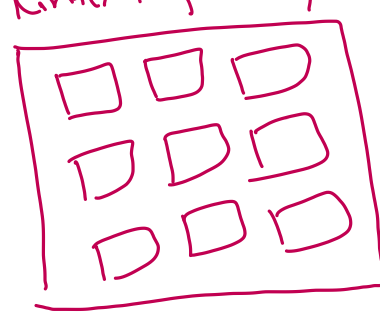
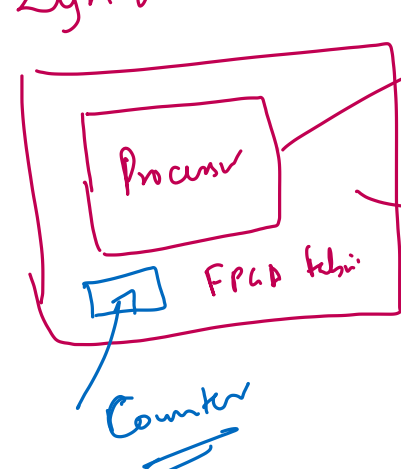


Kintex/Spartan/Virtex/Artix



FPGA fabric  
Cubes → Stream → WS/mux/FF  
Switch matrix  
Routing

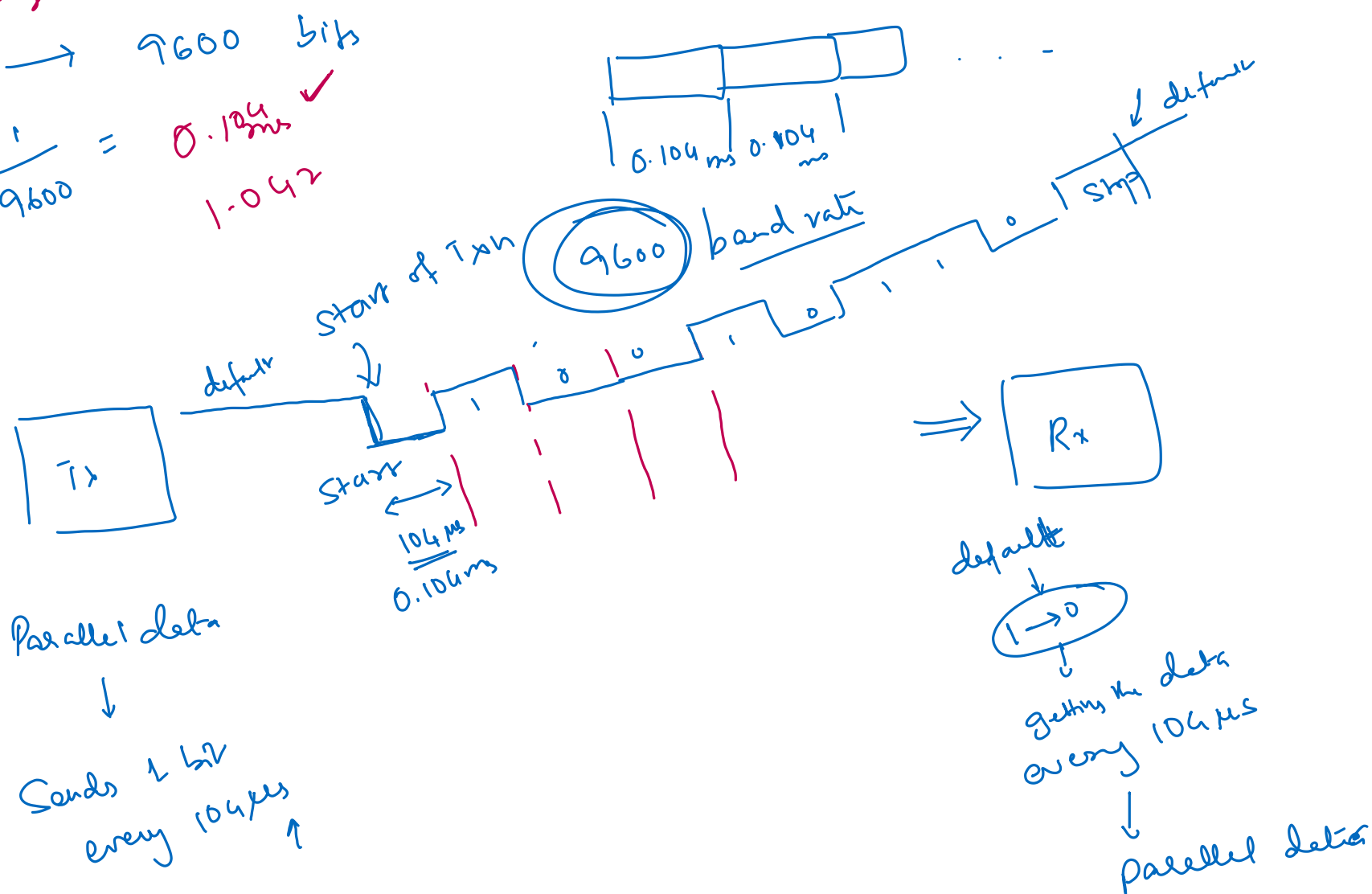
Zynq



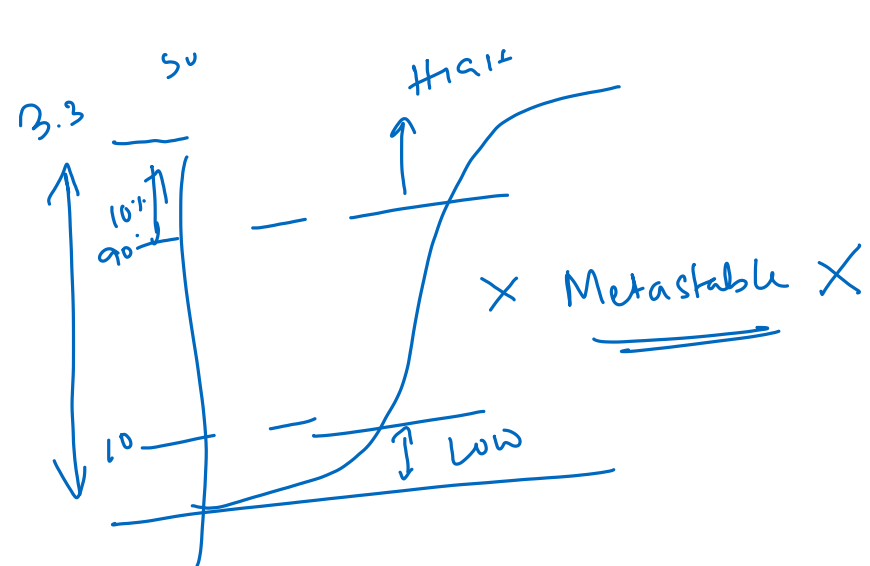
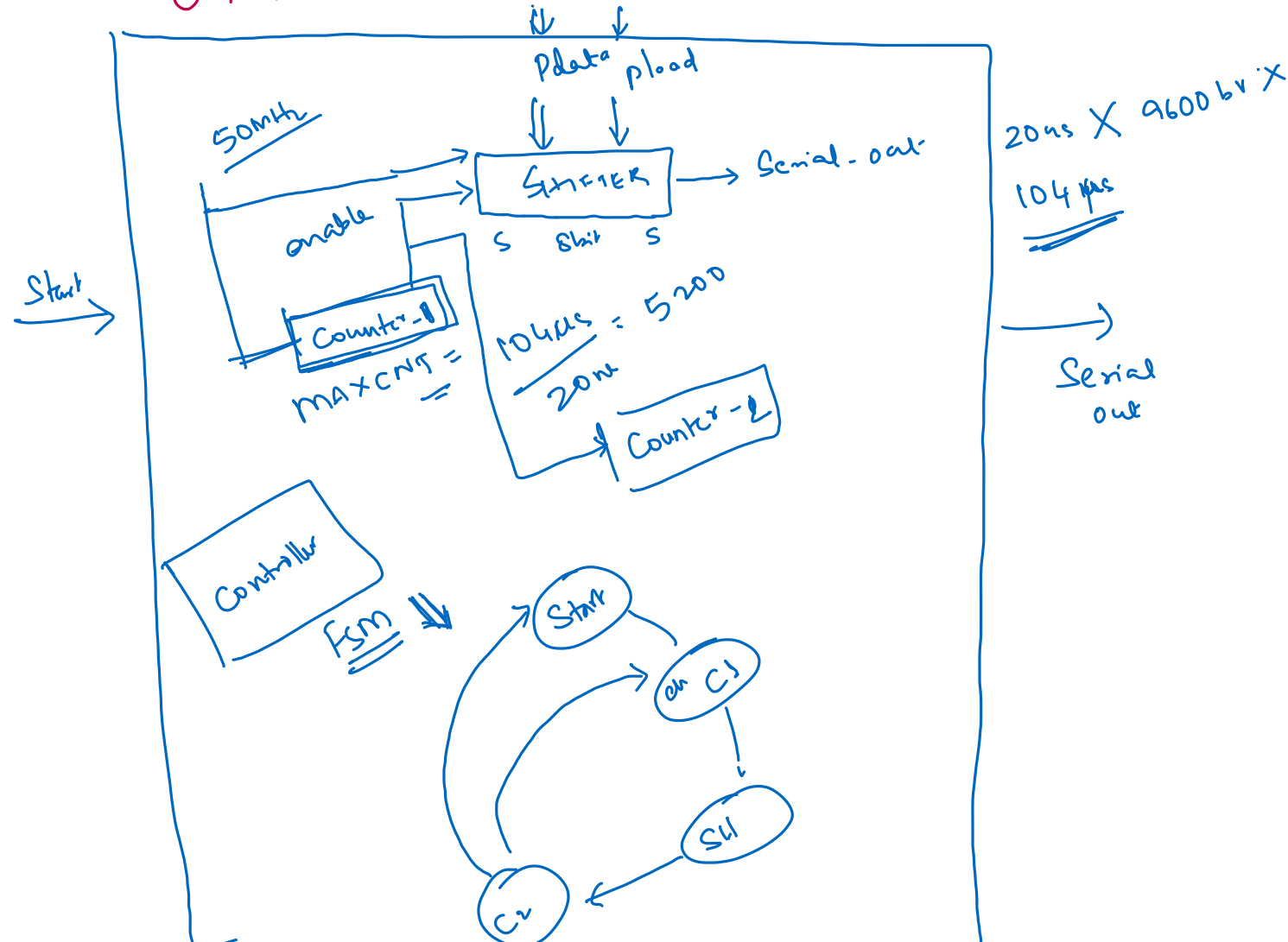
PS  
Processing System  
Region  
PL  
Programmable  
Logic Region

### UART System Design

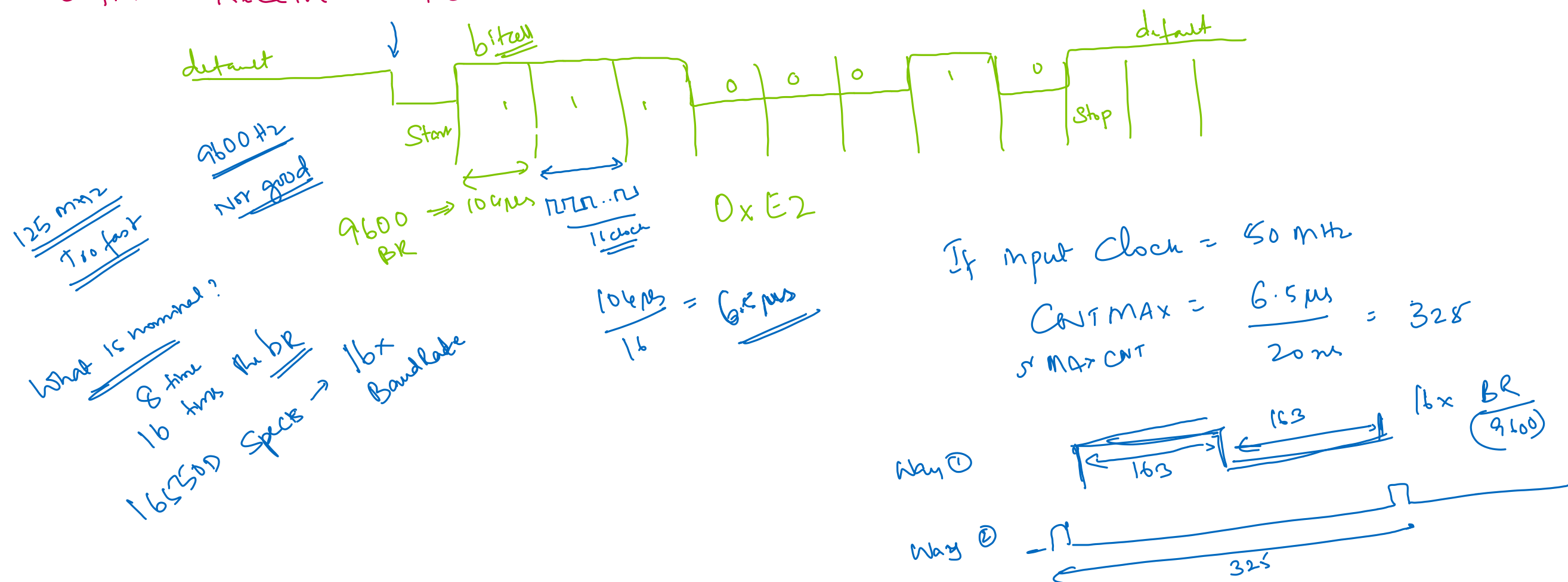
1 sec → 9600 bits  
 $\frac{1}{9600} = 0.104 \mu s$  ✓  
1.042



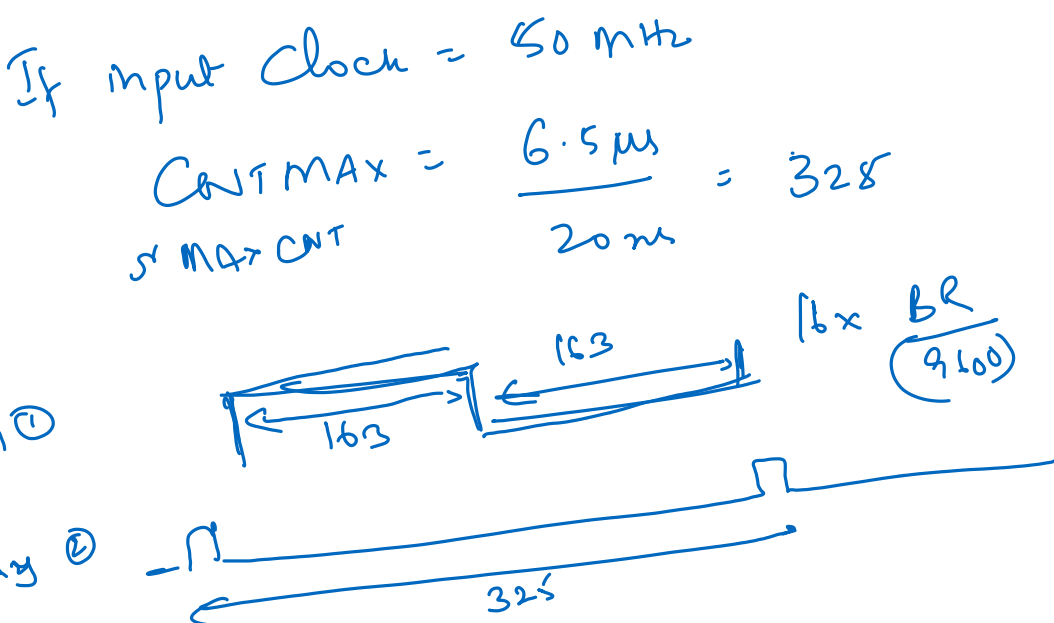
### UART Transmitter Micro Architecture:



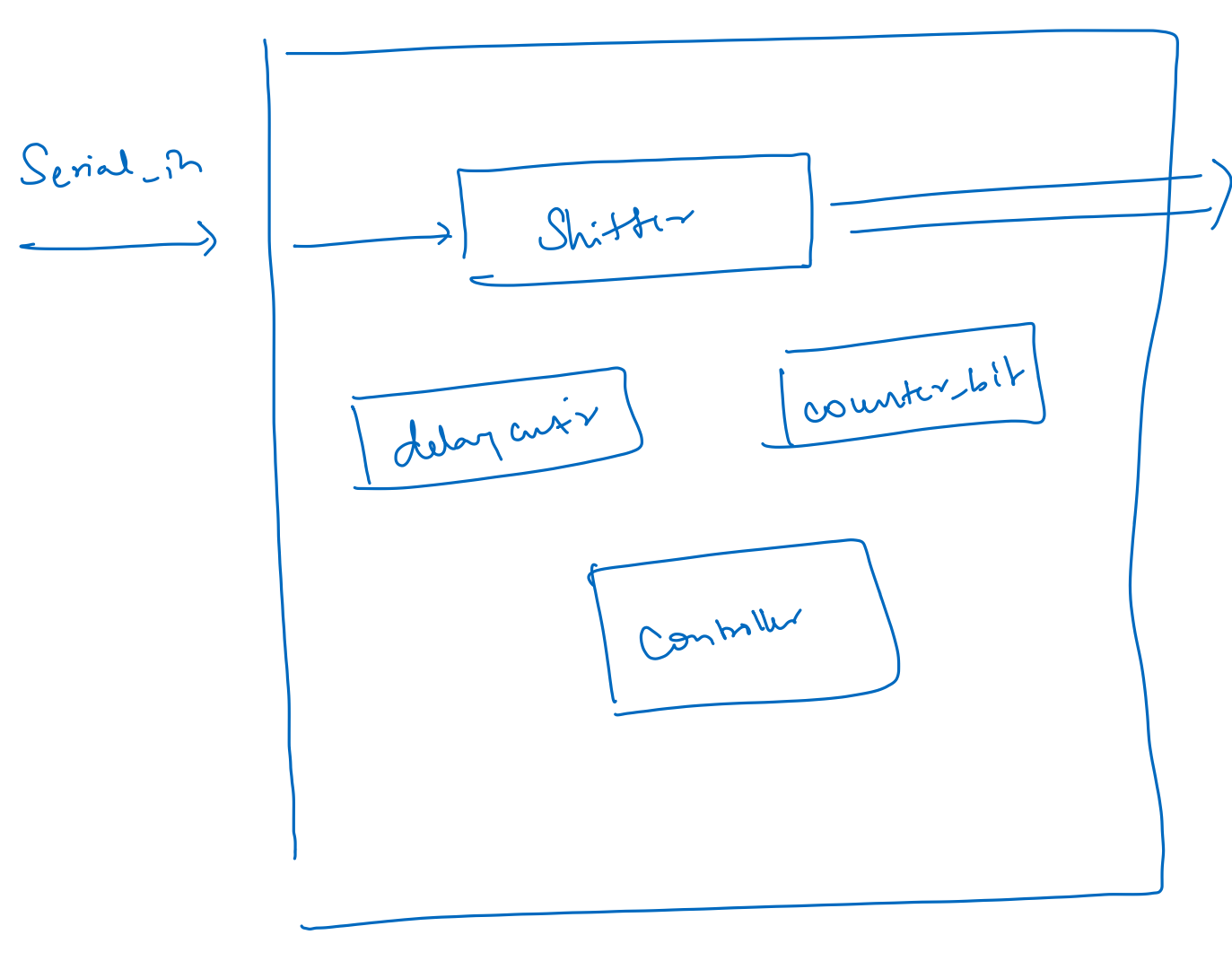
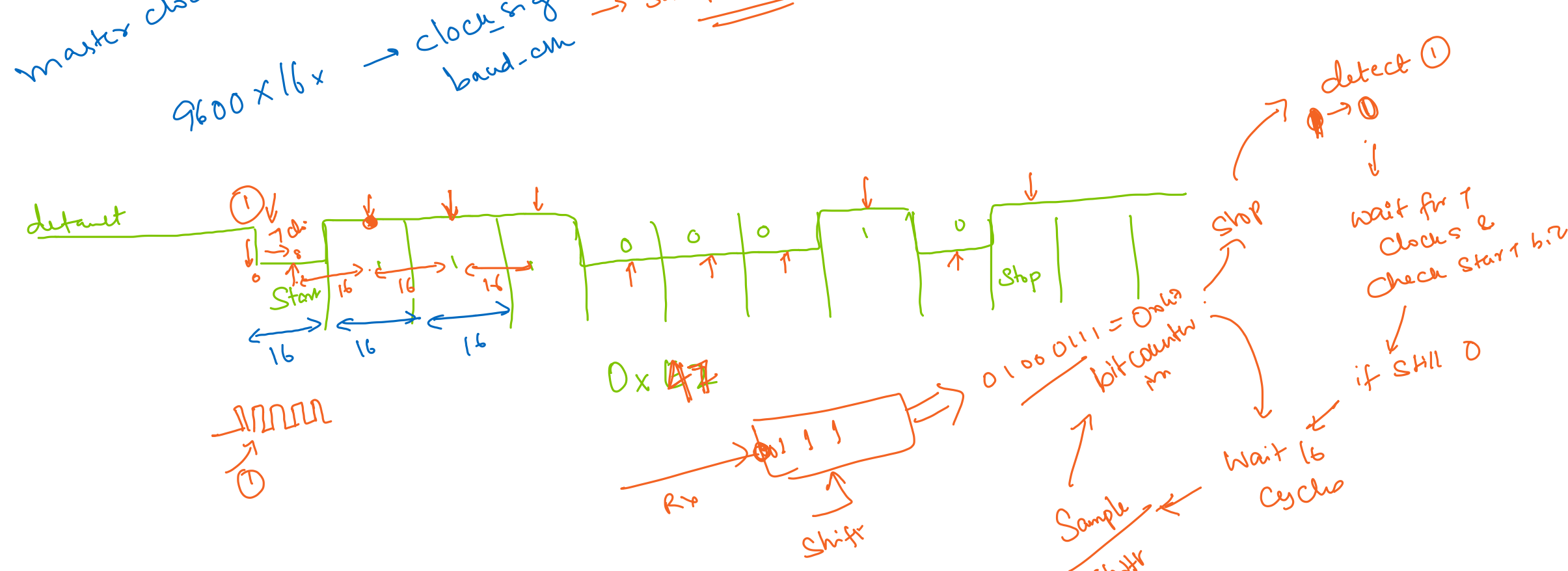
### UART Receiver Micro architecture



What is nominal?  
8 time the br  
16 time the br  
165500 Specs → 16x Baudrate



master clock = 50 MHz  
9600 x 16x → clock sig  
band-ctrl → Sampling signal



### UART

