



IP Integrator and IP Catalog

Objectives

- ▶ After completing this module, you will be able to:
 - Achieve greater design productivity using Vivado IP Integrator
 - Rapidly create and reuse subsystem level IP with Vivado and IP Integrator
 - Describe the IP Packager features
 - Differentiate between the free and evaluation base IP available in IP Catalog
 - Use the Clocking Wizard to configure and add clocking resources to the design

Outline

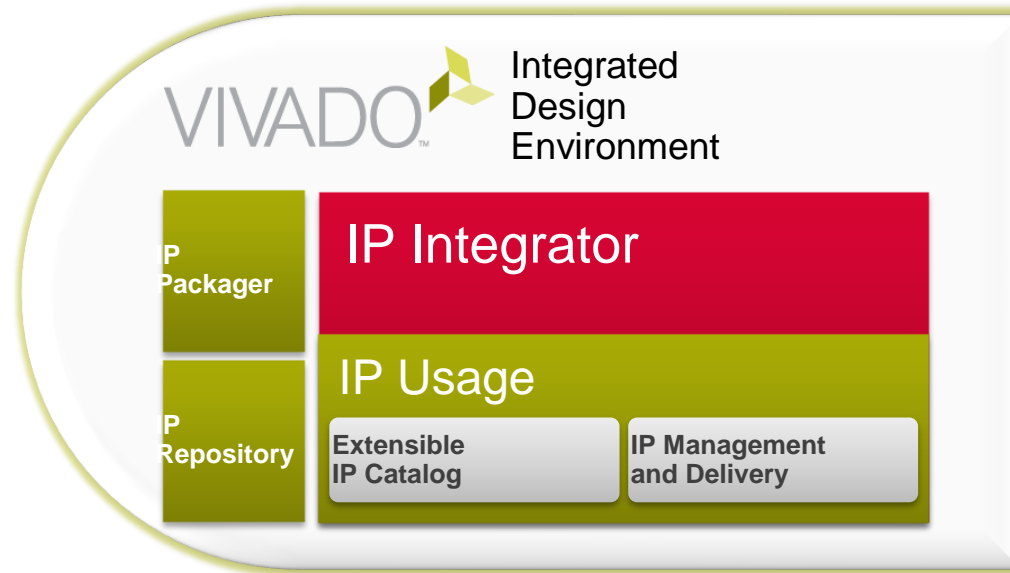
- ▶ *IP Integrator*
- ▶ IP Packager
- ▶ IP Catalog
- ▶ Clocking Wizard
- ▶ Summary

Challenges of Designing with Complex IP

- ▶ Modern IP contains multiple complex interfaces
 - Many signals, complex port mappings in RTL
 - Connectivity in overall design not apparent
- ▶ Modern IP is highly parameterizable
 - Designer must maintain consistency between interconnected IP blocks
 - Designer must understand interactions between blocks
- ▶ Subsystems containing multiple IP blocks are often difficult to capture and reuse
 - How to best capture IP for reuse
- ▶ To help designers be more productive when integrating IP, Xilinx has the IP Integrator in the Vivado Design Suite

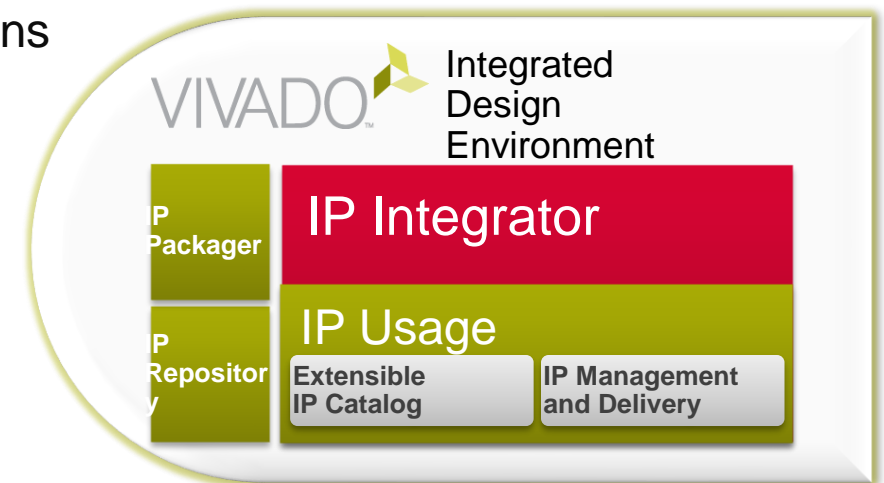
What is IP Integrator?

- ▶ A hierarchical IP integration tool for processor based and non-processor-based systems
- ▶ A graphical and scriptable IP configuration and connection environment



Benefits of Vivado IP Integrator

- ▶ Interface Level Connectivity
 - Connect complex interfaces between IP in a single step
 - Users can create custom interface definitions
- ▶ Integration and Reuse of IP
 - Rapid creation of complex IP by packaging the contents of a diagram
- ▶ Automatic Generation of HDL
 - Instantiates all IP in a diagram and makes all the interconnections
- ▶ Take advantage of IP metadata
 - Propagate correct parameters to connected IP
 - Recognition of unique data types
- ▶ Processor based system support



Vivado IP Integrator User Interface

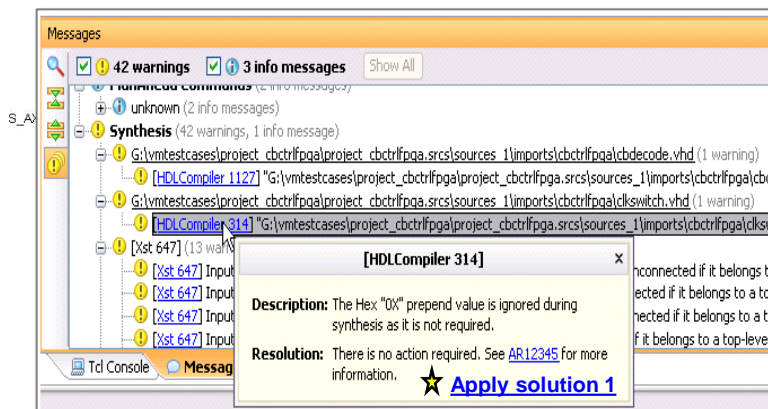
The screenshot displays the Vivado IP Integrator User Interface, which is used for creating and managing hardware designs. The interface is divided into several main sections:

- Flow Navigator:** Located on the left, it provides a high-level overview of the design process, including Project Manager, IP Integrator, Simulation, Implementation, and Program and Debug.
- System Hierarchy View:** This view shows the design hierarchy, including the project name, sources, and the design itself. It also displays the sub-block properties for the selected block.
- Interface Connections with Live DRCs:** This view shows the interface connections between the design blocks, including the AXI Interconnect, AXI Video Direct Memory Access, and AXI Memory Interconnect. It also displays the live Design Rule Checks (DRCs) for the design.
- Extensible IP Repository:** This view shows the IP repository, which contains a list of available IP blocks. The repository is searchable and includes a list of IP blocks with their descriptions and versions.
- TCL Console:** This console displays the Tcl commands and their output, providing a way to interact with the design and the IP repository.

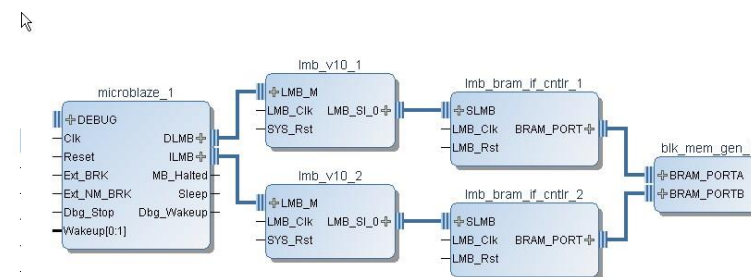
The interface also includes a top menu bar with options like File, Edit, Flow, Tools, Reports, Window, Layout, View, and Help. The bottom status bar shows the current design and the IP repository.

Intelligent IP Integration: Correct by Construction Design

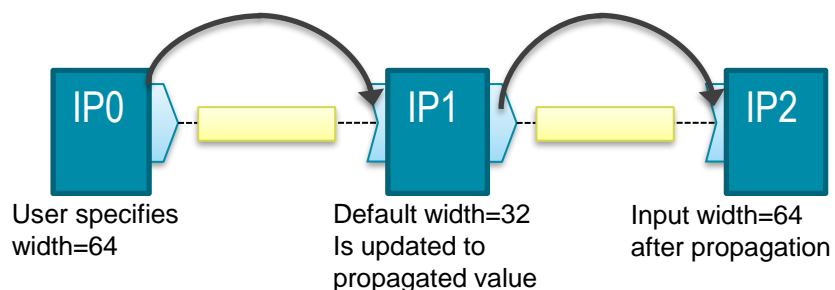
Real-time DRCs



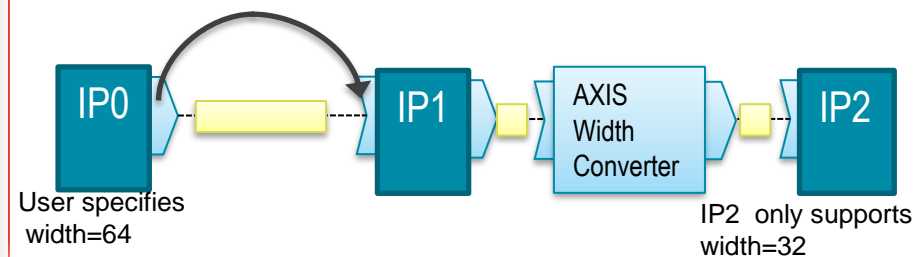
Auto Connection



Parameter Propagation



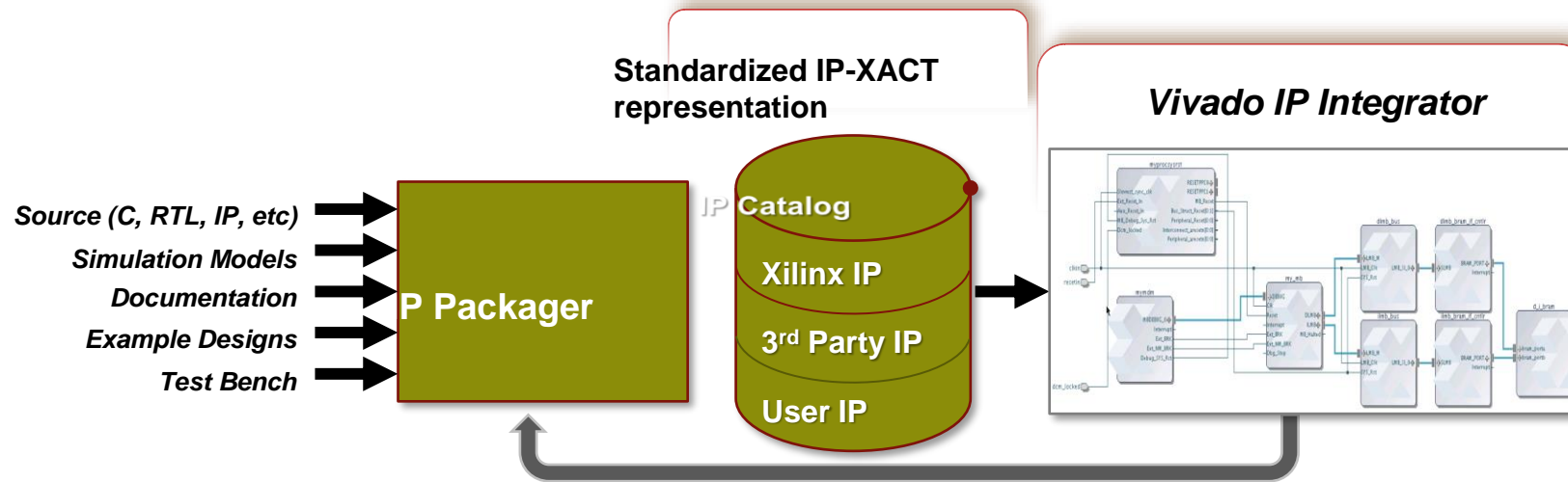
Parameter Resolution



IP Packager

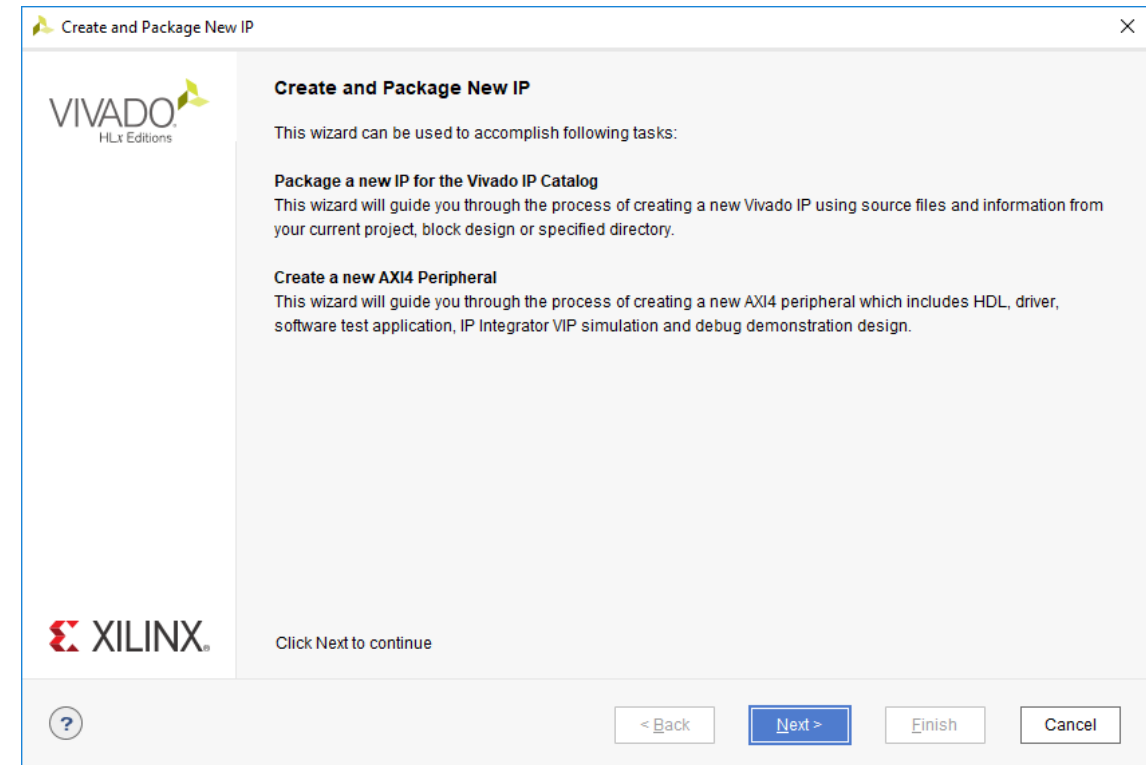
Reusing Your IP

- ▶ IP from many sources can be packaged and made available in Vivado
- ▶ All IP available in the Vivado IP Catalog can be used to create IP Integrator designs
- ▶ Any IP Integrator diagram can be quickly packaged as a single complex IP



Capture Your IP Using the Vivado IP Packager

- ▶ Wizard-based flow
 - Automates generation of IP-XACT IPs
 - Many pieces of meta-data automatically inferred
 - Users can add additional meta-data



Customizing IP for Reuse in IP Packager

Packaging Steps

- ✓ Identification
- ✓ Compatibility
- ✓ File Groups
- ✓ Customization Parameters
- ✓ Ports and Interfaces
- Addressing and Memory
- ✓ Customization GUI
- Review and Package

Identification

Vendor: xilinx.com

Library: XUP

Name: my_ip

Version: 1.0

Display name: my_ip

Description: Add your own description

Vendor display name:

Company url:

Root directory: c:/vivado_tutorial/lab3/lab3.srcs

Xml file name: c:/vivado_tutorial/lab3/lab3.srcs/component.xml

Categories

+ | - | ↑ | ↓

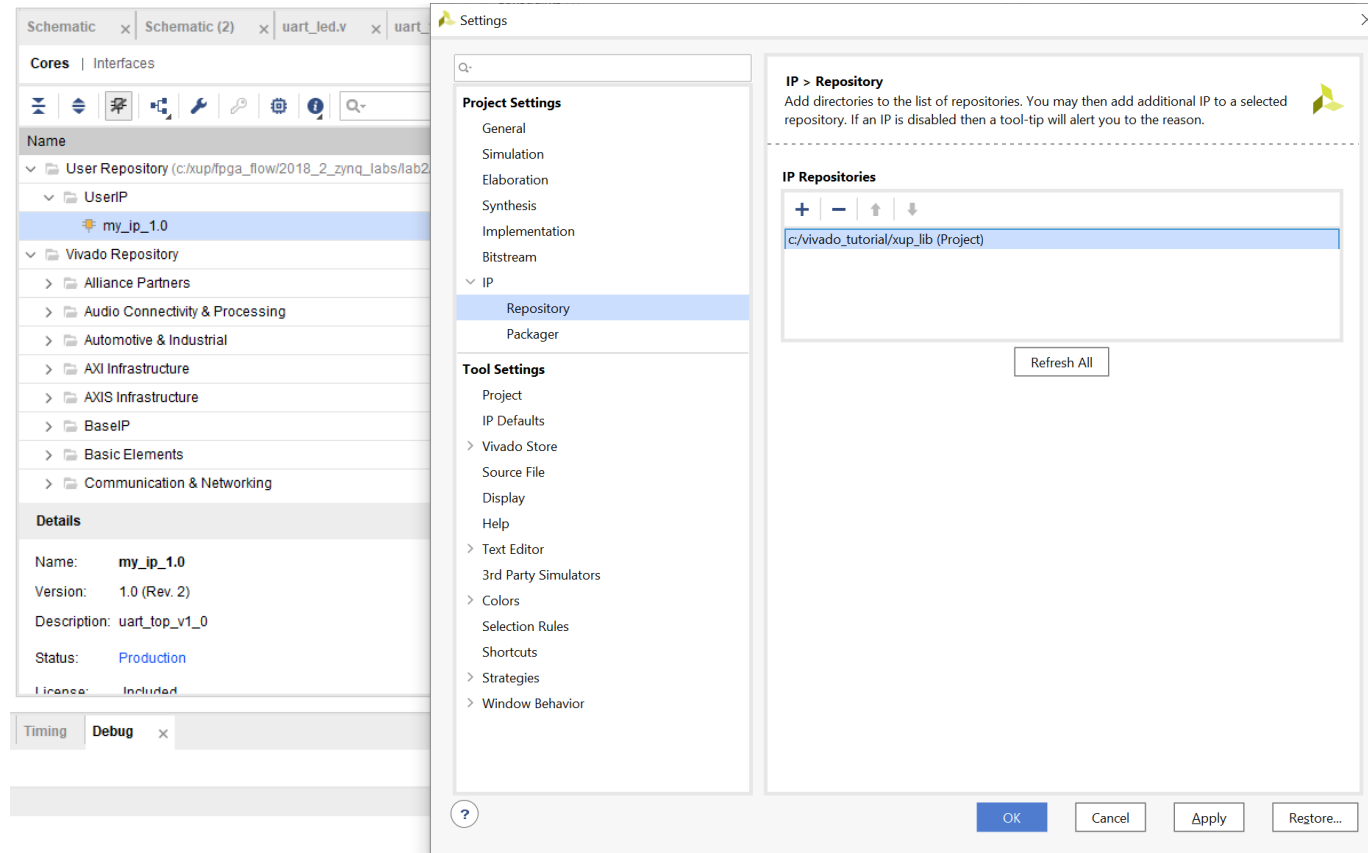
XUP_LIB

Select Options

Add, Edit or change defaults

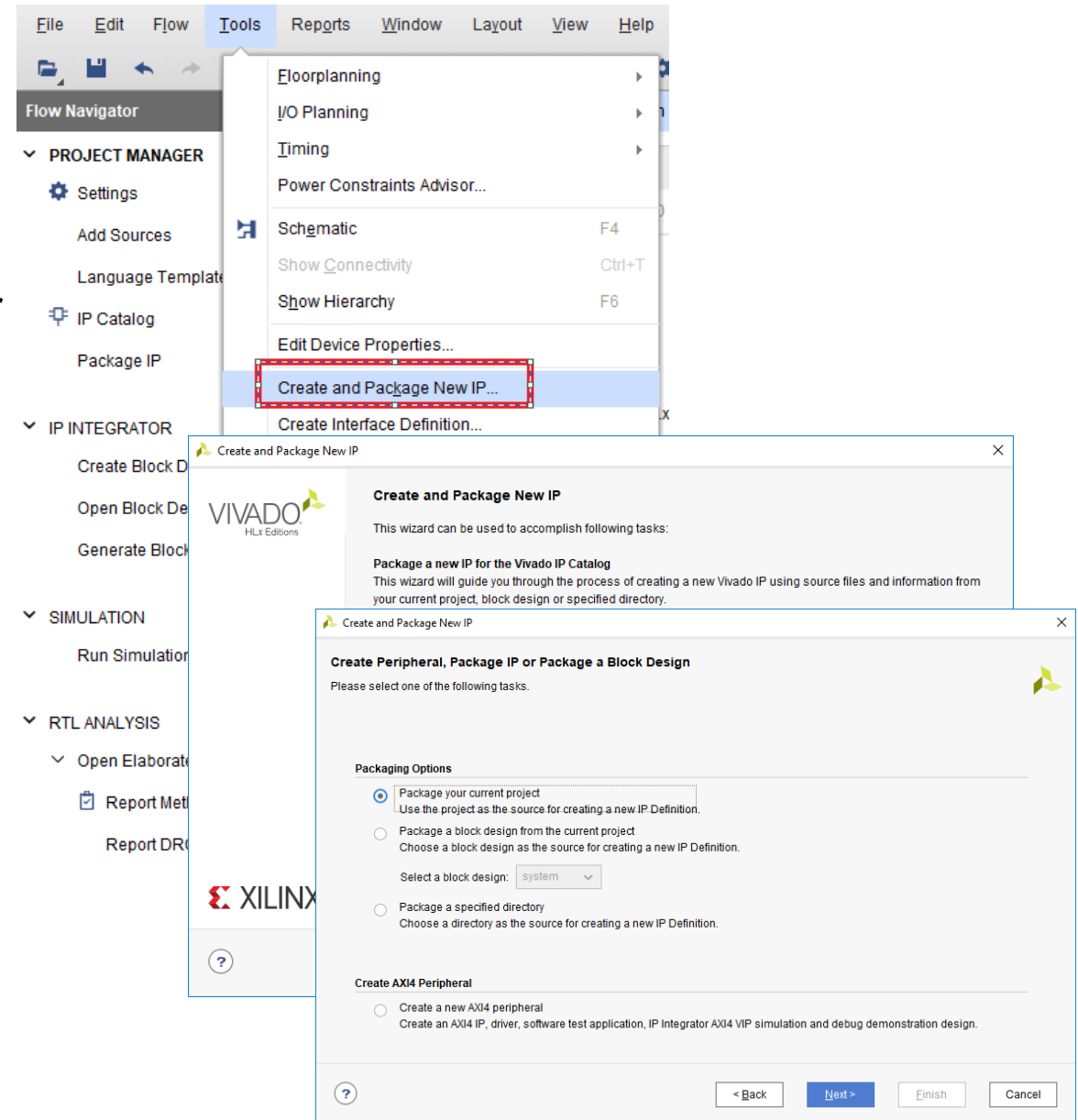
Using and Reusing Packaged IP

- ▶ The Vivado IP Catalog can be extended by adding additional IP Repositories. Third party IP, your custom IP, and Xilinx provided IP are displayed in the identical manner



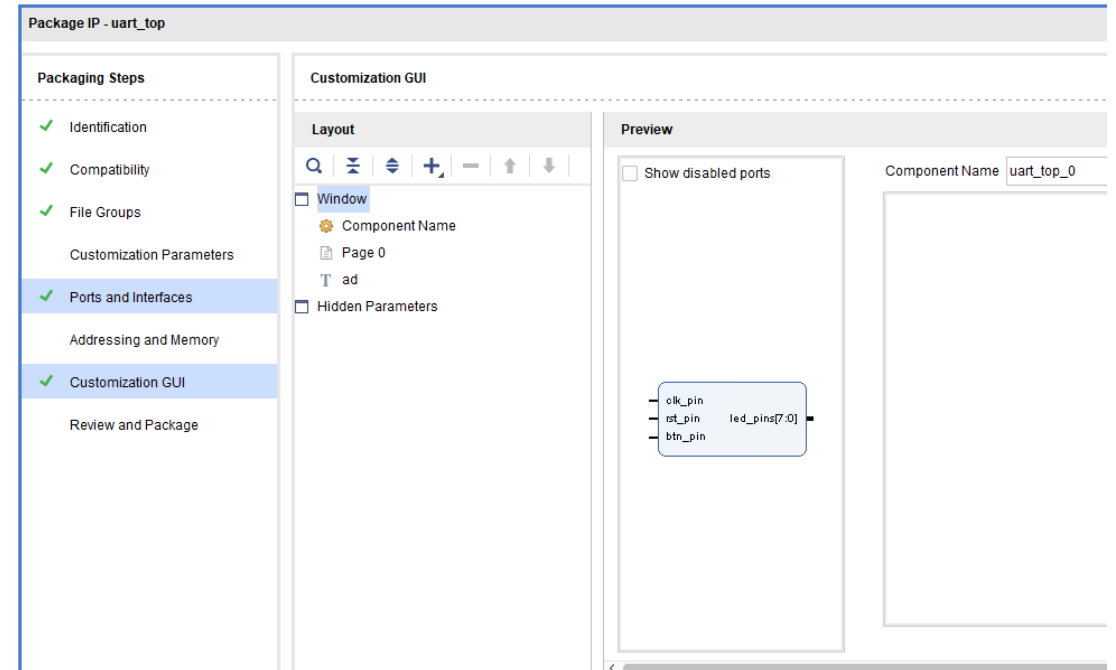
IP Packager

- ▶ The IP Packager allows a core to be packaged and included in the IP Catalog, or for distribution
- ▶ Complete set of files include
 - Source code, Constraints, Test Benches (simulation files), documentation
- ▶ IP Packager can be run from Vivado on the current project, or on a specified directory



IP Packager

- ▶ Automatically analyse project/files to determine parameters
- ▶ Initial Summary
- ▶ Identifies
 - Files
 - Parameters
 - Ports
 - Interfaces
- ▶ Creates GUI Layout for IPI



IP Packager

- ▶ Modify configuration
 - Properties
 - Compatibility
 - Files
 - Custom parameters
 - Ports
 - Interfaces
 - Address and Memory
 - IP and security

Project Summary × Package IP - uart_led ×

Packaging Steps

- ✓ Identification
- ✓ Compatibility
- ✓ File Groups
- ✓ Customization Parameters
- ✓ Ports and Interfaces
- Addressing and Memory
- ✓ Customization GUI
- Review and Package

Identification

Vendor: xilinx.com

Library: XUP

Name: my_ip

Version: 1.0

Display name: my_ip

Description: Add your own description

Vendor display name:

Company url:

Root directory: c:/vivado_tutorial/lab3/lab3.srcs

Xml file name: c:/vivado_tutorial/lab3/lab3.srcs/component.xml

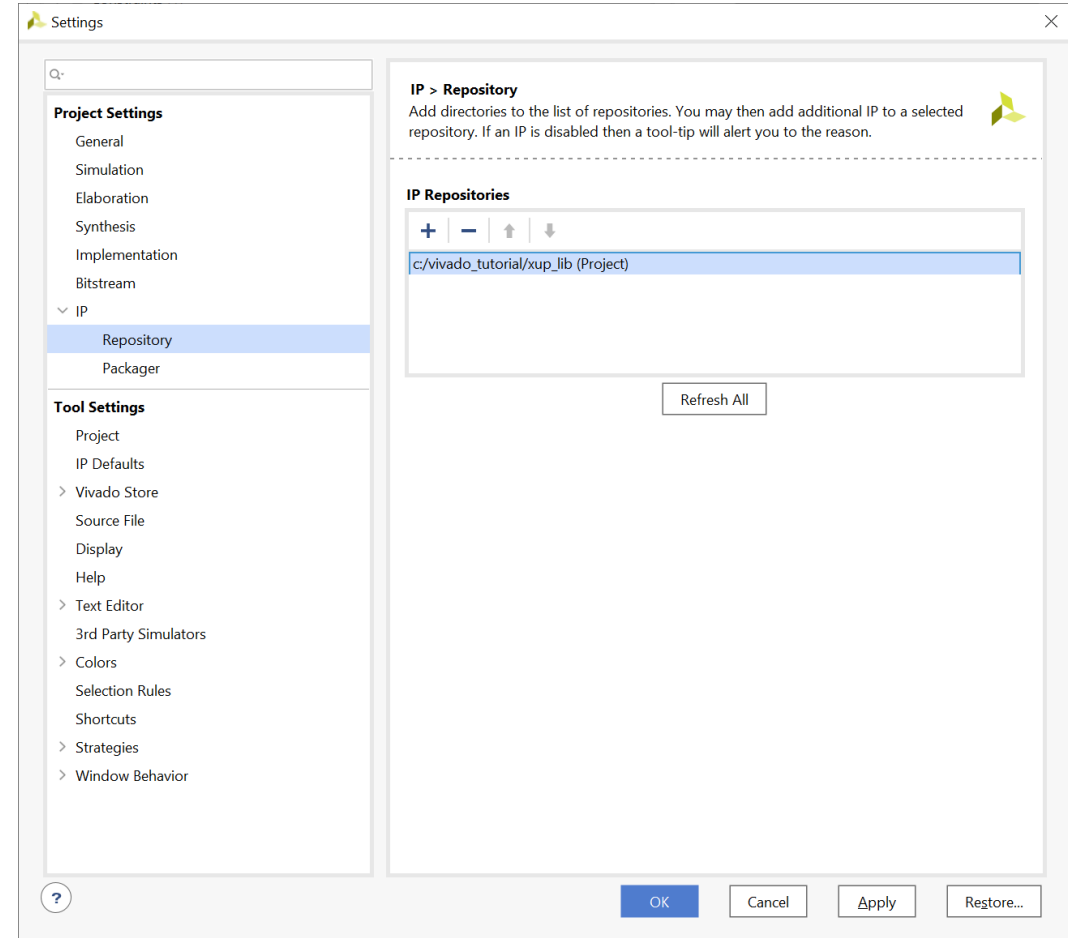
Categories

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XUP_LIB

IP Repository

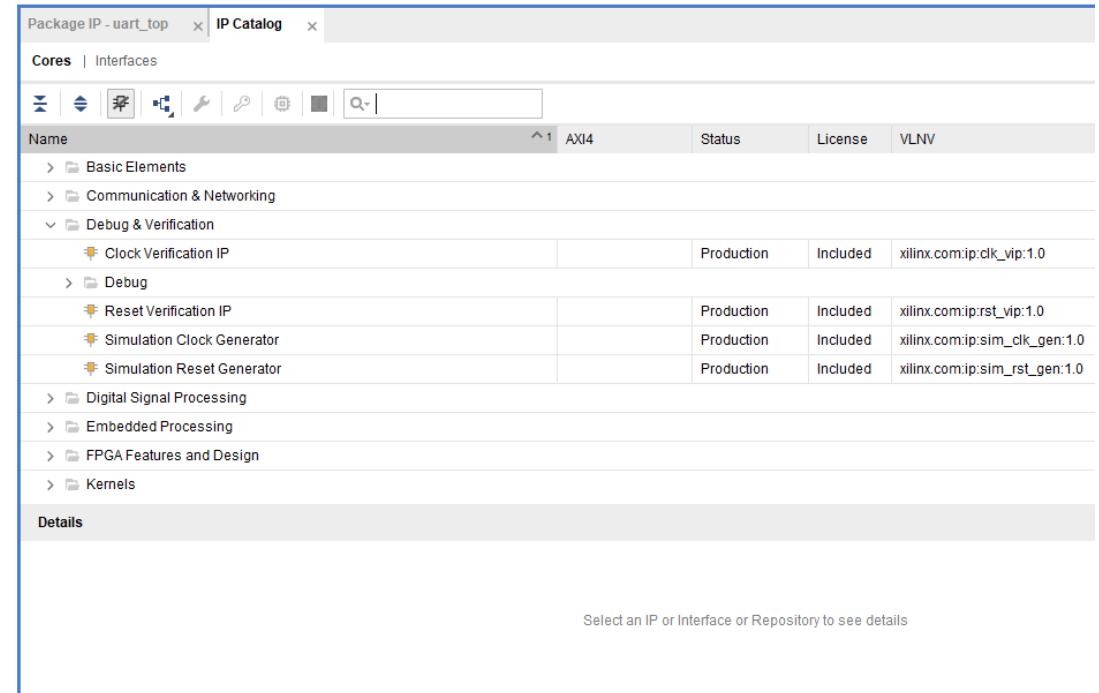
- ▶ Creates component.xml file for the IP
- ▶ Specify the directory in the repository
- ▶ Displays IP in the repository



IP Catalog

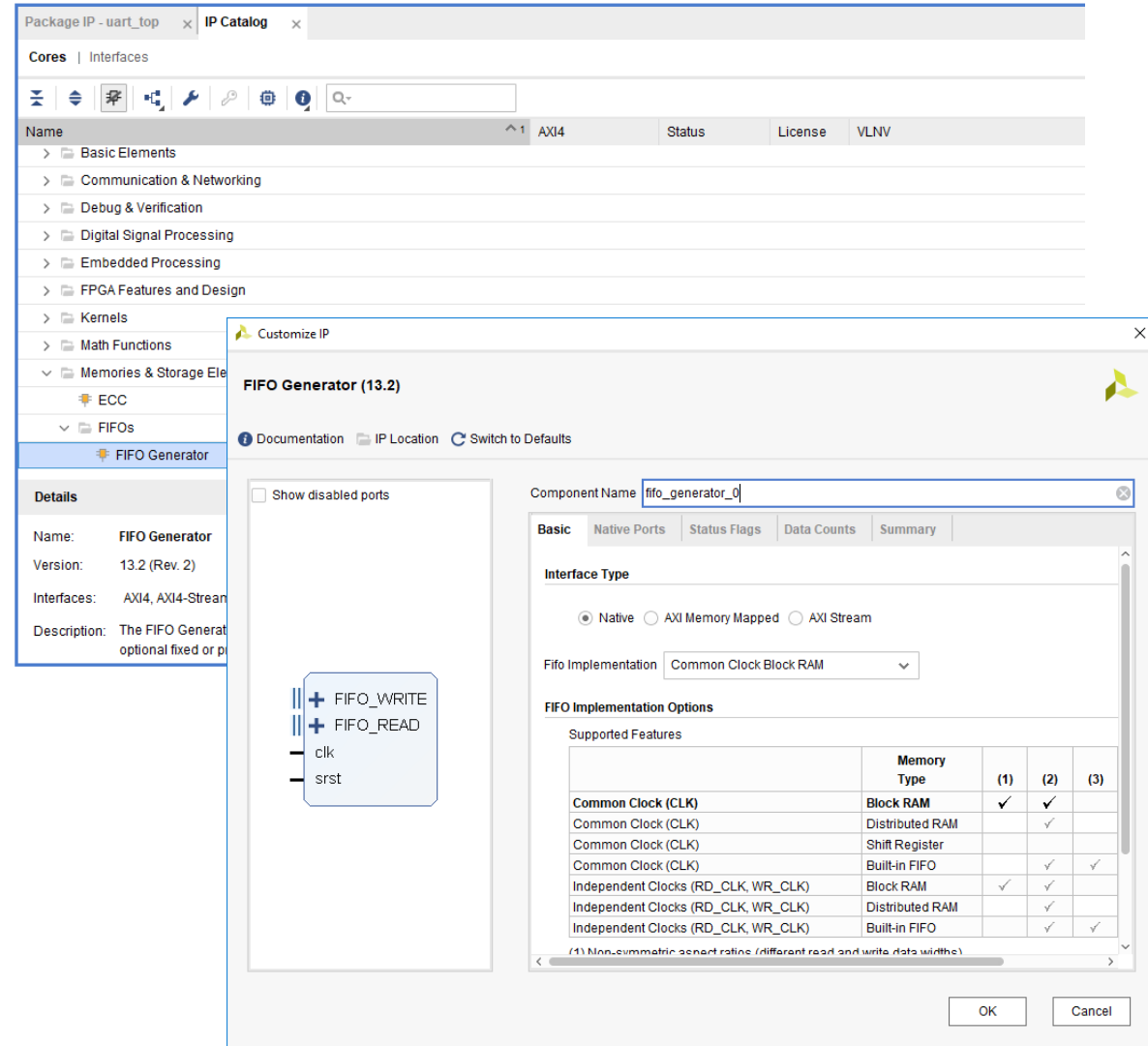
IP Catalog

- ▶ The IP Catalog contain a collection of IP that can be used to assemble a system
- ▶ Supported by IPI
- ▶ Facilitates quick system construction
- ▶ Each IP block has its own configuration parameters
- ▶ Most of the IP are free, some require licenses
- ▶ Stored as source code in the install directory
 - Always synthesized with the latest tools
 - Some proprietary source code is encrypted



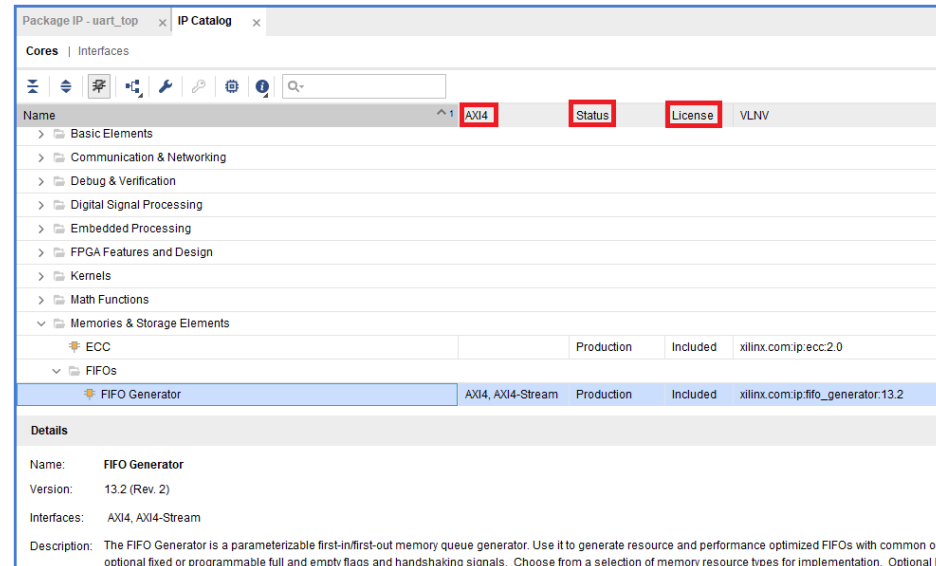
Vivado IP Catalog

- ▶ Integrated IP Support
 - Instant access to IP customization
 - Vivado IP GUI look and feel
 - Support for Vivado synthesis and implementation
 - Selectable IP output products
 - Full Tcl support



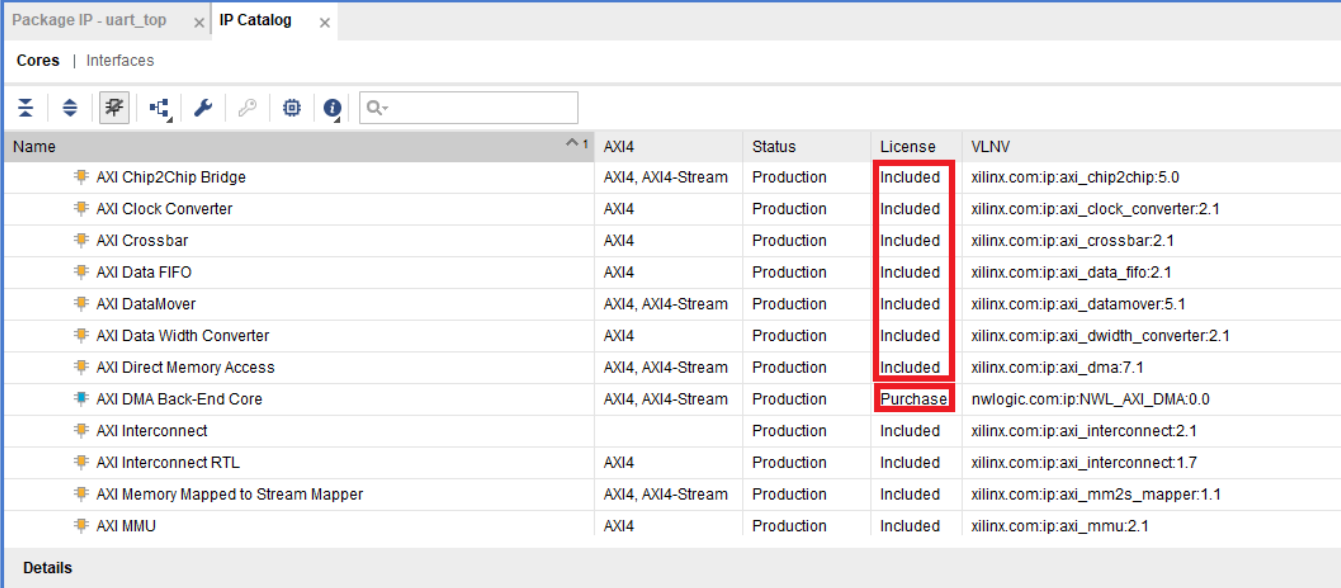
Peripheral and Non-Peripheral Type IP

- ▶ Many IP in the catalog are peripheral type
 - Peripheral type are indicated by AXI4, AXI4-Stream
- ▶ Non-peripheral IP listing do not have entry in the AXI4 column
- ▶ Status column indicates if the IP is of production or pre-production category
- ▶ License column indicates if the IP is free (Included) or costs money (Purchase)



IP Peripherals Included as Source (Free)

- ▶ Bus and bridge controllers
- ▶ Debug cores
- ▶ DMA and Timers
- ▶ Inter-processor communication
- ▶ External peripheral controller Memory and memory controller
- ▶ High-speed and low-speed communication peripherals
- ▶ Other cores



Package IP - uart_top x IP Catalog x				
Cores Interfaces				
Name	AXI4	Status	License	VLNV
AXI Chip2Chip Bridge	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip:axi_chip2chip:5.0
AXI Clock Converter	AXI4	Production	Included	xilinx.com:ip:axi_clock_converter:2.1
AXI Crossbar	AXI4	Production	Included	xilinx.com:ip:axi_crossbar:2.1
AXI Data FIFO	AXI4	Production	Included	xilinx.com:ip:axi_data_fifo:2.1
AXI DataMover	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip:axi_datamover:5.1
AXI Data Width Converter	AXI4	Production	Included	xilinx.com:ip:axi_dwidth_converter:2.1
AXI Direct Memory Access	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip:axi_dma:7.1
AXI DMA Back-End Core	AXI4, AXI4-Stream	Production	Purchase	nwlogic.com:ip:NWL_AXI_DMA:0.0
AXI Interconnect		Production	Included	xilinx.com:ip:axi_interconnect:2.1
AXI Interconnect RTL	AXI4	Production	Included	xilinx.com:ip:axi_interconnect:1.7
AXI Memory Mapped to Stream Mapper	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip:axi_mm2s_mapper:1.1
AXI MMU	AXI4	Production	Included	xilinx.com:ip:axi_mmu:2.1
Details				

IP Cores Included as Evaluation

- ▶ AXI CAN controller
- ▶ AXI USB2 device
- ▶ Video IP
- ▶ Telecoms/ Wireless IP

Package IP - uart_top x IP Catalog x				
Cores Interfaces				
Name				
> SDAccel DSA Infrastructure	AXI4	Status	License	VLNV
> Standard Bus Interfaces				
> PCI				
SD Card Host Controller	AXI4	Production	Purchase	logicbricks.com:logicbricks:logisdhc:0.0
> Video & Image Processing				
2D Graphics Accelerator Bit Block Transfer	AXI4	Production	Purchase	logicbricks.com:logicbricks:logibitbtt:0.0
AXI4-Stream to Video Out	AXI4-Stream	Production	Included	xilinx.com:ip:v_axi4s_vid_out:4.0
AXIS FIFO monitor	AXI4, AXI4-Stream	Production	Purchase	omnitek.tv:ip:omni_axis_fifo_mon:0.0
AXIS N to M	AXI4, AXI4-Stream	Production	Purchase	omnitek.tv:ip:omni_axis_n_to_m:0.0
AXI Video Direct Memory Access	AXI4, AXI4-Stream	Production	Included	xilinx.com:ip:axi_vdma:6.3
Bitmap 2.5D Graphics Accelerator	AXI4	Production	Purchase	logicbricks.com:logicbricks:logibmp:0.0
Chroma Down-Sampler	AXI4, AXI4-Stream	Production	Purchase	omnitek.tv:ip:omni_chroma_down:0.0

Xilinx IP Evaluation

Register for Access

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IP Evaluation Package Formats

IP Evaluation packages may be provided with the following:

- Vivado® Design Suite
- ISE® Design Suite CORE Generator™ IP customization GUIs
 - Use these to generate IP implementation netlists and Unisim-based functional simulation models
- 4 Month Hardware Evaluation License Keys
 - Many cores can be evaluated in hardware either "out of the box" (Processor/EDK IP cores), or after installing a Full System Evaluation License Key (applies to most fee-based cores shipped with Vivado). Such cores typically cease to function in a programmed device after some number of hours. The actual number of hours varies, depending upon the core.

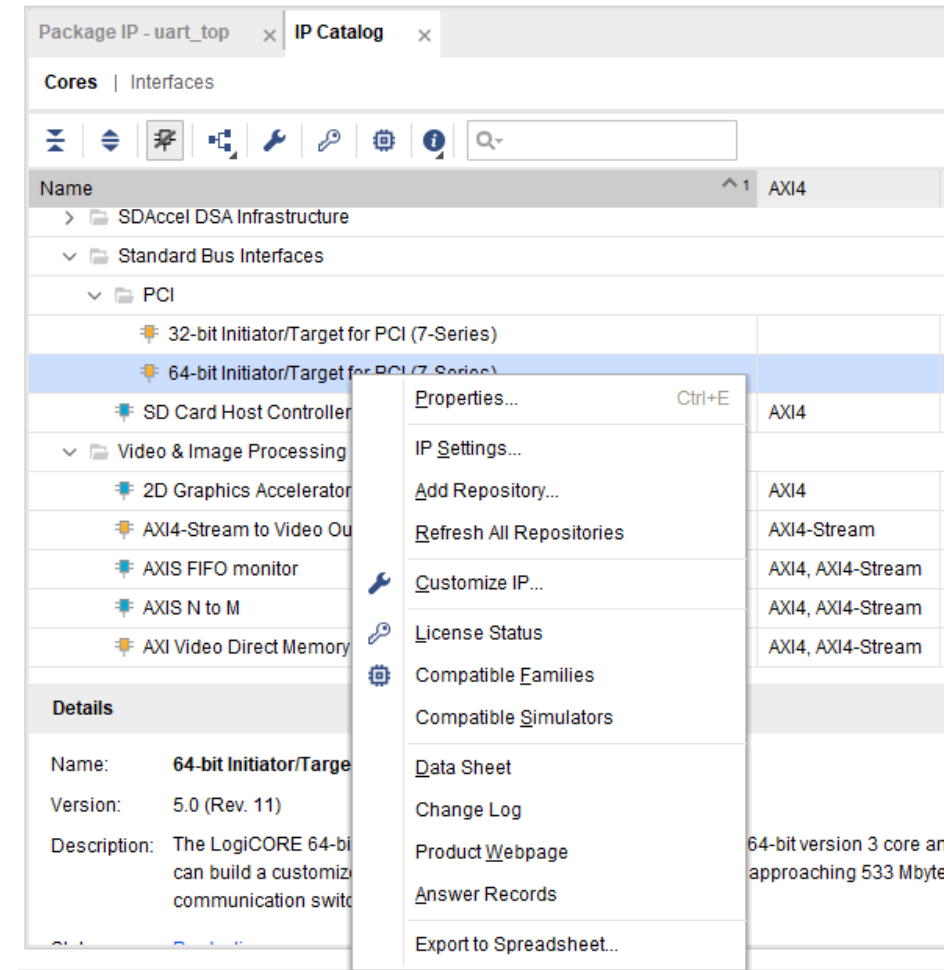
In some limited cases, the following may be provided instead:

IP customization GUIs which can be used to generate tailored, off-the-shelf, hardware models for simulation

Xilinx developed, delivered, and supported Evaluation IP installs with a 90-day evaluation license

IP Cores

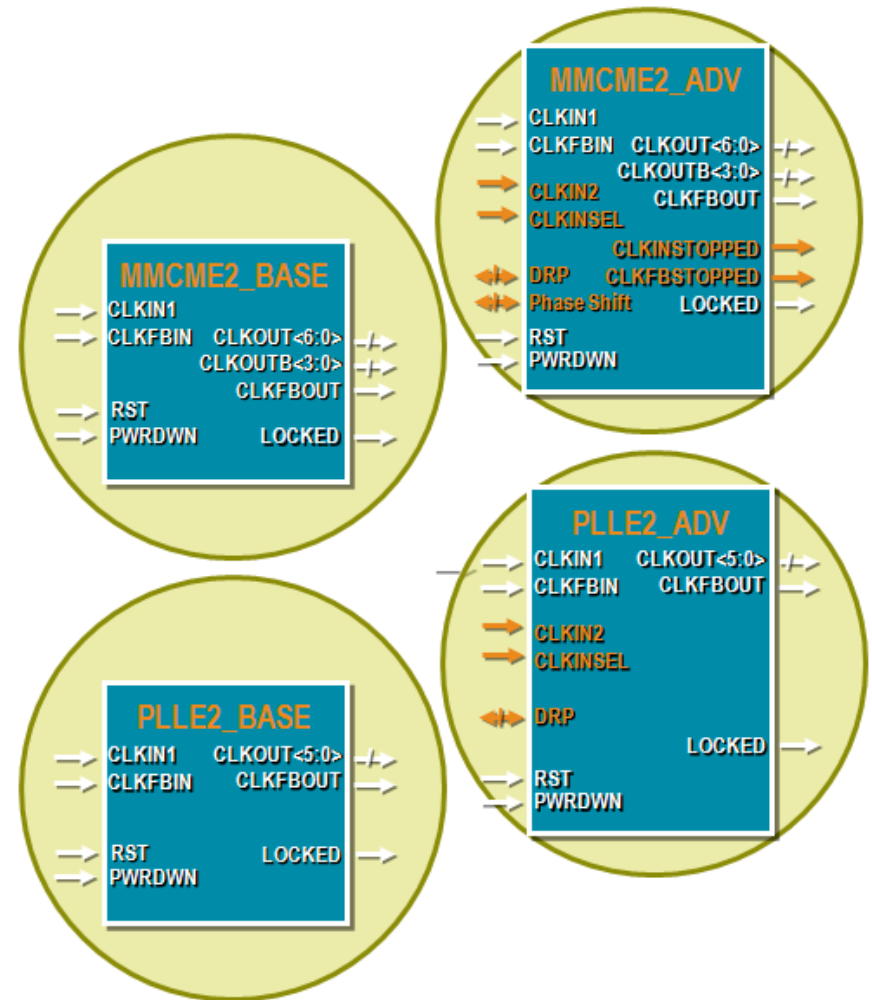
- ▶ Right click to customize
- ▶ Determine compatibility
- ▶ Product Guide (datasheet) > Document Navigator
- ▶ Change Log
- ▶ Product Webpage
- ▶ Answer record
- ▶ Export complete IP Catalog to excel



Clocking Wizard

Clocking Resources: MMCM and PLL


- ▶ Up to 24 CMTs per device
- ▶ One MMCM and one PLL per CMT
- ▶ Two software primitives (instantiation)
 - *_BASE has only the basic ports
 - *_ADV provides access to all ports
- ▶ PLL is primarily intended for use with the I/O phaser for high-speed memory controllers
- ▶ The MMCM is the primary clock resource for user clocks



Inference

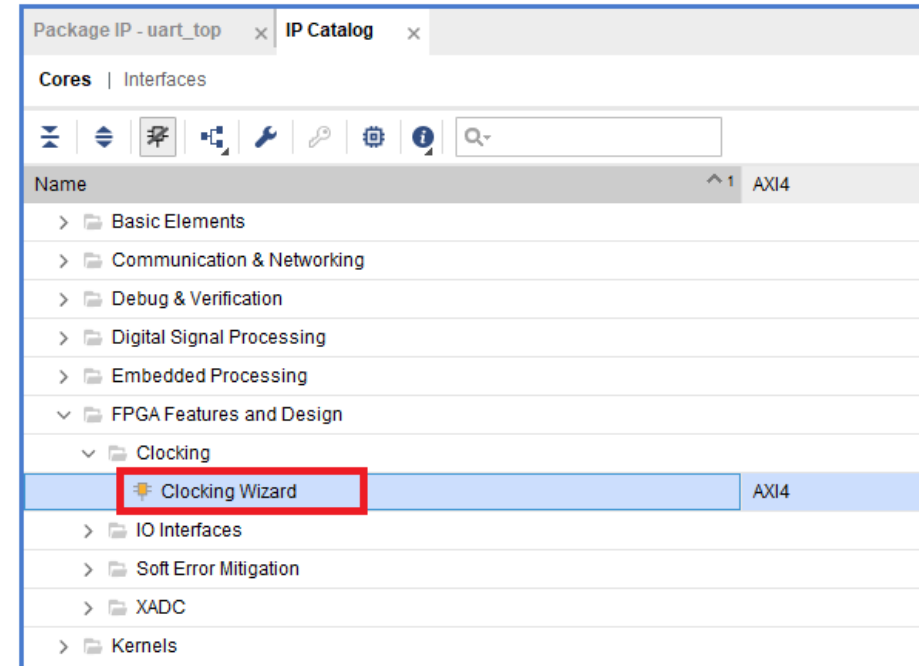
- ▶ Clock networks are represented by nets in your RTL design
 - The mapping of an RTL net to a clock network is managed by using the appropriate clock buffer to generate that net
- ▶ Certain resources can be inferred
 - A primary input net (with or without an IBUF instantiated) will be mapped to a global clock if it drives the clock inputs of clocked resources
 - The BUFG will be inferred
 - BUFH drivers will be inferred whenever a global clock (driven by a BUFG) is required in a clock region
 - BUFHs for each region required will be inferred
- ▶ BUFIO, BUFR, and BUFMR cannot be inferred
 - Instantiating these buffers tells the tools that you want to use the corresponding clock networks
- ▶ PLLs and MMCMs cannot be inferred

Instantiation

- ▶ All clocking resources can be directly instantiated in your RTL code
 - Simulation models exist for all resources
 - Refer to the Library Guide for HDL Designs
 - Use the Language Templates () 
- ▶ PLLs and MMCMs have many inputs and outputs, as well as many attributes
 - Optimal dividers for obtaining the desired characteristics may be hard to derive
 - The Clocking Wizard via the IP Catalog
 - Only *_ADV available

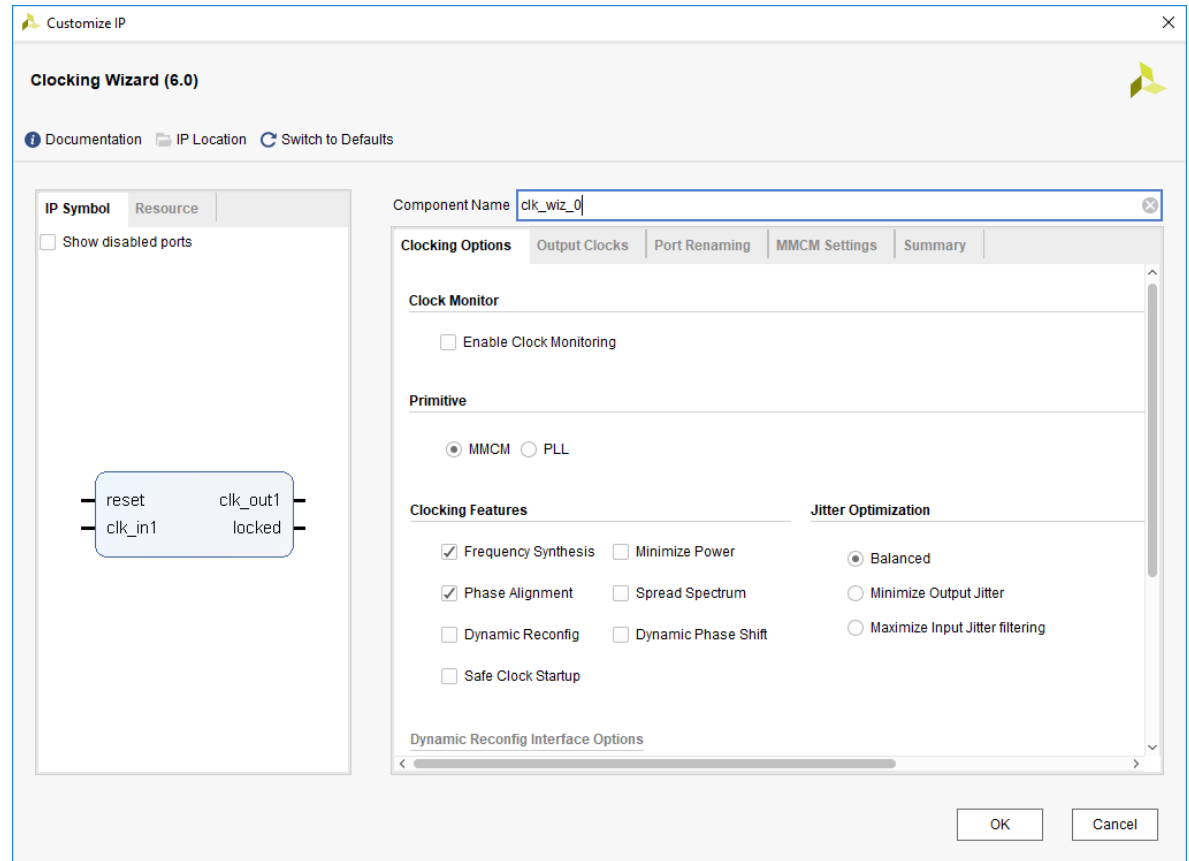
Invoking Clocking Wizard

- ▶ Click on the IP Catalog
- ▶ Expand FPGA Features and Design > Clocking
- ▶ Double-click on Clocking Wizard
- ▶ The Clocking Wizard walks you through the generation of complete clocking subsystems



The Clocking Wizard: Clocking Options

- ▶ Select Primitives to be used
 - MMCME2_ADV
 - PLLE2_ADV
- ▶ Specify the primary input frequency and source type
 - Optionally, select and specify secondary input clock
- ▶ Select clocking features
 - Frequency synthesis
 - Phase alignment
 - Dynamic phase shift
 - ...



The Clocking Wizard: Output Clocks

- ▶ Select the desired number of output clocks
- ▶ Set the desired output frequencies
- ▶ Select optional ports

Customize IP

Clocking Wizard (6.0)

Documentation IP Location Switch to Defaults

Component Name: clk_wiz_0

Output Clocks

The phase is calculated relative to the active input clock.

Output Clock	Port Name	Output Freq (MHz)		Phase (degrees)		R
		Requested	Actual	Requested	Actual	
<input checked="" type="checkbox"/> clk_out1	clk_out1	100.000	100.000	0.000	0.000	5
<input type="checkbox"/> clk_out2	clk_out2	100.000	N/A	0.000	N/A	5
<input type="checkbox"/> clk_out3	clk_out3	100.000	N/A	0.000	N/A	5
<input type="checkbox"/> clk_out4	clk_out4	100.000	N/A	0.000	N/A	5
<input type="checkbox"/> clk_out5	clk_out5	100.000	N/A	0.000	N/A	5
<input type="checkbox"/> clk_out6	clk_out6	100.000	N/A	0.000	N/A	5
<input type="checkbox"/> clk_out7	clk_out7	100.000	N/A	0.000	N/A	5

☐ USE CLOCK SEQUENCING

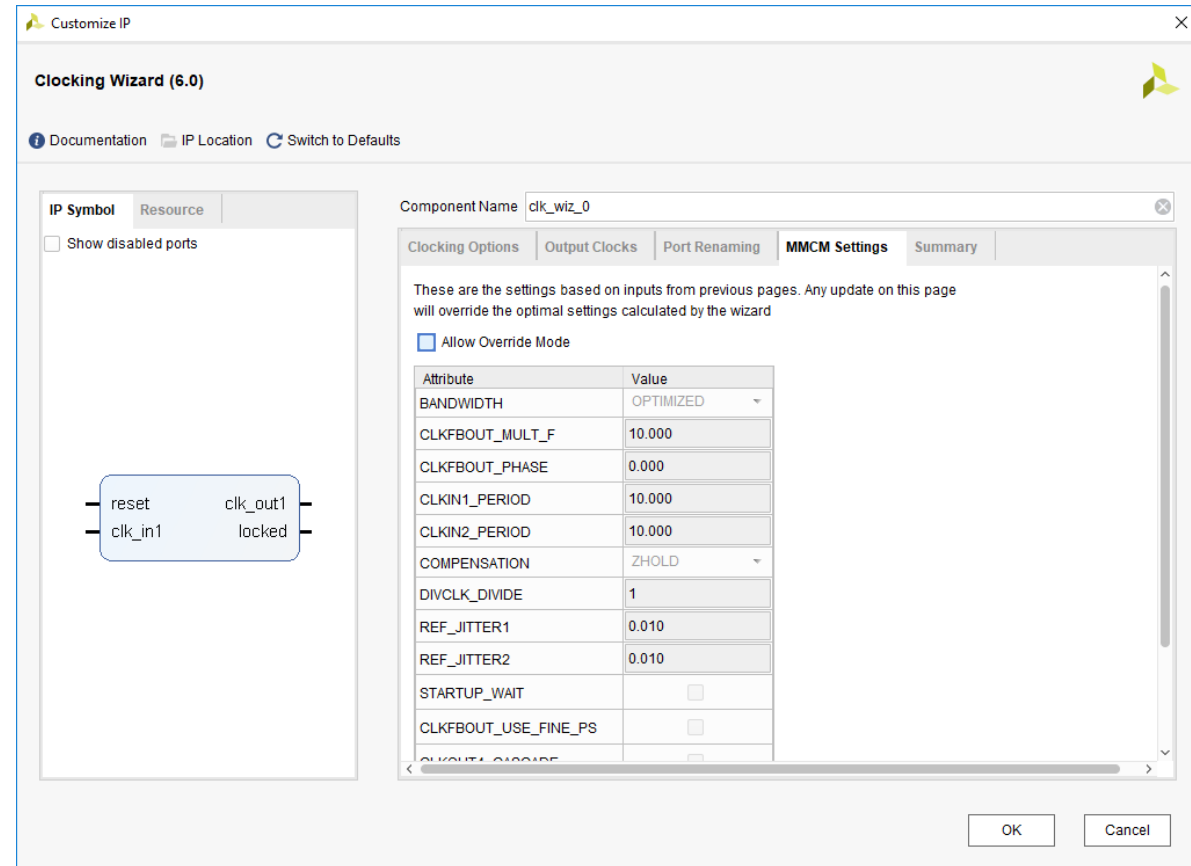
Clocking Feedback

Output Clock	Sequence Number	Source	Signaling
clk_out1	1	Automatic Control On-Chip	Single

OK Cancel

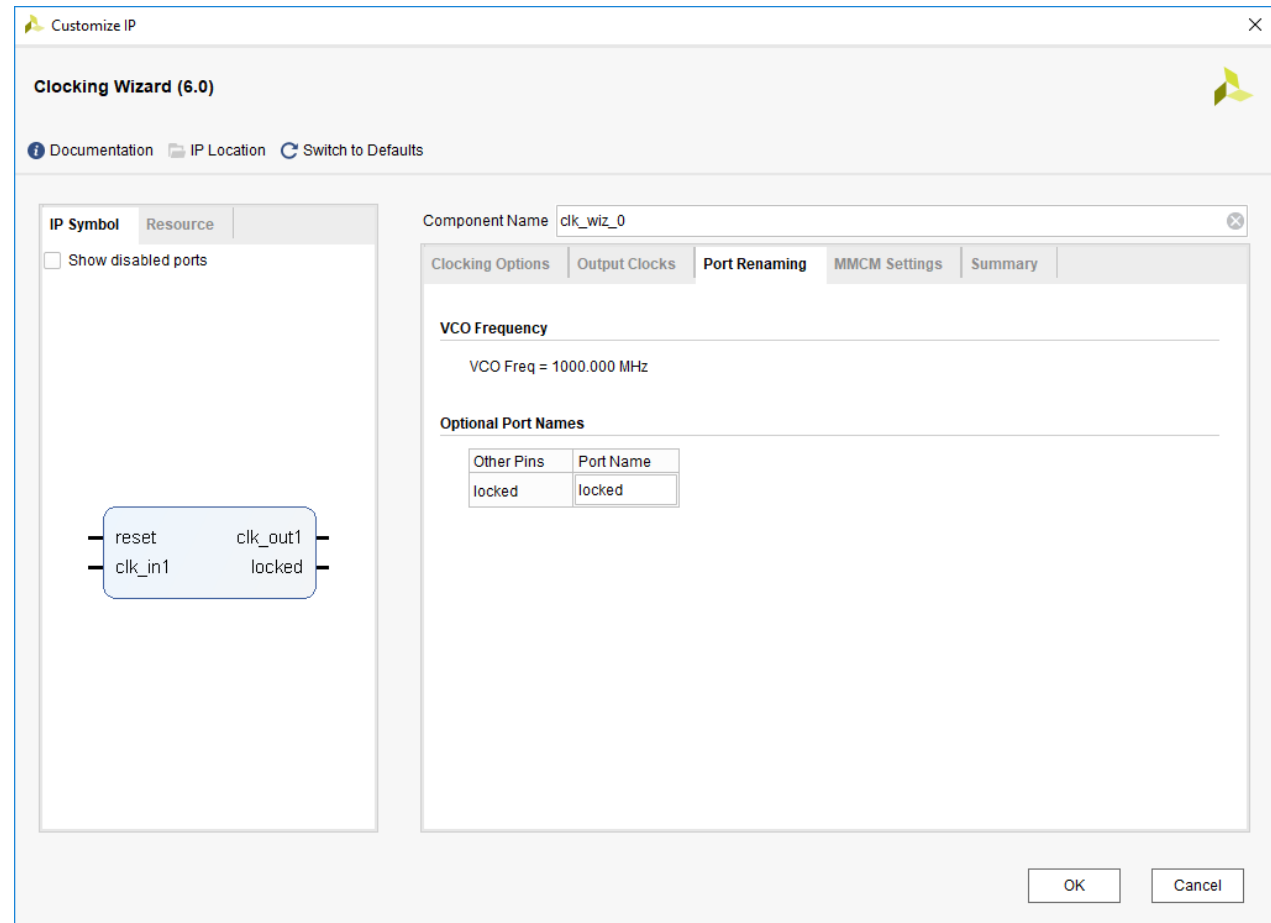
The Clocking Wizard: MMCM Settings

- ▶ Allows overriding of wizard settings
- ▶ Sets the phase, period, jitter...



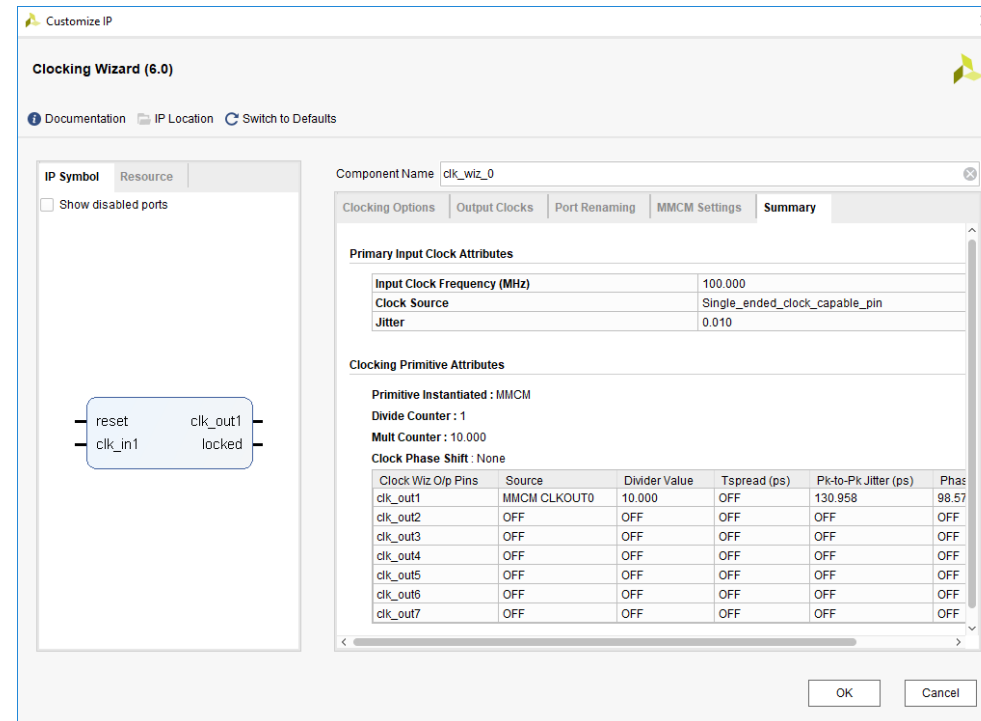
The Clocking Wizard: Port Renaming

- ▶ Change input/output port names
- ▶ Change optional port names



The Clocking Wizard: Summary

- ▶ Shows the input, output frequencies
- ▶ Other attributes depending on the selections made

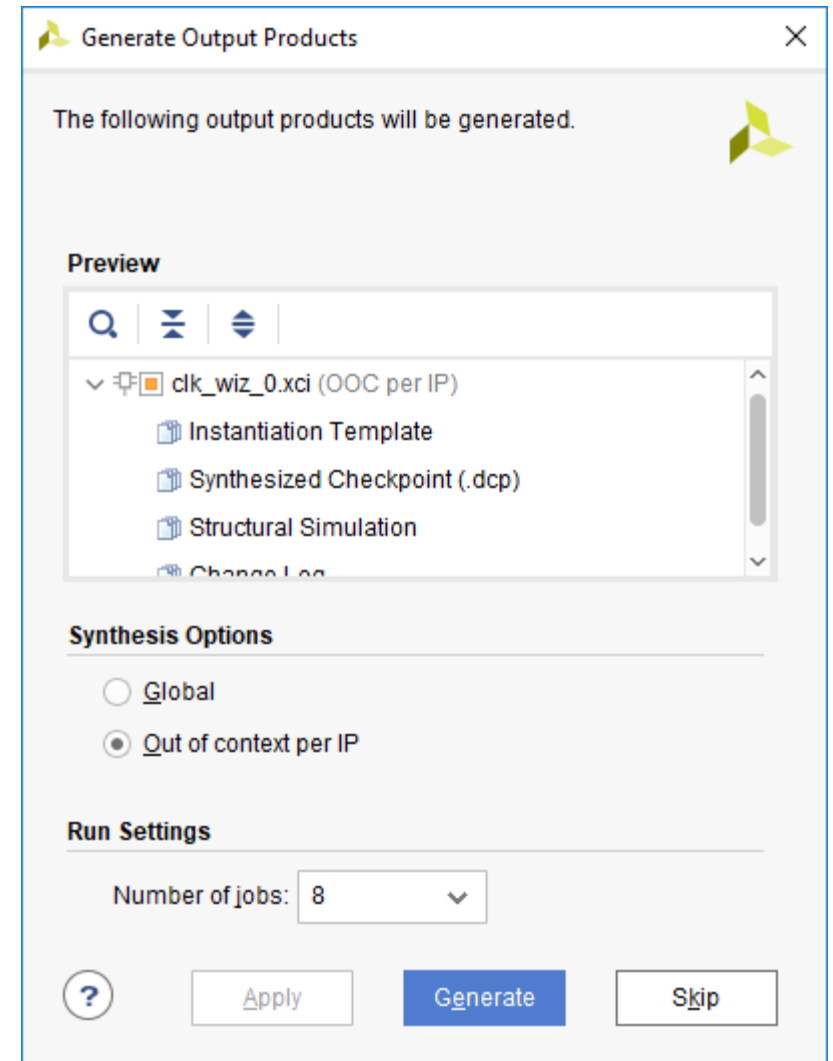


- ▶ The Resource tab on the left provides summary of type and number of resources used

IP Symbol	Resource
	1 MMCM
	1 IBUFG
	2 BUFG

Generating Output Products

- ▶ Generate Instantiation Template
- ▶ Synthesis model
- ▶ Simulation model
- ▶ Implementation related files
- ▶ Examples on how to use the product
- ▶ Optionally, synthesized design checkpoint so it can be used in the implementation without re-synthesizing in the project



Summary

Summary

- ▶ Vivado is an IP Centric design environment, allowing multiple ways to add/manage IP
 - Automatic RTL generation
 - Rapid assembly, packaging, and reuse of IP subsystems
 - Processor based system design support
- ▶ Vivado IP Integrator provides unique time to market advantages when designing with complex IP
- ▶ The IP Packagers provides flexibility of IP reuse and repackaging
- ▶ The IP Catalog provides access to extensive IP resources
 - Simple IP to highly complex IP
 - Grouped according to functionality
- ▶ The Clocking Wizard enables the configuration of complex clocking resources



Thank You

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