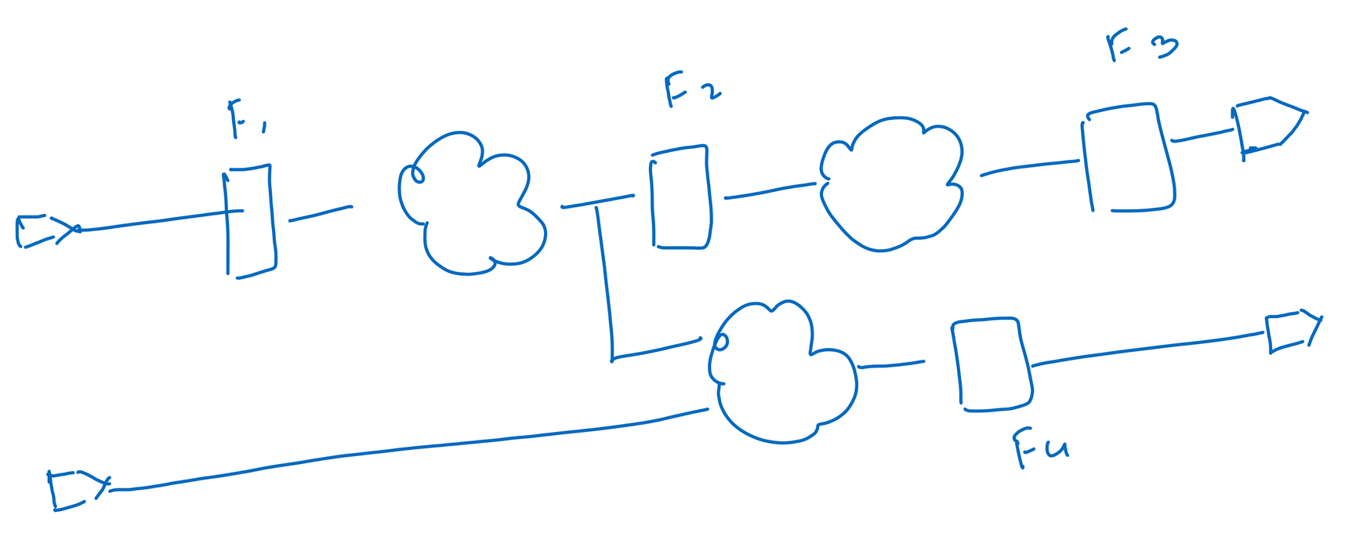
Static Timing Analysis



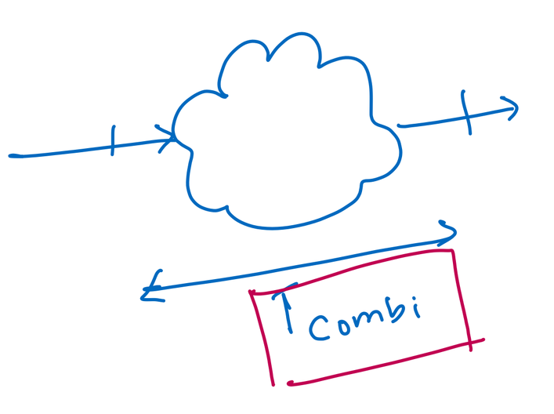
Analyse Timing Path:

A Section between a pair of flip flops

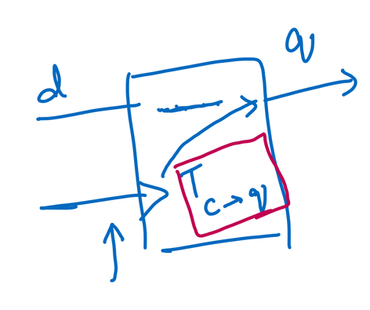
Data Launch — Data Capture } w.r.t Clock

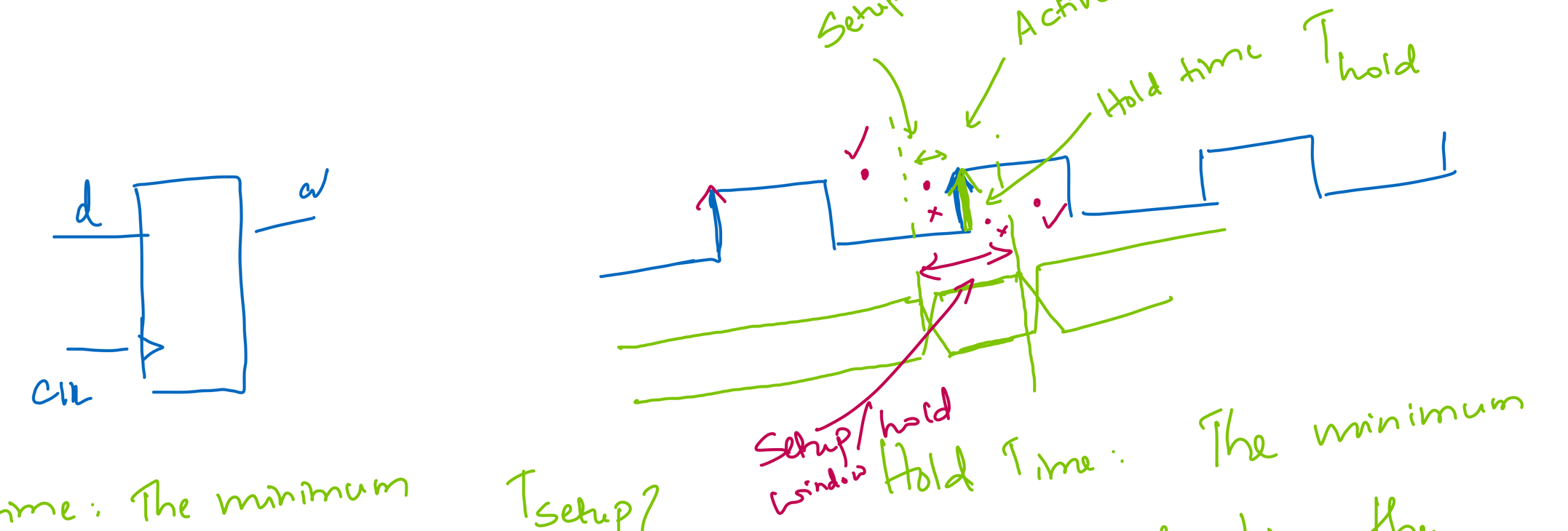
Ex: $F_1 - F_2$, $F_2 - F_3$, $F_1 - F_4$

Combinational Logic



Timing Parameters in a Flip Flop:





Setup time: The minimum time before which the data is required before arrival active edge of clock
⇒ Required Time (data)

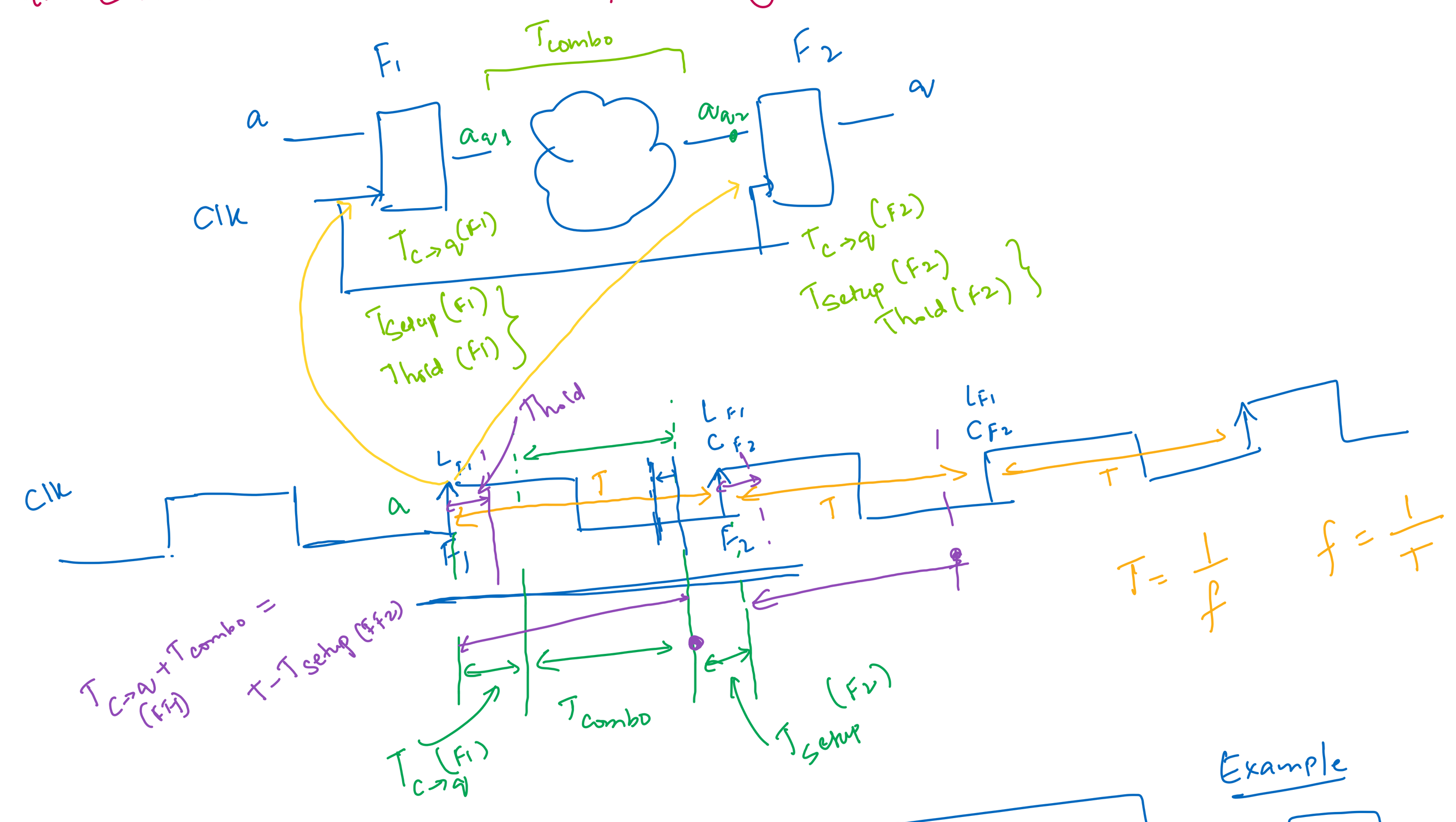
T_{setup}, T_{req} }

Hold Time: The minimum amount of time the data should be stable after the arrival of clock edge

Ultimately, the data arrival should satisfy T_{setup} & T_{hold}

Data should not change in Setup & Hold window

How to calculate the maximum frequency @ which a timing path can work

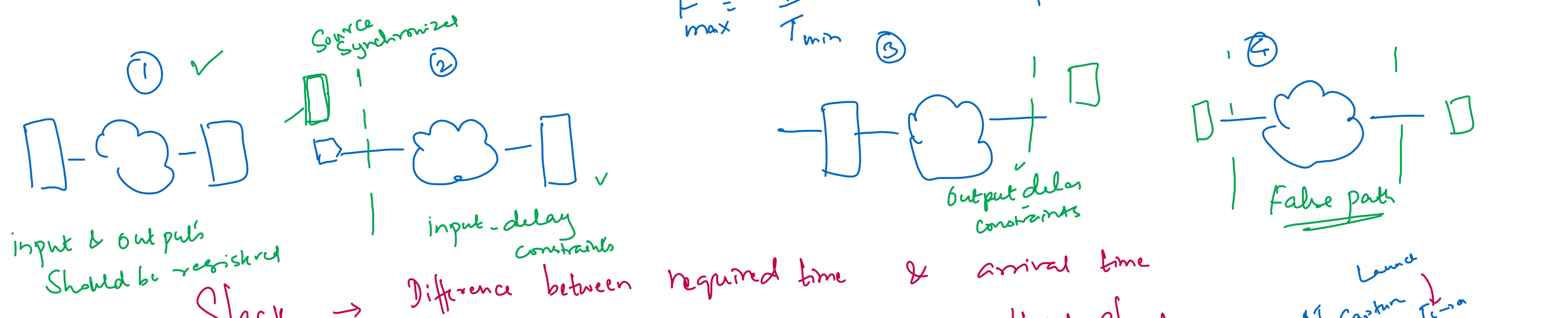


$T = \frac{1}{f}$ $f = \frac{1}{T}$

$$T_{min} = T_{c\to q}(F_1) + T_{combo} + T_{setup}(F_2)$$

$F_{max} = \frac{1}{T_{min}}$ the max frequency

Example → ~~10 ns~~ (boxed) 100 MHz; × 8 ns 125 MHz; ✓ 20 ns 50 MHz

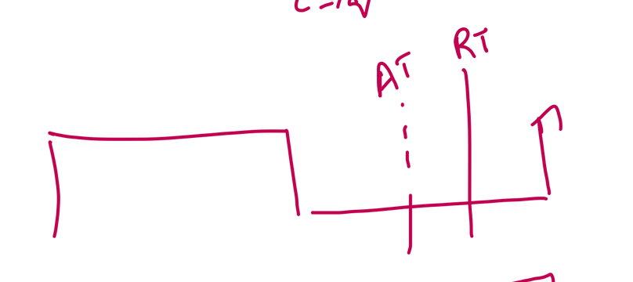


Slack → Difference between required time & arrival time

Setup Slack

RT = T_{setup} (boxed) T − T_{setup}

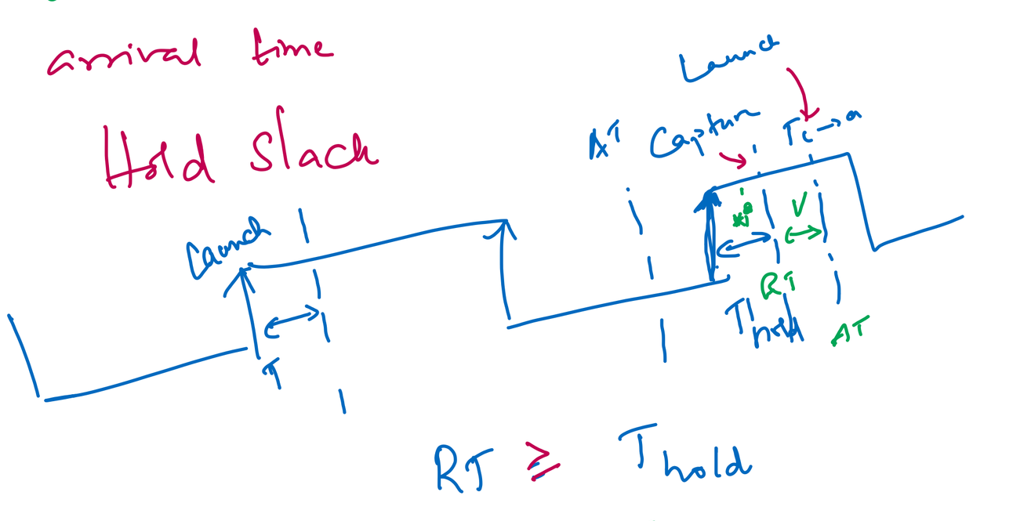
AT = $T_{c\to q} + T_{combo}$



Setup Slack = RT − AT (boxed), ideally it should be positive

If the value is negative then is Setup violation

Hold Slack



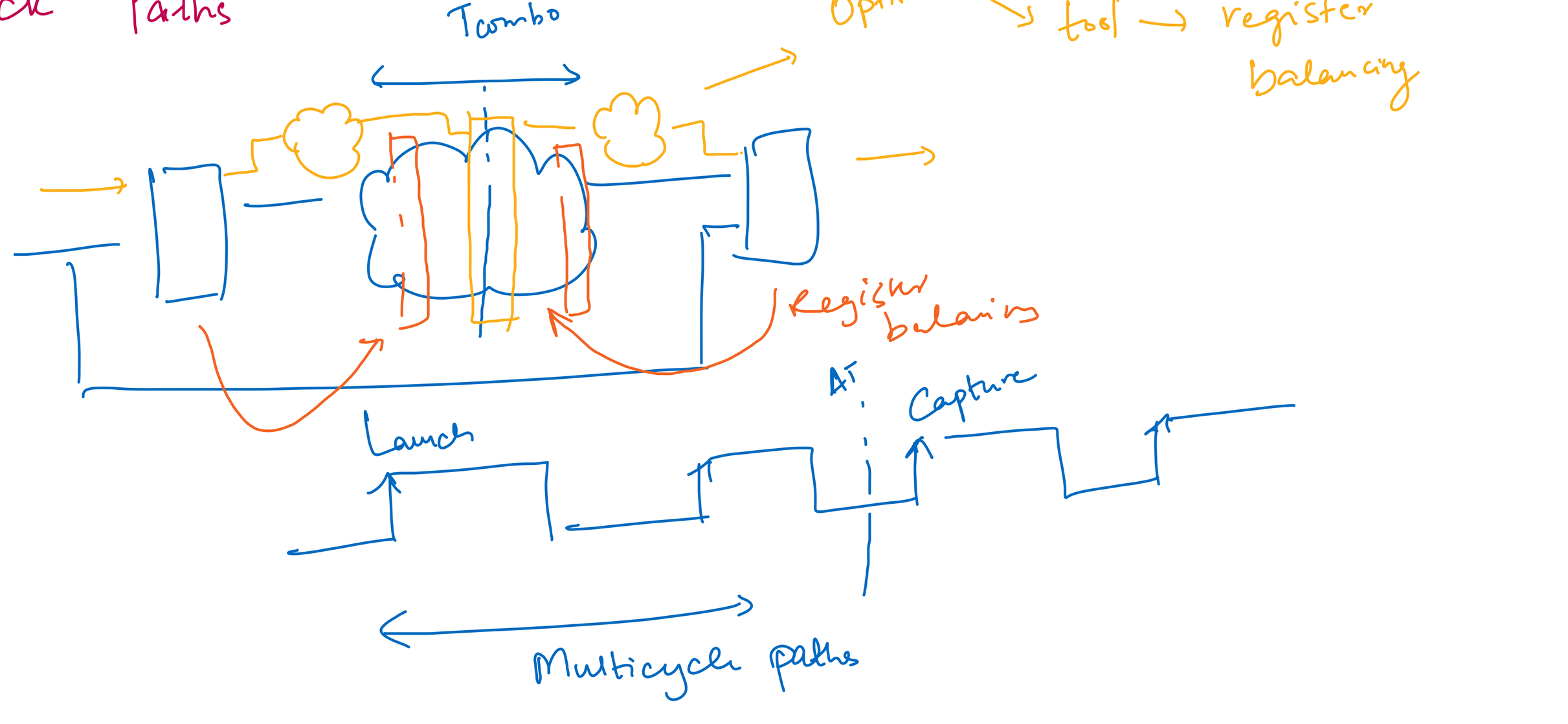
RT ≥ T_{hold}

AT < T_{hold}

AT − RT (boxed), ideally should be positive

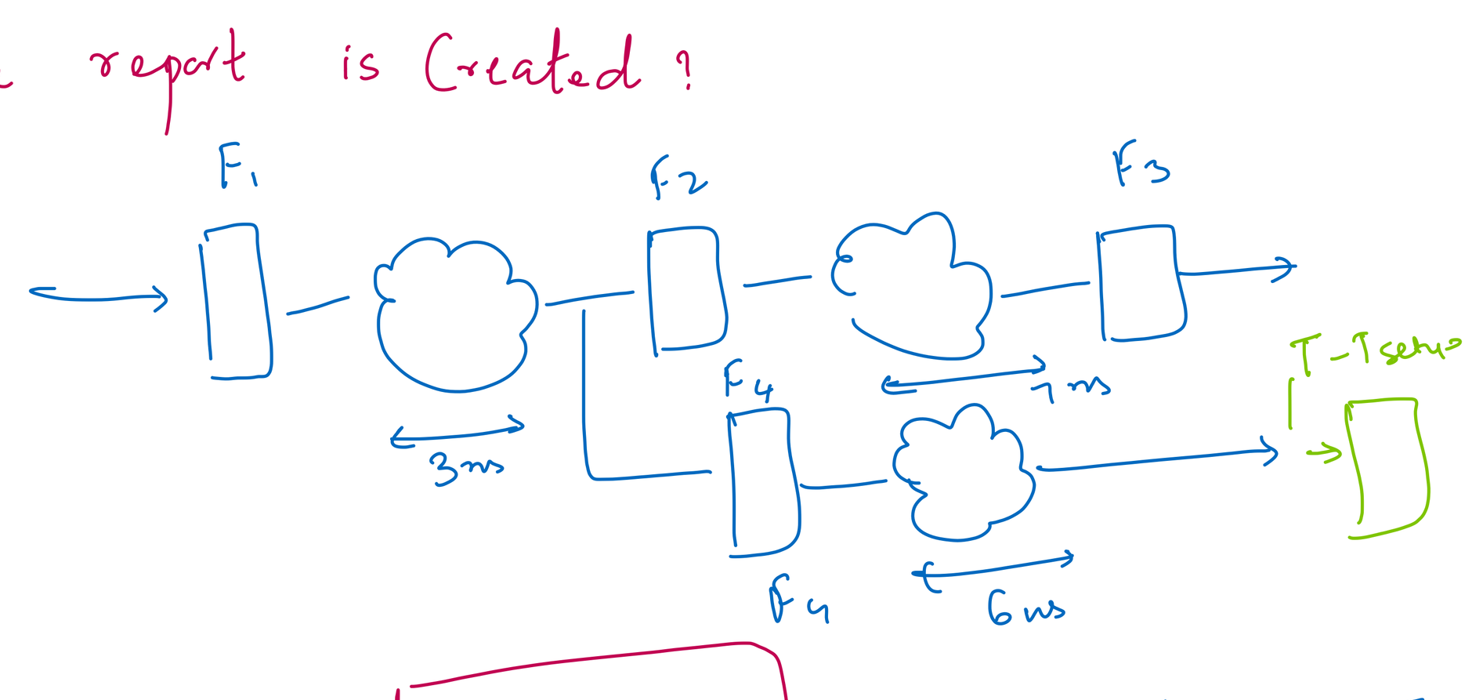
If negative the Hold Violation happens

Multi Clock Paths



Options → manually +1 FF layer extra; tool → register balancing

How the report is Created?



Flip Flops
$T_{c\to q}$ 1 ns
T_{setup} 0.5 ns
T_{hold} 0.2 ns

$F_1 - F_2$ ⇒ $T_{min(1-2)}$ = 1 + 3ns + 0.5ns = 4.5 ns

$F_2 - F_3$ ⇒ $T_{min(2-3)}$ = 1 + 7ns + 0.5ns = 8.5 ns

$F_1 - F_4$ ⇒ $T_{min(1-4)}$ = 1 + 3ns + 0.5 ns = 4.5 ns

F_4 − ⇒ T_{min} − T_{setup} = 1 + 6ns = 7ns + 0.5 = 7.6 ns

Which one has max delay

Critical path: A path having maximum delay } This determines max frequency for a circuit

F_{max} for whole circuit $= \frac{1}{T_{min(2-3)}} = \frac{1}{8.5} = 0.1176 \times 10^9$ = 117.6 MHz

Class Exercise: Find the Critical path & Calculate max frequency

FF
$T_{c\to q}$ = 0.3 ns
T_{setup} = 0.6 ns
T_{hold} = 0.1 ns