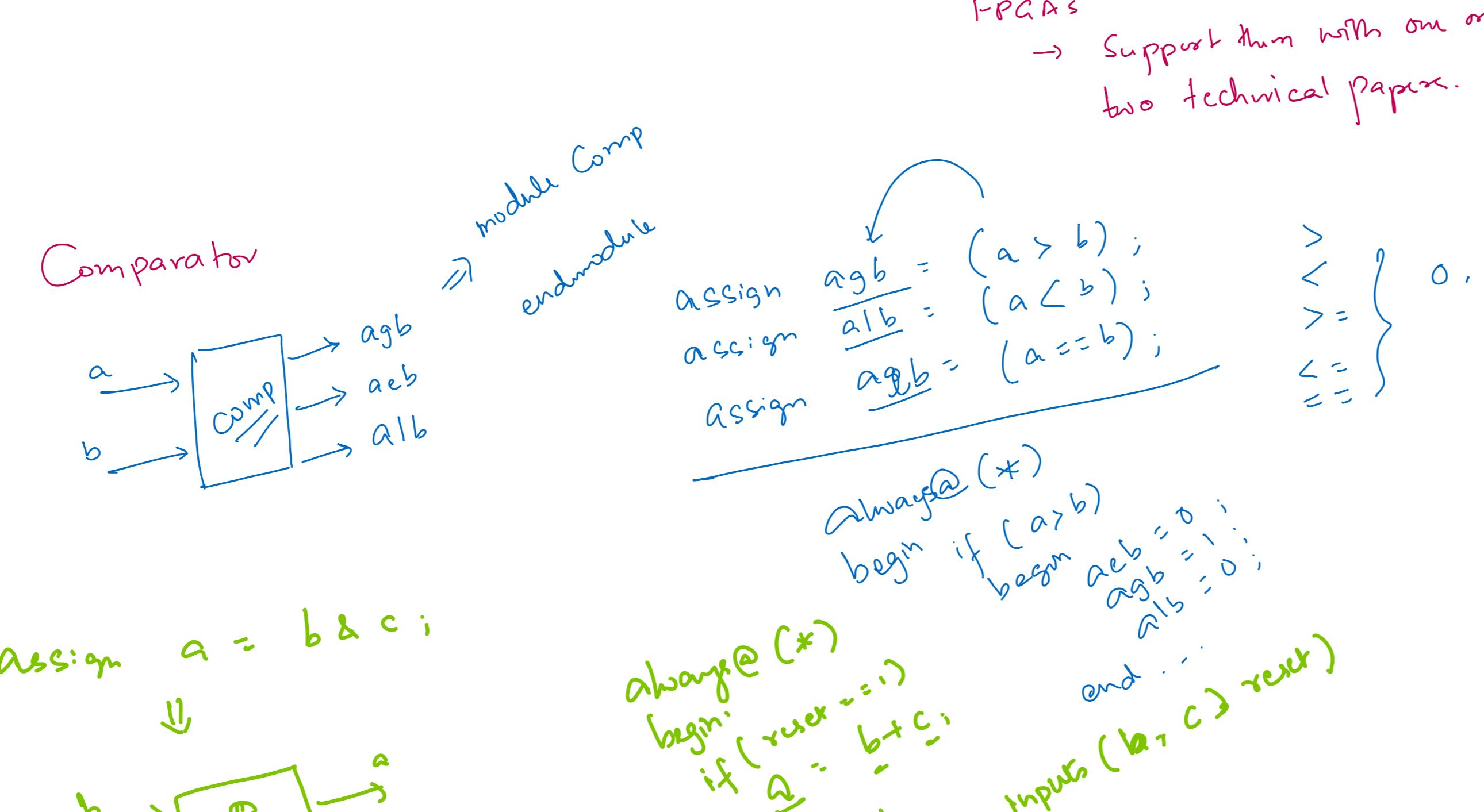


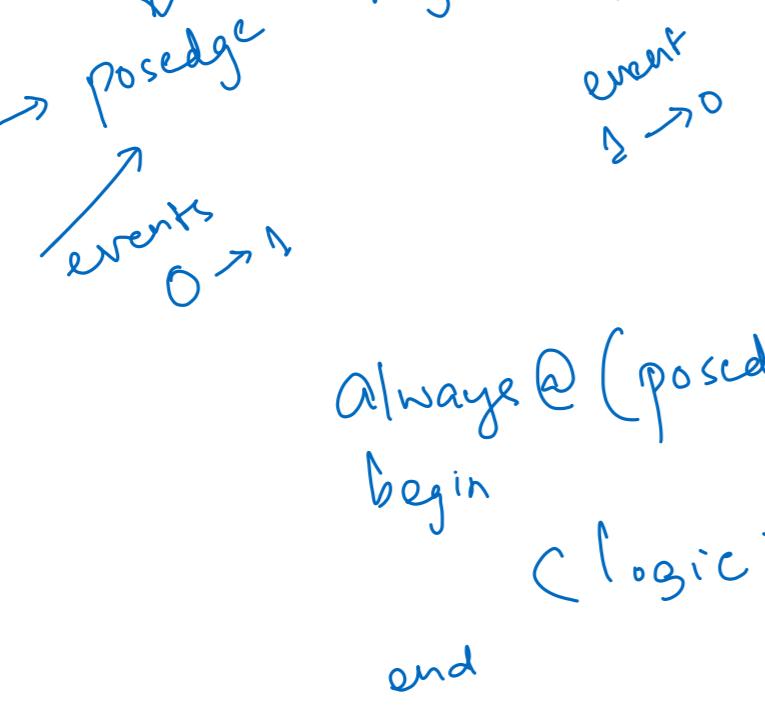
1. Verilog HDL is used to capture the behaviour of the circuits



Assignment: 25-May-2023

1. Read Sections on PLA, PLD from the Digital Logic Fundamentals Text Book.
2. List the applications (10) of FPGAs
→ Support them with one or two technical papers.

2. Comparator

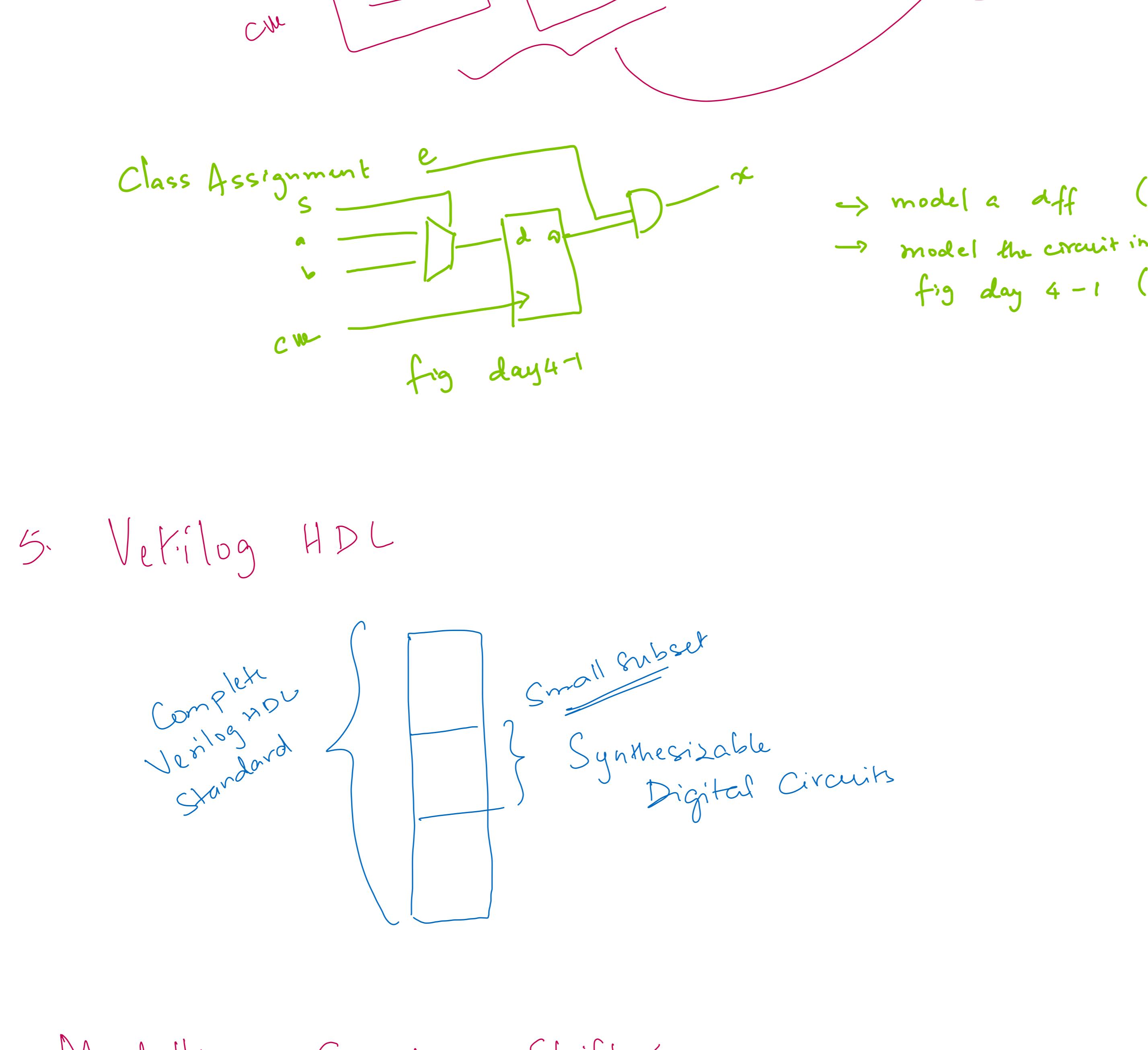


assign $a = b \& c$
assign $ab = (a > b)$,
assign $ab = (a < b)$,
assign $ab = (a = b)$,
 $\begin{cases} > \\ < \\ = \end{cases}$

always @ (*)
begin
if ($a > b$)
begin
ab = 1;
end
else if ($a < b$)
begin
ab = 0;
end
else
begin
ab = 1;
end
end

inputs (a, b, c) read

3. Sequential Circuits



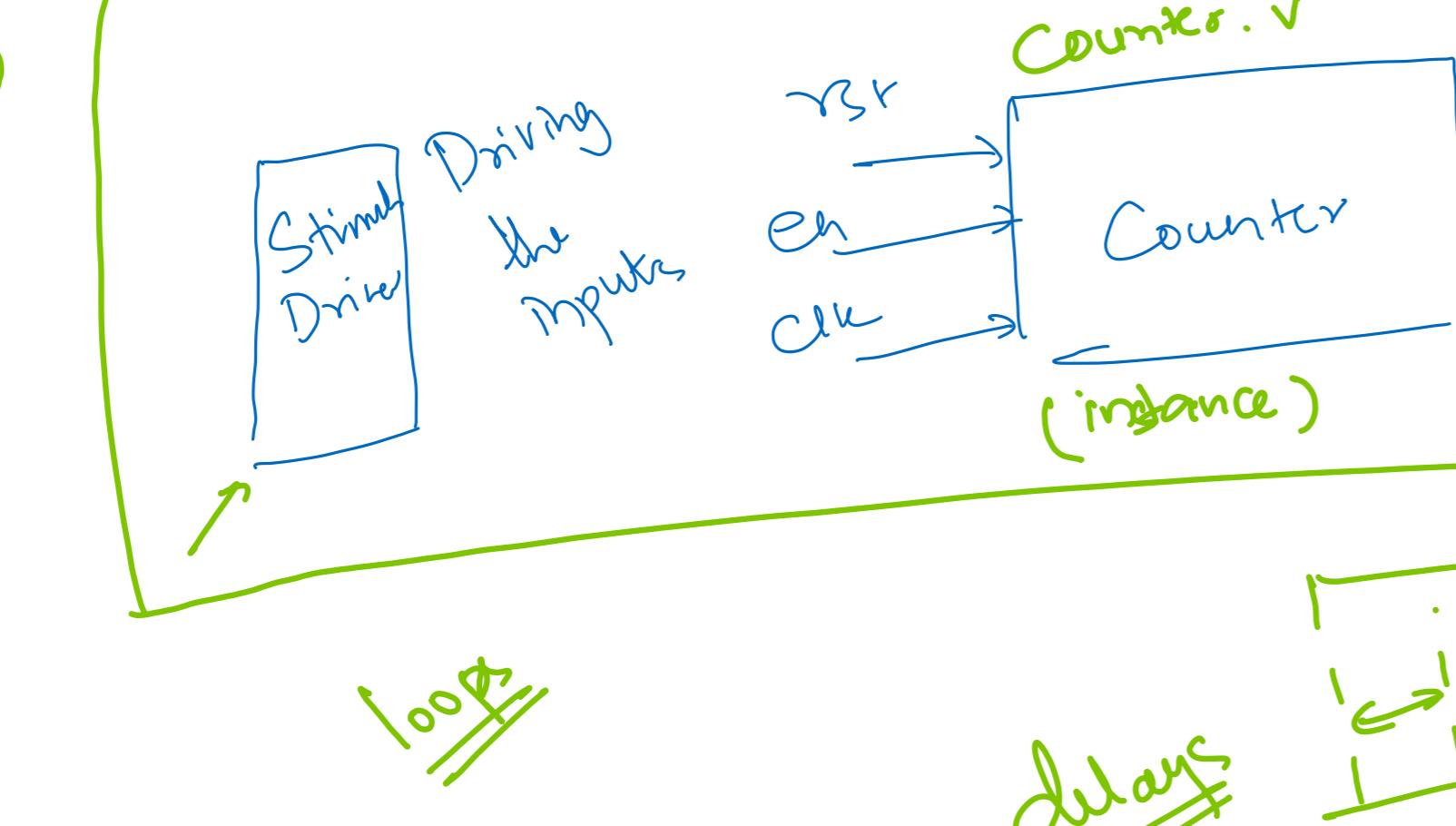
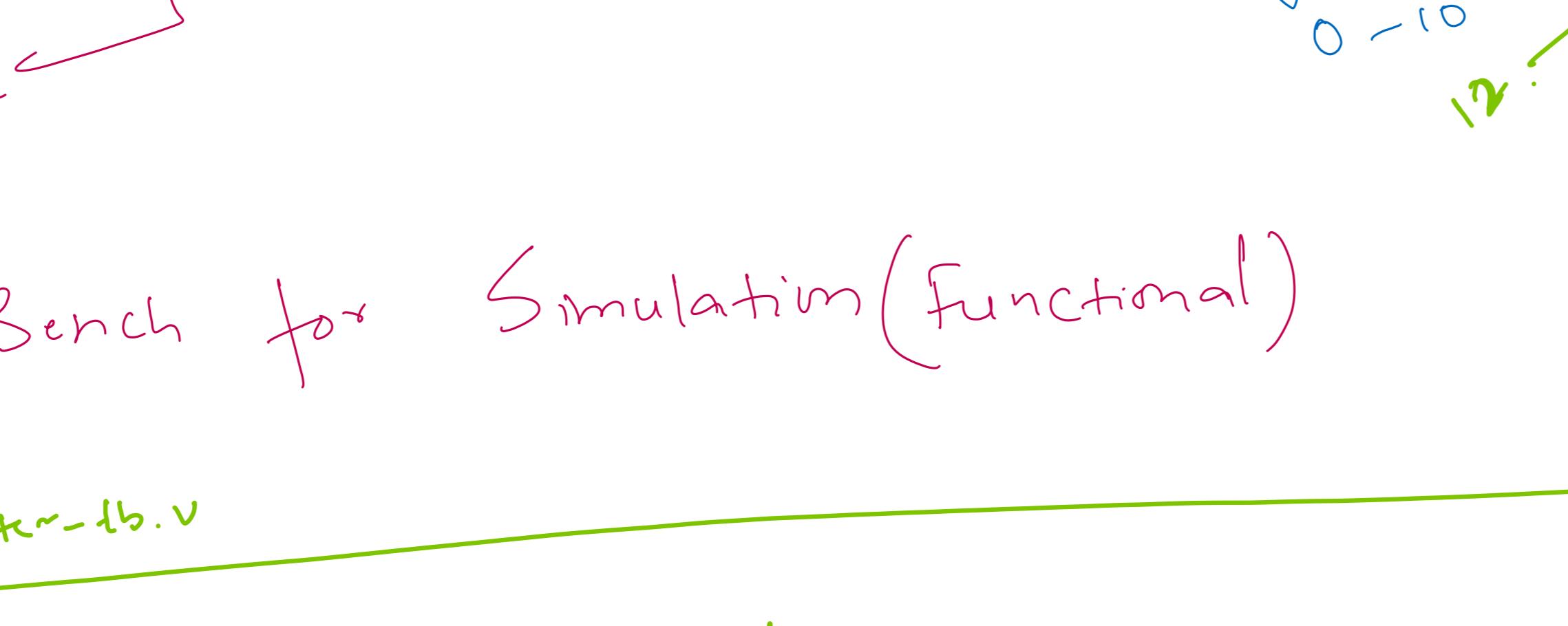
Two Conditions → Functionally Correct

Synthesizable

↳ Only synthesizable circuit

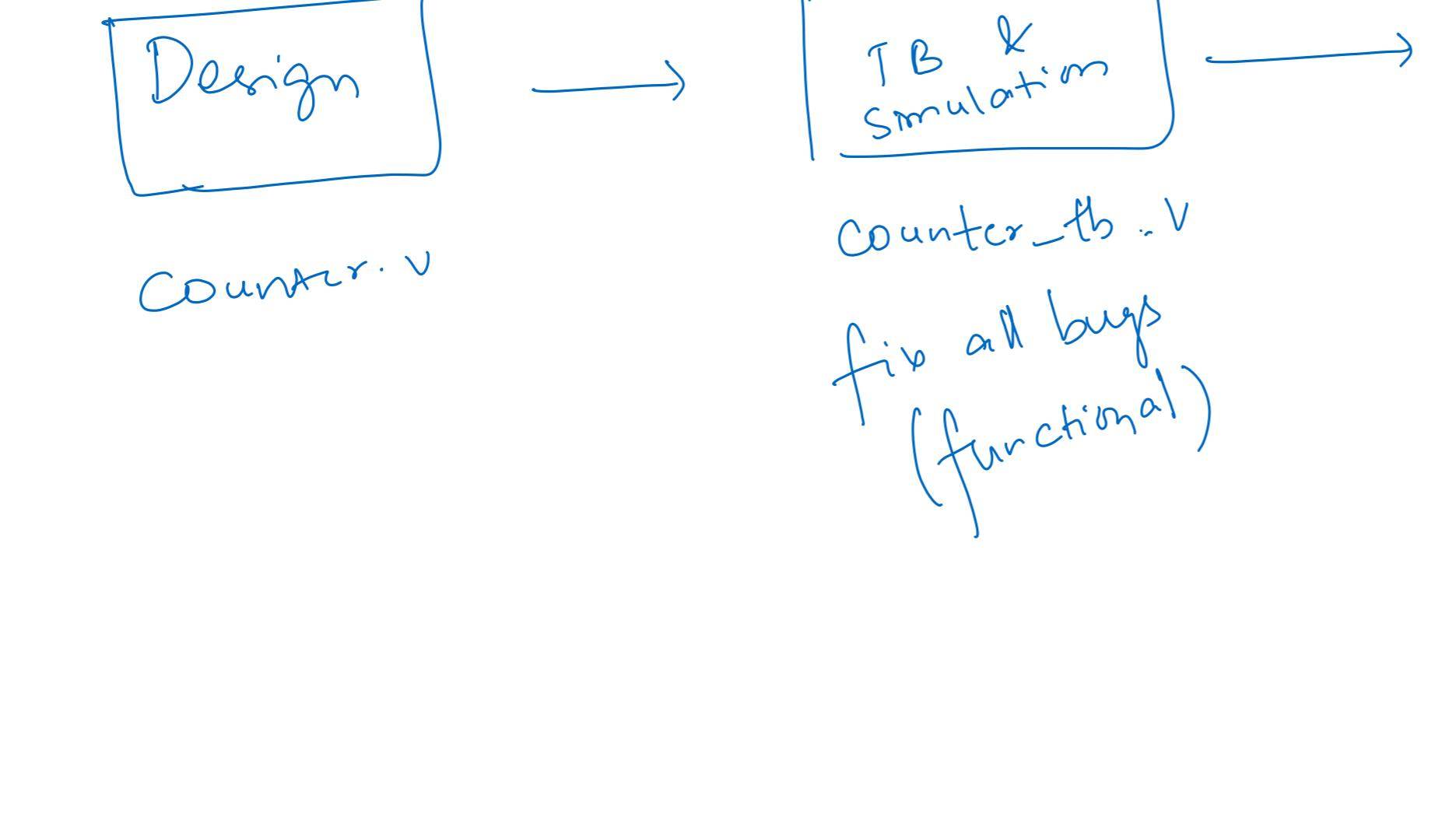
Can be taken to FPGAs

4. Micro Architecture Example

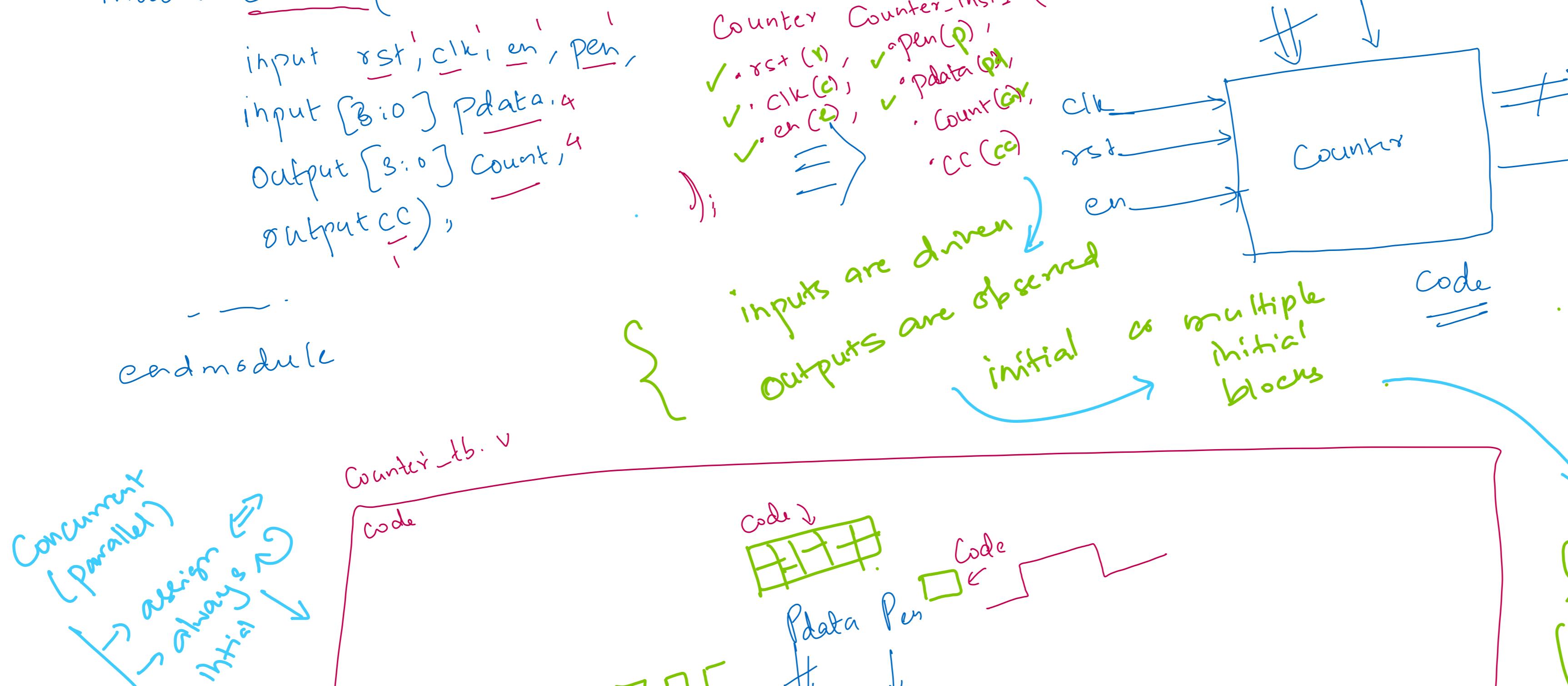


→ model a diff (10)
→ model the circuit in fig day 4-1 (20 min)

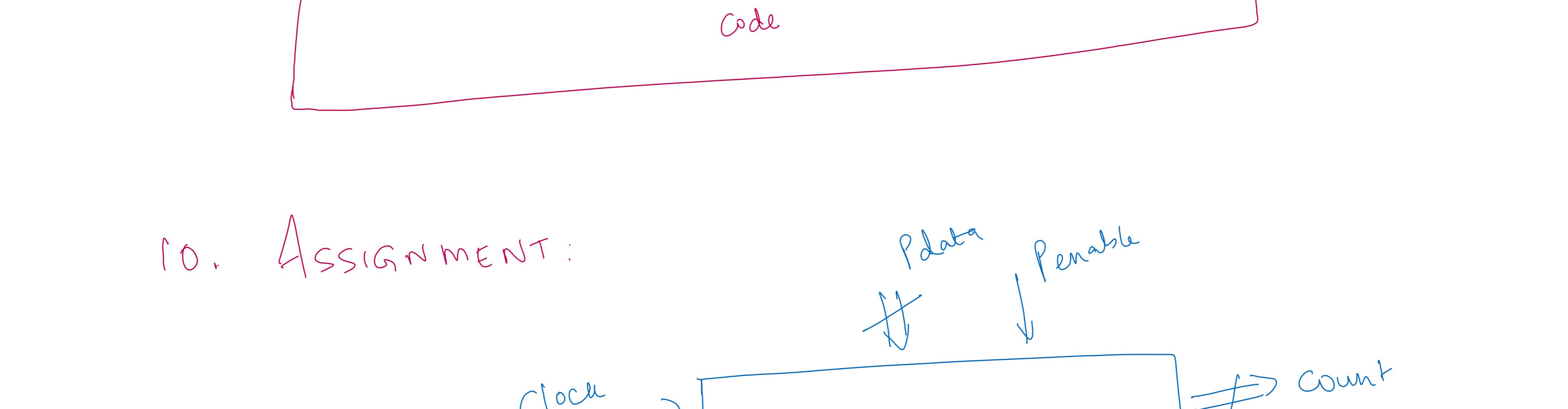
5. Verilog HDL



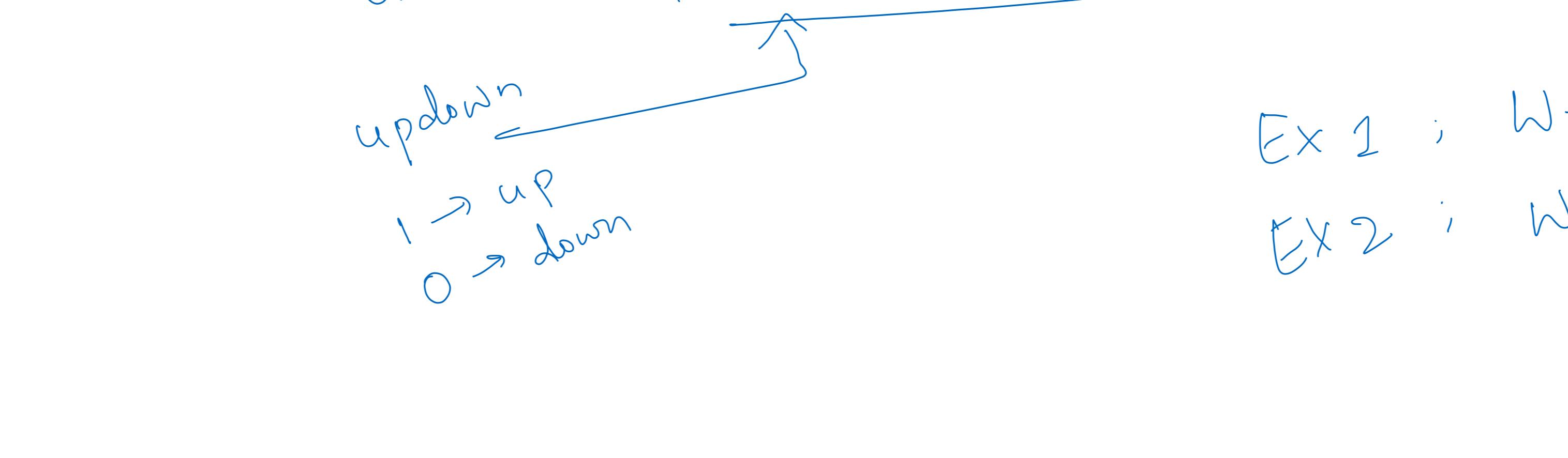
6. Modelling Counter, Shifter



7. Test Bench for Simulation (Functional)



8. Flow



100% + Validated

9. Waiting a test bench for Counter creation (copy)



10. ASSIGNMENT:



Ex 1 : Write Verilog design

Ex 2 : Write Verilog TB

for this and write all test cases to test the features