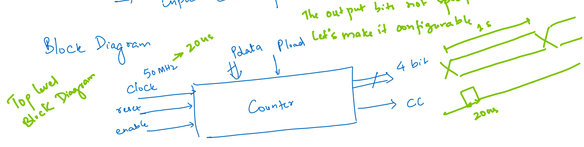
1. Design Example

Requirement:

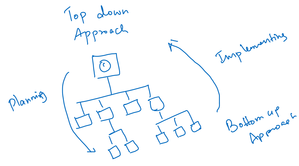
→ Counter that increments every 1 second

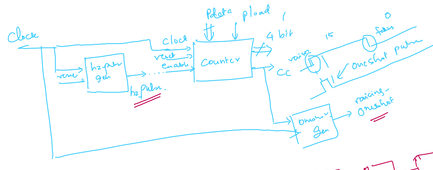
→ Input clock frequency is 50 MHz

Block Diagram



Micro Architecture

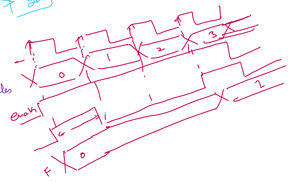




Corelogic for hz pulse-gen:

50 MHz = 50 000 000 clock cycles per second

A counter that can count from 0 to 50000000 and produce a pulse when 50 000 000 is reached. Mod 50000000 counter

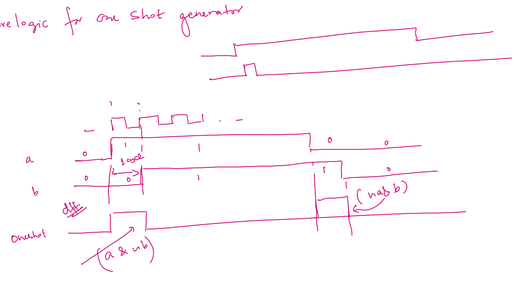


Size of the counter:

4 → 15
5 → 31
6 → 63
7 → 127 } 128
8 → 255
→ 50000000

$2^n \geq 50000000$

Corelogic for one shot generator



Verilog Coding

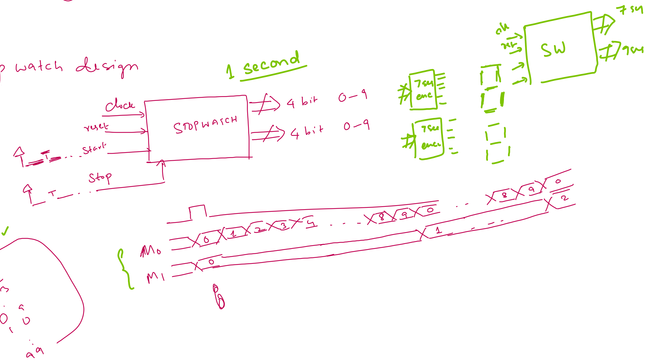
① Top level with pin details

② hz_pulse_gen coding & testing

③ oneshot_gen coding & testing

④ integrate in top level & test the top level

2. Stop watch design



3. Shifter Design