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# 7-Series Architecture Overview

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# Objectives

- **After completing this module, you will be able to:**
  - Describe the basic slice resources available in 7-Series FPGAs
  - List memory hierarchy and various memory resources available
  - Identify the basic I/O resources available in 7-Series FPGAs
  - List some of the dedicated hardware features of 7-Series FPGAs
  - Identify latest members of Virtex-7 device family
  - Identify the MMCM, PLL, and clock routing resources included with these families
  - Describe the additional dedicated hardware for all the 7-series family members
  - Understand the Zynq-7000 SoC architecture


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# Outline

- *Introduction to 7-Series FPGA*
- Logic Resources
- I/O Resources
- Memory and DSP48 Resources
- XADC
- Clocking Resources
- Zynq SoC
- Summary


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# Introduction

- **All Xilinx FPGAs contain the same basic resources**
  - Logic Resources
    - Slices (grouped into configurable logic blocks (CLB))
      - Containing combinatorial logic and register resources
    - Memory
    - Multipliers
  - Interconnect Resources
    - Programmable interconnect
    - IOBs
      - Interfaces between the FPGA and the outside world
  - Other resources
    - Global clock buffers
    - Boundary scan logic
- **Through various generations, Xilinx added new architectural resources to target various markets and application areas**



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# 7-Series FPGA Families

| Max. Capability | Spartan-7 | Artix-7 | Kintex-7 | Virtex-7 |
|---|---|---|---|---|
| Logic Cells | 102K | 215K | 478K | 1,955K |
| Block RAM(1) | 4.2 Mb | 13 Mb | 34 Mb | 68 Mb |
| DSP Slices | 160 | 740 | 1,920 | 3,600 |
| DSP Performance(2) | 176 GMAC/s | 929 GMAC/s | 2,845 GMAC/s | 5,335 GMAC/s |
| MicroBlaze CPU(3) | 260 DMIPs | 303 DMIPs | 438 DMIPs | 441 DMIPs |
| Transceivers | – | 16 | 32 | 96 |
| Transceiver Speed | – | 6.6 Gb/s | 12.5 Gb/s | 28.05 Gb/s |
| Serial Bandwidth | – | 211 Gb/s | 800 Gb/s | 2,784 Gb/s |
| PCIe Interface | – | x4 Gen2 | x8 Gen2 | x8 Gen3 |
| Memory Interface | 800 Mb/s | 1,066 Mb/s | 1,866 Mb/s | 1,866 Mb/s |
| I/O Pins | 400 | 500 | 500 | 1,200 |
| I/O Voltage | 1.2V–3.3V | 1.2V–3.3V | 1.2V–3.3V | 1.2V–3.3V |
| Package Options | Low-Cost, Wire-Bond | Low-Cost, Wire-Bond, Bare-Die Flip-Chip | Bare-Die Flip-Chip and High-Performance Flip-Chip | Highest Performance Flip-Chip |



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# 7-Series SoC Families

| | | Cost-Optimized Devices | | | | | | Mid-Range Devices | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Device Name | Z-7007S | Z-7012S | Z-7014S | Z-7010 | Z-7015 | Z-7020 | Z-7030 | Z-7035 | Z-7045 | Z-7100 |
| | Part Number | XC7Z007S | XC7Z012S | XC7Z014S | XC7Z010 | XC7Z015 | XC7Z020 | XC7Z030 | XC7Z035 | XC7Z045 | XC7Z100 |
| Processing System (PS) | Processor Core | Single-Core ARM® Cortex™-A9 MPCore™ Up to 766MHz | | | Dual-Core ARM Cortex-A9 MPCore Up to 866MHz | | | Dual-Core ARM Cortex-A9 MPCore Up to 1GHz[1] | | | |
| | Processor Extensions | NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor | | | | | | | | | |
| | L1 Cache | 32KB Instruction, 32KB Data per processor | | | | | | | | | |
| | L2 Cache | 512KB | | | | | | | | | |
| | On-Chip Memory | 256KB | | | | | | | | | |
| | External Memory Support[2] | DDR3, DDR3L, DDR2, LPDDR2 | | | | | | | | | |
| | External Static Memory Support[2] | 2x Quad-SPI, NAND, NOR | | | | | | | | | |
| | DMA Channels | 8 (4 dedicated to PL) | | | | | | | | | |
| | Peripherals | 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO | | | | | | | | | |
| | Peripherals w/ built-in DMA[2] | 2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO | | | | | | | | | |
| | Security[3] | RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot | | | | | | | | | |
| | Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only) | 2x AXI 32b Master, 2x AXI 32b Slave<br>4x AXI 64b/32b Memory<br>AXI 64b ACP<br>16 Interrupts | | | | | | | | | |
| Programmable Logic (PL) | 7 Series PL Equivalent | Artix®-7 | Artix-7 | Artix-7 | Artix-7 | Artix-7 | Artix-7 | Kintex®-7 | Kintex-7 | Kintex-7 | Kintex-7 |
| | Logic Cells | 23K | 55K | 65K | 28K | 74K | 85K | 125K | 275K | 350K | 444K |
| | Look-Up Tables (LUTs) | 14,400 | 34,400 | 40,600 | 17,600 | 46,200 | 53,200 | 78,600 | 171,900 | 218,600 | 277,400 |
| | Flip-Flops | 28,800 | 68,800 | 81,200 | 35,200 | 92,400 | 106,400 | 157,200 | 343,800 | 437,200 | 554,800 |
| | Total Block RAM (# 36Kb Blocks) | 1.8Mb (50) | 2.5Mb (72) | 3.8Mb (107) | 2.1Mb (60) | 3.3Mb (95) | 4.9Mb (140) | 9.3Mb (265) | 17.6Mb (500) | 19.2Mb (545) | 26.5Mb (755) |
| | DSP Slices | 66 | 120 | 170 | 80 | 160 | 220 | 400 | 900 | 900 | 2,020 |
| | PCI Express® | — | Gen2 x4 | — | — | Gen2 x4 | — | Gen2 x4 | Gen2 x8 | Gen2 x8 | Gen2 x8 |
| | Analog Mixed Signal (AMS) / XADC[2] | 2x 12 bit, MSPS ADCs with up to 17 Differential Inputs | | | | | | | | | |
| | Security[3] | AES & SHA 256b Decryption & Authentication for Secure Programmable Logic Config | | | | | | | | | |
| | Speed Grades: Commercial | -1 | | | -1 | | | -1 | | | -1 |
| | Speed Grades: Extended | -2 | | | -2,-3 | | | -2,-3 | | | -2 |
| | Speed Grades: Industrial | -1, -2 | | | -1, -2, -1L | | | -1, -2, -2L | | | -1, -2, -2L |



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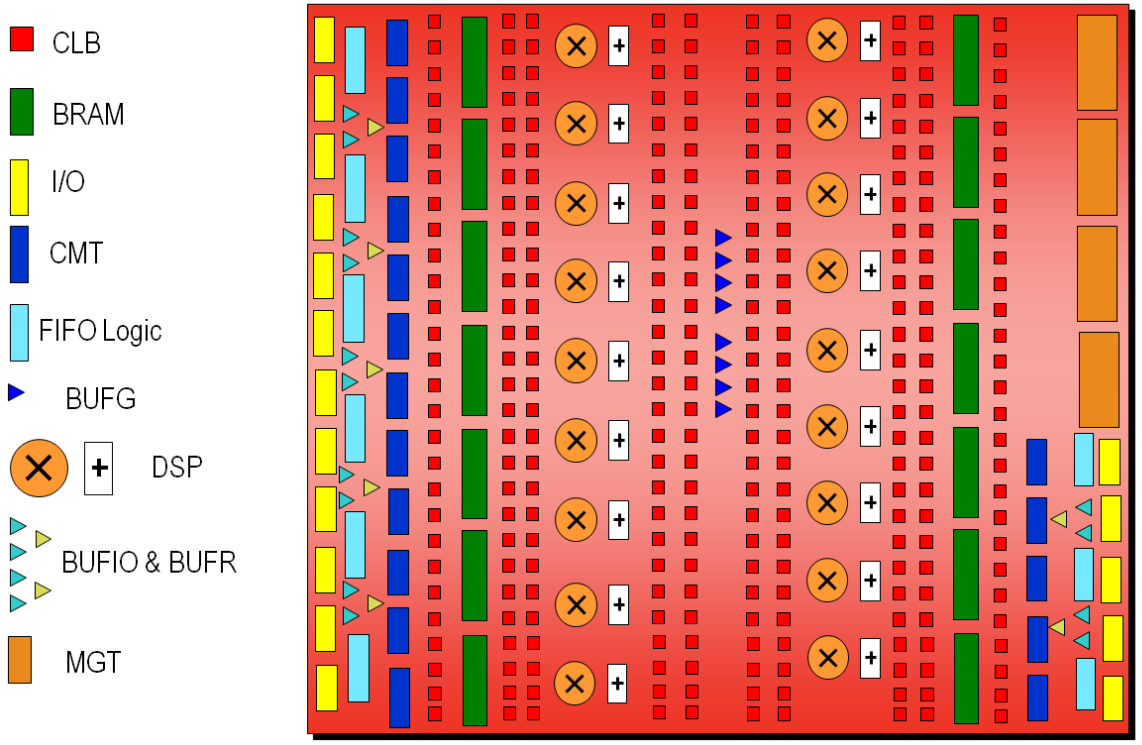
# 7-Series Architecture Alignment

- **Common elements enable easy IP reuse for quick design portability across all 7-series families**
  - Design scalability from low-cost to high-performance
  - Expanded eco-system support
  - Quickest time to market




Artix-7 Architecture Overview



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# Logic Resources



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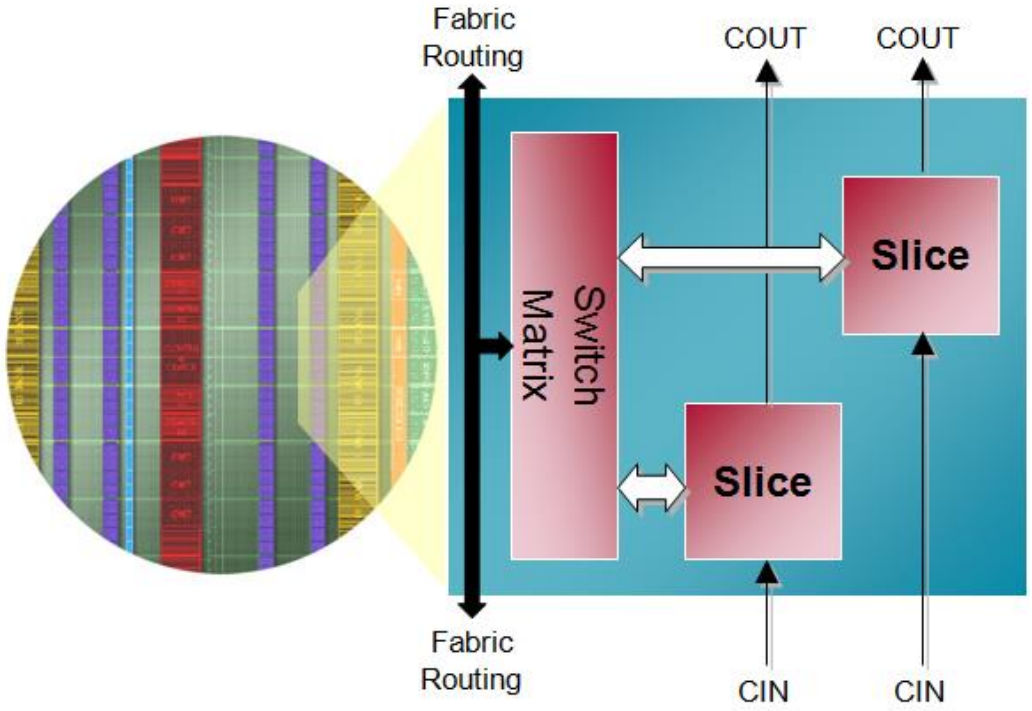
# Configurable Logic Block (CLB) in 7-Series FPGAs

- **Primary resource for design in Xilinx FPGAs**
  - Combinatorial functions
  - Flip-flops
- **CLB contains two slices**
- **Connected to switch matrix for routing to othe**
  - Carry chain runs vertically in a column from one slice to the one above



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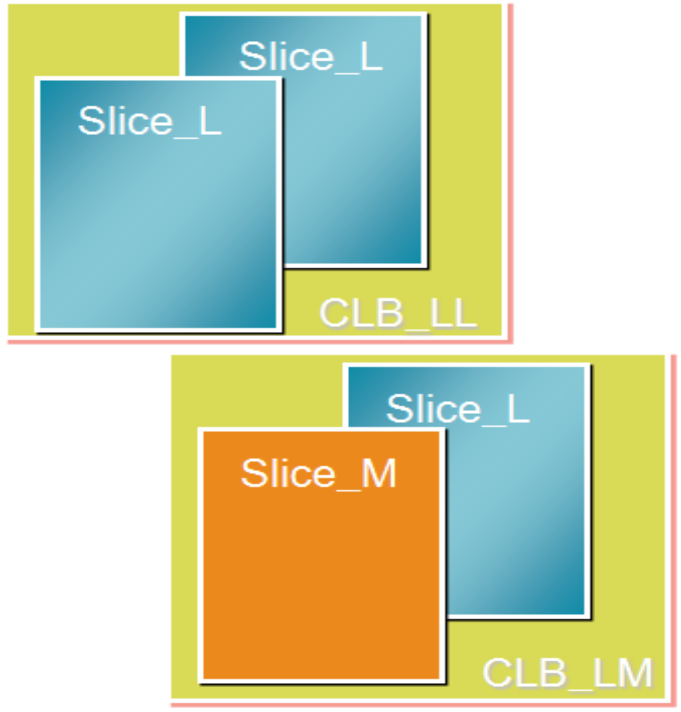
# Two Types of CLB Slices

- **Two types of CLB slices**
  - SLICEM: Full slice
    - LUT can be used for logic and memory/SRL
    - Has wide multiplexers and carry chain
  - SLICEL: Logic and arithmetic only
    - LUT can only be used for logic (not memory)
    - Has wide multiplexers and carry chain



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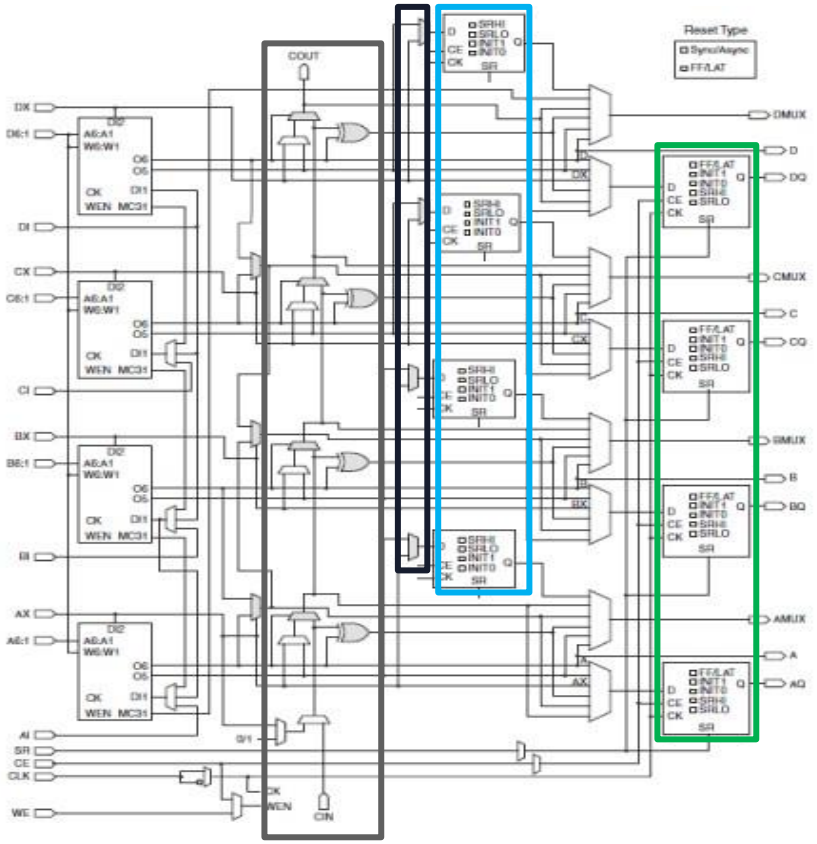
# Slice Resource

- **Four six-input Look-Up Tables (LUT)**
- **Multiplexers**
- **Carry chains**
- **SRL**
  - Cascade path is not shown
- **Four flip-flops/latches**
  - Four additional flip-flops
- **The implementation tool will pack multiple slices ure followed**



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# 6-Input LUT with Dual Output

- **LUTs can be two 5-input LUTs with common input**
  - Minimal speed impact to a 6-input LUT
  - One or two outputs
- **Any combinatorial function of six variables or two functions of five variables**


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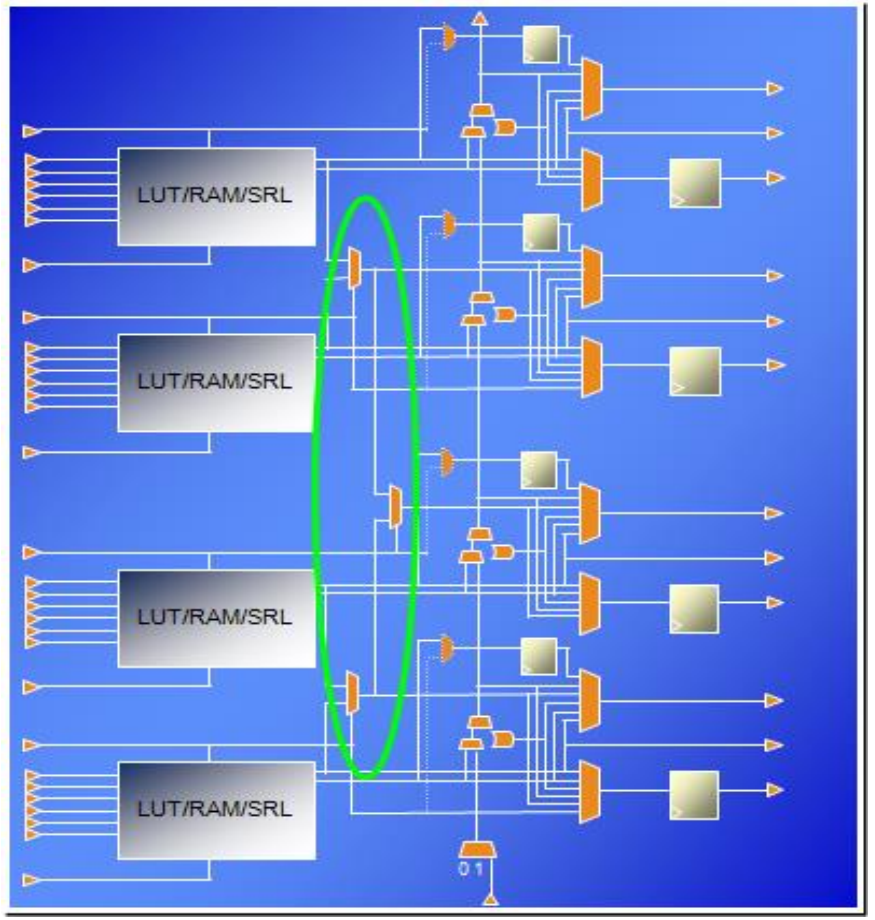
# Wide Multiplexers

- **Each F7MUX combines the outputs of two LUTs together**
  - Can implement an arbitrary 7-input function
  - Can implement an 8-1 multiplexer
- **The F8MUX combines the outputs of the two F7MUXes**
  - Can implement an arbitrary 8-input function
  - Can implement a 16-1 multiplexer
- **MUX is controlled by the BX/CX/DX slice input**
- **MUX output can drive out combinatorially or to the flip-flop/latch**



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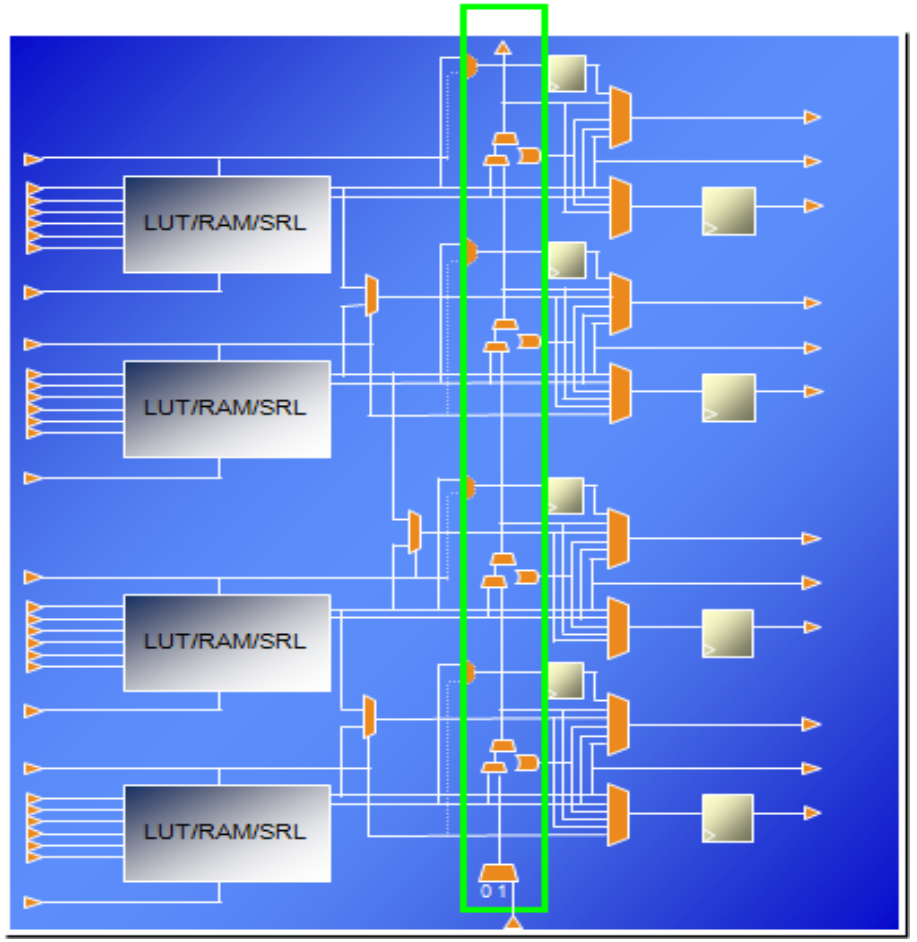
# Carry Chain

- **Carry chain can implement fast arithmetic addition and subtraction**
  - Carry out is propagated vertically through the four LUTs in a slice
  - The carry chain propagates from one slice to the slice in the same column in the CLB above
- **Carry look-ahead**
  - Combinatorial carry look-ahead over the four LUTs in a slice
  - Implements faster carry cascading from slice to slice



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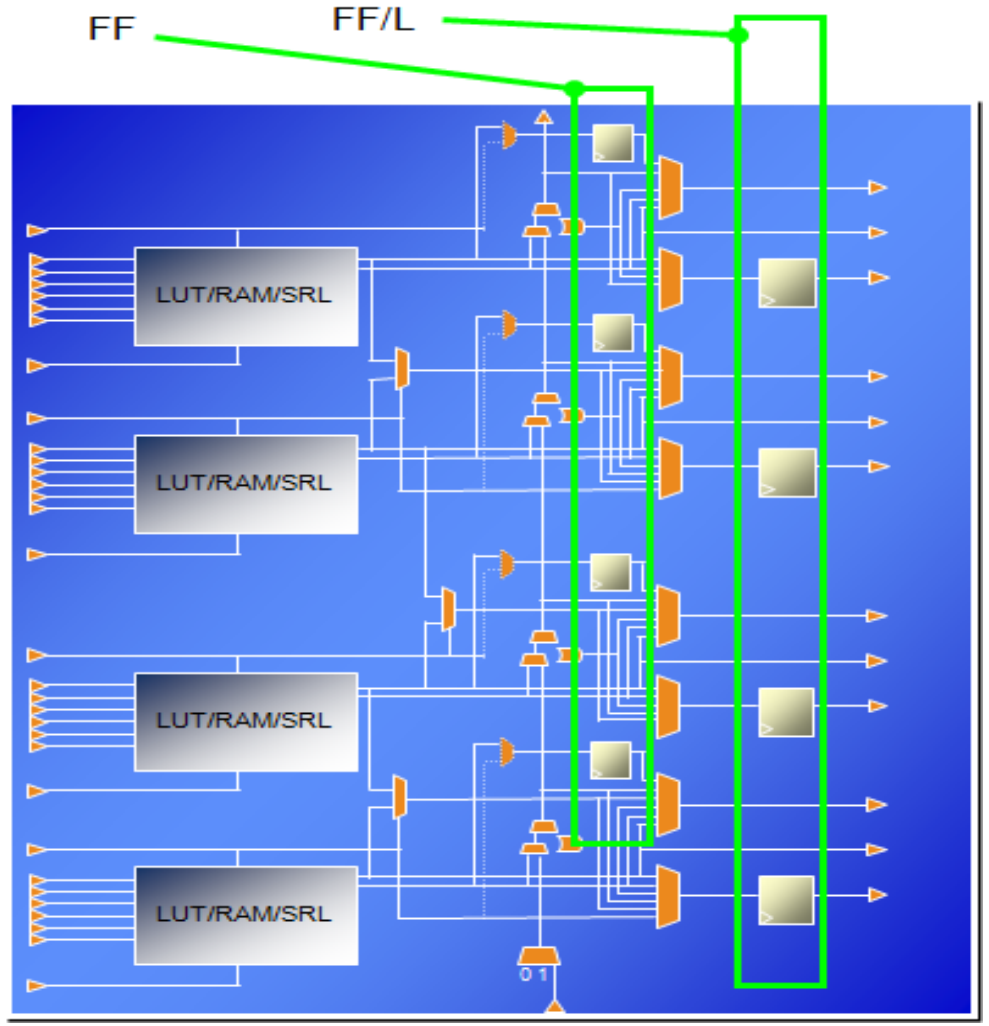
# Slice Flip-Flops and Flip-Flop/Latches

- **Each slice has four flip-flop/latches (FF/L)**
  - Can be configured as either flip-flops or latches
  - The D input can come from the O6 LUT output, the carry chain, the wide multiplexer, or the AX/BX/CX/DX slice input
- **Each slice also has four flip-flops (FF)**
  - D input can come from O5 output or the AX/BX/CX/DX input
    - These don't have access to the carry chain, wide multiplexers, or the slice inputs
- **If any of the FF/L are configured as latches, the four FFs are not available**



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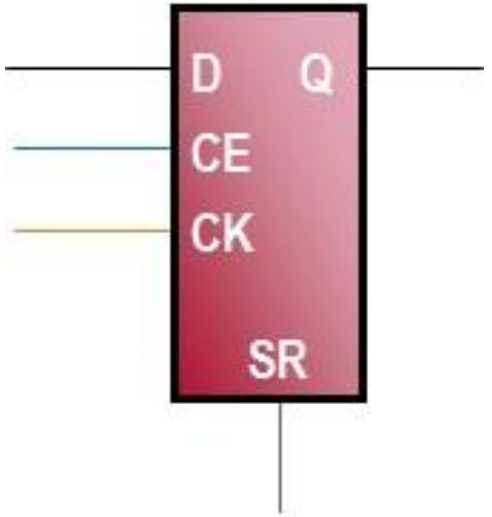
# Slice Flip-Flop Capabilities

- **All flip-flops are D type**
  - With Q output
- **All flip-flops have a single clock input (CK)**
  - Clock can be inverted at the slice boundary
- **All flip-flops have an active high chip enable (CE)**
- **All flip-flops have an active high SR input**
  - Input can be synchronous or asynchronous as determined by the corresponding configuration bit
  - Sets the flip-flop value to a pre-determined state as determined by the corresponding configuration bit



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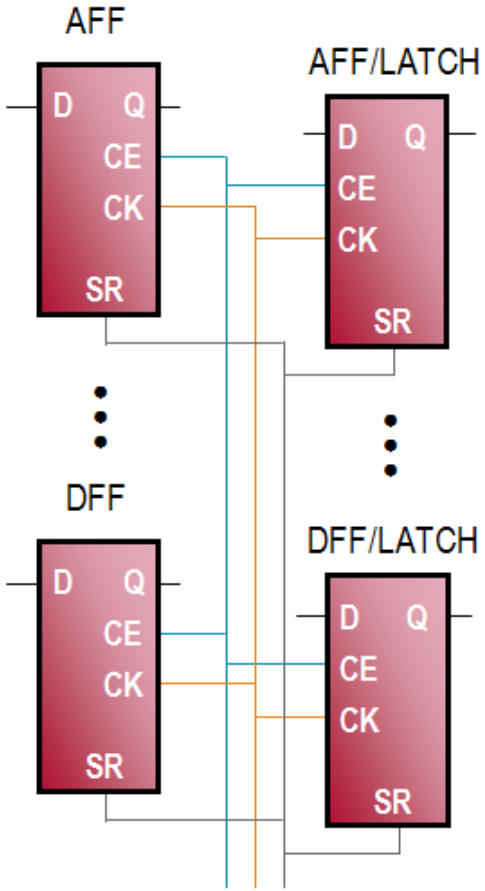
# Control Sets

- **All flip-flops and flip-flop/latches share the same CK, SR, and CE signals**
  - This is referred to as the "control set" of the flip-flops
  - CE and SR are active high
  - CK can be inverted at the slice boundary
- **If any one flip-flop uses a CE, all others must use the same CE**
  - CE gates the clock at the slice boundary
  - Saves power
- **If any one flip-flop uses the SR, all others must use the same SR**
  - The reset value used for each flip-flop is individually set by the SRVAL attribute



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# SLICEM Used as a Distributed SelectRAM Memory

- **SLICEM can be used for memory**
- **Synchronous write, asynchronous read**
  - Can be converted to synchronous read using the flip-flops available in the slice
- **Various configurations**
  - Single port
    - One LUT6 = 64x1 or 32x2 RAM
    - Cascadable up to 256x1 RAM
  - Dual port (D)
    - 1 read / write port + 1 read-only port
  - Simple dual port (SDP)
    - 1 write-only port + 1 read-only port
  - Quad-port (Q)
    - 1 read / write port + 3 read-only ports

| Single Port | Dual Port | Simple Dual Port | Quad Port |
|---|---|---|---|
| 32x2 | 32x2**D** | 32x6**SDP** | 32x2**Q** |
| 32x4 | 32x4**D** | 64x3**SDP** | 64x1**Q** |
| 32x6 | 64x1**D** | | |
| 32x8 | 64x2**D** | | |
| 64x1 | 128x1**D** | | |
| 64x2 | | | |
| 64x3 | | | |
| 64x4 | | | |
| 128x1 | | | |
| 128x2 | | | |
| 256x1 | | | |

**Each Port Has Independent Address Inputs**



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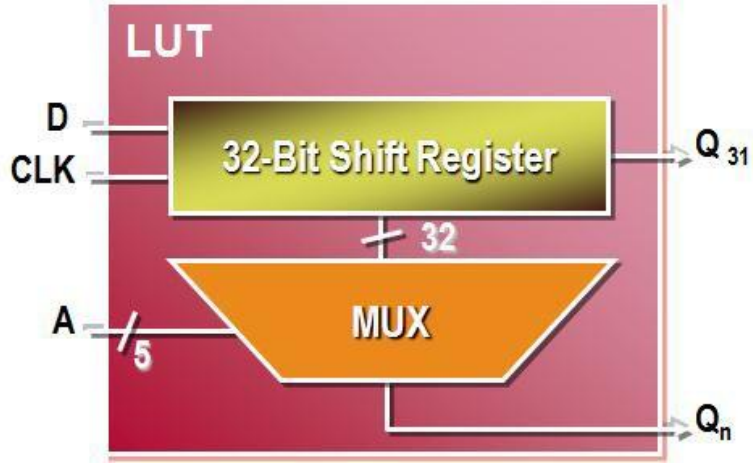
# SLICEM Used as 32-bit Shift Register

- **SRL = Shift Register Lut**
- **Versatile SRL-type shift registers**
  - Variable-length shift register
  - Synchronous FIFOs
  - Content-Addressable Memory (CAM)
  - Pattern generator
  - Compensate for delay / latency
- **Shift register length is determined by the address**
  - Constant value giving fixed delay line
  - Dynamic addressing for elastic buffer
- **Cascadable up to 128x1 shift register in one slice**




| SRL Configurations in One Slice (4 LUTs) |
|---|
| 16x1, 16x2, 16x4, 16x6, 16x8 |
| 32x1, 32x2, 32x3, 32x4 |
| 64x1, 64x2 |
| 96x1 |
| 128x1 |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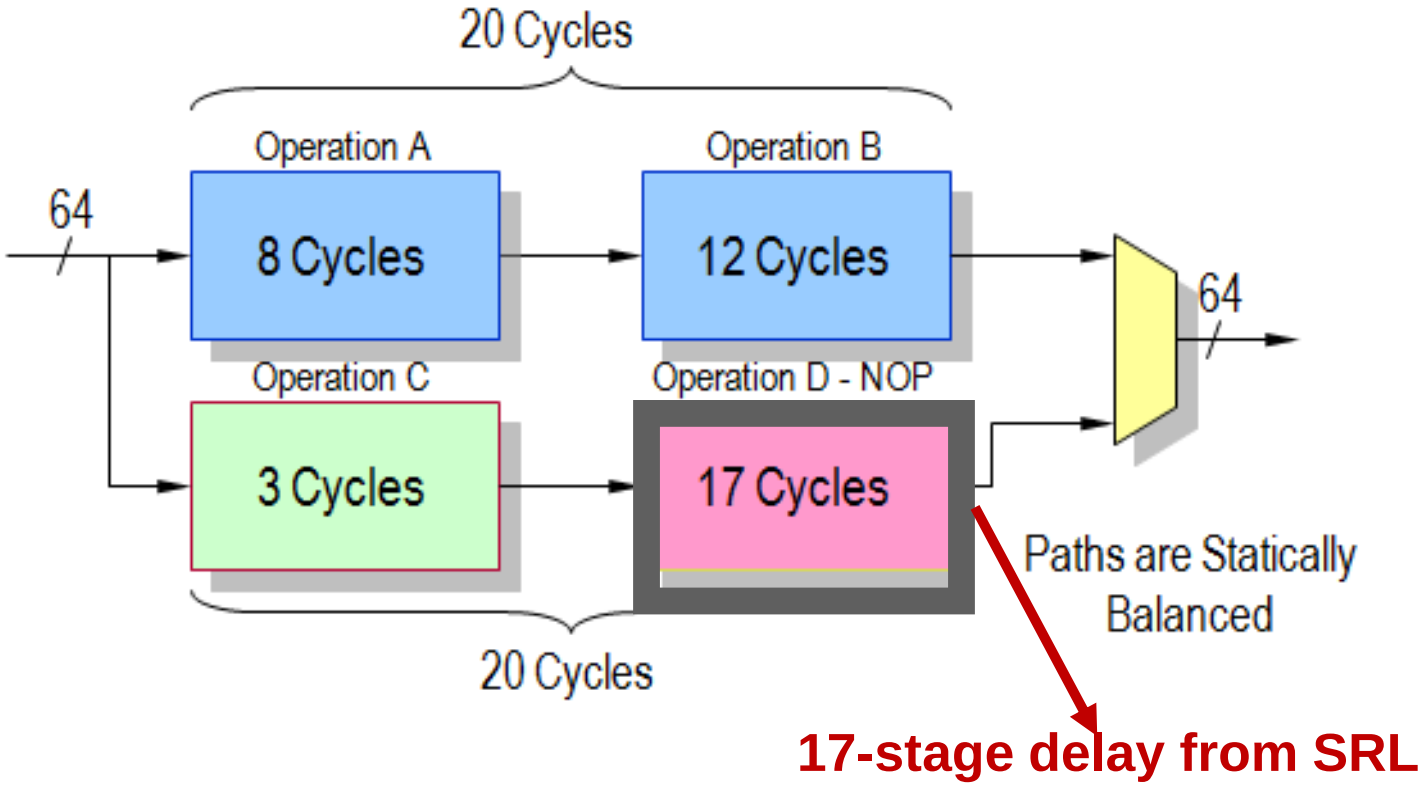
# Shift Register LUT Example

- **Operation D - NOP must add 17 pipeline stages of 64 bits each**
  - 1,088 flip-flops (hence 136 slices) or
  - 64 SRLs (hence 16 slices)



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# I/O Resources



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# I/O Interface Challenges

- **High-speed operation with maintained signal integrity**
  - Source-synchronous operation (clock forwarding)
  - System-synchronous operation (common systems clock)
  - Terminate transmission lines to avoid signal reflections
- **Drive and receive data on wide parallel buses**
  - Compensate for bus skew and clock timing errors
  - Conversion between serial and parallel data
  - Achieve very high bit rate (> 1 Gbps)
- **Single Data Rate (SDR) or Double Data Rate (DDR) interfaces**
- **Interface to many different standards**
  - Different voltages, drive strengths and protocols


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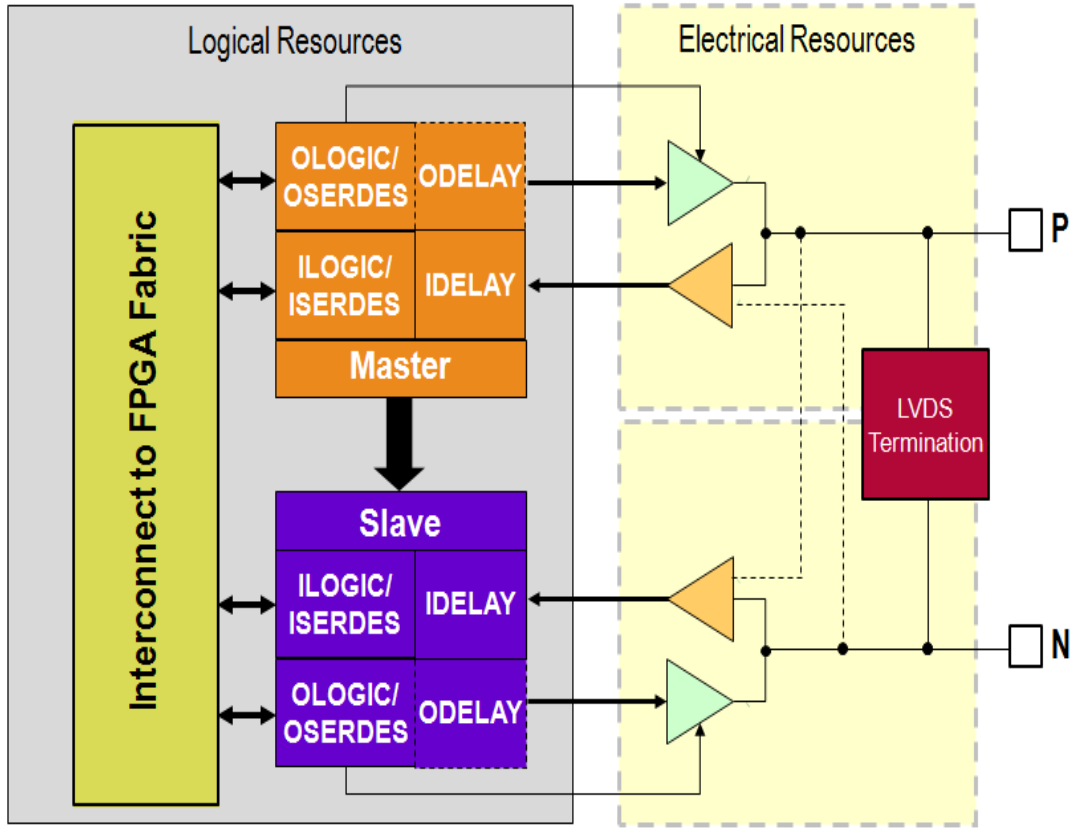
# 7-Series FPGA I/O

- **Wide range of voltages**
  - 1.2V to 3.3V operation
- **Wide I/O standards support**
  - Single ended and differential
  - Referenced voltage inputs
  - 3-state capability
- **Very high performance**
  - Up to 1600 Mbps LVDS
  - Up to 1866 Mbps single-ended for DDR3
- **Easy memory interfacing**
  - Hardware support for QDRII+ and DDR3
- **Digitally controlled impedance**
- **Power reduction features**



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# I/O Types

- **Two different types of I/O in 7-series FPGAs**
  - High Range (HR)
    - Supports I/O standards with Vcco voltages up to 3.3V
  - High Performance (HP)
    - Supports I/O standards with Vcco voltages up to 1.8V only
    - Designed for the highest performance
    - Has ODELAY and DCI capability

| I/O Types | Artix-7 Family | Kintex-7 Family | Virtex-7 Family | Virtex-7 XT/HT Family |
|---|---|---|---|---|
| High Range | All | Most | Some | |
| High Performance | | Some | Most | All |



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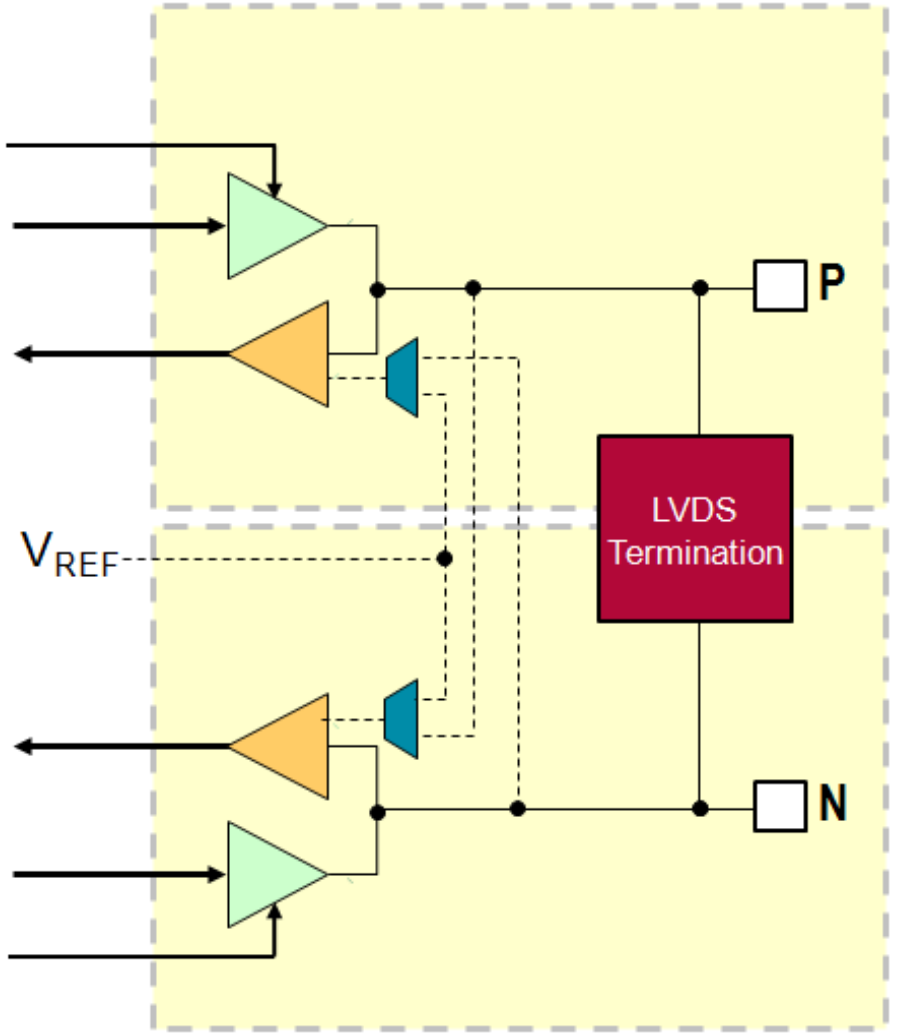
# I/O Electrical Resources

- **P and N pins can be configured as**
  - Individual single-ended signals or
  - Differential pair
- **Receiver can be standard CMOS or voltage comparator**
  - When standard CMOS
    - Logic 0 when "near" ground
    - Logic 1 when "near" $V_{CCO}$
  - Referenced to $V_{REF}$
    - Logic 0 when below $V_{REF}$
    - Logic 1 when above $V_{REF}$
  - Differential
    - Logic 0 when $V_P < V_N$
    - Logic 1 when $V_P > V_N$



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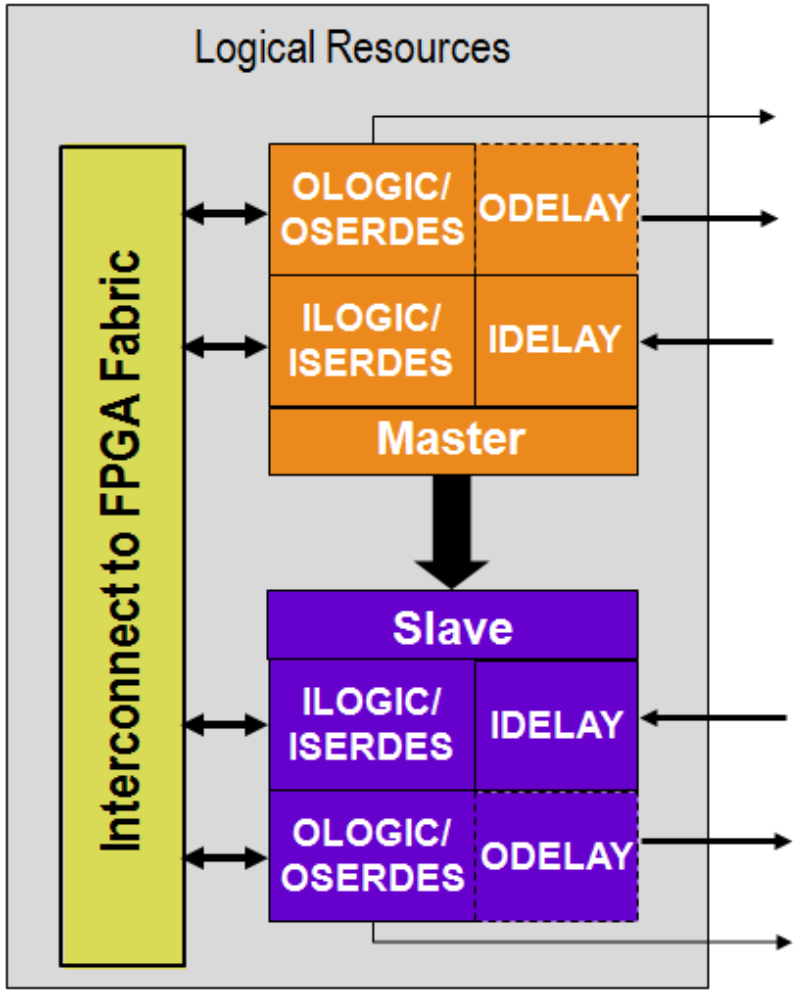
# I/O Logical Resources

- **Two blocks of logic per I/O pair**
  - Master and slave
  - Can operate independently or concatenated
- **Each block contains**
  - ILOGIC/ISERDES
    - SDR, DDR, or high-speed serial input logic
  - OLOGIC/OSERDES
    - SDR, DDR, or high-speed serial output logic
  - IDELAY
    - Selectable fine-grained  input delay
  - ODELAY
    - Selectable fine-grained output delay
    - Only available on High Performance I/O



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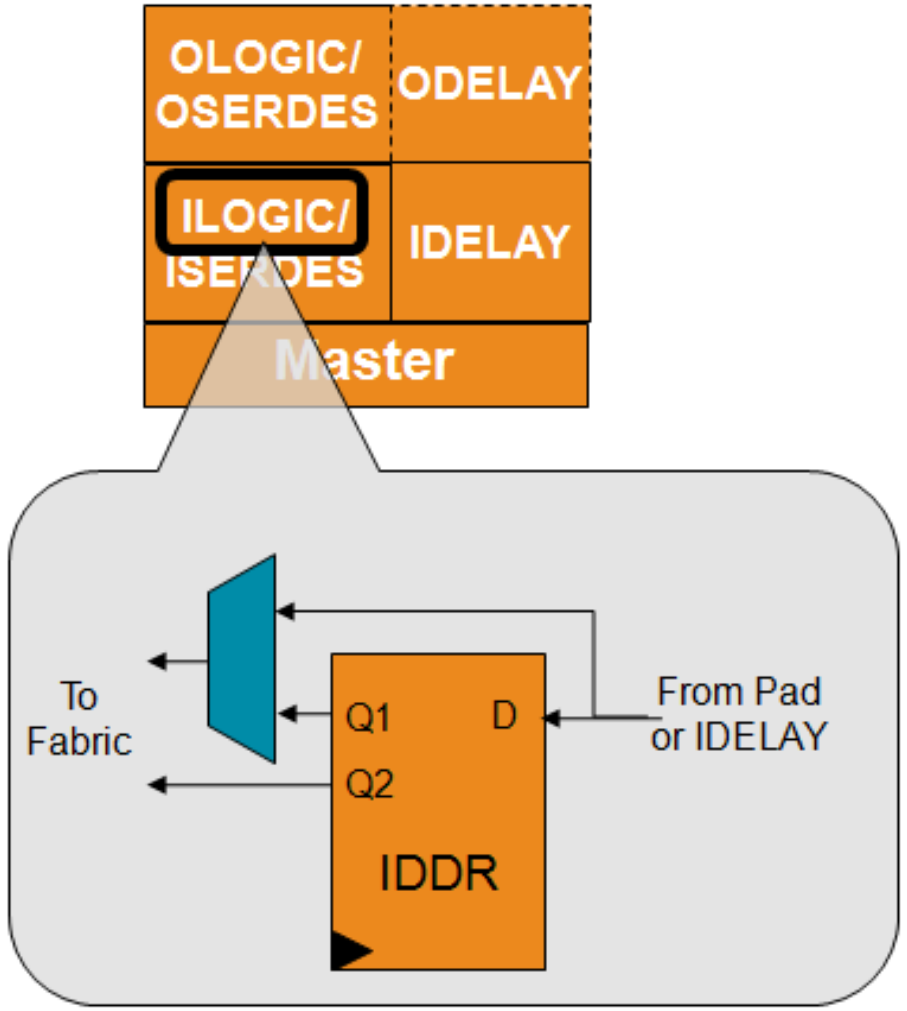
# ILOGIC: Input SDR and DDR Logic

- **Two types of ILOGIC blocks**
  - ILOGICE2 for High Performance banks
  - ILOGICE3 for High Range banks
    - Has zero hold delay capability
- **ILOGIC inputs come from the input receiver**
  - Directly or via the IDELAY block
- **Outputs drive the FPGA fabric**
  - Directly (no clocked logic) or
  - Via the IDDR
    - In SDR mode on rising or falling edge of clock
    - In DDR mode on both edges of clock
      - Can also use two clocks, 180° out of phase



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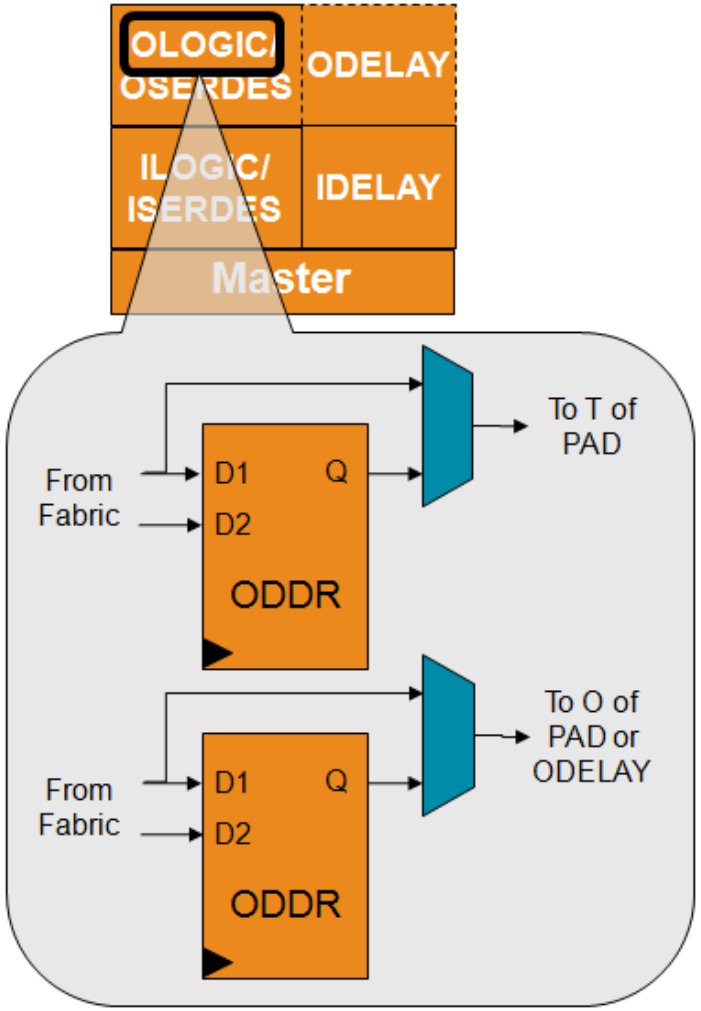
# OLOGIC: Output SDR and DDR Logic

- **OLOGICE2 for HP banks, OLOGICE3 for HR banks**
- **Output of OLOGIC connects to the output driver directly, or via the ODELAY**
  - ODELAY is available in HP banks only
- **Output is driven directly from the fabric**
  - Directly, through an SDR flip-flop or via the ODDR using both edges of clock
- **Each OLOGIC block contains two ODDR**
  - One for controlling the data to the output driver
  - One for controlling the 3-state enable
  - Both ODDR are driven by same clock and reset
- **SAME_EDGE or OPPOSITE_EDGE only**



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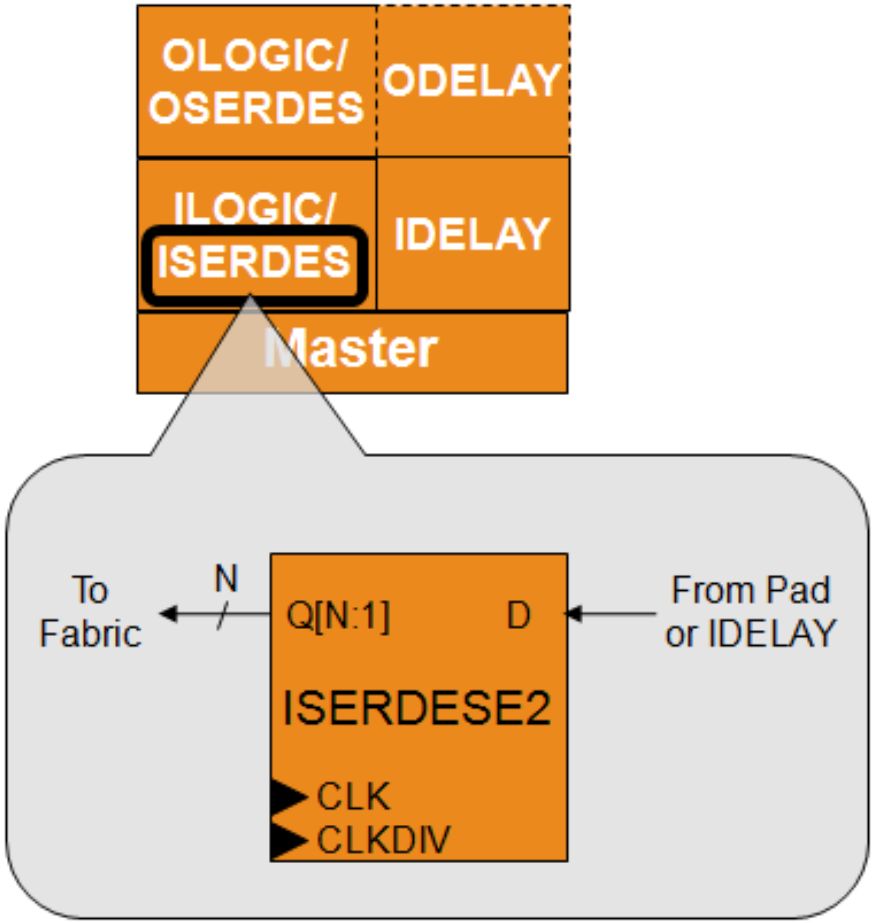
# ISERDES: Input Serial-to-Parallel Converter

- **Clocks in data from input pad or IDELAY**
  - D is clocked on high speed clock (CLK)
  - Can be SDR or DDR
- **Sends de-serialized data to fabric**
  - Q is clocked on low speed clock (CLKDIV)
- **CLK and CLKDIV must be in phase**
- **De-serializes data**
  - Single data rate: 2, 3, 4, 5, 6, 7, 8
  - Double data rate: 4, 6, 8
- **Cascade with slave for wider ratios**
  - Double data rate: 10, 14
- **Has BITSLIP logic for framing parallel data**



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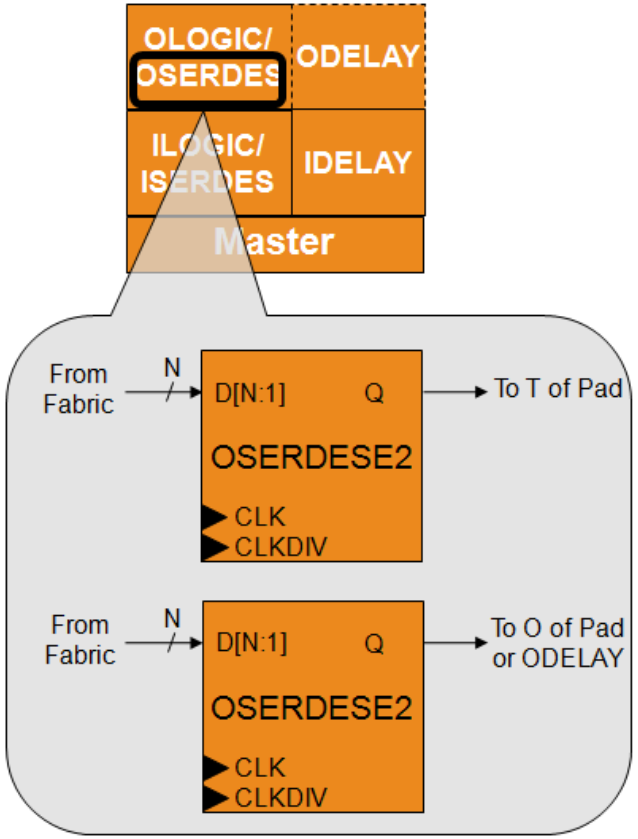
# OSERDES: Output Parallel-to-Serial Converter

- **Serializes out data to output pad or ODELAY**
  - Q is clocked on high speed clock (CLK)
  - Can be SDR or DDR
- **Parallel data comes from fabric**
  - D is synchronous to low speed clock (CLKDIV)
- **CLK and CLKDIV must be in phase**
- **Serializes data**
  - Single data rate: 2, 3, 4, 5, 6, 7, 8
  - Double data rate: 4, 6, 8
- **Cascade with slave for wider ratios**
  - Double data rate: 10, 14




- **When using 3-state serializer, both the data and 3-state width must be 4**
  - Clocks are shared between both serializers



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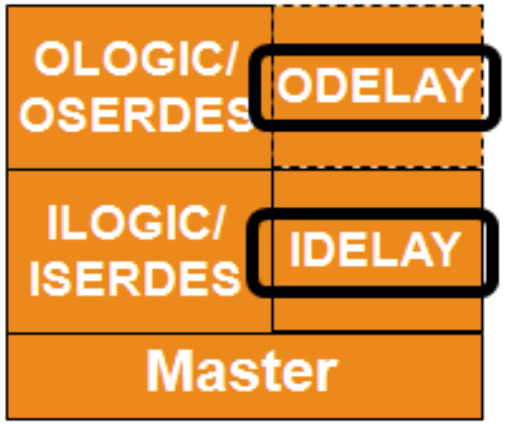
# IDELAY and ODELAY

- **Separate IDELAY and ODELAY delay lines**
  - IDELAY is available in both HR and HP banks
  - ODELAY is only available in HP banks
- **Delay line elements are calibrated using the IDELAYCTRL cell**
  - Delay is process, temperature, and voltage independent
- **IDELAY and ODELAY have almost identical capabilities**
  - IDELAY can also be accessed from the fabric
- **Tap counter value can be accessed via FPGA fabric**
  - Monitor, increment, decrement, or set the tap value; tap value can be from 0 to 31
- **Reference frequency can be 200 MHz in all speed grades; 300 MHz is also allowed in fastest speed grade**
  - Results in 78 ps or 52 ps per tap





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# Memory and DSP48 Resources



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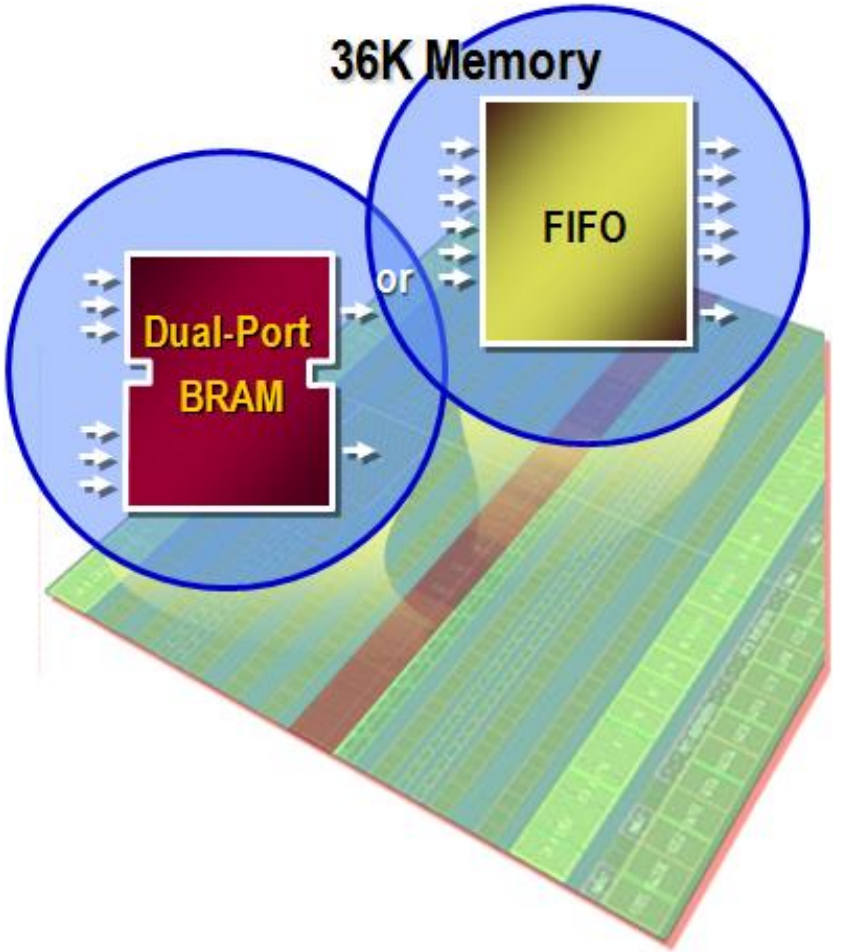
# 7-Series Block RAM and FIFO

- **All members of the 7-series families have the same Block RAM/FIFO**
- **Fully synchronous operation**
  - All operations are synchronous; all outputs are latched
- **Optional internal pipeline register for higher frequency operation**
- **Two independent ports access common data**
  - Individual address, clock, write enable, clock enable
  - Independent data widths for each port





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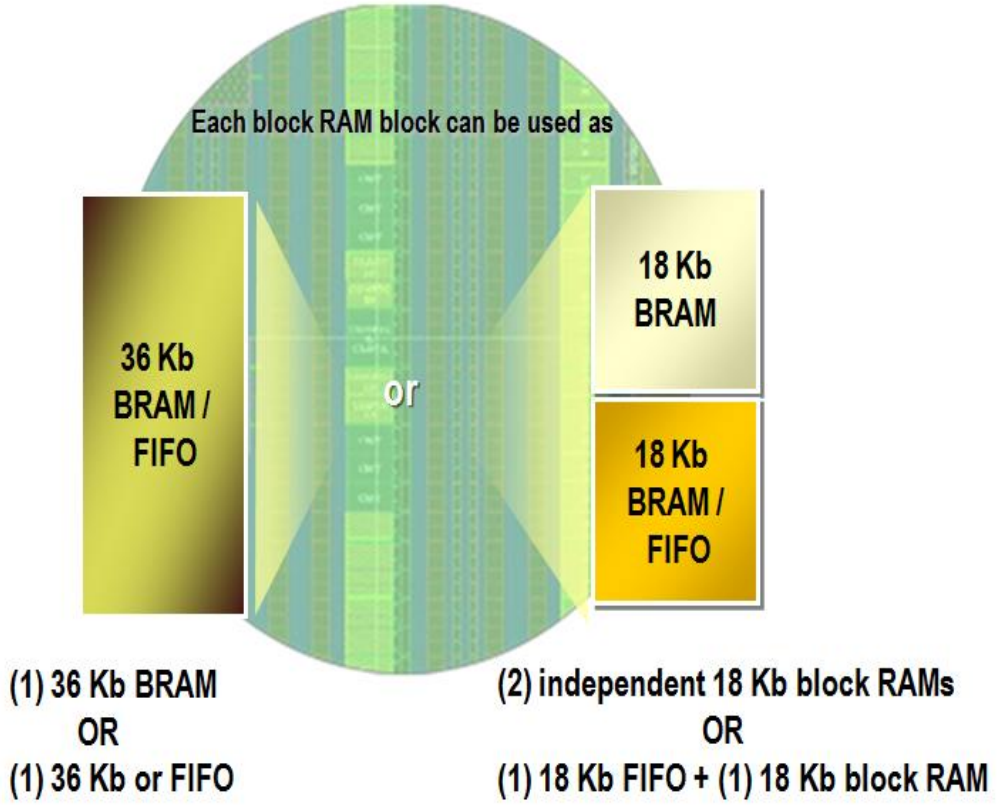
# 7-Series Block RAM and FIFO

- **Multiple configuration options**
  - True dual-port, simple dual-port, single-port
- **Integrated cascade logic**
- **Byte-write enable in wider configurations**
- **Integrated control for fast and efficient FIFOs**
- **Integrated 64 / 72-bit Hamming error correction**
- **Separate Vbram voltage supply rail to ensure block memory functionality in -1L**



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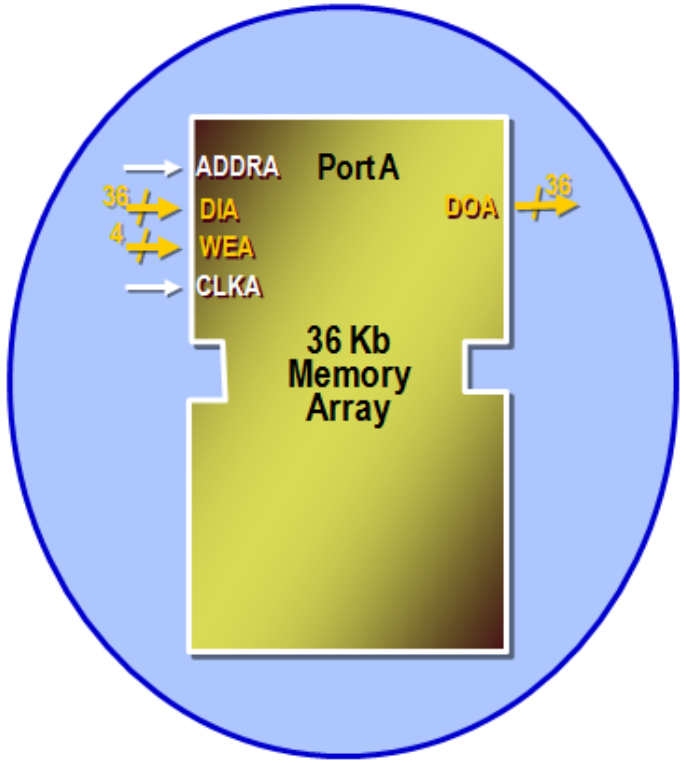
# Single-Port Block RAM

- **Single read/write port**
  - Clock: CLKA, Address: ADDRA, Write enable: WEA
  - Write data: DIA, Read data: DOA
- **36-kbit configurations**
  - 32k x 1, 16k x 2, 8k x 4, 4k x 9, 2k x 18, 1k x 36
- **18-kbit configurations**
  - 16k x 1, 8k x 2, 4k x 4, 2k x 9, 1k x 18, 512 x 36
- **Configurable write mode**
  - WRITE_FIRST: Data written on DIA is available on DOA
  - READ_FIRST: Old contents of RAM at ADDRA is presented on DOA
  - NO_CHANGE: The DOA holds its previous value (saves power)
- **Optional output register for maximum performance (DOA_REG=1)**





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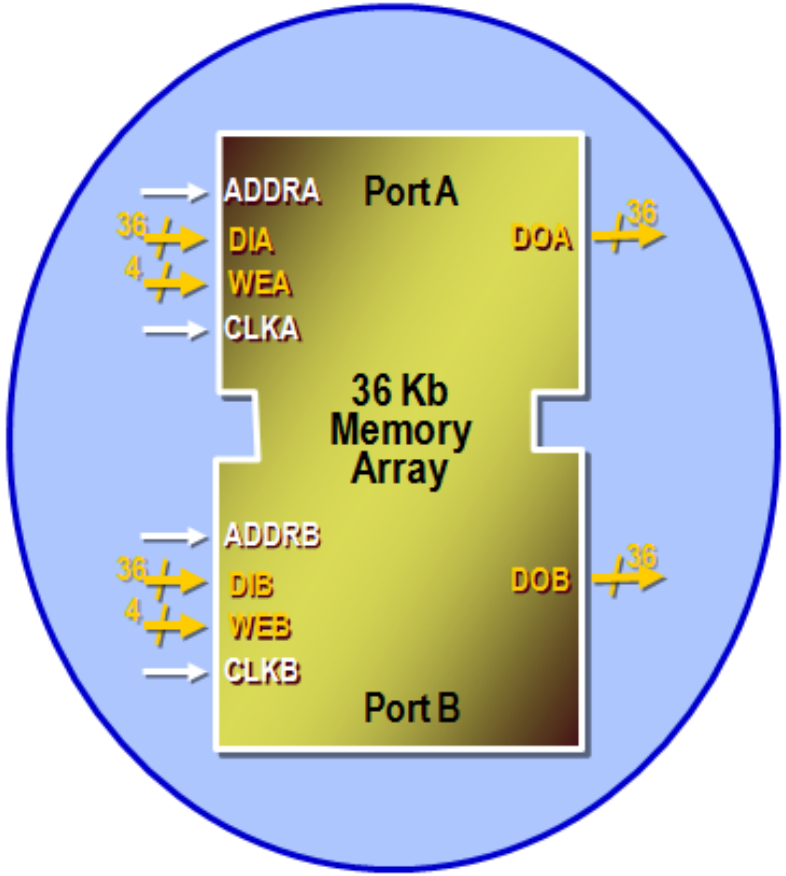
# Dual-Port Block RAM

- **Two separate read/write ports**
  - Each port has separate clock, address, data in, data out, and write enable
    - Clocks can be asynchronous to each other
  - The two ports can have different widths
    - Same configurations as when single ported
  - The two ports can have different write modes
- **No contention avoidance when both ports access the same address, except**
  - If clocked by the same clock, and the write port is READ_FIRST, the read port gets the old data



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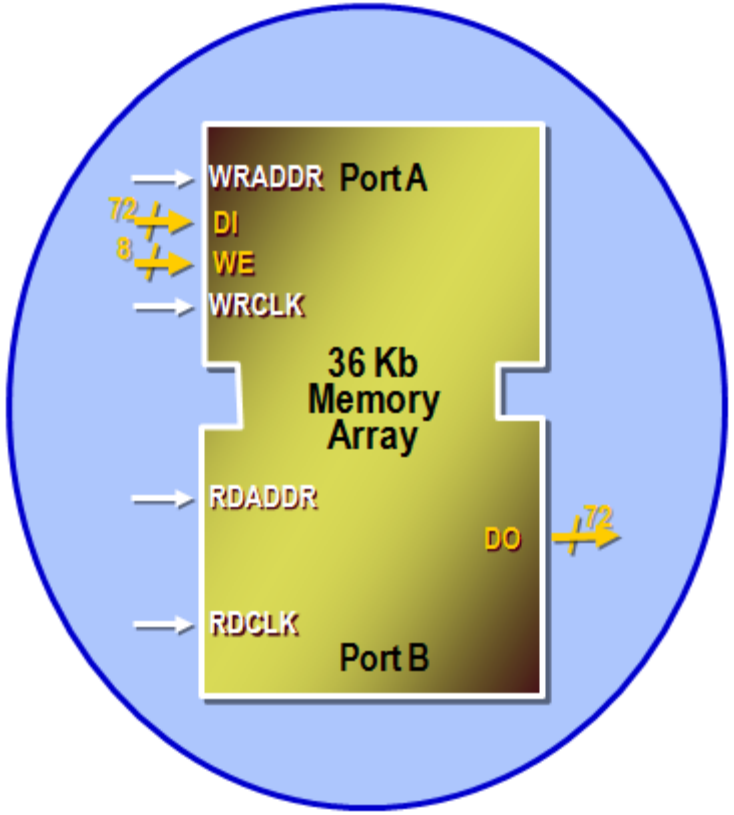
# Simple Dual-Port Block RAM

- **One read port and one write port**
  - Each port has separate clock and address
- **In 36-kbit configuration, one of the two ports must be 72 bits wide**
  - The other port can be x1, x2, x4, x9, x18, x36, or x72
- **In 18-kbit configuration, one of the two ports must be 36 bits wide**
  - The other port can be x1, x2, x4, x9, x18, or x36





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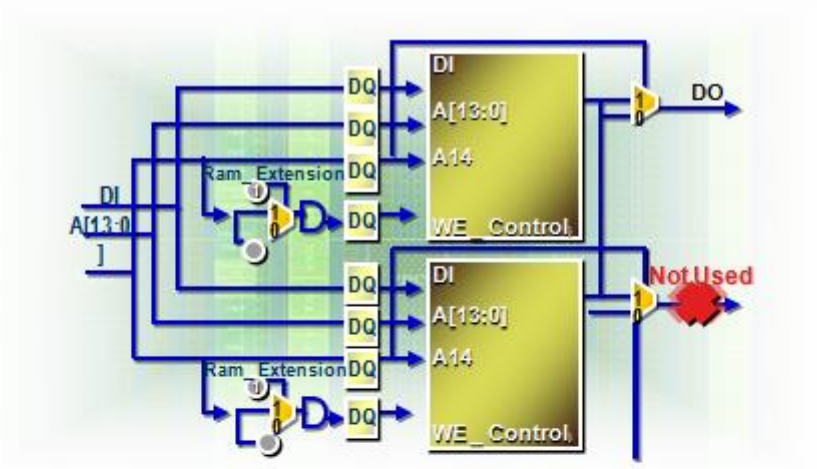
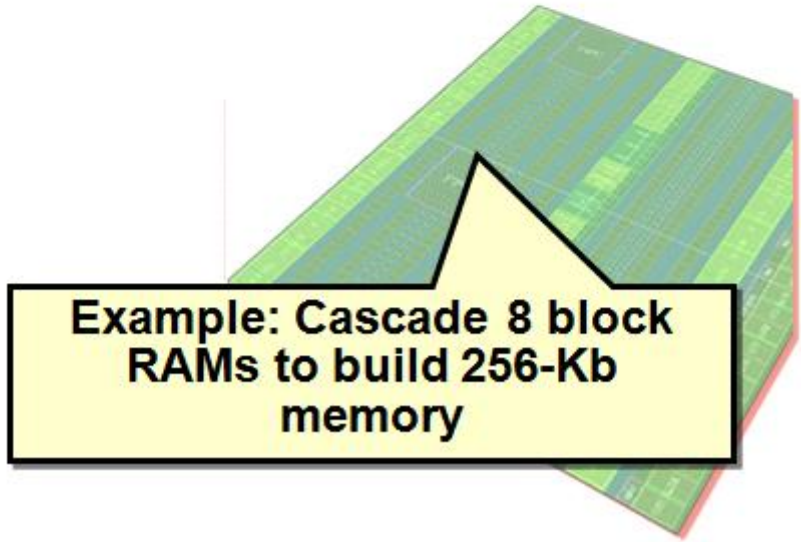
# Block RAM Cascading

- **Built-in cascade logic for 64Kx1**
  - Cascade *two* vertically adjacent 32Kx1 block RAMs without using external CLB logic or compromising performance
  - Saves resources and improves speed of larger memories
- **Cascade option for larger arrays**
  - 128Kb, 256Kb, 512Kb, 1 Mb, …
  - Using external CLB logic for depth expansion
    - Not quite as fast as cascaded block RAMs
  - Width expansion uses parallel block RAMs



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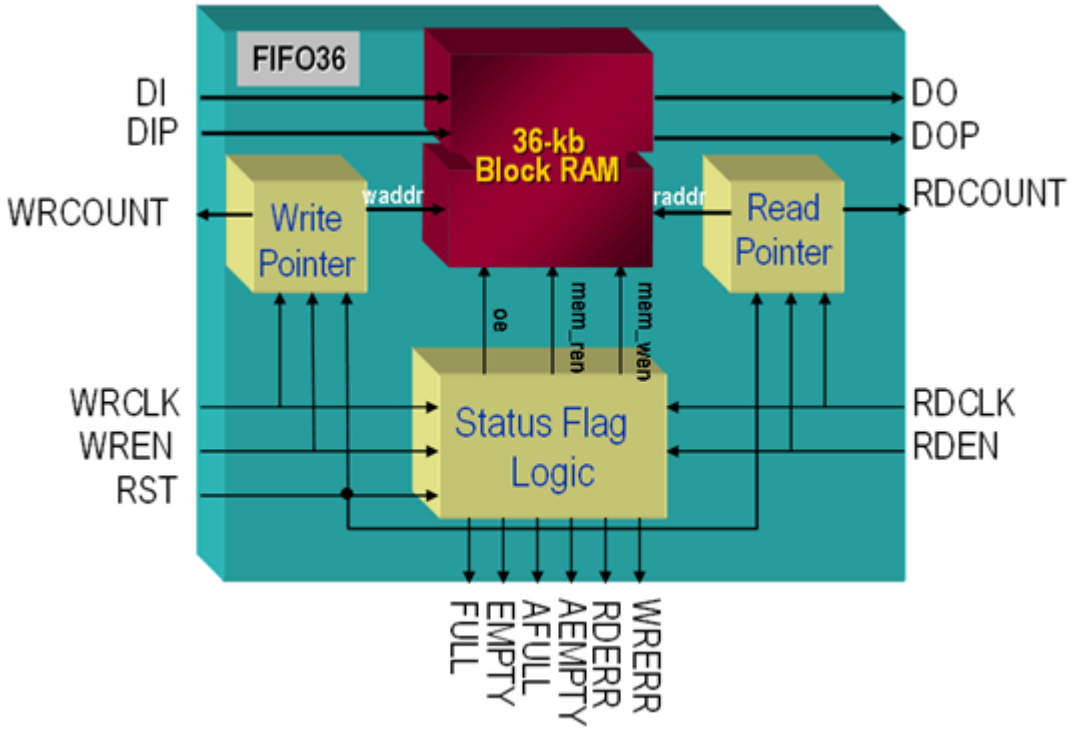
# FIFO

- **Full featured**
  - Synchronous or asynchronous read and write clocks
  - Four flags
    - Full, empty, programmable almost-full/empty
  - Optional first-word-fall-through
- **FIFO configurations**
  - Any 36-Kb block RAM: 8Kx4, 4Kx9, 2Kx18, 1Kx36, 512x72
  - Any 18-Kb block RAM: 4Kx4, 2Kx9, 1Kx18, 512x36
  - Write and read width must be equal




- **Can use the integrated error correction when used in the x72 width**



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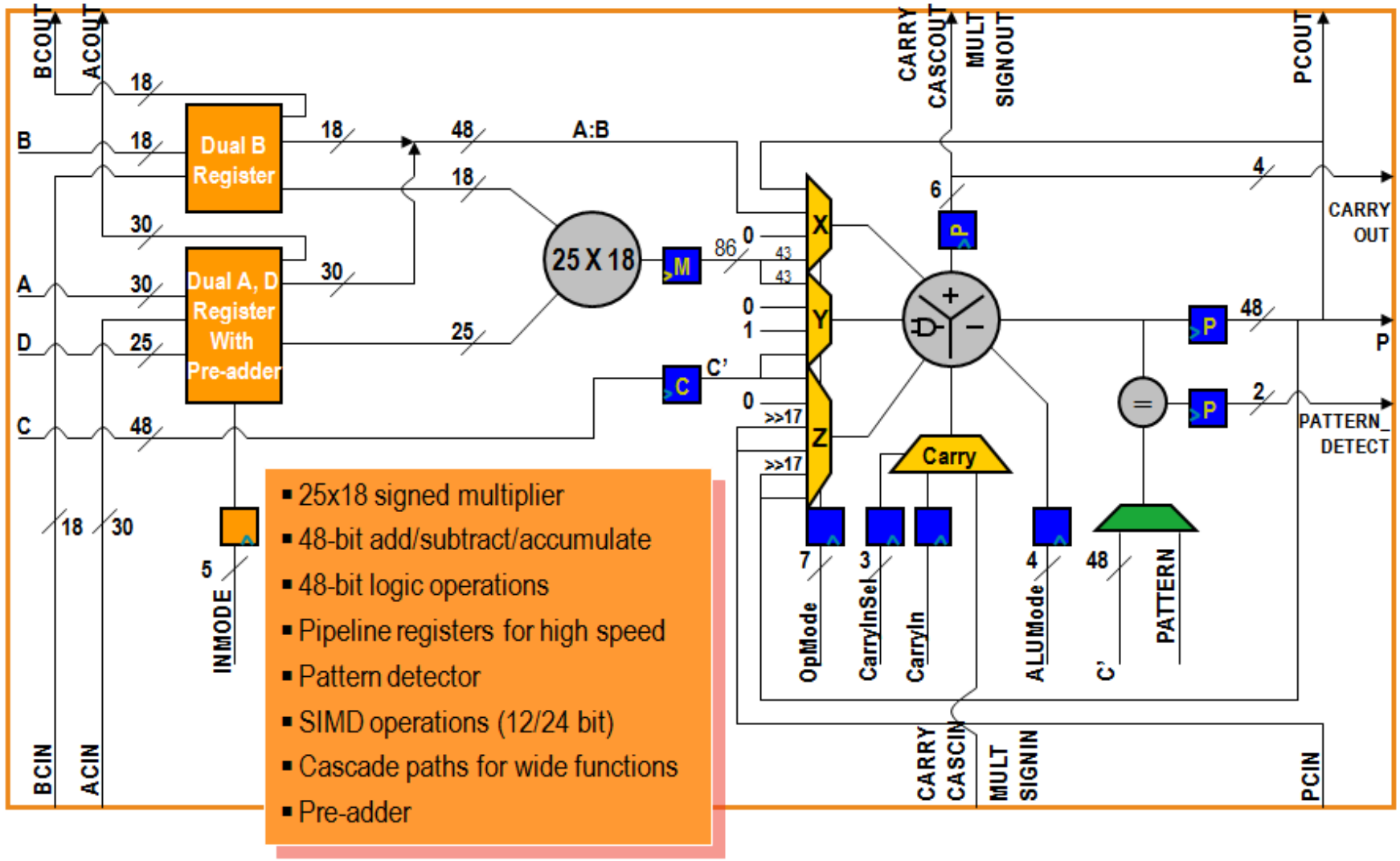
# 7-Series DSP48E1 Slice



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# Using DSP48 for Non-DSP Function

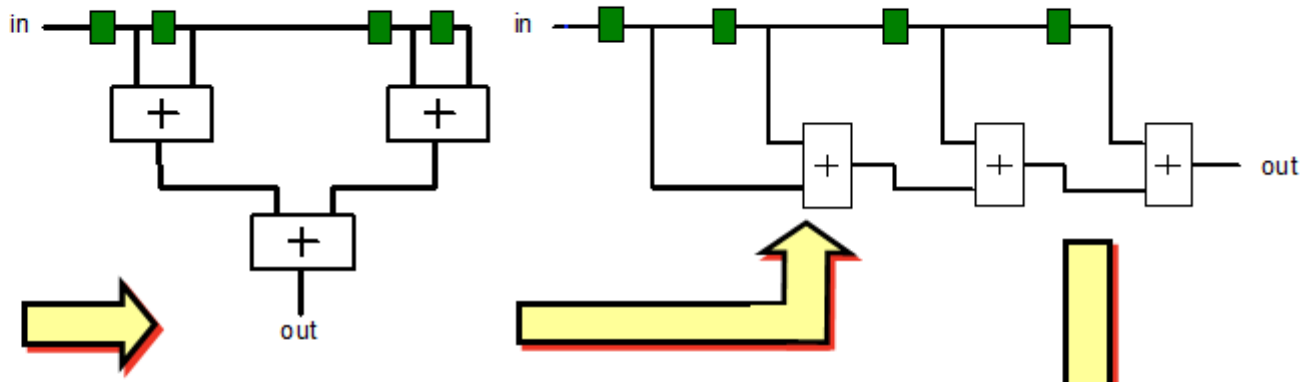
**START:** This is the typical adder tree found in many signal processing designs

1

**Remove** all **pipelining** from the tree. This makes it easier to understand and visualize the changes

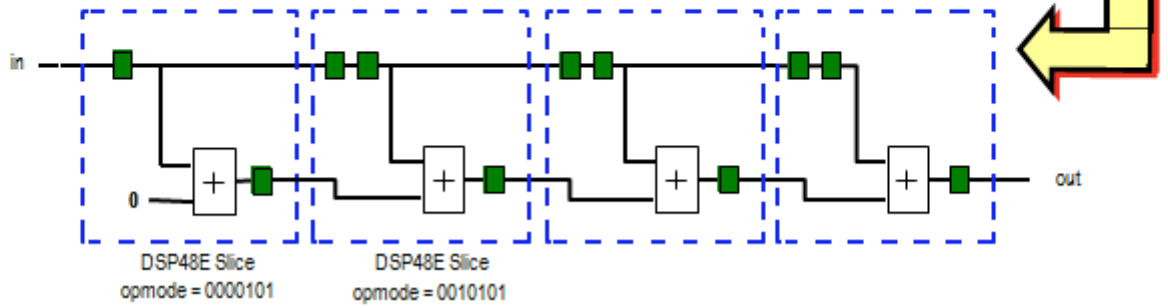
2

**Rearrange** the tree. Notice that functionally has not changed. The diagram has just been redrawn




3

**Pipelining** is required for performance. Adding one in the chain requires one in the data path delay as well. Determining mapping to DSP48E is easy now



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# XADC



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# XADC and AMS

- **XADC is a high quality and flexible analog interface new to the 7-series**
  - Dual 12-bit 1Msps ADCs, on-chip sensors, 17 flexible analog inputs, and track & holds with programmable signal conditioning
  - 1V input range
  - 16-bit resolution conversion
  - Built in digital gain and offset calibration
- **Analog Mixed Signal (AMS)**
  - Using the FPGA programmable logic to customize the XADC and replace other external analog functions; for example, linearization, calibration, filtering, and DC balancing to improve data conversion resolution


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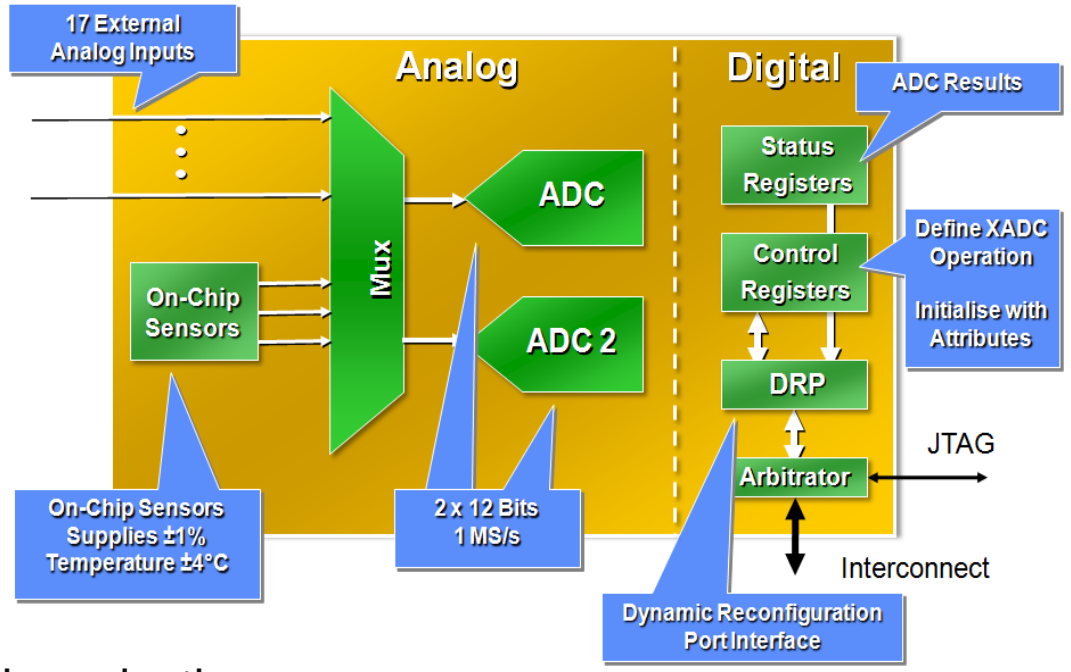
# XADC Block Diagram

- **Fast sampling**
  - Conversion time of 1 us with support for simultaneous sampling
  - Flexible timing modes (self and externally triggered sampling modes)
  - Separate track/hold amplifier for each ADC ensures maximum throughput using multiplexed analog input channels
- **Flexible analog inputs**
  - Differential analog inputs with high common mode noise rejection
  - Support for unipolar, bipolar, and true differential input signal types



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# XADC's Other Features

- **Internal and external multiplexing and sampling**
  - Can sample internal power supplies and temperature
  - Multiplexes internal sources and 17 external analog inputs
  - Can control an external analog multiplexer to reduce pin count
- **Flexible triggering**
  - Conversion data is stored in internal status registers
  - Internal control registers control source selection, sampling, and alarms
  - Registers can be accessed internally via the dynamic reconfiguration port (DRP)
  - Register can be accessed via JTAG
    - Available on power up, before configuration
- **Operates over a wide temperature range (–40°C to +125°C)**


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# Clocking Resources



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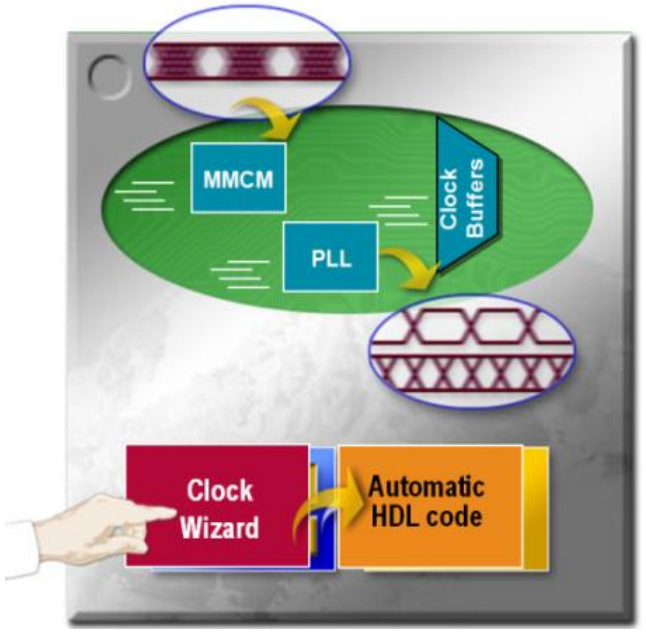
# 7-Series FPGAs Clock Management

- **Global clock buffers**
  - High fanout clock distribution buffer
- **Low-skew clock distribution**
  - Regional clock routing
- **Clock regions**
  - Each clock region is 50 CLBs high and spans half the device
- **Clock management tile (CMT)**
  - One Mixed-Mode Clock Managers (MMCMs) and one Phase Locked Loop (PLL) in each Clock
  - Performs frequency synthesis, clock de-skew, and jitter-filtering
  - High input frequency range
- **Simple design creation through the Clocking Wizard**





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# Clock-Capable Inputs

- **All synchronous designs need at least one external clock reference**
  - These clocks need to be brought into the FPGA
- **Every 7-series FPGA has clock-capable inputs in every I/O bank**
  - These inputs are regular I/O pins with dedicated connections to internal clock resources
  - Each I/O bank has 4 clock capable pins
    - 2x Multi-Region Clock Capable (MRCC)
    - 2x Single Region Clock Capable (SRCC)
  - Each clock input can be used as a single-ended clock input, or can be paired with an adjacent pin to form a differential clock input
    - Each bank can therefore have four single-ended or four differential clock inputs

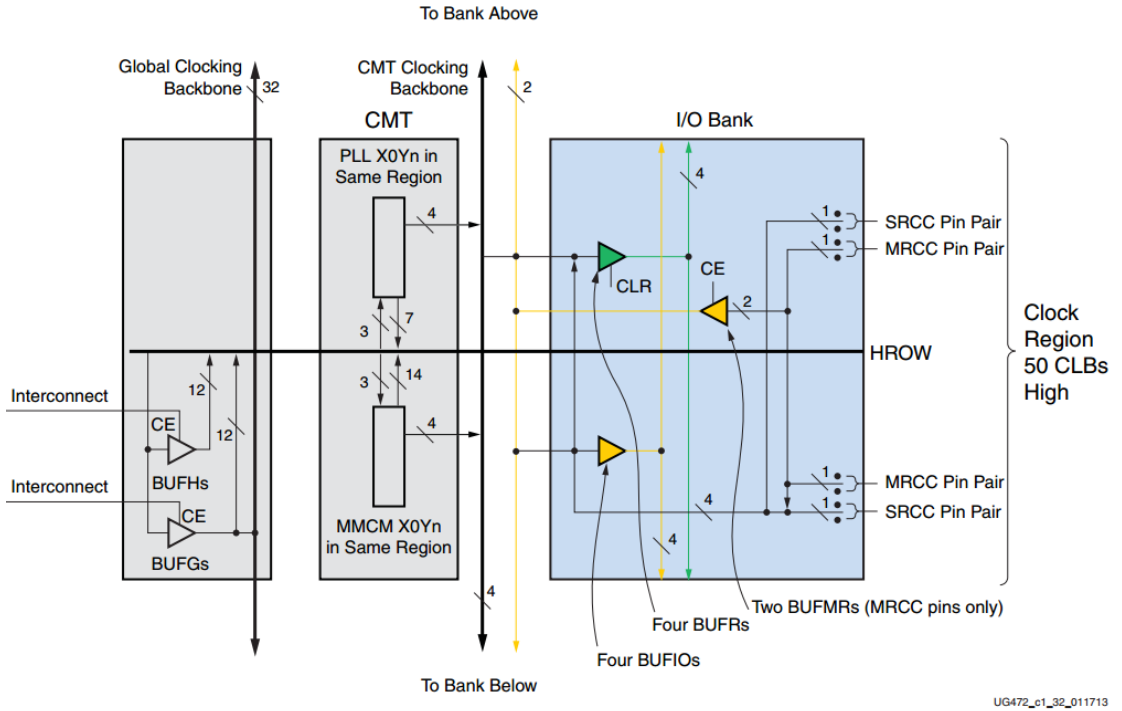


*Figure 1-3:* **Single Clock Region (Right Side of the Device)**



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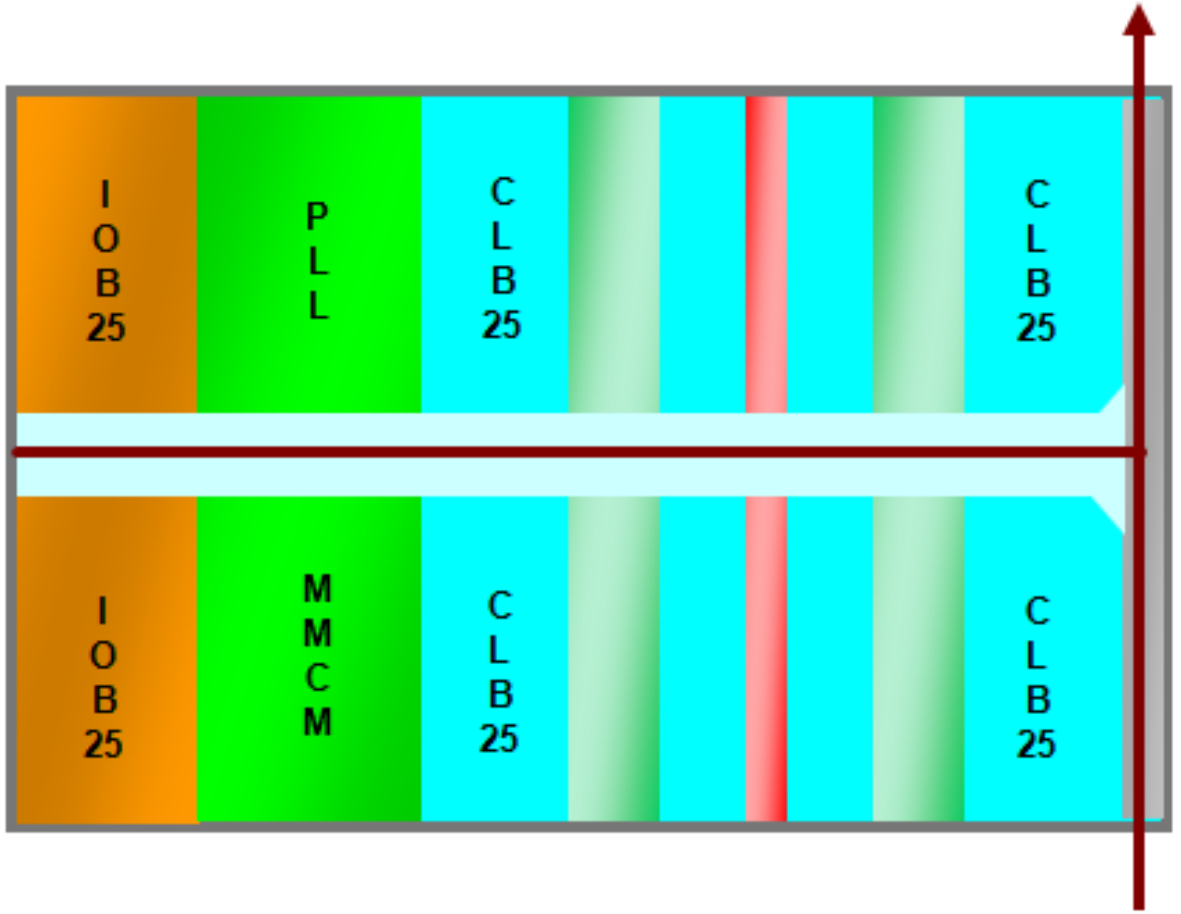
# 7-Series FPGA Clock Regions

- **Larger clock region than previous families**
  - 50 CLBs high, 50 I/Os high
  - Same size as I/O bank
  - Half width of device
  - 2–24 regions per device for 7-Series
- **Resources per clock region**
  - 12 global clock networks
    - Driven by BUFH
  - 4 regional clock networks
    - Driven by BUFR
  - 4 I/O clock networks
    - Driven by BUFIO



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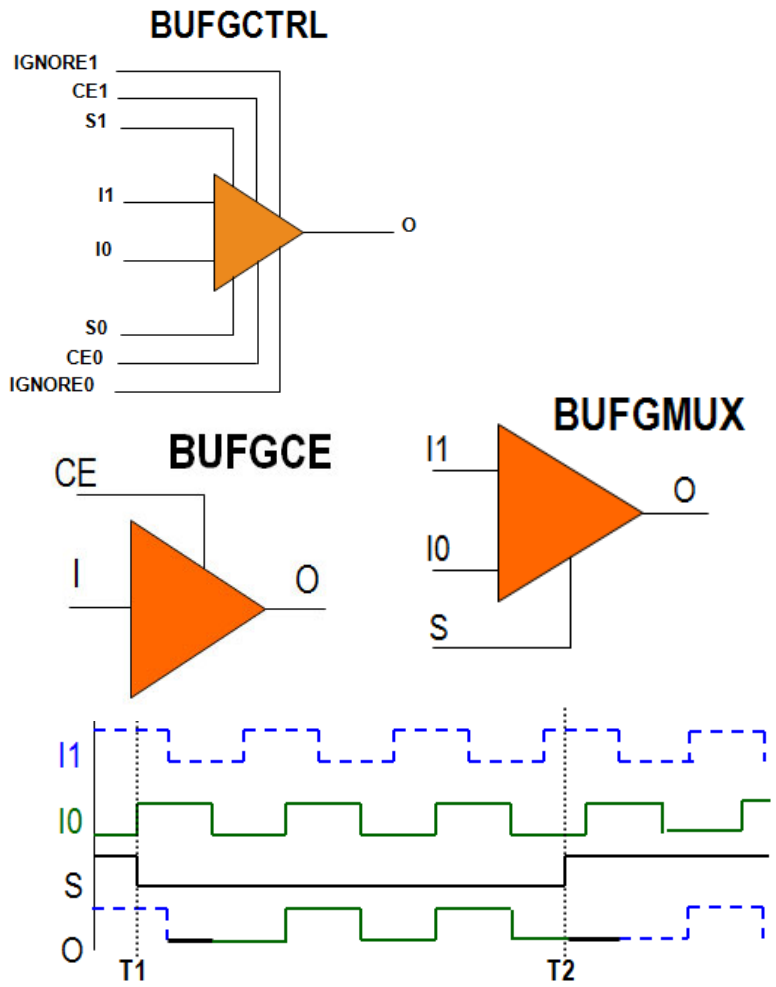
# Global Clock Buffer (BUFGCTRL)

- **BUFGCTRLs (or BUFG) reside in the center of the device**
- **BUFGCTRLs can be driven by**
  - Clock-capable I/O (CCIO) in the same half
  - CMT outputs in the same half
  - Gigabit transceiver clocks in the same half
  - Other BUFG, interconnect, or BUFR
- **BUFGCTRL outputs drive the vertical global clock spine**
- **BUFGCTRL component implements**
  - Simple clock buffer (BUFG)
  - Clock buffer with clock switching (BUFGMUX or BUFGMUX_CTRL)
  - Clock buffer with clock enable (BUFGCE)



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# Zynq SoC



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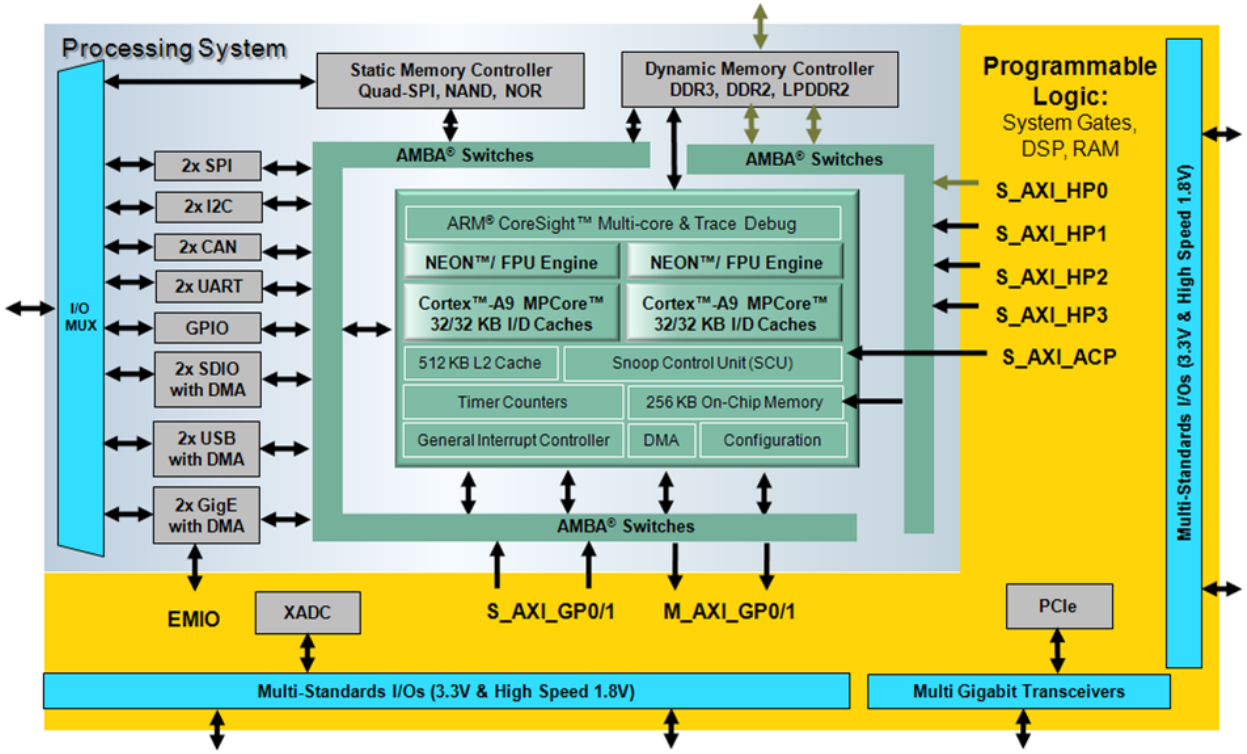
# Zynq-7000 Family Highlights

- **Complete ARM®-based processing system**
  - Application Processor Unit (APU)
    - Dual ARM Cortex™-A9 processors
    - Caches and support blocks
  - Fully integrated memory controllers
  - I/O peripherals
- **Tightly integrated programmable logic**
  - Used to extend the processing system
  - Scalable density and performance
- **Flexible array of I/O**
  - Wide range of external multi-standard I/O
  - High-performance integrated serial transceivers
  - Analog-to-digital converter inputs



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# The PS and the PL

- **The Zynq-7000 SoC architecture consists of two major sections**
  - PS: Processing system
    - Single/Dual ARM Cortex-A9 processor based
    - Multiple peripherals
    - Hard silicon core
  - PL: Programmable logic
    - Shares the same 7-series programmable logic as
      - Artix™-based devices: Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015 and Z-7020
      - Kintex™-based devices: Z-7030, Z-7035, Z-7045 and Z-7100

| Features | Zynq-7000S | Zynq-7000 | |
|---|---|---|---|
| Devices | Z-7007S, Z-7012S, Z-7014S | Z-7010, Z-7015, Z-7020 | Z-7030, Z-7035, Z-7045, Z-7100 |
| Processor Core | Single-core ARM® Cortex™-A9 MPCore™ | Dual-core ARM Cortex-A9 MPCore | |
| Maximum Frequency | Up to 766MHz | Up to 866 MHz | Up to 1GHz |
| External Memory Support | DDR3, DDR3L, DDR2, LPDDR2 | | |
| Key Peripherals | USB 2.0, Gigabit Ethernet, SD/SDIO | | |
| Dedicated Peripheral Pins | Up to 128 | Up to 128 | 128 |



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# Summary



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# Summary

- **The 7-series FPGA slices contain four 6-input LUTs, eight registers, and carry logic**
  - LUTs can perform any combinatorial function of up to six inputs
  - LUTs are connected with dedicated multiplexers and carry logic
  - Some LUTs can be configured as shift registers or memories
  - Slices also contain carry logic and the MUXF7 and MUXF8 multiplexers
  - The MUXF7 multiplexers combine LUT outputs to create 7-input functions or 8-input multiplexers
  - The MUXF8 multiplexers combine the MUXF7 outputs to create 8-input functions or 16-input multiplexers
  - The carry logic can be used to implement fast addition, subtraction, and comparison operations
- **The 7-series FPGA IOBs contain DDR registers as well as SERDES resources**
- **The SelectIO™ interfaces enable direct connection to multiple I/O standards**


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# Summary

- The 7-series FPGA includes dedicated block RAM and DSP slice resources
- The 7-series FPGAs includes dedicated MMCMs, PLLs, and routing resources to improve your system clock performance and generation capability
- The 7-series FPGAs include other dedicated hardware such as XADC
- The Zynq-7000 processing platform is a system on a chip (SoC) processor with embedded programmable logic fabric of either Artix or Kintex 7-series FPGA


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# Thank You

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