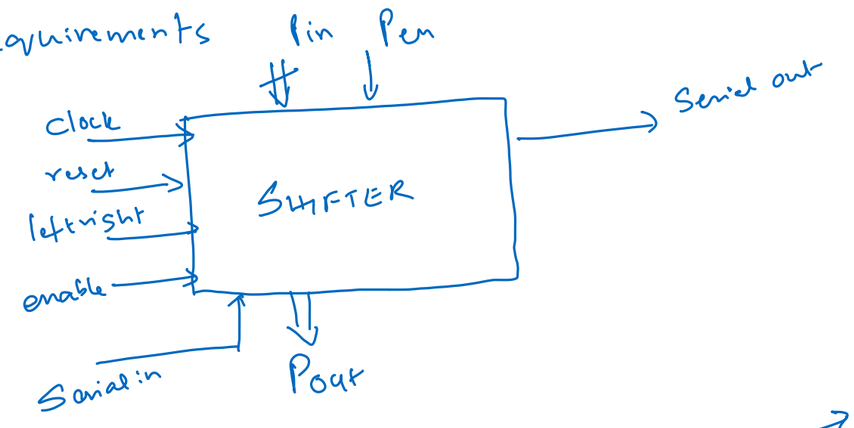
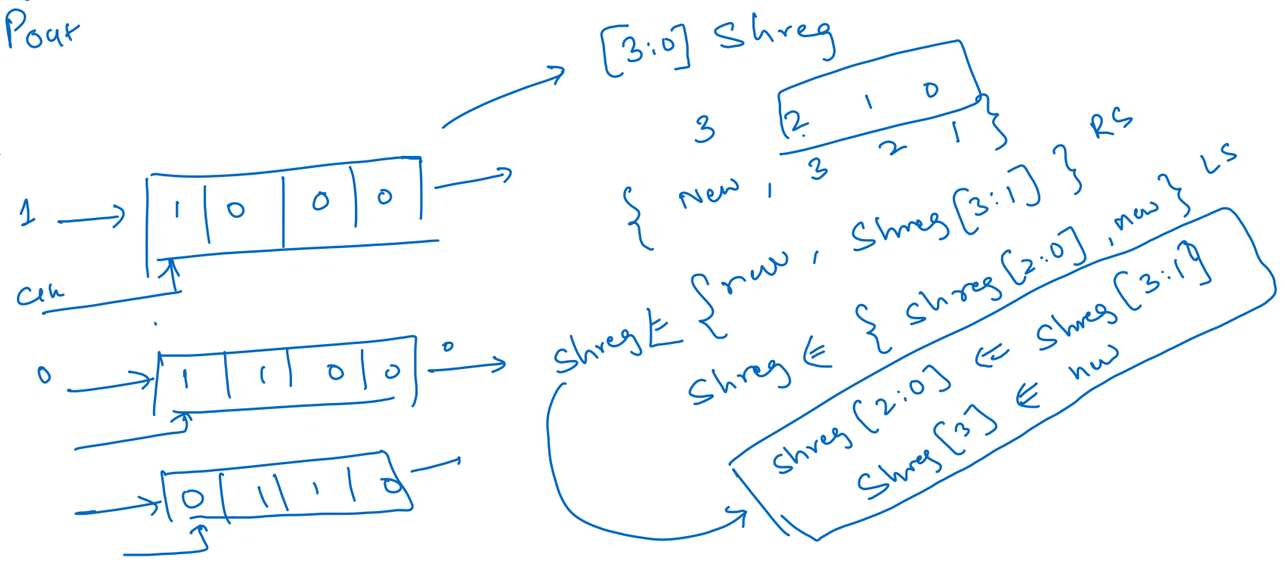
1. Modelling a shifter

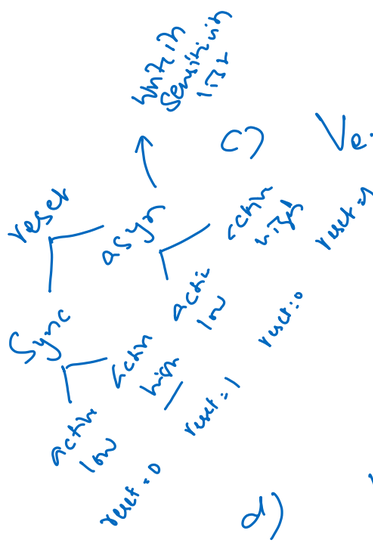
a) Requirements



b) Core Technique



c) Verilog design

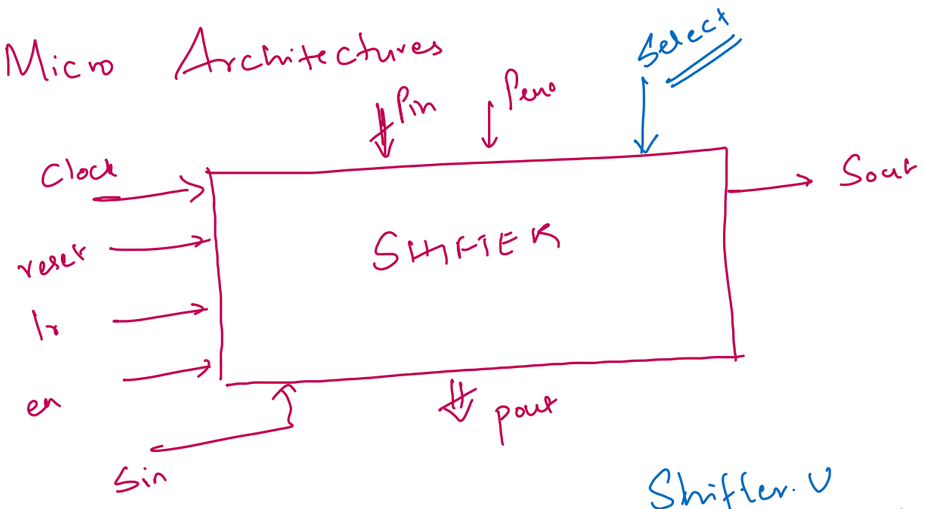


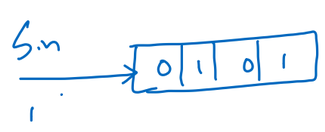
→ Asynchronous reset working in active low

→ Works on negative edge of clock

d) Verilog TB and test all cases

2. Creating Micro Architectures



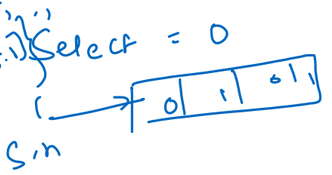


Select = 1

1 0 1 0
1 1 0 1
1 1 1 0
1 1 1 1

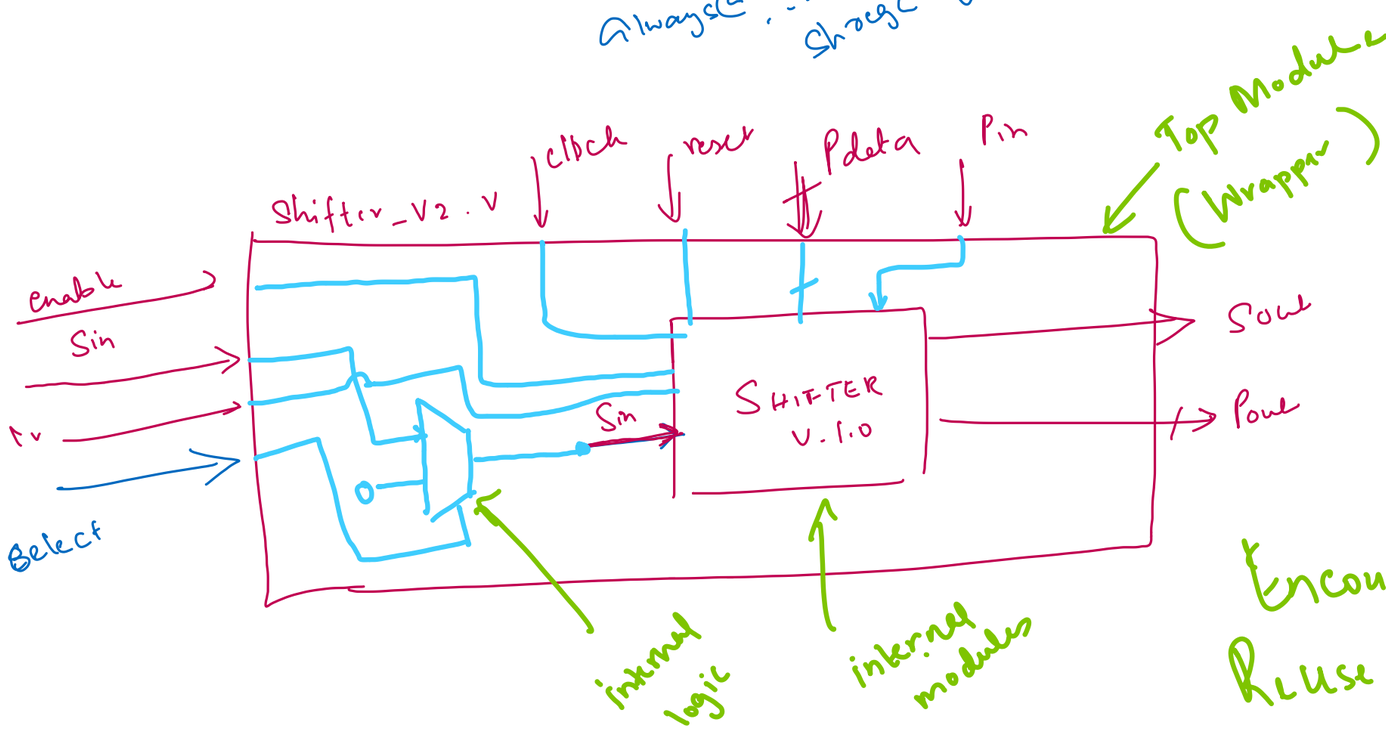
0010
0001
0000

Select = 0



Shifter.v

```
design data = Select ? Sin : 0 ;;
always@ ::
Shreg<= { data, Shreg[3:1]}
```



Encourages Reuse of existing modules