Purushotham Sannakariyappa
Principal Consultant
Mindful Learning India Ltd.
Bangalore – 560078, INDIA
Email: purushotham@mindfullearning.in
Phone: +91 7204004535

Mindful Learning

Invoice

Original for Recipient

Date: 18th July 2023

To,
ProBits Technologies Pvt Ltd.,
#77, Shankara, Concord Layout,
4 th Cross, RR Nagar, Bengaluru: 560098

Kind Attn: Mrs. Chaitra Dixit

Sub: Invoice – Invoice PROBITS-BLR-INV-ML000063 for Online Training for Quest Global

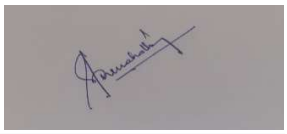
Dear Sir/Madam,

Please find the invoice for below mentioned training programs.

Item No	Particulars	Unit	QTY	Cost per hour (INR)	Total cost (INR)
1	Online FPGA Training for Quest Global 30 May 2023 – 7 July 2023	66 Hours		3000	198000
				Total	**198000**
Amount Payable in Words: INR One Lakh Ninety Eight Thousand Only **Purchase Order Number: PROPO-2324-010 Reference/ PT Number: PT-74 Dated: 15/May/2023** **Invoice Number: PROBITS-BLR-INV-ML000063**					
Payment	**One Lakh Ninety Eight Thousand INR Only before 30 Days from Invoice Date**				
Payment to be made	On or before 18th August 2023				

Trainer's Name	Purushotham S
PAN Number	BCKPS3244M
Service Tax Number	NA
GST Number	NA
Account Details	Bank: **HDFC Bank** Account Holder Name: **PURUSHOTHAM S** Account Number: **1226-114-0006466** IFS Code: HDFC0001226 Branch: **RVS Paradise, Jayanagar 4T Block, Bangalore - 560040** Account Type: **Savings**

Yours truly,



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Reference:

May-29-2023, Mon	09.00 am to 1.00 pm	4	VILT	Day 8	Introduction to VHDL	Mr Purusotham
May-30-2023, Tue	09.00 am to 1.00 pm	4	VILT	Day 9	Introduction to VHDL & Functional Verification using Verilog HDL	Mr Purusotham
May-31-2023, Wed	09.00 am to 1.00 pm	4	VILT	Day 10	Functional Verification using Verilog HDL	Mr Purusotham
Jun-01-2023, Thu	09.00 am to 1.00 pm	4	VILT	Day 11	FPGA Architecture	Mr Purusotham

Jun-19-2023, Mon	09.00 am to 1.00 pm	4	VILT	Day 12	FPGA Design Flow	Mr Purusotham
Jun-20-2023, Tue	09.00 am to 1.00 pm	2	VILT	Day 13	FPGA Design Flow & FPGA programming	Mr Purusotham
Jun-21-2023, Wed	09.00 am to 1.00 pm	4	VILT	Day 14	FPGA programming & IP Cores, Processors and Interfacing	Mr Purusotham
Jun-22-2023, Thu	09.00 am to 1.00 pm	4	VILT	Day 15	Project - Design of UART Transmitter and Receiver & IP Cores, Processors and Interfacing	Mr Purusotham
Jun-23-2023, Fri						
Jun-24-2023, Sat	NA				Weekly Holiday	
Jun-25-2023, Sun	NA				Weekly Holiday	
Jun-26-2023, Mon	09.00 am to 1.00 pm	4	VILT	Day 16	IP Cores, Processors and Interfacing	Mr Purusotham
Jun-27-2023, Tue	09.00 am to 1.00 pm	4	VILT	Day 17	Project - Using FIFO in UART design + Softcore processors	Mr Purusotham
Jun-28-2023, Wed	09.00 am to 1.00 pm	4	VILT	Day 18	Project - Implementing UART communication using Microblaze + Cross Clock Domains	Mr Purusotham
Jun-29-2023, Thu	09.00 am to 1.00 pm	4	VILT	Day 19	Cross Clock Domains	Mr Purusotham
Jun-30-2023, Fri						
Jul-01-2023, Sat	NA				Weekly Holiday	
Jul-02-2023, Sun	NA				Weekly Holiday	
Jul-03-2023, Mon	09.00 am to 1.00 pm	4	VILT	Day 20	Hard Core Processors and Interfacing	Mr Purusotham
Jul-04-2023, Tue	09.00 am to 1.00 pm	4	VILT	Day 21	Hard Core Processors and Interfacing	Mr Purusotham
Jul-05-2023, Wed	09.00 am to 1.00 pm	4	VILT	Day 22	Hard Core Processors and Interfacing	Mr Purusotham
Jul-06-2023, Thu	09.00 am to 1.00 pm	4	VILT	Day 23	Hard Core Processors and Interfacing	Mr Purusotham
Jul-07-2023, Fri	09.00 am to 11.00 pm	4	VILT	Day 24	Project - Store and retrieve UART data on DDR Memory	Mr Purusotham