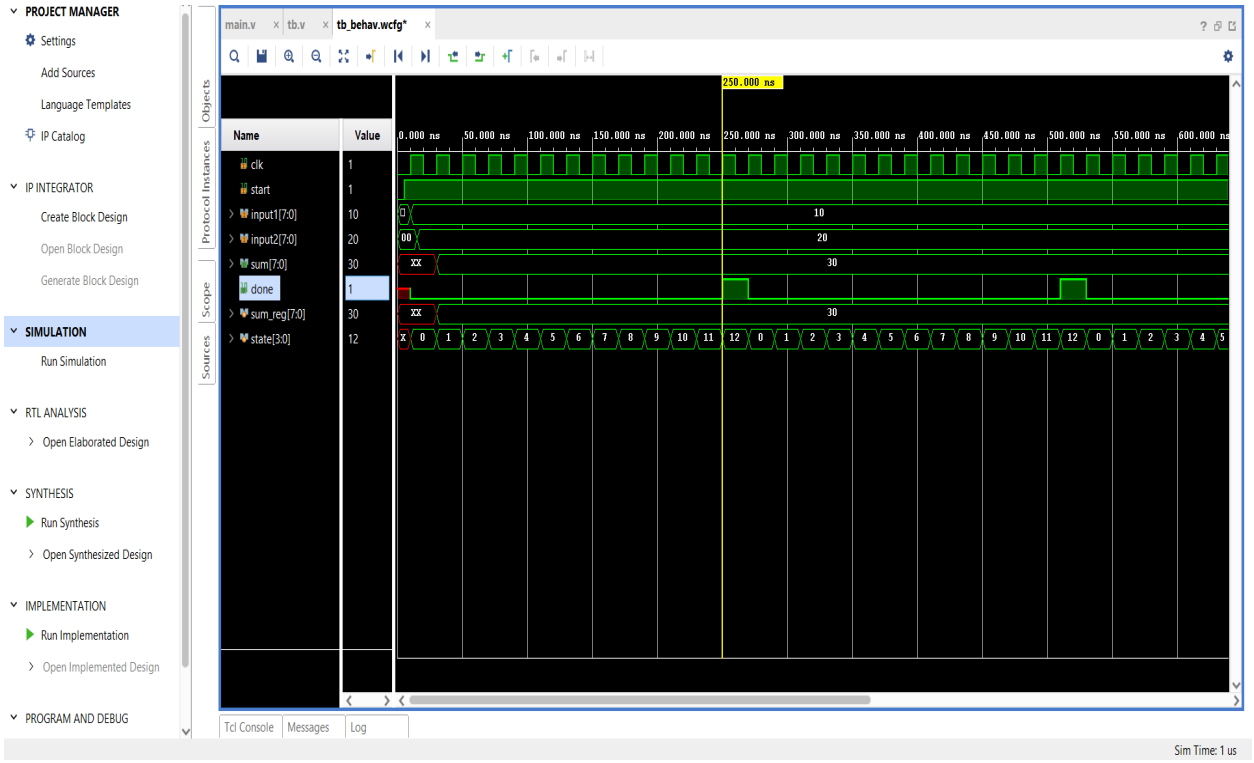
LAB 2

Case 1 : with only single adder

In 1 clock cycle -> load the values in Input 1 and Input 2
In 2 -11 clock cycle -> Adder takes 10 clock cycles thus represented by state machine with 10 states
In 12 clock cycle -> it will provide the output
Now based on this 1 pair of Inputs takes 12 cycles to process and provide output
Based on this for N=400 , it would take around **4800 cycles** to process and provide output .

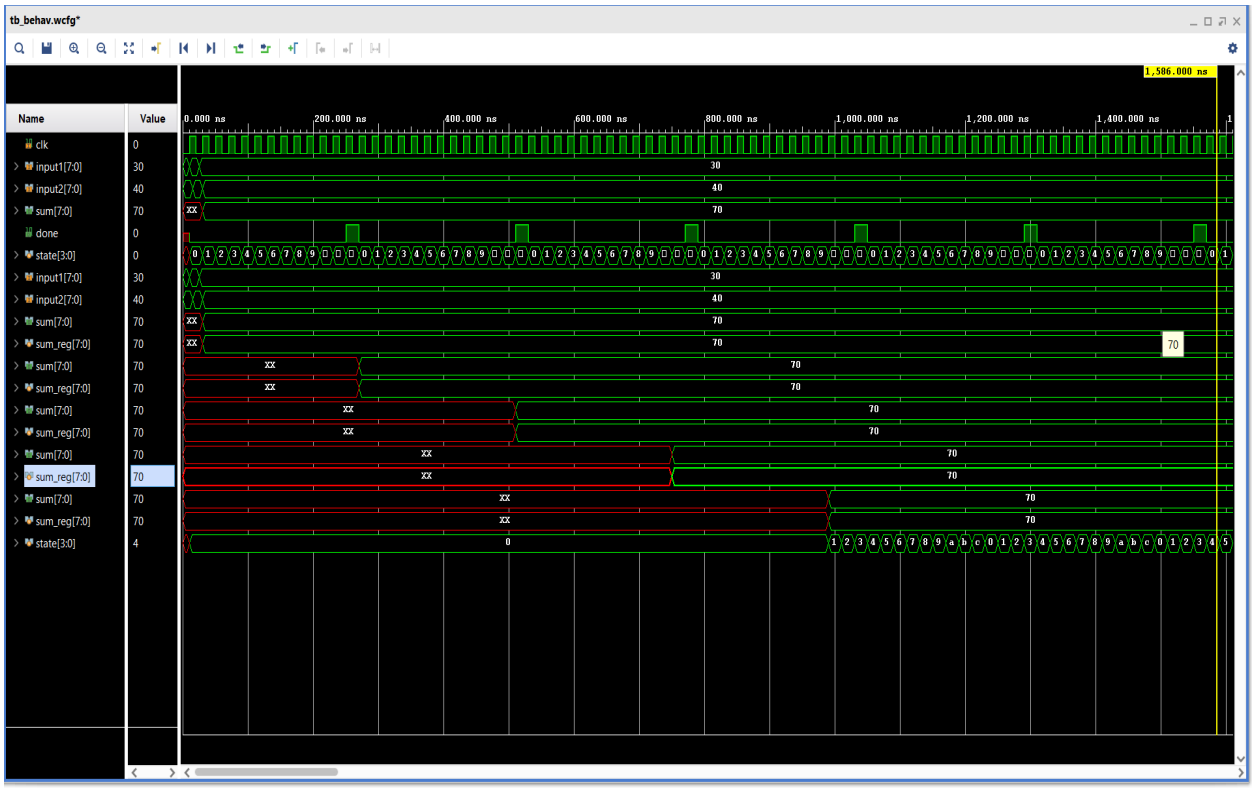


Simulation for 1 adder

Case 2 : with 5 adder in parallel in pipeline structure

Load Input 1 and Input 2 for Adder 1 -> (Cycle 1)
Load Input 1 and Input 2 for Adder 2 ->(Cycle 2)
Load Input 1 and Input 2 for Adder 3 ->(Cycle 3)
Load Input 1 and Input 2 for Adder 4 ->(Cycle 4)
Load Input 1 and Input 2 for Adder 5 ->(Cycle 5)
Adder 1 performs the addition -> (Cycles 2-11)
Adder 2 performs the addition -> (Cycles 3-12)
Adder 3 performs the addition -> (Cycles 4-13)
Adder 4 performs the addition -> (Cycles 5-14)
Adder 5 performs the addition ->(Cycles 6-15)

Output from Adder 1 available ->(Cycle 12)
Output from Adder 2 available -> (Cycle 13)
Output from Adder 3 available ->(Cycle 14)
Output from Adder 4 available -> (Cycle 15)
Output from Adder 5 available -> (Cycle 16)
Load Input 1 and Input 2 for Adder 1 ->(Cycle 17) and so on ..
SO based on this we get 16 cycles to get output from all the parallel 5 adders for 1 input pair each parllelly
Now in order to get for N=400
Total cycles required will be 16/5 *400
1280 cycles!



Simulation for 5 adder