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minimal Fab SOI-CMOS PDK

Minimal Fab PDK Authors

Oct. 17, 2023

Contents of minimal Fab SOI-CMOS PDK

- Documentation
  1. Device/Process Explanation
  2. Device Characteristics
  3. Design Manual
- Electrical Data
  1. SPICE Model
  2. PCELL
  3. DRC/LVS Rule

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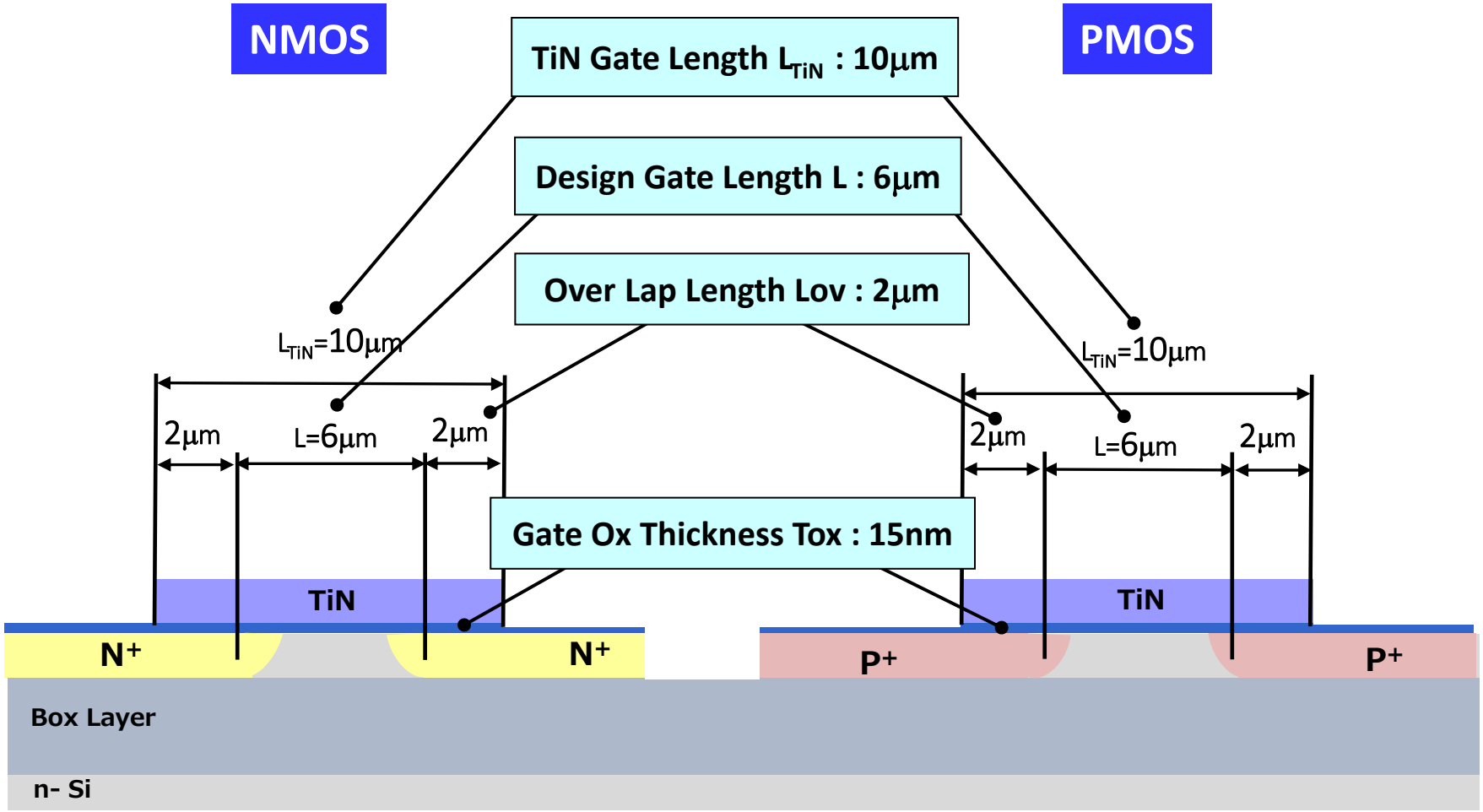
Cross-Sectional View of minimal Fab SOI-CMOS



Fabrication Process of SOI-CMOS
- Gate Last Formation -

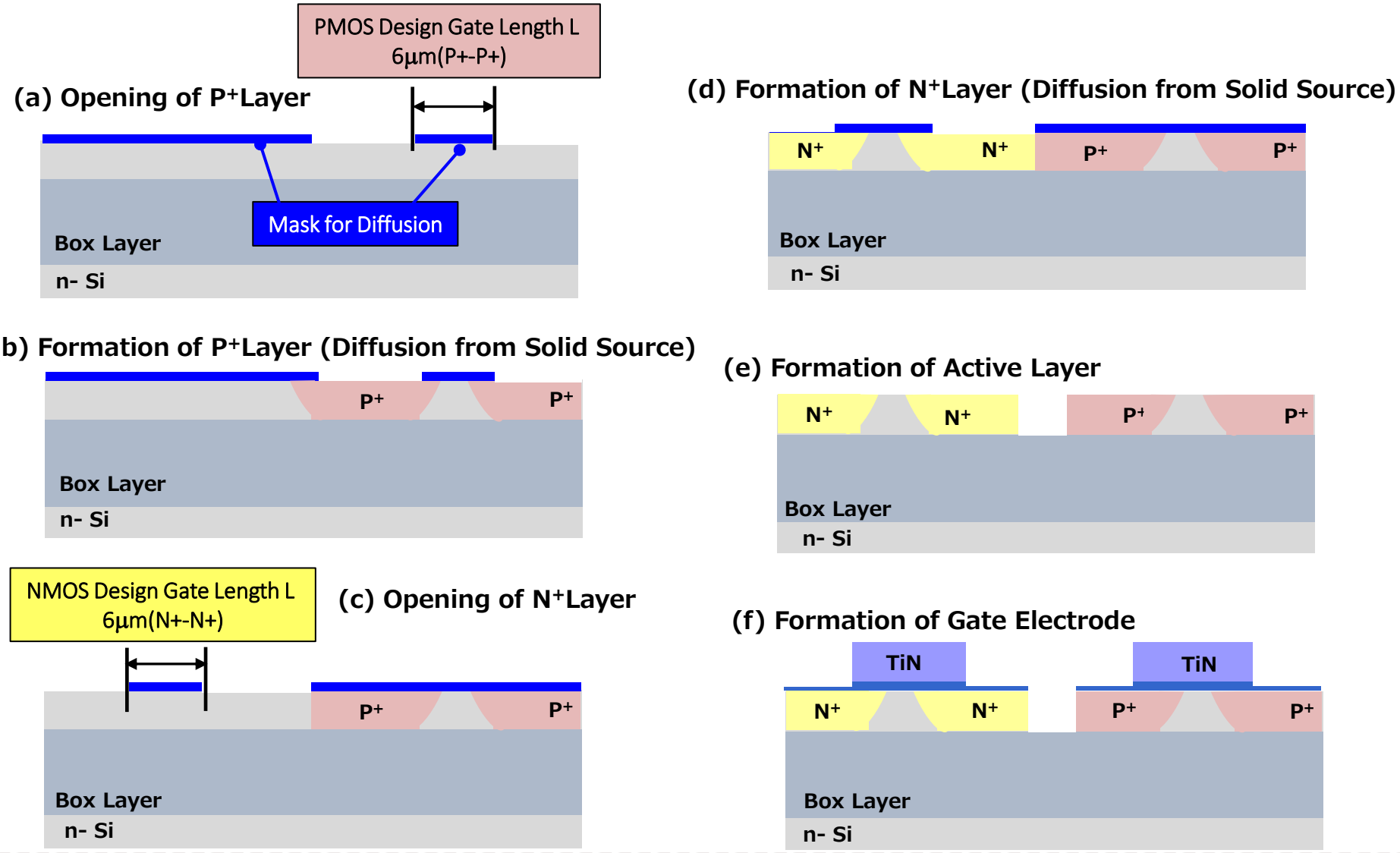


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Table of MOSFET Characteristics

Parameters	Dimensions	Bias	Typical Value	Units
NMOS				
Threshold Voltage	L/W=6/24	Vds=0.05V	0.25	V
Idsat	L/W=6/24	Vds=Vgs=3V	62.5	μA/μm
Subthreshold Slope	L/W=6/24		71	mV/dec
BVDSS	L/W=6/24		>7	V
PMOS				
Threshold Voltage	L/W=6/24	Vds=-0.05V	-0.71	V
Idsat	L/W=6/24	Vds=Vgs=-3V	12.9	μA/μm
Subthreshold Slope	L/W=6/24		65	mV/dec
BVDSS	L/W=6/24		>7	V

Ta=25℃

Table of Sheet & Contact Resistance

Parameters	Dimensions	Bias	Typical Value	Units
Sheet Resistance				
N+Diffusion	W/L=46.5μm/13μm	2V	180	Ω/sq
P+Diffusion	W/L=46.5μm/13μm	2V	1.2K	Ω/sq
TiN	W/L=46.5μm/13μm	2V	20	Ω/sq
Al	W/L=48μm/6μm	10mA	0.20	Ω/sq
Contact Resistance				
Al-N+	5μm×5μm	10mA	150	Ω
Al-P+	5μm×5μm	10mA	200	Ω
Al-TiN	5μm×5μm	10mA	0.9	Ω

Ta=25℃

Table of Gate Oxide

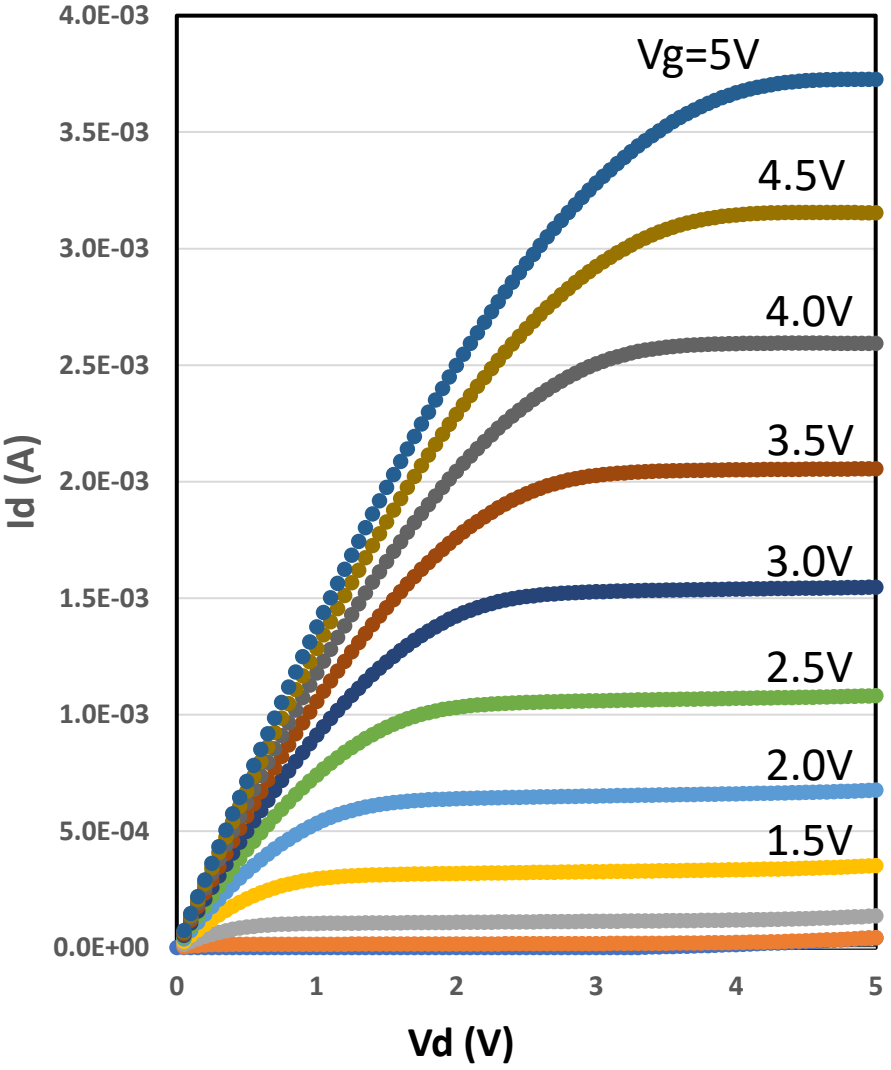
Parameters	Dimensions	Bias	Typical Value	Units
Cox	Gate N	2V	2.3	fF/μm2
Cox	Gate P	-2V	2.3	fF/μm2
BVox	Gate N		>12	V
BVox	Gate P		>-12	V

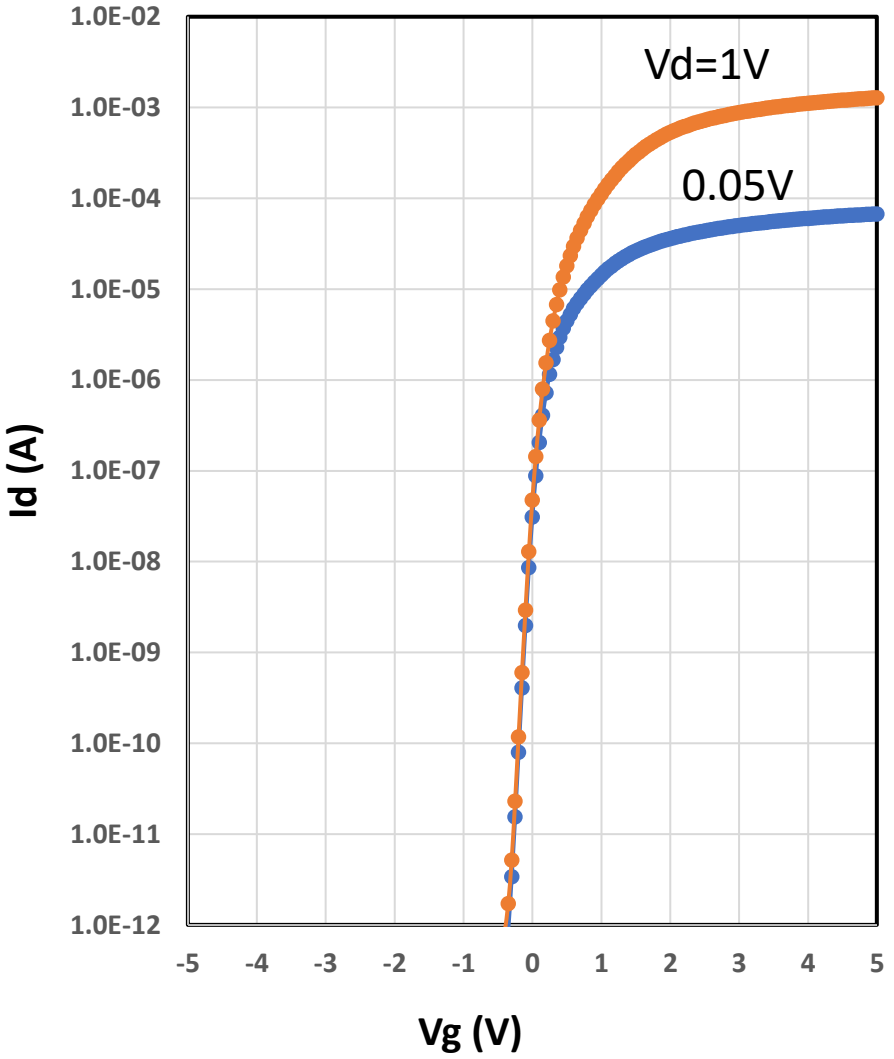
Table of MOSFET Capacitance

Parameters	Dimensions	Bias	Typical Value	Units
NFET Overlap Cap.	100μm × 100μm	2V	5	fF/μm
PFET Overlap Cap.	100μm × 100μm	-2V	6.8	fF/μm
NFET Diffusion Cap.	100μm × 100μm	2V	0.086	fF/μm2
PFET Diffusion Cap.	100μm × 100μm	-2V	0.086	fF/μm2

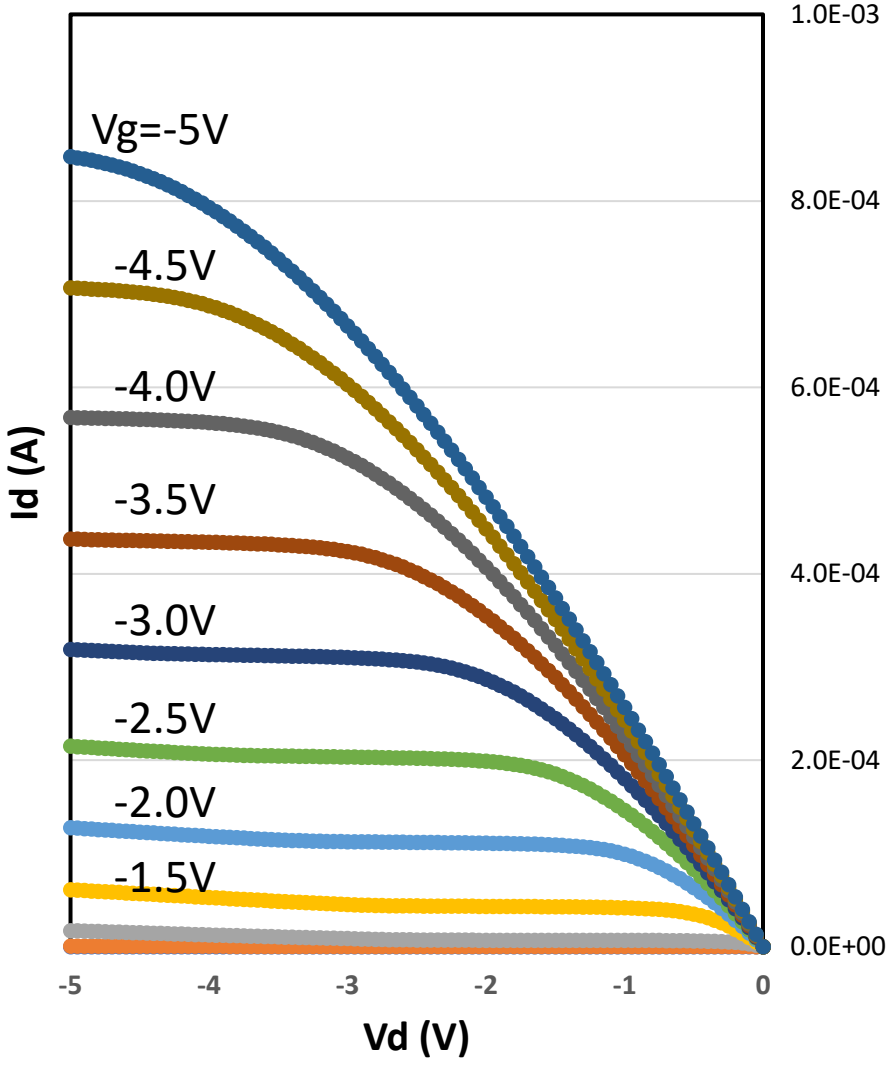
Ta=25℃

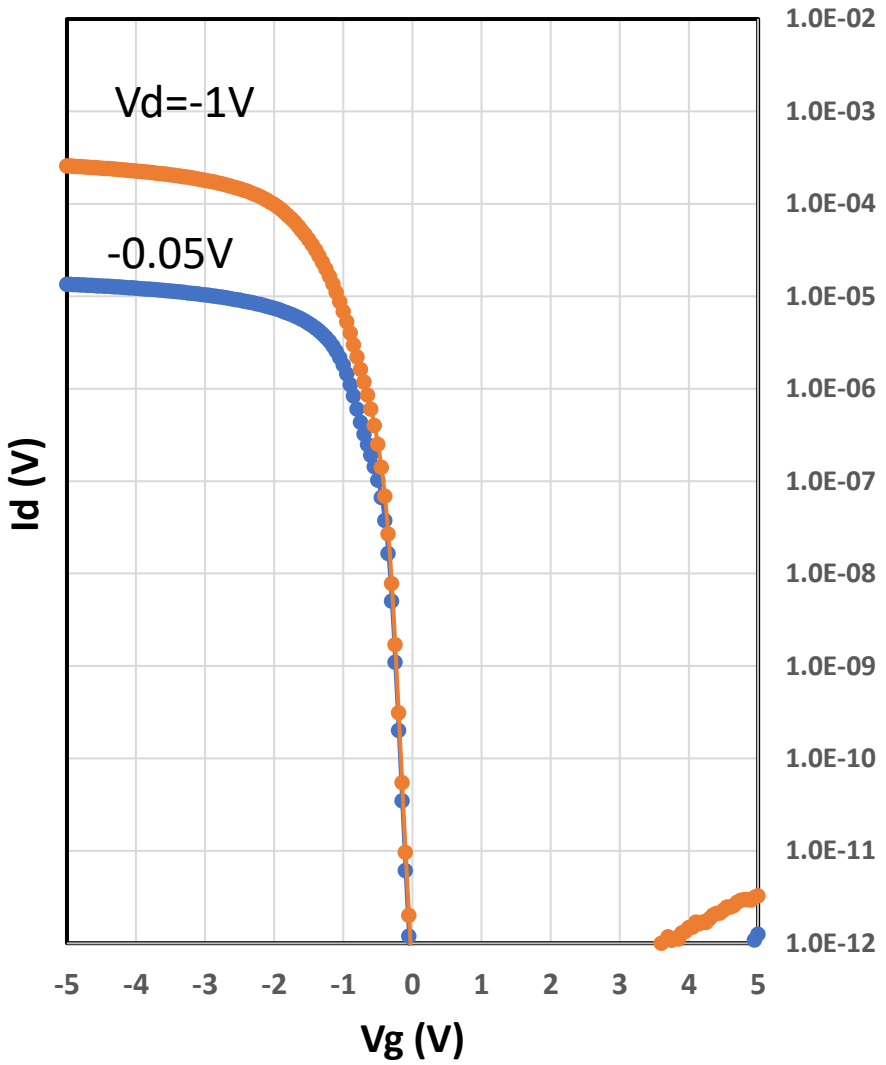
NFET VDID/VGID Characteristics (L/W=6μm/24μm)



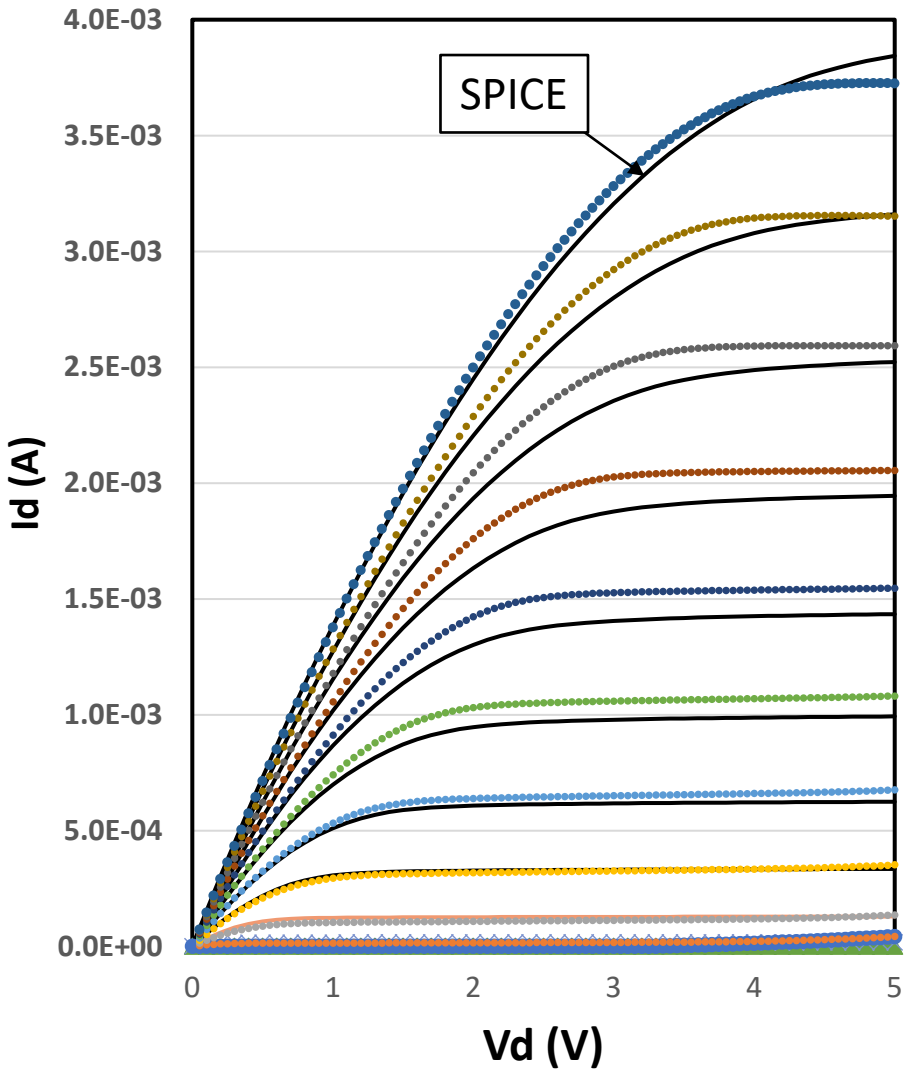


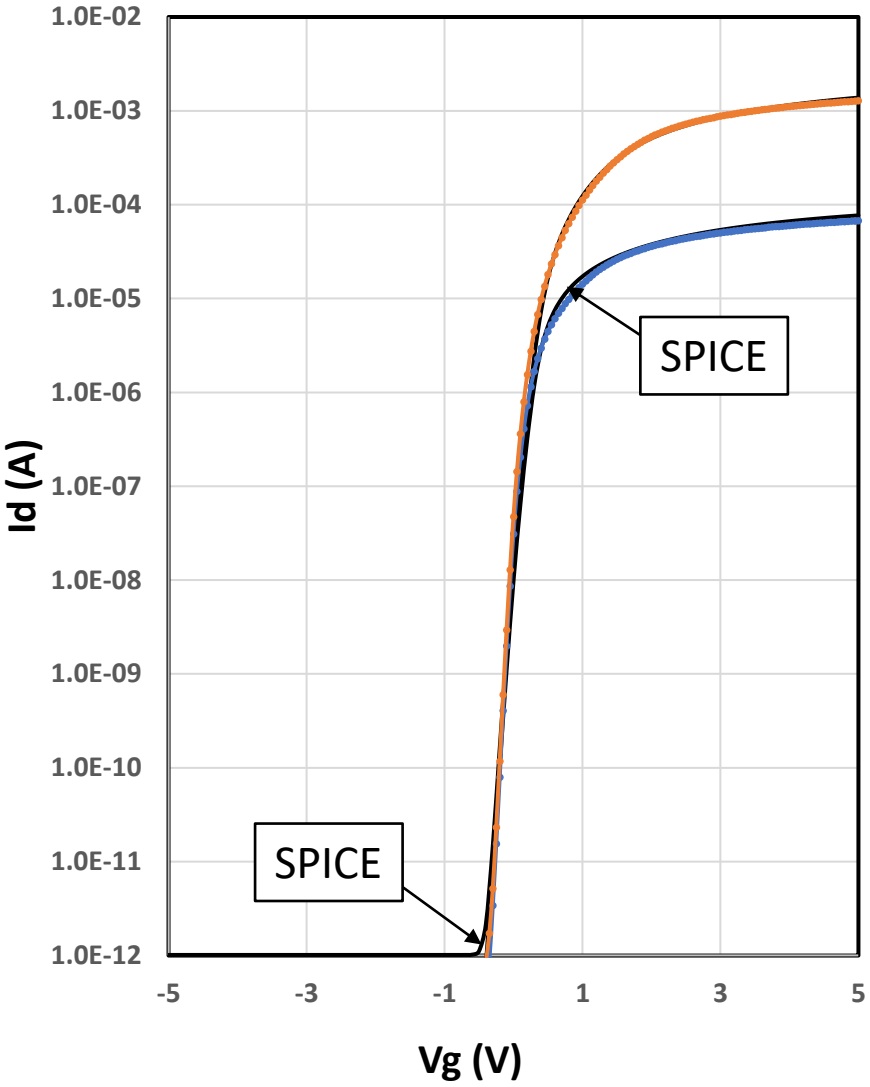
PFET VDID/VGID Characteristics (L/W=6μm/24μm)



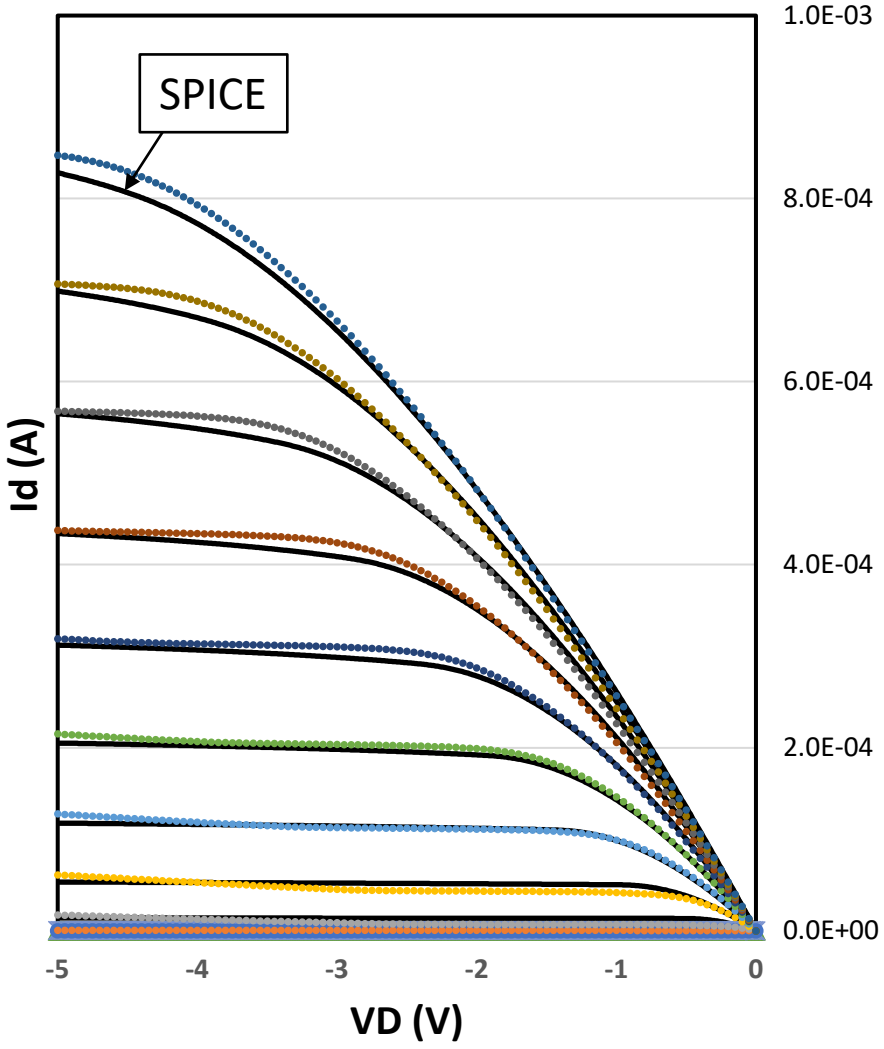


NFET VDID/VGID Characteristics (L/W=6μm/24μm) Measured vs SPICE Model





PFET VDID/VGID Characteristics (L/W=6μm/24μm) Measured vs SPICE Model



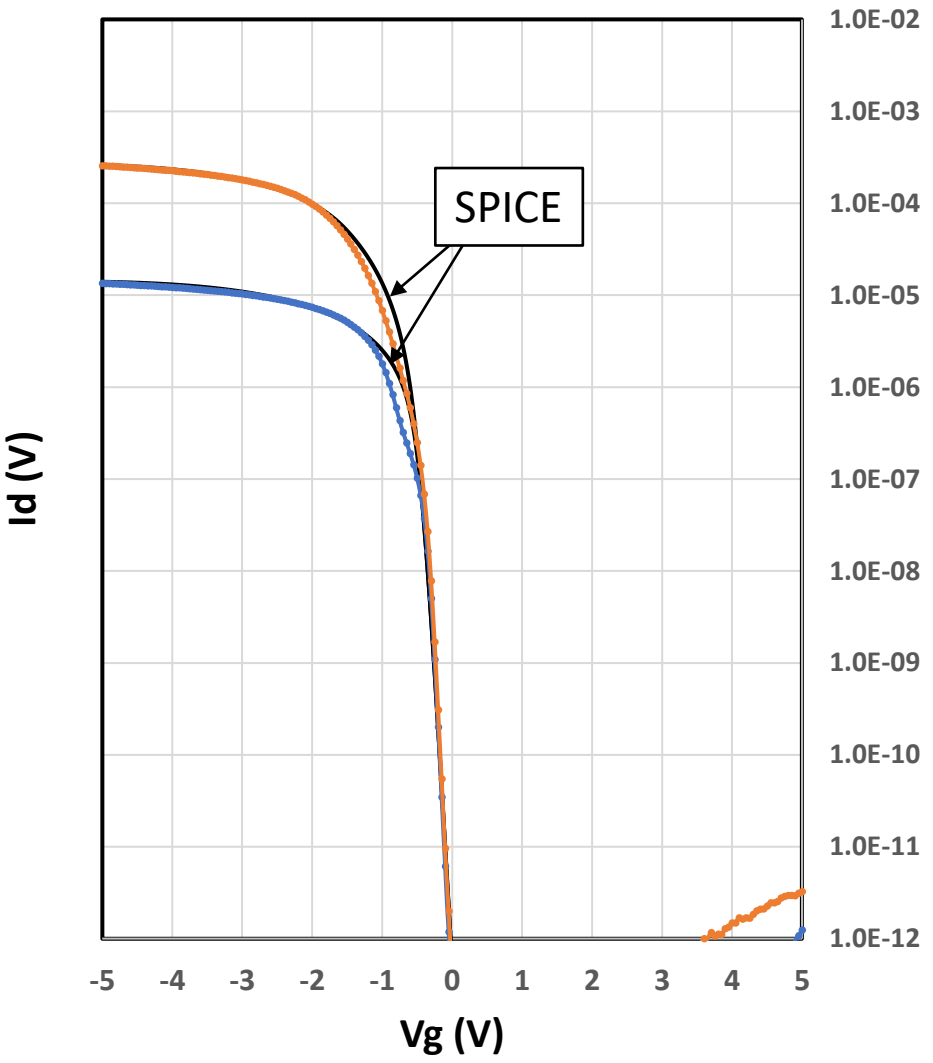


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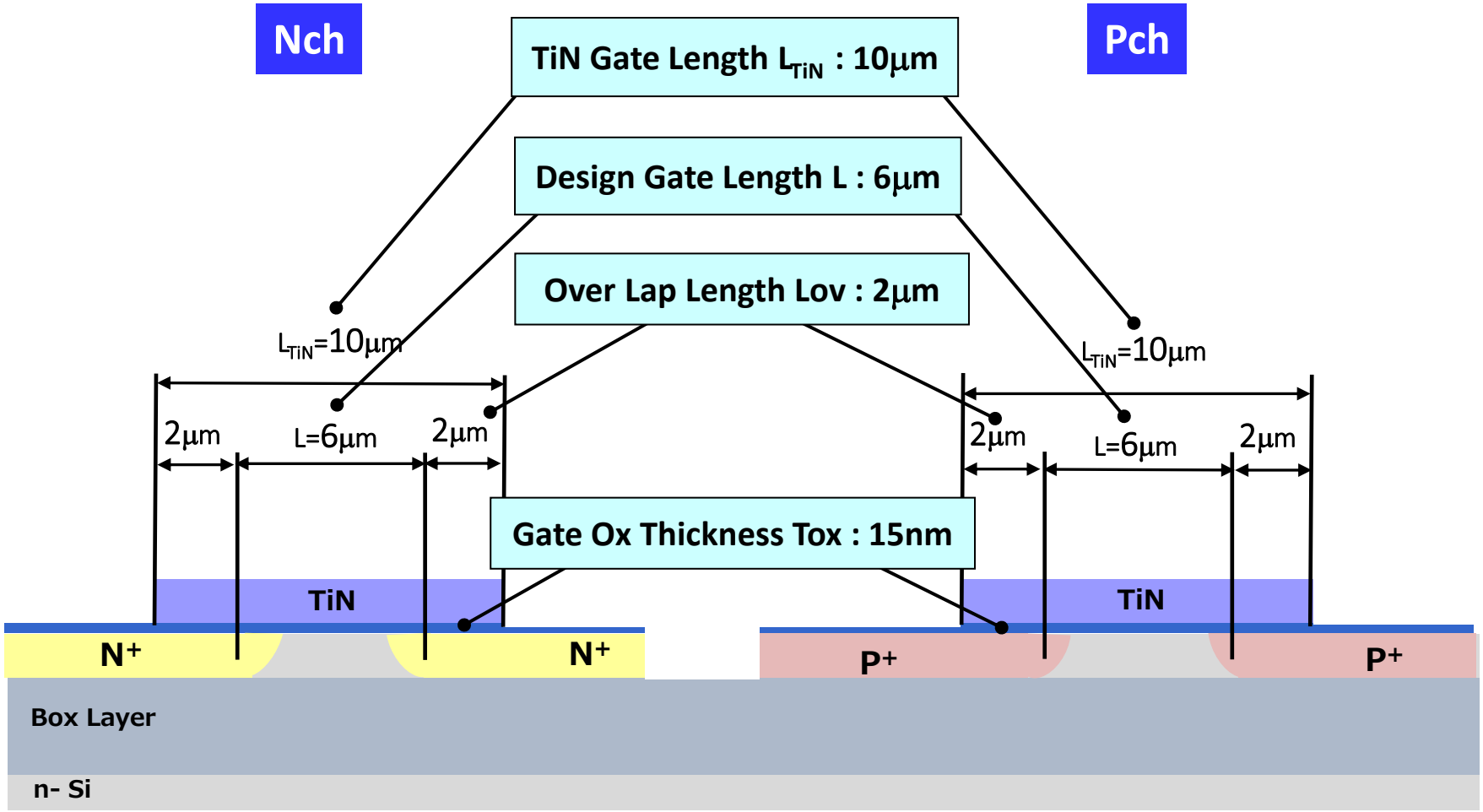
Table of Device List

Name	Symbol	L(μm)	W(μm)	Spice Model	Symbol of PCELL	Contents
NMOS	NMOS	6～40μm	13～40μm	MF_NMOS.txt	Nch	
PMOS	PMOS	6～40μm	13～40μm	MF_PMOS.txt	Pch	
Bridge	BR	25～100μm	10～20μm	MF_NMOS.txt	Bridge	TiN wiring for Local Bridge
Nbridge	NB	25～100μm	10～20μm	MF_NMOS.txt	Nbridge	N-Diffused Layer wiring for Local Bridge
Ndiff_cap	ND	25～100μm	25～100μm	MF_NMOS.txt	Ndiff_cap	Gate-N-Diffused Layer for Capacitor
Pdiff_cap	PD	25～100μm	25～100μm	MF_PMOS.txt	Pdiff_cap	Gate-P-Diffused Layer for Capacitor
R_ndiff	RN	25～100μm	10～20μm	MF_NMOS.txt	R_ndiff	N-Diffused layer for Resistance
R_pdiff	RP	25～100μm	10～20μm	MF_PMOS.txt	R_pdiff	P-Diffused layer for Resistance
TiN_cap	TI	25～100μm	25～100μm	MF_NMOS.txt	TiN_cap	Gate-Al Capacitor

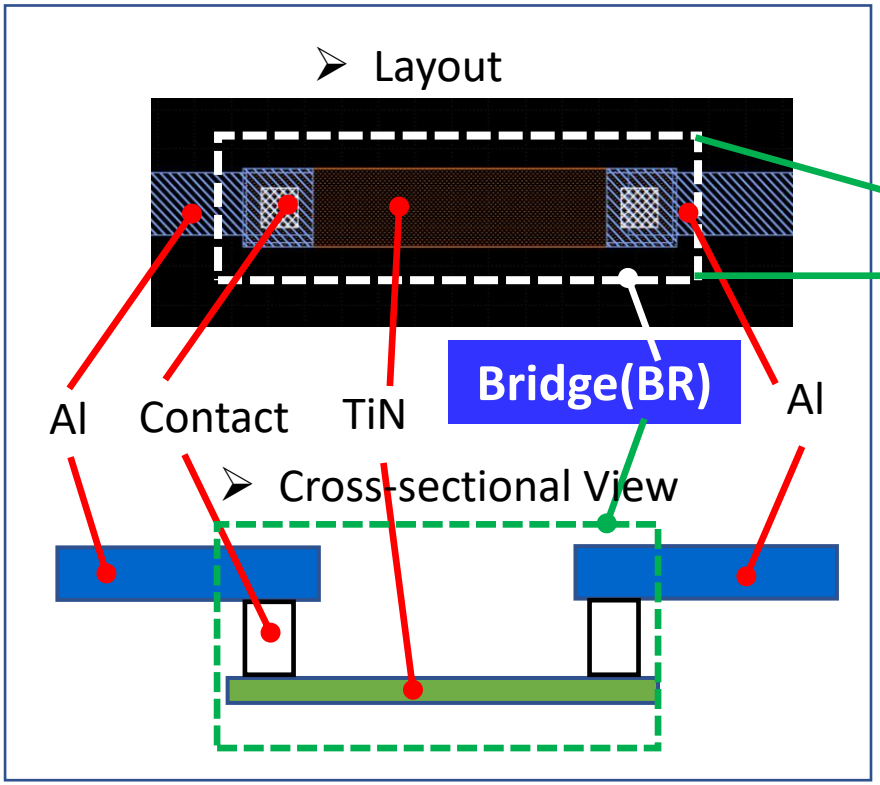
Cross-Sectional View of PCELL (1)

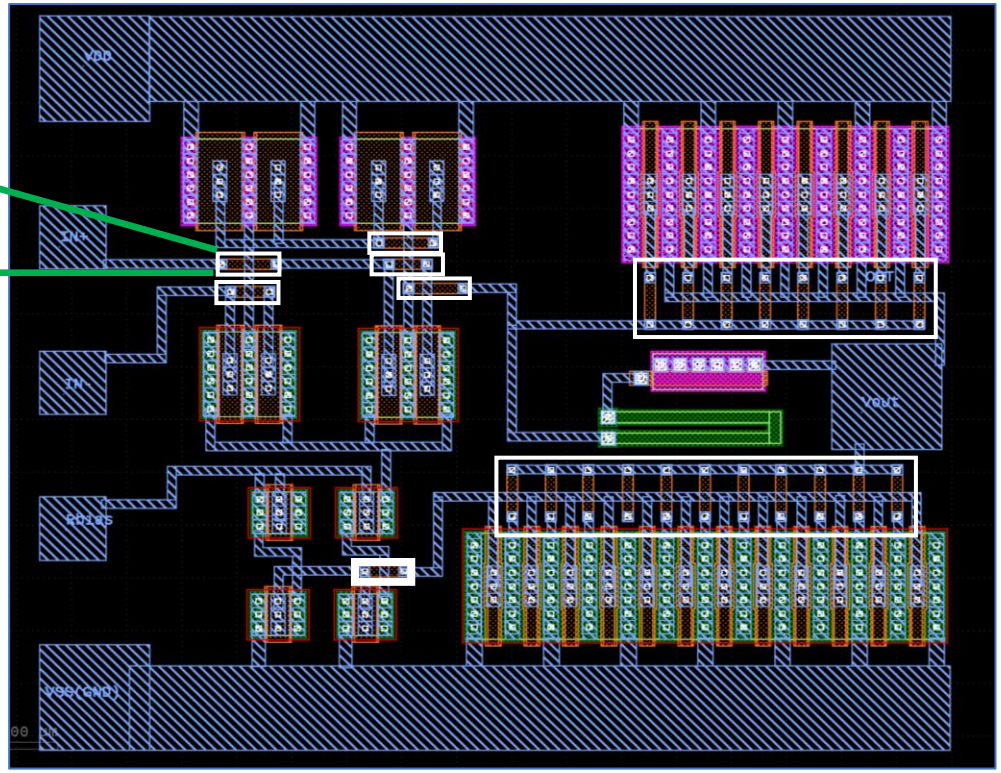


Cross-Sectional View of PCELL (2)

Bridge(BR) : Local wiring by TiN

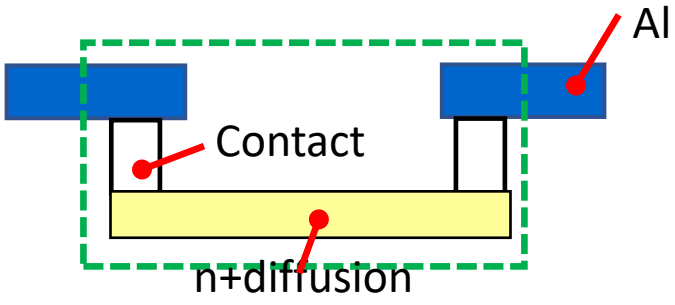
- Layout & Cross-sectional View
- Applied Circuit (OPamp)



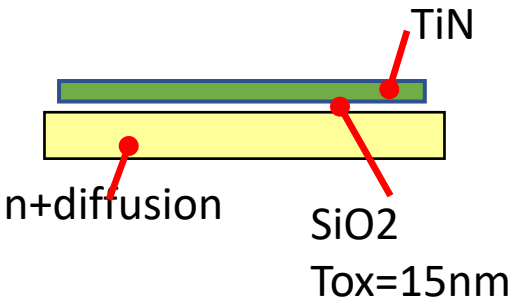


Cross-Sectional View of PCELL (3)

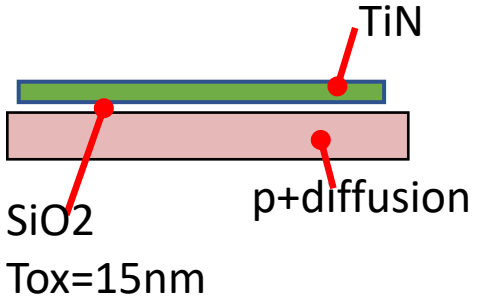
NBridge(NB) :
Local wiring by n+



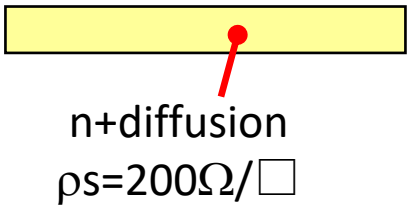
Ndiff_cap(ND) :
Capacitor btw TiN & n+



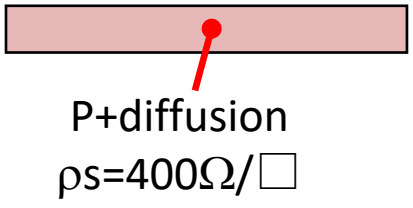
Pdiff_cap(PD) :
Capacitor btw TiN & p+



R_ndiff(RN) :
Resistance by n+



R_pdiff(RP) :
Resistance by p+



TiN_cap(TI) :
Capacitor btw Al & TiN

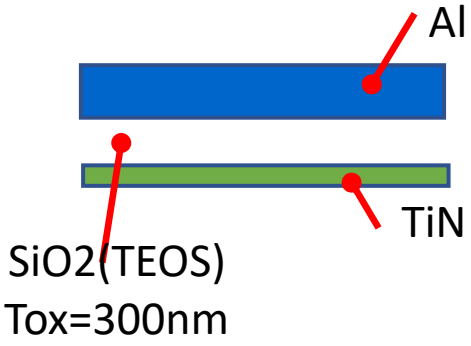
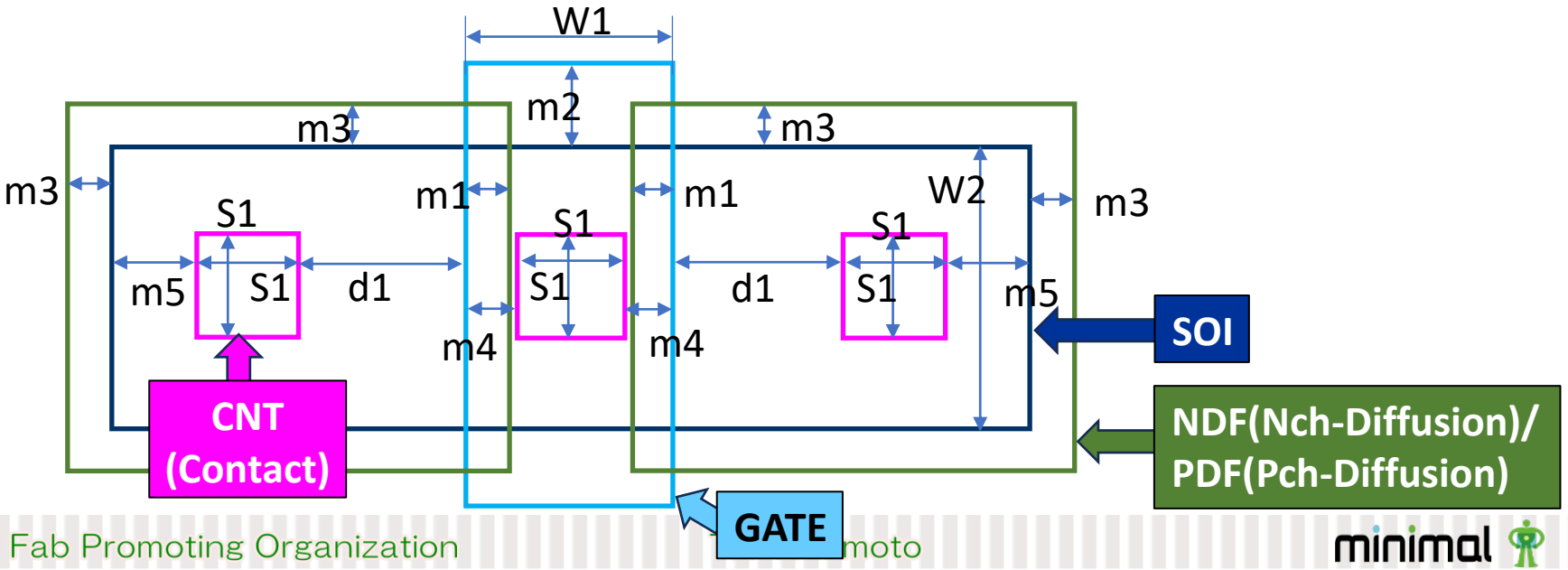


Table of Drawn Layers for Each Device

Drawn Layer Name	GDS Layer No.	Data W/B	Used Layer									Contents
			NMOS	PMOS	BR	NB	ND	PD	RN	RP	TI	
Alignment Mark	1	W										
N-channel	13	W	○									Channel doping of NMOS
P-Diff (PDF)	2	W		○				○		○		Source/Drain doping of PMOS
N-Diff (NDF)	3	W	○			○	○		○			Source/Drain doping of NMOS
SOI	4	B	○	○		○	○	○	○	○		Active Layer (Silicon Island
TiN-Gate	5	B	○	○	○						○	Gate
Contact (CNT)	6	W	○	○	○	○	○	○	○	○	○	Source/Drain/Gate Contact
Al	7	B	○	○	○	○	○	○	○	○	○	Al wiring

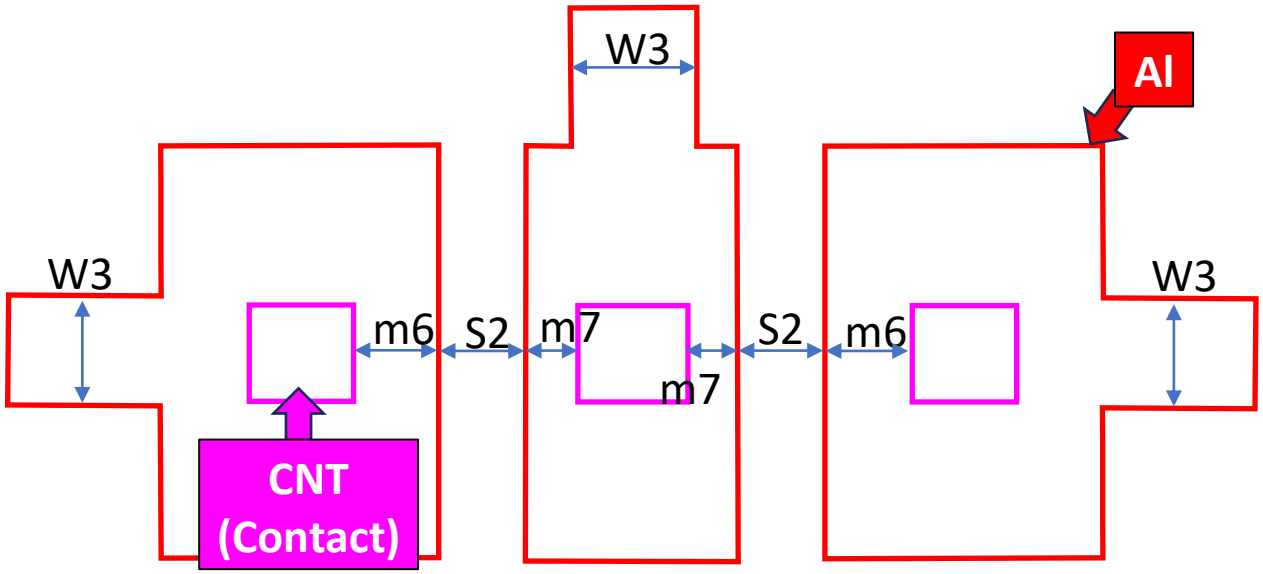
Layout Rule (1) : Device Layer

Description	Symbol	Layout Rule (μm)
TiN Minimum Gate Width	W1	10
SOI Minimum Width	W2	13
CNT Size	S1	5
TiN-NDF(or PDF) Overlap	m1	2
TiN Minimum Fringe	m2	4
SOI-NDF(or PDF) Minimum Enclosure	m3	2
Gate TiN-CNT Distance	d1	8
Gate TiN-CNT Minimum Enclosure	m4	2.5
SOI-CNT Minimum Enclosure	m5	4



Layout Rule (2) : Wiring Layer

Description	Symbol	Layout Rule (μm)
Al Minimum Width	W3	6
Al Minimum Space	S2	4
Al-CNT Minimum Enclosure	m6	4
Al-Gate CNT Minimum Enclosure	m7	2.5
TiN Minimum Width		6
TiN Minimum Space		6
SOI Minimum Width		6
SOI Minimum Space		4



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