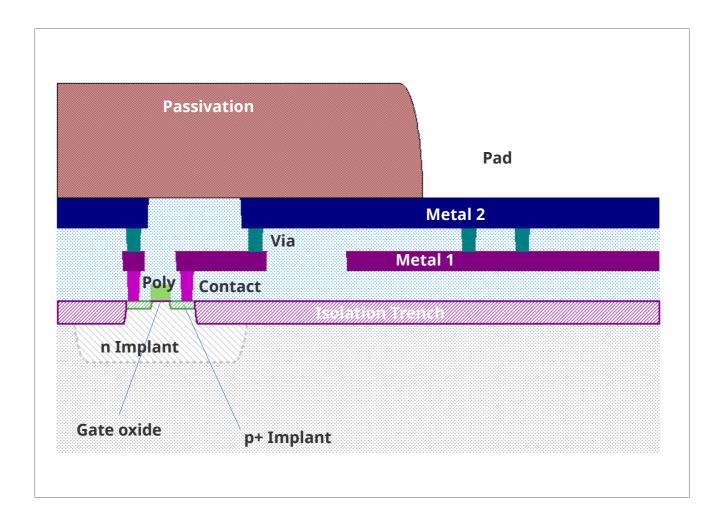
SILICON4ALL INC.

Design Manual

Process NCC-1701 Version 1.0

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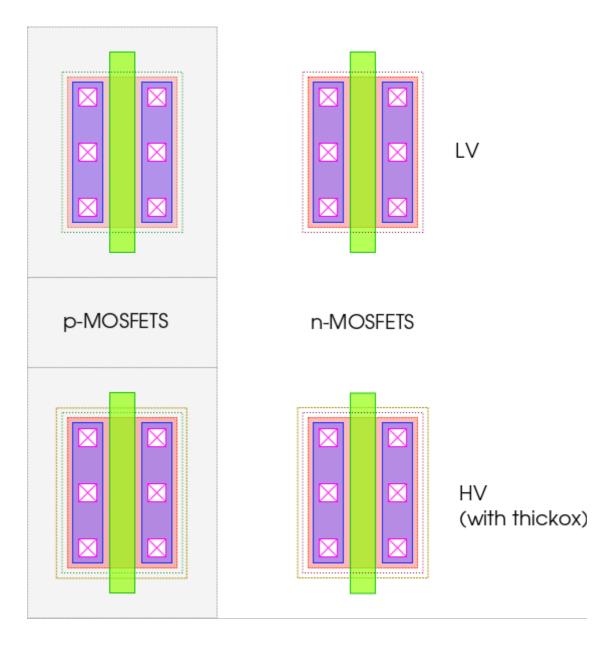
Process Description

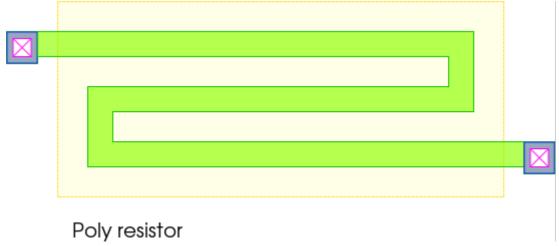


Drawing Layers

GDS Layer Number	Layer Name	Comment
1	nwell	n implant (well)
2	diff	Diffusion (active area)
3	pplus	p+ implant marker
4	nplus	n+ implant marker
5	poly	Polysilicon
6	thickox	Thick oxide marker for high-Vt transistors
7	polyres	High resistance polysilicon marker for poly resistors
8	contact	Polysilicon or diffusion contact
9	metal1	First metal
10	via	Via between first and second metal
11	metal2	Second metal
12	pad	Pad opening
13	border	Drawing boundary

Devices





Design Rules

Naming Scheme

Rule name	Description	Example
x_A	Min area of X	$w^*h \ge A$
x_W	Min width of layer X	≥ W
x_S	Min space of layer X	≥ S ≥ S ≥ S
x_y_S	Min separation of layer X to Y	X
x_y_O	Min enclosure of Y in X	X Y ≥ O
x_X	Special rules	

Detailed Rules

Rule Name	Measurement	Condition	Description of error		
CONT_S	contact space (square metric)	≥ 360 nm	contact space < 360 nm		
		No other contact in this area 360 nm			
CONT_W	contact width	180 nm	contact width != 180 nm		
CONT_X	contact is either inside poly or inside diff (but outside poly)		invalid contact		
	diff poly Invalid contacts				
DIFF_A	diff area	$\geq 0.5 \ \mu m^2$	diff area < 0.5 μm²		
DIFF_CONT_O	diffusion area to diffusion contact overlap	≥ 110 nm	diff to contact overlap < 110 nm		
DIFF_GATE_O	diff overlap over poly	≥ 420 nm	diff to poly overlap < 420 nm		
DIFF_NPLUS_X	diff is either inside or outside nplus, never crossing		Invalid nplus		

	nplus	Invalid diff	
DIFF_NWELL_S	diff to nwell distance	≥ 300 nm	diff to nwell distance < 300 nm
DIFF_NWELL_X	diff either inside or outside nwell, never crossing		diff crossing nwell boundary
	See DIFF_NPLUS_	_X	
DIFF_POLY_S	diff to non-gate poly distance	≥ 100 nm	diff to poly distance < 100 nm
DIFF_PPLUS_X	diff is either inside or outside pplus, never crossing		Invalid pplus
	See DIFF_PPLUS_X		
DIFF_S	diff space	≥ 600 nm	diff space < 600 nm
DIFF_W	diff width	≥ 500 nm	diff width < 500 nm
METAL1_CONT_O	metal1 to contact overlap	≥ 60 nm	metal1 to contact overlap
METAL1_CONT_X	No contact without metal1		contact outside metal1
	metal	Invalid contacts	
METAL1_S	metal1 space	≥ 300 nm	metal1 space < 300 nm
METAL1_VIA_O	metal1 to via overlap	≥ 50 nm	metal1 to via overlap
METAL1_VIA_X	No via without metal1		via outside metal1
	See METAL1_CONT_X		
METAL1_W	metal1 width	≥ 300 nm	metal1 width < 300 nm
METAL1_X	metal1 density	≥ 20% , ≤ 80%	metal1 density < 20%

		I		
			metal1 density > 80%	
METAL2_PAD_O	metal2 to pad overlap	≥ 2 µm	metal2 to pad overlap < 2 μm	
METAL2_PAD_X	No pad without metal2		pad outside metal2	
	See METAL1_CON	See METAL1_CONT_X		
METAL2_S	metal2 space	≥ 500 nm	metal2 space < 500 nm	
METAL2_SW	metal2 space if at least one opponent is wide metal with width $\geq 3 \mu m$	≥ 700 nm	metal2 space < 700 nm for wide metal2 (≥ 3 μm)	
METAL2_VIA_O	metal2 to via overlap	≥ 100 nm	metal2 to via overlap < 100 nm	
METAL2_VIA_X	No via without metal2		via outside metal2	
	See METAL1_CON	NT_X		
METAL2_W	metal2 width	≥ 400 nm	metal2 width < 400 nm	
NWELL_A	nwell area	$\geq 2 \ \mu m^2$	nwell area < 2 μm²	
NWELL_DIFF_O	nwell to diff overlap	≥ 400 nm	nwell to diff overlap < 400 nm	
NWELL_S	nwell space (projected)	≥ 1 µm	nwell space < 1 μm	
NWELL_W	nwell width	≥ 1.2 µm	nwell width < 1.2 μm	
PAD_S	pad space	≥ 10 µm	pad space < 10 μm	
PAD_W	pad width	≥ 10 µm	pad width < 10 μm	
POLY_CONT_O	poly area to poly contact overlap	≥ 60 nm	poly to contact overlap < 60 nm	
POLY_CONT_S	poly to diff contact distance	≥ 130 nm	poly to contact distance < 130 nm	
POLY_S	poly space	≥ 300 nm	poly space < 300 nm	
POLY_W	poly width	≥ 250 nm	poly width < 250 nm	
POLY_X1	poly edge length	≥ 70 nm	poly edges with length < 70 nm	
			≥ 70 nm	

POLY_X2	poly extension over diff	≥ 250 nm	poly extension over gate < 250 nm
		diff	≥ 250 nm ≥ 250 nm
POLYRES_POLY_O	polyres to poly overlap	≥ 300 nm	polyres to poly overlap < 300 nm
POLYRES_X	diff is not allowed under polyres		diff not allowed in polyres
VIA_S	via space	≥ 250 nm	via space < 250 nm
VIA_W	via width	200 nm	via width != 200 nm

Other rules

Rule Name	Measurement	Condition	Description
MANHATTAN	Angles of edges	0° or 90°	Manhattan geometry only
GRID	Design grid	5 nm	All geometry is on-grid on a 5 nm grid
GATE_WELLFORMED			Gate areas must be rectangular Gates must entirely cover the diff area
INSIDE_BORDER			All drawing must be inside border