

512K x 8 HIGH-SPEED CMOS STATIC RAM

MARCH2008

FEATURES

HIGH SPEED: (IS61/64C5128AL)

- High-speed access time: 10ns, 12 ns
- Low Active Power: 150 mW (typical)
- Low Standby Power: 10 mW (typical) CMOS standby

LOW POWER: (IS61/64C5128AS)

- · High-speed access time: 25ns
- Low Active Power: 75 mW (typical)
- Low Standby Power: 1 mW (typical) CMOS standby
- TTL compatible interface levels
- Single 5V ± 10% power supply
- Fully static operation: no clock or refresh required
- Available in 36-pin SOJ (400-mil), 32-pin sTSOP-I, 32-pin SOP, 44-pin TSOP-II and 32pin TSOP-II packages
- Commercial, Industrial and Automotive temperature ranges available
- Lead-free available

DESCRIPTION

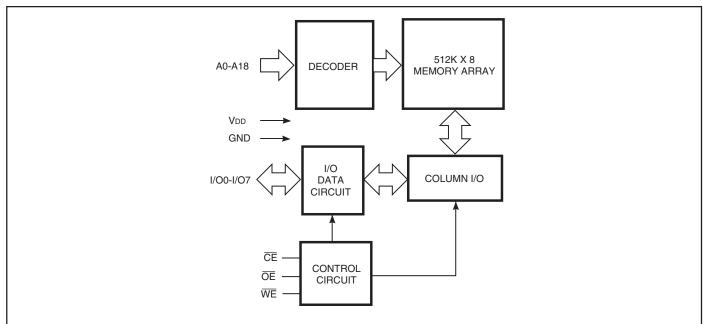
The *ISSI* IS61C5128AL/AS and IS64C5128AL/AS are high-speed, 4,194,304-bit static RAMs organized as 524,288 words by 8 bits. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns with low power consumption.

When $\overline{\text{CE}}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{\textbf{CE}}$ and $\overline{\textbf{OE}}$. The active LOW Write Enable ($\overline{\textbf{WE}}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{\textbf{UB}}$) and Lower Byte ($\overline{\textbf{LB}}$) access.

The IS61C5128AL/AS and IS64C5128AL/AS are packaged in the JEDEC standard 36-pin SOJ (400-mil), 32-pin sTSOP-I, 32-pin SOP, 44-pin TSOP-II and 32-pin TSOP-II packages

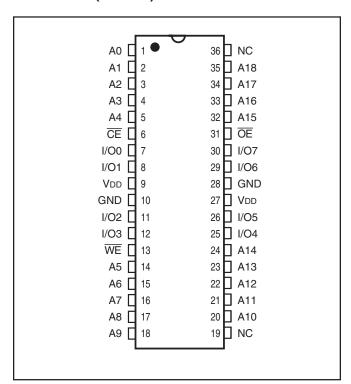
FUNCTIONAL BLOCK DIAGRAM



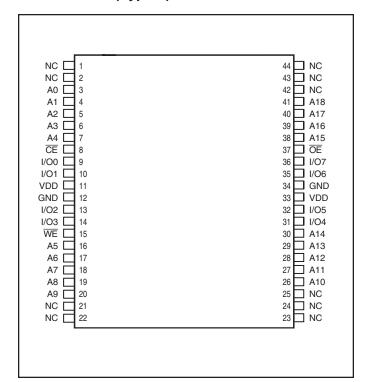


HIGH SPEED (IS61/64C5128AL) PIN CONFIGURATION

36-Pin SOJ (400-mil)



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A18	Address Inputs			
CE	Chip Enable Input			
ŌĒ	Output Enable Input			
WE	Write Enable Input			
I/O0-I/O7	Bidirectional Ports			
VDD	Power			
GND	Ground			
NC	No Connection			

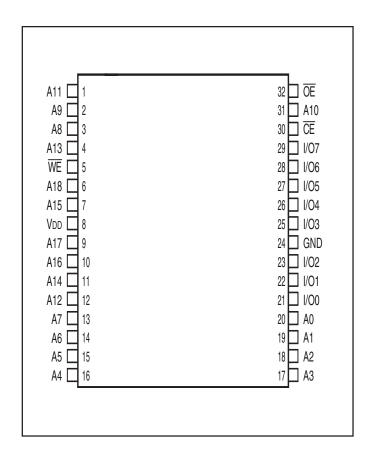


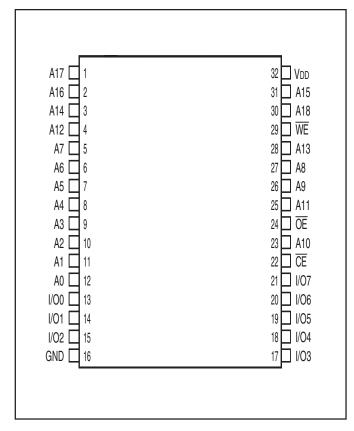


LOW POWER (IS61/64C5128AS) PIN CONFIGURATION

32-pin sTSOP (TYPE I)

32-pin SOP 32-pin TSOP (TYPE II)





PIN DESCRIPTIONS

A0-A18	Address Inputs
CE	Chip Enable 1 Input
ŌĒ	Output Enable Input
WE	Write Enable Input
1/00-1/07	Input/Output
VDD	Power
GND	Ground

IS64C5128AL/AS



TRUTH TABLE

					I/O PIN
Mode	WE	Œ	ŌĒ	I/O0-I/O7	V _{DD} Current
Not Selected	Х	Н	Х	High-Z	ISB1, ISB2
Output Disabled	Н	L	Н	High-Z	lcc1, lcc2
Read	Н	L	L	Dоит	lcc1, lcc2
Write	L	L	Х	DIN	lcc1, lcc2

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit	
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V	
Тѕтс	Storage Temperature	-65 to +150	°C	
Рт	Power Dissipation	1.5	W	
Іоит	DC Output Current (LOW)	20	mA	

Notes:

 Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
Соит	Output Capacitance	Vout = 0V	7	pF

Notes:

- 1. Tested initially and after any design or process changes that may affect these parameters.
- 2. Test conditions: $TA = 25^{\circ}C$, f = 1 MHz, VDD = 5.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
Vон	Output HIGH Voltage	$V_{DD} = Min., IoH = -4.0 mA$		2.4	_	V
Vol	Output LOW Voltage	VDD = Min., IOL = 8.0 mA			0.4	V
VIH	Input HIGH Voltage			2.2	V _{DD} + 0.5	V
VIL	Input LOW Voltage(1)			-0.3	0.8	V
ILI	Input Leakage	$GND \leq V IN \leq V DD$	Com.	-1	1	μΑ
			Ind.	-2	2	
			Auto.	- 5	5	
ILO	Output Leakage	GND ≤ Vout ≤ Vdd	Com.	-1	1	μA
		Outputs Disabled	Ind.	- 2	2	·
		-	Auto.	- 5	5	

Note: 1. $V_{IL} = -3.0V$ for pulse width less than 10 ns.





OPERATING RANGE: HIGH SPEED OPTION (IS61/64C5128AL)

Range	Ambient Temperature	V DD	Speed (ns)	
Commercial	0°C to +70°C	5V ± 10%	10	
Industrial	-40°C to +85°C	5V ± 10%	10	
Automotive	-40°C to +125°C	5V ± 10%	12	

OPERATING RANGE: LOW POWER OPTION (IS61/64C5128AS)

Range	Ambient Temperature	V _{DD}	Speed (ns)	
Commercial	0°C to +70°C	5V ± 10%	25	
Industrial	-40°C to +85°C	5V ± 10%	25	
Automotive	-40°C to +125°C	5V ± 10%	25	



HIGH SPEED OPTION (IS61/64C5128AL) POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		-10 Min.	ns Max.	-12 Min.	ns Max.	Unit
			Com	IVIIII.		WIIII.		
Icc1	VDD Operating	$V_{DD} = V_{DD} \text{ MAX.}, \overline{CE} = V_{IL}$	Com.		45	_	45	mA
	Supply Current	IOUT = 0 mA, f = 0	Ind.	_	50	_	50	
			Auto.	_	55	_	55	
lcc2	VDD Dynamic Operating	$V_{DD} = V_{DD} \text{ max.}, \overline{CE} = V_{IL}$	Com.	_	50	_	45	mA
	Supply Current	IOUT = 0 mA, f = fMAX	Ind.	_	55	_	50	
	,		Auto.	_	70	_	60	
			typ.(2)		30		25	
IsB1	TTL Standby Current	VDD = VDD MAX.,	Com.	_	15	_	15	mA
	(TTL Inputs)	VIN = VIH Or VIL	Ind.	_	20	_	20	
	, ,	$\overline{\textbf{CE}} \ge V_{IH}, f = 0$	Auto.	_	30	_	30	
ISB2	CMOS Standby	VDD = VDD MAX.,	Com.		8		8	mA
	Current (CMOS Inputs)	$\overline{CE} \leq V_{DD} - 0.2V$,	Ind.	_	12	_	12	
		$V_{IN} \ge V_{DD} - 0.2V$, or	Auto.	_	20	_	20	
		$V_{IN} \le 0.2V, f = 0$	typ. ⁽²⁾		2			

Note

LOW POWER OPTION (IS61/64C5128AS)

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

				-25	ns		
Symbol	Parameter	Test Conditions		Min.	Max.	Unit	
lcc	Average operating	CE=VIL, VDD=Max.	Com.	_	10	mA	
	Current	IOUT=0 mA, f=0	Ind.	_	15		
			Auto.	_	20		
lcc1	V _{DD} Dynamic Operating	VDD=Max., CE=VIL	Com.	_	25	mA	
	Supply Current	IOUT = 0 mA, f = fMAX	Ind.	_	30		
			Auto.	_	40		
			typ.(2)	1	5		
ISB1	TTL Standby Current	V _{DD} =Max.,	Com.	_	1	mA	
	(TTLInputs)	$V_{IN} = V_{IH} \text{ or } V_{IL}, \overline{CE} \ge V_{IH},$	Ind.	_	1.5		
		f = 0	Auto.	_	2		
IsB2	CMOSStandby	V _{DD} =Max.,	Com.	_	0.8	mA	
	Current (CMOS Inputs)	$\overline{CE} \ge V_{DD} - 0.2V$,	Ind.	_	0.9		
		$V_{IN} \ge V_{DD} - 0.2V$	Auto.	_	2		
		or $V_{IN} \leq V_{SS} + 0.2V$, $f = 0$	typ.	0.	2		

^{1.} At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

^{2.} Typical values are measured at $V_{DD} = 5V$, $T_A = 25\%$ and not 100% tested.

^{1.} At f = fmax, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

^{2.} Typical values are measured at VDD = 5V, TA = 25% and not 100% tested.



READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

		-10		-12	2	-25	5	
Symbol	Parameter	Min. N	/lax.	Min.	Max.	Min.	Max.	Unit
trc	Read Cycle Time	10	_	12	_	25	_	ns
taa	Address Access Time	_	10	_	12	_	25	ns
tона	Output Hold Time	3	_	3	_	3	_	ns
tace	CE Access Time	_	10	_	12	_	25	ns
tdoe	OE Access Time	_	5	_	6	_	15	ns
thzoe(2)	OE to High-Z Output	0	5	0	6	0	8	ns
tlzoe(2)	OE to Low-Z Output	0	_	0	_	2	_	ns
thzce(2)	CE to High-Z Output	0	5	0	6	0	8	ns
tLZCE ⁽²⁾	CE to Low-Z Output	2	_	2	_	2	_	ns

Notes:

- 1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
- 2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
- 3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

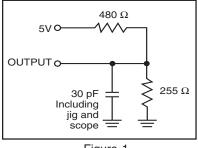


Figure 1

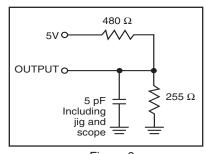
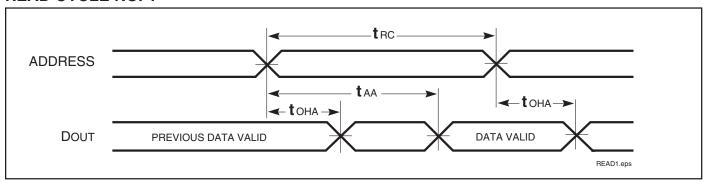


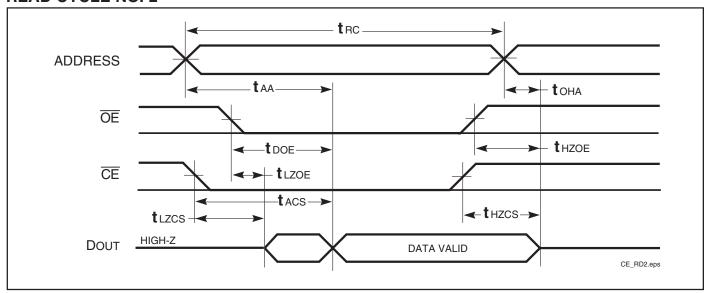
Figure 2



AC WAVEFORMS READ CYCLE NO. 1(1,2)



READ CYCLE NO. 2(1,3)



- 1. WE is HIGH for a Read Cycle.
- 2. The device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
- 3. Address is valid prior to or coincident with $\overline{\text{CE}}$ LOW transitions.



IS64C5128AL/AS



WRITE CYCLE SWITCHING CHARACTERISTICS(1,3) (Over Operating Range)

		-1	0	-1:	2	-2	5	
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
twc	Write Cycle Time	10	_	12	_	25	_	ns
tsce	CE to Write End	7	_	9	_	18	_	ns
taw	Address Setup Time to Write End	7	_	9	_	18	_	ns
tha	Address Hold from Write End	0	_	0	_	0	_	ns
tsa	Address Setup Time	0	_	0	_	0	_	ns
tpwe1	WE Pulse Width (OE =High)	7	_	9	_	15	_	ns
tPWE2	WE Pulse Width (OE=Low)	7	_	9	_	15	_	ns
tsp	Data Setup to Write End	6	_	6	_	15	_	ns
t HD	Data Hold from Write End	0	_	0	_	0	_	ns
thzwe ⁽²⁾	WE LOW to High-Z Output	_	6	_	6	_	15	ns
tlzwe ⁽²⁾	WE HIGH to Low-Z Output	3	_	3	_	5	_	ns

Notes:

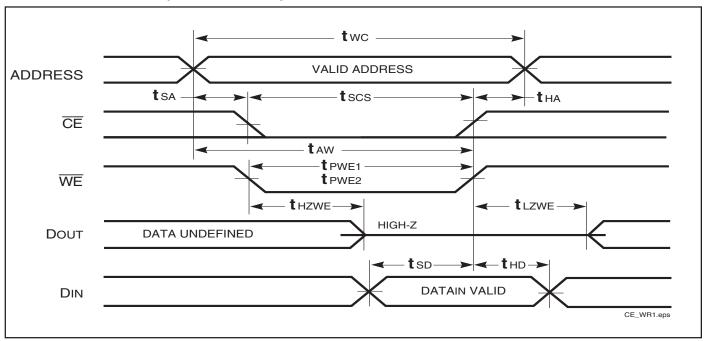
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

^{1.} Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.

^{3.} The internal write time is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.



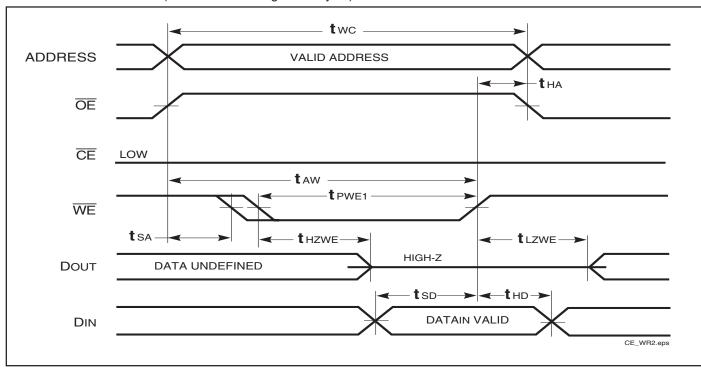
AC WAVEFORMS WRITE CYCLE NO. 1 (WE Controlled)(1,2)



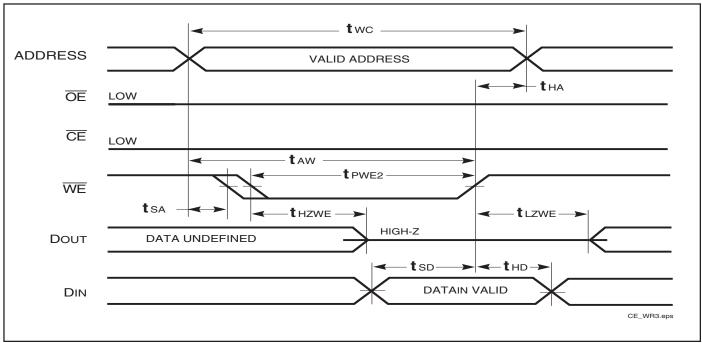
- 1. The internal write time is defined by the overlap of $\overline{\textbf{CE}}$ LOW and $\overline{\textbf{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
- 2. I/O will assume the High-Z state if $\overline{\text{OE}} \ge V_{\text{IH}}$.



WRITE CYCLE NO. 2 (OE is HIGH During Write Cycle) (1,2)



WRITE CYCLE NO. 3 (OE is LOW During Write Cycle) (1)



- 1. The internal write time is defined by the overlap of $\overline{\textbf{CE}}$ LOW and $\overline{\textbf{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
- 2. I/O will assume the High-Z state if $\overline{\text{OE}} \geq V_{\text{IH}}.$

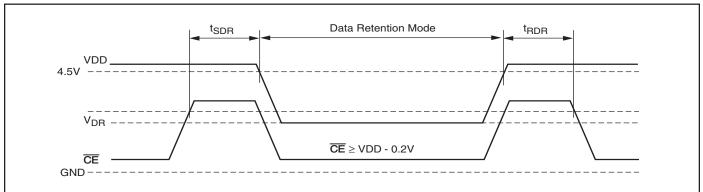


DATA RETENTION SWITCHING CHARACTERISTICS (HIGH SPEED) (IS61/64C5128AL)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
VDR	V _{DD} for Data Retention	See Data Retention Waveform		2.9	5.5	V
lor	Data Retention Current	$V_{DD}=2.9V, \overline{CE} \ge V_{DD}-0.2V$ $V_{IN} \ge V_{DD}-0.2V, \text{ or } V_{IN} \le V_{SS}+0.2V$	Com. Ind.		8 10	mA
			Auto. typ. (1)	_ 1	15	
tsdr	Data Retention Setup Time	See Data Retention Waveform		0	_	ns
t RDR	RecoveryTime	See Data Retention Waveform		trc	_	ns

Note:

DATA RETENTION WAVEFORM (CE Controlled)



^{1.} Typical Values are measured at $V_{DD}=5V$, $T_A=25^{\circ}C$ and not 100% tested.



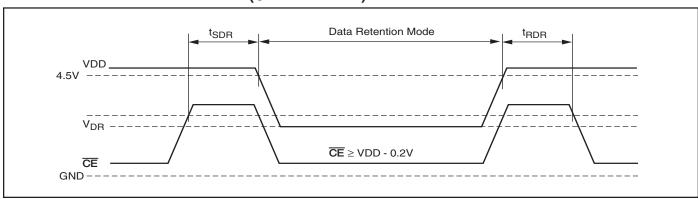


DATA RETENTION SWITCHING CHARACTERISTICS (LOW POWER) (IS61/64C5128AS)

Symbol	Parameter	Test Condition		Min.	Max.	Unit
VDR	VDD for Data Retention	See Data Retention Waveform		2.9	5.5	V
lor	Data Retention Current	$V_{DD}=2.9V, \overline{CE} \ge V_{DD}-0.2V$ $V_{IN} \ge V_{DD}-0.2V, \text{ or } V_{IN} \le V_{SS}+0.2V$	Com. Ind.		0.8 0.9	mA
			Auto. typ. (1)	— 0.2	2	
tsdr	Data Retention Setup Time	See Data Retention Waveform		0	_	ns
t RDR	RecoveryTime	See Data Retention Waveform		trc	_	ns

Note:

DATA RETENTION WAVEFORM (CE Controlled)



^{1.} Typical Values are measured at $V_{DD}=5V$, $T_A=25^{\circ}C$ and not 100% tested.



HIGH SPEED (IS61/64C5128AL) ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package				
10	IS61C5128AL-10KI IS61C5128AL-10KLI IS61C5128AL-10TI	400-mil Plastic SOJ 400-mil Plastic SOJ, Lead-free 44-pin TSOP-II				
	IS61C5128AL-10TLI	44-pin TSOP-II, Lead-free				

Automotive Range: -40°C to +125°C

Speed (ns)	Order Part No.	Package
12	IS64C5128AL-12KA3	400-mil Plastic SOJ
	IS64C5128AL-12TA3	44-pin TSOP-II
	IS64C5128AL-12TLA3	44-pin TSOP-II, Lead-free

LOW POWER (IS61/64C5128AS)

ORDERING INFORMATION

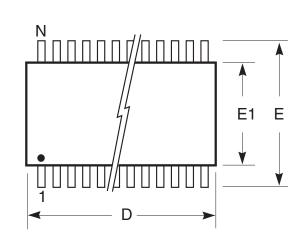
Industrial Range: -40°C to +85°C

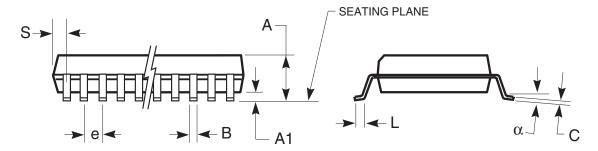
Speed (ns)	Order Part No.	Package
25	IS61C5128AS-25QI	450-mil Plastic SOP
	IS61C5128AS-25QLI	450-mil Plastic SOP, Lead-free
	IS61C5128AS-25HI	32-pin STSOP-I
	IS61C5128AS-25HLI	32-pin STSOP-I, Lead-free
	IS61C5128AS-25TI	32-pin TSOP-II
	IS61C5128AS-25TLI	32-pin TSOP-II, Lead-free



450-mil Plastic SOP

Package Code: Q (32-pin)





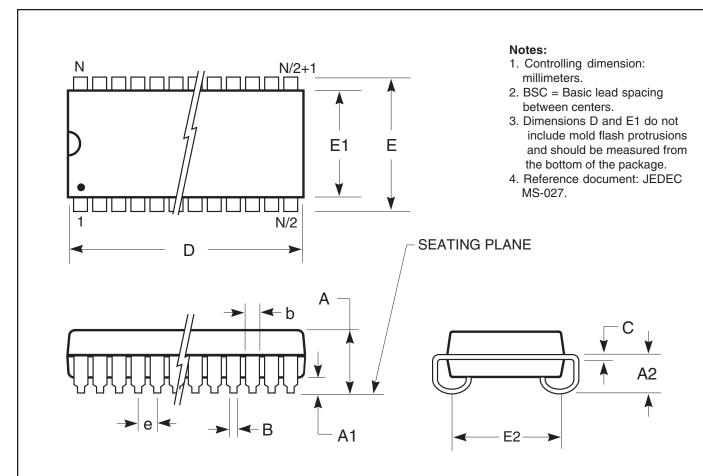
	MILLIM	ETERS		INCHES				
Symbol	Min.	Max.		Min.	Max.			
No. Leads			32					
A	_	3.00		_	0.118			
A1	0.10	_		0.004	_			
В	0.36	0.51		0.014	0.020			
С	0.15	0.30		0.006	0.012			
D	20.14	20.75		0.793	0.817			
Е	13.87	14.38		0.546	0.566			
E1	11.18	11.43		0.440	0.450			
е	1.27 E	3SC		0.050	BSC			
L	0.58	0.99		0.023	0.039			
α	0°	10°		0°	10°			
S	_	0.86		_	0.034			

Notes:

- 1. Controlling dimension: inches, unless otherwise specified.
- 2. BSC = Basic lead spacing between centers.
- 3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
- Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



400-mil Plastic SOJ Package Code: K



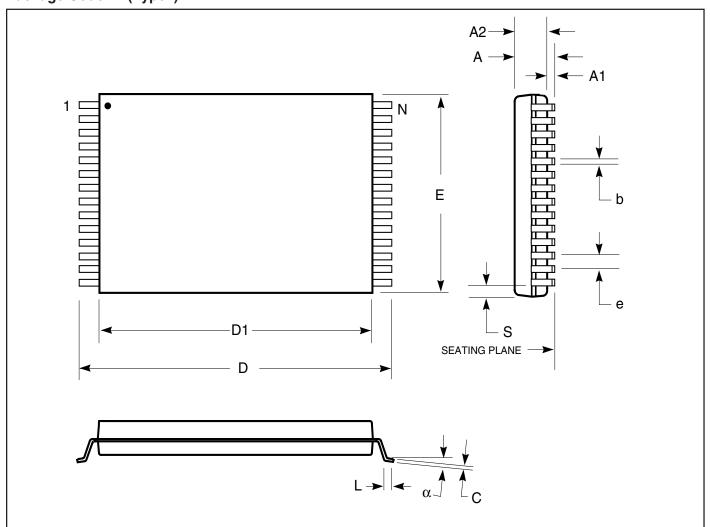
	Millim	eters	Inche	es	Millim	eters	Inche	es	Millin	neters	Inch	es
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads	(N)	28				3	2				36	
Α	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	_	0.025	_	0.64	_	0.025	_	0.64	_	0.025	_
A2	2.08	_	0.082	_	2.08	_	0.082	_	2.08	_	0.082	_
В	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
С	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	18.29	18.54	0.720	0.730	20.82	21.08	0.820	0.830	23.37	23.62	0.920	0.930
Е	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40	BSC	0.370) BSC	9.40	BSC	0.370) BSC	9.40	BSC	0.370	BSC
е	1.27	BSC	0.05	0 BSC	1.27 E	3SC	0.050) BSC	1.27	BSC	0.050) BSC



Millimeters		eters	Inches		Millim	eters	Inche	es	Millin	neters	Inch	es
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
No. Leads (N)			0			42	2				44	
Α	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148	3.25	3.75	0.128	0.148
A1	0.64	_	0.025	_	0.64	_	0.025	_	0.64	_	0.025	_
A2	2.08	_	0.082	_	2.08	_	0.082	_	2.08	_	0.082	_
В	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020	0.38	0.51	0.015	0.020
b	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032	0.66	0.81	0.026	0.032
С	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013	0.18	0.33	0.007	0.013
D	25.91	26.16	1.020	1.030	27.18	27.43	1.070	1.080	28.45	28.70	1.120	1.130
Е	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445	11.05	11.30	0.435	0.445
E1	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E2	9.40	BSC	0.370	BSC	9.40	BSC	0.370) BSC	9.40	BSC	0.370) BSC
е	1.27	BSC	0.05	0 BSC	1.27 E	3SC	0.050) BSC	1.27	BSC	0.050) BSC



Plastic STSOP - 32 pins Package Code: H (Type I)



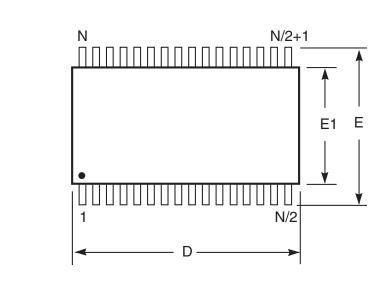
	Plas	tic STS()P (H - T	уре	l)		
	Millim	eters	Inches				
Symbol	Min	Max	M	in	Max		
Ref. Std.							
N			32				
Α	_	1.25	_	-	0.049		
A1	0.05	_	0.0	02	_		
A2	0.95	1.05	0.0	37	0.041		
b	0.17	0.23	0.0	07	0.009		
С	0.14	0.16	0.00	055	0.0063		
D	13.20	13.60	0.5	20	0.535		
D1	11.70	11.90	0.4	61	0.469		
Е	7.90	8.10	0.3	11	0.319		
е	0.50	BSC	(0.020	BSC		
L	0.30	0.70	0.0	12	0.028		
S	0.28	Тур.	0.011 Typ.				
α	0°	5°	0	0	5°		

- Controlling dimension: millimeters, unless otherwise specified.
- 2. BSC = Basic lead spacing between centers.
- Dimensions D1 and E do not include mold flash protrusions and should be measured from the bottom of the package.
- 4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP

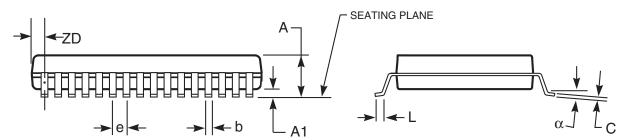
Package Code: T (Type II)



Notes:

- 1. Controlling dimension: millimieters, unless otherwise specified.
- unless otherwise specified.

 BSC = Basic lead spacing between centers.
- Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
- Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



					Plastic T	SOP (T -	Type II)						
	Millim	eters	Inche	s	Millim	Millimeters		Inches		Millimeters		Inches	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Ref. Std.													
No. Leads (N) 32				44	ŀ				50				
Α	_	1.20	_	0.047	_	1.20	_	0.047	_	1.20	_	0.047	
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018	
С	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830	
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405	
Е	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471	
е	1.27	BSC	0.050 E	3SC	0.80	BSC	0.032	BSC	0.80	BSC	0.031	BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024	
ZD	0.95	REF	0.037	REF	0.81	REF	0.032	2 REF	0.88	REF	0.035	REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	