Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor PCI 16-Bit Read Implementation

Application Note

September 2004

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Revision History

Date	Revision	Description
September 2004	002	Updated Intel® product branding.
December 2003r	001	Initial release of this document.

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1.0 Introduction

1.1 Scope

This document describes the PCI 16-bit memory read implementation reference design of the Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor. The IXP42X product line and IXC1100 control plane processors' PCI controller drives all byte enables low (asserted) during a memory cycle read of non-prefetch memory. However, I/O reads and memory-cycle writes do drive individual byte enables.

If an external PCI device has non-prefetch memory and requires either a 16-bit or 8-bit read, there is a possibility that the device will not respond correctly to the IXP42X product line and IXC1100 control plane processors' memory reads. This is because the processors always perform a 32-bit read to the non-prefetch memory region specified in register PCI_NP_AD.

The 8-bit or 16-bit external device should respond with a "target abort," as per the PCI Revision 2.2 specification, if a 32-bit read is performed to its non-prefetch memory and it requires a 16-bit or 8-bit read.

The IXP42X product line and IXC1100 control plane processors will drive all the byte enables asserted during all memory cycle reads of the external PCI device, no matter what the PCI_NP_CBE register contains in the byte enable bits.

1.2 Terminology and Abbreviations

PCI	Peripheral Component Interconnect

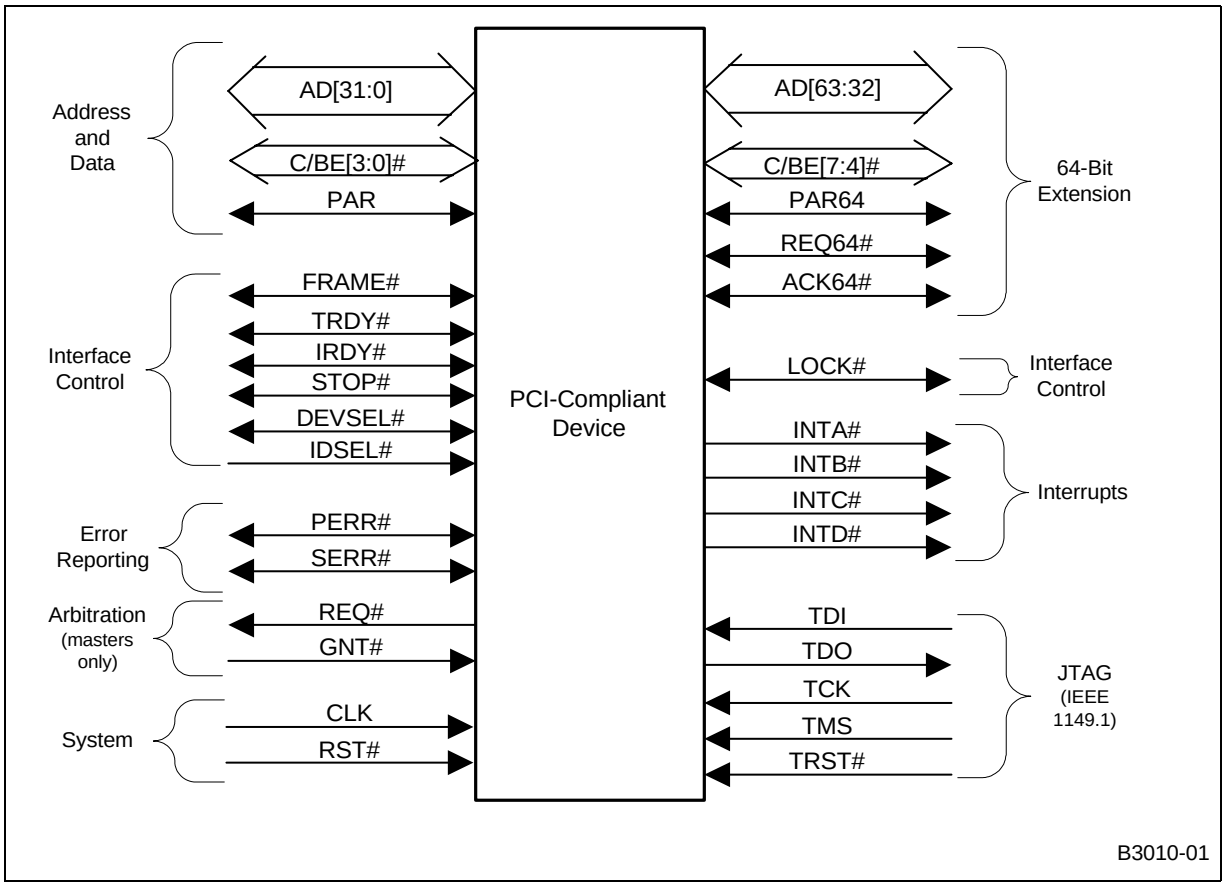
1.3 Related Documents

Document Title	Document #
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual	252480
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet	252479
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Specification Update	252702
PCI Local Bus Specification, Revision 2.2	

1.4 Overview

The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data and addressing, interface control, arbitration and system functions. Figure 1 shows the pins in functional groups with required pins on the left side and optional pins on the right side. The direction indication of signals in the figure assumes a combination master/target device.

Figure 1. PCI Pins List

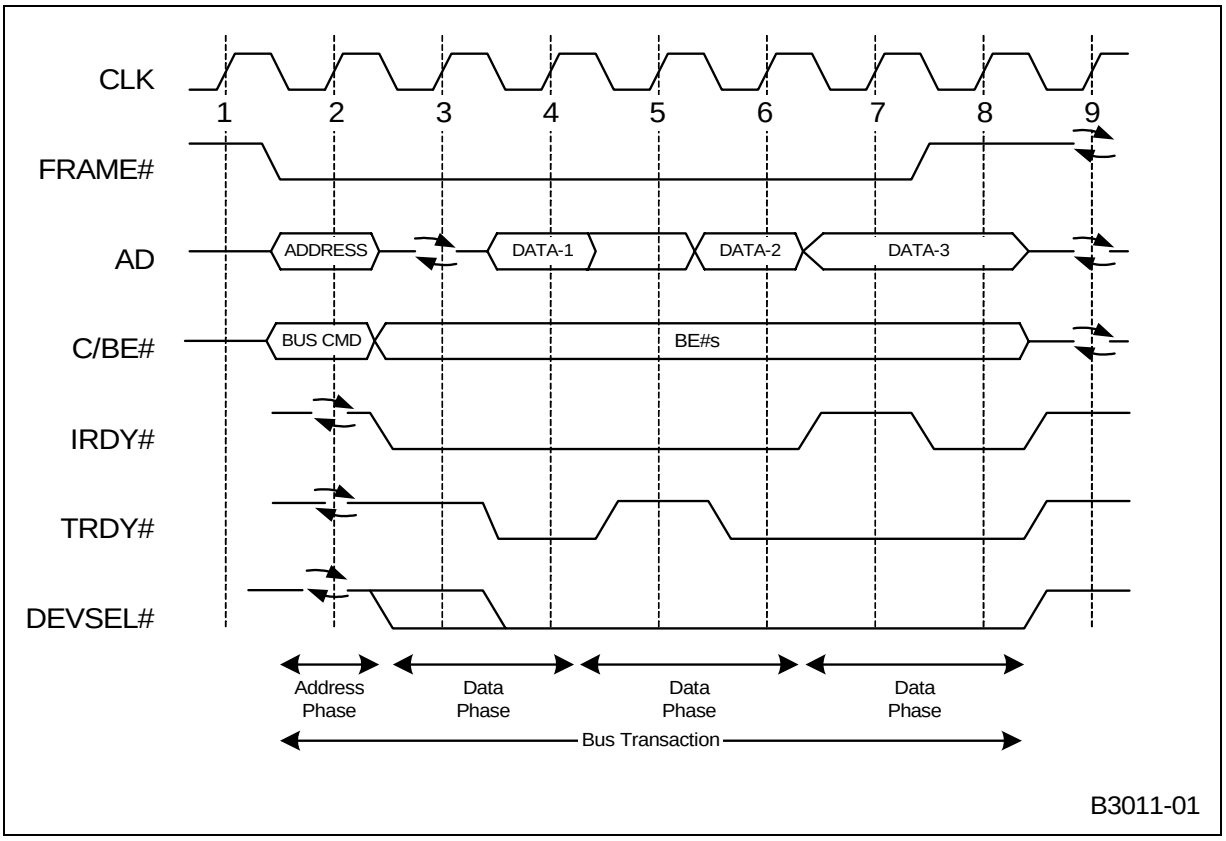


1.5 PCI Revision-2.2 Specification

This section outlines the PCI Revision 2.2 timing diagram for read transaction. Figure 2 illustrates a read transaction and starts with an address phase which occurs when FRAME# is asserted for the first time and occurs on clock 2.

During the address, AD[31:00] contain a valid address and C/BE[3:0]# contain a valid bus command.

Figure 2. PCI Revision-2.2 Read Transaction



1.6 Processors' PCI Controller

The IXP42X product line and IXC1100 control plane processors' 32-bit memory access is the same as Figure 2. The C/BE[3:0] stay as low, when an 8-bit or 16-bit memory read transaction is issued.

Figure 3. Processors' PCI Memory Cycle Read Transaction

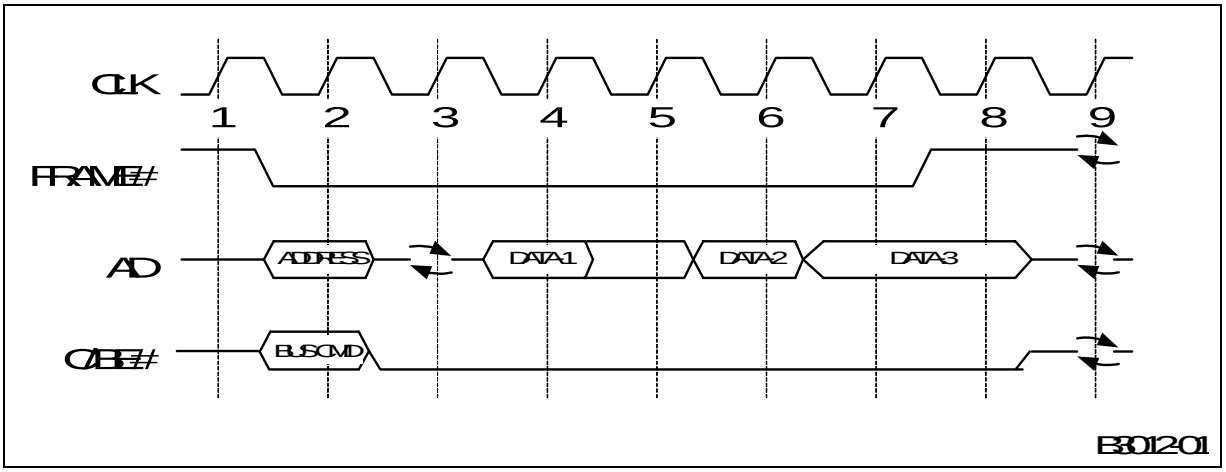


Table 1 shows the correct C/BE[3:0] status when 16-bit memory read transaction. The C/BE# is `1100` when accessing the *lower* 16-bit data on the PCI bus and `0011` when accessing the *upper* 16-bit data. For more information on 8-bit memory read transaction implementation, contact an Intel representative.

Table 1. C/BE# Access Method

C/BE[3:0]#	Read Data [31:16]	Read Data[15:0]
1100		X
0011	X	

2.0 PCI 16-Bit Read Implementation

Figure 4 shows the PCI 16-bit read implementation reference schematic. The implementation's required components are:

- TC7MB3257FK/SN74CBT3257 — Two pieces
- NL17SZ32 — Two pieces
- 10-KΩ resister — Two pieces

Table 2 shows the pin descriptions.

Table 2. PCI 16-bit Read Implementation Pin Description

No	Pin	Description
1	C/BE0_425	Connect to processor's C/BE#0 pin
2	C/BE1_425	Connect to processor's C/BE#1 pin
3	C/BE2_425	Connect to processor's C/BE#2 pin
4	C/BE3_425	Connect to processor's C/BE#3 pin
5	16bit_En_n	Connect to processor's GPIO
6	IRDY_425	Connect to processor's IRDY pin
7	HiByte_en_n	Connect to processor's GPIO
8	C/BE0_Tar	Connect to target device C/BE#0
9	C/BE1_Tar	Connect to target device C/BE#1
10	C/BE2_Tar	Connect to target device C/BE#2
11	C/BE3_Tar	Connect to target device C/BE#3

This implementation required two IXP42X product line and IXC1100 control plane processors GPIO pin to configure for PCI 32-bit or 16-bit access and upper/lower 16-bit access as shown in Table 3. From the datasheets of the Toshiba* TC7MB3257FK and Texas Instruments* SN74CBT3257 multiplexer/demultiplexers, the propagation delay is about 11 ns.

Table 3. PCI 16-bit Read Implementation Pin Logic

No	Items	16bit_En_n	HiByte_En_n
1	32-bit memory transaction or PCI I/O transactions or PCI configuration transactions	High	High
2	16-bit memory transaction for upper 16-bit	Low	High
3	16-bit memory transaction for lower 16-bit	Low	Low

Figure 4. PCI 16-Bit Read Implementation Reference Schematic Read Transaction