Computer Architecture: Project #2

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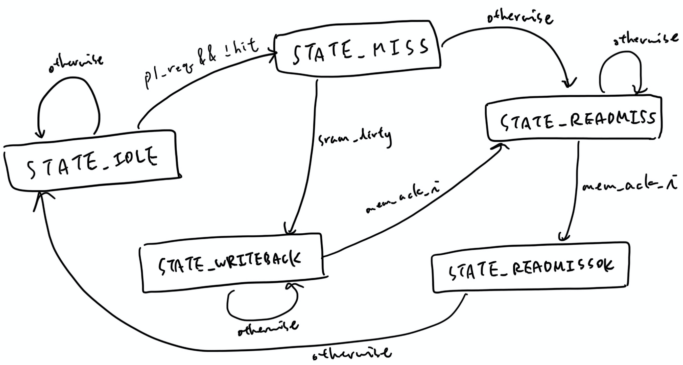
1 Implementation

We connected new modules in CPU first, then starting working on cache. We encountered lots of strange bug during the implementation, therefore we printed lots of things(the commented block in testbench). Note that our implementation of "read value" of the line that is "read miss" will print the value that will be written back to data memory.

2 Cache Controller



The condition to transfer between states is given on the edges. When we transfer from one edge to another, we also modify four variables(*mem_enable, mem_write, cache_we, write_back*) to appropriate values.

3 Difficulties

Didn't notice that Q&A section under the homework website has been updated(no email is sent or something), and debugged for several hours...Also, it take time to understand the given code, maybe more comments will help a lot.

4 Work division

We do this project together

1. Code: b07902047 & b07902139
2. Report: b07902047 & b07902139