Intel 16 UHDLPSPRF SRAM Compiler

DATABOOK

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1 About this Document

1.1 Audience

The information in this document is intended for an SoC design team that is using this IP.

1.2 References

- For additional web resources, contact your Intel representative.
- Contact your Intel Representative to obtain documents referenced in this databook.

Document Title	Type
ASIC Hard-IP Requirements and Integration Guidelines	Confidential
Reliability Requirements Document (RRD)	Confidential

1.3 Customer Support

For IP support issues, contact your Intel representative.

1.4 Terminology

Table 1. Terminology

Term	Definition
1RW SRAM	Single (one) port SRAM. 1RW functionality with 1 read or 1 write
BIST	Built In Self-Test
Bank	Bank: Continuous Memory array block
CM	Column multiplexer
DFT	Design For Testability
DFx Wrapper	RTL wrapper which contains DFT logic and Redundancy Registers (if redundancy is ordered from compiler)
DSE	Dual Supply Enable
HIP	Hard IP (the memory IP)
HVQK	High Voltage Quick Kill
LEF	Library Exchange Format
NB	Number of bits per word
NW	Number of words (total number of memory locations) in a memory
PME	Power Mode Enable
RV	Reliability Verification
Scan	Scan chain for write input data, read output data, control chain with enables such as read or write addresses
SDF	Standard Delay Format
TVC	Transient Voltage Collapse
UHDLPSPRF	Ultra-High Density Low Power Single Port Short Range SRAM.

Term	Definition
VIH	Voltage Input High
VIL	Voltage Input Low
VOH	Voltage Output High
VOL	Voltage Output Low

1.5 Document Revision History

Document Revision Number	Date	Comments
1.0	28 Feb 2022	UV release of the databook.
1.1	24 June 2022	FV release of the databook.

2 Overview

The Ultra-High-Density, Low-Power, Single Port UHDLPSPRF SRAM compiler supports one read or one write (1RW) operation in a cycle. This single power rail, single block architecture uses the HDCLP bitcell.

2.1 Features

The UHDLPSPSR compiler supports the following features:

- **Bit Write Enable:** Supports writing a subset of a word.
- **Power Management**. Lightsleep, Deepsleep and Shutoff modes to provide granular reduction in leakage power.

2.1.1 Compiler Features

Compiler Features

- Bitcell Type: 6T HDC-LP (Intel 16)
- Periphery Device Type: ULP/LP/NOMINAL/LPLVT/LVT

Functionality

- Ports: 1RW
- Clocks: 1 clock
- Bit Write: Supported
- Throughput: 1 cycle
- Latency: Self-timed < 1-cycle
- Read Assist(VMIN/Yield): No
- Write Assist(VMIN/Yield): Yes (TVC)

Standard Array Ranges

- Column Mux: 4 and 8
- Number of Entries: 512 through 4096 and 1024 through 8192
- NW Increment: 32 for CM4 and 64 for CM8
- Number of data bits (NB): 4 through 80 for CM4 and 4 through 40 for CM8
- NB increment: 1

Integration

- Metal Usage: Exclusively up to M4
- Dual Rail: No

Power Modes

- Lightsleep: Voltage to bitcells is lowered. Saves leakage power.
- Deepsleep: Voltage to bitcells is lowered, powers down periphery logic and sets outputs to zero. Saves leakage power.

- Shutoff: Powers down the entire array and sets outputs to zero. Saves on leakage power.

DFT Features

- No DFT features supported at this time.

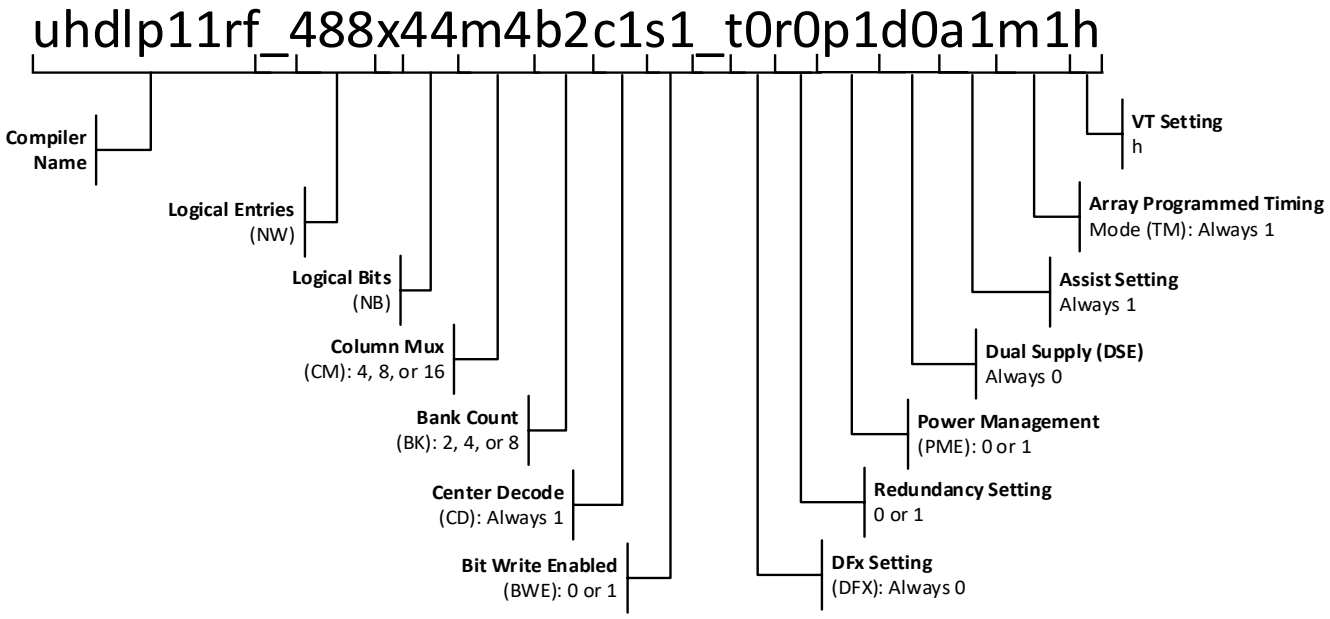
DFM Features

- Margin Control: 1 fuse bit enable and 3 fuse bits for read/write margin control
- Read Assist(VMIN/Yield): No
- Write Assist(VMIN/Yield):
  - Two fuse bits for write-assist pulse width modulation
  - Two fuse bits for write-assist bias level
  - One fuse bit for write-assist enable

2.2 Naming Convention

UHDLPSPRF IPs follow the naming convention shown in Figure 1:

Figure 1. Naming Convention



The nomenclature methodology illustrated in Figure 1 represents all the features available within the compiler. For more specifics regarding allowable word size ranges and compile time options, refer to the sections 2.3 and 2.4.

2.3 Compiler Ranges

Table 2. Compiler Ranges

Column Mux (CM)	Bank	Word Width Increment	Word Depth Increment	Word Width (NB)		Word Depth (NW)	
				Min	Max	Min	Max
4	2	1	32	4	80	512	4096
8	2	1	64	4	40	1024	8192

2.4 Compiler Options

Table 3 lists all available compile time options.

Table 3. Compile Time Options

Feature	Options	Description
Bank	Refer to Table 2	Number of banks. Redistributes the array content to allow larger arrays at the cost of area.
CM	Refer to Table 2	Column Mux. Increasing this modifies the aspect ratio of the array. The tradeoff being the greater NW comes at the cost of maximum NB.
NW	Refer to Table 2	Number of Words/entries of the array. The logical number of addressable datums.
NB	Refer to Table 2	Number of Bits or the size of an entry. The logical size of an addressable datum.
BWE	True, False	Bit Write Enable: Enable pin included for each din pin. Disabling this removes the bit-write mask feature.
PME	True, False	Power Management Enable: Shutoff power management included. Lightsleep, deepsleep, and shutoff features are disabled when this is false.
Timing Derate Enable	Ture, False	When this option is enabled, a predetermined margin is added to the timings in the liberty file and datasheet to account for additional performance degradation due to RC scaling and aging. Enabling Timing Derate has no impact on the physical implementation of the IPs.

2.5 Design Specifications

Table 4. Design Specifications

Parameter	Specification	Comment
Process Technology	Intel 16	
Voltage Condition	VNOM = 0.75 V – 1.00 V	▪ Nominal voltage of the Voltage bands ▪ 1.00 V band support will be 'customer triggered' ▪ Also, refer to section 9.1 for current RV conditions supported
Temperature Range	-55°C to +125°C	
Bitcell	6T HDC-LP (Intel 16)	
Top Metal Layer	M4	Signal ports on M4. Power ports on M4.
Read Latency	< 1 cycle	

3 Architecture

3.1 Block Diagram

Not available for this IP.

3.2 Architecture Scheme

Not available for this IP.

3.3 Compiler Instance Organization

SRAMs are constructed using a compiler/tiling tool. UHDLPSPSRs are built with the following top-level specifications:

- FUB Y dimension is a multiple of 0.090 µm.
- FUB X dimension is a multiple of 0.108 µm.
- SRAMs have M4 ports for signals and power.
- All signal ports have a minimum 0.740 µm lengths.
- SRAM completely uses up to M4. Partition is expected to connect all ports with the via4 dropped down from M5.

3.4 Compiler Instance Logical to Physical Mapping

Figure 2. CM4 Logical to Physical Mapping

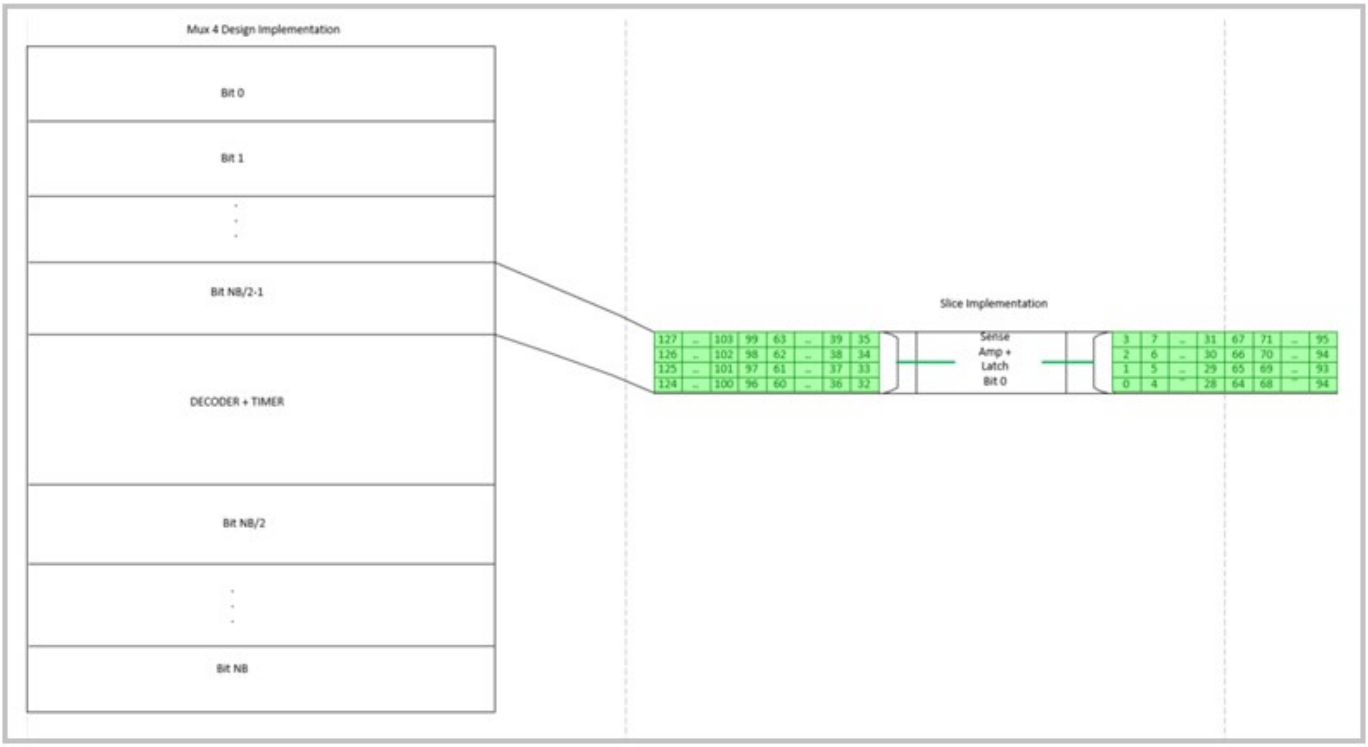
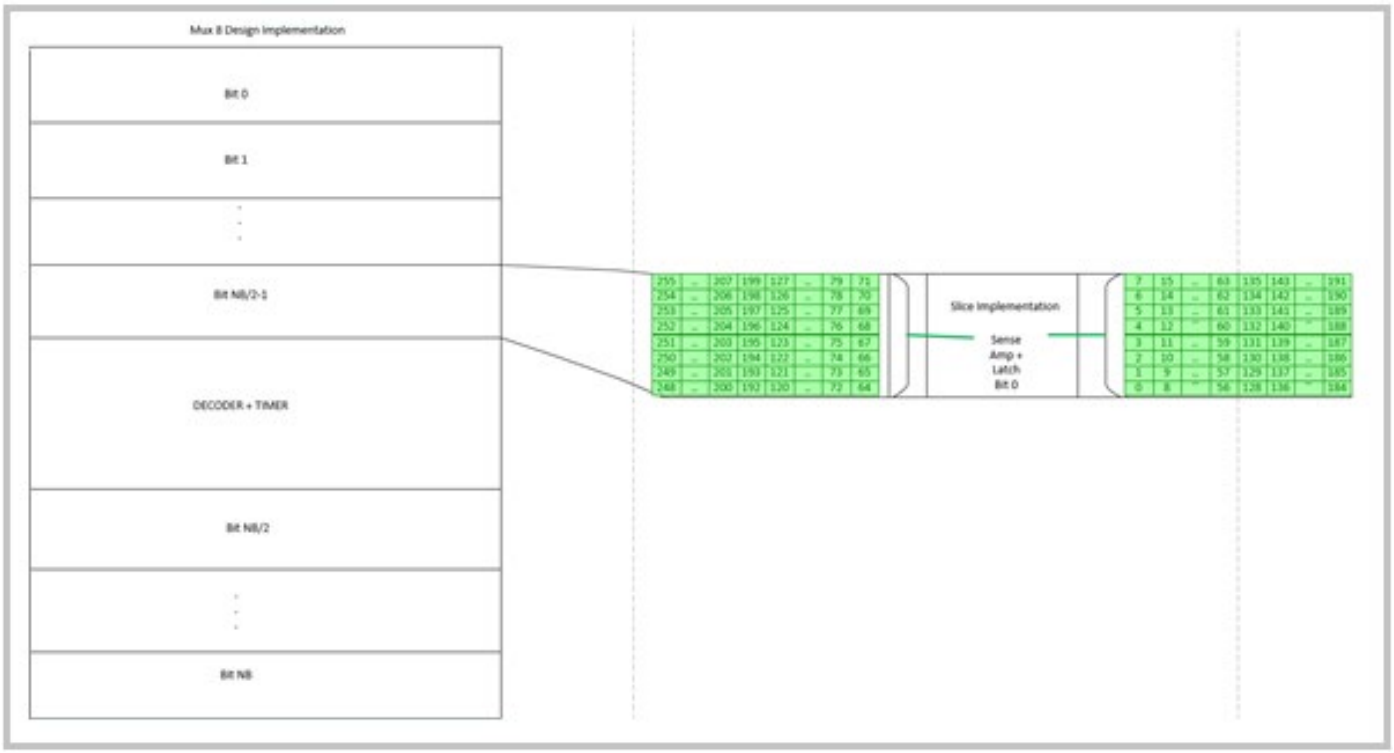


Figure 3. CM8 Logical to Physical Mapping



4 IP Signal Description

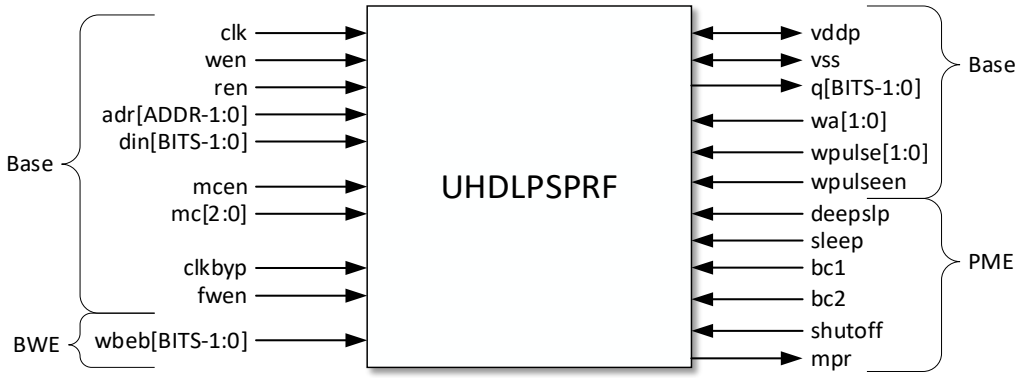
4.1 Signal Description Overview

The UHDLPSPSR compiler contains different signal types, and the status of these signals determine the specific operational modes as listed below:

- Functional read/write signals: Addresses, write/read enable, clock, data-in and data-out
- Embedded test signals for memory BIST
- Test and debug signals: Margin control settings
- Power management signals: Control signals (lightsleep, deepsleep, and shutoff) to reduce static power of the memory IP
- Repair mechanism signals: redundancy signals
- Power supply signals: VDDARY, VDDP, VDDRED, and VSS

4.2 Top-level I/O Diagram

Figure 4. SRAM Top-level I/O Diagram



4.3 Pin Functions and Signal Descriptions

Table 5 lists the functional definitions for each potential pin of the array. For timing requirements on each pin, see section 0, Timing Characterization.

Table 5. Pin Descriptions

Pin Name	Direction	Features (Default or Optional)	Active/ Polarity	Description
Input/Output Control Signals				
clk	Input	Base	Clock	The clock pin for the array. This pin is used for both reads and writes.
wen	Input	Base	High	The write enable pin for the array. A high value enables a write operation on the next rising edge of clk. This should be mutually exclusive with ren.
ren	Input	Base	High	The read enable pin for the array. A high value enables a read operation on the next rising edge of clk. This should be mutually exclusive with wen.
adr[]	Input	Base	High	The address bus for the array. This vectored signal will be of size log (NW)/log (2), rounded up. This encoded address selects the specific word to read or write on the next rising clock edge.
din[]	Input	Base	High	The write data input bus. This is the same size as NB. If a write is enabled on the next rising edge of clk, this data is written to the address provided by adr[].
q[]	Output	Base	High	The read data output bus. This is the same size as NB. When a read is enabled, this will change to read the data stored at adr[] sometime after the next rising edge of clk. If the array is put into shutdown, deepsleep, or firewall mode, this bus takes on all zero values.
wbeb[]	Input	BWE	Low	The Write Bit Enable bus. This bus is the same size as NB. This operates as a bit-write enable mask for din[]. Each bit index applies to a bit of the din[] bus of the same index (aka wbe[7]⇔din[7]). When this signal is low, the corresponding bit of din[] is written to the entry selected with adr[] during a valid write operation sometime after the rising edge of clk. When this signal is high, writing for that specific bit of din[] is blocked.
Array Functional Control Signals and Associated Fuses				
mcen	Input	Base	High	Margin Control Enable is a fuse pin. This signal is used to select between the internally programmed setting for the array (default) and a user provided setting. Enabling this by setting it high, will set the array to utilize mc[] as overrides for the default values and should be fuse driven for DVFS implementation.
mc[2:0]	Input	Base	High	Read/Write Margin Control bits are fuse pins. This three-bit bus can be used to override an array's default read/write margin setting. Should be fuse-driven for DVFS implementation.

Pin Name	Direction	Features (Default or Optional)	Active/ Polarity	Description
clkbyp	Input	Debug	High	clkbypis a fuse pin. Under normal operation, the array utilizes an internally generated self-timed clock and executes command on the rising edge of the clock. In debug mode, when this signal is enabled by driving it high, the array bypasses its self-timed clock and uses both edges of input clk to execute read and write commands. This signal must be held stable during an operation cycle. A noop cycle must be inserted before entering this mode and after exiting it.
wa[1:0]	Input	Assist	High	TVC write assist bias control bits are fuse pins. This bus varies the strength of the write-assist circuit.
wpulse[1:0]	Input	Assist	High	TVC write assist pulse width control bits are fuse pins. This bus varies the width of the write-assist pulse.
wpulseen	Input	Assist	High	TVC write assist enable is a fuse pin. Setting this signal to high enables write-assist.
fwen	Input	Base	High	Input and output firewall enable. Driving this signal high causes the array to ignore the value of key input signals and force q[] output bus to zero. It also serves as an asynchronous reset signal for all input latches and should not be tied-off.
Power Mode Signals				
sleep	Input	PME	High	The lightsleep enable signal. When this is high, the array will drop into lightsleep retention mode. This mode is superseded by deepsleep or shutoff.
deepslp	Input	PME	High	The deepsleep enable signal. When this is high, the array drops into deepsleep retention mode and zeroing out the q[] bus. This mode is superseded by shutoff.
shutoff	Input	PME	High	This shutoff enable signal. When this is high, the array drops into shutoff, losing all data and zeroing out the q[] bus.
mpr	Output	PME	High	MPR, or the Memory Power Ready signal, signals when the array has completed power-on. This signal rises shortly after shutoff rises and falls sometime after shutoff falls.
bc1	Input	PME	High	Sleep Bias Control 1 is a fuse signal. One of two bias-control signals used to adjust the bias voltage during lightsleep and deepsleep.
bc2	Input	PME	High	Sleep Bias Control 2 is a fuse signal. One of two bias-control signals used to adjust the bias voltage during lightsleep and deepsleep.
Power Rails				
vss	Inout	Power	Power	The ground rail.
vddp	Input	Power	Power	The standard VCC rail for the array. All ASIC periphery logic is on this rail, and, when DSE is disabled, the array will be on this rail as well.

5 Modes of Operation

5.1 Memory Operations and Settings for Power Mode Enable

Table 6. PME Modes

Shutoff	deepslp	sleep	fwen	q[NBIT-1:0]	Mpr	Functional Inputs	Bias Control	Timing Control	Assist Control
							(BC1/BC2)	(MC[2:0] / MCEN)	(WA/WPULSE)
0	0	0	0	q-1	0	Driven 1 or 0	Driven 1 or 0	Driven 1 or 0	Driven 1 or 0
0	0	0	1	Clamped 0	0	Allowed to Float	Driven 1 or 0	Allowed to float	Allowed to float
0	0	1	0	q-1	0	Driven 1 or 0	Driven 1 or 0	Driven 1 or 0	Driven 1 or 0
0	0	1	1	Clamped 0	0	Allowed to Float	Driven 1 or 0	Allowed to float	Allowed to float
0	1	Allowed to float	Allowed to Float	Clamped 0	0	Allowed to Float	Driven 1 or 0	Allowed to Float	Allowed to Float
1	Allowed to Float	Allowed to Float	Allowed to Float	Clamped 0	1	Allowed to Float	Allowed to Float	Allowed to float	Allowed to float

5.2 Truth Table for Read and Write Operations

Table 7. Truth Table for Read-Write Operations

Mode	CLK	WEN	DIN	REN	Memory Array	Q
Idle	0	X	X	X	NC	Q-1
Disabled	X	0	X	0	NC	Q-1
Write	0→1	1	Data-In	0	Mem[ADR] =Data-In	Q-1
Read	0→1	0	X	1	NC	Q= Mem[ADR]

5.2.1 Contention Memory Behavior during Read – Write Operations

When read and write occur simultaneously, both operations fail and the bitcell value will be corrupted.

6 Timing

6.1 Timing Modes and Fuse Pin Settings

Three control pins and one enable are used to define the timing mode for both read and write, with eight timing modes supported, as shown in Table 8. The default timing mode, TM1, occurs when mce=0, the minimum functional voltage that the memory supports.

Table 8. Platform Timing Mode Alignment

Timing Mode	mc[2:0]	VNOM (V)	Voltage Range (V)	Comment
TM7	111	1.0	0.90 - 1.05	▪ Vhigh ▪ 1.00 V band support will be 'customer triggered' ▪ Also, refer to section 9.1 for current RV conditions supported
TM6	110	-	0.765 – 1.05	Reserved: Tcc and Tcq arcs reflect large invalid numbers
TM5	101	0.85	0.765 – 1.05	Vmed
TM4	100	-	0.675 – 1.05	Reserved: Tcc and Tcq arcs reflect large invalid numbers
TM3	011	0.75	0.675 – 1.05	Vlow
TM2	010	-	0.585 – 1.05	Reserved: Tcc and Tcq arcs reflect large invalid numbers
TM1	001	0.65	0.585 – 1.05	Vulow (Not supported by UHDLPSPRF)
TM0	000	-	0.585 – Burn-in	Test Mode (Supports Burn-In and Debug) Tcc and Tcq arcs reflect large invalid numbers

6.1.1 Timing Mode Characterization Points

Table 9. Timing Mode Characterization Points

Timing Mode	Minimum Voltage Supported by Timing Mode (V)	PVT Voltage Band			
		Vhigh [2] 1.0 V	Vmed 0.85 V	Vlow 0.75 V	Vulow 0.65 V
TM7	0.90	111	101 [1]	011 [1]	001 [1]
TM5	0.765	101	101	011 [1]	001 [1]
TM3	0.675	011	011	011	001 [1]
TM1	0.585	001	001	001	001
TM0	Slow test/debug setting	000	000	000	000

NOTES:

1. Copied from fastest timing mode setting that supports the specified PVT voltage band.
2. 1.00 V band support will be 'customer triggered'.
   Also, refer to section 9.1 for current RV conditions supported.

6.1.2 Fuse Pin Guidelines

- Fuse pins (also called trim bits) are a pre-defined set of pins based on compiler type. They generally include all configuration pins to program memories with optimal settings and to help with debug, such as TM (timing mode) pins, assist setting pins (technology requirement), and other miscellaneous pins like sleep bias level control.
- All fuse pins should be programmable to allow optimization in production (setting requirements may change based on silicon learnings). Do not tie off any fuse pins.
- Fuse pins have two types of settings: safe power-up settings, and standard functional settings.
  - Safe power-up settings are the most pessimistic known configuration settings that the silicon is expected to work with. These settings are used for first-time silicon power-up.
  - Standard functional settings are used after a successful silicon power-up. They represent the memory operational settings chosen by customers to meet the SoC target specification.
- A dedicated set of fuse pins should be assigned to each memory compiler type. Fuse pins can be shared by instances from the same compiler even if they reside in different SoC partitions.
- If Control and Status Registers (CSRs) are used instead of fuses, CSR initialization and loading should not depend on any memory to avoid potential race conditions at boot-up time.
- Applicable timing mode settings should be defined with valid conditional arcs for each memory type to configure target frequency, voltage range, and temperature range values.
- Even though a majority of the low power/PME (Power Mode Enable) configuration pins are not fuse pins, proper timing constraints should be applied on them during static timing analysis for correct implementation.

Fuse pin settings and static timing analysis constraints are explained in sections 6.1.3 and 6.1.4.

6.1.3 Fuse Pin Settings and Recommended Timing Constraints

Table 10. SRAM Compiler Fuse Pin Settings

Pin Name	Description	Recommended Static Timing Analysis Constraints (STA/PV)	Fuse/CSR Settings	
			Safe power-up Settings	Standard Functional Settings
mcen	Margin-control enable [0] Hardwired to select default voltage band [1] Enables override with mc* pin settings	case_analysis	0	1
mc[2:0]	Margin control bus	case_analysis	000	Setting depends on voltage band. Refer to Table 8.

Pin Name	Description	Recommended Static Timing Analysis Constraints (STA/PV)	Fuse/CSR Settings	
			Safe power-up Settings	Standard Functional Settings
clkbyp	Self-timed clock bypass [0] self_time (default) [1] debug, HVQK/BurnIn	case_analysis	0	0
wa[1:0]	Write assist level control [00] Highest droop (default) [01] Second highest droop [10] Smaller droop [11] Smallest droop	multicycle_path	00	00
wpulse[1:0]	Write assist pulse width control [00] Widest pulse (default) [01] Second widest pulse [10] Narrower pulse [11] Narrowest pulse	multicycle_path	00	00
wpulseen	Write assist enable [0] Disable [1] Enable	multicycle_path	1	1
[bc2,bc1]	Sleep bias voltage level control during lightsleep/deepsleep (PME pins)	multicycle_path	00	Refer to Table 13.

6.1.4 Low Power Mode Pins

Table 11. SRAM Compiler PME Pin Constraints

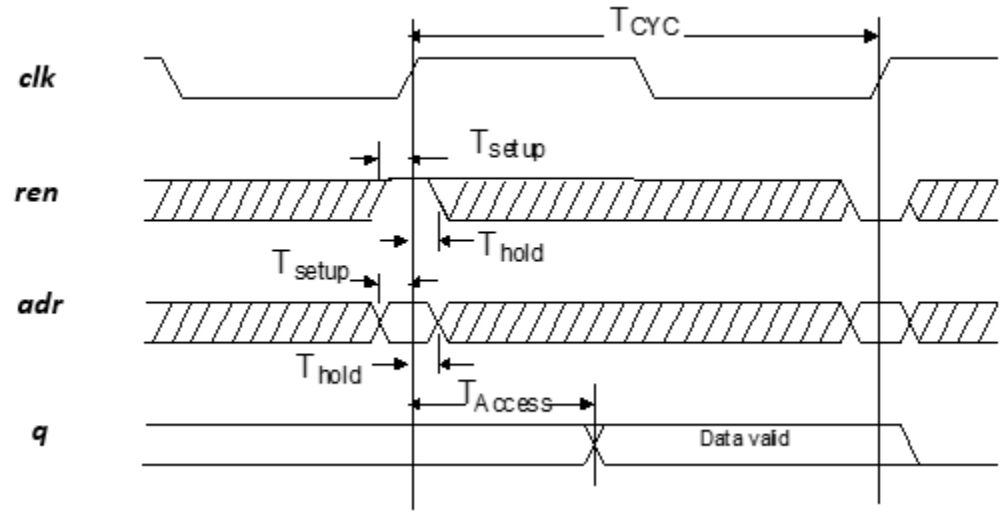
Pin Name	Description	Recommended Static Timing Analysis Constraints (STA/PV)
sleep	Lightsleep retention mode enable	Use multicycle_path if PME is enabled, else tie off.
deepslp	Deepsleep retention mode enable	Use multicycle_path if PME is enabled, else tie off.
shutoff	Shutoff enable	Use multicycle_path if PME is enabled, else tie off.

6.2 Read and Write Timing Waveforms

The diagrams in Figure 5, and Figure 6 illustrate the read and write timing waveforms. All timing events are referenced off the rising edge of the clock clk.

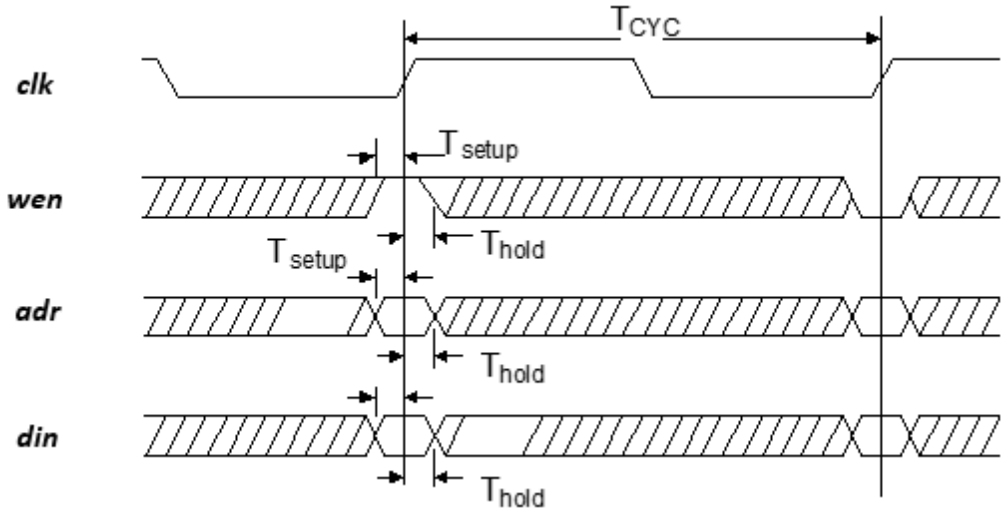
Memory read occurs at the selected address when read enable ren is asserted prior to the high phase of the clock (refer to Figure 5).

Figure 5. Read Timing Waveform



Memory write occurs at the selected address when write enable wen is asserted prior to the high phase of the clock (Figure 6).

Figure 6. Write Timing Waveform



6.3 Reset

fwen (firewall enable) pin is set to 0 during normal active operation. Value of 1 resets the SRAM data outputs. This pin has built-in reset function for internal self-timed clock.

6.4 Clock

UHDLPSPRF SRAM arrays utilize only one clock signal "clk" and operates in self-time or clock-bypass modes. Input clock can have an imbalanced duty cycle. However, a minimum high and minimum low pulse-width is required (as specified in the liberty files) to assure correct functionality.

In self-time mode, read/write operations are initiated by rising the edge of the input clock to complete by the end of a self-timed period. This self-timed interval can be adjusted by changing the Margin Control input settings (mcen/mc[2:0]). The input clock period must be equal or greater than the TCC value specified in the liberty files per the mc settings for the operations to complete successfully.

6.4.1 Self-Timed Bypass Mode

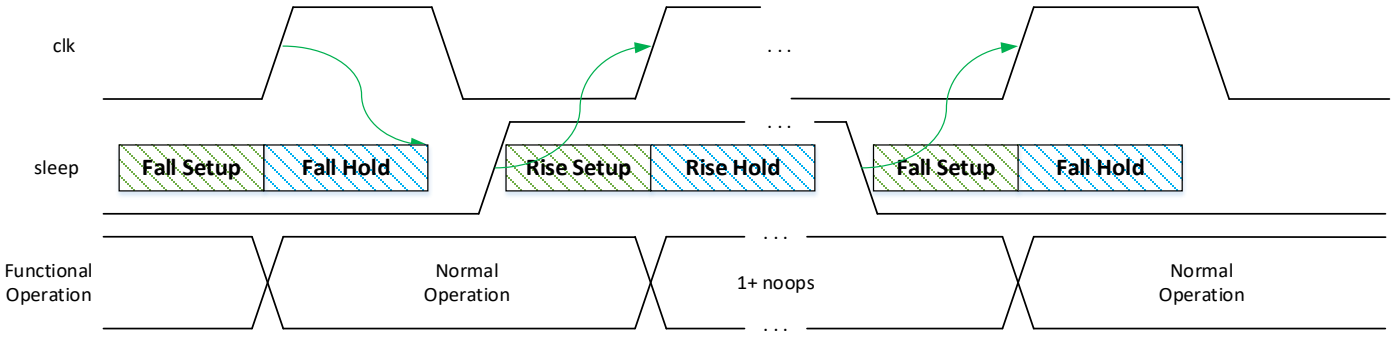
In clock-bypass mode, read/write operations are initiated by rising the edge of the input clock and self-timed pulse while ignoring Margin Control settings. Instead, the falling edge of the input clock is utilized to initiate sensing operation in read cycles and the end of WL in write cycles. Therefore, read/write margins can be adjusted by changing the input clock period. In high frequencies, read data outputs are available in the second phase of clock after its falling edge. However, in low frequencies, read data may be available sooner in the first phase. The input clock period must be equal or greater than the TCC value specified in the liberty files for the operations to complete successfully.

Clock-bypass enable input signal (clkbyp) is not registered. Therefore, it needs to hold stable during the operations (as specified in timing liberty file). In addition, to avoid any functional failures, a noop cycle must be inserted before entering clock-bypass mode and after exiting it. Clock-bypass mode is considered a test mode only, and the power/performance of arrays might not comply with the PPA spec.

6.5 Timing Diagrams: Inputs, Outputs, Asynchronous and Synchronous

Figure 7 illustrates the timing constraints for lightsleep.

Figure 7. Lightsleep Timing Constraints

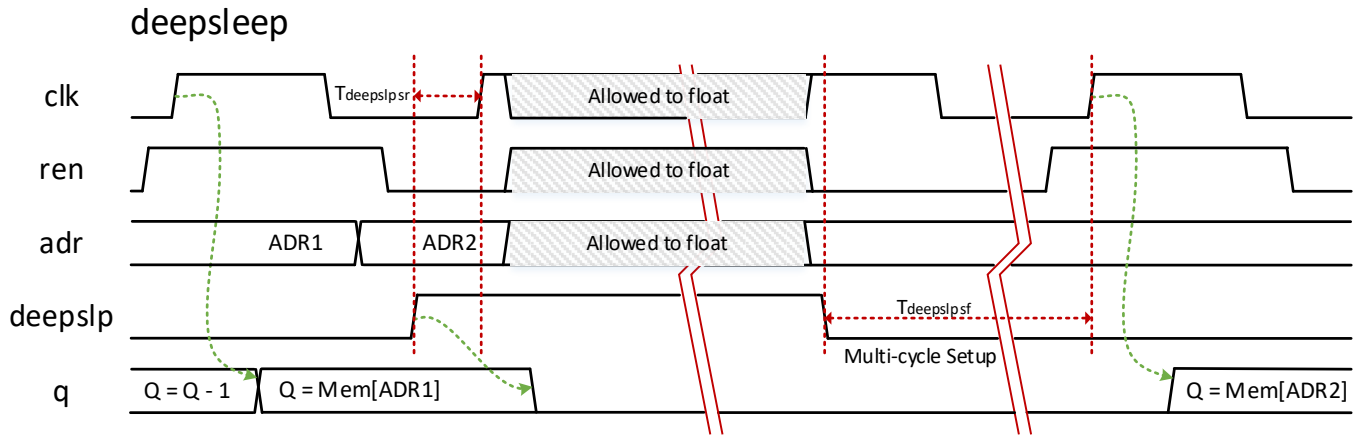


If setup and hold requirements are met before their respective rising edges of the clock, sleep can be entered and exited from within a cycle (may not be possible in all IP sizes, please refer to liberty file), and that functional pins (like ren, wen, and the clock) are ignored while sleep is asserted. Additionally, if sleep arrives *late* and an operation occurs in the cycle following sleep's assertion, the read or write may occur, resulting in either an invalid read (and the corruption of the q[] bus) or the corruption of the data in the array.

$T_{sleephf}$ may be long relative to T_{CQ}. This is because asserting sleep in the middle of an operation may corrupt the operation itself, so sleep must be held low for a certain period of time when a valid operation is occurring.

Figure 8 demonstrates the timing constraints for the deepsleep.

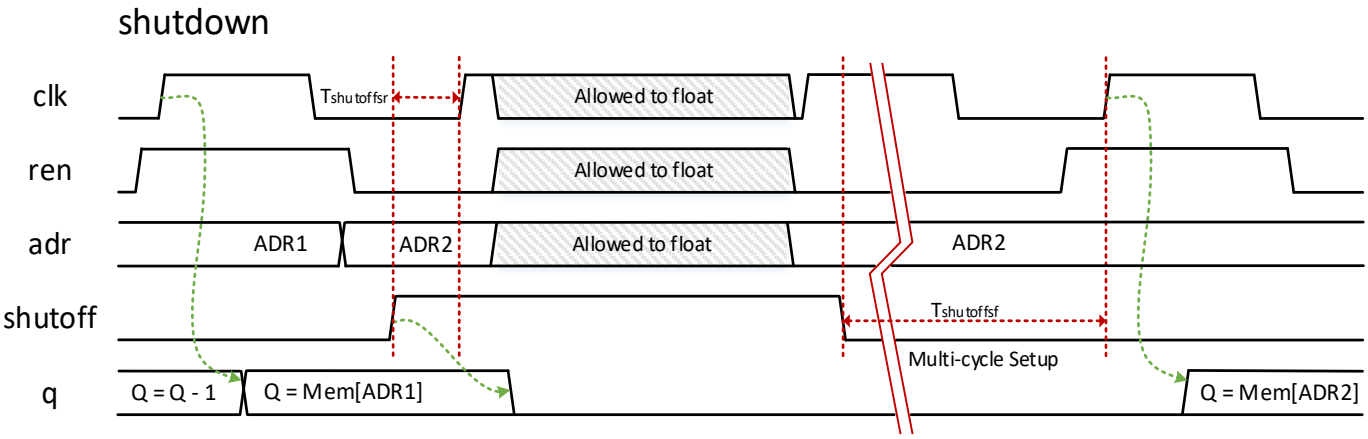
Figure 8. Deepsleep Timing Constraints



During deepsleep, non-PME inputs are firewalled and can be floated since power is cut-off to the array periphery. The output q[] bus will be zeroed out when entering deepsleep and remains so until the next legal read operation. Also note that exiting deepsleep is a multi-cycle (slow) operation. Although functional inputs are explicitly firewalled by the deepsleep signal, they still need to be driven to 1 or 0 before deepsleep is deasserted (or fwen must be utilized) to avoid short-circuit current during wakeup.

Figure 9 demonstrates the timing constraints for shutdown.

Figure 9. Shutdown Timing Constraints



Shutdown signal explicitly firewalls various functional input signals, allowing them to float. Additionally, the output bus goes to zero when entering shutoff, and will remain so until the next legal read operation. The array's contents become invalid during shutoff. Exiting shutoff is a slow, multi-cycle operation, requiring all functional inputs to stay firewalled until the MPR signal goes low. Clock can freely toggle during power-up.

7 Power Supply and Management

7.1 Power-on Sequence

As these arrays do not support DSE, power-on sequencing is straight forward. During the rise of VDDP, all internal states are unknown (X). Array data can only be initialized with a write operation to that address. The read data bus q[] will be unknown until the first read is performed. All signal and fuse inputs should be settled before performing operations on the array.

7.2 Power Saving Modes and Features

UHDLPSPRF arrays feature three distinct power-saving modes: lightsleep, deepsleep, and shutoff.

7.2.1 Lightsleep

Lightsleep is a fast power-saving mode, that supports the ability to lower voltage on the bitcell, in addition to turning off the wordline drivers. This in turn saves leakage power, while retaining data in order to wake up quickly.

When lightsleep is active, the input signals clk, ren and wen are firewalled and output data on the q[] bus is retained.

In this mode, it is possible to turnoff power to the wordline drivers without lowering the bitcell voltage by setting bc2 = bc1 = 0. For other bc2/bc1 bias settings see Table 13.

7.2.2 Deepsleep

Deepsleep is more dominant than lightsleep, power-gating the periphery logic in addition to the savings realized with lightsleep alone. The tradeoff, however, is that significantly more time is required to wake up after going into deepsleep than lightsleep.

As in lightsleep, it is possible to turn off power to the wordline drivers without lowering bitcell voltage by setting bc2 = bc1 = 0. For other bc2/bc1 bias settings see Table 13.

When deepsleep is active, the input signals clk, ren, wen and sleep signals are firewalled. The output bus q[] is set to 0 and remains that way until the next legal read operation.

7.2.3 Shutoff

Shutoff turns off the entire array, does not retain state, requires additional time to enter and leave, but also leads to the greatest savings in power. During shutoff all inputs associated with fwen are firewalled, including sleep, deepslp, BC1 and BC2 signals. The q[] bus is set to 0 until the next legal read operation.

7.3 Power Supplies

UHDLPSPRF arrays are single rail designs without any hardened DFx/BIST/redundancy logic. These arrays support two power planes: VDDP and VSS, shared by both the internal control logic and bitcells.

7.4 Power Mode Definitions and Models

The power modes in Table 12 are supported as configured.

Table 12. Power Modes

Mode	Controlling Signal	Description
standby	none	The default standby operating mode is without PME enabled. This is the default mode for performing reads/writes and has the highest leakage level.
lightsleep	sleep, bc1, bc2	When the sleep signal is enabled, the array drops into a lightsleep mode which lowers the overall array leakage. While saving power, normal operation is not possible and the state is retained. bc1 and bc2 can be used to reach greater levels of leakage savings, based on their settings. However, some settings may be invalid depending on the actual voltage level of vddp/vddary while still guaranteeing data retention. (Table 13) The wordline drivers are powered down, saving additional leakage. The retention voltage is determined by BC1/BC2 input settings. SRAM outputs are preserved in their current state.
deepsleep	deepslp, bc1, bc2	When the deepslp signal is enabled, the array drops into a deepsleep mode which lowers the overall array leakage. While saving power, normal operation is not possible and state is retained. bc1 and bc2 can be used to reach greater levels of leakage savings, based on their settings. However, some settings may be invalid depending on the actual voltage level of vddp/vddary while still guaranteeing data retention. (Table 13) The wordline drivers and all periphery logic are powered down, providing additional leakage savings over light-sleep. The retention voltage is determined by BC1/BC2 input settings. SRAM outputs are set to 0 and will stay at 0 till next functional read.
shutoff	shutoff	When shutoff is enabled, the array powers down. State is NOT retained in this mode. SRAM outputs are set to 0 and will stay at 0 until the next functional read.

Based on the settings of bc1 and bc2, the behavior described in Table 13 can be expected:

Table 13. Variable Sleep Modes

Setting (bc2 bc1)	BPBL=NW/(Bank*CM)	Description: Bitcell Supply Rail Droop and Restrictions
0 0	128 < BPBL ≤ 512	Disables droop (bitcell sleep bypass), ***must*** use for vddp < 0.75 V
0 0	64 ≤ BPBL ≤ 128	Disables droop (bitcell sleep bypass)
0 1	128 < BPBL ≤ 512	Highest droop, illegal for vddp < 0.75 V, optimal setting for vddp ≥ 0.75 V
0 1	64 ≤ BPBL ≤ 128	Highest droop, optimal leakage setting
1 0	128 < BPBL ≤ 512	Medium droop, illegal for vddp < 0.75 V
1 0	64 ≤ BPBL ≤ 128	Medium droop
1 1	128 < BPBL ≤ 512	Smallest droop, illegal for vddp < 0.75 V
1 1	64 ≤ BPBL ≤ 128	Smallest droop

Note: If IPs with different values of NW/(Bank * CM) are sharing bc1/bc2 fuses, the worst-case setting should be used to avoid the illegal scenario mentioned above.

7.4.1 Leakage Power Management

The Intel 16 UHDLPSPRF compiler supports the following power management features:

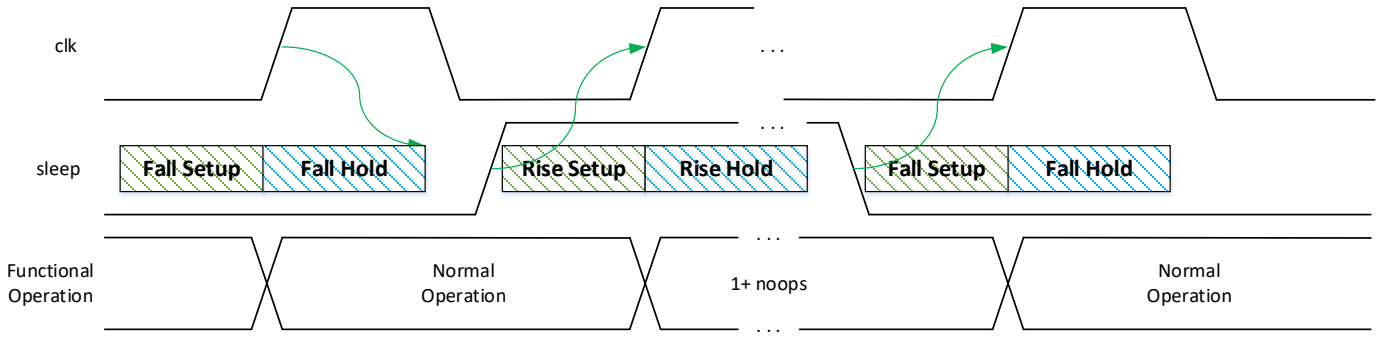
- **Light-Sleep mode**: When the SLEEP pin is asserted, the memory array optionally drops the voltage on the bitcell, retaining state but saving leakage power. Additionally, the wordline drivers are powered down, saving additional leakage. The retention voltage is determined by BC1/BC2 input settings. SRAM outputs are preserved in their current state.
- **Deep-Sleep mode**: When the DEEPSLP pin is asserted, the memory array optionally drops the voltage on the bitcell, retaining state but saving leakage power. Additionally, the wordline drivers and all periphery logic are powered down, providing additional leakage savings over light-sleep. The retention voltage is determined by BC1/BC2 input settings. SRAM outputs are set to 0, and will stay clamped till next functional read
- **Firewall mode:** In this mode, the SRAM supports input firewalling, and sets the data output to 0. To enable firewalling, assert the FWEN signal
- **Shut-off mode**: When the SHUTOFF pin is asserted, the VDDP/VDDARY supply is power-gated and the array bitcells and periphery are shut off. Memory content is not retained, and the memory outputs are set to 0.

7.5 Allowable Power Scenarios

7.5.1 Active/Lightsleep Power Scenario

In this mode of operation, the array can enter sleep at the end of an active cycle so long as the associated checks are not violated. For very large arrays or high frequencies, this may necessitate a no-op cycle to correctly enter or exit sleep. For this mode of operation, a selection of input signals is firewalled. Firewalls and the voltage on the bitcell are optionally lowered in an effort to save on leakage, based on the settings of the non-latched fuse signals BC1 and BC2. Figure 10 shows an example of an array entering, remaining in, then leaving lightsleep.

Figure 10. Cycling through Lightsleep



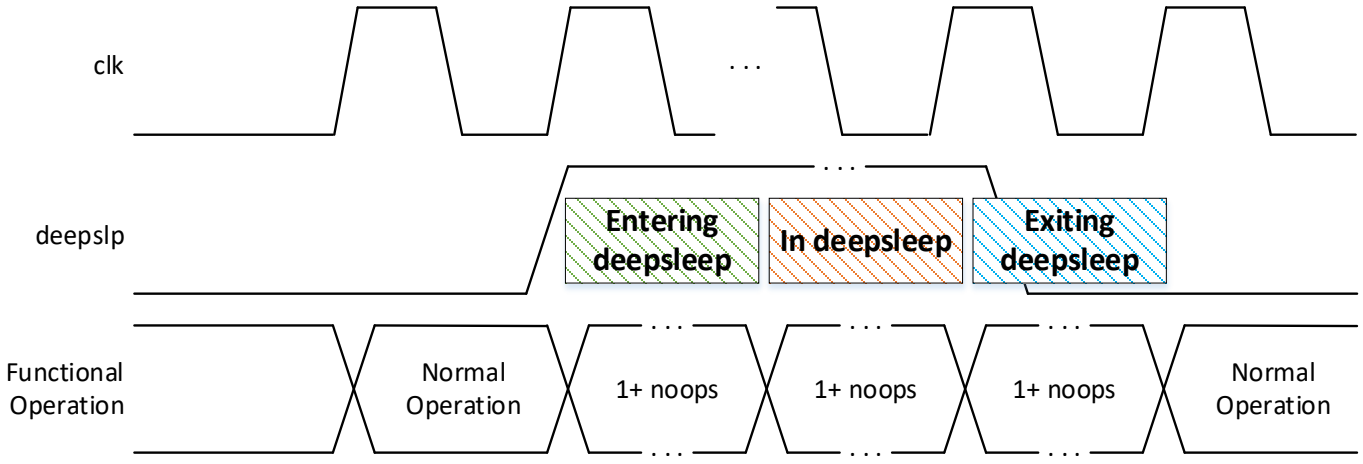
Sleep signal must meet the hold requirement when it is asserted in an active operation cycle. In addition, sleep must be de-asserted in the cycle previous to the next desired operation. All associated setup/hold checks are expected to be met, as they communicate the timing required for the array to enter/exit sleep mode.

During the noop associated with exiting lightsleep, all input signals *must be valid*, setting up to the rising edge of the clock. In other words, Xs on the enables is not allowed during this specific cycle, however Xs on inputs for previous noop cycles is permitted.

7.5.2 Deepsleep Power Scenario

In this mode of operation, the array enters deepsleep when the deepslp signal is asserted. This takes some time to achieve, because a quantity of noop cycles is required upon entering deepsleep before the array fully enters the mode. The number of noops depends upon the over-arching clock frequency but is a static quantity of time for a given array on the order of nanoseconds.

Figure 11. Cycling through Deepsleep

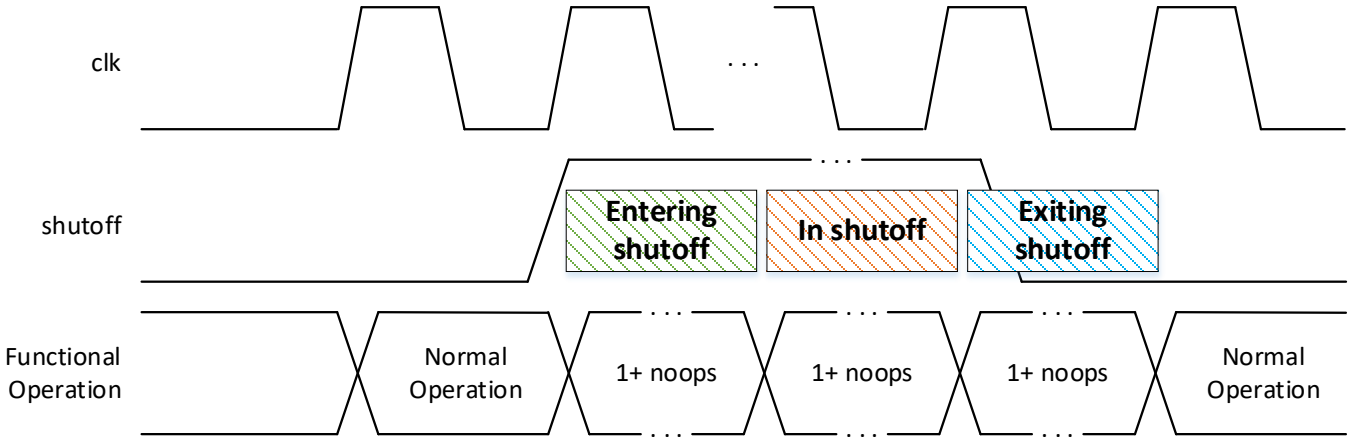


Once the array is in deepsleep, it can remain there indefinitely. When seeking to exit deepsleep, another delay of multiple noops is required to power up the array once deepslp is deasserted. This is done to reduce the peak current during bring-up, as the entire periphery needs to be powered back up. Once the falling hold requirement has been met, the array may be used normally again.

7.5.3 Shut Down Scenario

In this mode of operation, the array enters shutoff when the shutoff signal is asserted. This takes some time to achieve, so some quantity of noop cycles is required upon entering shutoff before the array fully enters the mode. The number of noops depends upon the over-arching clock frequency but is a static quantity of time for a given array on the order of nanoseconds.

Figure 12. Cycling through Shut Down



Once the array is in shutoff, it can remain there indefinitely. When seeking to exit shutoff, another delay of multiple noops is required to power up the array once shutoff is deasserted. This is done to reduce the peak current during bring-up, as the entire array and periphery needs to be powered back up. Once the falling hold requirement has been met, the array may be used normally again.

8 Integration

8.1 Collateral Views

Table 14 shows a list of industry standard collateral views provided for each memory instance, based on release maturity milestone.

Collateral views are validated with QAcockpit flows.

Table 14. Collateral Views Included in the Release

#	View Type	EV	UV	FV
1	Verilog RTL model, including UPF support	Yes	Yes	Yes
2	LEF	Yes	Yes	Yes
3	Liberty NLDM with UPF & POCV support (.lib)	Yes	Yes	Yes
4	Noise overrides (.tcl) are only provided if HIP noise spec is violated	-	-	Yes
5	RV model (Apache Redhawk* AVM)	-	-	Yes
6	LVS netlist (.sp)	-	Yes [1]	Yes
7	Layout (.gds, .oas)	-	Yes [1]	Yes
8	Tessent* MBIST model (.lvlib), Logical to physical map	Yes	Yes	Yes
9	Bit map support (.map)	-		Yes
10	FastScan* ATPG model (.fs_lib), TetraMAX* ATPG model (.max)	Yes	Yes	Yes
11	Instance datasheet (.txt, .html)	Yes	Yes	Yes
12	Compiler data book (.pdf)	Yes	Yes	Yes
13	Release notes (.txt)	Yes	Yes	Yes

Note:

1. No validation of layout and LVS netlist in UV.

8.1.1 Halo Description

Refer to the integration guide documentation listed in section 1.2 for more information.

8.2 Physical Integration

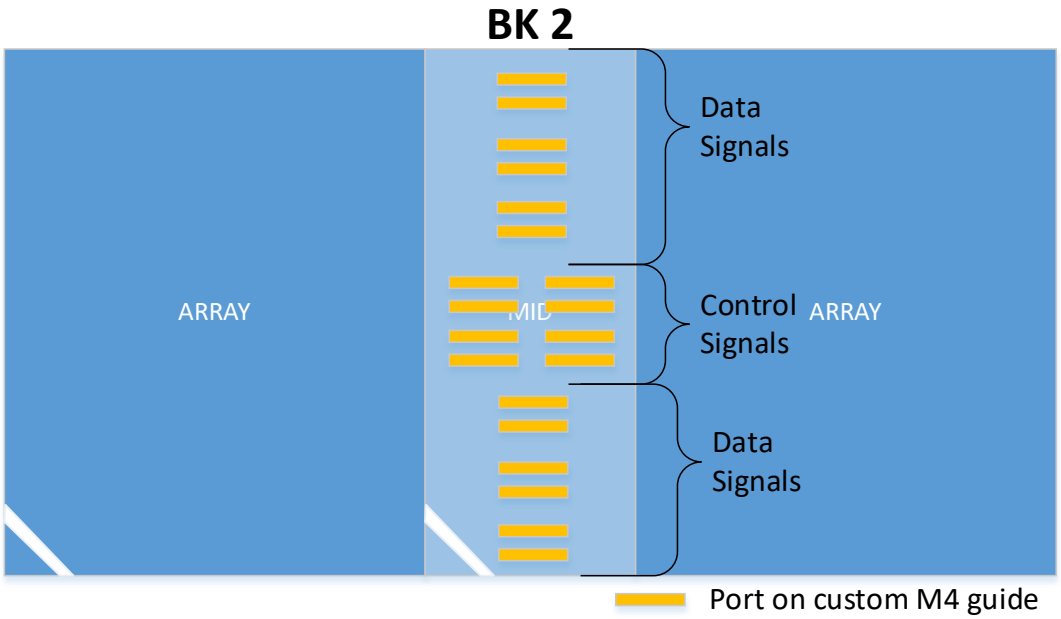
Memory macros are designed to be fully compliant with the Intel Hard-IP (HIP) integration methodology. Table 15 summarizes the integration properties.

Table 15. Physical Array Properties

Property	Description
Layers Used	All metal layers are fully used up to M4
Power Ports	All power ports are on M4. Power ports are not guaranteed to be on SOC power rails. Global power buses must limit IR drop from C4 bump to memory power grid to 5 mV. VDDP: Can be shared with VDD of ASIC VSS: Common ground connection
Signal ports	Signal Ports are on M4. Access to signal ports is only reached by dropping vias from M5. M4 signal ports meet HIP integration specifications.
ESD Requirement	All memory power rails should be compliant with ESD requirements. No ESD protection provided within memory IP.
Decoupling Cap Requirements	Power supply noise must be managed to limit IR drop from C4 bump to memory power pins to 5 mV.
Abutments	Requirements and recommendations detailed in descriptions and figures below.

Both signal and power pins are on M4 and are internal to the macro. The pins are designed to only be accessed by wires routed above in M5. When an UHDLPSPRF macro is placed in the N orientation, the 0,0 origin is in the lower left corner and the signal pins are in specific regions based on the value of Bank as shown in Figure 13.

Figure 13. Pin Placement



8.3 Abutment and Flipping

- Abutment in the X & Y directions is allowed for the SRAM HIP
- UHDLPSPSR HIPs may be flipped over the X, Y, and X and Y axes, without invalidating abutment

Figure 14. Abutment Orientations, Allowed Abutments in X

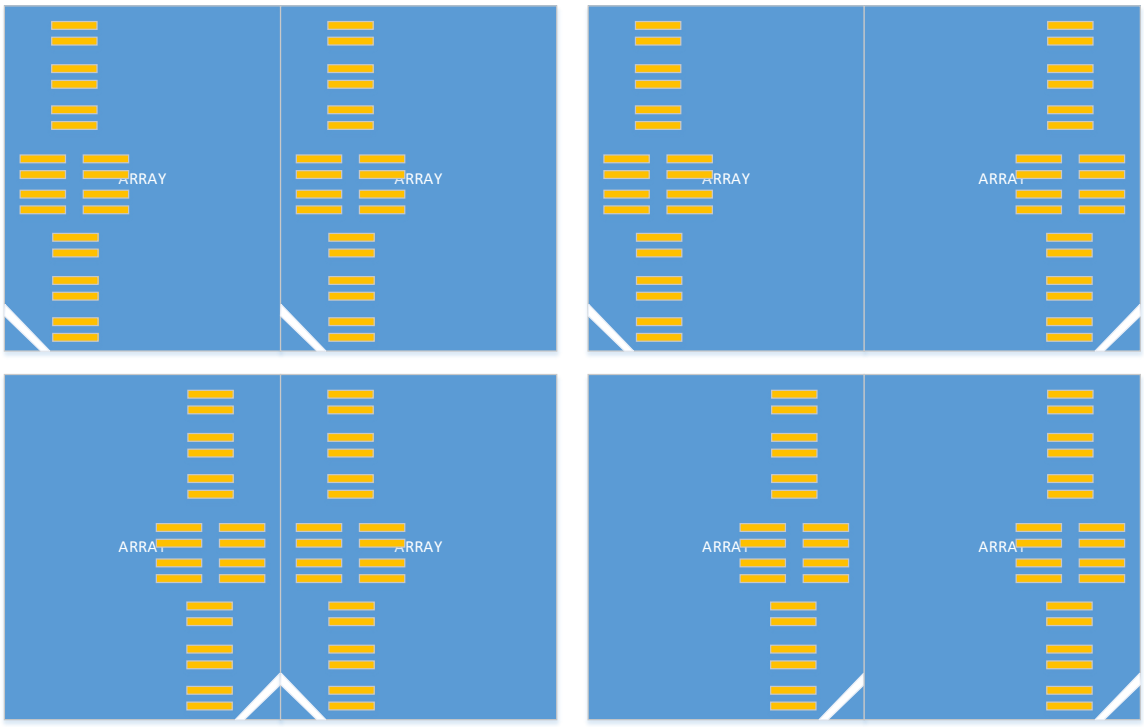


Figure 15. Abutment Orientations, Allowed Abutments in Y

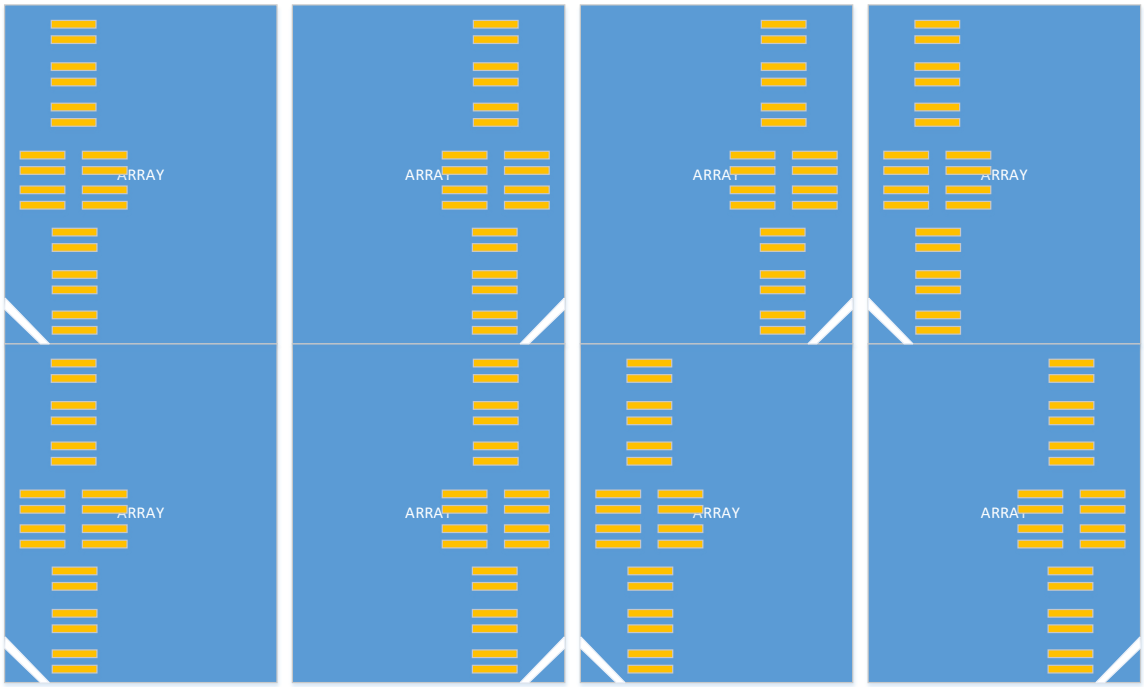


Figure 16. Abutment Orientations, Allowed Abutments in both X and Y

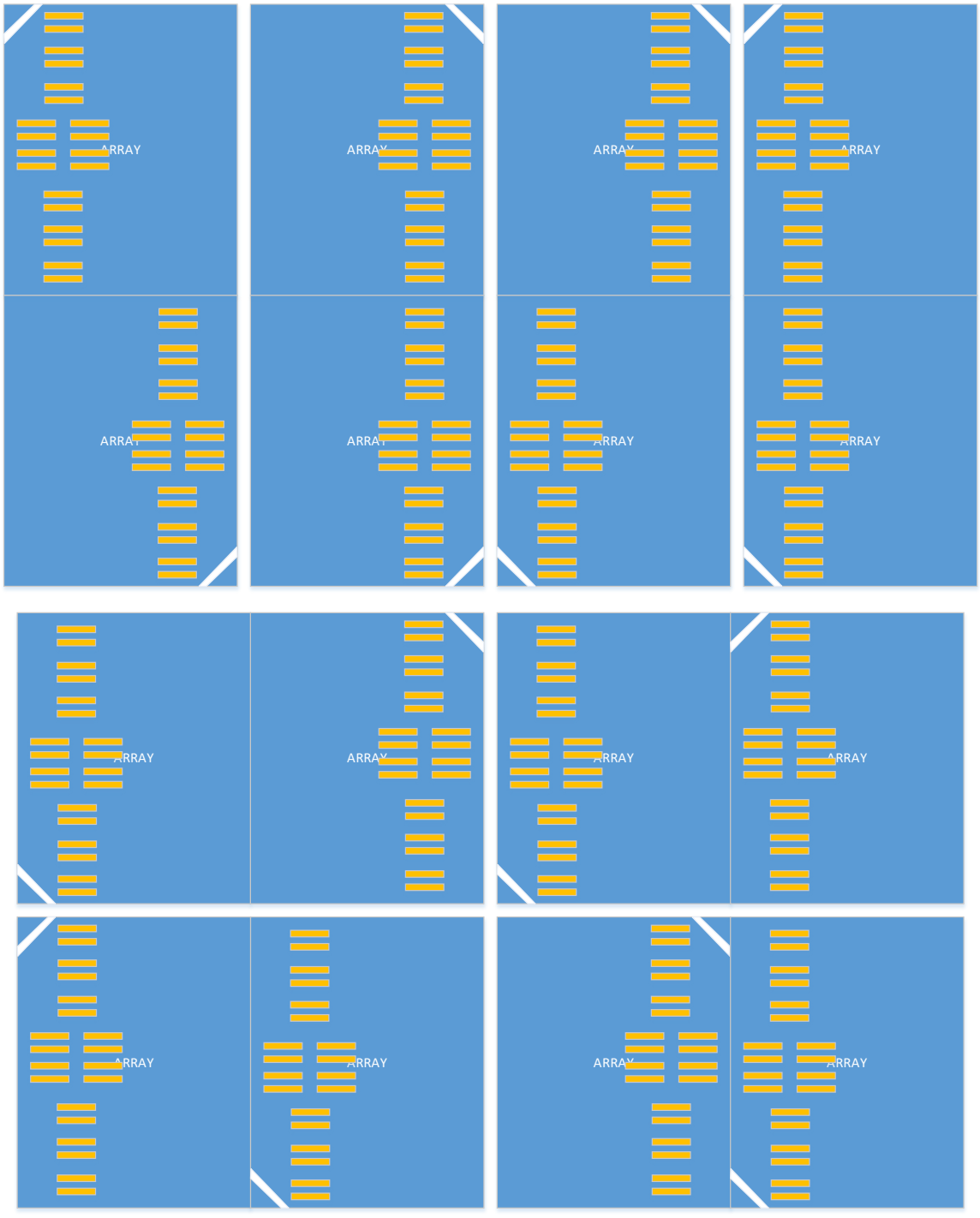
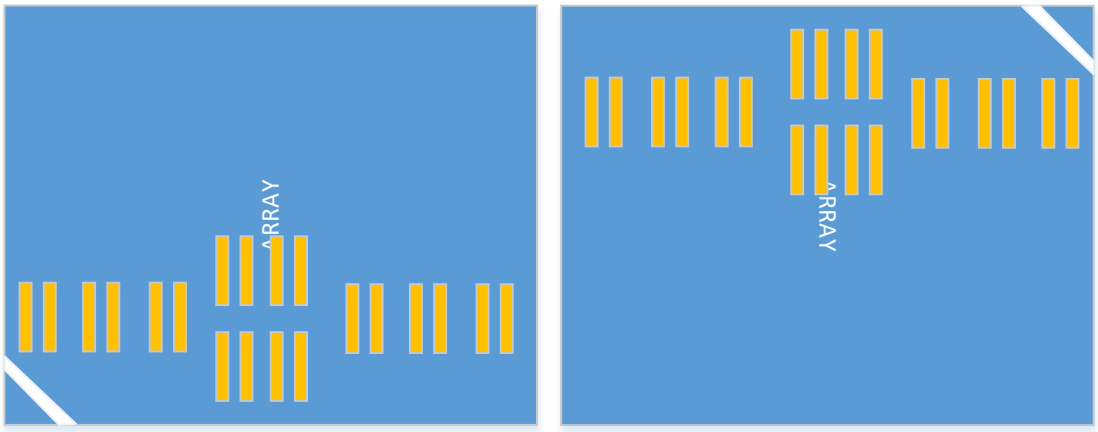


Figure 17. Abutment Orientations, ***Not Allowed***: Rotated (90 or 270 degrees) orientations are not allowed



8.4 MOSFET Device Types Used

Depending on the VT settings for the array, the periphery contains some combination of ulp, lp, lplvt, lvt and nominal devices. NSRHDCLP / PSRHDCLP (NMOS / PMOS SRAM Low-Power) devices are used in the bitcell array.

8.5 Consumption Checklist

The CMO team put together a comprehensive list of paranoia checks based on memory compiler collateral release/consumption milestones to help ensure successful memory integration by SoC teams.

The memory consumption checklist contains various checks to cover the following stages of SoC design flow:

1. Floorplan
2. RTL integration
3. Synthesis
4. UPF flow
5. Place & Route
6. Timing
7. Power
8. Noise
9. RV
10. Tape-in/Signoff

For more details on the memory consumption checklist, contact your Intel representative.

8.6 SRAM Hard-IP Physical Specifications

Each HIP is designed as follows:

- All input/output ports are on metal 4
- Power and ground ports (VDDP, VSS) are on metalVDDP and VSS power tracks are placed throughout the SRAM as per standard SoC guides
- Each HIP is enclosed by a HIP-level white-space buffer, per platform integration rules
- ½ DG_03 (drc_integration) and DG_03 (drcd) errors are expected at IP level but are clean at partition level where 2 SRAMs abut due to a relaxation in the DG_03 length requirement which is built into the runset. For non-abutting edges, the partition level completes the diffCheck (108:0) layer to meet minimum DG_03 length.

9 RV and HVQK/Burn-in Conditions

9.1 RV Conditions

The compiler meets RV specs provided in the Reliability Requirements Document (RRD). Refer to the RRD for RV setpoint conditions.

RV has been validated at the following conditions:

- Max voltage : 0.85 V voltage band
- Max frequency : 1.2 GHz

For any usage above this frequency and voltage band, contact the Intel QRE team.

Note: The ren and wen pins should not be tied high.

The RV analysis was completed assuming lower activity factors on the internal nodes. Setting the ren and wen pins high would break these assumptions, and then the IP will not converge at the RV conditions listed in the RRD document.

9.2 HVQK and Burn-In Test Operating Conditions

CMO requires product teams to switch to self-time bypass mode during HVQK and Burn-In tests by setting the following constraint on clkbyp pin:

- clkbyp = 1

10 BMOD (Behavioral MODel)

The BMOD is a Verilog model designed to emulate the functions of its corresponding hard-IP memory block. This model is presented as a single file with possibly multiple modules and macro defines included. All modules and macros included are uniquified with a memory name prefix and are therefore usable only by the top-level and internal modules contained within the model.

This scenario allows multiple SRAM instantiations of different configurations to be used together without conflict. The BMOD requires no external files to support its use and is therefore the complete representation of the SRAM hard block. Any similarity to macro names found within the BMOD to actual libraries is coincidental and not necessarily intended to match any real synthesis libraries.

10.1 BMOD Features

- Full Emulation of all function modes
  - Normal Operations
    - Read
    - Write, including bit/byte write enable resolution
- Partial emulation of test modes
  - Functional aspects of sleep modes
    - Read/write disabled in these modes
  - All timing and voltage selection inputs are not modeled in the Verilog model
- SDF annotation ready
  - The [IP].sv file contains a specify block and annotation buffers. This view is the default BMOD view. The INTC_FUNCTIONAL define can be used to bypass the timing wrapper functionality.
  - The [IP]_fast_func.sv file contains the same hierarchy, but no specify block or buffers. This model is sometimes known as the FAST FUNCTIONAL model.
- SVA indications of Error and Warning conditions (selectable, on by default)
  - Read/Write (same address, same cycle) collision
  - Address out-of-range
- Verilog messaging, for non-SVA capable simulators, for Error and Warning conditions (selectable, on by default)
  - Read/Write on the same cycle (same address) with X propagation
  - Address out-of-range
- X propagation for hazards
  - Read/Write (same address) collision
    - X read-data and x-write location
  - Address out-of-range
- X propagation in UPF enabled simulations
  - X propagation of appropriate internal registers with power domain shutoff (UPF only)
- Defines for control of simulation modes (refer to section 10.2, BMOD Defines)

- Enabling/disable of power pins in interface
- Controlling timing wrapper

- Tasks for array and output control
  - Array initialization via $readmemh file load, using INTC_MEM_INIT

Table 16. Array Initialization

Task Name	Purpose	Usage	Location in BMOD	Comments
INTC_MEM_INIT	Load from file	INTC_MEM_INIT (filename)	[IP]_DFX_WRP.[IP]. INTC_MEM_INIT	The INTC_MEM_PATH_SIZE define defaults to 256 characters and can be overridden via defparam if a longer or shorter file path size is required.

10.2 BMOD Defines

- INTC_EMULATION: Used to turn on Emulation Mode
- Fault Injection:
  - INTC_MEM_${IP}_fault_norepair/INTC_MEM_fault_norepair, insert non repairable fault
  - INTC_MEM_${IP}_fault_repair/INTC_MEM_fault_repair, insert repairable fault
  - INTC_MEM_${IP}_fault_sing/INTC_MEM_fault_sing, insert single fault
- INTC_SVA_OFF: Controls the assertions that are defined in the RTL.
- INTC_MEM_NOXHANDLING: Turns on/off the X-handling portion of the code.
- INTC_NO_PWR_PINS: Controls the declaration of the power pins(vddp/vss).
- INTC_FUNCTIONAL: Used only in the [IP].sv to bypass the timing wrapper functionality.

10.3 RTL X-Handling

Table 17. RTL X-Handling

Interface signals											Output	
clk	adr	wen	datain	wbeb	ren	bc1/bc2	fwen	shutoff	deepslp	sleep	Array	O/P Data
X											FC	FC
	X	0									NC	NC
	X	1		1							NC	NC
	X	1		0							FC	NC
		X		0							EC	NC
		X									NC	NC
		X		1							NC	NC
		1	X								EC	NC
		1	X	1							NC	NC
		1		X							EC	NC
		0		X							NC	NC
					X						NC	FC
								X			FC	FC
0							X	0			NC	NC
X	X	X	X	X	X		1	0	X	X	NC	NC
								X			FC	NC
											NC	NC
										X	FC	FC
									X		FC	FC
						X	0		1		FC	NC

FC = Fully Corrupted
NC = Not Corrupted
EC = Entry Corrupted

10.4 ATPG Models

Two different ATPG models are included in the delivery: One for FastScan tool, and another one for TetraMAX tool. Only the memory hard block function is described in the ATPG models. DFX wrapper description is not included.

10.4.1 FastScan ATPG Model

The FastScan ATPG model is called "[IP].fs_lib". The array model is written in FastScan model language and utilizes the _cram primitive to model the memory array.

The "<fubname>.fs_lib" file is loaded as the ATPG model for the SRAM HIP in FastScan ATPG environment. The model is simple and straightforward and models all functional features of the SRAM HB's operation. Also, the read/write X propagation found in the BMOD is present in the ATPG model and will therefore provide X output in FastScan tests that attempt to read and write at the same time. This will prevent real silicon failures where the output of the memory and contents of the ARRAY will be undetermined due to the read/write collision.

10.4.2 TetraMAX ATPG Model

The TetraMAX ATPG model is called "[IP].max". The ATPG memory functional model is written in structural Verilog.

The "[IP].max" file is loaded as ATPG model for the SRAM HIP in TetraMAX ATPG environment. The model is simple and straightforward and models all functional features of the SRAM HB's operation. Also, the read/write X propagation found in the BMOD is present in the ATPG model

and will therefore provide X output in TetraMAX tests that attempt to read and write at the same time. This will prevent real silicon failures where the output of the memory and contents of the ARRAY will be undetermined due to the read/write collision.

10.5 DFx Wrapper Model

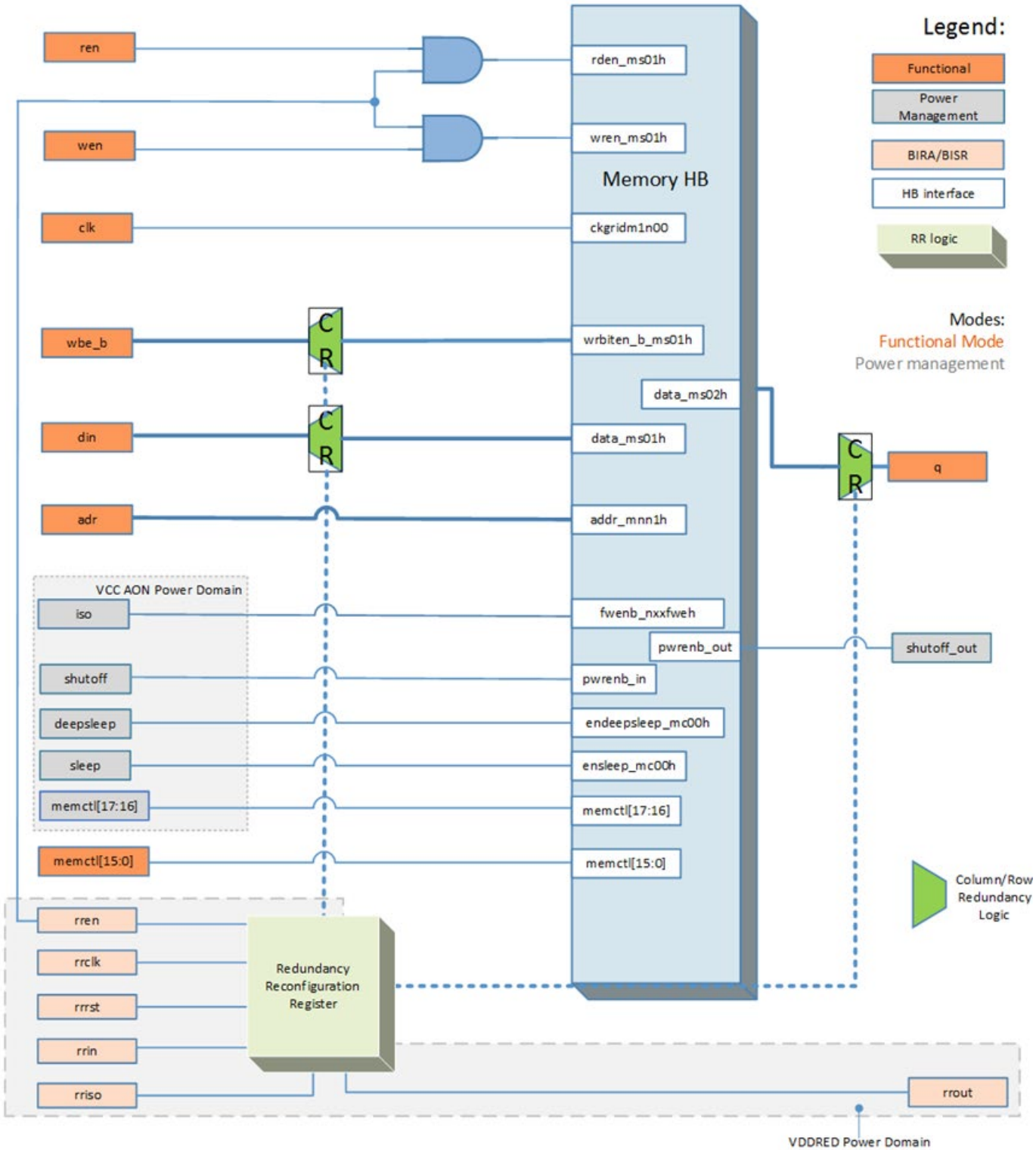
A synthesizable RTL wrapper model is provided for SoC level integration. This model supports the following modes:

- Functional
- Power management
- Column Redundancy

Note: Integration must recognize the capture flops connected to Always-On power domain signals to implement the proper level-shifter requirements.

DFx wrapper model logic is described in Figure 18.

Figure 18. DFx Wrapper Model



10.6 Repair Mechanism

10.6.1 DFx Wrapper Redundancy (Column)

SRAM repair guidelines vary between projects based on a variety of factors such as unit memory size, process, operating voltage, temperature, and more and as such are beyond the scope of this document. This section describes the compiler redundancy functionality for column. Each project should consult their QRE team for specific repair guidelines to meet yield and minimum voltage distribution goals.

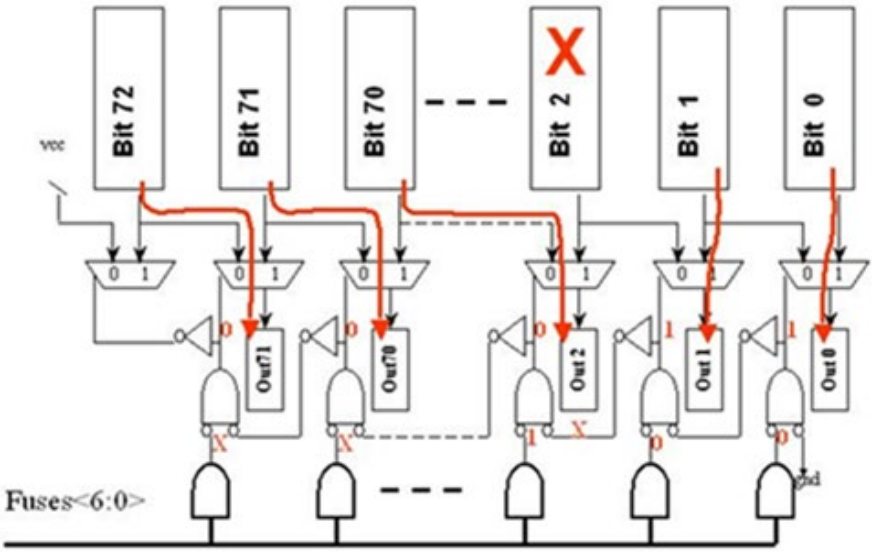
Table 18. rrbus Field

rrbus (DFX_MISC_SSA_REG)	BMOD Function	Comments
rrbus[credbits:0]	Repair column address	Credbits is the number of address bits to select column repair position and includes the enable bit
rrbus[credbits+1]	Repair column enable	

SRAMs can have additional bits to support column redundancy. Column redundancy logic is implemented outside the SRAM using a soft wrapper; additional I/O(s) are added in the hard memory to support the soft wrapper. The bit shift logic for column redundancy implementation is shown below.

Each column redundancy implementation requires (log2D + 1) fuse bits; log2D bits represent the faulty column, these bits are decoded to generate D control signals to select the bit-shifting muxes. D is the number of data bits in the SRAM. The extra fuse bit is for column redundancy enable. For example, a 2048x64 SRAM requires log2(64) + 1 = 7 fuse bits to implement a single column redundancy.

Figure 19. Bit Shifting Replacement Logic



Observations:

- Suppose bit 2 'slice' is found to have a defect needing repair.
- Assuming there are no defects in bit 0 'slice', bits 72:3, and 1,0 now provide the actual data as depicted by the arrows.
- All the redundant mux control logic is DC and therefore 'set-up' before data arrives at the mux.
- Because the redundant muxes only span a distance of 1 bit, there is a really minimal mux delay added to the data path.
- Writing data is not depicted but is also muxed using the same control circuits.

For the DFx wrapper, users can turn off column redundancy by simply ordering a memory without column redundancy and implement their own logic for column redundancy outside the wrapper. The memory must be ordered as wide as needed to provide the extra column(s) worth of redundant elements that are used as redundant columns. Also, logic must be placed to implement the column redundancy scheme desired. Note that turning off the built-in column redundancy logic for a memory that was ordered with column redundancy will NOT make the extra column in the HB available at the DFx wrapper interface! Also, turning on the built-in column redundancy logic for a memory that was ordered without column redundancy will result in connection errors! One possible need to implement column redundancy outside the DFx wrapper would be for sharing logic over many memories, resulting in a smaller logic footprint.

For DFx wrappers, column redundancy is only an order time option. However, a user can still provide their own column redundancy solution by ordering the desired memory, without the column redundancy option selected, and asking for a wider memory to accommodate the extra needed I/O column(s).

If customer provides their own column redundancy, then care must be taken to mux both the data I/O and the bit write enable inputs.

Reconfiguration registers hold repair information including fault address and repair enable. The fuse bits with repair information are downloaded to reconfiguration registers to enable appropriate repair.

Figure 20 and Figure 21 describe reconfiguration register timing and scan sequence details.

Figure 20. Reconfiguration Register Timing Diagram

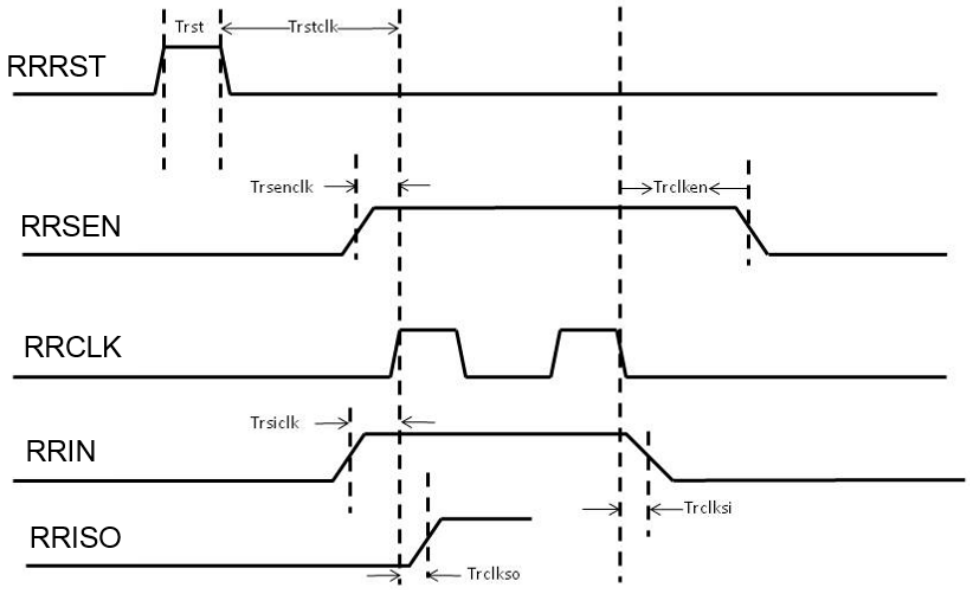


Figure 21. Reconfiguration Register Scan Sequence

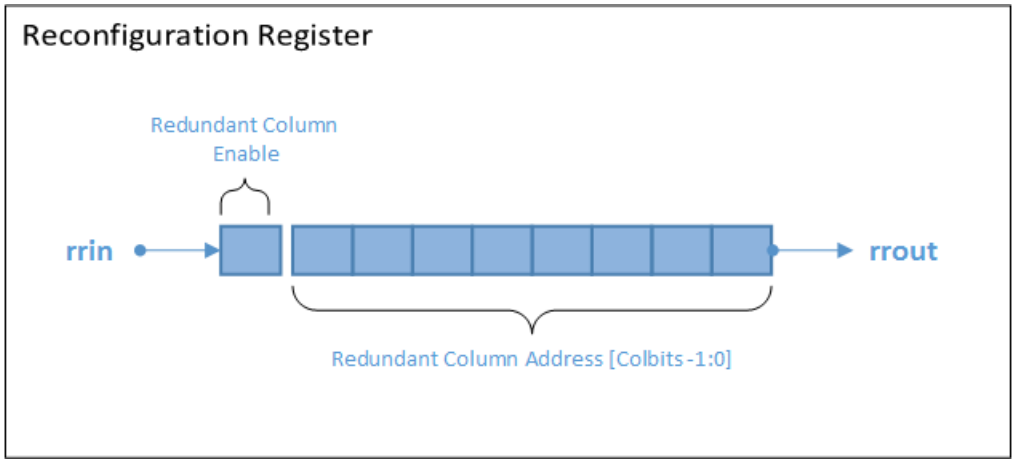


Table 19 contains SRAM redundancy repair operation truth table.

Table 19. Truth Table for 1RW SRAM Redundancy Repair Operation

Function	rriso	rrrst	rren	rrclk	rrin	rrout
Normal	1	X	X	X	X	NC
Normal	0	0	0	X	X	NC
Redundancy Scan	0	0	1	0->1	Fuse Data	Shifted Address (lower column LSB)
Reset	0	1	X	X	X	Reset (All other bits in the reconfiguration register are also reset)

10.7 Frontend Model Views

Table 20. Frontend Model Views

View	Description
[IP].f	BMOD simulator file list
[IP].sv	BMOD with integral timing wrapper
[IP]_DFX_WRP.f	DFX wrapper simulator file list
[IP]_DFX_WRP.sv	DFX wrapper
[IP]_fast_func.sv	BMOD without timing wrapper
[IP]_fast_func.f	Fast Func simulator file list
[IP].upf	Universal Power Format for BMOD
upf_global_defs.tcl	This tcl file defines the supply variable
[IP].fs_lib	FastScan ATPG Model
[IP]_fastscan.do.cat	FastScan dofile
[IP].max	TetraMAX ATPG Model
[IP].lvlib	MBIST Logic Vision Model

The file structure is shown below:

rtl

```
|-- [IP].f
|-- [IP].sv
|-- [IP]_DFX_WRP.f
|-- [IP]_DFX_WRP.sv
|-- [IP]_fast_func.f
|-- [IP]_fast_func.sv
```

lvlib

```
|-- [IP].lvlib
|-- [IP]_DFX_WRP.lvlib
```

atpg

|-- models

```
|   |-- [IP].No_Fault_List
|   |-- [IP].fs_lib
|   |-- [IP].max
|   |-- [IP]_DFX_WRP_scan_exceptions.tcl
|   |-- [IP]_fastscan.do.cat
```

|-- bitmap

```
|-- [IP]_mbist.map
|-- [IP]_spbist.map
```

upf

```
|-- [IP].upf
|-- upf_global_defs.tcl
```