ECE1388

Final Project (tentative)

1. Summary and Goal

The final project guides student teams through a simplified practical flow of a complete integrated circuit (IC) design starting from the project definition and system outline to the complete verified IC layout including a padframe. The project aims to help students apply skills learned in this course and other courses to the design of a die-level CMOS integrated circuit (a.k.a. "chip").

The function of the chip is that of students' choice subject to limitations described below in the "Scope" section.

The goal of the project is for students to develop/polish and demonstrate a number of skills including but not limited to:

- understanding and mastery of the IC design flow as described herein
- knowledgeable utilization of all course material within the final project
- performing optimal circuit and layout design as part of an IC design flow
- demonstrated ability to work efficiently within an IC design team
- ability to communicate results effectively by way of oral presentations/ updates
- understanding all presentations and participation by asking/answering questions.

2. Milestones

The final project runs between the 7^{th} and the 14^{th} weeks of the course with the following tentative schedule:

Week	Topic	Format
7	Group formation and project definition	*Project launch and discussion*
8	System outline	*Short written update 1*
9	Circuit cells and simulations	*Initial presentation (covers weeks 7-9)*
10	Complete schematic	*Short written update 2*
11	Cell layout	*Short written update 3*
12	Complete layout within a pad frame	*Final presentation (covers all weeks)*
14	LVS final check and final report	*Final report submission to a TA*

3. Scope

The project focuses on the flow of the design of a complete CMOS integrated circuit chip. A default technology of choice will be announced in class. A padframe library for this technology including both cell schematics and layouts will be provided. Students should plan to utilize no more than approximately $4mm^2$ area in this technology (including the padframe). Certain deviations from this area guideline are permitted with proper justification.

A degree of freedom in choosing the function(s) and specifications of the chip is allowed, subject to the instructor's approval during/before the first week of the project. If you are looking for a project idea, please choose from manuscripts from the following publications only:

IEEE Transactions on Biomedical Circuits and Systems
IEEE Biomedical Circuits and Systems Conference
IEEE Journal of Solid-State Circuits
IEEE International Conference on Solid-State Circuits
IEEE Spectrum
Science
Nature

Please do not select papers that are more than 6 years old. Any paper that is older or is chosen from another conference/journal will need to be approved by the instructor on a case-by-case basis.

4. Presentations and written updates format

Oral presentations should be in the form of *high-quality well-polished* slides with key messages clearly and concisely presented. Each presentation will be short (approximately 3 to 10 minutes per team depending on the number of groups). So it is important to focus your presentation and only present the most important information. You may find if useful to practice your presentation before the class.

In each presentation, please order your slides to answer the following three key questions in this order:

- What?
    - E.g., what are you doing?
    - Tip: it helps to give a brief tutorial on the subject to introduce the subject
- Why?
    - E.g., why are you doing this?
    - Tip: the question "Why?" is most often overlooked.
        - 1. Explain why the topic you choose is important and where the proposed IC is used (imaging explaining this to your grandparents).
        - 2. Explain how your approach differs from a conventional one, by describing the latter first.
- How?
    - E.g., how you will go about doing this?
    - Here you can present your approach

Please see section "Group formation and project definition" for an example of such an organization.

In each presentation/written update please include *three* references to *specific topics* covered in the lecture notes (lecture week and page #) or a corresponding textbook (Section # and page #), mark it with a BIG green checkmark symbol and state the textbook chapter and page(s) number(s). Every presentation/written update should include three checkmarks on *new* (non-repeating) topics. By week 12 you should have

demonstrated that you've utilized at least 70% of the course lecture material topics in your design.

Every week please submit a *stapled* hardcopy of your slides or written update (as applicable) to the instructor in the beginning of the class (if using dark background for slides, please do not print it).

Additional presentation information is provided in "Presentation Tips" section.

Written updates can follow the same format and should be short (no more than 10 slides). They should not include much text, other than short sentences organized hierarchically with bullets. Inclusion of images is encouraged.

5. Guidelines

5.1. Group formation and project definition

Students should work in team unless approved otherwise by the instructor (team size is announced in class each year and depends on enrollment). Each team designs one chip. The project work should be divided approximately uniformly among all team members. This applies to the work done both outside the class meeting times and during class presentations/reporting.

Each team has to come up with a project definition. The project definition should include:

- the project title
- targeted function(s) performed by the chip (*what do you propose to do*?)
- detailed specifications of the chip (*what specifically do you propose to achieve*?)
- proposed applications / impact / importance / motivation / rationale (*why do you choose to do this*?)
- rough block diagram of the chip (*how do you propose to accomplish the proposed by means of a VLSI architecture*?)
- rough floorplan of the chip (*how do you propose to accomplish the proposed by means of a VLSI layout implementation corresponding to the VLSI architecture*?)
- references to any relevant sources of information should be made on all slides that use information from other sources (e.g., a footnote containing: authors, manuscript name, location of research). *No existing material can be reused without a proper reference.*

Some level of guessing in defining rough block diagram and floorplan is allowed at this stage in the project as long as some thought is given to them. Qualitative rather than qualitative treatment of these is sufficient at this stage. These are to be refined in the next phases of the project (and usually require some experience and iteration back from the layout phase).

5.2. System outline

First, refine/repeat the information covered in "*Group formation and project definition*" section above in a compact and concise way. Do not forget to include motivation for your project topic choice in each update/presentation. Next, consider some key points regarding the system outline milestone as described next.

Define the refined block diagram of the chip you want to implement, with the functional description of the major parts (e.g.: integrator, multiplier, etc). The description

should be fully quantitative with clear specification of where signals flow (What is input and output, and how components are interfaced?) and how data is handled (analog, digital, continuous-time, discrete). Find values or ranges of operational values for any parameters governing the system (e.g. coefficients of filters), and analyze the operation at the system level (What are the output waveforms and intermediate waveforms for given input waveforms?). When in doubt or certain parts are not clearly defined or optimized at the system level, do some necessary simulations (at the block-diagram level).

Define the refined floor plan of the chip you want to implement. Place all major functional blocks of the system within the padframe and state their approximate dimensions. Here you can rely on your own or existing estimates of the size of layouts of your functional blocks. You will need to open the padframe library in order to obtain pad cell dimensions and to see an example of pad organization in a padframe. You should show how you propose to organize pads in your own padframe (as long as it is rectangular).

Tips: show refined system block diagram, with quantitative description of operation including I/O and interfacing waveforms (obtained from top-level simulations, if necessary); show refined floor plan.

5.3. Circuit cells and simulations

Come up with (elegant) circuits implementing parts of the system (e.g. amplifiers, integrators, modulators, ...). Retain the hierarchy and organizational structure of the block diagram level design. Make sure signals interface properly (in format, impedance, and in timing) between different circuit cells, according to the arrangement of the blocks. Define all bias levels (or how they are constructed from other supplied bias levels through additional bias circuitry) and voltage or current waveforms used in the timing and control of the circuits. Simulate the design.

Tips: clearly annotate the circuit diagrams and corresponding signal diagrams of all cells used to represent the functional blocks in your system, retaining the hierarchical structure. Define bias levels and signal / control waveforms, and include simulation results. Keep showing the system block diagram (or floorplan) on each presentation slide (e.g., in a corner) and highlight on it the block being presented in a current slide.

5.4. Complete schematic

Arrange instances of the cells combining to construct the overall system and implement all its functions. Pay much attention to the detail of correctly interfacing the circuit blocks, and make sure the design reflects the hierarchical and modular structure of the system-level block diagram. Typically, the amount of circuitry needed to interface all blocks together should be much smaller than the actual circuitry contained within the circuit blocks themselves.

Tips: Same as the cell-level design, but now at the top-level of the hierarchy. Keep showing the system block diagram (or floorplan) on each presentation slide (e.g., in a corner) and highlight on it the block being presented in a current slide. Use vectorized instances for arrays of cells and buses when appropriate (e.g., a 16x8 array of SRAM cells should be shown as one symbol with an instance label showing that it is instantiated in a 16x8 array).

5.5. Cell layout

Layout key cells in Cadence using Analog Artist.

Make sure the cells abut properly when later combined together (e.g. as instances in an array). There should be a sufficient number of Vdd and GND connections to wells and substrate (one bulk contact per 5 or fewer transistors connecting to that bulk). Lines should be sized according to the amount of current they need to accommodate. While short lines locally connecting gates can be poly, lines that carry current or that need to respond fast to voltage changes should be metals. For large-scale signal interconnect on a 2-D grid, use odd metals horizontally and even metals vertically (or vice versa) and make sure to be consistent in order to avoid cross-over via bridges.

Tips: Label the I/O interfaces and signal/power lines of all cells with meaningful names (GND, Vdd, CARRY, Vin, Iout,...) which conform with the schematic. Run a DRC on the layout file for each cell. Then run LVS on the layout and schematics files, and correct the layout vs. the schematics until both converge. To your advantage, you should start running DRC and LVS on the cells in the earliest stages of the layout. Keep showing the system block diagram (or floorplan) on each presentation slide (e.g., in a corner) and highlight on it the block being presented in a current slide.

5.6. Complete layout within a padframe and final project presentation

Combine the cells in the layout to implement the complete schematics as previously defined, and add the interfacing circuitry at appropriate levels in the hierarchy of cells. Retain the structure of the schematics, with coinciding names for the cells in the layout and the subcircuits in the schematic. Make sure to interconnect power and signal lines correctly, with power lines (GND, Vdd, ...) having a large width. Use shielding for sensitive signals.

Include the total layout in a pad frame (provided) and route the external pin connections. Keep in mind the useful area that you can fill up with your circuits to fit within the padframe. Avoid wasting silicon area. Is your chip area core-limited or pad-limited? You are not required to complete top-level DRC or LVS at this stage but should show your chip core layout within a padframe, even if not wired up to it yet.

Every group should give a final presentation in class focusing on the final product – the complete chip and including key points from the entire project.

5.7. LVS final check and final report

Run a complete DRC on the entire chip layout file. Then run LVS on the complete layout and schematics files, and correct the layout vs. the schematics until both converge. To your advantage, you should start running LVS and DRC on the cells in the earliest stages of the layout. The final LVS check also marks the end of the project (approximately two weeks after the final project presentations). You have the chance to make changes according to discussions in class, etc.

Every project group will generate a final report (2 pages or text, plus figures including schematic diagrams, layouts or key blocks and the entire chip) in electronic format (see below), describing the chip. It should be clear from the report what the chip is supposed to do, and who did exactly what in the project. The report should be to the

point, with as little general background formulation and as much chip specifics as possible. Please include the final LVS report results page.

Electronic format: The report needs to be submitted as a hardcopy and in HTML format to the TA, and needs to include all graphics and other referenced documents. All class reports may be posted on the web, accessible from the class web page. The total size of your submission can not exceed 2MB (save all images at a monitor resolution). Also send a pointer to your Cadence library to the TA. Make sure to use a library name that is representative of your project.

6. Presentation Tips

- Include names of all presenters on the first slide, and next to the name: a photo of each presenter so names are easy to remember by everyone, the program the presenter is enrolled in (e.g., PhD), his/her group (e.g., electronics), and university where the previous degree was obtained.

- Number your slide pages

- Do not use acronyms in the title

- Min font size in slides is 16

- Do not make slides overly verbose and do not try to fit all unimportant details about your project into the slides.

- Bullets: one line of text per bullet (no text paragraphs)

- Every borrowed figure should include a citation to the source at the bottom of the page (actual authors, paper name, journal name, do not use [1], [2], etc)

- Each presenter should use up the same time (e.g., 1min per person - this time will be assigned in class for each upcoming presentation)

- Do not have more than 2 (3 max) slides per minute

- If the presentation generates questions from audience members who got sincerely interested in the subject as a result of the presentation, this is a bonus for the presenters.

- Please use a pointer when presenting

- Each week remind the audience *what* you are doing and *why*. Do not skip this.

- When presenting cell schematics/layouts, keep showing the system block diagram on each slide (e.g., in a corner) and highlight on it the block being presented in a current slide.

- When presenting schematics, consider redrawing circuits in a circuit drawing program (e.g., Visio or Xcircuit). You can try capturing Cadence schematics but make sure those are not too busy. This means use three-terminal, not four-terminal MOS symbols to avoid drawing bulk connection wires that obscure the view, turn off labels for the symbol instance number and other irrelevant labels of MOS symbols.

- When presenting layouts, make sure that it can be properly seen (ideally bring it to white background, zoom in sufficiently close, etc)

- Bring a watch to time yourself. When the time is up and a bell rings, you have to wrap up you presentation with 2-3 sentences.

7. Evaluation

Quality of delivery/engagement: oral presentations, written updates, presence in class (including no late arrivals), class participation (questions/comments to presenters)	50 %
Technical content: system design, circuit schematic, layout, DRC, LVS and final report	50 %