

Summary (Part 1.4)							
Design Functional Description	Path Logical Effort - G	Path Parasitic Delay - P	Path Delay - D	Area in Lambda - Al	Area in Microns - Am	Dynamic Power Dissipation - Pd	Power Delay Product - PD
INV-NAND5	2.33	6	59.55	60944.00	12188.80	0.000226291	0.013474788
INV-INV-NAND5	2.33	7	33.85	133056.00	26611.20	0.001889997	0.063973599
INV-NAND3-INV-NAND2	2.22	7	27.45	79696.00	15939.20	0.000972526	0.026692128
INV-INV-NAND3-INV-NAND2	2.22	8	26.44	152064.00	30412.80	0.001739192	0.045987999
INV-INV-INV-NAND3-INV-NAND2	2.22	9	26.80	154112.00	30822.40	0.002637234	0.070688623

Design Functional Description	F	f^A	Df	Path Delay - (seconds)	
INV-NAND5		716.80	26.77	53.55	1.66E-09 1660ps
INV-INV-NAND5		716.80	8.95	26.85	9.42E-10 942ps
INV-NAND3-INV-NAND2		682.67	5.11	20.45	7.63E-10 763ps
INV-INV-NAND3-INV-NAND2		682.67	3.69	18.44	7.36E-10 736ps
INV-INV-INV-NAND3-INV-NAND2		682.67	2.97	17.80	7.46E-10 746ps

Part 3.3 (Summary Part 2 and Part 3 Simulation Results)			
	Part 2 Results		Part 3 Results
2.2 Circuit Delay	1.45E-09	1.45us	1.07E-09 1.07us
2.3 Total Power Dissipation	1.05E-03	1.05mW	6.35E-04 635uW
2.4 Static Power Dissipation	6.78E-09	6.78nW	3.64E-09 3.64nW
2.5 Dynamic Power Dissipation	1.05E-03	1.05mW	6.35E-04 635uW

2 Stage Design	G	P	F	f^	Df	D	Path delay (seconds)	Al	Am	Pd	PD	
INV-NAND5	2.33	6.00		716.80	26.77	53.55	59.55	1.66E-09	60944.00	12188.80	2.26E-04	1.35E-02
B	16.00		tau		2.78E-11	R	6100.00					
H	19.20					C	1.52E-15					

Stage	g	f^A	Branching of Cout	Cout	Cin	P/N Ratio	
1. INV		1.00	26.77	16.00	16.73	10.00	2.00
2. NAND5		2.33	26.77	1.00	192.00	16.73	0.40

1. INV Size

p constant	n constant	constant		
1.00	-2.00	0.00	p	6.66666667
1.00	1.00	10.00	n	3.333333333

Activity Factor (α)	0.1
frequency (f)	1.00E+07
Vdd	3.3
Unit Cap	1.00E-15

2.NAND5 Size

p constant	n constant	constant		
1.00	-0.40	0.00	p	4.78
1.00	1.00	16.73	n	11.95

Power				
Node	Branchout	Unit Cap	P/N multiplier	Pswitching (W)
INV out node	16.00	115	3.33	4.17E-06
NAND5 out node	1	207	2.39	2.25E-06
Total Per wordline				6.43E-06
Wordlines	32			2.06E-04
Shot Circuit Power		110% Total		2.26E-04

Stick Diagrams

Brief Description: 10 inverters at the top left corner, stacked NAND5s on the right

	W - tracks	H - tracks		
NAND5	6	9	Total W - tracks	26
INV	2	5	Total H - tracks	293
Lambda	0.2		Total Area - lambda	60944
Lambda per track	8		Total Area - um	12188.8

3-stage	G	P	F	f^	Df	D	Path Delay (seconds)	Al	Am	Pd	PD
INV-INV-NAND5	2.33	7.00	716.80	8.95	26.85	33.85	9.42E-10	133056	26611.2	1.89E-03	6.40E-02
B	16.00	tau	2.78E-11	R	6100.00						
H	19.20			C	1.52E-15						

Stage	g	f^	Branching of Cout	Cout	Cin	P/N Ratio
1. INV	1.00	8.95	1.00	89.49	10.00	2.00
2. INV	1.00	8.95	16.00	50.06	89.49	2.00
3. NAND5	2.33	8.95	1.00	192.00	50.06	0.40

1. INV 2/1

p constant	n constant	constant		
1.00	-2.00	0.00	p	6.67
1.00	1.00	10.00	n	3.33

Activity Factor (α)	0.1
frequency (f)	1.00E+07
Vdd	3.3
Unit Cap	1.00E-15

Power

2. INV 2/1

p constant	n constant	constant		
1.00	-2.00	0.00	p	59.66
1.00	1.00	89.49	n	29.83

Node	Branchout	Unit Cap	P/N multiplie	Pswitching (W)
INV out node	1	6	3.33	2.18E-07
INV out node	16.00	115	29.83	3.74E-05
NAND5 out node	1	207	7.15	1.61E-05
Total Per wordline				5.37E-05
Wordlines	32			1.72E-03
Shot Circuit Power		110%	Total	1.89E-03

3. NAND5 2/5

p constant	n constant	constant		
1.00	-0.40	0.00	p	14.30
1.00	1.00	50.06	n	35.75

Stick Diagrams

Brief Description: 10 sets of stacked inverters at the top left corner, stacked NAND5s on the right

W - tracks H - tracks

NAND5	6	9 Total W - tracks	56
INV-INV	5	9 Total H - tracks	297
Lambda	0.2	Total Area - lambda	133056
Lambda per track	8	Total Area - um	26611.2

4-stage	G	P	F	f^	Df	D	Path Delay (seconds)	Al	Am	Pd	PD
INV-NAND3-INV-NAND2	2.22	7	682.67	5.11	20.45	27.45	7.63E-10	79696	15939.2	9.73E-04	2.67E-02
B	16.00	tau	2.78E-11	R	6100.00						
H	19.20			C	1.52E-15						

Stage	g	f^	Branching of Cout	Cout	Cin	P/N Ratio
1. INV	1.00	5.11	16.00	3.20	10.01	2.00
2. NAND3	1.67	5.11	1.00	9.80	3.20	0.67
3. INV	1.00	5.11	1.00	50.10	9.80	2.00
4. NAND2	1.33	5.11	1.00	192.00	50.10	1.00

1. INV

p constant	n constant	constant	
1.00	-2.00	0.00	p
1.00	1.00	10.00	n

2. NAND3

p constant	n constant	constant	
1.00	-0.67	0.00	p
1.00	1.00	3.20	n

3. INV

p constant	n constant	constant	
1.00	-2.00	0.00	p
1.00	1.00	9.80	n

4. NAND2

p constant	n constant	constant	
1.00	-1.00	0.00	p
1.00	1.00	50.10	n

Stick Diagrams

Brief Description: 10 inverters at the top left corner, stacked NAND3-INV-NAND2s on the right

	W - tracks	H - tracks	
NAND3-INV-NAND2	14	9	Total W - tracks 34
INV	2	5	Total H - tracks 293
Lambda	0.2		Total Area - lambda 79696
Lambda per track	8		Total Area - um 15939.2

Activity Factor (α)	0.1
frequency (f)	1.00E+07
Vdd	3.3
Unit Cap	1.00E-15

Power

Node	Branchout	Unit Cap	P/N multiplie	Pswitching (W)
INV out node	16	8	3.33	2.90E-07
NAND3 out	1.00	12	0.64	8.36E-08
INV out node	1.00	7	3.27	2.49E-07
NAND2 out	1	198	12.52	2.70E-05
Total Per wordline				2.76E-05
Wordlines	32			8.84E-04
Shot Circuit Power		110%	Total	9.73E-04

5-stage	G	P	F	f^	Df	D	Path delay (seconds)	Al	Am	Pd	PD	
INV-INV-NAND3-INV-NAND2		2.22	8.00	682.67	3.69	18.44	26.44	7.36E-10	152064	30412.8	1.74E-03	4.60E-02
B	16.00		tau	2.78E-11	R		6100.00					
H	19.20				C		1.52E-15	assuming 1fF/um				

Stage	g	f^	Branching of Cout	Cout	Cin	P/N Ratio	
1. INV		1.00	3.69	1.00	36.82	9.98	2.00
2. INV		1.00	3.69	16.00	8.49	36.82	2.00
3. NAND3		1.67	3.69	1.00	18.80	8.49	0.67
4. INV		1.00	3.69	1.00	69.38	18.80	2.00
4. NAND2		1.33	3.69	1.00	192.00	69.38	1.00

1. INV

p constant	n constant	constant		
1.00	-2.00	0.00	p	6.65
1.00	1.00	9.98	n	3.33

Activity Factor (α)	0.1
frequency (f)	1.00E+07
Vdd	3.3
Unit Cap	1.00E-15
Power	Assuming unit capacitance is 1fF

2. INV

p constant	n constant	constant		
1.00	-2.00	0.00	p	24.55
1.00	1.00	36.82	n	12.27

Node	Branchout	Unit Cap	P/N multiplier	Pswitching (W)
INV out node	1	6	3.33	2.17E-07
INV out node	16.00	83	12.27	1.11E-05
NAND3 out	1.00	12	1.70	2.22E-07
INV out node	1.00	7	6.27	4.78E-07
NAND2 out	1	198	17.34	3.74E-05
Total Per wordline				4.94E-05
Wordlines	32			1.58E-03
Shot Circuit Power		110% Total		1.74E-03

4. INV

p constant	n constant	constant		
1.00	-2.00	0.00	p	12.53
1.00	1.00	18.80	n	6.27

5. NAND2

p constant	n constant	constant		
1.00	-1.00	0.00	p	34.69
1.00	1.00	69.38	n	34.69

Stick Diagrams

Brief Description: 10 sets of stacked inverters at the top left corner, stacked NAND3-NAND2-INVns on the right

	W - tracks	H - tracks		
NAND3-INV-NAND2	14	9	Total W - tracks	64
INV-INV	5	9	Total H - tracks	297
Lambda	0.2		Total Area - lambda	152064
Lambda per track	8		Total Area - um	30412.8

Schematic Simulation

Total Avg Power		Avg Static Power consumption over each address	
		Address	uW
pa<0>	1.10E-06	0	7.013
pa<1>	4.52E-06	1	7.796
pa<2>	6.24E-07	2	7.643
pa<3>	3.00E-07	3	7.682
pa<4>	1.15E-07	4	6.173
pab<0>	6.94E-06	5	6.317
pab<1>	2.97E-06	6	6.539
pab<2>	3.44E-08	7	6.207
pab<3>	2.32E-07	8	6.656
pab<4>	6.83E-08	9	6.718
Supply power	1.04E-03	10	8.313
Total	1.05E-03	11	6.847
		12	6.54
		13	6.857
Calculated Switching power		14	6.539
1.74E-03		15	6.532
Simulated Total Power		16	6.783
1.05E-03		17	7.274
Simulated Static Power		18	6.518
6.78E-15		19	6.991
Estimated Switching Power from Simulation		20	6.535
1.05E-03		21	5.348
Theories on differences		22	6.093
Calculation assumed two NAND3 gates on the third stage		23	6.494
NAND3 consumes more power than NAND2, that's why t		24	7.297
		25	7.478
		26	7.449
		27	5.98
		28	5.958
		29	6.594
		30	7.144
		31	6.507
		Average	6.78E-09

Delay From Plot 1.45E-09 1.45 ns

Extracted Simulation

Delay From Plot 1.07E-09 1.07 ns Wordline 16
 Delay From Plot 1.46E-09 1.46ns Wordline 31

Average Power 6.35E-04
 Avg Static Power consumption rolling address 3.64E-09 10.89 uW

Dynamic Power Dissipation
 6.35E-04

6-stage	G	P	F	f^	Df	D	Path Delay (seconds)	Al	Am	Pd	PD
INV-INV-INV-NAND3-INV-NAND2	2.22	9.00	682.67	2.97	17.80	26.80	7.46E-10	154112	30822.4	2.64E-03	7.07E-02
B	16.00	tau	2.78E-11	R	6100.00						
H	19.20			C	1.52E-15						

Stage	g	f^	Branching of Cout	Cout	Cin	P/N Ratio
1. INV	1.00	2.97	1.00	29.54	9.95	2.00
2. INV	1.00	2.97	1.00	87.74	29.54	2.00
3. INV	1.00	2.97	16.00	16.29	87.74	2.00
4. NAND3	1.67	2.97	1.00	29.02	16.29	0.67
5. INV	1.00	2.97	1.00	86.20	29.02	2.00
6. NAND2	1.33	2.97	1.00	192.00	86.20	1.00

1. INV						Activity Factor (α)	0.1
p constant	n constant	constant				frequency (f)	1.00E+07
1.00	-2.00	0.00 p	6.63			Vdd	3.3
1.00	1.00	9.95 n	3.32			Unit Cap	1.00E-15
2. INV						Power	
p constant	n constant	constant				Node	Branchout
1.00	-2.00	0.00 p	19.69			INV out node	1
1.00	1.00	29.54 n	9.85			INV out node	6
						INV out node	6
						INV out node	83
						NAND3 out	12
						INV out node	7
						NAND2 out	198
						Total Per wordline	7.49E-05
						Wordlines	32
						Shot Circuit Power (scp)	110% Total + scp
							2.64E-03

3. NAND3						Stick Diagrams	
p constant	n constant	constant				Brief Description:	10 sets of stacked inverters at the top left corner, stacked NAND3-NAND2-INVn on the right
1.00	-0.67	0.00 p	6.51			W - tracks	H - tracks
1.00	1.00	16.29 n	9.77			NAND3-INV-NAND2	14
						INV-INV-INV	5
						Lambda	0.2
						Lambda per track	8
4. INV						9 Total W - tra	64
p constant	n constant	constant				13 Total H - trac	301
1.00	-2.00	0.00 p	19.35			Total Area - l	154112
1.00	1.00	29.02 n	9.67			Total Area - l	30822.4

5. NAND2					
p constant	n constant	constant			
1.00	-1.00	0.00 p	43.10		
1.00	1.00	86.20 n	43.10		

Scrap
Optimizing 5-Stage

INV-INV-NAND3-NAND2-INV

Stage	g	f^	Branching of Cout		Cin	
1. INV		1.00	3.69	1.00	36.82	9.98
2. INV		1.00	3.69	16.00	8.49	36.82
3. NAND3		1.67	3.69	1.00	18.80	8.49
4. NAND2		1.33	3.69	1.00	52.03	18.80
5. INV		1.00	3.69	1.00	192.00	52.03

INV-INV-INV-NAND3-NAND2

Stage	g	f^	Branching of Cout		Cin	
1. INV		1.00	3.69	1.00	36.82	9.98
2. INV		1.00	3.69	1.00	135.87	36.82
3. INV		1.00	3.69	16.00	31.34	135.87
4. NAND3		1.67	3.69	1.00	69.38	31.34
5. NAND2		1.33	3.69	1.00	192.00	69.38

Design Funct	Path Logical	IPath Parasitic	F	f^	Df	Path Delay - IArea in LambArea in MicrcDynamic Pow			
INV-NAND5	2.33	6.00	716.80	26.77	53.55	59.55	60944	12188.8	
INV-INV-NAN	2.33	7.00	716.80	8.95	26.85	33.85	133056	26611.2	
INV-INV-NAN	2.22	7.00	682.67	5.11	20.45	27.45	79696	15939.2	
INV-INV-NAN	2.22	8.00	682.67	3.69	18.44	26.44	152064	30412.8	
INV-INV-INV-	2.22	9.00	682.67	2.97	17.80	26.80	154112	30822.4	
B	16.00								
H	19.20								

Design Funct	Word Line W	Word Line Height - Tracks
INV-NAND5	8.00	5.00
INV-INV-NAND5		
INV-INV-NAND3-NAND2		
INV-INV-NAND3-NAND2-INV		
INV-INV-INV-NAND3-NAND2-INV		
Lambda	0.20	
Word Lines	32.00	

Width - um	Height - um
12.80	256.00

Power Delay Product - PD