TFA9894D/E

High Efficiency Class-D Audio Amplifier

Rev. 1 — 13 June 2018

Objective data sheet
COMPANY CONFIDENTIAL

1 General description

The TFA9894 is a high efficiency 10 V boosted class-D audio amplifier with a sophisticated SpeakerBoost and Protection algorithm. It can deliver up to 5.6 W (AVG) output power into an 8 Ω speaker and up to 6.2 W (AVG) output power into 4 Ω speaker, at a battery supply voltage of 4.0 V. The internal adaptive DC-to-DC converter raises the power supply voltage up to 10 V, providing ample headroom for major improvements in sound quality.

A safe working environment is provided for the speaker under all operating conditions. The TFA9894 maximizes acoustic output while ensuring membrane displacement and voice coil temperature do not exceed their rated limits. This function is based on a speaker box model that operates in all speaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures that the quality of the audio signal is never degraded by unwanted clipping or distortion in the amplifier or speaker.

The adaptive sound maximizer algorithm uses feedback to calculate both the temperature and the excursion accurately, allowing the TFA9894 to adapt to changes in the acoustic environment.

Internal adaptive DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary. This maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption.

The device can be configured to drive either a hands-free speaker (4 Ω to 8 Ω) for audio playback, or a receiver speaker (32 Ω), for handset playback, allowing it to be embedded in platforms supporting both a hands-free speaker and a handset speaker. The maximum output power, the gain, and the noise levels are lower in handset call use case than in hands-free call use case.

The TFA9894 also incorporates battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery, which could cause a system undervoltage. This circuitry minimizes the impact of a falling battery voltage by preventing unexpected device switch off due to excessive current drawn from the battery.

The device features a second order closed loop architecture, used in a class-D audio amplifier, providing excellent audio performance and high supply voltage ripple rejection. The audio input interface is TDM and the control settings are communicated via an I2C-bus interface.

The TFA9894 is available in a 48-bump Wafer Level Chip-Size Package (WLCSP) with a 400 µm pitch.

2 Features and benefits

- Sophisticated SpeakerBoost and Protection algorithm that maximizes speaker performance while protecting the speaker:
  - Fully embedded software, no additional license fee, or porting required
  - Fully integrated solution, including DSP, amplifier, DC-to-DC, thermal sensing
- Adaptive excursion control - guarantees that the speaker membrane excursion never exceeds its rated limit
- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit
- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker-box leakage
- Clip avoidance - DSP algorithm prevents clipping even with sagging supply voltage
- Automatic bandwidth extension to increase low-frequency response
- TFA9894 high output power: 5.6 W (AVG) into 8 Ω at 4.0 V supply voltage (THD = 1 %, VBST = 10 V), 6.2 W (AVG) into 4 Ω at 4.0 V supply voltage (THD = 1 %, VBST = 9 V)
- Support handset (16 Ω or 32 Ω) and hands-free (4 Ω or 8 Ω) speaker configurations.
- High efficiency, low power dissipation, and low noise speaker driver (Dynamic Range > 110 dB).
- Adaptive DC-to-DC converter increases the supply voltage smoothly when switching between fixed boost and adaptive boost mode, preventing large battery supply spikes and limiting quiescent power consumption.
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- Very low noise output (typical 14 µV with null DATA input at Fs = 48 kHz)
- I^2C-bus control interface (400 kHz)
- Speaker current and voltage monitoring (via the TDM-bus), as well as DSP data output (with and without pilot tone) for Acoustic Echo Cancellation (AEC) at the Host.
- Various sample frequencies supported: 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz
- Configurable full duplex 4-wires TDM input interface.
- Programmable interrupt control via a dedicated interrupt pin
- Thermal foldback and over temperature protection
- 15 kV system-level ESD protection without external components on amplifier output

3 Applications

- Mobile phones & Tablets
- Portable Gaming Devices
- Portable Navigation Devices (PND)
- Notebooks/Netbooks
- Internet of Things applications embedding high-quality audio

4 Quick reference data

Table 1. Quick reference data

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}; in application, V_{BAT} must not be lower than V_{DDD} levels.		2.7	-	5.5	V
V_{DDE}	digital supply voltage	on pin VDDE		1.65	1.8	3.6	V
V_{DDD}	digital supply voltage	on pin V_{DDD}		1.65	1.8	1.95	V
V_{DDP}	power supply voltage	on pin V_{DDP}		2.7	-	10.2	V
R_L	Speaker Impedance			3.2	-	38.4	Ω
I_{BAT}	battery supply current	active state; on pin VBAT; operating mode with load R_L = 8 Ω; DC-to-DC in adaptive boost mode; P_o = 380 mW, (average music power); V_{BAT} = 4.0 V; V_{DDP} = 10 V		-	125	-	mA
		active state; on pin VBAT; operating mode with load R_L = 8 Ω; external V_{DDP} = 10 V ; f_i = 1 kHz; P_{out} = 4 W		-	1.73	-	mA
		idle state; on pin VBAT; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; low power mode enabled		-	2.7	-	mA
		idle state; on pin VBAT; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; V_{BAT} = 4.0 V; external V_{DDP} = 10 V		-	1.5	-	mA
		power-down state; on pin VBAT; DC-to-DC in power-down mode or external V_{DDP} = 10 V; T_j = 25 °C; no clock.		-	1	-	µA
I_{VDDP}	power supply current	active state; on pin VDDP; operating mode with load R_L = 8 Ω; external V_{DDP} = 10 V ; f_i = 1 kHz; P_{out} = 4 W		-	507	-	mA
		idle state; on pin VDDP; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; V_{BAT} = 4.0 V; external V_{DDP} = 10 V		-	10	-	mA
		power-down state; on pin VDDP; external V_{DDP} = 10 V; T_j = 25 °C; no clock.		-	1.0	-	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDD}	digital supply current	active state (CoolFlux active); on pin VDDD; operating mode with load R_L = 8 Ω; DC-to-DC in adaptive boost mode; P_o = 380 mW (average music power); V_{BAT} = 4.0 V; V_{DDP} = 10 V		-	20	-	mA
		Idle state; on pin VDDD; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; low power mode enabled		-	3.9	-	mA
		power-down state; on pin VDDD; DC-to-DC in power-down mode; T_j = 25 °C; no clock. input data not toggling		-	10	-	µA
I_{DDE}	digital supply current	power-down state; on pin VDDE; DC-to-DC in power-down mode; T_j = 25 °C; no clock; input data not toggling		-	1	-	µA
$P_{o(AVG)}$	Average output power	THD+N = 1 %; (R_L = 8 Ω; L_L = 44 µH); V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		5.3	5.6	-	W
		THD+N = 1 %; (R_L = 6 Ω; L_L = 30 µH); V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		5.8	6.1	-	W
		THD+N = 1 %; (R_L = 4 Ω; L_L = 30 µH); V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		6.0	6.2	-	W
		THD+N = 1 %; (R_L = 8 Ω; L_L = 44 µH); external V_{DDP} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		-	5.6	-	W
		THD+N = 1 %; (R_L = 6 Ω; L_L = 30 µH); external V_{DDP} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		-	7.5	-	W
		THD+N = 1 %; (R_L = 4 Ω; L_L = 30 µH); external V_{DDP} = 9 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		-	9.0	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 2.0 W; R_L = 4 Ω or 8 Ω		-	0.04	0.09	%
		P_o = 2.0 W; R_L = 4 Ω or 8 Ω; external V_{DSDP} = 10 V		-	0.04	-	%
ΔG	Gain variation over freq.	BW = 20 Hz to 15 kHz; V_{BAT} = 3.4 V to 5 V		−0.1	-	0.7	dB
V_{POP}	Pop noise	at mode transition and gain change; with C_L < 200 pF[2]		-	-	2	mV
		at mode transition and gain change; with C_L < 200 pF[2]; external V_{DDP} = 10 V		-	-	5	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{n(o)}$	output noise voltage	a-weighted; no input signal; low noise mode; f_s = 48 kHz	[3]	-	14	18	µV
		a-weighted; no input signal; low noise mode; f_s = 44.1 kHz	[3]	-	15	18	µV
		a-weighted; no input signal; low noise mode; f_s = 16 kHz, high performance or 32 kHz, high performance	[3]	-	15	18	µV
		external mode; a-weighted; no input signal; (noise shaper noise not included); V_{DDP} = 6 V		-	28	-	µV
		external mode; a-weighted; no input signal; (noise shaper noise not included); V_{DDP} = 10V		-	36	-	µV
DR	dynamic range	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; no signal applied		110	114	-	dB
		a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; no signal applied; external V_{DDP} = 10 V		-	105	-	dB
S/N	signal-to-noise ratio	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; with signal applied		100	-	-	dB
		a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; with signal applied; external V_{DDP} = 10 V		-	95	-	dB
η_{po}	output power efficiency	on pin V_{BAT}; Input: 100 Hz sinewave; R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; P_o = 4 W		-	82	-	%
		total input power from all supplies; f_i = 100 Hz sinewave; R_L = 8 Ω; V_{BAT} = 4.0 V, external V_{DDP} = 10 V, P_o = 4.0 W		-	88	-	%

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] When C_L is above 200 pF, Low Power Mode must be disabled.
[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9894DUK	WLCSP48	wafer-level chip-scale package; 48 bumps; 2.51 mm x 3.55 mm x 0.50 mm body; RDL; no backside coating	SOT1887-4

Type number	Package		
	Name	Description	Version
TFA9894EUK	WLCSP48	wafer-level chip-scale package; 48 bumps; 2.51 mm x 3.55 mm x 0.525 mm body; RDL; backside coating	SOT1887-5

6 Block diagram

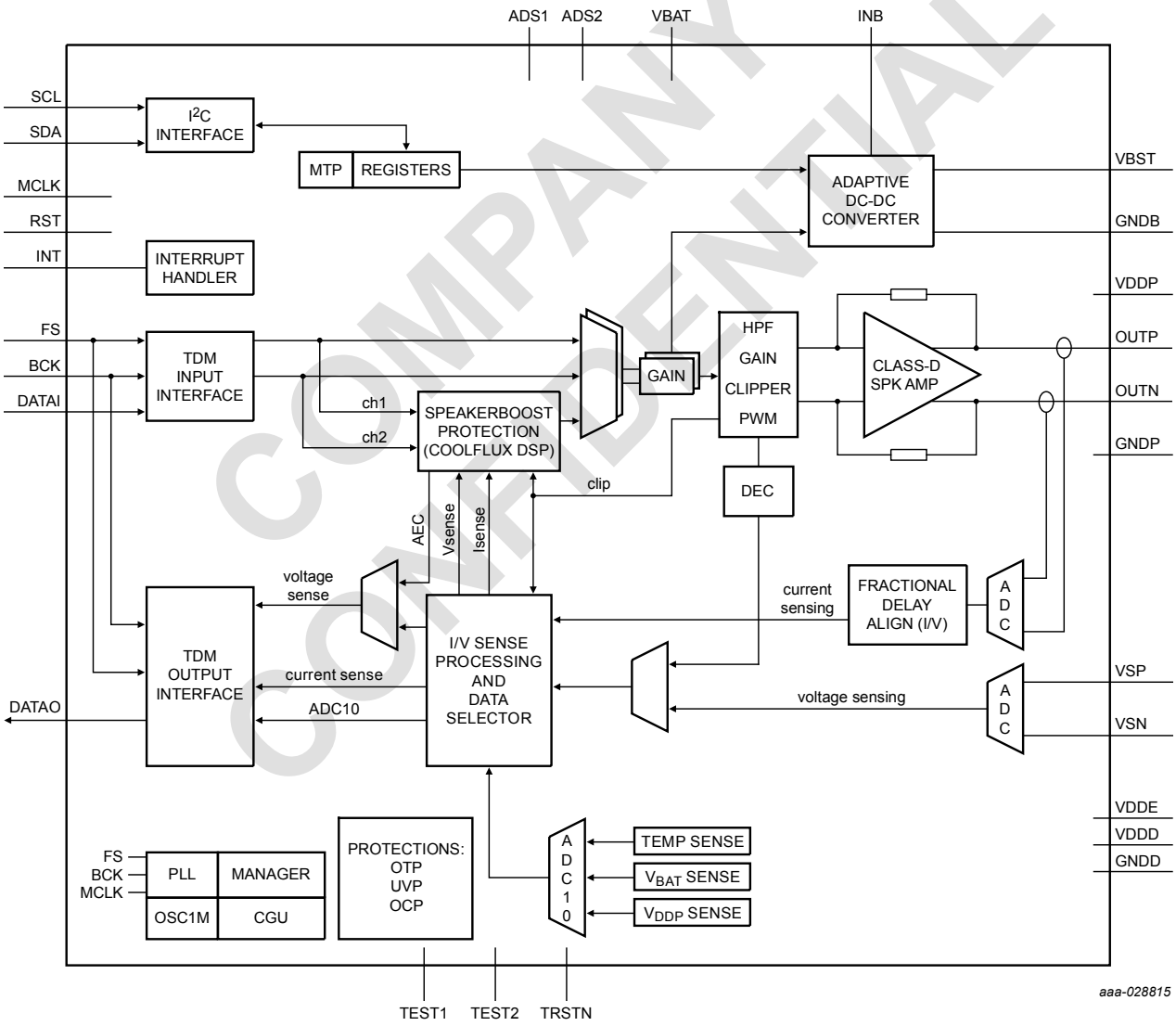
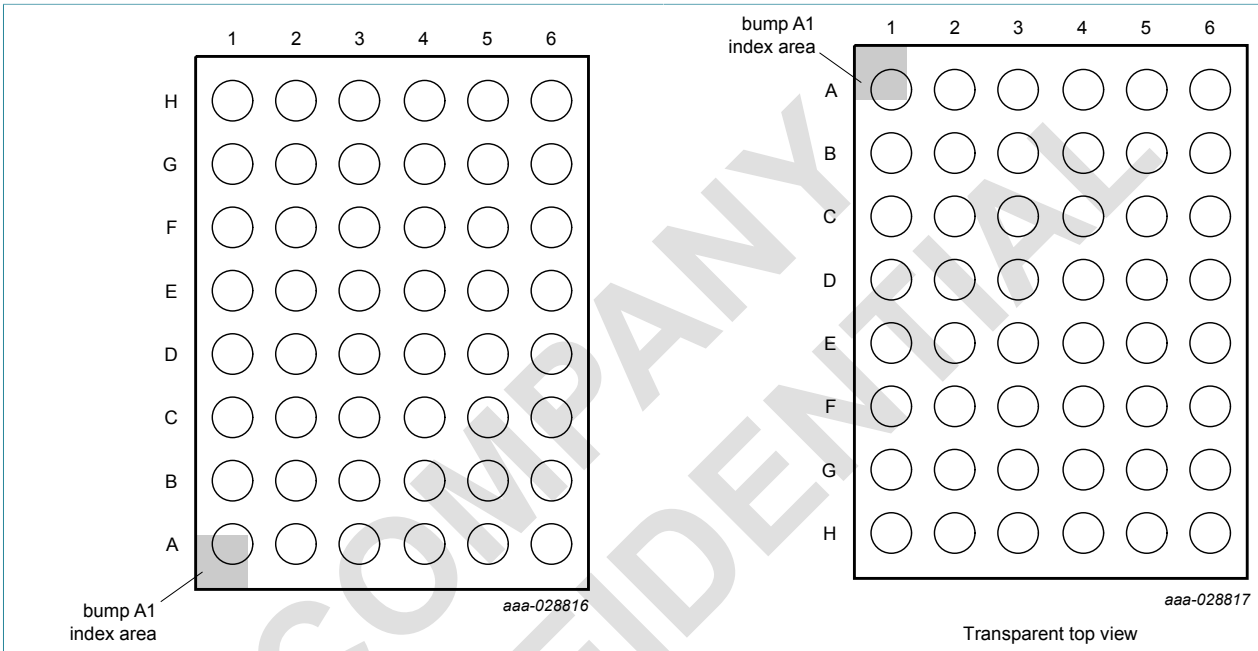


Figure 1. Block diagram

7 Pinning information

7.1 Pinning



a. Bottom view

b. Transparent top view

Figure 2. Bump configuration

	1	2	3	4	5	6
A	FS	VDDD	VDDE	GNDD	INT/ TDO	SCL
B	BCK	MCLK/ TCK	VDDE	GNDD	GNDD	SDA
C	DATAO	GNDD	VDDE	VDDE	GNDD	VBAT
D	DATAI	GNDD	ADS2/ TMS	ADS1/ TDI	TRSTN	VSN/ TEST4
E	RST	GNDD	GNDD	TEST2	TEST1	VSP/ TEST3
F	GNDB	GNDB	GNDB	GNDP	GNDD	GNDD
G	INB	INB	INB	GNDP	VDDP	OUTN
H	VBST	VBST	VBST	OUTP	VDDP	VDDP

aaa-030877

Transparent top view

Figure 3. Bump mapping

Table 3. Pinning

Symbol	Pin	Type	Description
FS	A1	I	digital audio frame sync for TDM interface
VDDD	A2	P	digital supply voltage
VDDE	A3	P	pad digital supply voltage (to be connected to VDDD)
GNDD	A4	P	digital ground
INT/TDO	A5	O	digital interrupt output / JTAG TDO
SCL	A6	I	digital I^2C-bus clock input
BCK	B1	I	digital audio bit clock input for TDM interface
MCLK/TCK	B2	I	master clock input / JTAG TCK
VDDE	B3	P	pad digital supply voltage (to be connected to VDDD)
GNDD	B4	P	digital ground
GNDD	B5	P	digital ground
SDA	B6	I/O	digital I^2C-bus data input/output
DATAO	C1	O	digital audio data output for TDM interface
GNDD	C2	P	digital ground
VDDE	C3	P	pad digital supply voltage (to be connected to VDDD)
VDDE	C4	P	pad digital supply voltage (to be connected to VDDD)
GNDD	C5	P	digital ground
VBAT	C6	P	battery supply voltage
DATAI	D1	I	digital audio data input for TDM interface
GNDD	D2	P	digital ground
ADS2/TMS	D3	I	digital address select input 2 / JTAG TMS
ADS1/TDI	D4	I	digital address select input 1 / JTAG TDI
TRSTN	D5	I	JTAG test reset
VSN/TEST4	D6	I/O	voltage sensing inverting / test signal IO 4
RST	E1	I	digital reset input
GNDD	E2	P	digital ground
GNDD	E3	P	digital ground
TEST2	E4	I/O	test signal IO 2; for test purposes only, connect to PCB ground
TEST1	E5	I/O	test signal IO 1; for test purposes only, connect to PCB ground
VSP/TEST3	E6	I/O	voltage sensing non-inverting / test signal IO 3
GNDB	F1	P	boosted ground
GNDB	F2	P	boosted ground
GNDB	F3	P	boosted ground
GNDP	F4	P	power ground

Symbol	Pin	Type	Description
GNDD	F5	P	digital ground
GNDD	F6	P	digital ground
INB	G1	P	DC-to-DC boost converter input
INB	G2	P	DC-to-DC boost converter input
INB	G3	P	DC-to-DC boost converter input
GNDP	G4	P	power ground
VDDP	G5	P	power supply voltage
OUTN	G6	P	inverting output
VBST	H1	O	boosted supply voltage output
VBST	H2	O	boosted supply voltage output
VBST	H3	O	boosted supply voltage output
OUTP	H4	P	non-inverting output
VDDP	H5	P	power supply voltage
VDDP	H6	P	power supply voltage

8 Functional description

The TFA9894 is a highly efficient Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated SpeakerBoost and Protection algorithm, depicted in block diagram of Figure 1.

TFA9894 contains a TDM input/output interface for communicating with the audio host. The interface is compliant with standard TDM interfaces and supports a wide range of TDM configurations. It can also be configured to output current sense and voltage sense information. The audio hosth can use this information.

The SpeakerBoost and Protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core, maximizes the acoustical output of the speaker while limiting membrane excursion and voice coil temperature to safe levels. The mechanical protection implemented guarantees that speaker membrane excursion never exceeds its rated limit, to an accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to an accuracy of approximately ±10 °C during music playback. Furthermore, advanced signal processing ensures that the audio quality always remains acceptable.

The protection algorithm implements an adaptive speaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

The SpeakerBoost and Protection algorithm boosts the output sound pressure level within given mechanical, thermal, and quality limits. An optional Bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high quality in quiet environments.

The frequency response of the TFA9894 can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 10 are processed with 24-bit single precision.

At low battery voltage levels, the gain (from TDM interface to speaker output) is automatically reduced to limit battery current (when battery safeguard is enabled).

The SpeakerBoost and Protection algorithm or the host application (external) can controll the output volume. In the latter case, the boost features of the SpeakerBoost and Protection algorithm must be disabled to avoid neutralizing external volume control.

The digital audio stream is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

An adaptive DC-to-DC converter boosts the battery supply voltage when the audio stream crosses two programmable voltage thresholds. It switches automatically to Follower mode (V_{BST} = V_{BAT}; no boost) when the audio output voltage is lower than the battery voltage.

8.1 Amplifier use cases

The system is optimized to support the following three main use cases:

- **Power-down**: all functions are switched off to conserve battery power; the I^2C-bus interface is operational for device configuration before it is being activated.
- **Hands-free call or Multimedia playback**: audio and/or multimedia streams are amplified by the amplifier, configured in speaker mode, and played on the main speaker (4 Ω to 8 Ω).
- **Handset call**: the amplifier is configured in receiver mode, producing less output power, adapted to the receiver speaker (16 Ω or 32 Ω).

The TFA9894 has a flexible architecture with features that are programmable via the I^2C-bus interface. Dedicated control settings are provided for configuring the use cases and algorithms. The SpeakerBoost and Protection algorithm is active in hands-free and multimedia use cases.

8.1.1 Power-down use case

Power consumption is at a minimum in the power-down use case. Much of the digital circuitry is disconnected from the V_{DDD} supply lines to minimize power consumption. Power consumption can be reduced further (by about 5 µA) by turning off the internal oscillator (setting bit MANAOOSC to 1).

In the power-down use case:

- The digital pins are powered and at their default state (output pin INT is driving and DATAO is tri-stated).
- The DC-to-DC converter output is about 0.6 V lower than V_{BAT} (forward biased diode).
- The amplifier outputs are floating.
- Loaded SpeakerBoost and Protection algorithm parameter settings are retained.

8.1.2 Handsfree / Multimedia playback use case

The main purpose of this use case is to amplify the mono audio stream to a high quality audio playback and, optionally, to maximise the sound pressure level. The CoolFlux DSP is enabled and executes the SpeakerBoost and Protection algorithm. Current and voltage sensing are activated to support the SpeakerBoost and Protection algorithm. In addition, the adaptive DC-to-DC converter is active to maximize amplifier output power. The audio stream to be amplified by the TFA9894 is input on the TDM interface. This use case is active during Operating state of the device manager (Figure 5).

8.1.3 Handset call use case

The handset call use-case in most cases is done in follower mode, meaning DC-DC converter is not boosting, while Coolflux DSP is disabled and bypassed. This use case is active during Operating state of the device manager (Figure 5).

8.1.4 Low power mode

In order to minimize both output noise and power consumption, the TFA9894 embeds a complementary Low Power Mode (LPM) feature. This feature disables specific modules automatically when the device detects that the output signal level is low enough. LPM operates only during the Operating state of the device manager (Figure 5), and it should only be activated when the DC-to-DC is in follower mode (DCA = 0), more specifically

during Handset call use case. It is not recommended to activate it during Handsfree call use case as it can generate pop on the amplifier outputs.

Note: *This mode is disabled as long as R_{on} calibration is not executed (MTPEX = 0).*

The Low Power Mode is by default active and can be disabled using the LPM1MODE bit. Status of the LPM mode is reflected in the LP1 status flag (register STATUS_FLAGS2). An interrupt is also available to monitor this mode (ISTLP1). When the output level is detected low, the LPM mode disables the modules highlighted in Figure 4 in order to minimize power consumption. The amplifier remains powered and active such that output signal is still available on the speaker. When an output capacitance higher than 200 pF is present on the amplifier outputs OUTP/OUTN, the Low Power mode must be disabled.

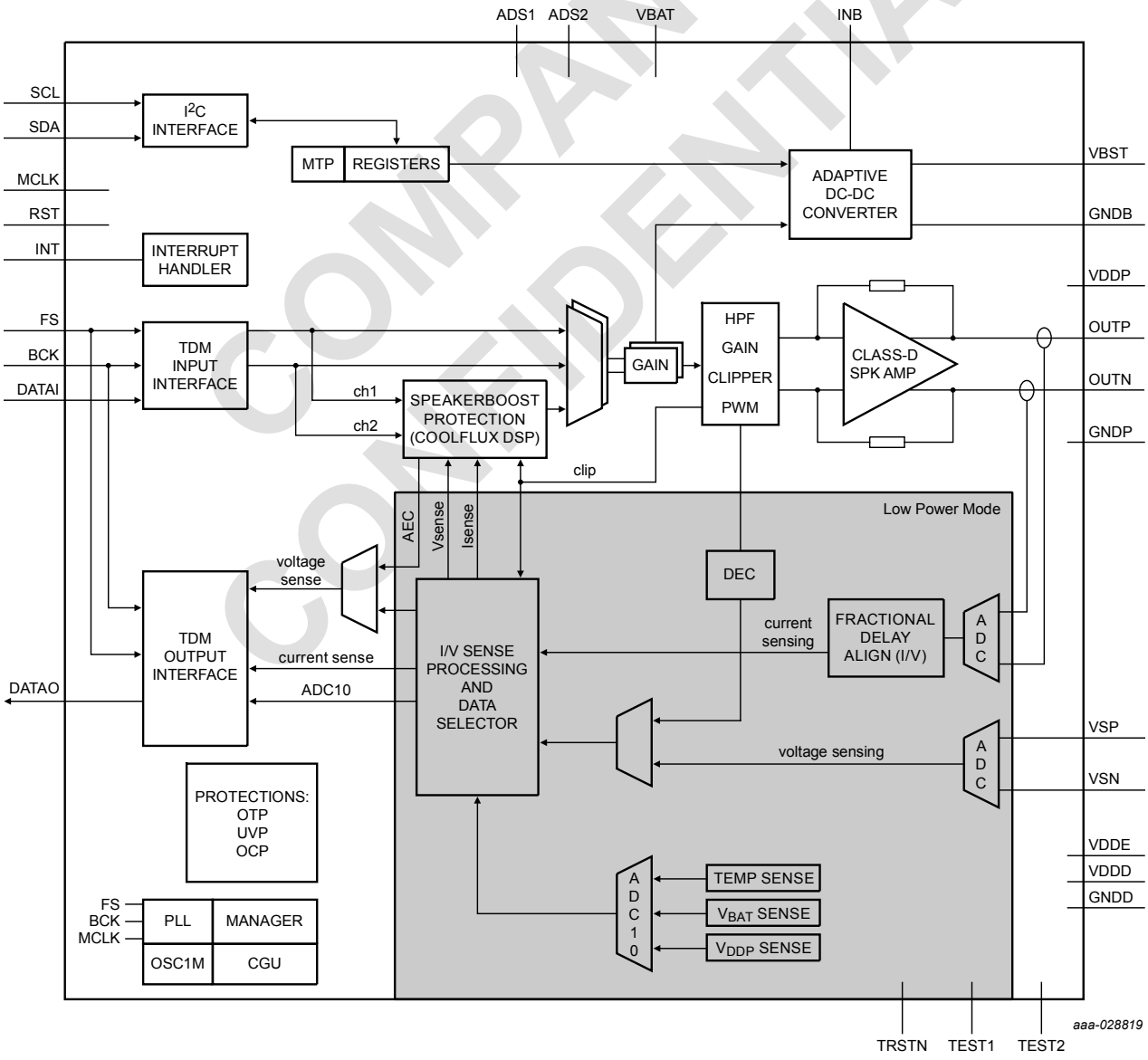


Figure 4. LPM disabled blocks

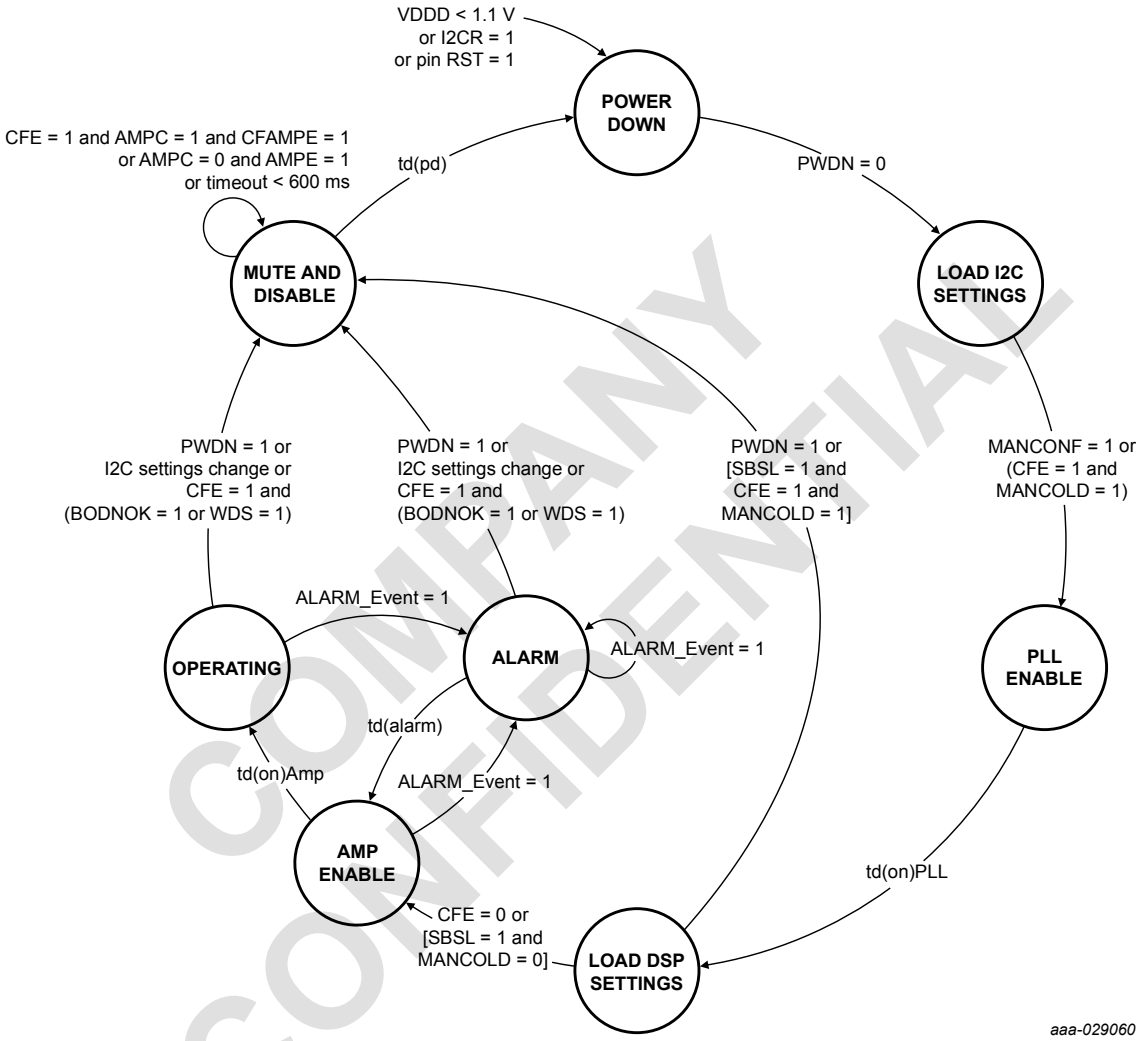
8.2 Device manager

The device manager state diagram shown in Figure 5 illustrates the actions and timing needed to switch from Power-down to Operating state (and back to Power-Down). The state diagram shows four primary states:

- **Power-down**, which is equivalent to the power-down use case.
- **Load I^2C settings**, which can be used to configure the hardware IP blocks.
- **Load DSP settings**, which can be used to load the SpeakerBoost and Protection algorithm settings.
- **Operating**, covers the Multimedia Playback (or Handsfree Call) and handset Call.

Additional timing-related states are supported: *PLL enable, AMP enable, Mute & Disable* and *Alarm* state. Assuming I^2C settings have previously been uploaded for both Hardware and DSP, a typical startup time from *Power Down* to *Operating* (audio played back on speaker), will take $t_{d(on)PLL} + t_{d(on)AMP}$. This is the time needed to turn on the PLL (in *PLL enable* state) and the Amplifier (in *AMP enable* state)

The current state of the device manager can be read via status bit MANSTATE.



1. In any state, as soon as NOCLK = 1 (lost clock) or CLKOOR = 1 (clock out of range), an immediate transition to the mute & disable state is triggered unconditionally.
2. ALARM_Event = 1 when: OTDS = 0, UVDS = 0, or OCDS = 1
3. CFAMPE is an internal control signal from Cooflux to amplifier.

Figure 5. Device manager state diagram

The Table 4 lists relevant control bits to select Primary States.

Table 4. Primary states selection

State	PWDN[1]	MANSCONF[1]	SBSL[1]	AMPC[1]	AMPE[1]	CFSM[1]	TDM input[2]
Power-down (via TDM)[3]	don't care	don't care	don't care	don't care	don't care	don't care	inactive
Power-down (via I^2C)[3]	1 (default)	don't care	don't care	don't care	don't care	don't care	don't care
Load I^2C settings	0	0	don't care	don't care	don't care	don't care	don't care

State	PWDN[1]	MANSCONF[1]	SBSL[1]	AMPC[1]	AMPE[1]	CFSM[1]	TDM input[2]
Load DSP Settings	0	1	0	don't care	don't care	don't care	don't care
Operating (CFE=1)	0	1	1	1	don't care[4]	0	active
Operating (CFE=0)	0	1	don't care	0	1	0	active

[1] I^2C control bit.
[2] TDM active means that the input frequency on BCK and FS are valid and in the proper range.TDM inactive means there is no valid clock signal on BCK or FS.
[3] Power-down can also be triggered under unconditioned events (see Section 8.2.7).
[4] Controlled internally by Coolflux

8.2.1 Power-down state

Power consumption is at a minimum in this state, which is equivalent to the power-down use case (see Section 8.1.1). The Operating to Power-down state sequence is described in Section 8.2.7. I^2C control bit PWDN must be set to 0 to exit Power-down state and switch to Load I^2C settings state.

8.2.2 Load I^2C settings

Transitions between use cases involves changes to I^2C control settings. If the transition involves a 'primary control change' (see Section 8.2.7.1), an Operating-to-Power-down-to-Operating sequence may be needed. Since transitions between use cases need to be pop and click noise free, some I^2C control settings associated with the target use case may need to be set after the device manager has left Mute & Disable state and before switching back to Operating state. These settings can be set in the Load I^2C settings state.

The device manager switches from Load I^2C settings to Load DSP settings when the host sets MANSCONF to 1 (to indicate that the I^2C-bus control settings have been loaded). If a cold boot sequence is executed by setting MANCOLD to 1 (Section 8.2.3), the device manager switches immediately from Load I^2C settings to Load DSP settings regardless of the state of MANSCONF, meaning that I^2C settings must not be applied by the Host (as the Load I^2C settings state is skipped).

8.2.3 Load DSP Settings

The Load DSP Settings state is intended to configure the Coolflux DSP by loading the SpeakerBoost and Protection algorithm parameters as well as the use case profiles into its Random-Access Memory (RAM).

After a first Power on Reset, the TFA9894 device is forced into cold boot to avoid any amplifier activation (transition into Operating state) without proper DSP settings. Cold boot is controlled by setting the MANCOLD bit to 1, which is the case by default after a first Power on Reset. In such case, when the loading of parameters is completed, the manager will exit Load DSP Settings state but it is not allowed to transition to Operating state. It will transition back to Mute & Disable state instead.

A handshake protocol has been implemented between the host and the Cooflux DSP in order to insure proper parameters transfer to RAM. When the loading of the configurations is complete, the Coolflux DSP sets the ACS flag to 0 indicating to the host

that the cold boot has succeeded. The host then writes the SBSL bit to 1, allowing the manager to proceed to Mute & Disable state.

The MANCOLD bit is reset automatically to 0 when manager transitions through Mute & Disable state. As such, if the host requires to have additional cold boot (not triggered by the initial Power on Reset) it must write explicitly the MANCOLD bit to 1, prior to exiting the Power Down state.

DSP Parameters are retained as long as the supply voltage (V_{DDD}) is within the normal operating range. If supply voltage is too low or removed, the parameters are lost. The SpeakerBoost and Protection algorithm parameters only need to be loaded once, as long as the supply voltage is not removed. So the device can be reset and activated again without having to reload these settings (warm boot sequence). In such case, the MANCOLD bit is 0. The host controls the transition from Load DSP Settings state to AMP Enable state by asserting the SBSL bit to 1. Additionally, the host can hold the manager in Load DSP Settings state (while SBSL = 0) in order to upload firmware profiles corresponding to new use cases.

An internal reference clock (oscillator) is provided during cold boot sequence, such that the TFA9894 DSP can be configured without the needs for external clock. It is then switched automatically to external clock (BCK/FS) used as reference for the PLL, once the cold boot sequence is completed. Automatic switch to external clock can be disabled by setting bit ACKCLDDIS = 1 and then the PLL reference is controlled by bit REFCKSEL.

Note: *When the Coolflux DSP is disabled (CFE = 0), the Load DSP Settings state is passed through, no cold boot sequence is triggered and PLL is clocked on external clock selected by REFCKEXT bit. There is no auto switch of PLL reference as described above.*

8.2.4 Operating state

This is the main state during which the TFA9894 is fully operational, outputting TDM incoming audio stream to the speaker. In Operating state, depending on the selected use-case (see Section 8.1), the Coolflux DSP, the DC-DC and the Amplifier are enabled/activated.

Valid BCK and FS clocks are needed on the TDM input interface to enter Operating state. In addition, the TFA9894 expects the same frequency on FS as selected via bits AUDFS.

8.2.5 Alarm state

When a protection mechanism is triggered, the TFA9894 device manager switches to Alarm state. In Alarm state, the class-D amplifier outputs are floating. When any of the following event occurs, Alarm state is entered:

- OverTemperature Protection (OTP), bit OTDS
- UnderVoltage Protection (UVP), bit UVDS
- OverCurrent Protection (OCP), bit OCDS

When all alarm conditions are cleared, Alarm state is exited after $t_{d(alarm)}$.

8.2.6 Mute & disable state

The TFA9894 device manager goes through Mute & Disable state when a power-down is triggered by the host (from Operating State) In this state the analog amplifier is still engaged and firmware executes the mute sequence. At the end of the mute sequence, firmware sets AMPE control bit to 0 to mark the end of the mute sequence.

The device manager features a time-out function (enabled by setting bit MUTETO to 0) that forces the TFA9894 to power-down if firmware does not properly mute and disable the device during the Mute & Disable state. The reaction time is at least 600 ms. The mute and unmute sequences are managed by the Coolflux firmware to avoid pops and clicks with fast transition times and if it is not completed within 600 ms then the time-out will trigger.

Once AMPE is set to 0 or if the time-out is reached (> 600 ms) the device manager will disable all analog blocks, assert all internal resets and finally stop all clocks during $t_{d(pd)}$ before switching to Power-down state.

In case of an unconditional branch to Mute & Disable state (from any state) when the clock is lost (NOCLK = 1 or CLKOR = 1), the manager will not wait for the firmware mute sequence nor for the time-out expiration. It will directly execute the disabling part stated above.

8.2.7 Operating to power-down sequence

The TFA9894 switches to Power-down state when:

- I^2C control bit PWDN is set to 1. This is the default way of proceeding and will nicely transition the manager state machine to Power-down state, while going through Mute & Disable first.
- There is no valid PLL reference clock signal (the reference clock can be BCK or FS). This condition is checked in any states and if it occurs, it will immediately bring the manager to Mute & Disable state. An interrupt is triggered upon clock removal.
- The reset input (pin RST) goes HIGH (all digital circuits are reset). This is an unconditioned event. It will immediately bring the manager to Power-down state, regardless of it actual state (manager will not follow any states transitions other than going directly into power down). After a reset, the I2C settings are cleared and must be reloaded by host
- V_{DDD} is switched off (< 1.3 V, power-on reset). This is an unconditioned event. It will immediately bring the manager to Power-down state, regardless of it actual state (manager will not follow any states transitions other than going directly into power down). An interrupt is triggered upon POR detection. After a POR, the I^2C settings are cleared and must be reloaded by host
- I^2C control bit I2CR is set to 1 (I^2C registers are reset to their default values, in opposition with PWDN = 1 where I^2C registers are kept unreset). This is an unconditioned event. It will immediately bring the manager to Power-down state, regardless of it actual state (manager will not follow any states transitions other than going directly into power down)

The I^2C-bus is operational in Power-down state as soon as V_{DDD} > 1.65 V (exiting POR). Upon POR exit, the calibration values (stored in MTP) are automatically loaded in I^2C registers.

The audio pop and click noise at the outputs is at a minimum when the power-down use case is selected via bit PWDN or by removing the TDM clock.

8.2.7.1 Primary control changes

A primary control change triggers a smooth power-down sequence but the device starts up again after it reaches the Power-down state.

The device manager sets MANSCONF back to 0 (see Section 8.2.2) when a primary control change is activated.

The primary control changes are:

- PLL reference clock selections (bits REFCKEXT, REFCKSEL, MCLKSEL)
- Audio sample frequency (bits AUDFS)
- TDM settings (bits TDMNBCK)
- Coolfux DSP enable (bits CFE)

8.2.8 Status flags

The device manager sets a number of status flags during the Power-down to Operating state sequence (see Table 5). It sets the AREFS flag to 1 in the PLL enable state to indicate that the analog references have been enabled (all internal references need to be active before the amplifier can start up). It sets CLKS to 1 to signal that the clocks are stable (all clocks must be stable before the amplifier can start up). It sets the AMPS flag to 1 in AMP Enable state to indicate that the amplifier has started up. SWS is set to 1 when the amplifier starts switching.

The current state of the device manager can be read via status bits MANSTATE.

Table 5. Status flags per states

Flags	Power-down	Load I^2C settings	PLL enable	Amplifier enable	Operating state	Mute & disable	Alarm
AREFS	0	0	1	1	1	1	1
CLKS	0	0	1	1	1	1	1
AMPS	0	0	0	1	1	1	1
SWS	0	0	0	0	1	1	0

8.3 Interrupt

The interrupt output pin (INT) on the TFA9894 can be used to monitor status changes in the device. It has a 1.8 V push-pull output stage and is configured via I^2C control bits INTP as active-LOW, active-HIGH, pull-up or pull-down:

- **active-LOW**: INT is HIGH by default and goes LOW in response to an interrupt event
- **active-HIGH**: INT is LOW by default and goes HIGH in response to an interrupt event
- **pull-up**: INT is floating by default (pulled HIGH via an external pull-up resistor) and goes LOW in response to an interrupt event
- **pull-down**: INT is floating by default (pulled LOW via an external pull-down resistor) and goes HIGH in response to an interrupt event

Interrupt handler is implemented as illustrated in Figure 6.

All interrupts are disabled by default (except for POR (IEVDDS = 1) and can be individually enabled or disabled via the INTERRUPT_ENABLE registers.

The polarity of the interrupt status flags can be set via the INTERRUPT_POLARITY registers. If a polarity status bit is set to 0 (active-LOW), an interrupt is generated when

the associated status flag is set to 0. If a polarity status bit is set to 1 (active-HIGH), an interrupt is generated when the associated status flag is set to 1.

As illustrated in Figure 6, the INTERRUPT_OUT registers will always reflect the status of an interrupt source regardless of the interrupt activation (through the INTERRUPT_ENABLE registers). The INTERRUPT_ENABLE registers are only used to prevent a specific interrupt source to toggle the INT line.

Therefore, the source of the interrupt is determined by reading the interrupt status in the INTERRUPT_OUT registers and applying a logical bit-to-bit AND (in Host) with the corresponding INTERRUPT_ENABLE registers.

Interrupts are associated with a flag in STATUS_FLAGS registers as described in Table 6.

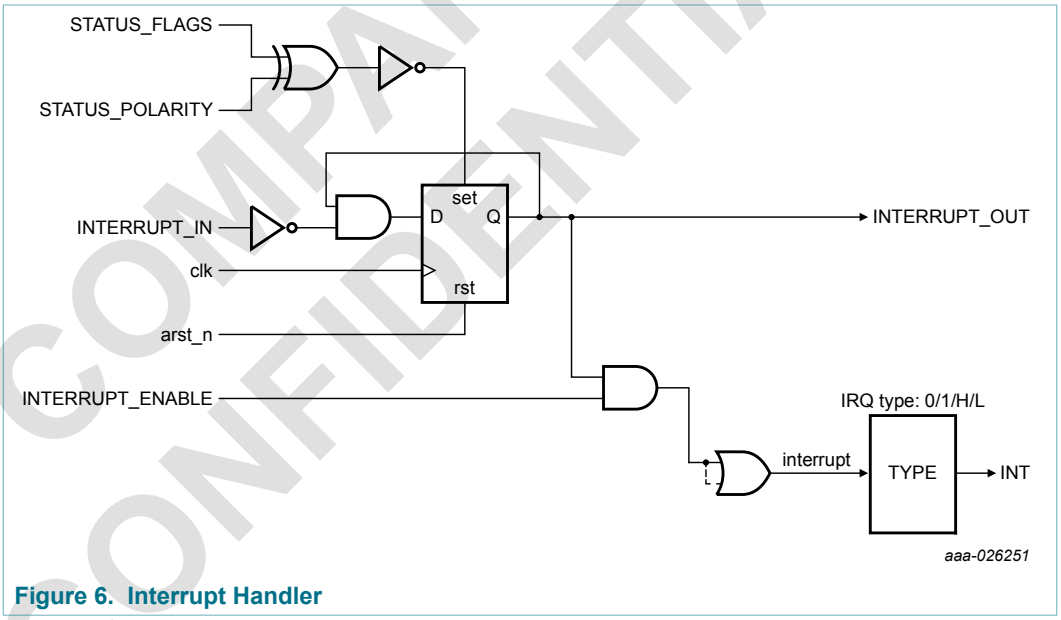


Figure 6. Interrupt Handler

Table 6. Interrupts and associated flags

Interrupt Bit Name	Interrupt. Register Address	Flag Bit Name	Flag Register Address	Sticky Flag
ISTVDDS	#40h	VDDS	#10h	Yes
ISTBSTOC	#40h	DCOCPOK	#11h	Yes[1]
ISTOTDS	#40h	OTDS	#10h	Yes[1]
ISTOCPR	#40h	OCDS	#10h	Yes[1]
ISTUVDS	#40h	UVDS	#10h	Yes[1]
ISTMANALARM	#40h	MANALARM	#11h	No
ISTTDMER	#40h	TDMERR	#11h	No
ISTNOCLK	#40h	NOCLK	#10h	Yes[2]
ISTCFMER	#40h	-	-	-
ISTCFMAC	#40h	-	-	-

Interrupt Bit Name	Interrupt. Register Address	Flag Bit Name	Flag Register Address	Sticky Flag
ISTSPKS	#40h	SPKS	#11h	No
ISTACS	#40h	ACS	#10h	No
ISTWDS	#40h	WDS	#10h	Yes[2]
ISTBODNOK	#40h	BODNOK	#10h	Yes[1]
ISTLP1	#40h	-	-	-
ISTCLKOOR	#40h	CLKOOR	#11h	No

[1] Only active when AMPE=1
[2] Permanent. Cannot be reset by reading status flag. Reset when device goes to Powerdown.

Some flags are sticky, meaning that once the event has triggered an interrupt and set the corresponding flag, the flag will not be cleared until the STATUS_FLAGS register is read. Other flags are non-sticky, meaning that the flag will be automatically cleared as soon as the condition that has triggered the interrupt (and set the flag) has disappeared. Therefore, based on the qualification (sticky or non-sticky) of the flag associated to the interrupt source, an interrupt must be cleared differently:

- Interrupts with sticky flag: First: read access to corresponding STATUS_FLAGS register (to clear out the flag). Second: write '1' into the corresponding bit of the INTERRUPT_IN registers, to clear out the interrupt status.
- Interrupts with non sticky flag: Write '1' into the corresponding bit of the INTERRUPT_IN registers, to clear out the interrupt status (clearing out the flag is useless in this case)

Note: *All bits located inside the same STATUS_FLAGS register are all cleared with a single read access to this register.*

8.4 Clocking

TFA9894 is clocked on an internal PLL that uses four different sources as reference for locking:

- Internal 1 MHz oscillator.
- TDM bit clock pin BCK.
- TDM Frame sync pin FS.
- Dedicated Master clock MCLK pin.

Given the low accuracy of the oscillator, it should not be used as PLL reference during normal operating mode:

Clocking reference is configured using the following I2Csettings:

- REFCKSEL to select between external clock (default) or internal oscillator.
- REFCKEXT to select the source for the external clock: BCK (default), FS or MCLK. When either BCK of FS is selected, the PLL is configured automatically based on the TDM configuration (sample sizes, number of slots) and audio FS settings that imply a corresponding given frequency for BCK/FS.
- MCLKSEL to select the frequency of the clock provided on MCLK pin.

As explained in Figure 5 (note 1), as soon as the clock is lost, the manager will transition into Mute & disable state. However, based on which external clock source is used for

the system (REFCKEXT: BCK, FS or MCLK), and which TDM signal is removed (BCK or FS), the response of the manager to this event can be configured using the TDMPRES I^2C setting. This setting is used to indicate how the system shall react when the TDM signals are removed and/or restored, as follows:

- TDMPRES = "00": TDM signal removal/restore is ignored. System does not shutdown (when BCK or FS is removed) nor restart (when BCK or FS is restored) but a TDM error flag is raised.
- TDMPRES ="01": TDM signal removal/restore is ignored ONLY if MCLK is selected as system clock reference for the PLL (REFCKEXT set to MCLK). Otherwise it is not ignored and system will either shutdown (if BCK or FS is removed) or restart (if BCK or FS is restored).
- TDMPRES = "10": TDM signal removal/restore is ignored ONLY if BCK or FS is selected as system clock reference for the PLL (REFCKEXT set to BCK or FS). Otherwise it is not ignored and system will either shutdown (if BCK or FS is removed) or restart (if BCK or FS is restored).
- TDMPRES = "11": TDM signal removal/restore is never ignored, meaning that removal or restore of BCK or FS will trigger a system shutdown or restart.

he above configuration using TDMPRES I^2C setting is only effective when the system clock selected for the PLL is different from the signal that is removed/restored. When both are identical, then the TDMPRES setting has no influence on the behavior of the manager. It will systematically trigger a system shutdown or restart up removal or restore.

Table 7. TDMPRES setting influence on manager

TDMPRES	REFCKEXT	Removed Signal	Manager Shutdown	Manager Restart	NOCLK Flag set	TDMERR Flag set
0	BCK	BCK	Yes	Yes	Yes	No
1	BCK	BCK	Yes	Yes	Yes	No
2	BCK	BCK	Yes	Yes	Yes	No
3	BCK	BCK	Yes	Yes	Yes	No
0	BCK	FS	No	n/a	No	Yes
1	BCK	FS	Yes	Yes	No	No
2	BCK	FS	No	n/a	No	Yes
3	BCK	FS	Yes	Yes	No	No
0	FS	BCK	No	n/a	No	Yes
1	FS	BCK	Yes	Yes	No	No
2	FS	BCK	No	n/a	No	Yes
3	FS	BCK	Yes	Yes	No	No
0	FS	FS	Yes	Yes	Yes	No
1	FS	FS	Yes	Yes	Yes	No
2	FS	FS	Yes	Yes	Yes	No
3	FS	FS	Yes	Yes	Yes	No
0	MCLK	MCLK	Yes	Yes	Yes	No
1	MCLK	MCLK	Yes	Yes	Yes	No
2	MCLK	MCLK	Yes	Yes	Yes	No

TDMPRES	REFCKEXT	Removed Signal	Manager Shutdown	Manager Restart	NOCLK Flag set	TDMERR Flag set
3	MCLK	MCLK	Yes	Yes	Yes	No
0	MCLK	BCK	No	n/a	No	Yes
1	MCLK	BCK	No	n/a	No	Yes
2	MCLK	BCK	Yes	Yes	No	No
3	MCLK	BCK	Yes	Yes	No	No
0	MCLK	FS	No	n/a	No	Yes
1	MCLK	FS	No	n/a	No	Yes
2	MCLK	FS	Yes	Yes	No	No
3	MCLK	FS	Yes	Yes	No	No

8.5 DC-to-DC converter

The DC-to-DC converter in the TFA9894 operates independently of the amplifier.

Four converter modes are supported:

- ***Disable mode***, when the class-D amplifier is supplied externally.
- ***Follower mode***, when input pin INB is switched low-ohmic to pin VBST (no boost; V_{BST} = battery voltage).
- ***Fixed boost mode***, when the battery voltage is boosted at fixed value.
- ***Adaptive boost mode***, when the DC-to-DC converter boosts the battery voltage in line with the audio signal. In this mode, 2 configurations are available (Two-levels mode or Tracking mode)

The DC-to-DC converter mode is selected via I^2C control bits DCDIS, DCA, DCIE and DCTRACK. The relationship between I^2C control settings and converter mode is described in Table 8, ad the DC-DC switching frequency is automatically set based on audio sampling frequency selected by AUDFS, as described in Table 9. To ensure the DC-to-DC converter functions correctly, the value of the external coil connected to the boost input (pin INB) needs to be specified via I^2C control bits DCCV. To ensure the DC-to-DC converter remains stable under all conditions, the VBST output needs to be loaded with sufficient effective capacitance (see Table 84). The higher the coil value, the lower the coil switching losses, but also the more capacitance is needed to ensure stability.

Table 8. DC-to-DC converter mode selection

DCDIS	DCA	DCIE	DCTRACK	DC-to-DC boost converter mode
1	don't care	don't care	don't care	Disabled mode
0	0	don't care	don't care	Follower mode
0	1	0	don't care	Fixed Boost mode
0	1	1	0	Adaptive boost mode (2-levels)
0	1	1	1	Adaptive boost mode (tracking)

Table 9. DC-to-DC converter switching frequency

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = 1.8 V; V_{DDP} = V_{BST} = 10 V; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{sw}	PWM switching frequency	f_s = 48, 96 kHz	-	2048	-	kHz
		f_s = 44.1 kHz	-	1881.6	-	kHz

[1] L_{BST} = boot converter inductance; R_L = load resistance; L_L = load inductance (speaker).

8.5.1 Disabled mode

In Disabled mode, the DC-to-DC converter is switched off. Pin INB is connected internally to VBST via a diode (see Section 9). When the amplifier is supplied from an external source, select this mode. In that case, the brownout detector must always be activated. It is recommended to connect pin INB to VBAT through a high ohmic resistor (1 MΩ) and to connect pin VBST to VDDP.

8.5.2 Follower mode

In Follower mode, the DC-to-DC converter is bypassed (not boosting). The voltage on input INB is switched low-ohmic to V_{BST}. When the TFA9894 starts up, the DC-to-DC converter is in Follower mode by default. It is advised to turn the amplifier on without an input signal before switching on the DC-to-DC converter to minimize pop noise at start-up.

8.5.3 Fixed boost mode

In Fixed Boost mode, the DC-to-DC converter converts the battery voltage to a programmed output voltage. The boost algorithm (running on Host) also limits the coil current to a programmable maximum value. The programmed output voltage and maximum coil current are set via control bits DCVOS and DCMCC respectively.

8.5.4 Adaptive boost mode

In Adaptive boost mode, boosting is only activated when the audio signal level is higher than the battery voltage. This function reduces idle dissipation while ensuring maximum power is delivered to the speaker.

The DC-to-DC converter ramps the supply voltage (V_{BST}) up smoothly to prevent high peak currents at the transition from Follower mode to Adaptive Boost mode.

The Adaptive boost mode can be configured either in Two-levels mode (Section 8.5.4.1) or Tracking mode (Section 8.5.4.2). Selection is done by using the DCTRACK parameter as described in Table 8. The behaviors of the TFA9894 in Adaptive Boost mode are illustrated in Figure 7 and Figure 8.

The DC-to-DC converter senses the voltage level at the digital interface input. It then takes advantage of the propagation delay (t_{PD}) between the interface input and the BTL output to ensure that the boosted voltage is at the correct level when required, ahead of the output signal.

8.5.4.1 Two-levels mode

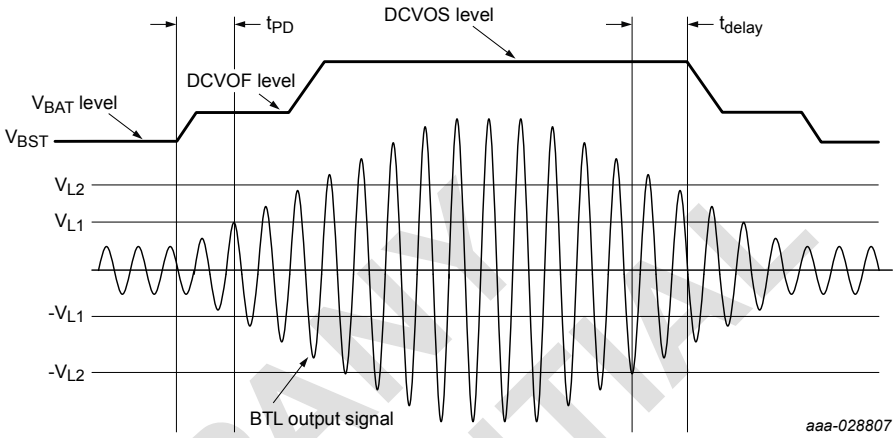


Figure 7. DC-to-DC two-levels adaptive boost behavior

In Two-levels adaptive mode, the converter will settle at one of two boost voltage levels as illustrated in Figure 7. When the BTL output signal rises above V_{L1}, set by DCTRIP, the DC-to-DC converter boosts the supply voltage to the first boost-level set by DCVOF. V_{L1} is defined as:

$$V_{L1} = 1.935(V_{BAT} - 200\text{mV}) \times 10^{-\left(\frac{5.6+0.2DCTRIP}{20}\right)} \quad (1)$$

If the level of the BTL output signal rises above V_{L2}, set by DCTRIP2, the boosted supply voltage settles at the programmed boost voltage, set by DCVOS. V_{L2} is defined as:

$$V_{L2} = 1.935(\text{DCVOF} - 200\text{mV}) \times 10^{-\left(\frac{5.6+0.2DCTRIP2}{20}\right)} \quad (2)$$

When the BTL output signal level drops below the boost thresholds (V_{L1} and V_{L2}), the converter waits for (t_{delay}) before reducing the boosted supply voltage. t_{delay} is programmed using DCHOLD bit setting. The recommended value for f_s = 16 kHz is DCHOLD = 00110b. The recommended value for f_s = 48 kHz is DCHOLD = 01011b.

8.5.4.2 Tracking mode

The TFA9894 also embeds tracking mode where the two-levels of the boost output voltages are replaced by a dynamic 63-levels envelop as depicted in Figure 8, that automatically follows the BTL output level. When the BTL output signal rises above V_{L1}, as defined in Equation 1, the DC-to-DC converter switch from Follower mode to 63-levels tracking mode.

When entering Tracking Mode, an offset is automatically added between the DC-to-DC boost output voltage and the BTL output level. This offset is defined by the parameter DCTRIPT which ranges from 5.6 dB to 11.8 dB.

The maximum DC-to-DC boost output voltage in Tracking Mode is controlled using the DCVOS parameter. If the BTL output signal level remains at a level which does not require the DC-to-DC to boost up to the limit of DCVOS, then DC-to-DC output will remain below this level and will not be clamped as depicted in Figure 8.

The envelop levels are dynamically adjusted based on the BTL output level, the configured DC-to-DC offset level (DCTRIP) used to trigger the Tracking mode and the configured offset controlled by DCTRIPT parameter.

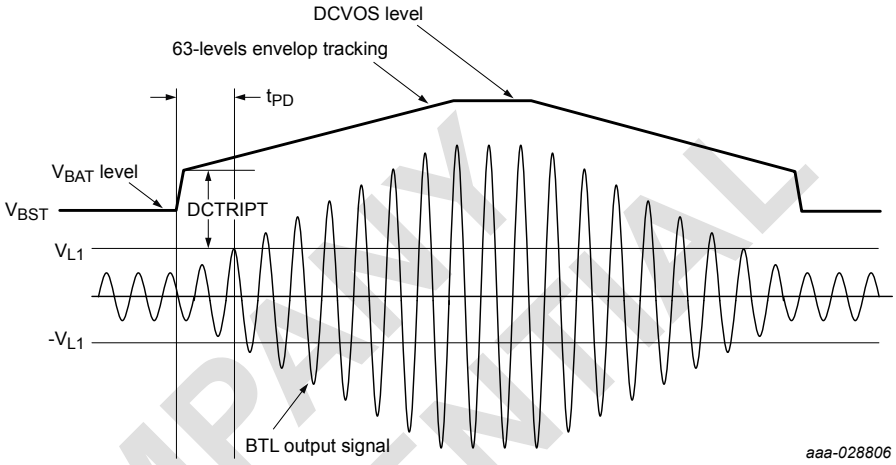


Figure 8. DC-to-DC tracking boost behavior

8.5.5 Coil current limitation

The TFA9894 embeds a current limitation function that allows to:

- Limit average current drawn from the battery.
- Adapt current to the coil saturation current specification and thus better optimize the size of the boost convert coil.

Drawback of such limitation is that it limits the output power. This current limitation is configured using the DCMCC parameter.

8.5.6 PFM Mode

In order to improve efficiency at lower output power, the TFA9894 embeds a dedicated Pulse Frequency Mode. Based on signal output level, the DC-DC will switch automatically between PFM and PWM modes for maximum efficiency at each power level.In PFM mode the DCDC switching frequency is variable and up to 2048 kHz. Above 2 MHz (when PFM mode reaches its maximum deliverable output power), the DC-DC will switch to a PWM mode with a fixed frequency of 2048 kHz.

8.6 Battery Supply Safeguard (BSS)

The TFA9894 employs a safeguard mechanism to protect the connected battery. This feature limits the TFA9894 current when the battery voltage falls below a programmable safeguard threshold. The safeguard mechanism is twofold:

- The TFA9894 hardware quickly adapts the maximum clip level at low battery, resulting in a clipped output audio signal.
- The firmware running on Coolflux DSP reduces the gain such that clipping (due to hardware clipper triggered) does not occur.

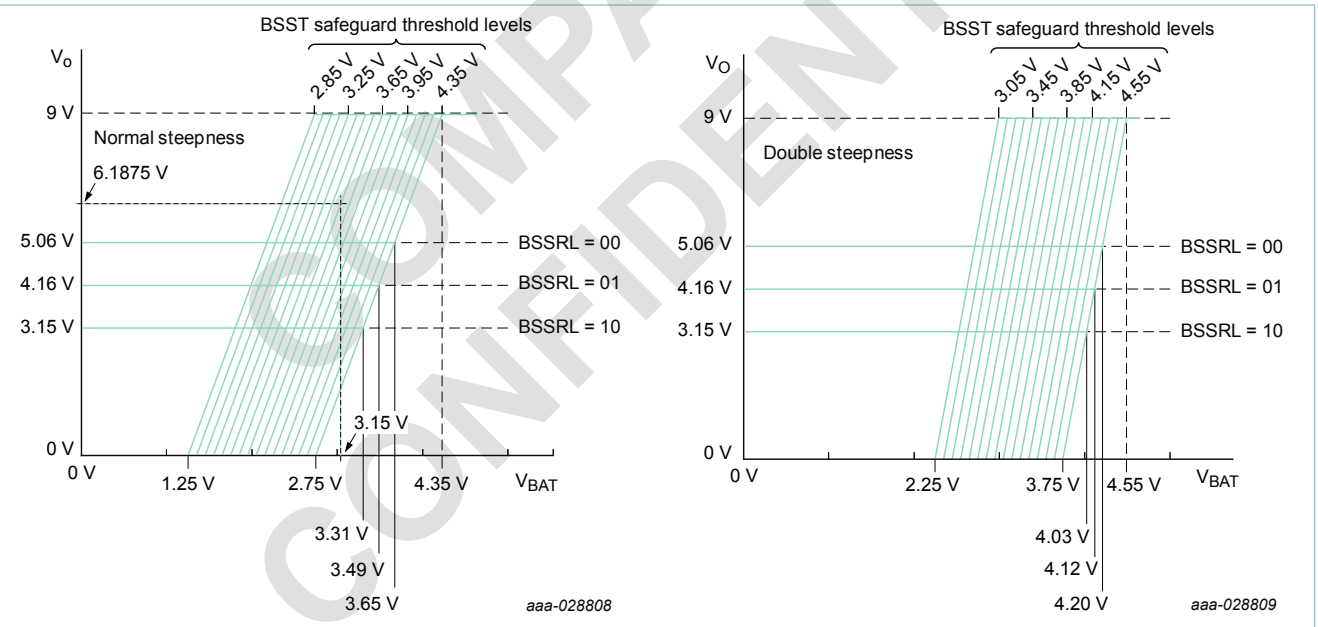
In order to limit the battery current, the BSS limits the maximum output voltage on the PWM outputs. The battery current depends on the level of the audio output voltage applied to the speakers. The BSS reduces the maximum output voltage once the battery

voltage falls below the safeguard threshold, thus limiting the current drawn from the battery. The battery voltage is sensed via pin V_{BAT}.

A graph of maximum output voltage as a function of the battery voltage at different battery supply safeguard settings is shown in Figure 9. The settings that determine the behavior of the BSS are:

- BSST sets the BSS safeguard threshold.
- BSSS sets the steepness of the slope of $V_{O(max)}$ vs.V_{BAT} with BSS active; $V_{O(max)}$ will be reduced by a factor of 5.625 V/V (BSSS = 0) or 11.25 V/V (BSSS = 1).
- BSSRL sets the clipping level; the maximum output voltage will not be reduced below this value, regardless of how far the battery voltage falls.

The maximum audio output voltage is assumed to be 9 V when V_{BAT} is at or exceeds the safeguard threshold. This is the maximum TFA9894 output voltage assuming 8 Ω loads are connected at the PWM outputs.



a. BSSS = 0

b. BSSS = 1

Figure 9. BSS Peak Output Voltage as a function of V_{BAT}

When V_{BAT} falls below the BSS safeguard threshold, the maximum output voltage is reduced as illustrated in Figure 9. If the battery safeguard threshold was set to 3.65 V (BSST = 1000; see Table 10) with BSSS = 0, for example, and the battery voltage drops by 0.5 V below this threshold to 3.15 V, the maximum output voltage will be limited to 6.1875 V (9 − (0.5 × 5.625)) (as illustrated in Figure 9). Note that if the output signal is already below this limit, it will not be reduced, hence, nothing happens on the output.

By default (BSSRL = 10), the maximum reduction in the $V_{O(max)}$ is limited to 5.85 V. So $V_{O(max)}$ will drop by 5.85 V, at a minimum value of 3.15 V, but not below. So if V_{BAT} drops by 1.04 V or more, below the selected safeguard level (1.04 V × 5.625 ≅ 5.85 V; BSSS = 0), any further fall in V_{BAT} has no effect on $V_{O(max)}$, which is clamped at 3.15 V minimum.

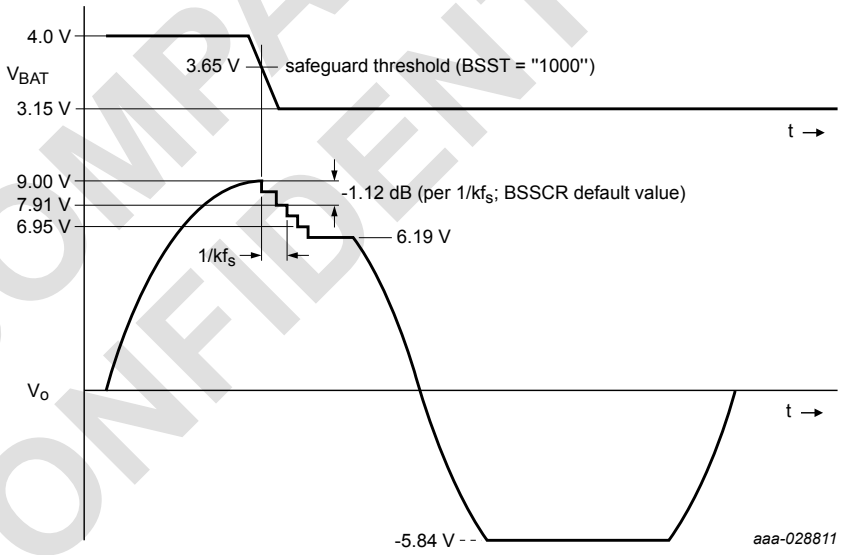
Notes:

- Setting BSSRL = 11 is not permitted as it can cause deadlock.

- Undervoltage protection is activated if the battery voltage drops below $V_{P(uvp)}$.

The dynamic behavior of the battery supply safeguard is illustrated in Figure 10 and Figure 11. In Figure 10, the battery voltage falls from 4.0 V to 3.15 V. The BSS mechanism is activated at the selected threshold (3.65 V). So the battery voltage falls 0.5 V below the threshold, which causes the maximum output voltage to fall by 2.81 V (0.5 × 5.625; BSSS = 0) to 6.19 V.

The BSS hardware clipper reacts very quickly to a fall in battery voltage and reduces the maximum output voltage by limiting the minimum and maximum PWM duty cycles. The result is a clipped signal at the output. The clip rate is programmable and is determined by the setting of I^2C control bits BSSCR (see Table 12). By default, the output signal is clipped at a rate of 1.12 dB per sample period ($1/kf_s$), in 2 steps. There is delay of $2/kf_s$ (maximum) between the battery voltage dropping below the safeguard threshold and the safeguard mechanism reacting (not shown in Figure 11).



k = 0.50 at a sample rate f_s of 96 kHz
k = 1.00 at a sample rate f_s of 32 kHz, 44.1 kHz or 48 kHz
k = 2.00 at a sample rate f_s of 16 kHz

Figure 10. BSS Clipped Output (HW Clipper)

The SpeakerBoost and Protection algorithm reacts after t_{resp} (approximately 5 ms with f_s = 48 kHz) to reduce the gain and limit distortion due to clipping (Figure 11). The SpeakerBoost and Protection algorithm only reduces the gain when the output signal is being clipped. As long as the output signal is below the clip level, the gain is not reduced. When the battery voltage rises again, the output voltage increases smoothly at a rate determined by the SpeakerBoost and Protection algorithm release rate (Table 14). The default release rate is 0.625 dB per second (so it takes 1.6 seconds, $t_{release}$, for the output voltage to rise by 1 dB).When the battery voltage rises back again, the battery safeguard is released and the output voltage increases back to it maximum level as illustrated in Figure 11.

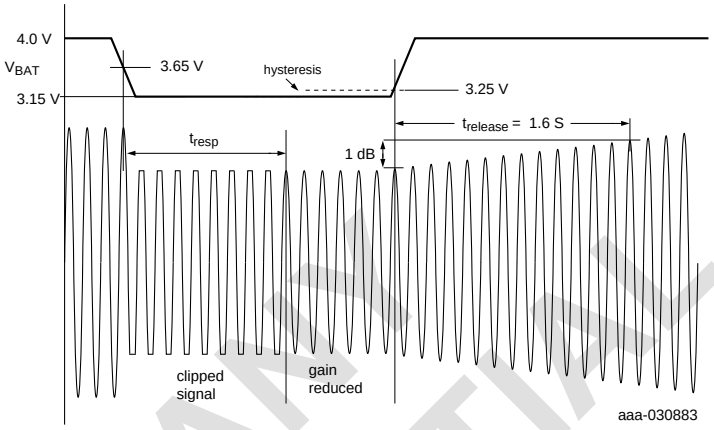


Figure 11. BSS Firmware Release Output Level

There is a programmable hysteresis between the lowest battery voltage and the release threshold. By default, the output voltage starts to increase when the battery voltage rises to 0.10 V above the lowest measured battery voltage; see Figure 11 and Table 15.

The firmware behavior depicted in Figure 11 illustrates a typical system response to a trigger of the BSS mechanism. However, this behavior may be affected by the different firmware features (see Section 8.14.1.3) that are enabled at the time the BSS is triggered. As such, the signal observed on the amplifier outputs may vary from the above description, specifically for the t_{resp} timing, the gain reduction and the $t_{release}$ timing.

To achieve a reaction time in the region of 40 µs (at a sample rate of 48 kHz), filtering on the battery sense input should be implemented as described in Section 14.1.

The battery safeguard mechanism (hardware clipping) can be bypassed by setting bit BSSBY to 1. The battery safeguard mechanism should be bypassed when the firmware counterpart is not implemented/running on the host.

Note: *To ensure the battery supply safeguard mechanism functions correctly, the sense pin (pin V_{BAT}) should be connected as close as possible to the positive battery terminal. Otherwise, the battery supply safeguard may be triggered too early due to the additional voltage drop caused by the track impedance.*

Table 10. Battery supply safeguard threshold level

BSST	battery safety threshold voltage (V)	
	BSSS = 0 (default)	BSSS = 1
0000	2.85	3.05
0001	2.95	3.15
0010	3.05	3.25
0011	3.15	3.35
0100 (default)	3.25	3.45
0101	3.35	3.55
0110	3.45	3.65
0111	3.55	3.75
1000	3.65	3.85

BSST	battery safety threshold voltage (V)	
1001	3.75	3.95
1010	3.85	4.05
1011	3.95	4.15
1100	4.05	4.25
1101	4.15	4.35
1110	4.25	4.45
1111	4.35	4.55

Table 11. Battery voltage source selection

BSSR	battery voltage measured
0	minimum value measured (default value)
1	average value measured

Table 12. Battery supply safeguard clip rate

BSSCR	clip rate (dB/sample)
00	0.56
01 (default)	1.12
10	2.32
11	infinite

Table 13. Output voltage reduction limit

BSSRL	maximum reduction in V_o (V)	$V_{o(max)}$ (V)
00	3.94	5.06
01	4.84	4.16
10 (default)	5.85	3.15
11[1]	not permitted	

[1] If BSSRL is set to 11, a deadlock situation can occur where the output is reduced to 0 V; the deadlock can only be resolved by a complete system reset.

Table 14. Battery supply safeguard release rate

BSSRR	Release rate (dB/s)	$t_{release}$ (s)[1]
000	0.626	1.6
001	0.626	1.6
010	0.626	1.6
011 (default)	0.625	1.6
100	0.5	2.0
101	0.417	2.4
110	0.357	2.8
111	0.313	3.2

[1] $t_{release}$ is the time taken for the output voltage to rise by 1 dB.

Table 15. Battery supply safeguard Hysteresis

BSSHY	Hysteresis setting (V)
00	no hysteresis
01	0.05
10 (default)	0.10
11	0.20

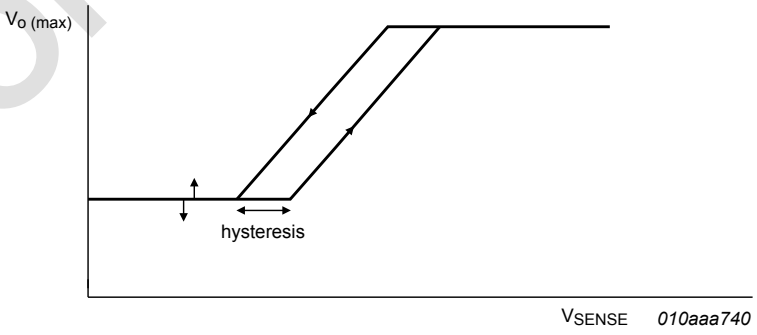


Figure 12. BSS Hysteresis of clip vs release thresholds

8.7 PWM

8.7.1 PWM High-pass filter

The high-pass filter (HPF) is implemented in the PWM controller. It blocks the DC components in the incoming audio stream. The cut-off frequency, $f_{high(-3dB)}$, is determined by the sample rate, f_s, and is defined in Equation 3:

$$f_{high(-3dB)} = \frac{-k \cdot f_s \cdot \ln(4095/4096)}{2\pi} \quad (3)$$

where k depends on the sample rate:

- k = 0.50 at a sample rate at f_s of 96 kHz
- k = 1.00 at a sample rate at f_s of 32 kHz, 44.1 kHz, or 48 kHz
- k = 2.00 at a sample rate at f_s of 16 kHz

The cutoff frequency, $f_{high(-3dB)}$, is about 1.9 Hz at a sample rate of 48 kHz. The high-pass filter is enabled by default and can be bypassed separately via I^2C control bits HPFBYP.

8.7.2 PWM controller

The PWM controller translates the digital input signal into a 3-level PWM output signal. The PWM switching frequency depends on the sample rate, as detailed in Table 16.

Table 16. Class-D PWM switching frequencies

Sample rate	f_{PWM}
f_s = 16 kHz or 32 kHz (sample rate)	256 kHz
f_s = 44.1 kHz	352.8 kHz
f_s = 48 kHz or 96 kHz	384 kHz
f_s = 16 kHz or 32 kHz; high performance (sample rate)	384 kHz

8.8 Output spectrum

The TFA9894 output spectrum has a sigma-delta converter characteristic. Figure 13 illustrates the output power spectrum of theTFA9894 when it is receiving a signal without audio content. The quantization noise is shaped above the band of interest. The corner frequency where the noise is increasing is given in Equation 4:

$$f_{corner} = 0.5 \cdot k \cdot f_s \quad (4)$$

where k depends on the sample rate, as described in Section 8.7.1.

When the SpeakerBoost and Protection algorithm is enabled (CoolFlux DSP is not bypassed), a pilot tone is added in the spectrum. This pilot tone has an amplitude of 100 mV at the class-D audio amplifier outputs. The frequency of the pilot tone is given in Equation 5:

$$f_{pilot} = \frac{k \times f_s}{1024} \quad (5)$$

where k depends on the sample rate, as described in Section 8.7.1.

The pilot tone is used in the measurement of the speaker voice coil temperature.

The impedance of the voice coil changes if the temperature changes. Current sensing is used to measure the voice coil impedance, using the pilot tone as a reference. Once the change in impedance has been measured, the SpeakerBoost and Protection algorithm uses the temperature coefficient of the coil to calculate the voice coil temperature. A notch filter, implemented in the SpeakerBoost and Protection algorithm, suppresses audio frequencies around the pilot tone to ensure that the voice coil temperature is measured accurately. The pilot tone disappears from the audio spectrum after about two seconds of audio silence (input audio stream below −70 dBFS)

The CoolFlux DSP output data is available on the TDM output. The pilot tone can optionally be included in this data stream (see Section 8.15.2).

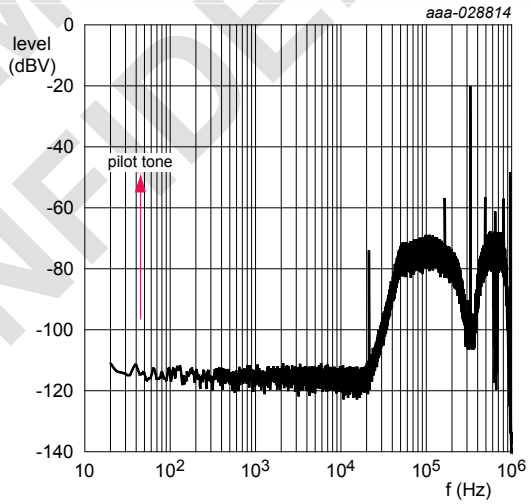


Figure 13. Output power spectrum, f_s = 48 kHz

8.9 Protection mechanisms

The following protection circuits are included in the TFA9894:

- OverTemperature Protection (OTP)
- UnderVoltage Protection (UVP)
- OverCurrent Protection (OCP)
- BrownOut Detection (BOD)
- WatchDog Timer (WDT)

The reaction of the device to fault conditions differs depending on the protection circuit involved.

8.9.1 OverTemperature Protection (OTP)

OTP prevents heat damage to the TFA9894. It is triggered when the junction temperature exceeds $T_{act(th\_prot)}$. When this happens, the output stages are set floating. OTP is cleared automatically via an internal timer, after which the output stages will start to operate normally again.

The overtemperature status can be monitored via status bit OTDS. The interrupt output pin (INT) is activated when this flag is raised (OTDS = 0). The OTP circuit is not the same as the temperature sensor circuit discussed in Section 8.10.3.

8.9.2 Supply voltage protection (UVP)

UVP prevent the device behaving unpredictably when V_{BAT} when is outside the specified operating range.

- UVP is activated, setting the outputs floating, if V_{BAT} drops below the under voltage protection threshold, $V_{uvp(VBAT)}$. When the supply voltage rises above $V_{uvp(VBAT)}$ again, the system will be restarted after approximately $t_{d(alarm)}$.

The undervoltage status can be monitored via status bits UVDS. The interrupt output pin (INT) is activated when UVDS flag is raised (UVDS = 0).

8.9.3 OverCurrent Protection (OCP)

OCP will detect a short circuit across the load or between one of the amplifier outputs and one of the supply lines. If the output current exceeds the over current protection threshold ($I_{O(ocp)}$), it will be limited to $I_{O(ocp)}$ while the amplifier outputs are switching (the amplifier is not powered down completely). This is called current limiting. The amplifier can distinguish between an impedance drop at the speaker and a low-ohmic short circuit across the load or to one of the supply lines. The impedance threshold depends on which supply voltage is being used:

- In the event of a short circuit across the load or a short to one of the supply lines, the audio amplifier is switched off completely. It will try to restart again after $t_{d(alarm)}$. If the short-circuit condition is still present after this time, this cycle will be repeated. Average dissipation will be low because of the short duty cycle.
- In the event of an impedance drop (e.g. due to dynamic behavior of the speaker), the same protection mechanism will be activated. The maximum output current is again limited to $I_{O(ocp)}$, but the amplifier will not switch off completely (thus preventing audio holes from occurring). This will result in a clipped output signal without artifacts.

The overcurrent status can be monitored via status bit OCDS. The interrupt output pin (INT) is activated when this flag is raised (OCDS = 1).

OCP can be bypassed by setting bits TSTOCP and BYPOCP to 1. Overcurrents are still flagged via bit OCDS when OCP is bypassed.

8.9.4 Brownout detection

The TFA9894 includes a BrownOut Detector (BOD) that flags when the digital supply voltage drops below a programmable threshold level. This protection prevents DSP misbehavior due to the digital supply voltage dropping below the minimum operating threshold. If MANROBOD is set to 1, the device manager will power down the device and restart. The host will then need to initiate a cold boot sequence (MANCOLD = 1; see Section 8.2.3) to reactivate the device. An interrupt will be generated to alert the audio

host to a brown-out if the BOD interrupt is enabled (IEBODNOK = 1). The host should then reload the SpeakerBoost and Protection algorithm protection configuration settings. The BOD is controlled by the manager and activated in all states except Power Down, Load I2C Settings and Mute & disable states (Figure 5). It is recommended to always power down & restart on a BOD event (MANROBOD = 1), as otherwise, the Coolflux DSP could be in a unknown state resulting in a misbehavior of the device.

The following I^2C settings are use to configure the BOD:

- **BODTHLVL** sets the brownout detection threshold voltage ($V_{th(BOD)}$; see Figure 14)
- **BODFILT** sets the BOD reaction time ($t_{d(BOD)}$). This is the length of time that V_{DDD} must be below the brownout detection threshold before a brownout is flagged. A voltage spike lasting less than the filter time will not cause the BOD to flag a brownout.
- **BODHYS** enables/disables BOD hysteresis (Figure 14). When hysteresis is enabled, the supply voltage needs to be $V_{hys(BOD)}$ above $V_{th(BOD)}$ before the BOD stops flagging the brownout.

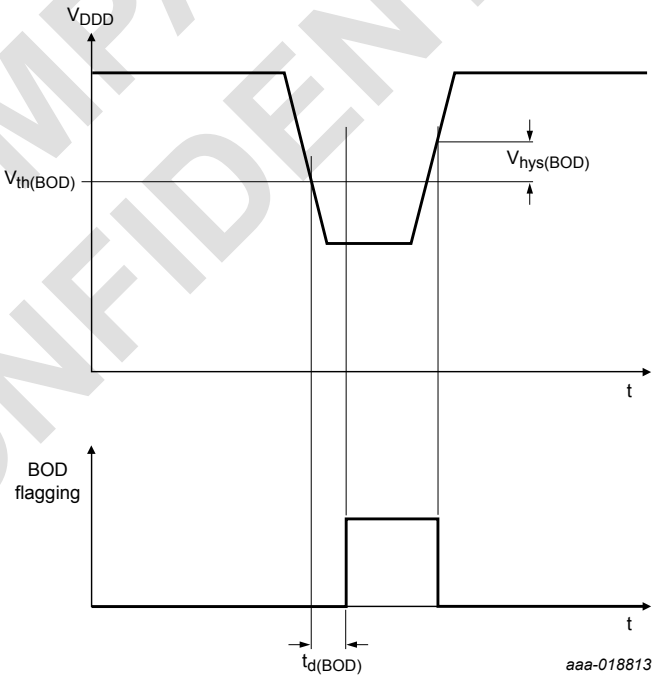


Figure 14. Brownout detection diagram

8.9.5 Watchdog Timer (WDT)

The watchdog timer detects timing errors in the CoolFlux DSP (timing errors can be generated if the supply voltage (V_{DDD}) is too low or a wrong reference clock is used and can affect the behavior of the SpeakerBoost and Protection algorithm or if the DSP firmware crashes.).

If MANWDE is set to 1, the device manager will power down the device in response to a watchdog timing error. The host will then need to initiate a cold boot sequence to reactivate the device. An interrupt will be generated to alert the audio host for a watchdog event, if the watchdog interrupt is enabled (IEWDS = 1). The host should then reload the SpeakerBoost and Protection algorithm protection configuration settings.

8.10 Monitoring and sensors

8.10.1 Battery supply voltage monitor

The battery is connected to pins V_{BAT}. The battery voltage level can be monitored on this via the I^2C-bus. Status bits BATS in the Battery status register can be used to calculate the battery voltage. This status readout is also used internally by the Battery supply safeguard mechanism (see Section 8.6) to monitor the battery level. The formula for the battery supply monitor is given in Equation 6:

$$V_{mon} = \frac{BATS \cdot 5.5}{1023} \quad (6)$$

If BATS = 670, for example, the converted battery voltage is 3.6 V.

8.10.2 V_{DDP} supply voltage monitor

The V_{DDP} voltage level can be monitored via the I^2C-bus. Status bits VDDPS in the V_{DDP} status register can be used to calculate V_{DDP} . The formula for the V_{DDP} supply monitor is given in Equation 7:

$$V_{mon} = \frac{VDDPS \cdot 13}{1023} \quad (7)$$

If VDDPS = 709, for example, the converted V_{DDP} voltage is 9.0 V.

8.10.3 Temperature sensor

The TFA9894 is equipped with a temperature sensor. The average die temperature can be read via bits TEMPS in the Temperature status register. For example, if TEMPS = 00011111, the die temperature is 31 °C. TEMPS is a two's complement value.

8.10.4 Current sensing

The current sensing circuit measures the differential output current, assuming this is equal to the speaker current. Current sensing is not disturbed by capacitance (< 1 nF) on the output lines or on the long speaker tracks. The current sensing transfer function is given in Equation 8:

$$TDM_{OutRMS} = I_{OutRMS} \,/\, 3.33 \text{ A [xFS]} \quad (8)$$

If the speaker current is 1.0 A_{RMS}, the current sense TDM output stream has a value of 0.3 full scale.

Figure 15 illustrates the current sense feedback paths. Current sense is primarily used inside CoolFlux DSP as part of the SpeakerBoost and Protection but can also be output on TDM for additional processing/usage inside host.

Note: *The delay between current sensing and voltage sensing can be adjusted via I^2C setting FRACTDEL. The range is one period of the sample rate with an accuracy of 1/64 × f_s.*

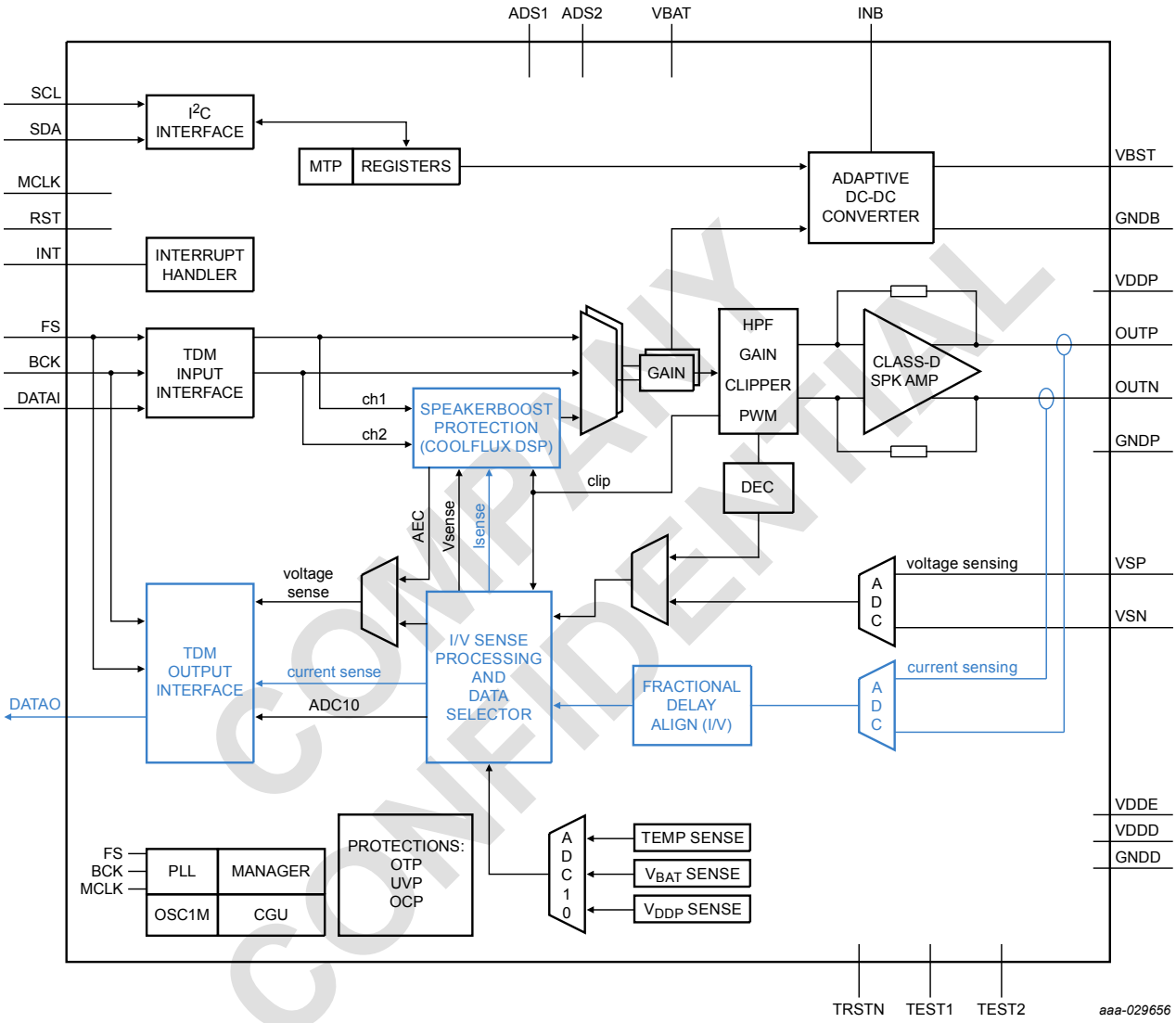


Figure 15. Current sense paths

8.10.5 Voltage sensing

In TFA9894, the voltage sensing is done either internally before signal is being output to speaker (this is similar to voltage sensing done on legacy devices of NXP Semiconductors), or externally at speaker pads. (see Figure 16). Voltage sense is primarily used inside CoolFlux DSP as part of the SpeakerBoost and Protection but can also be output on TDM for additional processing/usage inside host. For Acoustic Echo Cancellation support inside the host, it is preferred to use directly the DSP dedicated AEC output (to TDM) rather than voltage sensing.

For internal voltage sensing, the circuit measures the signal after the PWM generator. The amplifier transfer function from PWM generator to the amplifier outputs (OUTP and OUTN) is a fixed gain and is linear. The voltage sensing signal transfer function after the PWM generator to the TDM output is given in Equation 10:

$$TDM_{OutRMS} = V_{OutRMS} / 18.34\ \text{V}\ [\text{xFS}] \quad (9)$$

The voltage sense TDM output stream has a value of 0.054525 full scale when the voltage across the speaker is 1 V_{RMS}.

For external voltage sensing, the circuit measures the real voltage across the speaker by connecting the VSP and VSN input pins to the speaker pads. The speaker voltage signal is filtered, converted by an ADC (with an OSR of 128) and decimated to 1 f_s. The voltage sensing transfer function from the VSP / VSN input signals to the TDM output is given in Equation 10:

The voltage sense TDM output stream has a value of 0.04382 full scale when the voltage across the speaker is 1 V_{RMS}.

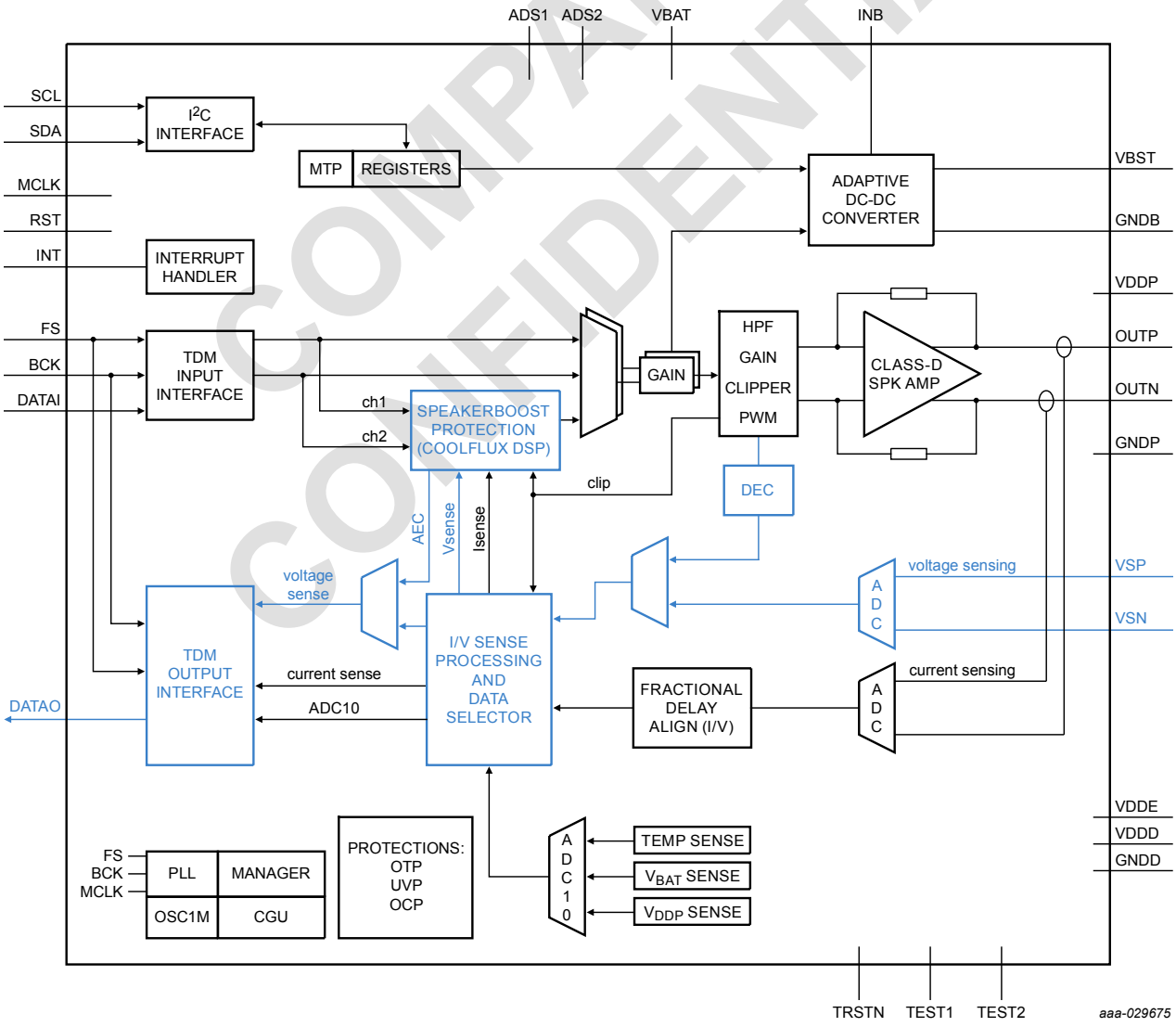


Figure 16. Voltage Sense paths

The voltage sense feedback signal is taken after the battery supply safe guard (BSS) hence the returned numerical value is impacted by the clipping described in Section 8.6.

Therefore it is really important, when using the voltage sensed data, to always associate the corresponding clipping information.

The clipping information is available from 2 sources:

- Digital Clipping flag, taken at the output of the battery safe guard, indicating that the digital signal provided to the Class-D amplifier is clipped by the BSG mechanism.
- Analog clipping flag, taken at the PWM generator output indicating that the amplifier is clipping.

These 2 clipping flag are available in following locations:

- TDM output (Section 8.15.2). In TDM each clip fag (analog or digital) is available either independently or combined as an OR function of the 2 flags.
- Flag (CLIPS bit). The status is reflecting a combined OR of the 2 flags.

The digital clipping flag can be disabled using the battery safe guard bypass (BSSBY bit). The analog clipping flag cannot be disabled and is always active.

8.11 Amplifier transfer function

The transfer function from the TDM input to the amplifier PWM outputs (RMS), assuming TDM input data at 0 dBFS is specified within range from −1 to +1 (full scale), is given in Equation 11 (This is measured with no load R_L on outputs OUTP / OUTN):

$$V_{O(RMS)} = TDM_{IN} \times (11.33)\,\mathrm{V}\ [\mathrm{V}] \tag{10}$$

This transfer gain is only valid at the default gain settings (INPLEV = ’0’ and TDMSPKG = ’0000’). Two separate gain blocks can influence this gain:

- **TDM input Level**: located after the TDM interface, attenuates the incoming signal by −6 dB or 0 dB (default), depending on I^2C setting INPLEV.TFA9894 full scale output is supported with an input signal at −6 dBFS. In order to support 0 dBFS input, the TDM input signal is attenuated by −6 dB internally using INPLEV.
- **TDM gain attenuation**: after the TDM input level gain, the signal gain of the full path up to the Class-D output can be amplified by between 6 dB and 21 dB using TDMDCG or TDMSPKG in the GAIN_ATT register. The TDM gain attenuation must be adapted to the V_{BST} level and speaker resistance for best performance. Recommended settings for TDMSPKG and TDMDCG are listed in Table 17.

Table 17. Recommended TDM gain settings

TDMSPKG/TDMDCG Settings (binary)	R_L = 4 Ω	R_L = 6 Ω	R_L = 8 Ω	R_L = 32 Ω
V_{BST} = 8.5 V (V_{BAT} = 3.6 V)	13 dB ("1000")	15 dB ("0110")	15 dB ("0110")	15 dB ("0110")
V_{BST} = 10.0 V (V_{BAT} = 4 V)	14 dB ("0111")	16 dB ("0101")	17 dB ("0100")	16 dB ("0101")

8.12 Low noise gain switch

The TFA9894 embeds a low-noise-gain switch feature used to reduce the noise at the amplifier output. The switching from normal to low noise gain is automatic and controlled through a zero-crossing detector to prevent audio artifacts. The switch reduces the analog gain in the amplifier to reduce the noise and this gain reduction is compensated with a digital gain to insure a correct output signal as depicted in Figure 17. By default, the switching is done automatically based on the output signal level. When the output signal raises above detection threshold the gain is immediately switched back to normal mode to allow the amplifier to deliver higher power. Low Noise Gain switch is controlled using the LNMODE setting. When LNMODE = "00" the switch is handled automatically with a signal detector. When LNMODE = "01" or "10" the gain is forced to normal gain and when LNMODE ="11" the gain is forced to low noise gain.

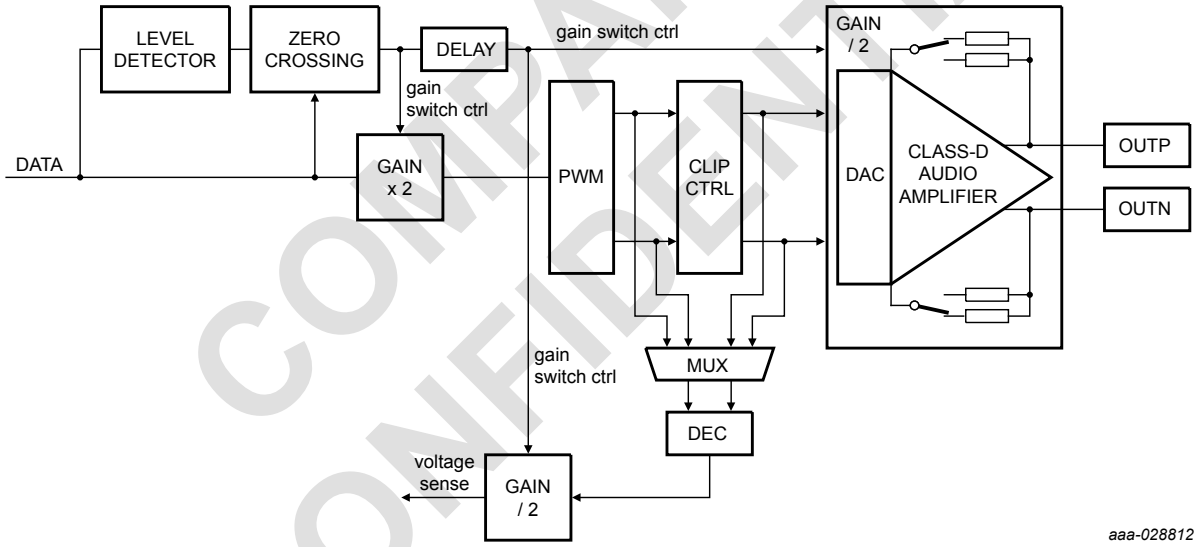


Figure 17. Low noise gain switch

8.13 96 kHz support

The TFA9894 supports 96 kHz audio sampling frequencies with the following limitations:

- DC-DC Adaptive Boost mode must be disabled (DCIE = 0).
- Low power mode must be disabled (LPM1MODE = "01").
- DSP must be bypassed.
- The stream content must be limited to 43 kHz bandwidth in the host providing the TDM stream.

8.14 Coolflux DSP

8.14.1 SpeakerBoost and Protection

The system level block-diagram of the CoolFlux DSP is depicted in Figure 18. The digital audio inputs are processed in the DSP and fed to the digital inputs of the amplifiers. The current and voltage flowing through (across) the speaker is measured continuously and provided as additional inputs to the SpeakerBoost and Protection algorithm. Input selector (InputSelector) allows to select between Left input, Right input or Mono (Left + Right)/2, as described in Table 18. For further description of Coolflux InputSelector settings please refer to Application Note.

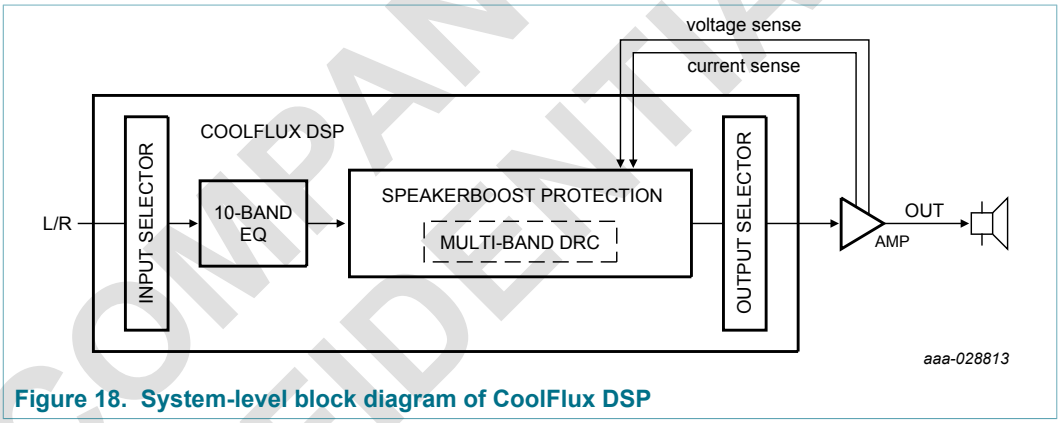


Figure 18. System-level block diagram of CoolFlux DSP

Table 18. Typical system Input Configurations

Mono Left	Mono Right	Mono Mix (L+R)/2
TDMSPKE = 1 (sink0 enable) TDMDCE = 0 (sink1 disable) TDMSPKS = 0 (sink0 uses slot0) - InputSelector(0xffff0f): CF uses sink0	TDMSPKE = 0 (sink0 disable) TDMDCE = 1 (sink1 enable) - TDMDCS = 1 (sink1 uses slot1) InputSelector(0xfffff1): CF uses sink1	TDMSPKE = 1 (sink0 enable) TDMDCE = 1 (sink1 enable) TDMSPKS = 0 (sink0 uses slot0) TDMDCS = 1 (sink1 uses slot1) InputSelector(0xffff01): CF uses sink0 and sink1

When the SpeakerBoost and Protection algorithm is enabled, a pilot tone is added. This pilot tone has an amplitude of 100 mV at the class-D audio amplifier outputs. The frequency of the pilot tone is given in Equation 12:

$$f_{pilot} = \frac{k \cdot f_s}{1024} \tag{11}$$

where k depends on the sample rate, as described in Section 8.7.1

The pilot tone is used in the measurement of the speaker voice coil temperature.

The impedance of the voice coil will change if the temperature changes. Current sensing is used to measure the voice coil impedance, using the pilot tone as a reference. Once the change in impedance has been measured, the SpeakerBoost and Protection

algorithm uses the temperature coefficient of the coil to calculate the voice coil temperature.

A notch filter, implemented in the SpeakerBoost and Protection algorithm, suppresses audio frequencies around the pilot tone to ensure the voice coil temperature is measured accurately. The pilot tone disappears from the audio spectrum after about two seconds of audio silence (input audio stream below −70 dBFS).

The CoolFlux DSP output data is available on the TDM output. The pilot tone is not included in the AEC reference data stream. See Section 8.15.2 on selecting the channel to be transmitted on the TDM output.

The CoolFlux DSP processes the incoming samples in blocks. The block size and corresponding delay are determined by the sample rate (see Table 19).

Table 19. Block size/delay for a given sample rate

Sample rate (kHz)	Block size (no. of samples)	Total DSP delay(s)[1]
44.1/48[2]	32	$2*32 / f_s + t_{LookAhead}$[3]

[1] The delay in the hardware processing ($28 / f_s$) is excluded.
[2] For f_s = 96 kHz the DSP must be disabled/bypassed
[3] $t_{LookAhead}$ is a buffer of 192 samples at fs.

The modules shown in the DSP block diagram are described in the following sections.

8.14.1.1 10-band equalizer

Ten fully programmable cascaded second-order biquad Infinite Impulse Response (IIR) filter sections have been integrated into the DSP. The IIR filters are implemented using the Direct Form 1 structure and can be configured individually (they are indexed 1 to 10). This makes it possible to implement any type of second-order filter (low-pass, high-pass etc.) using a variety of design methodologies (Butterworth, Chebyshev etc.) to achieve the required frequency response. The biquad filtering is implemented in 24-bit single precision according to the following transfer function:

$$H(z) = \frac{b_0 b_1 z^{-1} b_2 z^{-2}}{1 a_1 z^{-1} a_2 z^{-2}} \quad (12)$$

Coefficients b_0, b_1, b_2, a_1, and a_2 are all 24-bit fixed point values. An additional headroom value is used with each of the coefficients for maximum precision.

By default, the filters are disabled (headroom = −8388608) to minimize power consumption. Samples are processed in blocks of 32 samples (see Table 19) to enhance performance (as in the SpeakerBoost and Protection algorithm). The biquad filters do not introduce any additional buffering delay in the TFA9894.

To ensure that no significant audio artifacts are generated during processing, the coefficients and the input data should be aligned to ensure there is no digital clipping at 0 dB FS. This can be achieved by reducing the (TDM) input level, if necessary, or by configuring a section of the biquad filter bank to reduce the gain. Since the biquad filter bank was designed for 24-bit precision or more, 19-bit SNR range is available.

The biquads are processed sequentially from index 1 to index 10.

Biquad filters with indices 1 and 2 are processed internally in 48-bit double precision. These filters are recommended for low frequency filtering where the increased precision will be of most value. The coefficients remain single precision.

8.14.1.2 Multiband Dynamic Range Compressor (DRC)

A highly configurable and scalable DRC is available to improve audio performance. A block diagram of the DRC is shown in Figure 19.

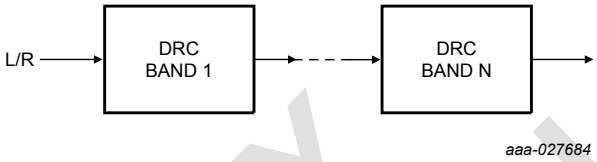


Figure 19. Simplified multi-band DRC block diagram

The audio input can be processed as a cascade of individually configurable band-limited DRCs. There is a pool of 3 sub-bands.

8.14.1.3 Speaker boost

The SpeakerBoost and Protection algorithm contains three main blocks:

- Audio processing
- Feature extraction
- Control matrix

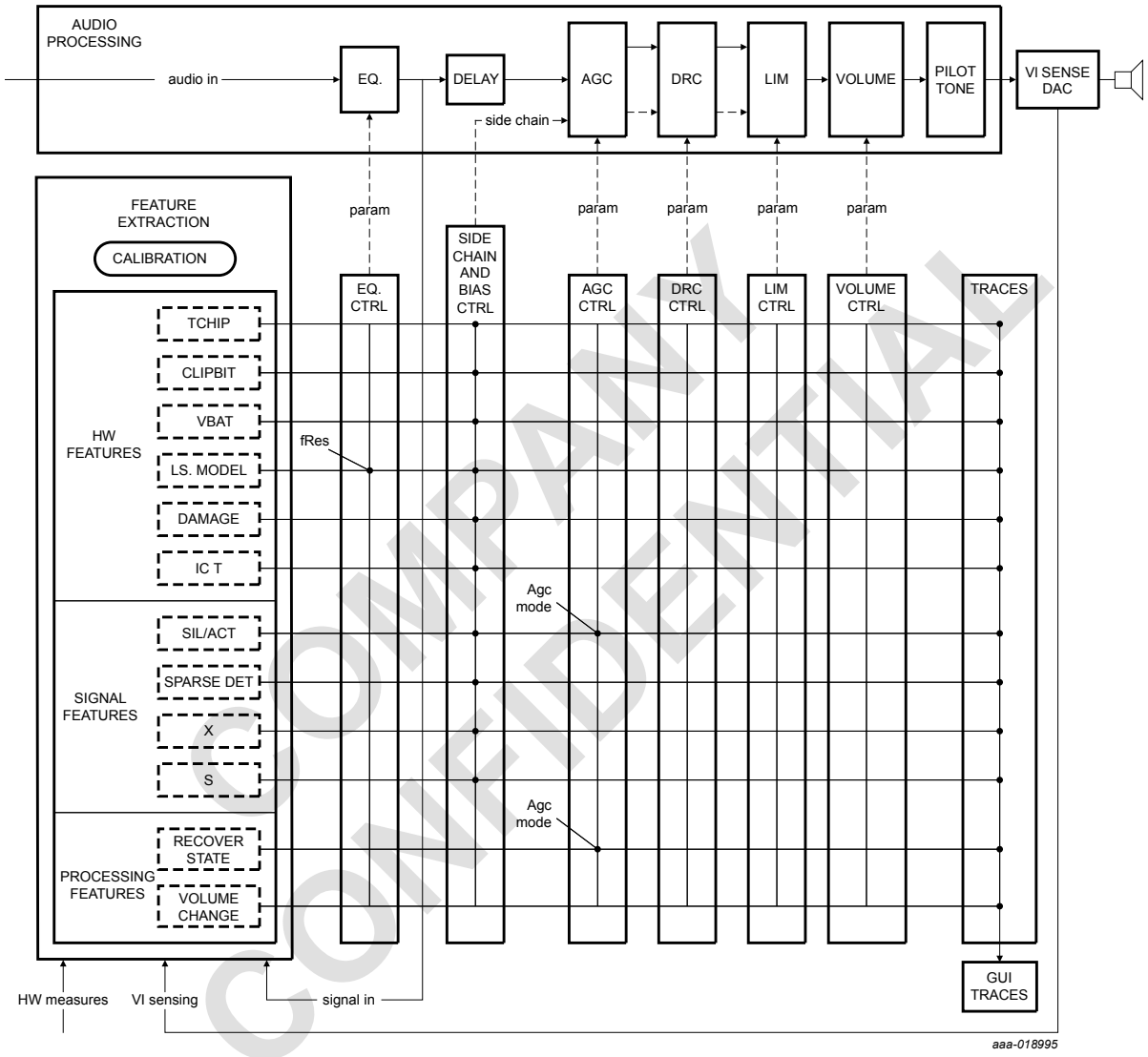


Figure 20. Algorithm block diagram

Audio processing

The Audio processing block bundles together all processing that directly affects the audio output signal. It contains the following modules (see Figure 20):

SBFilters: The SBFilters module compensates for the resonance peak. In addition, the frequency bandwidth can be reduced using a low cut filter to create signal headroom for higher frequencies and in this way increase SPL levels.

Delay: A delay is added to the audio signal to enable look-ahead in the control matrix.

Automatic Gain Control (AGC): AGC regulates the gain on the audio signal so that the average output level remains constant. Gain control is implemented using the signal energy of the side chain measured by an envelope detector.

Dynamic range compressor/limiter: Two Dynamic Range Compressors (DRC) with side chain control are used to compress and limit the output to prevent clipping and/or excursion overshoots. The first DRC is typically used to gently compress the

dynamic range in a way that still allows overshoots at the output. It acts as a kind of 'pre-compressor' for the next DRC stage which is generally used as a limiter. This arrangement produces a smoother overall compression effect. The second DRC/limiter then protects the output from exceeding the amplifier clip level and/or speaker excursion or any other limiting feature controlling the gain reduction stages.

Volume control: This module applies volume or muting to the output signal. It also smooths sudden changes in volume or muting to prevent click/pop artifacts.

Pilot tone: This module filters the output with a notch filter to free up bandwidth for a pilot tone. The pilot tone allows the coil resistance to be tracked at the low frequencies (DC resistance) used to measure the coil temperature.

Feature extraction

A set of features is extracted from HW sensors, VI sensing signals, the input signal, and user input. These features are used in the control matrix to adapt parameters and to create the side chain signal used to control the AGC and gain reduction in the DRC. The following features are currently implemented in (see Figure 20):

Hardware features:

- **Tchip**: IC temperature measured by on chip temperature sensor
- **ClipBit**: HW detection of amplifier clipping
- **vBat**: HW battery voltage sensing
- **Speaker model**: estimation and tracking of the speaker model.
  - **Impedance:** Speaker Impedance used to translate into Excursion based on Speaker parameters.
  - **T:** voice coil temperature
  - **Re:** voice coil DC resistance
  - **fRes:** resonance frequency of the speaker
  - **damage:** flag to indicate that the estimated speaker parameters are beyond the expected range

Signal features:

- **SparseSig**: presence of signals that are sparse in the frequency domain (such as sine waves)
- **Sil/Act**: discriminator between silence and activity
- **S**: Signal representing output level before any gain processing has been applied.
- **X**: Estimation of speaker membrane excursion before any gain processing has been applied. Estimated excursion is based on the speaker model

Algorithm features:

- **RecoveryState**: The recovery state is triggered when features and/or side chain change suddenly. Normally, the AGC gain reacts very slowly on these kinds of transitions which can cause high gain reduction in Compressor/Limiter and therefore also distortions in the output signal. However, when RecoveryState has been triggered, the AGC can be set into a fast reaction mode to quickly compensate for this.
- **VolumeChange**: When the user changes volume, the SpeakerBoost and Protection algorithm will gradually change the output level. During this transition the VolumeChange will be active. This mechanism is also used when muting.

Control matrix

Some audio processing blocks feature a number of parameters and/or control inputs that interact with the behavior of that module. These parameters and control inputs are dynamically controlled in a matrix, which implements a set of rules that define the effect, based on a number of features. The controls are represented as dots in the top level block diagram in Figure 20. Note that not all audio processing blocks have dynamically controlled parameters.

8.14.1.4 Speaker impedance calibration

The speaker must be calibrated before use. The speaker is generally calibrated once during the manufacturing process. The SpeakerBoost and Protection algorithm needs to know the speaker impedance at 25 °C to work properly.

The algorithm calculates the instantaneous impedance of the speaker at the ambient temperature and uses this information to estimate the speaker impedance at 25 °C.

The ambient temperature can be programmed via bits EXTTS in the Speaker control register or the algorithm can use the temperature sensor information provided via status bits TEMPS (see Section 8.10.3). EXTTS is a two's complement value. Bit TROS is used to select the source of the temperature used in the calibration calculation. If TROS = 0, the TFA9894 assumes that the speaker temperature and the die temperature are equal to the ambient temperature. Self heating in the TFA9894 is negligible during the speaker calibration process as long as the DC-to-DC converter is in Follower mode (the default setting). In DC-to-DC converter Boost mode, the die temperature will increase a few degrees due to self-heating, making calibration unreliable.

Table 20. Temperature reference selection

TROS	Temperature reference for the SpeakerBoost and Protection algorithm
0	TFA9894 temperature sensor information (TEMPS)
1	external temperature measured and specified via bits EXTTS

The speaker impedance can be calibrated once (MTPOTC = 1), or after every V_{DDD} power-on reset (MTPOTC = 0). If one-time calibration is selected, the result of the calibration is stored in MTP (Multi Time Programmable) non-volatile memory (after each power-on reset (POR), the MTP value is copied to its respective I^2C register). Once the one-time calibration sequence has been executed, bit MTPEX is set to 1 to indicate that speaker calibration has been completed. MTPEX can be reset to 0 with MTPOTC = 1 to execute one-time calibration again.

Note: *Speaker impedance calibration should be carried out at an ambient temperature of between 15 °C and 40 °C. If the speaker temperature and the die temperature are the same, the algorithm can use the temperature sensor information to calculate the reference temperature. Otherwise, the speaker temperature must be measured externally and programmed via the I^2C-bus. The SpeakerBoost and Protection algorithm must be configured, as appropriate for the connected speaker, before speaker calibration is activated.*

8.15 TDM interface

8.15.1 Functional description

The programmable TDM interface supports up to 16 slots in full-duplex, slave mode only, through 4 dedicated pins (FS/BCK/DATAI/DATAO).

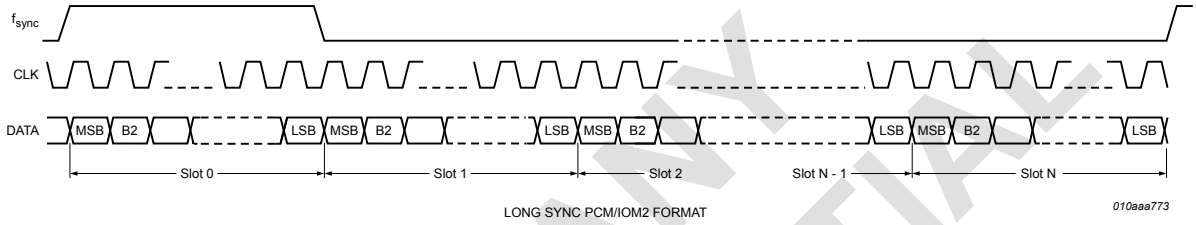


Figure 21. TDM interface format

An example TDM interface timing diagram is illustrated in Figure 21 and specific timings in Figure 22, showing the frame synchronization (sync) pulse, the data clock, and a single data line. The frame sync pulse indicates the start of a new frame. A frame consists of a configurable number of slots and each slot can represent a channel data sample. Note that empty slots are permitted (no data present during the sampling period). The frame sync period is the same as the sample rate period of all the input and output channels that are time-division multiplexed onto the data line.

The TDM interface is configured via the I^2C TDM_CONFIG registers (TDM_CONFIG0 to TDM_CONFIG4). The TDM interface settings can be divided into five sections:

- **Overall settings**, used to enable the interface.
- **Signal structure**, in which the structure of the frame sync pulse (FS), the bit clock (BCK) and the data pins (DATAI, DATAO) are configured.
- **Frame structure**, determines how the data is configured in a frame.
- **Line settings**, determine the output configuration for unused bits.
- **Channel selection**, selects the audio content on the data inputs and outputs.

8.15.1.1 Overall settings

The TDM interface is enabled through the following settings:

- **TDME**, to enable and disable the TDM interface
- **TDMDCE, TDMSPKE**, to enable audio input channels 0 and 1 (sink0/sink1)
- **TDMCSE, TDMVSE, TDMCFE, TDMCF2E**, to enable data output channels 0, 1, 2 and 3 (source0/source1/source2/source3)

Note: *The data clock (on pin BCK) or the frame synchronization pulse (on pin FS) must be selected as the PLL references clock (REFCKEXT must be set to "00" for BCK or "01" for FS).*

8.15.1.2 TDM signal structure

The signal structure indicates how the signaling on the input/output pins is constructed. The signal structure control settings need to be in line with the signals received on the TDM input/output pins. The default settings conform to the Philips I^2S format.

- **TDMNBCK** sets the number of bit clock periods (on the BCK pin) in one frame sync period (FS pin). For example, if the TDM interface is configured for 8 slots per frame

(see TDMSLOTS) with 16 bits in each slot (see TDMSLLN) and no bits remaining after the last slot (see TDMBRMG), then 128 periods (8 × 16) must be selected.

- **TDMCLINV** selects edge-triggering for transmitted/received data. The default (TDMCLINV = 0) is rising edge on BCK for data received, and falling edge for data transmitted. If TDMCLINV = 1, data received is triggered on the falling edge of BCK and transmitted data on the rising edge.
- **TDMFSPOL** sets the polarity of the start of the frame sync signal; slot 0 starts on the rising edge of the frame sync pulse when TDMFSPOL = 0 and on the falling edge if TDMFSPOL = 1.

8.15.1.3 TDM frame structure

The frame structure indicates how data bits are coded in a frame sync period:

- **TDMSLOTS** sets the number of slots in a frame sync period; default is two slots (as in the I^2S interface).
- **TDMSLLN** sets the number of bits in a slot.
- **TDMBRMG** specifies the number of bits remaining at the end of the last slot; for example, if the number of bit clock periods in a frame sync period is set to 100 (TDMNBCK) and the number of slots to 4 with 24 bits per slot, then 4 bits will remain after the last slot (00100).
- **TDMSSIZE** sets the bit length of the audio samples; value cannot be greater than TDMSLLN.
- **TDMADJ** sets the data adjustment. If the data is justified to the Most Significant Bit (MSB), the MSB will be aligned with the frame sync edge, independent of the number of bits selected. If LSB justified, then the LSB is aligned with the frame sync edge and the MSB location will depend on the number of bits used (as indicated by TDMSSIZE).
- **TDMDEL** determines whether or not the slots are delayed by one data clock period; the Philips I^2S format specifies a single clock period delay (default setting).

8.15.1.4 Line settings

The line settings determine how the unused bits are transmitted:

- **TDMTXDFO** selects the data format of the unused bits in a slot when data is transmitted (output). These ‘remaining’ bits can be transmitted zero, tri-state or the MSB bits can be transmitted (sign extension for MSB justified configuration).
- **TDMTXUS** sets the format of the unused slots on the DATAO data pin; these ‘remaining’ slots can be all zeros,or tri-state.

8.15.1.5 Channel selection

The following control bits configure TDM interface input signal channel selection:

- **TDMSPKS:** indicates which slot is selected to receive the audio signal on channel 0 (sink0) to be amplified and output on OUTP/OUTN
- **TDMDCS:** indicates which slot is selected to receive the audio signal on channel 1 (sink1) to be used internally for DC-DC activation in stereo setup (2 × TFA9894) using a single DCDC.

The following control bits configure TDM interface output signal channel selection:

- **TDMCS, TDMVS, TDMCFS, TDMCF2S:** indicates which slot is used to transmit output data channel 0, 1, 2 and 3 (source0, source1, source 2 and source 3)

The transmitted data selection/mapping is detailed in Section 8.15.2.

8.15.2 TDM output interface mapping

The TDM interface is used to receive mono/stereo audio streams and to output sensed data. It can be embedded in a multi-slot configuration, but internally the TFA9894 only supports maximum of 2 slots input and maximum 4 slots output configuration as described below

Input data (sink0 and sink1):

- Audio channel one (sink0 by default): This channel is the main audio channel, from TDM input to OUTP/OUTN pins.
- Audio channel two (sink1 by default): This channel is the secondary audio channel dedicated to DC-DC activation in stereo configurations (2 × TFA9894)

Output Data (mapped on source2 and source3), selected with TDMCFSEL, TDMCF2SEL bits:

- DSP audio output
- AEC Reference
- Loopback (from sink0 or sink1)

Output data (mapped on source0 and source1):

- Voltage sense signal, Current sense signal
- Temperature and battery voltage
- Battery safeguard minimum level ($V_{BAT(min)}$)
- Class D power voltage monitor (V_{DDP})
- Clipping flags (analog & digital)

From Section 8.15.2.1 to Section 8.15.2.8:

- The source0 and source1 configurations are selected using TDMSRCMAP bits.
- The sensed values A and B are selected using TDMSRCAS and TDMSRCBS bits
- The clip bits can be enabled/disabled using TDMSRCACLIP and TDMSRCBCLIP bits

Table 21. TDM supported output data map

Mode	No. of Slots	Source	Slot Size (bits)	Supported	Comments
Mono	1	-	16/24	no	not enough bandwidth (on 1 slot) to return required SpeakerBoost data for TFA9894.
		Slot 1 → Source0 or Source 1	32	yes	TFA9894 uses 1 slot of 32 bits for return (output) path (see Section 8.15.2.4).
Mono	2	Slot 1 → Source0 Slot 2 → Source1	16/24/32	yes	a single TFA9894 uses 2 slots (over 2) for return (output) path (see Section 8.15.2.1 to Section 8.15.2.3).
Stereo	2	-	16/24	no	not enough bandwidth (on 2 slots) to return required SpeakerBoost data for both TFA9894 devices.
		Slot 1 → Source0 or Source 1	32	yes	each TFA9894 uses 1 slot of 32 bits for return (output) path (see Section 8.15.2.8).
Stereo	4	Slot 1 → Source0 Slot 2 → Source1	16/24/32	yes	each TFA9894 uses 2 slots (over 4) for return (output) path (see Section 8.15.2.5 to Section 8.15.2.7).

8.15.2.1 Mono_2slot_32bit output mapping

Table 22 describes the TDM slot output mapping for mono, using 2 × 32-bit output slots for a single TFA9894. (TDMSRCMAP = "000")

Table 22. Mono_2slot_32bit output mapping

Description	Slot no.	Bits	Comments
sense data 1 (source0)	1	31:16	current sensing
		15:14	analog clip flags (Bit_15 reserved, Bit_14 clip flag)
		13:12	digital clip flags (Bit_13 reserved, Bit_12 clip flag)
		11:10	header indicating type of data output on bits[9:0]: 00: battery level (V_{BAT}) 01: temperature level (Temp) 10: Battery Safeguard Level ($V_{BAT(min)}$) 11: ClassD Power Voltage (V_{DDP})
		9:0	10-bit monitored value corresponding to header (bits[11:10]) This 10-bit value is a time-multiplexed buffer of 4 values identified by header in bits[11:10]. Values (V_{BAT}/Temp/V_{DDP}/$V_{BAT(min)}$) are output cyclically at $f_s/4$.
sense data 2 (source1)	2	31:16	voltage sensing
		15:14	analog clip flags (Bit_15 reserved, Bit_14 clip flag)
		13:12	digital clip flags (Bit_13 reserved, Bit_12 clip flag)
		11:10	header indicating type of data output on bits[9:0]: 00: battery level (V_{BAT}) 01: temperature level (Temp) 10: Battery Safeguard Level ($V_{BAT(min)}$) 11: ClassD Power Voltage (V_{DDP})
		9:0	10-bit monitored value corresponding to header (bits[11:10]) This 10-bit value is a time-multiplexed buffer of 4 values identified by header in bits[11:10]. Values (V_{BAT}/Temp/V_{DDP}/$V_{BAT(min)}$) are output cyclically at $f_s/4$.

8.15.2.2 Mono_2slot_24bit output mapping

Table 23 describes the TDM slot output mapping for mono, using 2 × 24-bit output slots for a single TFA9894. (TDMSRCMAP = "001")

Table 23. Mono_2slot_24bit output mapping

Description	Slot no.	Bits	Comments
sense data 1 (source0)	1	23:8	current sensing
		7:0	voltage sensing: 8 MSBs
sense data 2 (source1)	2	23:16	voltage sensing: 8 LSBs
		15:14	analog clip flags (Bit_15 reserved, Bit_14 clip flag)
		13:12	digital clip flags (Bit_13 reserved, Bit_12 clip flag)
		11:10	header indicating type of data output on bits[9:0]: 00: battery level (V_{BAT}) 01: temperature level (Temp) 10: Battery Safeguard Level ($V_{BAT(min)}$) 11: ClassD Power Voltage (V_{DDP})
		9:0	10-bit monitored value corresponding to header (bits[11:10]) This 10-bit value is a time-multiplexed buffer of 4 values identified by header in bits[11:10]. Values (V_{BAT}/Temp/V_{DDP}/$V_{BAT(min)}$) are output cyclically at $f_s/4$.

8.15.2.3 Mono_2slots_16bits output mapping

Table 24 describes the TDM slot output mapping for mono, using 2 × 16-bit output slots for a single TFA9894 (TDMSRCMAP = "010")

Table 24. Mono_2slot_16bit output mapping

Description	Slot no.	Bits	Comments
sense data 1 (source0)	1	15:2	current sensing 14-bit data returned
		1	analog clip flag ORed with digital clip flag
		0	sync bit: 1 indicates beginning of new 10-bit data frame for sensed data; sensed values are output on slot 2, in bit[01] and bit[10]
sense data 2 (source1)	2	15:2	voltage sensing 14-bit data returned
		1	sensed value A (1 bit over 10; synchronized with sync bit of slot 1
		0	sensed value B (1 bit over 10; synchronized with sync bit of slot 1
			Notes • Sensed values A and B are transmitted over 10 slots (since 10-bit data) and reconstructed in the host • Sensed values A and B are selectable (via I^2C) from: V_{BAT}, Temp, V_{DDP}, $V_{BAT(min)}$ (default is V_{BAT} for both)

8.15.2.4 Mono_1slot_32bit output mapping

Table 25 describes the TDM slot output mapping for mono, using 1 × 32-bit output slot for a single TFA9894. (TDMSRCMAP = "011")

Table 25. Mono_1slot_32bits output mapping

Description	Slot Nbr	Bits	Comments
sense data 1 (source 0 or source1)	1	31:18	current sensing 14-bit data returned
		17	analog clip flag ORed with digital clip flag
		16	sync bit: 1 indicates beginning of new 10-bit data frame for sensed data; sensed values are output on bit[01] and bit[10]
		15:2	voltage sensing 14-bit data returned
		1	sensed value A (1 bit over 10; synchronized with sync bit (bit 16)
		0	sensed value A (1 bit over 10; synchronized with sync bit (bit 16)
			Notes • Sensed Value A & B are transmitted over 10 slots (since 10-bit data) and reconstructed in the Host • Sensed Value A & B are selectable (through I^2C) among: V_{BAT}, Temp, V_{DDP}, $V_{BAT(min)}$; by default Sensed Value A = V_{BAT} and Value B = V_{BAT}

8.15.2.5 Stereo_4slot_32bit output mapping

This mode is identical to Section 8.15.2.1 but with 2 devices connected to the TDM lines, hence 4 slots are used instead of 2.

8.15.2.6 Stereo_4slots_24bits output mapping

This mode is identical to Section 8.15.2.2 but with 2 devices connected to the TDM lines, hence 4 slots are used instead of 2.

8.15.2.7 Stereo_4slots_16bits output mapping

This mode is identical to Section 8.15.2.3 but with 2 devices connected to the TDM lines, hence 4 slots are used instead of 2.

8.15.2.8 Stereo_2slots_32bits output mapping

This mode is identical to Section 8.15.2.4 but with 2 devices connected to the TDM lines, hence 2 slots are used instead of 1.

8.15.2.9 Non-optimized output mapping

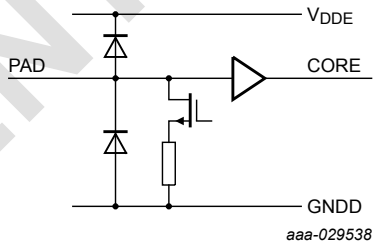
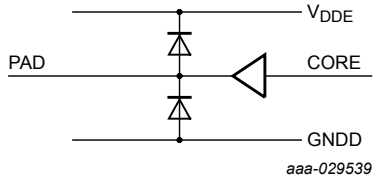
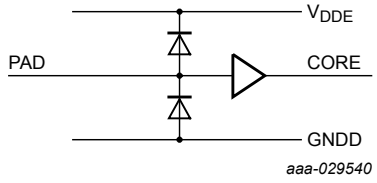
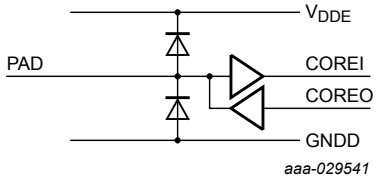
Table 26 describes the TDM slot output mapping for non-optimized mode, using 2 output slots (16 bits, 24 bits, or 32 bits) for a single TFA9894. (TDMSRCMAP = "100")

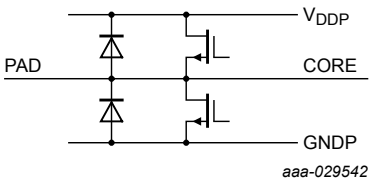
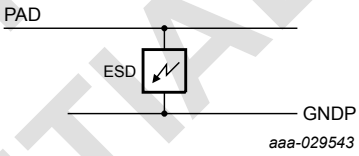
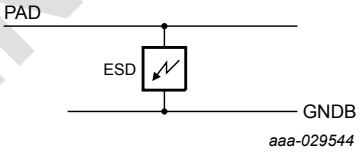
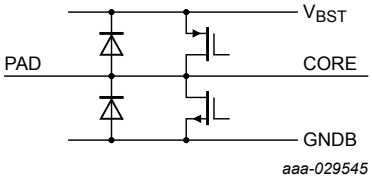
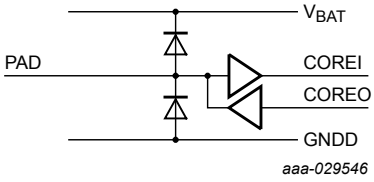
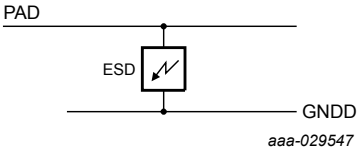
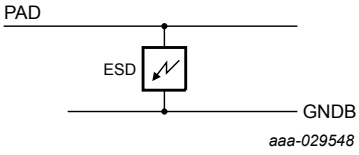
Table 26. Non-optimized output mapping

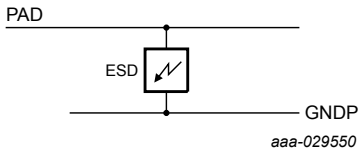
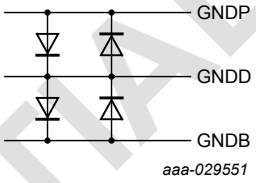
Description	Slot No.	Bits	Comments
sense data 1 (source0)	1	15:0 or 23:8 or 31:16	current sensing
		others	unused
sense data 2 (source1)	2	15:0 or 23:8 or 31:16	voltage sensing
		others	unused

9 Internal circuitry

Table 27. Internal circuitry

Pin	Symbol	Equivalent circuit
E1, C6	RST, TRSTN	
D5,D1	INT, DATAO	
D4, D3, D2, C2, B2, C1, C4, B4, A1	ADS1, ADS2, DATAI, FS, BCK, SCL, MCLK	
C5	SDA	

Pin	Symbol	Equivalent circuit
G4, G6	OUTP, OUTN	
E6	VSP	
E3	VSN	
G1, G2, G3	INB	
E5, E4	TEST1, TEST2	
D6, A2, A3, B3, C3	VBAT, VDDD, VDDE	
H1, H2, H3	VBST	

Pin	Symbol	Equivalent circuit
H4, H5, H6	VDDP	
F5, G5, F1, F2, F3, A4, A5, A6, B1, B5, B6, E2, F4, F6	GNDP, GNDB, GNDD	

10 I2C-bus interface and register settings

The TFA9894 supports the 400 kHz I^2C-bus microcontroller interface mode standard. The I^2C-bus is used to control theTFA9894 and to transmit and receive data. The TFA9894 can only operate in I^2C slave mode, as a slave receiver or as a slave transmitter.

10.1 TFA9894 addressing

The TFA9894 is accessed via an 8-bit code. Bits 1 to 7 contain the device address. Bit 0 (R/W) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for stereo applications. Address selection is via pins ADS1 and ADS2. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively, of the device address. The generic address is independent of pins ADS1 and ADS2.

Table 28. Address selection via pins ADS1 and ADS2

ADS2 pin voltage (V)	ADS1 pin voltage (V)	Address	Function
0	0	01101000	for write mode
		01101001	for read mode
0	V_{DDD}	01101010	for write mode
		01101011	for read mode
V_{DDD}	0	01101100	for write mode
		01101101	for read mode
V_{DDD}	V_{DDD}	01101110	for write mode
		01101111	for read mode
don't care	don't care	00011100 (generic address)	for write mode
		00011101 (generic address)	for read mode

10.2 I^2C-bus write cycle

The sequence of events that must be followed when writing data to the I2C-bus registers of the TFA9894 is detailed in Table 29. One byte is transmitted at a time. Each register stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The write cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA9894, followed by the R/W bit set to 0.
3. The TFA9894 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA9894 register address to which the first data byte is written.
5. The TFA9894 asserts an acknowledge.
6. The microcontroller transmits the first byte (the most significant byte).
7. The TFA9894 asserts an acknowledge.

8. The microcontroller transmits the second byte (the least significant byte).
9. The TFA9894 asserts an acknowledge.
10. The microcontroller can either assert the stop condition (P) or continue transmitting data by sending another pair of data bytes, repeating the sequence from step 6. In the latter case, the targeted register address has been auto-incremented by the TFA9894.

Table 29. I^2C bus write cycle

Start	TFA9894 address	R/$\overline{W}$		TFA9894 first register address		MSB		LSB		More data...	Stop
S	01101A_2A_1	0	A	ADDR	A	MS1	A	LS1	A	<..>	P

10.3 I^2C-bus read cycle

The sequence of events that must be followed when reading data from the I^2C-bus registers of the TFA9894 detailed in Table 30. One byte is transmitted at a time. Each of the registers stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The read cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA9894, followed by the R/W bit set to 0.
3. The TFA9894 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA9894 register address from which the first data byte is read.
5. The TFA9894 asserts an acknowledge.
6. The microcontroller asserts a repeated start (Sr).
7. The microcontroller retransmits the device address followed by the R/W bit set to 1.
8. The TFA9894 asserts an acknowledge.
9. The TFA9894 transmits the first byte (the MSB).
10. The microcontroller asserts an acknowledge.
11. The TFA9894 transmits the second byte (the LSB).
12. The microcontroller asserts either an acknowledge or a negative acknowledge (NA).
    - If the microcontroller asserts an acknowledge, the target register address is auto-increased by the TFA9894 and steps 9 to 12 are repeated.
    - If the microcontroller asserts a negative acknowledge, the TFA9894 frees the I^2C-bus and the microcontroller generates a stop condition (P).

Table 30. I^2C-bus read cycle

Start	TFA9894 address	R/$\overline{W}$		First register address			TFA9894 address	R/$\overline{W}$		MSB		LSB		More data...		Stop
S	01101A_2A_1	0	A	ADDR	A	Sr	01101A_2A_1	1	A	MS1	A	LS1	A	<....>	NA	P

10.4 I²C-bus registers

10.4.1 I²C registers summary table

Table 31. I²C registers summary table

Register	Address	Access	Reset	Module
sys_control0	0x00	RW	0x8245	SystemControl
sys_control1	0x01	RW	0x11ca	SystemControl
sys_control2	0x02	RW	0x55c8	SystemControl
device_revision	0x03	R	0x1a94	DeviceRevision
clock_control	0x04	RW	0x0000	ClockControl
clock_gating_control	0x05	RW	0x000e	ClockGating
status_flags0	0x10	R	0x021d	StatusFlags
status_flags1	0x11	R	0x0004	StatusFlags
status_flags2	0x12	R	0x018f	StatusFlags
status_flags3	0x13	R	0x0000	StatusFlags
battery_voltage	0x15	R	0x03ff	BatterySensor
temperature	0x16	R	0x0100	TemperatureSensor
vddp_voltage	0x17	R	0x0000	VddpSensor
tdm_config0	0x20	RW	0x0707	TDMConfiguration
tdm_config1	0x21	RW	0x8110	TDMConfiguration
tdm_config2	0x22	RW	0x3c0f	TDMConfiguration
tdm_config3	0x23	RW	0x0410	TDMConfiguration
tdm_config4	0x24	RW	0x5432	TDMConfiguration
interrupt_out_reg	0x40	R	0x0000	InterruptHandler
interrupt_in_reg	0x44	W	0x0000	InterruptHandler
interrupt_enable_reg	0x48	RW	0x0001	InterruptHandler
interrupt_polarity_reg	0x4c	RW	0xffe9	InterruptHandler
bat_prot_config	0x50	RW	0x9391	BatterySafeguard
cf_audio_control	0x51	RW	0x0000	CoolfluxControl
amplifier_config	0x52	RW	0xb617	Amplifier
gain_att_control	0x57	RW	0x0366	GainControl
low_noise_gain_control0	0x58	RW	0x0081	LowNoiseGainControl
mode1_detector_control0	0x5a	RW	0x0040	LowNoiseGainControl
tdm_source_control	0x5d	RW	0x0790	TDMSrcConfiguration
cursense_comp_control	0x61	RW	0x0073	CurSenseControl
dcdc_control0	0x70	RW	0xffde	DCDCControl
dcdc_control1	0x71	RW	0x018d	DCDCControl
dcdc_control2	0x72	RW	0x44e8	DCDCControl

Register	Address	Access	Reset	Module
dcdc_control3	0x73	RW	0x3806	DCDCControl
cf_controls	0x90	RW	0x0001	CoolfluxControl
cf_mad	0x91	RW	0x0000	CoolfluxControl
cf_mem	0x92	RW	0x0000	CoolfluxControl
cf_status	0x93	R	0x0000	CoolfluxControl
mtpkey2_reg	0xa1	RW	0x0000	MTPKey
mtp_status	0xa2	R	0x0003	MTPStatus
mtp_data_out_msb	0xa5	R	0x0000	MTPData
mtp_data_out_lsb	0xa6	R	0x0000	MTPData
temp_sensor_config	0xb1	RW	0x0000	TempSensor
software_profile	0xe0	RW	0x0000	SoftwareProfile
software_vstep	0xe1	RW	0x0000	SoftwareProfile
KEY2_protected_MTP0	0xf0	RW	0x0000	Calibration

10.4.2 I²C registers descriptions

Below register tables are under definition and subject to change.

Table 32. SYS_CONTROL0- address 00h reset value 0x8245h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	reserved	RW	1*	
14	DPSA	RW		Enable DPSA
			0*	DPSA off
			1	DPSA on
13	HPFBYP	RW		Bypass High Pass Filter
			0*	enable
			1	bypass
12	BSSS	RW		V_{bat} protection steepness
			0*	5.625 V/V
			1	11.25 V/V
11	TSTOCP	RW		OCP testing control
			0*	off
			1	on

Bit	Symbol	Access	Value	Description
10	BYPOCP	RW		Bypass OCP
			0*	OCP active
			1	OCP bypassed
9	FSSSEL	RW		Audio sample reference
			0	TDM data valid
			1*	CGU FS pulse gen
8:7	INTP	RW		Interrupt config
			0*	active low
			1	active high
			2	pull up
			3	pull down
6	AMPC	RW		CoolFlux control over amplifier
			0	no control
			1*	control
5	SBSL	RW		Coolflux configured
			0*	Coolflux not configured
			1	Coolflux configured
4	DCA	RW		Enable DCDC Boost converter
			0*	boost converter in follower mode
			1	enable boost mode
3	AMPE	RW		Enable Amplifier
			0*	tristate
			1	switching/active
2	CFE	RW		Enable CoolFlux DSP
			0	disable
			1*	enable
1	I2CR	RW		I^2C reset - Auto clear
			0*	Normal
			1	Reset
0	PWDN	RW		Power-down control
			0	Operating
			1*	Power down

Table 33. SYS_CONTROL1- address 01h reset value 0x11CAh

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	FAIMVBGOVRRL	RW		Overrule the enabling of VBG for faim erase/ write access
			0*	No overrule
			1	Overruled
14	reserved	RW	0*	
13	reserved	RW	0*	
12	MANWDE	RW		Watchdog enable
			0	disabled
			1*	enabled
11	MUTETO	RW		Time out SB mute sequence
			0*	timeout enabled, 400 ms
			1	timeout disabled
10:9	BODTHLVL	RW		BOD threshold
			0*	1.675 V
			1	1.625 V
			2	1.575 V
			3	reserved
8:7	BODFILT	RW		BOD filter
			0	no filter
			1	5 µs
			2	10 µs
			3*	15 µs
6	BODHYS	RW		Enable Hysteresis of BOD
			0	No Hysteresis
			1*	Hysteresis
5	BODE	RW		Enable BOD (only in direct control mode)
			0*	disable
			1	enable
4	MANROBOD	RW		Reaction on BOD
			0*	no restart
			1	restart
3	MANCOLD	RW		Execute cold start
			0	No cold start
			1*	Cold start

Bit	Symbol	Access	Value	Description
2	MANSCONF	RW		Device I^2C settings configured
			0*	HW I^2C not loaded
			1	HW I^2C loaded
1:0	AMPINSEL	RW		Amplifier input selection
			0	TDM Sink0
			1	TDM Sink1
			2*	Coolflux DSP output
			3	Disabled

Table 34. SYS_CONTROL2- address 02h reset value 0x55C8h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:13	AMPOCRT	RW		Amplifier on-off criteria for shutdown
			Others	minimum number of consecutive zeroes as output by noise shaper before amplifier goes into tristate to shut down
12:11	TDMPRES	RW		Control for HW manager
			0	tdm_presense is ignored
			1	tdm_presense is ignored when MCLK is selected as PLL reference clock
			2*	tdm_presense is ignored when TDM is selected as PLL reference clock
			3	tdm_presense is never ignored
10:5	FRACTDEL	RW		Current sense fractional delay
			0	bypassed
			46*	value * 1/64 delay
			Others	value * 1/64 delay
4	INPLEV	RW		TDM output attenuation
			0*	0 dB
			1	−6 dB

Bit	Symbol	Access	Value	Description
3:0	AUDFS	RW		Audio sample rate f_s
			3	16 kHz
			6	32 kHz
			7	44.1 kHz
			8*	48 kHz
			9	96 kHz
			11	16 kHz; high performance
			12	32 kHz; high performance
			Others	Reserved

Table 35. DEVICE_REVISION- address 03h reset value 0x1A94h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	REV	R		Revision info
			Others	revision information

Table 36. CLOCK_CONTROL- address 04h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:11	reserved	RW	0*	
10	reserved	RW	0*	
9	CLKREFSYNCEN	RW		Enable PLL reference clock synchronization for clock divider
			0*	disable
			1	enable
8	FSSYNCEN	RW		Enable FS synchronization for clock divider
			0*	disable
			1	enable
7	ACKCLDDIS	RW		Automatic PLL reference clock selection for cold start
			0*	Enable auto selection
			1	Disable auto selection
6	MANAOOSC	RW		Internal OSC1M off at PWDN
			0*	not off
			1	off

Bit	Symbol	Access	Value	Description
5:3	MCLKSEL	RW		Master Clock Selection
			0*	9.6 MHz
			1	11.2896 MHz
			2	12.288 MHz
			3	13 MHz
			4	19.2 MHz
			5	22.5792 MHz
			6	24.576 MHz
			7	9.6 MHz
2	REFCKSEL	RW		PLL internal reference clock
			0*	external source
			1	internal oscillator
1:0	REFCKEXT	RW		PLL external reference clock
			0*	TDM BCK
			1	TDM FS
			2	MCLK
			3	TDM BCK

Table 37. CLOCK_GATING_CONTROL- address 05h reset value 0x0Eh

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:4	reserved	RW	0*	
3	WDTCLKEN	RW		Enable Coolflux watchdog clock
			0	disable
			1*	enable
2	MTPSSEN	RW		Enable FAIM sub-system
			0	disable
			1*	enable
1	SPKSSEN	RW		Enable speaker sub-system
			0	disable
			1*	
0	reserved	RW	0*	

Table 38. STATUS_FLAGS0- address 10h reset value 0x21Dh

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	BODNOK	R		BOD Flag - VDD NOT OK
			0*	ok (Green)
			1	error
14	ADCCR	R		Control ADC
			0*	not ready
			1	ready (Green)
13	AREFS	R		References enable
			0*	disable
			1	enable (Green)
12	AMPS	R		Amplifier enable
			0*	disable
			1	enable (Green)
11	SWS	R		Amplifier engage
			0*	floating
			1	Switching (Green)
10	WDS	R		Watchdog
			0*	ok (Green)
			1	error
9	ACS	R		Cold Start
			0	Cold start done (Green)
			1*	Cold start required
8	NOCLK	R		Lost clock
			0*	clock detected (Green)
			1	disappeared
7	MTPB	R		MTP busy
			0*	idle (Green)
			1	busy
6	CLKS	R		Clocks stable
			0*	unstable
			1	stable (OK) (Green)
5	OCDS	R		OCP amplifier (sticky register, clear on read)
			0*	Current is OK (Green)
			1	Current is too high

Bit	Symbol	Access	Value	Description
4	UVDS	R		UVP alarm
			0	V_{bat} too low
			1*	V_{bat} OK (Green)
3	reserved	R	0*	
2	OTDS	R		OTP alarm
			0	Too high
			1*	OK (Green)
1	PLLS	R		PLL Lock
			0*	not locked
			1	locked (Green)
0	VDDS	R		POR
			0	POR cleared (Green)
			1*	POR detected

Table 39. STATUS_FLAGS1- address 11h reset value 0x04h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0*	
12	NOAUDCLK	R		Lost audio clock
			0*	TDM audio clock detected (green)
			1	disappeared
11	TDMLUTER	R		TDM lookup table error
			0*	ok (Green)
			1	error
10	TDMERR	R		TDM error
			0*	ok (Green)
			1	error
9	MANALARM	R		Alarm state
			0*	manager is not in alarm state
			1	manager is in alarm state
8	CLKOOR	R		External clock status
			0*	within range (Green)
			1	out of range
7	SPKS	R		Speaker status
			0*	No error (Green)
			1	Error (Not OK)

Bit	Symbol	Access	Value	Description
6	DCH107	R		DCDC level 1.07x
			0*	V_{bst} < 1.07 * V_{bat}
			1	V_{bst} > V_{bat} (Green)
5	DCH114	R		DCDC level 1.14x
			0*	V_{bst} < 1.14 * V_{bat}
			1	V_{bst} > V_{bat} (Green)
4	DCHVBAT	R		DCDC level 1x
			0*	V_{bst} < V_{bat}
			1	V_{bst} > V_{bat} (Green)
3	reserved	R	0*	
2	DCOCPOK	R		DCDC OCP nmos (sticky register, clear on read)
			0	Overcurrent
			1*	OK (Green)
1	DCDCA	R		DCDC active (sticky register, clear on read)
			0*	V_{bst} is V_{bat}
			1	V_{bst} > V_{bat} (Green)
0	DCIL	R		DCDC current limiting
			0*	normal (Green)

Table 40. STATUS_FLAGS2- address 12h reset value 0x18Fh

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:10	reserved	R	0*	
9	VDDPH	R		VDDP greater than VBAT flag
			0*	no (Green)
			1	yes
8	LA	R		Low amplitude detection
			0	low amplitude not detected
			1*	low amplitude detected (Green)
7	LP1	R		Low power MODE1 detection
			0	low power mode 1 not detected
			1*	low power mode 1 detected (Green)
6	MANOPER	R		Device in Operating state
			0*	not in operating
			1	operating state (Green)

Bit	Symbol	Access	Value	Description
5	MANMUTE	R		Audio mute sequence
			0*	not started (Green)
			1	started
4	CLIPS	R		Amplifier clipping
			0*	not clipping (Green)
			1	clipping
3	OCPOBN	R		OCPOK nmos B
			0	Overcurrent
			1*	No Overcurrent (Green)
2	OCPOBP	R		OCPOK pmos B
			0	Overcurrent
			1*	No Overcurrent (Green)
1	OCPOAN	R		OCPOK nmos A
			0	Overcurrent
			1*	No Overcurrent (Green)
0	OCPOAP	R		OCPOK pmos A
			0	Overcurrent

Table 41. STATUS_FLAGS3 - address 13h reset value 0x00h

*Address 13h: Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0*	
12:11	DCMODE	R		DCDC mode status bits
			0*	OFF mode
			1	Follower mode
			2	PWM mode
			3	PFM mode
10:7	reserved	R	0*	

Bit	Symbol	Access	Value	Description
6:3	MANSTATE	R		Device Manager status
			0*	power_down_state
			1	wait_for_source_settings_state
			2	reserved
			3	reserved
			4	enable_pll_state
			5	enable_cgu_state
			6	init_cooflux
			7	enable_amplifier_state
			8	alarm_state
			9	operating_state (Green)
			10	mute_audio_state
			11	disable_cgu_pll_state
			12	reserved
			13	reserved
			14	reserved
			15	reserved
2:0	TDMSTAT	R		TDM Status bits
			0*	TDM/I2S block disabled
			1	TDM/I2S block enabled and synchronized (Green)
			2	Reserved
			3	TDM/I2S synchronization error
			4	Sink buffer overrun
			5	Sink buffer underrun
			6	Source buffer overrun
			7	Source buffer underrun

Table 42. BATTERY_VOLTAGE- address 15h reset value 0x3FFh

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:10	reserved	R	0*	
9:0	BATS	R		Battery voltage (V)
			Others	VALUE * 5.5/1023

Table 43. TEMPERATURE- address 16h reset value 0x100h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0*	
8:0	TEMPS	R		IC Temperature (C)
			Others	VALUE (1 bit = 1 °C)

Table 44. VDDP_VOLTAGE- address 17h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:10	reserved	R	0*	
9:0	VDDPS	R		IC VDDP voltage (1023*VDDP/13V)
			Others	step of 13 V/1023 with 0 offset

Table 45. TDM_CONFIG0- address 20h reset value 0x707h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:13	reserved	RW	0*	
12:11	TDMOOMP	RW		Received audio compression
			0*	no compression
			1	reserved
			2	u-Law
			3	A-law
10	TDMADJ	RW		Data adjustment
			0	LSB justified
			1*	MSB justified
9	TDMDEL	RW		Data delay to FS
			0	no delay
			1*	1 bit delay
8	TDMFSPOL	RW		FS polarity
			0	rising FS edge
			1*	falling FS edge
7	TDMCLINV	RW		Reception data to BCK clock
			0*	rising edge
			1	falling edge
6	TDMCF2E	RW		Source 3 enable
			0*	disable
			1	enable

Bit	Symbol	Access	Value	Description
5	TDMCFE	RW		Source 2 enable
			0*	disable
			1	enable
4	TDMVSE	RW		Source 1 enable
			0*	disable
			1	enable
3	TDMCSE	RW		Source 0 enable
			0*	disable
			1	enable
2	TDMDCE	RW		Control audio tdm channel in sink1
			0	disable
			1*	enable
1	TDMSPKE	RW		Control audio tdm channel in sink0
			0	disable
			1*	enable
0	TDME	RW		Enable interface
			0	disable
			1*	enable

Table 46. TDM_CONFIG1- address 21h reset value 0x8110h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	TDMTXUS0	RW		Format unused slots DATAO
			0	transmit all zeroes
			1	reserved
			2*	tri-state
			3	reserved
13:12	TDMTXDFO	RW		Format unused bits
			0*	zero filling for both MSB and LSB
			1	sign extension for MSB, zero filling for LSB
			2	tri-state
			3	reserved
11:8	TDMSLOTS	RW		N-slots in Frame
			0	1 slot
			1*	2 slots
			2	3 slots
			3	4 slots
			4	5 slots
			5	6 slots
			6	7 slots
			7	8 slots
			8	9 slots
			9	10 slots
			10	11 slots
			11	12 slots
			12	13 slots
			13	14 slots
			14	15 slots
			15	16 slots

Bit	Symbol	Access	Value	Description
7:4	TDMFSLN	RW		FS length (master mode only)
			0	1 BCK period
			1*	1 slot
			2	2 slots
			3	3 slots
			4	4 slots
			5	5 slots
			6	6 slots
			7	7 slots
			8	8 slots
			9	9 slots
			10	10 slots
			11	11 slots
			12	12 slots
			13	13 slots
			14	14 slots
			15	15 slots
3:0	TDMNBCK	RW		TDM NBCK - Bit clock to FS ratio
			0*	32
			1	48
			2	64
			3	96
			4	128
			5	192
			6	256
			7	384
			8	200
			9	100
			10	144
			11	288
			12	512
			13	1
			14	reserved
			15	reserved

Table 47. TDM_CONFIG2- address 22h reset value 0x3C0Fh

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	reserved	RW	0*	
14:10	TDMSSIZE	RW		Sample size per slot
			0	1 bit
			1	2 bits
			2	3 bits
			3	4 bits
			4	5 bits
			5	6 bits
			6	7 bits
			7	8 bits
			8	9 bits
			9	10 bits
			10	11 bits
			11	12 bits
			12	13 bits
			13	14 bits
			14	15 bits
			15*	16 bits
			16	17 bits
			17	18 bits
			18	19 bits
			19	20 bits
			20	21 bits
			21	22 bits
			22	23 bits
			23	24 bits
			24	25 bits
			25	26 bits
			26	27 bits
			27	28 bits
			28	29 bits
			29	30 bits
			30	31 bits
			31	32 bits

Bit	Symbol	Access	Value	Description
9:5	TDMBRMG	RW		N-bits remaining
			0*	0 bits
			1	1 bit
			2	2 bits
			3	3 bits
			4	4 bits
			5	5 bits
			6	6 bits
			7	7 bits
			8	8 bits
			9	9 bits
			10	10 bits
			11	11 bits
			12	12 bits
			13	13 bits
			14	14 bits
			15	15 bits
			16	16 bits
			17	17 bits
			18	18 bits
			19	19 bits
			20	20 bits
			21	21 bits
			22	22 bits
			23	23 bits
			24	24 bits
			25	25 bits
			26	26 bits
			27	27 bits
			28	28 bits
			29	29 bits
			30	30 bits
			31	31 bits

Bit	Symbol	Access	Value	Description
4:0	TDMSLLN	RW		N-bits in slot
			0	reserved
			1	reserved
			2	reserved
			3	4 bits
			4	5 bits
			5	6 bits
			6	7 bits
			7	8 bits
			8	9 bits
			9	10 bits
			10	11 bits
			11	12 bits
			12	13 bits
			13	14 bits
			14	15 bits
			15*	16 bits
			16	17 bits
			17	18 bits
			18	19 bits
			19	20 bits
			20	21 bits
			21	22 bits
			22	23 bits
			23	24 bits
			24	25 bits
			25	26 bits
			26	27 bits
			27	28 bits
			28	29 bits
			29	30 bits
			30	31 bits
			31	32 bits

Table 48. TDM_CONFIG3- address 23h reset value 0x410h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:12	reserved	RW	0*	
11:10	TDMCF2SEL	RW		TDM Source 3 data selection
			0	DSP audio output
			1*	DSP AEC output
			2	TDM sink0 channel for loopback
			3	TDM sink1 channel for loopback
9:8	TDMCFSEL	RW		TDM Source 2 data selection
			0*	DSP audio output
			1	DSP AEC output
			2	TDM sink0 channel for loopback
			3	TDM sink1 channel for loopback
7:4	TDMDCS	RW		TDM slot for sink 1
			0	slot 0
			1*	slot 1
			2	slot 2
			3	slot 3
			4	slot 4
			5	slot 5
			6	slot 6
			7	slot 7
			8	slot 8
			9	slot 9
			10	slot 10
			11	slot 11
			12	slot 12
			13	slot 13
			14	slot 14
			15	slot 15

Bit	Symbol	Access	Value	Description
3:0	TDMSPKS	RW		TDM slot for sink 0
			0*	slot 0
			1	slot 1
			2	slot 2
			3	slot 3
			4	slot 4
			5	slot 5
			6	slot 6
			7	slot 7
			8	slot 8
			9	slot 9
			10	slot 10
			11	slot 11
			12	slot 12
			13	slot 13
			14	slot 14
			15	slot 15

Table 49. TDM_CONFIG4- address 24h reset value 0x5432h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:12	TDMCF2S	RW		Slot Position of source 3 data
			0	slot 0
			1	slot 1
			2	slot 2
			3	slot 3
			4	slot 4
			5*	slot 5
			6	slot 6
			7	slot 7
			8	slot 8
			9	slot 9
			10	slot 10
			11	slot 11
			12	slot 12
			13	slot 13
			14	slot 14
			15	slot 15
11:8	TDMCFS	RW		Slot Position of source 2 data
			0	slot 0
			1	slot 1
			2	slot 2
			3	slot 3
			4*	slot 4
			5	slot 5
			6	slot 6
			7	slot 7
			8	slot 8
			9	slot 9
			10	slot 10
			11	slot 11
			12	slot 12
			13	slot 13
			14	slot 14
			15	slot 15

Bit	Symbol	Access	Value	Description
7:4	TDMVSS	RW		Slot Position of source 1 data
			0	slot 0
			1	slot 1
			2	slot 2
			3*	slot 3
			4	slot 4
			5	slot 5
			6	slot 6
			7	slot 7
			8	slot 8
			9	slot 9
			10	slot 10
			11	slot 11
			12	slot 12
			13	slot 13
			14	slot 14
			15	slot 15
3:0	TDMCSS	RW		Slot Position of source 0 data
			0	slot 0
			1	slot 1
			2*	slot 2
			3	slot 3
			4	slot 4
			5	slot 5
			6	slot 6
			7	slot 7
			8	slot 8
			9	slot 9
			10	slot 10
			11	slot 11
			12	slot 12
			13	slot 13
			14	slot 14
			15	slot 15

Table 50. INTERRUPT_OUT_REG- address 40h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	ISTCLKOOR	R		Status clock out of range
			0*	ok
			1	trigger
14	ISTLP1	R		Status low power mode1 detect
			0*	ok
			1	trigger
13	ISTBODNOK	R		Status brown out detect
			0*	ok
			1	trigger
12	ISTWDS	R		Status watchdog reset
			0*	ok
			1	trigger
11	ISTACS	R		Status cold started
			0*	ok
			1	trigger
10	ISTSPKS	R		Status coolflux speaker error
			0*	ok
			1	trigger
9	ISTCFMAC	R		Status cfma ack
			0*	ok
			1	trigger
8	ISTCFMER	R		Status cfma error
			0*	ok
			1	trigger
7	ISTNOCLK	R		Status lost clock
			0*	ok
			1	trigger
6	ISTTDMER	R		Status TDM error
			0*	ok
			1	trigger
5	ISTMANALARM	R		Status manager alarm state
			0*	ok
			1	trigger

Bit	Symbol	Access	Value	Description
4	ISTUVDS	R		Status UVP alarm
			0*	ok
			1	trigger
3	ISTOCPR	R		Status OCP alarm
			0*	ok
			1	trigger
2	ISTOTDS	R		Status OTP alarm
			0*	ok
			1	trigger
1	ISTBSTOC	R		Status DCDC OCP
			0*	ok
			1	trigger
0	ISTVDDS	R		Status POR
			0*	ok
			1	trigger

Table 51. INTERRUPT_IN_REG- address 44h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	ICLCLKOOR	W		Clear clock out of range
			0*	retain
			1	clear
14	ICLLP1	W		Clear low power mode1 detect
			0*	retain
			1	clear
13	ICLBODNOK	W		Clear brown out detect
			0*	retain
			1	clear
12	ICLWDS	W		Clear watchdog reset
			0*	retain
			1	clear
11	ICLACS	W		Clear cold started
			0*	retain
			1	clear

Bit	Symbol	Access	Value	Description
10	ICLSPKS	W		Clear coolflux speaker error
			0*	retain
			1	clear
9	ICLCFMAC	W		Clear cfma ack
			0*	retain
			1	clear
8	ICLCFMER	W		Clear cfma err
			0*	retain
			1	clear
7	ICLNOCLK	W		Clear lost clk
			0*	retain
			1	clear
6	ICLTDMER	W		Clear TDM error
			0*	retain
			1	clear
5	ICLMANALARM	W		Clear manager alarm state
			0*	retain
			1	clear
4	ICLUVDS	W		Clear UVP alarm
			0*	retain
			1	clear
3	ICLOCPR	W		Clear OCP alarm
			0*	retain
			1	clear
2	ICLOTDS	W		Clear OTP alarm
			0*	retain
			1	clear
1	ICLBSTOC	W		Clear DCDC OCP
			0*	retain
			1	clear
0	ICLVDDS	W		Clear POR
			0*	retain
			1	clear

Table 52. INTERRUPT_ENABLE_REG- address 48h reset value 0x01h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	IECLKOOR	RW		Enable clock out of range
			0*	disable
			1	enable
14	IELP1	RW		Enable low power mode1 detect
			0*	disable
			1	enable
13	IEBODNOK	RW		Enable brown out detect
			0*	disable
			1	enable
12	IEWDS	RW		Enable watchdog reset
			0*	disable
			1	enable
11	IEACS	RW		Enable cold started
			0*	disable
			1	enable
10	IESPKS	RW		Enable coolflux speaker error
			0*	disable
			1	enable
9	IECFMAC	RW		Enable cfma ack
			0*	disable
			1	enable
8	IECFMER	RW		Enable cfma err
			0*	disable
			1	enable
7	IENOCLK	RW		Enable lost clk
			0*	disable
			1	enable
6	IETDMER	RW		Enable TDM error
			0*	disable
			1	enable
5	IEMANALARM	RW		Enable Manager Alarm state
			0*	disable
			1	enable

Bit	Symbol	Access	Value	Description
4	IEUVDS	RW		Enable UVP alarm
			0*	disable
			1	enable
3	IEOCPR	RW		Enable OCP alarm
			0*	disable
			1	enable
2	IEOTDS	RW		Enable OTP alarm
			0*	disable
			1	enable
1	IEBSTOC	RW		Enable DCDC OCP
			0*	disable
			1	enable
0	IEVDDS	RW		Enable POR
			0	disable
			1*	enable

Table 53. INTERRUPT_POLARITY_REG- address 4Ch reset value 0xFFE9h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	IPOCLKOOR	RW		Polarity clock out of range
			0	active low
			1*	active high
14	IPOLP1	RW		Polarity low power mode1 detect
			0	active low
			1*	active high
13	IPOBODNOK	RW		Polarity brown out detect
			0	active low
			1*	active high
12	IPOWDS	RW		Polarity watchdog reset
			0	active low
			1*	active high
11	IPOACS	RW		Polarity cold started
			0	active low
			1*	active high

Bit	Symbol	Access	Value	Description
10	IPOSPKS	RW		Polarity coolflux speaker error
			0	active low
			1*	active high
9	IPOCFMAC	RW		Polarity cfma ack
			0	active low
			1*	active high
8	IPOCFMER	RW		Polarity cfma err
			0	active low
			1*	active high
7	IPONOCLK	RW		Polarity lost clk
			0	active low
			1*	active high
6	IPOTDMER	RW		Polarity TDM error
			0	active low
			1*	active high
5	IPOMANALARM	RW		Polarity manager alarm state
			0	active low
			1*	active high
4	IPOUVDS	RW		Polarity UVP alarm
			0*	active low
			1	active high
3	IPOOCPR	RW		Polarity ocp alarm
			0	active low
			1*	active high
2	IPOOTDS	RW		Polarity OTP alarm
			0*	active low
			1	active high
1	IPOBSTOC	RW		Polarity DCDC OCP
			0*	active low
			1	active high
0	IPOVDDS	RW		Polarity POR
			0	active low
			1*	active high

Table 54. BAT_PROT_CONFIG- address 50h reset value 0x9391h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	BSSBY	RW		Bypass HW clipper
			0	active
			1*	bypassed
14	BSSR	RW		Battery voltage read out
			0*	minimum
			1	average
13	reserved	RW	0*	
12:11	BSSHY	RW		Battery Safeguard hysteresis
			0	No hysteresis
			1	0.05 V
			2*	0.1 V
			3	0.2 V
10:8	BSSRR	RW		Battery safeguard release time
			0	1.6 s
			1	1.6 s
			2	1.6 s
			3*	1.6 s
			4	2 s
			5	2.4 s
			6	2.8 s
			7	3.2 s
7:6	BSSRL	RW		Battery safeguard maximum reduction
			0	3.94 V
			1	4.84 V
			2*	5.85 V
			3	not permitted

Bit	Symbol	Access	Value	Description
5:2	BSST	RW		Battery safeguard threshold voltage level
			0	2.85 V (normal); 3.05 V (steep)
			1	2.95 V (normal); 3.15 V (steep)
			2	3.05 V (normal); 3.25 V (steep)
			3	3.15 V (normal); 3.35 V (steep)
			4*	3.25 V (normal); 3.45 V (steep)
			5	3.35 V (normal); 3.55 V (steep)
			6	3.45 V (normal); 3.65 V (steep)
			7	3.55 V (normal); 3.75 V (steep)
			8	3.65 V (normal); 3.85 V (steep)
			9	3.75 V (normal); 3.95 V (steep)
			10	3.85 V (normal); 4.05 V (steep)
			11	3.95 V (normal); 4.15 V (steep)
			12	4.05 V (normal); 4.25 V (steep)
			13	4.15 V (normal); 4.35 V (steep)
			14	4.25 V (normal); 4.45 V (steep)
			15	4.35 V (normal); 4.55 V (steep)
1:0	BSSCR	RW		Battery safeguard attack time
			0	0.56 dB/sample
			1*	1.12 dB/sample
			2	2.32 dB/sample
			3	inifinite dB/sample

Table 55. CF_AUDIO_CONTROL- address 51h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	VOL	RW		CF firmware volume control
			0*	0 dB
			1	−0.5 dB
			Others	value * −0.5 dB
7:4	reserved	RW	0*	
3	CFSM	RW		Coolflux firmware soft mute control
			0*	no mute
			1	muted
2:0	reserved	RW	0*	

Table 56. AMPLIFIER_CONFIG- address 52h reset value 0xB617h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	AMPGAIN	RW		Amplifier gain
			0	mute
			182*	value/128
			Others	value / 128
7:5	reserved	RW	0*	
4	reserved	RW	1*	
3	reserved	RW	0*	
2:0	CLIPCTRL	RW		Clip control setting
			0	skip 0 pulses
			1	skip 1 pulse
			2	skip 2 pulses
			3	skip 3 pulses
			4	skip 4 pulses
			5	skip 5 pulses
			6	evaluation mode 1
			7*	evaluation mode 2

Table 57. GAIN_ATT_CONTROL- address 57h reset value 0x366h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:10	reserved	RW	0*	
9:8	DCINSEL	RW		VAMP_OUT2 input selection
			0	TDM Sink0
			1	TDM Sink1
			2	Coolflux DSP output
			3*	disabled

Bit	Symbol	Access	Value	Description
7:4	TDMSPKG	RW		Total gain depending on INPLEV setting (channel 0)
			0	21.00 dB
			1	19.99 dB
			2	18.86 dB
			3	17.94 dB
			4	16.92 dB
			5	15.76 dB
			6*	14.98 dB
			7	13.94 dB
			8	12.84 dB
			9	11.92 dB
			10	10.90 dB
			11	9.74 dB
			12	8.96 dB
			13	7.95 dB
			14	6.81 dB
			15	5.90 dB
3:0	TDMDCG	RW		Second channel gain in case of stereo using a single coil. (Total gain depending on INPLEV). (In case of mono OR stereo using 2 separate DCDC channel 1 should be disabled using TDMDCE)
			0	21.00 dB
			1	19.99 dB
			2	18.86 dB
			3	17.94 dB
			4	16.92 dB
			5	15.76 dB
			6*	14.98 dB
			7	13.94 dB
			8	12.84 dB
			9	11.92 dB
			10	10.90 dB
			11	9.74 dB
			12	8.96 dB
			13	7.95 dB
			14	6.81 dB
			15	5.90 dB

Table 58. LOW_NOISE_GAIN_CONTROL0- address 58h reset value 0x81h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:10	reserved	RW	0*	
9:8	LNMODE	RW		Low noise gain mode control
			0*	auto
			1	fixed to high gain
			2	fixed to high gain
			3	fixed to low gain
7:6	reserved	RW	2*	
5:0	reserved	RW	1*	

Table 59. MODE1_DETECTOR_CONTROL0- address 5Ah reset value 0x40h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	RW	0*	
13:12	LPM1MODE	RW		Low power mode control
			0*	auto
			1	low power mode disabled
			2	low power mode disabled
			3	low power mode forced active
11:6	reserved	RW	1*	
5:0	reserved	RW	0*	

Table 60. TDM_SOURCE_CONTROL- address 5Dh reset value 0x790h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:11	reserved	RW	0*	
10:9	TDMSRCBCLIP	RW		Clip information (analog /digital) for source1
			0	none
			1	digital only
			2	analog only
			3*	analog and digital (ored in mode Mono_1slot_32bits and Mono_2slots_16bits)

Bit	Symbol	Access	Value	Description
8:7	TDMSRCACLIP	RW		Clip information (analog /digital) for source0
			0	none
			1	digital only
			2	analog only
			3*	analog and digital (ored in mode Mono_1slot_32bits and Mono_2slots_16bits)
6:5	TDMSRCBS	RW		Sensed value B
			0*	V_{bat}
			1	temperature
			2	min_vbat
			3	V_{ddp}
4:3	TDMSRCAS	RW		Sensed value A
			0	V_{bat}
			1	temperature
			2*	min_vbat
			3	V_{ddp}
2:0	TDMSRCMAP	RW		TDM source mapping
			0*	32 bits mono/stereo
			1	24 bits mono/stereo
			2	16 bits mono/stereo
			3	32 bits mono/stereo (compress mode)
			4	CS (source0) / VS (source1) only (16 msb bits)
			others	reserved

Table 61. CURSENSE_COMP_CONTROL- address 61h reset value 0x73h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	RW	0*	
7:5	LVLCLPPWM	RW		Set the amount of pwm pulse that may be skipped before clip-flag is triggered
			0	256
			1	512
			2	768
			3*	1024
			4	1280
			5	1536
			6	1792
			7	2047
4	ENCURCOMP	RW		Enable current sense compensation
			0	disable
			1*	enable
3	SIGCURCOMP	RW		Polarity of compensation for current sense
			0*	low
			1	high
2:0	DELCURCOMP	RW		Delay to allign compensation signal with current sense signal
			others	TBC default 0x4

Table 62. DCDC_CONTROL0- address 70h reset value 0xFFDEh

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:12	DCMCC	RW		maximum coil current
			0	0.00 A
			1	0.26 A
			2	0.52 A
			3	0.78 A
			4	1.04 A
			5	1.30 A
			6	1.56 A
			7	1.82 A
			8	2.08 A
			9	2.34 A
			10	2.60 A
			11	2.88 A
			12	3.14 A
			13	3.40 A
			14	3.66 A
			15*	3.92 A
11:6	DCVOS	RW		second boost voltage level
			30	6.0 V
			34	6.5 V
			38	7.0 V
			42	7.5 V
			47	8.0 V
			51	8.5 V
			55	9.0 V
			59	9.5 V
			63*	10.0 V
			Others	(I^2C setting + 10) * 0.12 + 1.25

Bit	Symbol	Access	Value	Description
5:0	DCVOF	RW		first boost voltage level
			13	4.0 V
			17	4.5 V
			22	5.0 V
			26	5.5 V
			30*	6.0 V
			34	6.5 V
			38	7.0 V
			42	7.5 V
			others	(I^2C setting + 10) * 0.12 + 1.25

Table 63. DCDC_CONTROL1- address 71h reset value 0x18Dh

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	reserved	RW	0*	
14:9	OVSCTLVL	RW	110111*	Threshold level to activate active overshoot control
			others	(val + 10) * 0.12 + 1.25 V
8	reserved	RW	0*	
7	DCENVSEL	RW		selection of data for adaptive boost algorithm, effective only when boost_intelligent is set to 1
			0	1Fs data
			1*	8Fs data
6	DCTRACK	RW		boost algorithm selection, effective only when boost_intelligent is set to 1
			0*	two-level adaptive boost algorithm
			1	tracking boost level algorithm
5	DCPWM	RW		DCDC PWM only mode
			0*	PWM_ONLY mode turned off
			1	PWM_ONLY mode turned on
4	DCDIS	RW		DCDC on/off
			0*	on
			1	off
3	DCSR	RW		soft ramp up/down
			0	immediate
			1*	gradually

Bit	Symbol	Access	Value	Description
2	DCIE	RW		adaptive boost mode
			0	off
			1*	on
1:0	DCCV	RW		slope compensation current, represents LxF (inductance x frequency) value
			0	0.7
			1*	1
			2	1.5
			3	2

Table 64. DCDC_CONTROL2- address 72h reset value 0x44E8h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	DCTRIPHYSTE	RW		Enable hysteresis on booster trip levels
			0*	disabled
			1	enabled
14:10	DCTRIPT	RW		Track adaptive boost trip levels, effective only when boost_intelligent is set to 1
			Others	equals adaptive boost trip-level from [5.6 to 11.8] dB
9:5	DCTRIP2	RW		2nd adaptive boost trip levels, effective only when DCIE is set to 1
			0	5.6 dB
			7*	7.0 dB
			Others	(N * 0.2 dB) + 5.6 dB
4:0	DCTRIP	RW		1st adaptive boost trip levels, effective only when DCIE is set to 1
			0	5.6 dB
			8*	7.2 dB

Table 65. DCDC_CONTROL3- address 73h reset value 0x3806h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	reserved	RW	0*	
14:8	reserved	RW	56*	
7:6	reserved	RW	0*	
5	reserved	RW	0*	

Bit	Symbol	Access	Value	Description
4:0	DCHOLD	RW		Hold time for DCDC booster, effective only when boost_intelligent is set to 1
			others	(N * 4) / (k * f_s), where N = register value and k = 2 for f_s = 16 kHz, k = 1 for f_s = 32 kHz/44.1 kHz/48 kHz, k = 0.5 for f_s = 96 kHz

Table 66. CF_CONTROLS- address 90h reset value 0x01h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	REQRSV	RW		Firmware event request reserved
			0*	idle
			1	requested
14	REQCAL	RW		Firmware event request calibration completed
			0*	idle
			1	requested
13	REQDMG	RW		Firmware event request speaker damage detected
			0*	idle
			1	requested
12	REQVOL	RW		Firmware event request volume ready
			0*	idle
			1	requested
11	REQMUTED	RW		Firmware event request mute sequence ready
			0*	idle
			1	requested
10	REQMIPS	RW		Firmware event request short on mips
			0*	idle
			1	requested
9	REQRST	RW		Firmware event request reset restart
			0*	idle
			1	requested
8	REQCMD	RW		Firmware event request rpc command
			0*	idle
			1	requested
7:6	reserved	RW	0*	

Bit	Symbol	Access	Value	Description
5	CFCGATE	RW		Coolflux clock gating disabling control
			0*	enable
			1	disable
4	CFINT	RW		Coolflux Interrupt - auto clear
			0*	no interrupt
			1	interrupt
3	AIF	RW		Auto increment
			0*	on
			1	off
2:1	DMEM	RW		Target memory for CFMA using I2C interface
			0*	PMEM
			1	XMEM
			2	YMEM
			3	IOMEM
0	RST	RW		reset for Coolflux DSP
			0	no reset
			1*	reset

Table 67. CF_MEM- address 92h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	MADD	RW		CF memory address
			others	memory address

Table 68. CF_MAD- address 91h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	MEMA	RW		activate memory access
			others	activate memory access

Table 69. CF_STATUS- address 93h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15	ACKRSV	R		firmware event acknowledge reserved
			0*	idle
			1	acknowledged

Bit	Symbol	Access	Value	Description
14	ACKCAL	R		firmware event acknowledge calibration completed
			0*	idle
			1	acknowledged
13	ACKDMG	R		firmware event acknowledge speaker damage detected
			0*	idle
			1	acknowledged
12	ACKVOL	R		firmware event acknowledge volume ready
			0*	idle
			1	acknowledged
11	ACKMUTED	R		firmware event acknowledge mute sequence ready
			0*	idle
			1	acknowledged
10	ACKMIPS	R		firmware event acknowledge short on mips
			0*	idle
			1	acknowledged
9	ACKRST	R		firmware event acknowledge reset restart
			0*	idle
			1	acknowledged
8	ACKCMD	R		firmware event acknowledge rpc command
			0*	idle
			1	acknowledged
7:0	ERR	R		CF error flags
			others	flags

Table 70. MTPKEY2_REG- address A1h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	RW	0*	
7:0	MTPK	RW		KEY2 to access KEY2 protected registers, customer key
			others	MTP KEY

Table 71. MTP_STATUS- address A2h reset value 0x03h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0*	
1	KEY2LOCKED	R		Indicates KEY2 is locked
			0	not locked
			1*	locked
0	KEY1LOCKED	R		Indicates KEY1 is locked
			0	not locked
			1*	locked

Table 72. MTP_DATA_OUT_MSB- address A5h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	MTPRDMSB	R		MSB word of MTP manual read data

Table 73. MTP_DATA_OUT_LSB- address A6h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	MTPRDLSB	R		LSB word of MTP manual read data
			others	LSB word of MTP manual read data

Table 74. TEMP_SENSOR_CONFIG- address B1h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:10	reserved	RW	0*	
9	TROS	RW		select temp speaker calibration
			0*	internal
			1	external
8:0	EXTTS	RW		external temperature (°C)
			0*	external temperature
			others	external temperature in °C

Table 75. SOFTWARE_PROFILE- address E0h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	SWPROFIL	RW		software profile data
			others	software profile data

Table 76. SOFTWARE_VSTEP- address E1h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	SWVSTEP	RW		software vstep information
			others	software vstep data

Table 77. KEY2_PROTECTED_MTP0- address F0h reset value 0x00h

*Register legend: * reset value*

Bit	Symbol	Access	Value	Description
15:7	CUSTINFO	RW		reserved space for allowing customer to store speaker information
			others	customer info
6:4	reserved	RW	0*	
3	reserved	RW	0*	
2	reserved	RW	0*	
1	MTPEX	RW		calibration Ron executed
			0*	not executed
			1	executed
0	MTPOTC	RW		calibration schedule
			0*	after each POR
			1	Once

11 Limiting values

Table 78. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT	−0.3	-	+6	V
V_{BST}	booster output voltage	on pin VBST	−0.3	-	+12	V
V_{INB}	booster input voltage	on pin INB	−0.3	-	+12[1]	V
V_{DDP}	power supply voltage	on pin VDDP	−0.3	-	+12	V
V_{OUTx}	voltage on speaker connections	on pin OUTN, OUTP	−0.3	-	+12	V
V_{DDD}	digital supply voltage	on pin VDDD	−0.3	-	+2.5	V
V_{DDE}	digital supply voltage	on pin VDDE	−0.3	-	+4.6	V
V_{LTESTx}	low-voltage test pins	on pin TEST1/TEST2	−0.3	-	+6	V
V_{HTESTx}	high-voltage test pins	on pin VSP, VSN	−0.3	-	+12	V
T_j	junction temperature		-	-	+125	°C
T_{stg}	storage temperature		−55	-	+150	°C
T_{amb}	ambient temperature		−40	-	+85	°C
V_{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)	−2	-	+2	kV
		according to Charge Device Model (CDM)	-500	-	+500	V

[1] Using NXP demo board, with a 1 mm wire/PCB track length on INB pin, AC pulse up to 15 V can be observed, without damaging the device as these spikes do not end up inside the actual device.

12 Thermal characteristics

Table 79. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board	37		K/W

13 Characteristics

13.1 DC Characteristics

Table 80. DC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT; V_{BAT} must not be lower than V_{DDD}		2.7	-	5.5	V
I_{BAT}	battery supply current	active state; on pin VBAT; operating mode with load R_L = 8 Ω; DC-to-DC in adaptive boost mode; P_o = 380 mW (average music power); V_{BAT} = 4.0 V; V_{DDP} = 10 V		-	125	-	mA
		active state; on pin VBAT; operating mode with load R_L = 8 Ω; external VDDP = 10 V; f_i = 1 kHz; P_{out} = 4 W		-	1.73	-	mA
		idle state; on pin VBAT; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; low power mode enabled		-	2.7	-	mA
		idle state; on pin VBAT; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; low power mode disabled		-	5.7	-	mA
		idle state; on pin VBAT; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; V_{BAT} = 4.0 V; external V_{DDP} = 10 V		-	1.5	-	mA
		power-down state; on pin VBAT; DC-to-DC in power-down mode or external V_{DDP} = 10 V; T_j = 25 °C; no clock.		-	1	-	µA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{VDDP}	power supply current	active state; on pin VDDP; operating mode with load R_L = 8 Ω; external V_{DDP} = 10 V; f_i = 1 kHz; P_{out} = 4 W		-	507	-	mA
		idle state; on pin VDDP; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; V_{BAT} = 4.0 V; external V_{DDP} = 10 V		-	10	-	mA
		power-down state; on pin VDDP; external V_{DDP} = 10 V; T_j = 25 °C; no clock.		-	1.0	-	µA
V_{DDP}	power supply voltage	on pin VDDP		2.7	-	10.2	V
V_{DDE}	digital supply voltage	on pin VDDE		1.65	1.8	3.6	V
V_{DDD}	digital supply voltage	on pin VDDD		1.65	1.8	1.95	V
I_{DDD}	digital supply current	active state (CoolFlux active); on pin VDDD; operating mode with load R_L = 8 Ω; DC-to-DC in daptive boost mode; P_o = 380 mW (average music power); V_{BAT} = 4.0 V; V_{DDP} = 10 V		-	20	-	mA
		idle state; on pin VDDD; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; low power mode enabled		-	3.9	-	mA
		idle state; on pin VDDD; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; low power mode disabled		-	5.2	-	mA
		power-down state; on pin VDDD; DC-to-DC in power-down mode; T_j = 25 °C; no clock; input data not toggling		-	10	-	µA
I_{DDE}	digital power supply	power-down state; on pin VDDE; DC-to-DC in power-down mode; T_j = 25 °C; no clock; input data not toggling		-	1.0	-	µA
Pins FS, BCK, DATAI, ADS1, ADS2, SCL, SDA, RST, TRST, MCLK (input)							
V_{IH}	HIGH-level input voltage			$0.7V_{DDE}$	-	V_{DDE}	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDE}$	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{in}	input capacitance		[2]	-	-	3	pF
I_I	input current	V_{DDD} = 1.8 V; V_{DDE} = 1.8 V or 3.3 V; V_{DDE} on input pin		-	-	0.1	µA
		V_{DDD} = 1.8 V; V_{DDE} = 1.8 V, V_{DDE} on input pin RST; 90 kΩ pull-down resistor		-	90	120	µA
		V_{DDD} = 1.8 V; V_{DDE} = 1.8 V; V_{DDE} on input pin TRST; 20 kΩ pull-down resistor		-	20	30	µA
		V_{DDD} = 1.8 V; V_{DDE} = 3.3 V, V_{DDE} on input pin RST; 90 kΩ pull-down resistor		-	165	220	µA
		V_{DDD} = 1.8 V; V_{DDE} = 3.3 V; V_{DDE} on input pin TRST; 20 kΩ pull-down resistor		-	37	50	µA
Pins DATAO, INT push-pull output stages (output)							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		V_{DDE} − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	500	mV
Pins SDA, open-drain outputs, external 10 kΩ resistor to V_{DDD}							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		V_{DDE} − 0.5	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	500	mV
Pins OUTP, OUTN							
R_{DSon}	total drain-source on-state resistance	(PMOS + NMOS transistors)		-	430	520	mΩ
Protection							
$T_{act(th\_prot)}$	thermal protection activation temperature			130	-	-	°C
$V_{uvp(VBAT)}$	undervoltage protection on pin VBAT			2.3	-	2.7	V
$I_{O(ocp)}$	overcurrent protection output current			2.5	-	-	A
DC-to-DC converter							
V_{BST}	voltage on pin V_{BST}	DCVOS = 111; fixed boost mode and switching amplifier		9.8	10	10.2	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

13.2 AC characteristics

Table 81. AC characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier output power							
$P_{o(AVG)}$	average output power	hands-free speaker, THD+N = 1 %					
		R_L = 8 Ω; L_L = 44 µH; V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		5.3	5.6	-	W
		R_L = 6 Ω; L_L = 32 µH; V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		5.8	6.1	-	W
		R_L = 4 Ω; L_L = 30 µH; V_{BST} = 9 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		6.0	6.2	-	W
		R_L = 8 Ω; L_L = 44 µH; external V_{DDP} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		-	5.6	-	W
		R_L = 6 Ω; L_L = 32 µH; external V_{DDP} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		-	7.5	-	W
		R_L = 4 Ω; L_L = 30 µH; external V_{DDP} = 9 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		-	9.0	-	W
		receiver speaker; THD+N = 1 %; V_{BST} = 10 V (internal DCDC only)					
		R_L = 32 Ω; voice mode; V_{BAT} = 4.0 V		0.15	0.2	-	W
		R_L = 32 Ω; audio mode; V_{BAT} = 4.0 V		1.10	1.5	-	W
Amplifier output pins (OUTP and OUTN)							
$\|V_O(offset)\|$	output offset voltage after trimming	absolute value; after trimming; V_{DDP} = 3.4 V to 10 V; V_{BAT} = 3.4 V to 5 V		-	-	1.0	mV
Amplifier performances							
η_{po}	output power efficiency	on pin V_{BAT}; operating mode with load R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V, P_o = 380mW (average music playback output power)	[2]	-	81	-	%
		on pin V_{BAT}; Input: 100 Hz sinewave; R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; P_o = 600 mW	[2]	-	91	-	%
		on pin V_{BAT}; Input: 100 Hz sinewave; R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; P_o = 4 W	[2]	-	82	-	%
		total input power from all supplies; f_i = 100 Hz sinewave; R_L = 8 Ω; V_{BAT} = 4.0 V, external V_{DDP} = 10 V; P_o = 4.0 W		-	88	-	%
THD+N	total harmonic distortion-plus-noise	P_o = 2.0 W; R_L = 4 Ω or 8 Ω	[1]	-	0.04	0.09	%
		P_o = 0.1 W; R_L = 32 Ω	[1]	-	0.04	0.09	%
		P_o = 2.0 W; R_L =4 Ω or 8 Ω; External V_{DSDP} = 10 V		-	0.04	-	%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{n(o)}$	output noise voltage	a-weighted; no input signal; low noise mode; f_s = 48 kHz	[2]	-	14	18	µV
		a-weighted; no input signal; low noise mode; f_s = 44 kHz.	[2]	-	15	18	µV
		a-weighted; no input signal; low noise mode; f_s = 16 kHz, high performance or f_s = 32kHz, high performance	[2]	-	15	18	
		external mode; a-weighted; no input signal; (noise shaper noise not included); V_{DDP} = 6 V		-	28	-	µV
		external mode; a-weighted; no input signal; (noise shaper noise not included); V_{DDP} = 10 V		-	36	-	µV
DR	dynamic range	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; no signal applied	[2]	110	114	-	dB
		a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; no signal applied; external V_{DDP} = 10 V		-	105	-	dB
S/N	signal-to-noise ratio	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; with signal applied	[2]	100	-	-	dB
		a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; with signal applied; external V_{DDP} = 10 V		-	95	-	dB
PSRR	power supply rejection ratio	from V_{BAT}					
		booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 217 Hz square wave; V_{ripple} = 50 mV_{pp}; V_{BAT} = 4.0 V		70	80	-	dB
		booster in follower; f_{ripple} = 20 Hz to 1 kHz sinewave; V_{ripple} = 200 mV_{RMS}; V_{BAT} = 3.4 V to 5.0 V		70	80	-	dB
		booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 1 kHz to 20 kHz sinewave; V_{ripple} = 200 mV_{RMS}; V_{BAT} = 3.4 V to 5.0 V		55	64	-	dB
		from VDDP					
		f_{ripple} = 20 Hz to 1 kHz sine wave; V_{ripple} = 0.2 V (RMS); V_{BAT} = 3.4 V to 5 V; external V_{DDP} at 10 V		-	80	-	dB

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔG	gain variation over frequency	BW = 20 Hz to 15 kHz; V_{BAT} = 3.4 V to 5 V; P_o = 2.0 W; R_L = 8 Ω		-0.1	-	0.7	dB
V_{POP}	pop noise	At mode transition and gain change, with C_L < 200 pF[3]		-	-	2	mV
		At mode transition and gain change, with C_L < 200 pF[3]; external V_{DDP} = 10 V		-	-	5	mV
R_L	load Impedance			3.2	8	38.4	Ω
C_L	load capacitance	[3]		-	200	1000	pF
L_L	load inductance	R_L ≤ 32 Ω		30	-	-	µH
f_{sw}	switching frequency	directly coupled to the TDM input frequency		256	-	384	kHz
$G_{(TDM-VO)}$	TDM to V_O gain	INPLEV = 0 dB		6	-	21	dBV
		INPLEV = −6 dB		0	-	15	dBV
Amplifier power-up, power-down and propagation delays							
$t_{d(on)PLL}$	PLL turn-on delay time	PLL locked on BCK; f_s = 48 kHz		-	1.3	-	ms
		PLL locked on FS; f_s = 48 kHz		-	4.5	-	ms
$t_{d(on)amp}$	amplifier turn-on delay time	f_s = 48 kHz[4]		-	55	-	µs
$t_{d(pd)}$	turn-off delay time			-	115	-	µs
$t_{d(alarm)}$	alarm delay time			-	300	-	ms
t_{PD}	propagation delay	f_s = 96 kHz		-	330	600	µs
		f_s = 44.1 kHz/48 kHz		-	610	700	µs
		f_s = 32 kHz		-	710	750	µs
		f_s = 16 kHz		-	800	850	µs
Booster inductance							
L	inductance			0.33	1.0	2.2	µH
f_b	booster switching frequency	fixed boost; V_{DDP} = 10 V; I_{load} = 1 A; f_s = 48 kHz		-	2.05	-	MHz
Sensing performance							
$\Delta V_{sense}/I_{sense}$	V_{sense}/I_{sense} ratio mismatch	pilot tone −40 dBFS	[5]	-	2	-	%
THD+N	total harmonic distortion-plus-noise on current sensing	f_i = 20 Hz to 20 kHz; V_i = −12 dBFs		-	-	0.75	%
S/N	signal-to-noise ratio on current sensing	I_O = 1 A (peak); a-weighted		62	65	-	dB
BrownOut Detection (BOD)							
$V_{th(BOD)}$	BOD threshold voltage	BODTHLVL = 10[6]		1.55	1.575	1.6	V
$V_{hys(BOD)}$	BOD hysteresis	BODHYS = 1		-	20	-	mV
$t_{t(BOD)}$	BOD delay time	BODFILT = 10		-	10	-	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clocks							
$t_{jit(p-p)}$	input clock jitter	MCLK (24.576 MHz)[7]		-	0.5	1.0	ns
		BCK (3.072 MHz)[7]		-	1.0	2.0	ns
		FS[8][7]		-	-	20	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
[3] When C_L exceeds 200 pF, Low Power Mode must be disabled.
[4] At power up, audio is output on OUTP/OUTN after $t_{d(on)amp}$ + $t_{d(on)PLL}$.
[5] Intended for Speaker protection. In combination with NXP Speaker protection a speaker temperature accuracy of ±10 °C can be realized.
[6] Recommended setting.
[7] Valid for V_{DDE} = 1.8 V and 3.3 V.
[8] The system is less sensitive to jitter when the PLL is locked on FS.

13.3 TDM timing characteristics

Table 82. TDM bus interface characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	pin FS; audio mode[2]		16	-	48	kHz
		on pin FS; 96 kHz mode		-	96	-	kHz
f_{clk}	clock frequency	on pin BCK; audio mode	[2]	$32f_s$	-	$384f_s$	kHz
		on pin BCK; 96 kHz mode		-	-	$96f_s$	MHz
t_{su}	set-up time	FS edge to BCK HIGH	[3]	10	-	-	ns
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to FS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
[2] The TDM bit clock input (BCK) is used as a clock input for the amplifier and the DC-to-DC converter. Note that both the BCK and FS signals need to be present for the clock to operate correctly.
[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

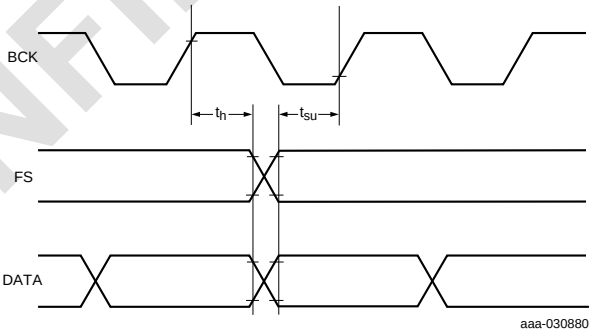


Figure 22. TDM timing

13.4 I²C timing characteristics

Table 83. I2C-bus interface characteristics

All parameters are guaranteed for V_{BAT} = 3.6 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 0 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
[3] After this period, the first clock pulse is generated.
[4] To be suppressed by the input filter.

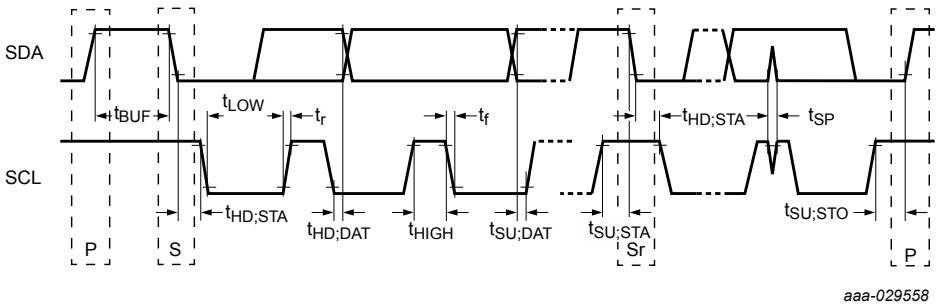


Figure 23. I2C timing

14 Application information

14.1 External components

The DC-to-DC converter needs a battery supply voltage capacitor (C_{VBAT}), an output capacitor (C_{VDDP}), and an inductor (L_{BST}) to work properly. The nominal values of these components are 22 µF, 33 µF, and 1 µH, respectively. If a larger coil is used, the capacitance must also be increased. A 1 µF decoupling capacitor (C_{VDDD}) must be connected close to the VDDD pin. The VDDE pin must be connected externally to the VDDD pin. One 4.7 kΩ resistor (RVS) must be connected between each voltage sensing input and its corresponding amplifier output (VSP/OUTP and VSN/OUTN).

14.1.1 DC-to-DC converter output capacitor

A ceramic capacitor is required at the output of the DC-to-DC converter (C_{VDDP}).

Capacitors constructed using X5R (−55 °C to +85 °C) or X7R (−55 °C to +125 °C) dielectric materials are preferred because they are compact, feature low ESR, and are sufficiently stable over a wide temperature range. The capacitance value decreases over the DC biasing voltage range (50 % to 85 % decrease). Consequently, the selected capacitor must have a nominal value three to four times higher than the required minimum effective capacitance.

Note: *The DC-to-DC converter capacitor connected to pin VBST (C_{VDDP}) is critical for stability. The recommended effective value (the capacitance value at the maximum boost voltage) of C_{VDDP} depends on the coil inductance, and is given in Table 84. The position of the capacitor and the layout of the board are also critical. It is recommended to connect C_{VDDP} as close as possible to the BST and GNDB pins without vias in the PCB tracks.*

In many applications, it is desirable to limit the height of components as much as possible. This can be achieved for C_{VDDP} by placing two smaller capacitors in parallel. The rated voltage should be 10 V or higher.

Table 84. DC-to-DC minimum output capacitor

Effective coil value (at maximum current)	Minimum effective capacitance (at the boost voltage)
0.47 µH	2 µF
1 µH[1]	4 µF
1.5 µH	12 µF
2.2 µH	20 µF

[1] Recommended value; larger values are not preferred because of the cost of and space needed for the coil (L_{BST}) and the capacitor (C_{VDDP}).

The values in the Table 85 and Table 86 are guaranteed for capacitors rated X5R or higher.

Table 85. DC-to-DC recommended output capacitor

Specification	Conditions	Min	Typ	Max	Unit
nominal capacitance; 20 % tolerance	6 Ω or 8 Ω speaker; 1 µH inductor (L_{BST})	-	33	-	µF
minimum effective capacitance	6 Ω or 8 Ω speaker; 1 µH inductor (L_{BST})	4	-	-	µF
rated voltage		10	-	-	V

14.1.2 Battery capacitor

C_{VBAT} must be at least half the value of C_{VDDP}.

Table 86. Battery Recommended capacitor

Specification	Min	Typ	Max	Unit
nominal capacitance; 20 % tolerance	-	22	-	µF
rated voltage	10	-	-	V

14.1.3 DC-to-DC converter inductor

An inductor is required at the output of the DC-to-DC converter (L_{BST}). For stability, the inductance of the coil should remain above 0.33 µH and below 2.2 µH under all conditions. The most commonly available values are 1 µH and 1.5 µH. A nominal value 1 µH provides the optimum balance between current capability, component size and efficiency.

The choice of inductor is configured using DCCV bit. It is strongly influenced by the impedance of the speaker used in the application. The speaker impedance determines the output current of the DC-to-DC converter. The coil current contains a ripple around the average current resulting in a peak inductor current, $I_{L(peak)}$. The value of the peak inductor current is determined by the minimum required battery voltage, the boost voltage and the inductor value.

Recommend specifications for the DC-to-DC convertor inductor are given in Table 87.

Table 87. DC-to_DC Recommended inductor

Specification	Min	Typ	Max	Unit
nominal inductance; 20 % tolerance	0.47[1]	-	2.2	µH
DC resistance	-	-	100	mΩ
saturation current	-	4.2	-	A

[1] 0.33 µH (min) at $I_{L(peak)}$.

14.2 PCB layout considerations

Great care should be taken when designing the PCB layout for a class-D amplifier and booster circuit since the layout can affect the audio performance, the booster performance, the Electromagnetic Compatibility (EMC) performance and/or the thermal performance.

14.2.1 DC-to-DC converter stability

To avoid stability problems, the DC-to-DC converter output capacitor must to be connected as close as possible to GNDB/GNDP via thick tracks as well as to V_{BST}/V_{DDP} in the top layer.

14.2.2 EMC considerations

EMC standards define to what degree a (sub)system is susceptible to externally imposed electromagnetic influences and to what degree a (sub)system is responsible for emitting electromagnetic signals in standby and in normal operating modes.

EMC immunity and emission values are normally measured over a frequency range from 180 kHz up to 3 GHz.

The coupling capacitors on pins V_{DDD}, V_{DDP}, and V_{BAT} and the booster inductor L_{BST} should be placed close to the TFA9894, referenced to a solid ground plane. The design should include a solid ground plane below the IC.

Long speaker cables (or traces) should be avoided when designing a filterless class-D amplifier. Long speaker cables have a negative effect on electromagnetic emissions. Speaker traces/cables of less than 10 cm are recommended.

14.2.3 Power supply considerations

In configurations where VDDE is supplied at 3.3 V and VDDD is supplied at 1.8 V, ensure at platform level that the ramping up of the V_{DDE} is achieved prior to the V_{DDD} and the ramping down of the V_{DDE} is achieved after the V_{DDD}.

14.3 Application diagrams

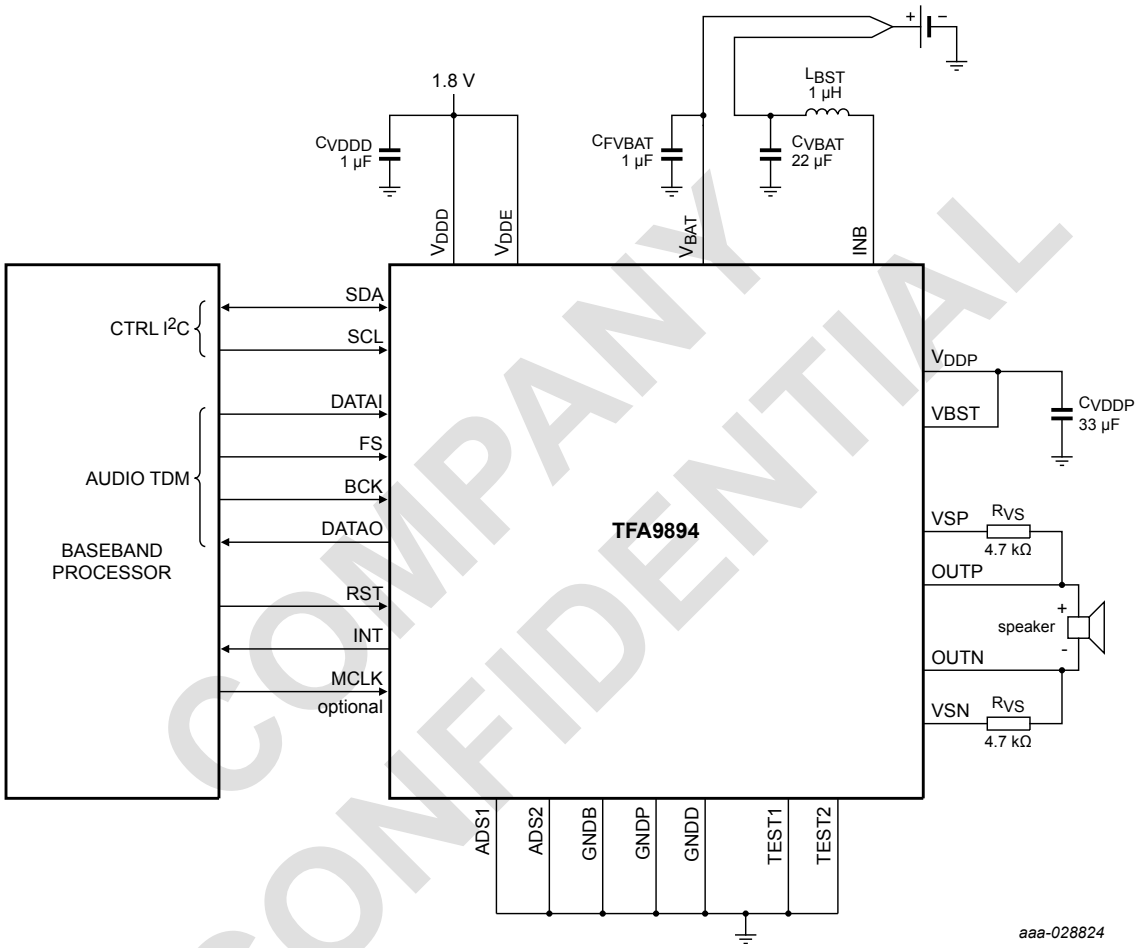


Figure 24. Typical mono application

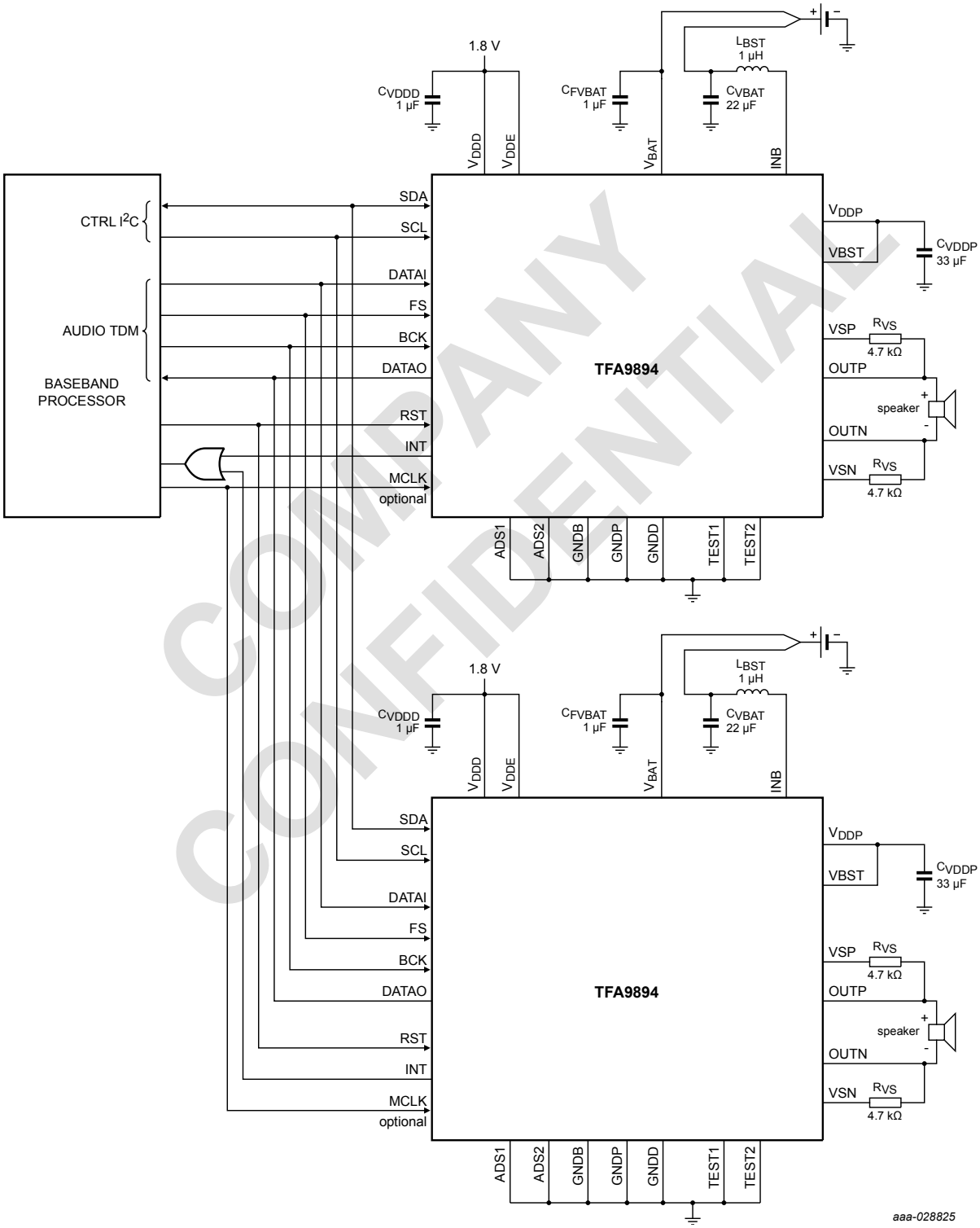
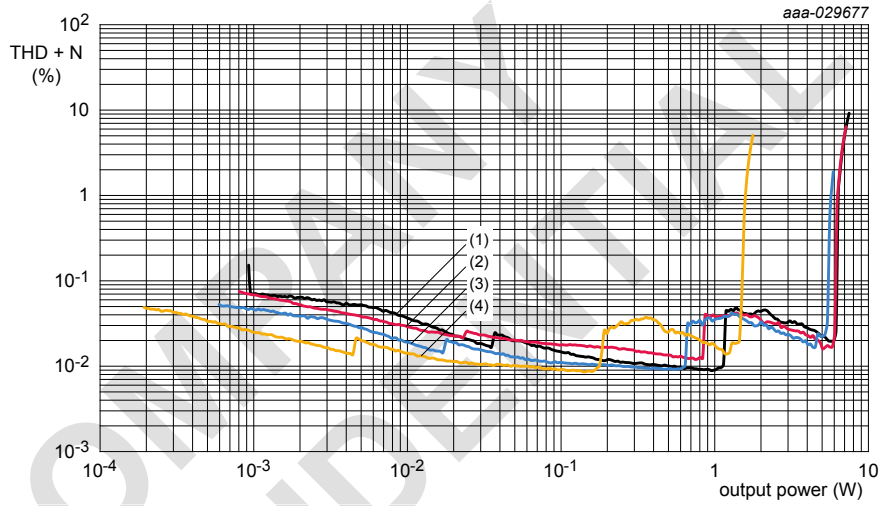


Figure 25. Typical stereo application

14.4 Curves measured in reference design

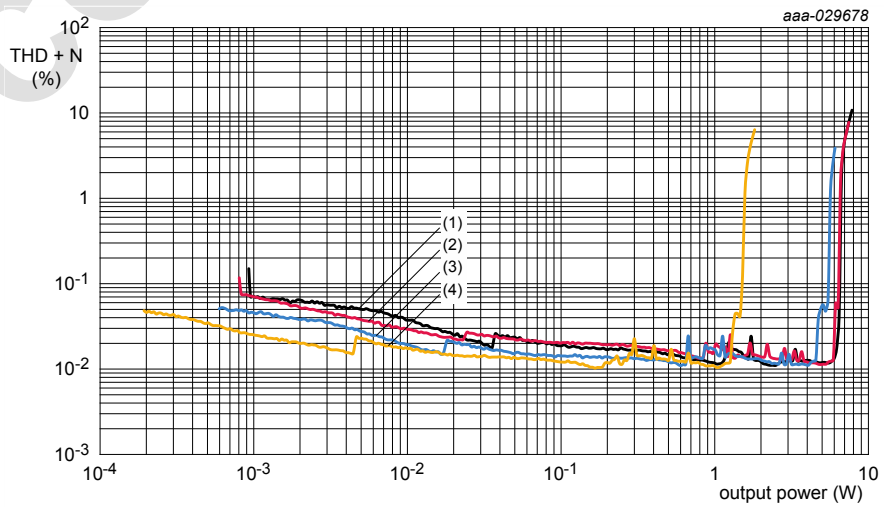
All measurements were taken on TFA9894UK reference device.

All measurements were taken with V_{BAT} = 4.0 V; V_{DDD} = 1.8 V; V_{BST} = 10 V; Adaptive boost mode; L_{BST} = 1 µH; R_L = 8 Ω; L_L = 44 µH; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; optimal settings, unless otherwise specified.



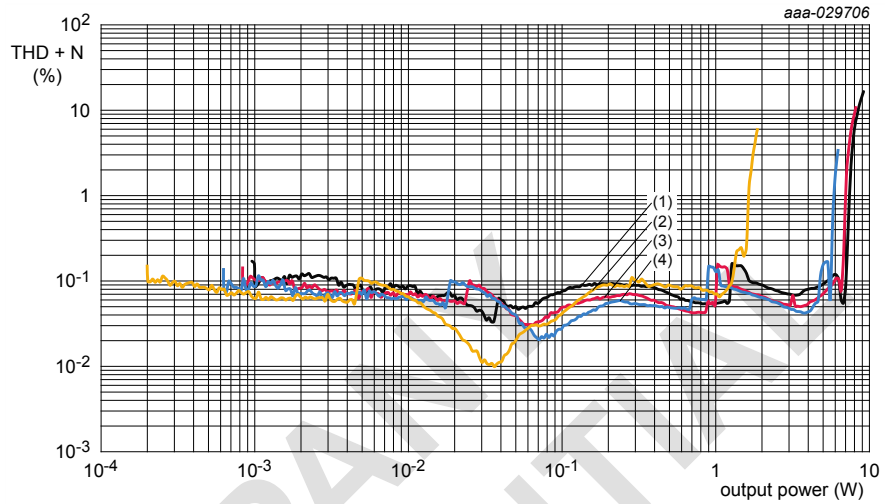
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 26. THD+N as a function of P_{out} (100 Hz)



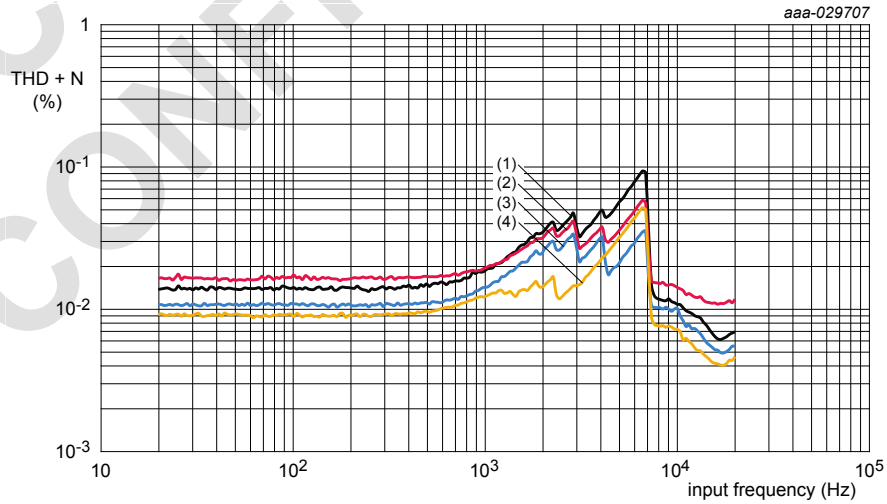
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 27. THD+N as a function of P_{out} (1 kHz)



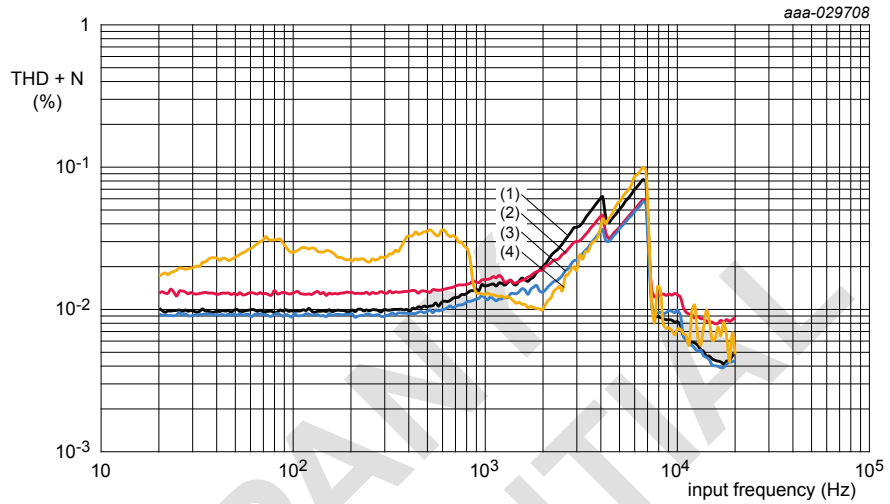
(1) 4 Ω
(2) 32 Ω
(3) 6 Ω
(4) 8 Ω

Figure 28. THD+N as a function of P_{out} (6 kHz)



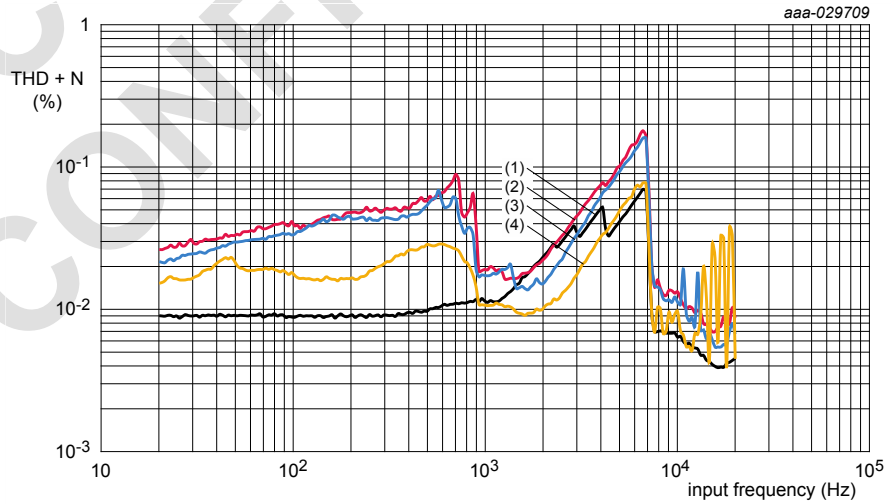
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 29. THD+N as a function of f_{in} (0.1 W)



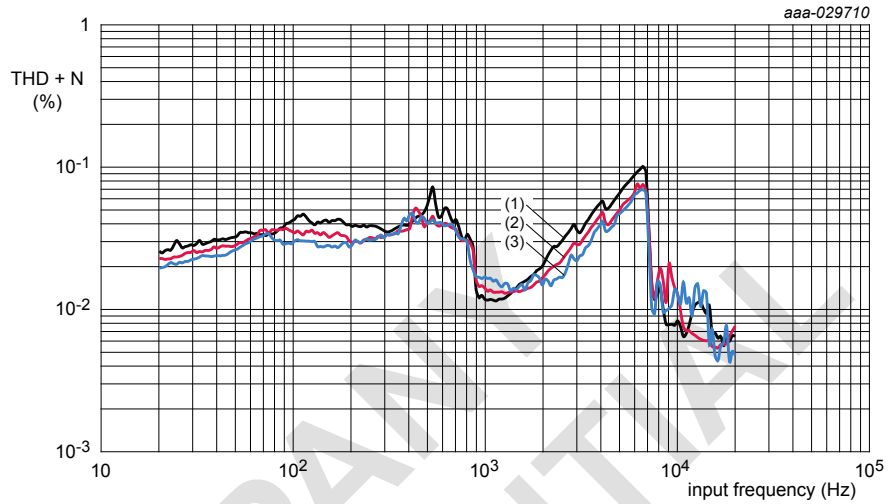
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 30. THD+N as a function of f_{in} (0.5 W)



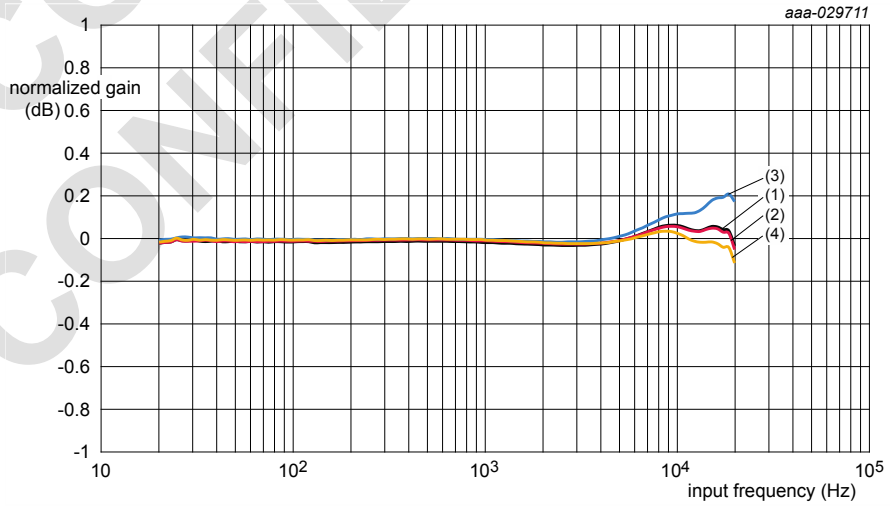
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 31. THD+N as a function of f_{in} (1.0 W)



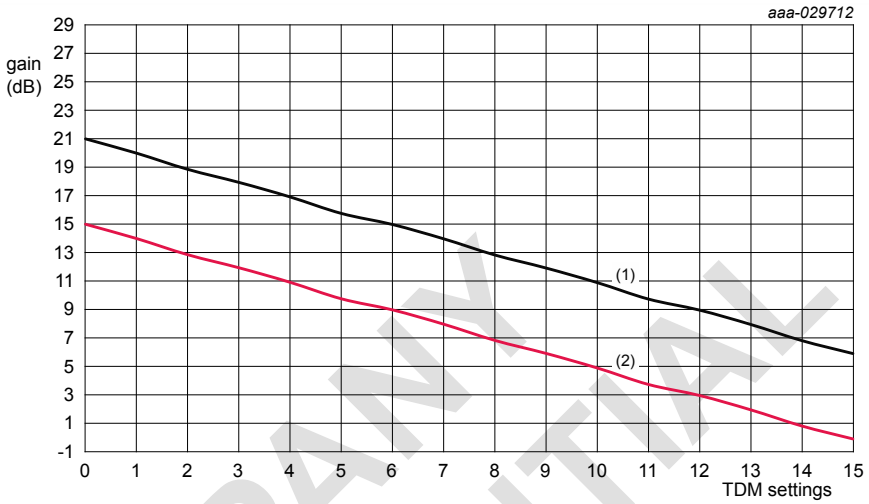
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω

Figure 32. THD+N as a function of f_{in} (2.0 W)



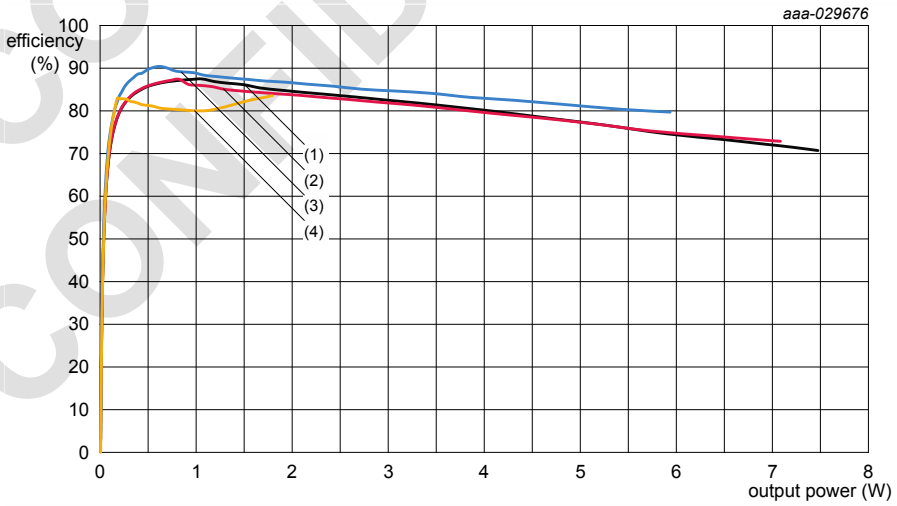
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 33. Normalized gain as as a function of f_{in}



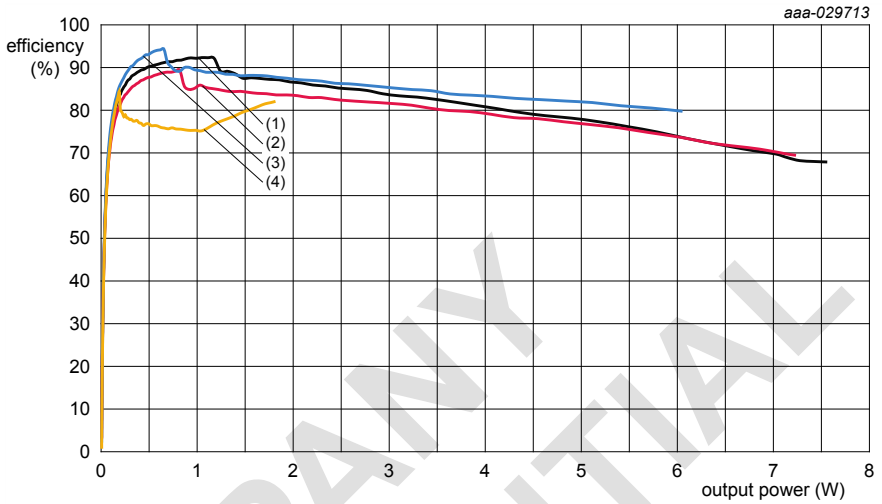
(1) INPLEV = 0
(2) INPLEV = 1

Figure 34. Gain as a function of TDM gain settings



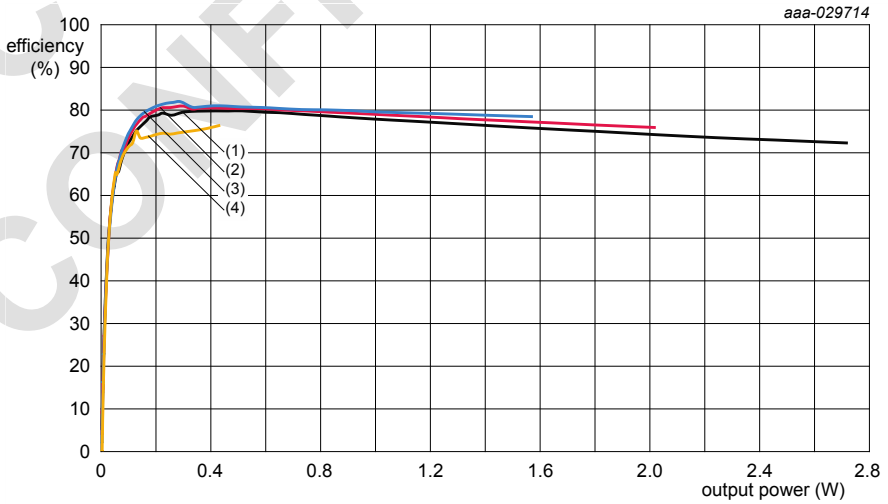
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 35. Efficiency as a function of P_{out} (100 Hz)



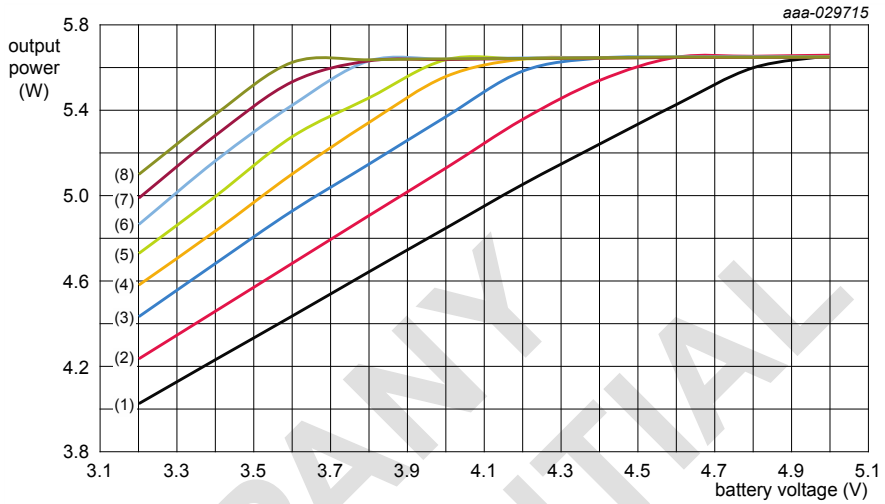
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 36. Efficiency as a function of P_{out} (1 kHz)



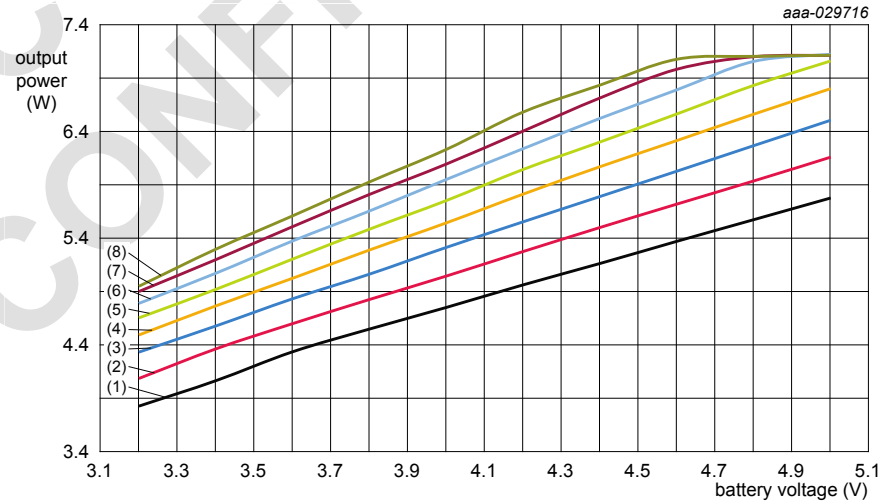
(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 37. Efficiency as a function of P_{out} (Music)



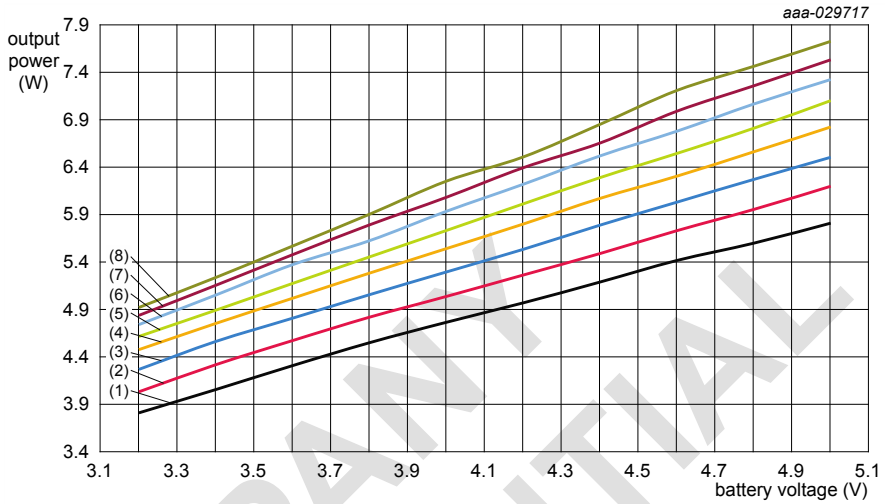
(1) DCMCC = 8; (2) DCMCC = 9;
(3) DCMCC = 10; (4) DCMCC = 11;
(5) DCMCC = 12; (6) DCMCC = 13;
(7) DCMCC = 14; (8) DCMCC = 15

Figure 38. P_{out} as a function of V_{bat} (8 Ω)



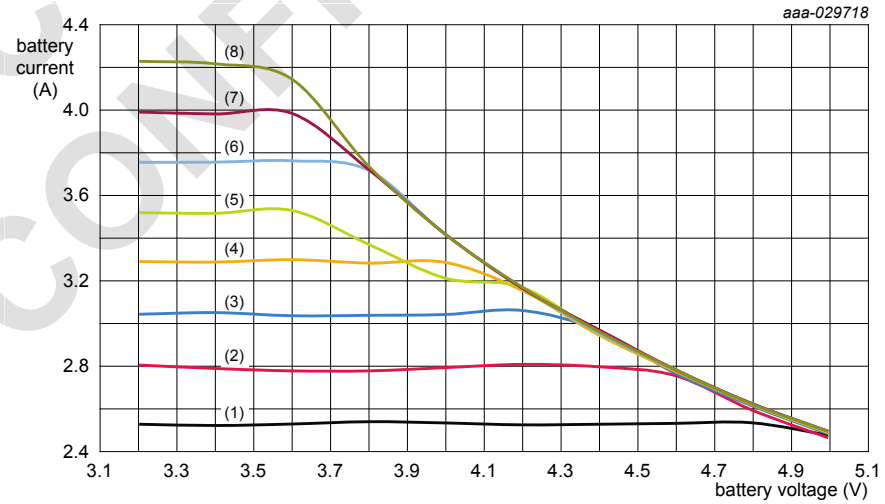
(1) DCMCC = 8; (2) DCMCC = 9;
(3) DCMCC = 10; (4) DCMCC = 11;
(5) DCMCC = 12; (6) DCMCC = 13;
(7) DCMCC = 14; (8) DCMCC = 15

Figure 39. P_{out} as a function of V_{bat} (6 Ω)



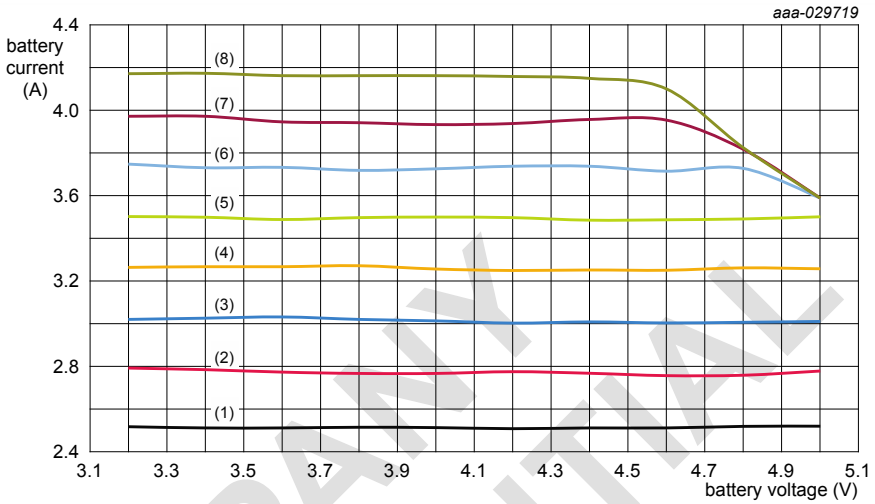
(1) DCMCC = 8; (2) DCMCC = 9;
(3) DCMCC = 10; (4) DCMCC = 11;
(5) DCMCC = 12; (6) DCMCC = 13;
(7) DCMCC = 14; (8) DCMCC = 15

Figure 40. P_{out} as a function of V_{bat} (4 Ω)



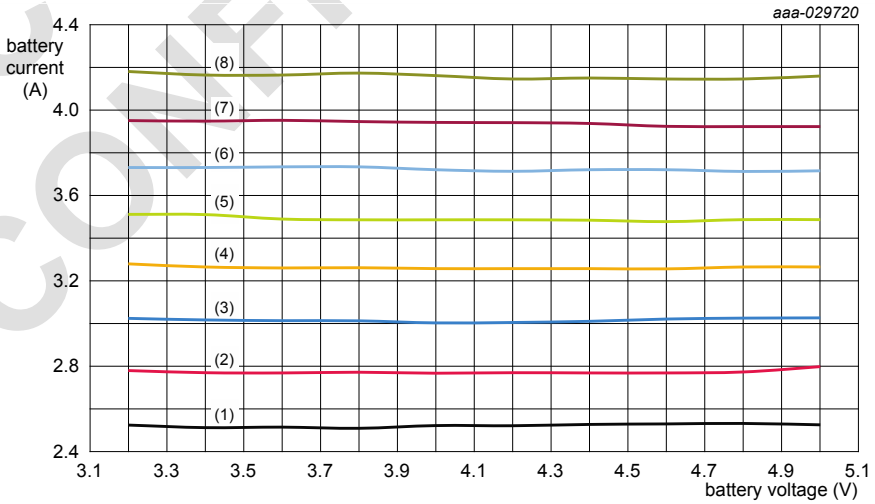
(1) DCMCC = 8; (2) DCMCC = 9;
(3) DCMCC = 10; (4) DCMCC = 11;
(5) DCMCC = 12; (6) DCMCC = 13;
(7) DCMCC = 14; (8) DCMCC = 15

Figure 41. I_{bat} as a function of V_{bat} (8 Ω)



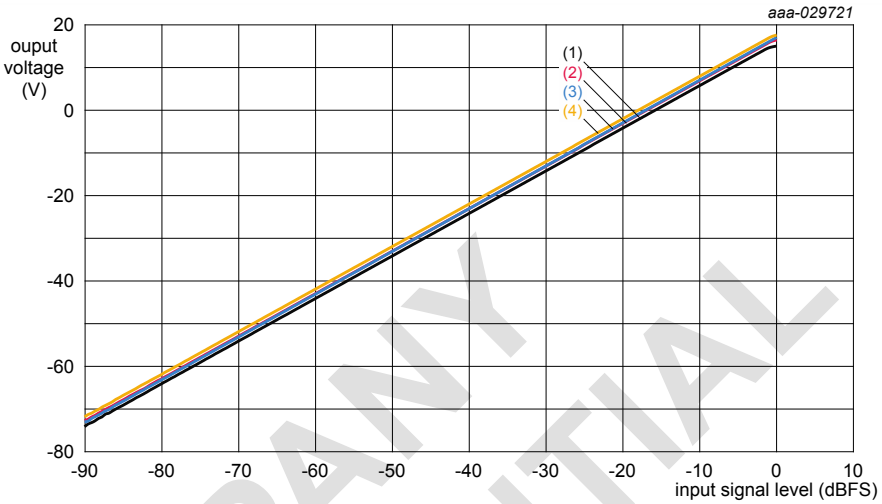
(1) DCMCC = 8; (2) DCMCC = 9;
(3) DCMCC = 10; (4) DCMCC = 11;
(5) DCMCC = 12; (6) DCMCC = 13;
(7) DCMCC = 14; (8) DCMCC = 15

Figure 42. I_{bat} as a function of V_{bat} (6 Ω)



(1) DCMCC = 8; (2) DCMCC = 9;
(3) DCMCC = 10; (4) DCMCC = 11;
(5) DCMCC = 12; (6) DCMCC = 13;
(7) DCMCC = 14; (8) DCMCC = 15

Figure 43. I_{bat} as a function of V_{bat} (4 ohms)



(1) 4 Ω
(2) 6 Ω
(3) 8 Ω
(4) 32 Ω

Figure 44. V_{out} as a function of input signal level

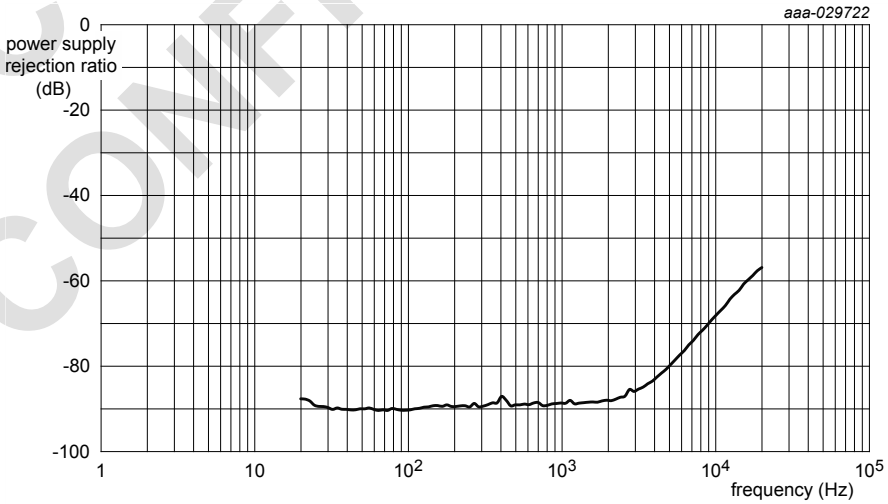


Figure 45. PSRR as a function of f_{in}

15 Package outline

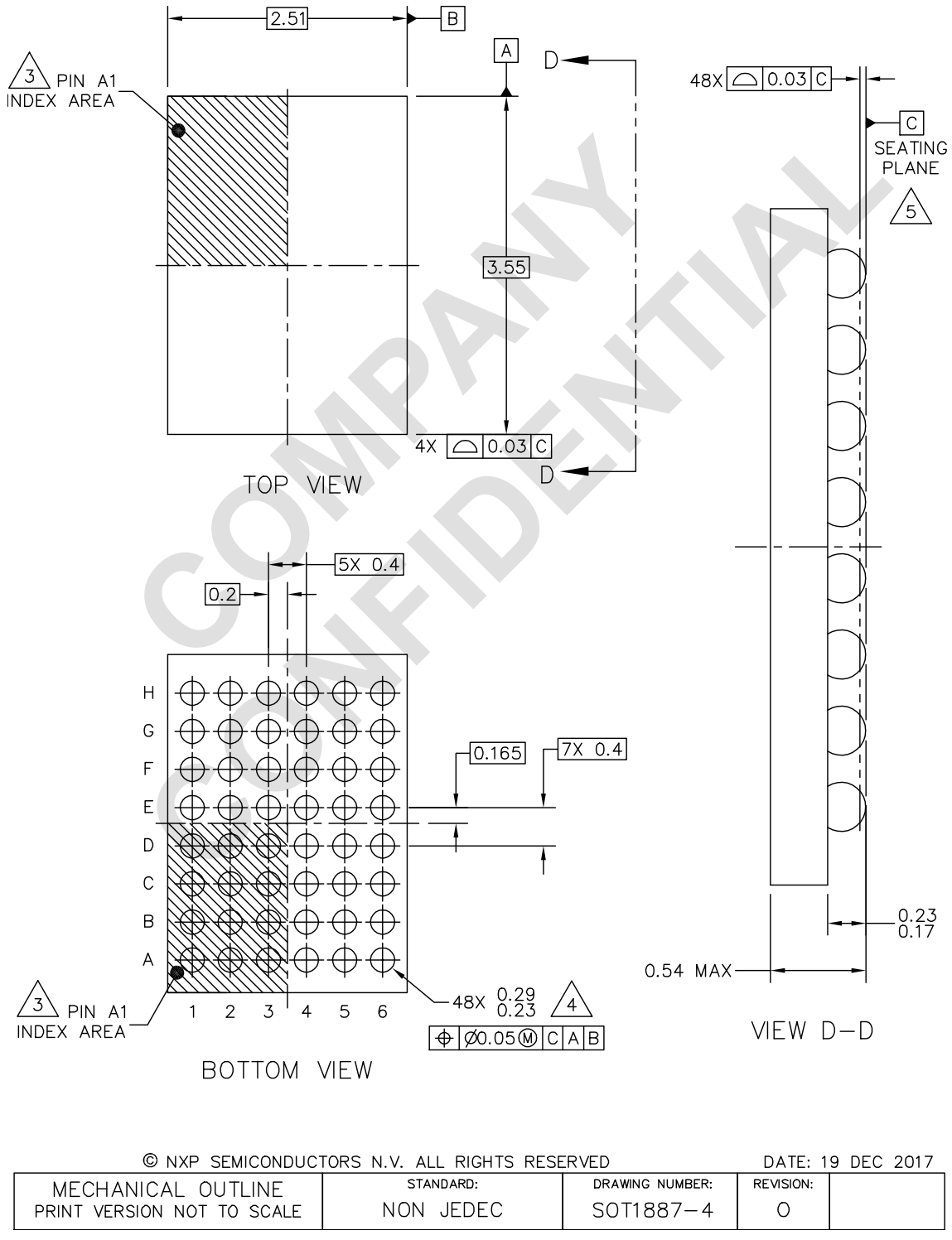


Figure 46. TFA9894DUK package outline SOT1887-4 (WLCSP48)

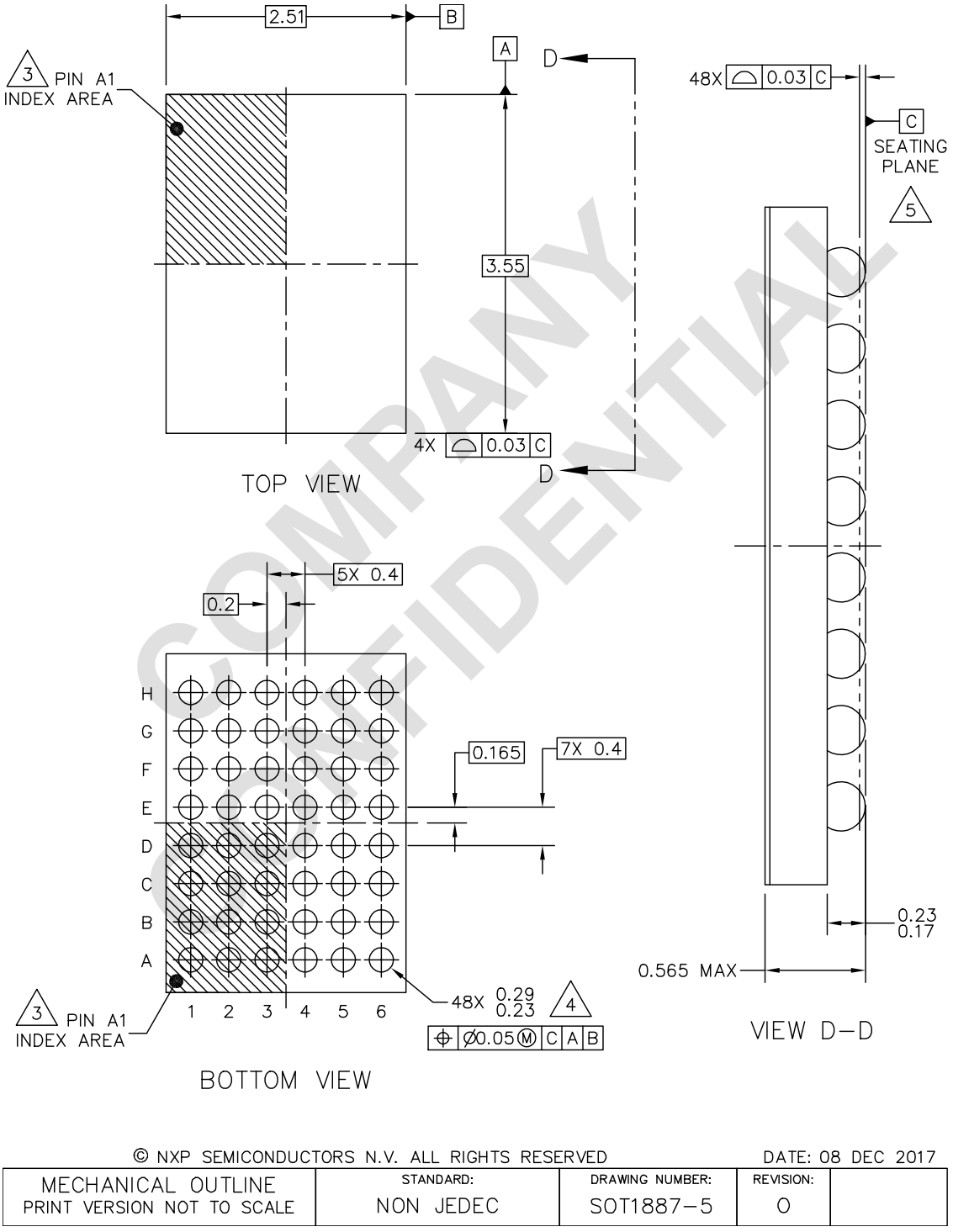


Figure 47. TFA9894EUK package outline SOT1887-5 (WLCSP48)

16 Soldering of WLCSP packages

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Scale Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

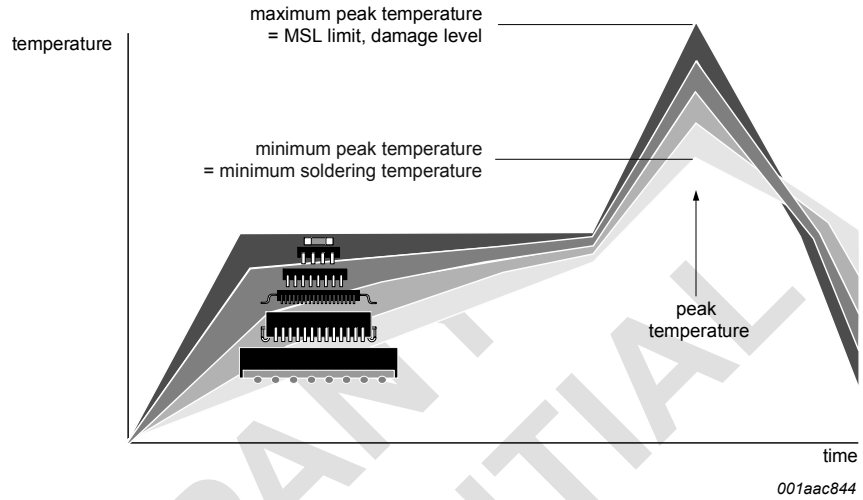
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 48) than a SnPb process, thus reducing the process window.
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board.
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 88.

Table 88. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must always be respected.

Studies have shown that small packages reach higher temperatures during reflow soldering (see Figure 48).



MSL: Moisture Sensitivity Level

Figure 48. Temperature profiles

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

16.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.3.3 Rework

In general, rework is not recommended. By rework, we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip are damaged. In that case it is recommended not to reuse the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The

surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

16.3.4 Cleaning

Cleaning can be done after reflow soldering.

17 Revision history

Table 89. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9894D_E v.1	20180613	Objective data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

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