ES7243

High Performance Stereo Audio ADC

FEATURES

- High performance multi-bit delta-sigma audio ADC
- 102 dB signal to noise ratio
- -85 dB THD+N
- 24-bit, 8 to 200 kHz sampling frequency
- I^2S/PCM master or slave serial data port
- Support TDM
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- Low power standby mode

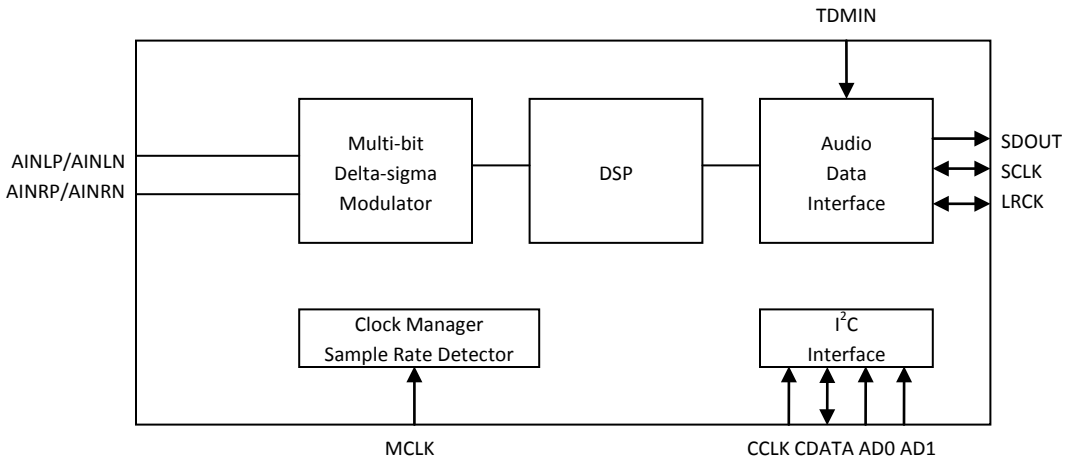
APPLICATIONS

- Mic Array
- Soundbar
- Audio Interface
- Digital TV
- A/V Receiver
- DVR
- NVR

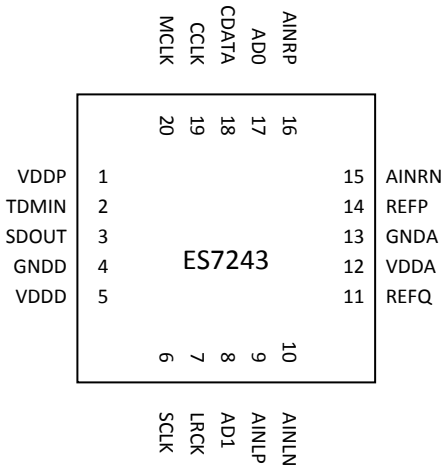
ORDERING INFORMATION

ES7243 -40°C ~ +85°C
QFN-20

BLOCK DIAGRAM

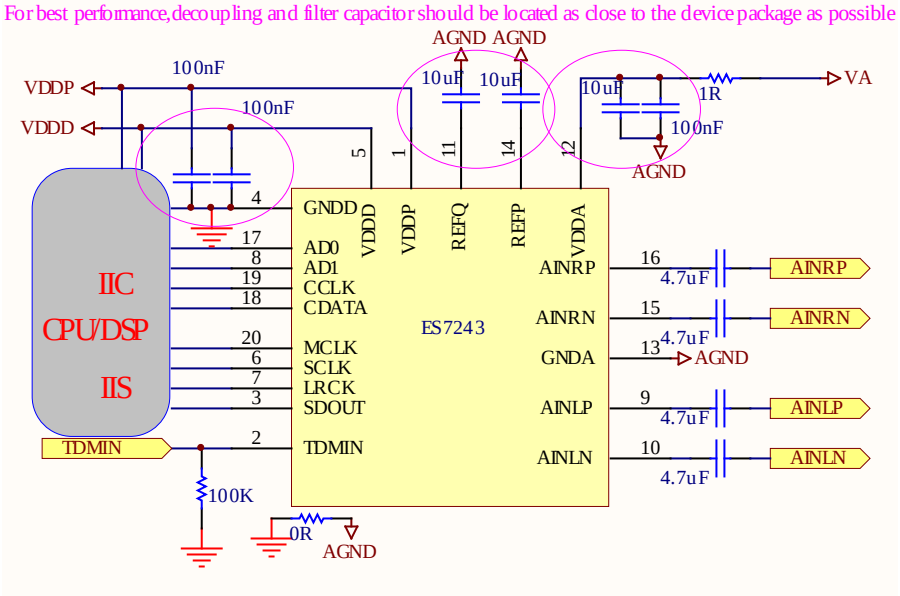


1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA	19, 18	I/O	I^2C clock and data
AD0, AD1	17,8	I	I^2C addresses
MCLK	20	I	Master clock
SCLK	6	I/O	Serial data bit clock
LRCK	7	I/O	Serial data left and right channel frame clock
TDMIN	2	I	TDM data in
SDOUT	3	O	Serial data output
AINLP, AINLN AINRP, AINRN	9, 10 16, 15	I	Analog left and right inputs
VDDP	1	I	Power supply for the digital input and output
VDDD/GNDD	5, 4	I	Digital power supply
VDDA/GNDA	12, 13	I	Analog power supply
REFP	14	O	Filtering capacitor connection
REFQ	11	O	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT



3. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (25 MHz, 26 MHz, etc).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

4. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^2C Interface Mode

	Chip Address		R/W		Register Address		Data to be written		
start	001000	AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

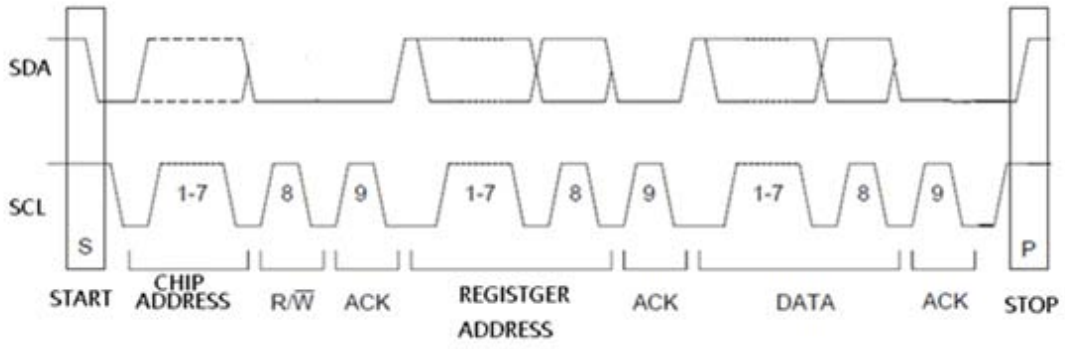


Figure 1a I²C Write Timing

Table 2 Read Data from Register in I²C Interface Mode

	Chip Address		R/W		Register Address		
Start	001000	AD0	0	ACK	RAM	ACK	
	Chip Address		R/W		Data to be read		
Start	001000	AD0	1	ACK	Data	NACK	Stop

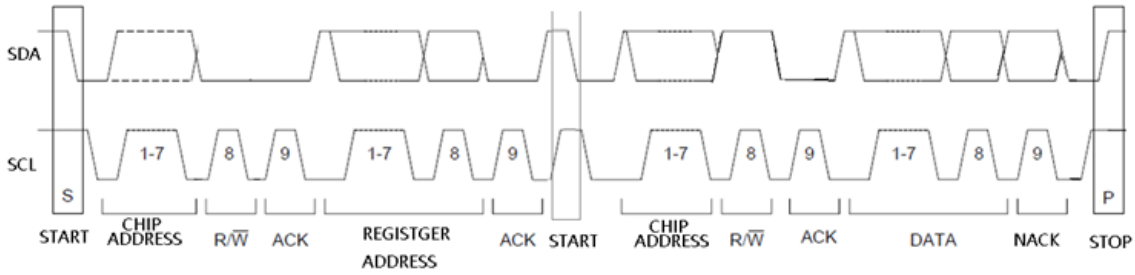


Figure 1b I²C Read Timing

5. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the output from the ADC through LRCK, SCLK and SDOUT pins. These formats are I²S, left justified and DSP/PCM mode. ADC data is out at SDOUT on the falling edge of SCLK. The relationships of SDOUT (SDATA), SCLK and LRCK with these formats are shown through Figure 2 to Figure 5. The device supports up to 8-ch of TDM, please refer to user guide for detail description.

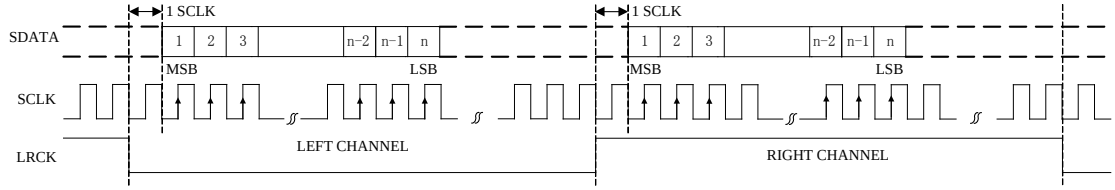


Figure 2 I²S Serial Audio Data Format Up To 24-bit

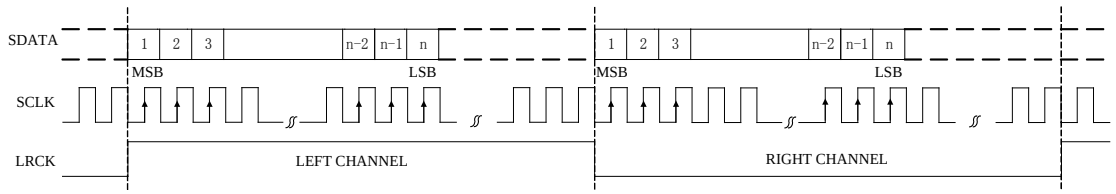


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

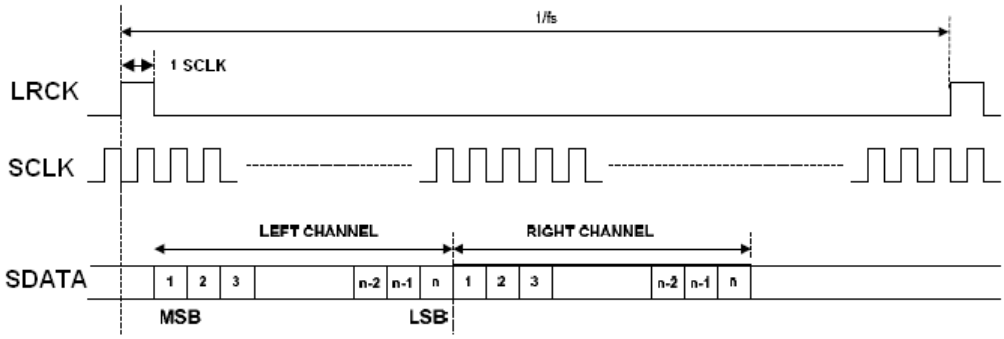


Figure 4 DSP/PCM Mode A

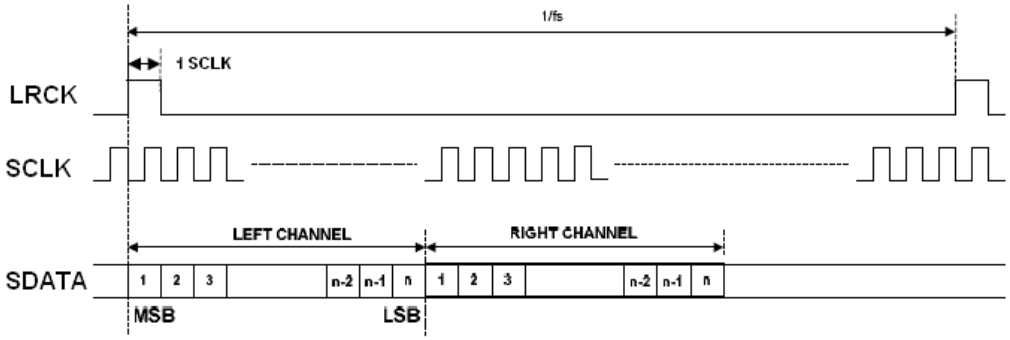


Figure 5 DSP/PCM Mode B

6. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+5.0V
Digital Supply Voltage Level	-0.3V	+5.0V
Input Voltage Range	DGND-0.3V	DVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDDA	3.0	3.3	3.6	V
VDDD	3.0	3.3	3.6	V
VDDP	1.6	3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDDA=3.3V, VDDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	95	102	104	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	95	100	105	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Quad Speed				
Passband	0		0.2083	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level		AVDD/3.3		Vrms
Input Impedance		20		KΩ

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDDD=3.3V, VDDP=3.3V, VDDA=3.3V		30		mA
Power Down Mode				
VDDD=3.3V, VDDP=3.3V, VDDA=3.3V		19		uA

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	–10	10	ns
SCLK falling to SDOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

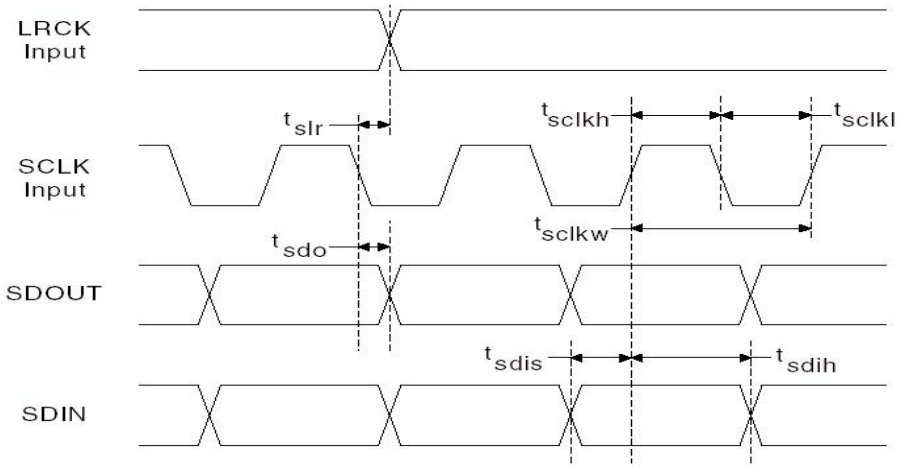


Figure 6 Serial Audio Port Timing

I^2C SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
SCL Clock Frequency	FSCL		400	KHz
Bus Free Time Between Transmissions	TTWID	1.3		us
Start Condition Hold Time	TTWSTH	0.6		us
Clock Low time	TTWCL	1.3		us
Clock High Time	TTWCH	0.4		us
Setup Time for Repeated Start Condition	TTWSTS	0.6		us
SDA Hold Time from SCL Falling	TTWDH		900	ns
SDA Setup time to SCL Rising	TTWDS	100		ns
Rise Time of SCL	TTWR		300	ns
Fall Time SCL	TTWF		300	ns

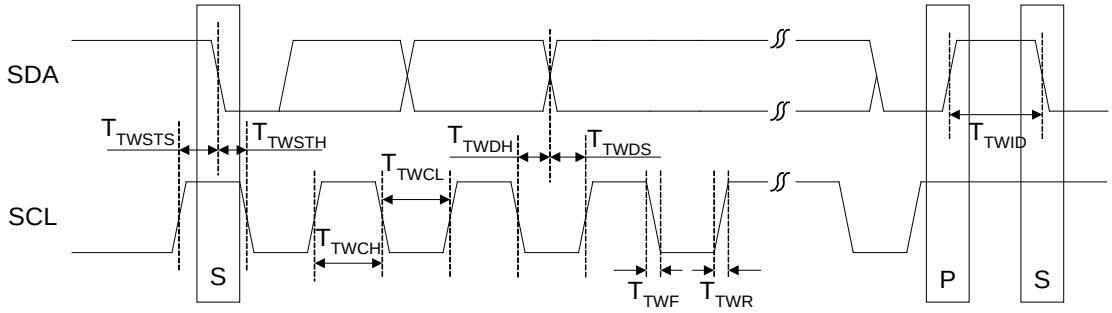


Figure 7 I²C Timing

7. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 – MODE CONFIGURE, DEFAULT 0000 0000

Bit Name	Bit	Description
Reserved	7	Reserved
MCLK_DIV	6:5	Configure internal main clock's frequence 00 – mclk div by 1 01 – mclk div by 2 10 – mclk div by 3 11 – mclk div by 4
ADC_HPF_DIS	4	ADC HPF switch 0 – ADC HPF enable 1 – ADC HPF disable
SPEED_MODE	3:2	Set output sampling frequence for chip 00 – single speed 01 – double speed 10 – quad speed 11 – not allowed
MS_MODE	1	Set chip as master mode or slave mode under software mode 0 – slave mode 1 – master mode
WORK_MODE	0	Set chip as hardward mode or software mode 0 – hardware mode 1 – software mode

REGISTER 0X01 – SERIAL DATA PORT, DEFAULT 0000 0000

Bit Name	Bit	Description
TDM_ENA	7	cascade mode enable 1 – TDM cascade mode 0 – normal mode
SP_BCLKINV	6	BCLK polarity 0 – normal 1 – invert version of bclk
SP_LRP	5	LRC polarity When chip work as I2S/Left Justify case:

		0 – L/R normal polarity Left/Right=High/Low (LJ) Left/Right=Low/High (I2S) 1 – L/R invert polarity Left/Right=Low/High (LJ) Left/Right=High/Low (I2S) when chip work as DSP mode case: 0 – Mode A, MSB is available on 2nd SCLK rising edge after LRCK rising edge 1 – Mode B, MSB is available on 1st SCLK rising edge after LRCK rising edge
SP_WL	4:2	The ata format of serial data port 000 – 24-bit 001 – 20-bit 010 – 18-bit 011 – 16-bit 100 – 32-bit
SP_PROTOCAL	1:0	The protocol of serial data port 00 – I2S 01 – LJ 10 – not allowed 11 – DSP

REGISTER 0X02 – LRCK DIVIDER, DEFAULT 0001 0000

Bit Name	Bit	Description
LRCKDIV	7:0	0xxx_xxxx – LRCK DIVIDER's coeficient = bin2dec(xxx_xxxx) * 16 1xxx_xxxx – LRCK DIVIDER's coeficient = bin2dec(xxx_xxxx) * 25

REGISTER 0X03 – BCLK DIVIDER, DEFAULT 0000 0100

Bit Name	Bit	Description
Reserved	7:6	Reserved
BCLKDIV	5:0	BCLK divider's coefficient 000000 – not allowed other – BCLK divider's coefficient

REGISTER 0X04 – CLOCK DIVIDER FOR ADC, DEFAULT 0000 0010

Bit Name	Bit	Description
Reserved	7:4	Reserved
CLK_ADC_DIV	3:0	Clock divider's coefficient for ADC under software mode 0000 – not allowed Other – Clock divider's coefficient for ADC

REGISTER 0X05 – MUTE CONTROL FOR ADC, DEFAULT 0001 0011

Bit Name	Bit	Description
Reserved	7:6	Reserved
AUTOMUTE_DETED	5	1 – chip is under mute state 0 – chip is under normal state
ADC_MUTE_SIZE	4	auto mute window size 0 – 4096 LRCK

		1 – 8192 LRCK
ADC_SDP_MUTE	3	Software Mute Enable 0 – Disable software mute sdp output 1 – Enable software mute sdp output
ADC_NOISETHD	2:1	ADC auto mute noise gate 00 – -96dB 01 – -84dB(default) 10 – -72dB 11 – -60dB
ADC_AUTOMUTE	0	Auto-mute control 0 – Auto-mute enable 1 – Auto-mute disable

REGISTER 0X06 – STATE CONTROL FOR CHIP, DEFAULT 0000 0000

Bit Name	Bit	Description
SP_TRI	7	Set SDOUT pad to 'Z' state 0 – '1' or '0' state 1 – 'Z' state
MCLK_DIS	6	disable mclk from pad 0 – enable 1 – disable
SEQ_DIS	5	0 – sequence enable 1 – sequence disable
RST_DIG	4	software reset for digital logic 0 – not reset 1 – Reset all digital logic except cp logic
RST_ADCDIG	3	software reset for digital logic 0 – not reset 1 – Reset adc logic(except cp, adc clock generate logic)
FORCE_CSM	2:0	force ADC state machine 100 – force csm_chip to PowDown 101 – force csm_chip to ChipIni 110 – force csm_chip to Normal 111 – force csm_chip to PowerUp 0xx – no force

REGISTER 0X07 – ANALOG CONTROL REGISTER 0, DEFAULT 1000 0000

Bit Name	Bit	Description
VMIDSEL	7:6	Vmid selection: 00 – Vmid disabled 01 – 50 kΩ divide 10 – 500 kΩ divide (default) 11 – 5 kΩ divide
PDN_ADCVREFGEN	5	Power down control for ADCVREF generate module 1 – power down 0 – normal
MODTOP_RST	4	Power down control for modulator top 1 – power down 0 – normal
PDN_MODL	3	Power down control for left chanel modulator

		1 – power down 0 – normal
PDN_MODR	2	Power down control for left chanel modulator 1 – power down 0 – normal
PDN_PGAL	1	Power down control for left chanel PGA 1 – power down 0 – normal
PDN_PGAR	0	Power down control for right chanel PGA 1 – power down 0 – normal

REGISTER 0X08 – ANALOG CONTROL REGISTER 1, DEFAULT 0001 0001

Bit Name	Bit	Description
Reserved	7	Reserved
GAIN_SW	6:4	PGA gain SW control
INPUT_SEL2	3	Low power control for output 0 – normal 1 – enter low power
GAIN_SEL	2:1	PGA gain SEL control SW3 SW2 SW1 SEL2 SLE1 00010 – 22.5dB 00011 – 25dB 00100 – 1dB 00101 – 3.5dB 01000 – 18dB 01001 – 20.5dB 10000 – 24.5dB 10001 – 27dB Other – not allowed
INPUT_SEL	0	AIN select 0 – AIN is not selected as analog audio input 1 – AIN is selected as analog audio input

REGISTER 0X09 – ANALOG CONTROL REGISTER 2, DEFAULT 1000 0000

Bit Name	Bit	Description
ANA_PDN	7	Power down control for whole analog 1 – power down 0 – normal
VMIDLOW	6:5	Vmid voltage: 00 – vdda/2 01 – vdda/2 - 50mV 10 – vdda/2 - 100mV 11 – vdda/2 - 150mV
ADC_LP_VRP	4	Low power control for analog VRP 1 – enter low power 0 – normal
ADC_LP_VCMMOD	3	Low power control for analog VCMMOD 1 – enter low power 0 – normal

ADC_LP_PGA	2	Low power control for analog PGA 1 – enter low power 0 – normal
ADC_LP_INT1	1	Low power control for analog INT1 1 – enter low power 0 – normal
ADC_LP_FLASH	0	Low power control for analog FLASH 1 – enter low power 0 – normal

REGISTER 0X0A – PERIOD FOR ANALOG CHARGING STATE, DEFAULT 1100 0000

Bit Name	Bit	Description
CHIPINI_CON	7:0	ChipIni state period control period=CHIPINI_CON*16/LRCK

REGISTER 0X0B – PERIOD FOR DIGITAL INITIATING STATE, DEFAULT 1100 0000

Bit Name	Bit	Description
POWERUP_CON	7:0	PowerUp state period control period=POWERUP_CON*16/LRCK

REGISTER 0X0C– PERIOD FOR DIGITAL INITIATING STATE, DEFAULT 0001 0010

Bit Name	Bit	Description
Reserved	7:6	Reserved
ADCBIAS_SWH	5:4	00 – bias1 01 – bias2 10 – bias3 11 – bias3
SRATIO_DIV	3:0	Clock divider's coefficient for ADC under hardware mode(Read only)

REGISTER 0X0D – CHIP STATE AND OSR SETTING, DEFAULT 1010 0000

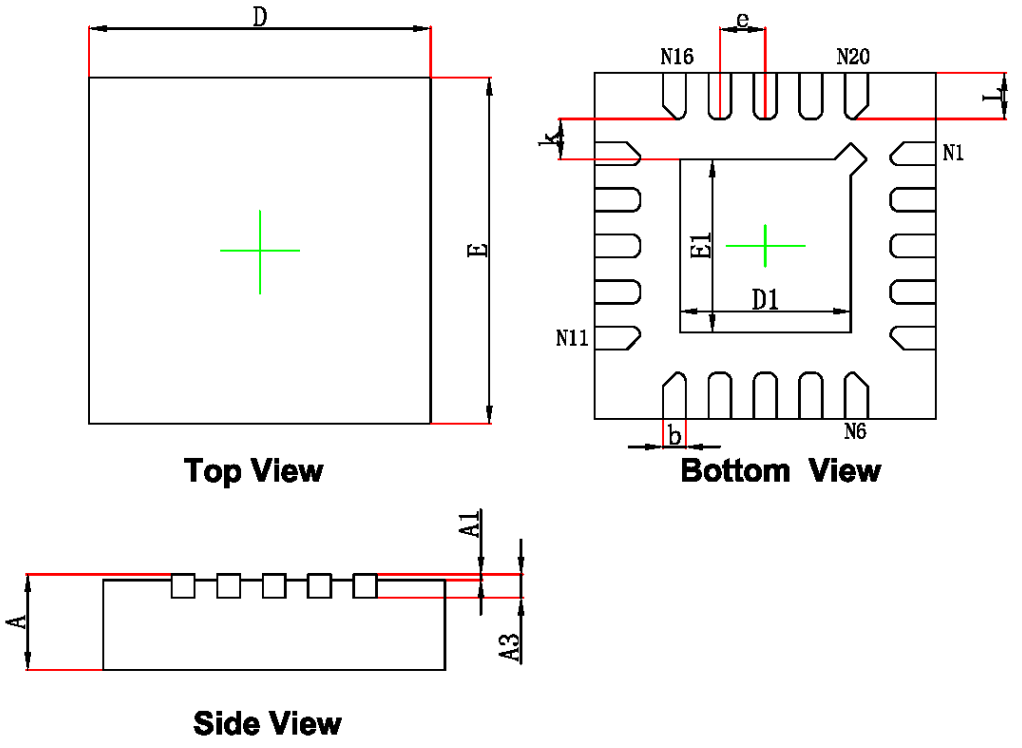
Bit Name	Bit	Description
ADC_CSM	7:6	the state of whole chip 00 – power down state 01 – chipini state 11 – powerup state 10 – normal state
ADC_OSR	5:0	output to the counter value of comb filter R – final ADC OSR as follows single speed – ADC_OSR * 4 double speed – ADC_OSR * 2 quad speed – ADC_OSR W – configure ADC OSR under software mode, the value is computed as follows: single speed – (((ADC OSR)>>2)<<2)/4 double speed – (((ADC OSR)>>2)<<2)/2 quad speed – (((ADC OSR)>>2)<<2)

REGISTER 0X0E – CHIP ID, DEFAULT 0100 0000

Bit Name	Bit	Description
CHIP_ID	7:0	Chip ID[7:5]: 000 – 93xx 001 – 71xx 010 – 72xx 011 – 73xx 100 – reserve 101 – 81xx 110 – 82xx 111 – 83xx Chip ID[4:0] – Chip Index

8. PACKAGE

QFNWB3×3-20L-A(P0.40T0.75/0.85)PACKAGE OUTLINE DIMENSIONS



Top View

Bottom View

Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
L	0.300	0.500	0.012	0.020

9. CORPORATE INFORMATION

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