North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	04
Experiment Title:	Combinational Logic Design
Course Code:	**CSE231L**
Section:	**17**
Course Name:	**Digital Logic Design Lab**
Lab Group #:	02
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Objectives

- Design a complete, minimal combinational logic system from specification to implementation.
- Minimize combinational logic circuits using Karnaugh maps.
- Learn various numerical representation systems.
- Implement circuits using 1st and 2nd canonical minimal forms

Equipment List

- Trainer Board
- 1* IC 7400 2-input NAND gates
- 2* IC 7408 2-input AND gates
- 1* IC 4073 Triple 3-input AND gates
- 1* IC 4075 Triple 3-input OR gates

Theory

K-Map:

K-Map or Karnaugh map is a visual technique used to simplify boolean expressions without having to use boolean algebra theorems and equation manipulations. A K-Map can be considered as a specialized form of a truth table. It consists of a grid of squares, where each square represents a minterm, and it is arranged in such a way that follows the Grey-Code sequence.

BCD:

BCD or binary coded decimal is a way to represent decimal numbers in binary form. In BCD, each decimal digit is represented by a 4-bit binary number. For example:

Decimal Number	BCD
2	0010
5	0101
8	1000

Excess-3:

The Excess-3 is also a 4-bit binary number derived from adding 3 (0011) to the BCD number. For example:

Decimal Number	BCD	Excess-3
2	0010	0101
5	0101	1000
8	1000	1011

Circuit Diagram:

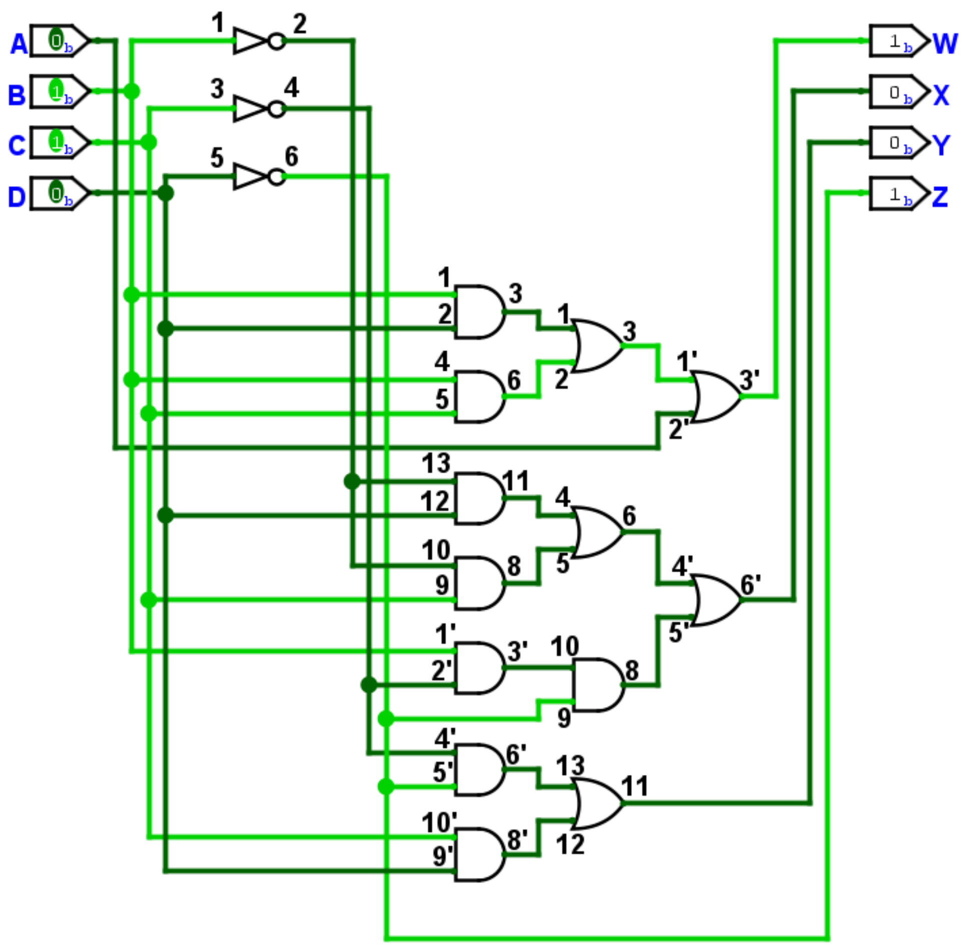

Figure E2: Minimal 1st canonical circuit of BCD to Excess-3 converter

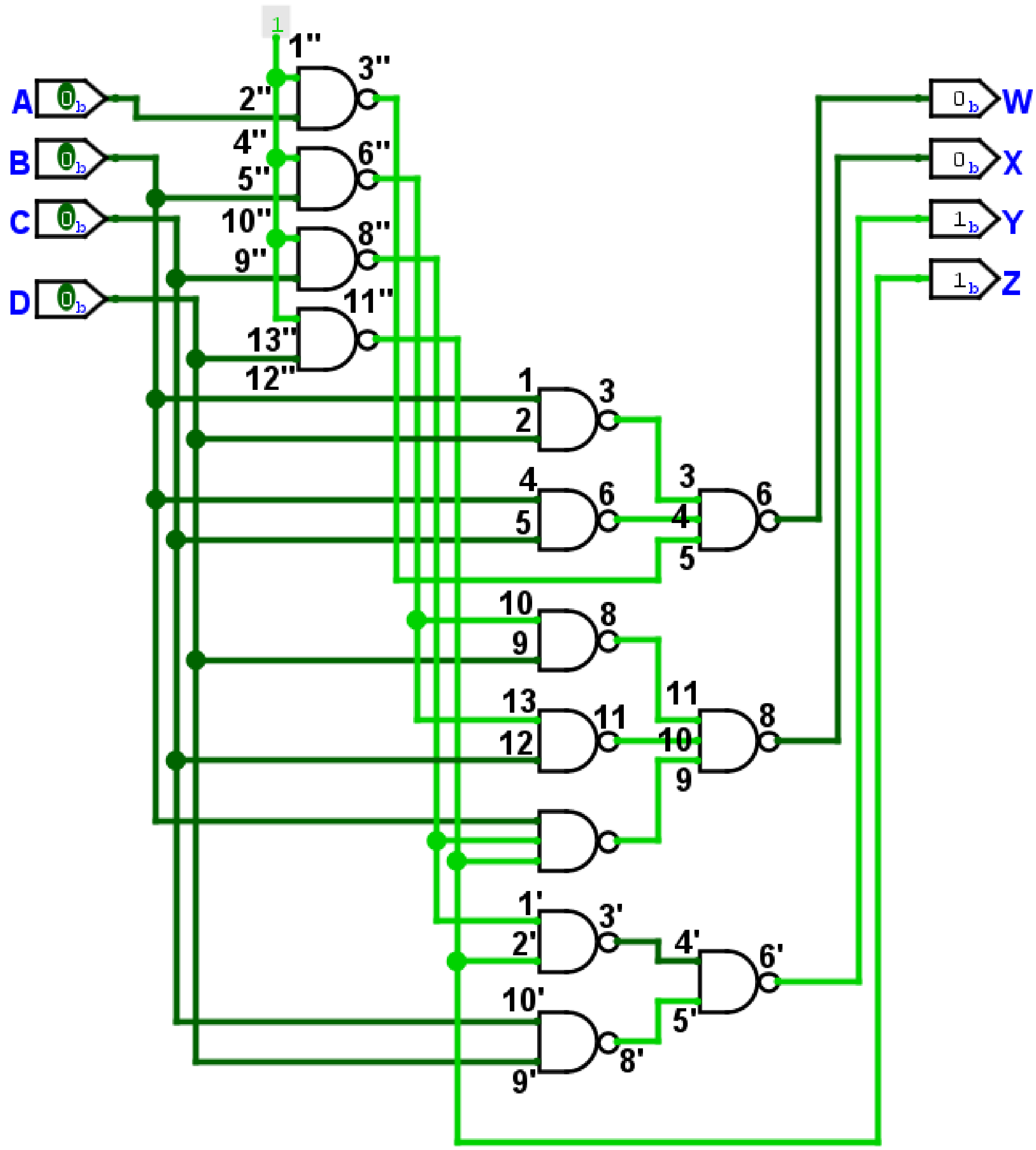

Figure E3: Minimal universal gate implementation of BCD to Excess-3 converter

Data Table & Equation

	Binary Coded Decimal (BCD)				Excess-3			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	1	0	1	0	X	X	X	X
11	1	0	1	1	X	X	X	X
12	1	1	0	0	X	X	X	X
13	1	1	0	1	X	X	X	X
14	1	1	1	0	X	X	X	X
15	1	1	1	1	X	X	X	X

Number of input bits:	4	Input variables:	4 (A, B, C, D)
Number of output bits:	4	Output variables:	4 (W, X, Y, Z)

K-Maps:

AB/CD	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

W

$$W = B\,D + B\,C + A$$

AB/CD	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	X	X	X	X
10	0	1	X	X

X

$$X = \overline{B}\,D + \overline{B}\,C + B\,\overline{C}\,\overline{D}$$

AB/CD	00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	X	X	X	X
10	1	0	X	X

Y

$$Y = \overline{C}\,\overline{D} + C\,D$$

AB/CD	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

Z

$$Z = \overline{D}$$

Discussion

The primary objective behind performing this experiment was to design a combinational logic circuit from the specification, in the form of BCD to Excess-3 converter, and implement it. Since no boolean function for the BCD to Excess-3 converter was available, we had to derive it from the corresponding BCD-Excess-3 Table E1, based on the idea of Sum of Products(Minterms) and Product of Sums(Maxterms). As there is a need to reduce the complexity of the circuit, in terms of minimization and number of gates reduction, Karnaugh maps were used to minimize the function. The obtained function was verified using the Combinational Analysis feature of Logisim and later implemented using basic logic gates and universal logic gates.

The biggest adversary we faced while implementing the circuit was the growing complexity of the circuit in terms of managing the wire connection between the gates. As a result, we simulated the circuit beforehand in Logisim and followed it to maintain the wire connection between the gates.

The successful completion of this experiment demonstrates the idea that digital circuits can be designed to deliver specific outputs, which in turn will perform another set of actions based on the output. It is awe-striking how typical its applications are in our everyday life, e.g., the LED display of digital clocks. In conclusion, we are grateful to our lab instructor for guiding us throughout the session while completing the experiment, which also would not have been possible without our fellow group mates' perseverance and continuous effort.

Logisim Simulation

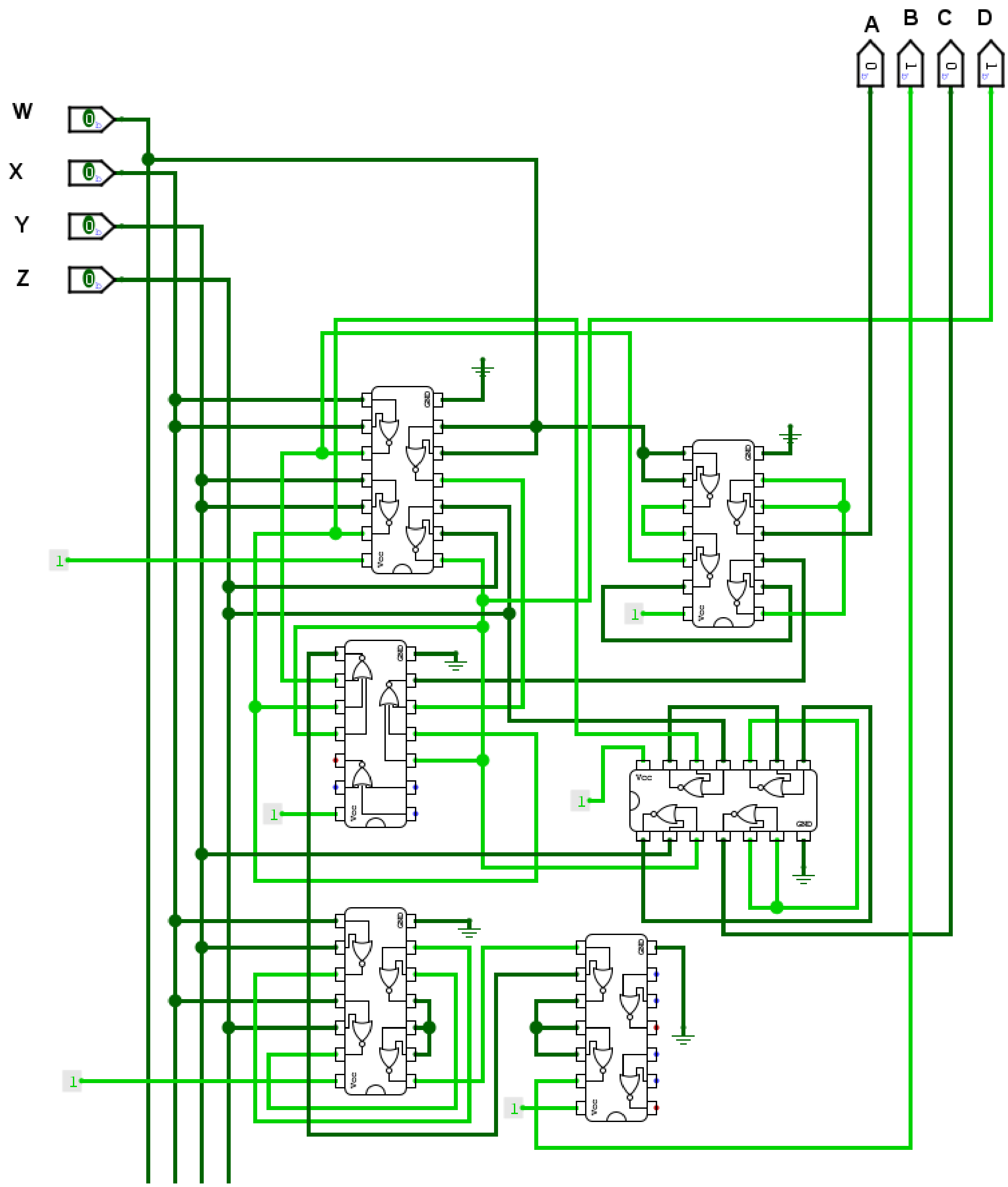

Fig: Minimal NOR logic implementation of Excess-3 to BCD converter.