North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	08
Experiment Title:	Synchronous Sequential Circuits
Course Code:	**CSE231L**
Section:	**17**
Course Name:	**Digital Logic Design Lab**
Lab Group #:	02
Written By:	Tanvir Ahmed
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Objectives:

1. Gain a practical understanding of State Diagrams and State Table
2. Designing and implementation of a Synchronous Sequential Circuit given a State Diagram
3. Understanding the concept of designing Sequential Circuits using Flip-Flop

Equipment List:

1. 1 * IC 74107 JK Flip-Flop
2. 1 * IC 7408 2-input AND gates
3. 1 * IC 7404 Hex inverters (NOT gates)
4. 1 * IC 7432 2-input OR gates
5. 1 * IC 7474 Dual D Flip-Flop
6. Trainer board
7. Wires

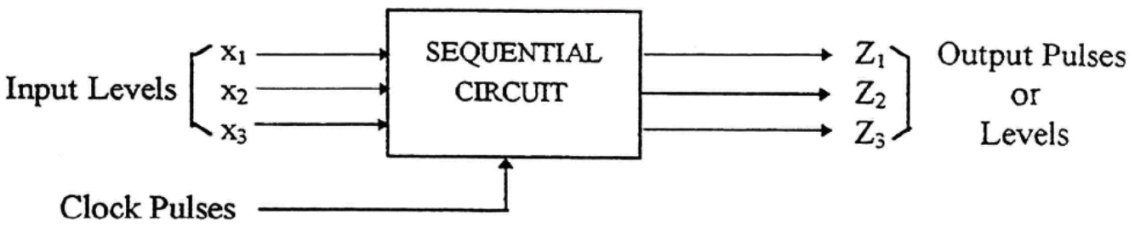
Theory:

Synchronous Sequential Circuits:

A synchronous circuit is a type of digital circuit where changes in the state of memory elements occur in sync with a clock signal. In such circuits, data is stored using memory devices like flip-flops or latches. The output of a flip-flop remains stable until its clock input receives a pulse, at which point the current input is transferred to the output.

These circuits rely on an electronic oscillator, known as a clock, which generates a series of pulses called the clock signal. This signal is applied to all storage elements, ensuring that, ideally, all changes in their logical states occur simultaneously. To function correctly, the inputs to the storage elements must stabilize before the next clock pulse, allowing the circuit's behavior to be predictable.

Synchronous circuits process inputs as pulses or as a combination of levels and pulses, with specific constraints on pulse width and propagation delay. These circuits are categorized into clocked sequential circuits and unclocked (or pulsed) sequential circuits. Clocked sequential circuits, which commonly use flip-flops or gated latches as memory elements, incorporate a periodic clock signal to synchronize all internal state transitions.



Clocked Sequential Circuit

State Table

A state table is a representation of a sequential circuit that consists of three parts: the present state, the next state, and the output. The **present state** refers to the state of the flip-flops before a clock pulse occurs, the **next state** indicates the state of the flip-flops after the clock pulse, and the **output** section specifies the output values corresponding to the present state.

State Diagram

A state diagram provides a graphical representation of flip-flops and their behavior. In this diagram, each state is depicted as a circle, and transitions between states are shown as directed lines or arcs connecting the circles.

Data Table & Equation:

Constructing a Sequential Circuit using JK Flip-Flops:

Present State		Input	Next State		Output	Flip-Flops Input			
A	B	X	A	B	Y	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	X	1	X
0	0	1	1	0	1	1	X	0	X
0	1	0	0	1	0	0	X	X	0
0	1	1	1	0	1	1	X	X	1
1	0	0	1	0	0	X	0	0	X
1	0	1	0	0	0	X	1	0	X
1	1	0	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X

Table: State Table for circuit using JK Flip-flops

0	1	1	0
X	X	X	X

$J_A=X$

X	X	X	X
0	1	X	X

$K_A=X$

1	0	X	X
1	0	X	X

$J_B=A'X'$

X	X	1	0
X	X	X	X

$K_B=X$

0	1	1	0
0	0	X	X

Y=A'X

Constructing a Sequential Circuit using T Flip-Flops:

Present State		Input	Next State		Output	Flip-Flops Input	
A	B	X	A	B	Y	T_A	T_B
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	0
0	1	1	1	0	1	1	1
1	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0
1	1	0	X	X	X	X	X
1	1	1	X	X	X	X	X

Table: State Table for circuit using T Flip-flops

0	1	1	0
0	1	X	x

$T_A=X$

1	0	1	0
0	0	X	x

$T_B=BX+A'B'X'$

0	1	1	0
0	0	X	X

$Y=A'X$

Constructing a Sequential Circuit using D Flip-Flops:

Present state		Input	Next state		Output	Flip-flop input functions	
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	1	1	1	1	1	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	1	0	X	X	X	X	X
1	1	1	X	X	X	X	X

Table: State Table for circuit using D Flip-flops

0	1	1	0
1	0	X	x

$D_A=A'X+AX'$

1	0	0	1
0	0	X	x

$D_B=A'X'$

0	1	1	0
0	0	X	X

$Y=A'X$

Discussion:

In this experiment, we studied the behavior of synchronous sequential circuits, focusing on the role of clock signals in synchronizing state transitions within memory elements like flip-flops. The clock pulse dictates when data is latched, ensuring predictable and stable circuit operation. We observed how delays in the clock distribution network can impact performance, highlighting the need for careful design to avoid timing issues.

We also compared clocked and unclocked sequential circuits. In clocked circuits, outputs change with each clock pulse and remain stable between pulses. In contrast, pulsed circuits change states in response to specific pulse durations. We saw that the pulse width and timing are crucial for correct operation in pulsed circuits.

This experiment demonstrated the importance of precise timing and synchronization for reliable circuit performance and reinforced the need for careful clock management in digital system design.

Logisim Simulation

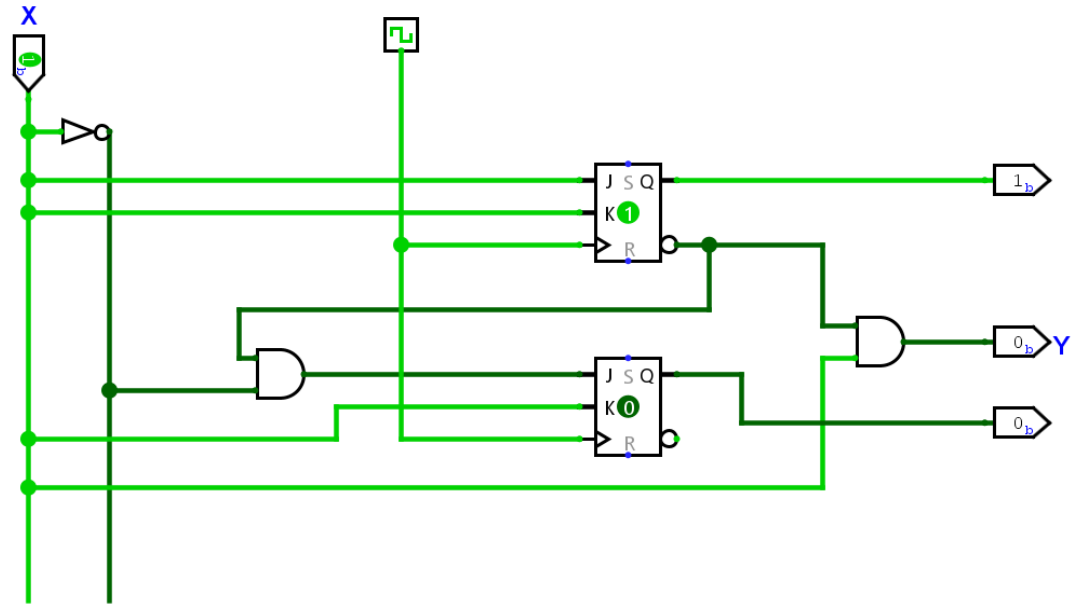


Fig : JK Flip-Flop

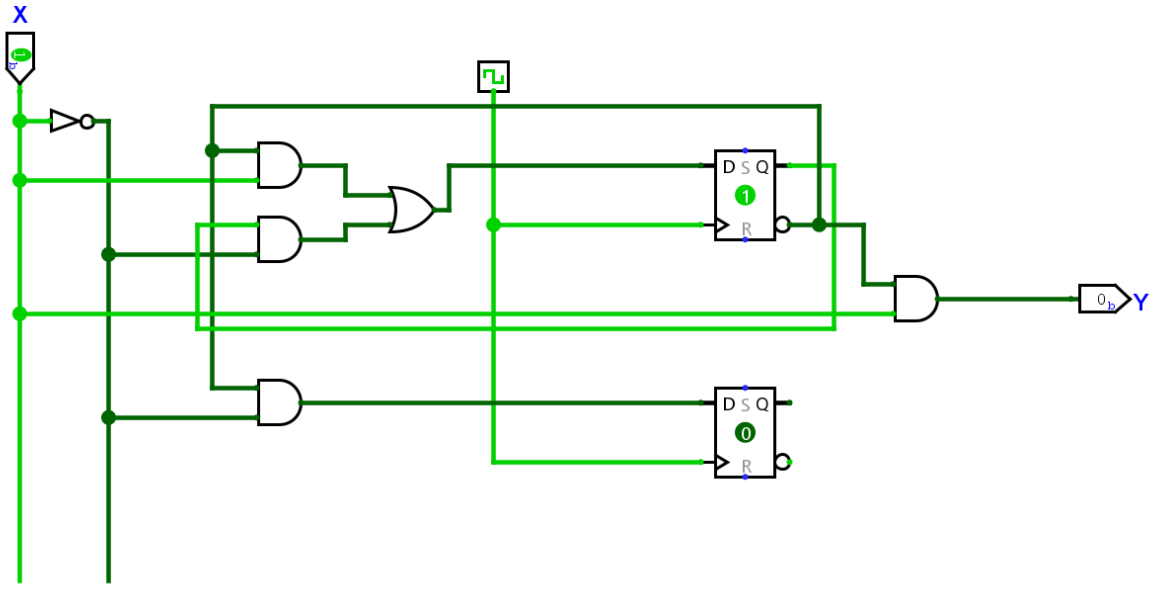


FIg : D Flip-Flop

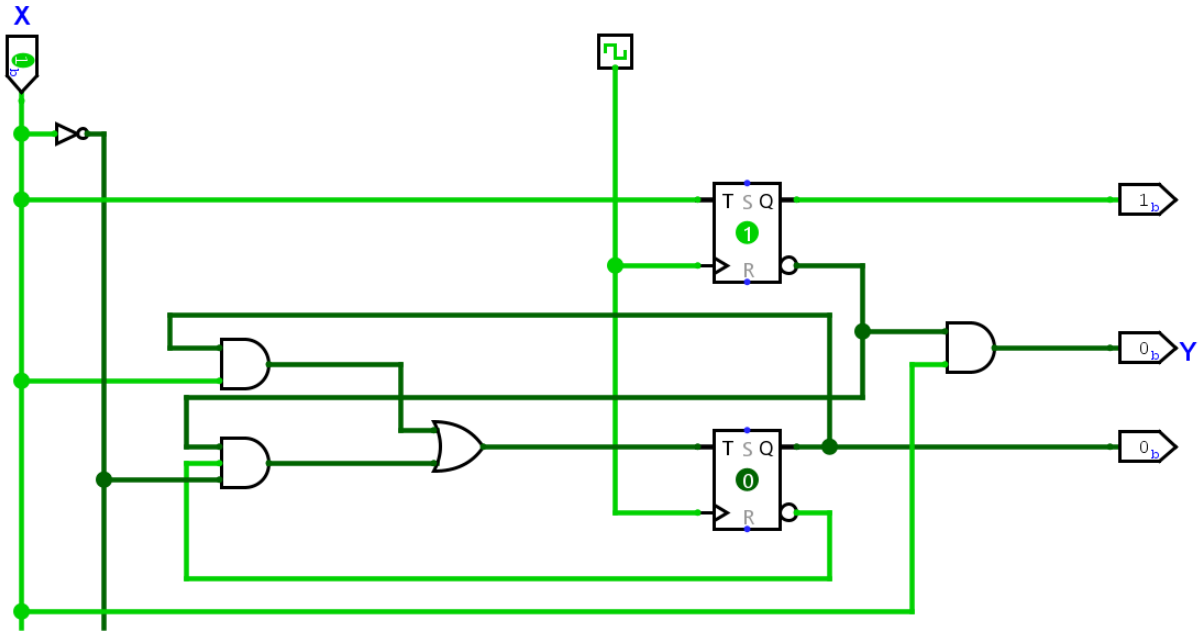


Fig : T Flip-Flop