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North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	06
Experiment Title:	Introduction to Multiplexers & 3 to 8 line Decoder
Course Code:	**CSE231L**
Section:	**17**
Course Name:	**Digital Logic Design Lab**
Lab Group #:	02
Written By:	
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Objectives

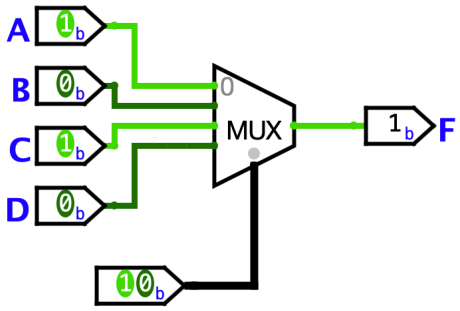
- Understand the concept of multiplexing in the context of digital logic circuits.
- Implement digital logic functions using multiplexers.
- Observe and analyze the operations of the 3 to 8 Line Decoder

Equipment List

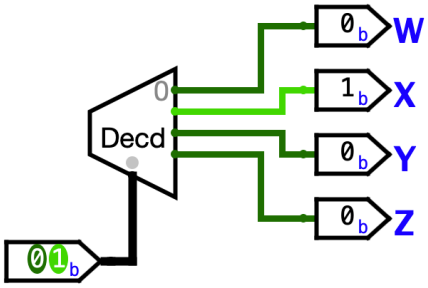
- Trainer board
- 1 x IC 7404 Hex Inverters (NOT gates)
- 1 x IC 74151 8:1 Line Multiplexer
- 1 x IC 74138 3 to 8 line Decoder

Theory

Multiplexers: A Multiplexer or Mux is a combinational circuit that chooses one of the input lines and directs it to the single output line based on the control input. A multiplexer contains 2^n input lines and n control lines. There are several types of muxes (based on the number of control lines n), like 2:1 Mux, 4:1 Mux, 8:1 Mux etc. Given below is the figure of 4:1 Mux:



Decoders: A Decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. A decoder enables one of the many output lines based on the input value. Each output line can be represented by a minterm. Given below is the figure of 2:4 Decoder.



Circuit Diagram

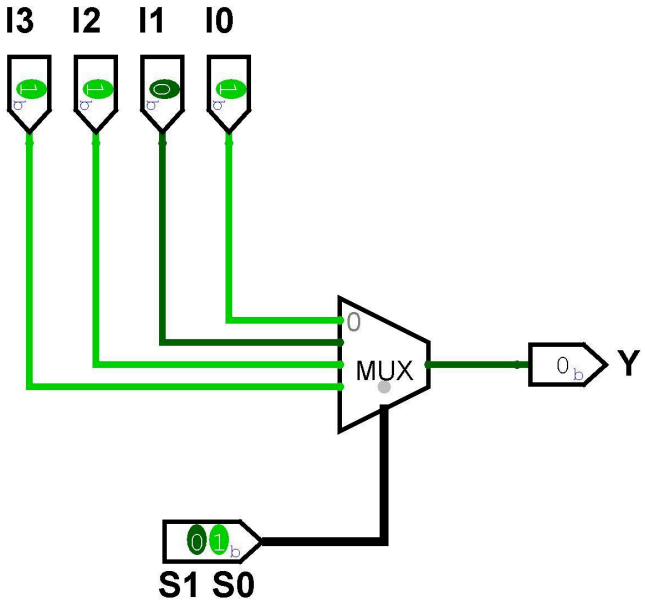


Fig. 4:1 MUX

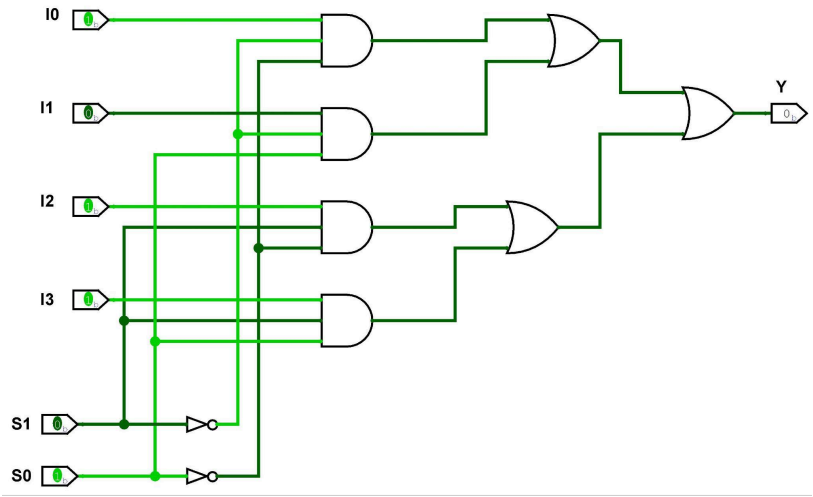


Fig. Logic Diagram of 4:1 MUX

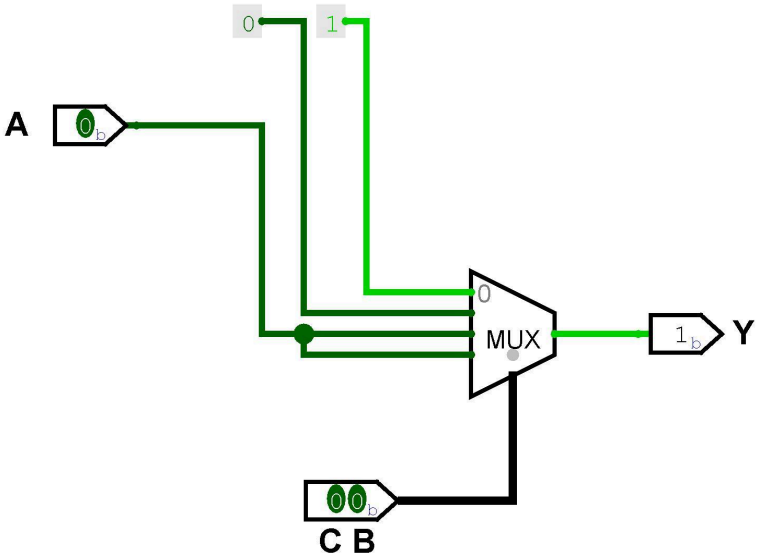


Fig. Implementation of Job 1 using 4:1 MUX

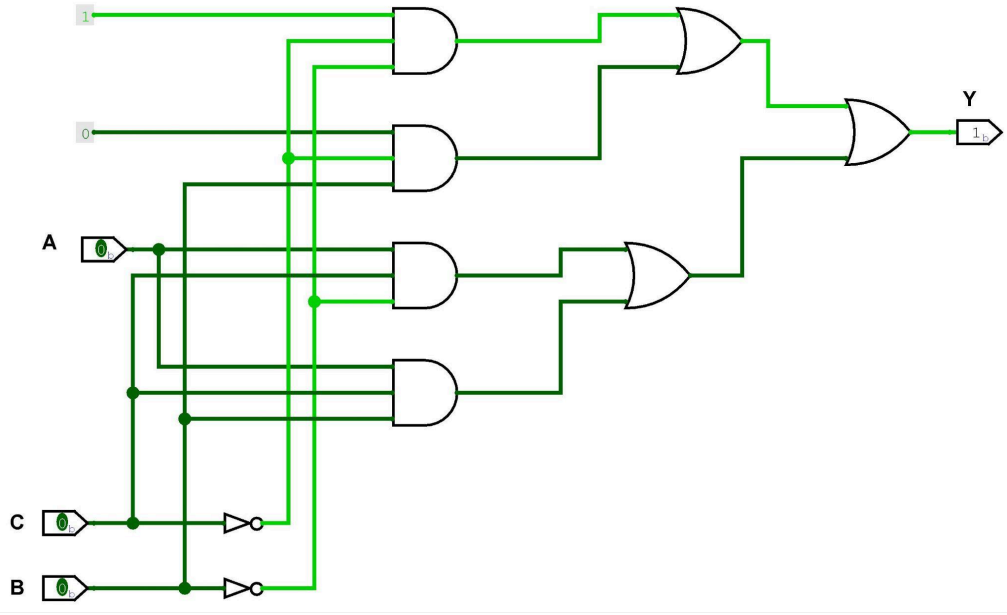


Fig. Logic Diagram of Job 1

Data Table & Equation

A	B	C	D	F	I
0	0	0	0	1	$I_0 = 1$
0	0	0	1	1	
0	0	1	0	0	$I_1 = D$
0	0	1	1	1	
0	1	0	0	0	$I_2 = D$
0	1	0	1	1	
0	1	1	0	0	$I_3 = 0$
0	1	1	1	0	
1	0	0	0	1	$I_4 = 1$
1	0	0	1	1	
1	0	1	0	0	$I_5 = 0$
1	0	1	1	0	
1	1	0	0	0	$I_6 = 0$
1	1	0	1	0	
1	1	1	0	1	$I_7 = 1$
1	1	1	1	1	

Table Job 2: Using an 8:1 MUX to implement a Boolean function

Enable Inputs		Select Inputs			Outputs							
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Table Job 3: Function table for 3 to 8 Line decoder

Discussion

The experiment was performed in order to implement and understand the usage of Multiplexers and Decoders in Digital Circuits. The experiment was divided into three subtasks, which included the demonstration of the Multiplexer and Decoder, and implementation of a boolean function using Multiplexer. In order to implement the circuits successfully, the circuits were simulated first using Logisim, and the wire/pin connections were followed to implement the circuits physically. In case of any discrepancies experienced, the simulated results were followed to debug the circuit.

The major adversary faced during conducting the experiment was managing the wire/pin connections between the IC and the trainer board. Other than that, no major issues were faced which hindered the way of completing the experiment.

The experiment provided us with an insight about the usefulness of Multiplexers and Decoders in Digital Circuits, that govern the day-to-day usage in our everyday life. In cases, where we have limited channels to send the signals, multiplexers can be used to select and send the desired signals, according to the requirement. This simplifies the circuit, as multiple inputs can be associated with one resource, instead of establishing one-to-one connections with the resource. Whereas, the decoder can be used to compose a n-bit signal into m-bit signal, which can be used in the conversion of analog to digital signals. In conclusion, the supervision of our lab instructor and the consistent effort by our

group members should be acknowledged for the successful completion of this experiment.

Data Sheet

Logisim Simulation

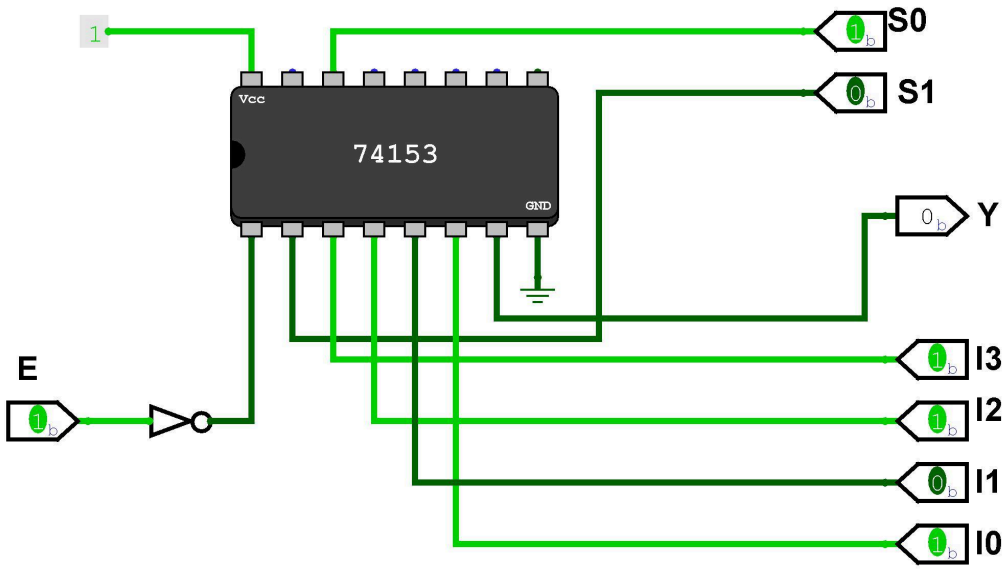


Fig. Simulation of 4:1 MUX for the Input I1.

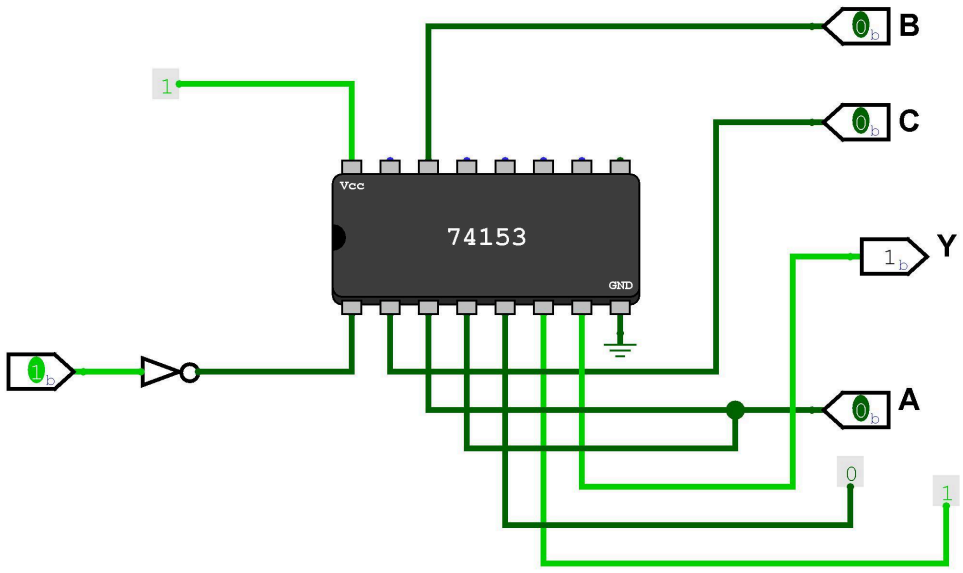


Fig. Simulation of Job 1(*Implementation of a boolean function using 4:1 MUX*)

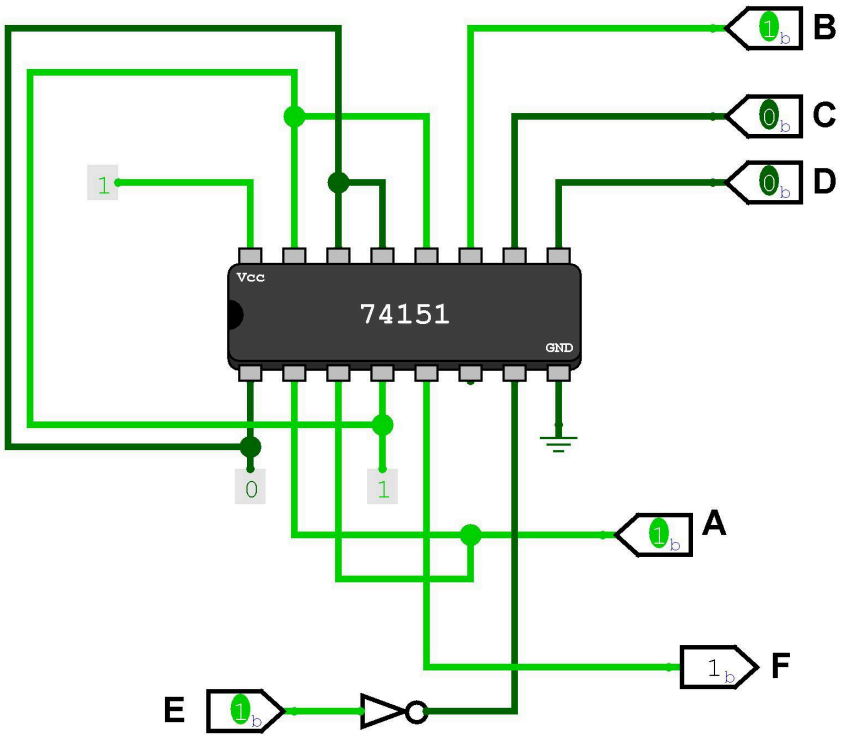


Fig. Simulation of Job 2(*Implementation of a boolean function using 8:1 MUX*)

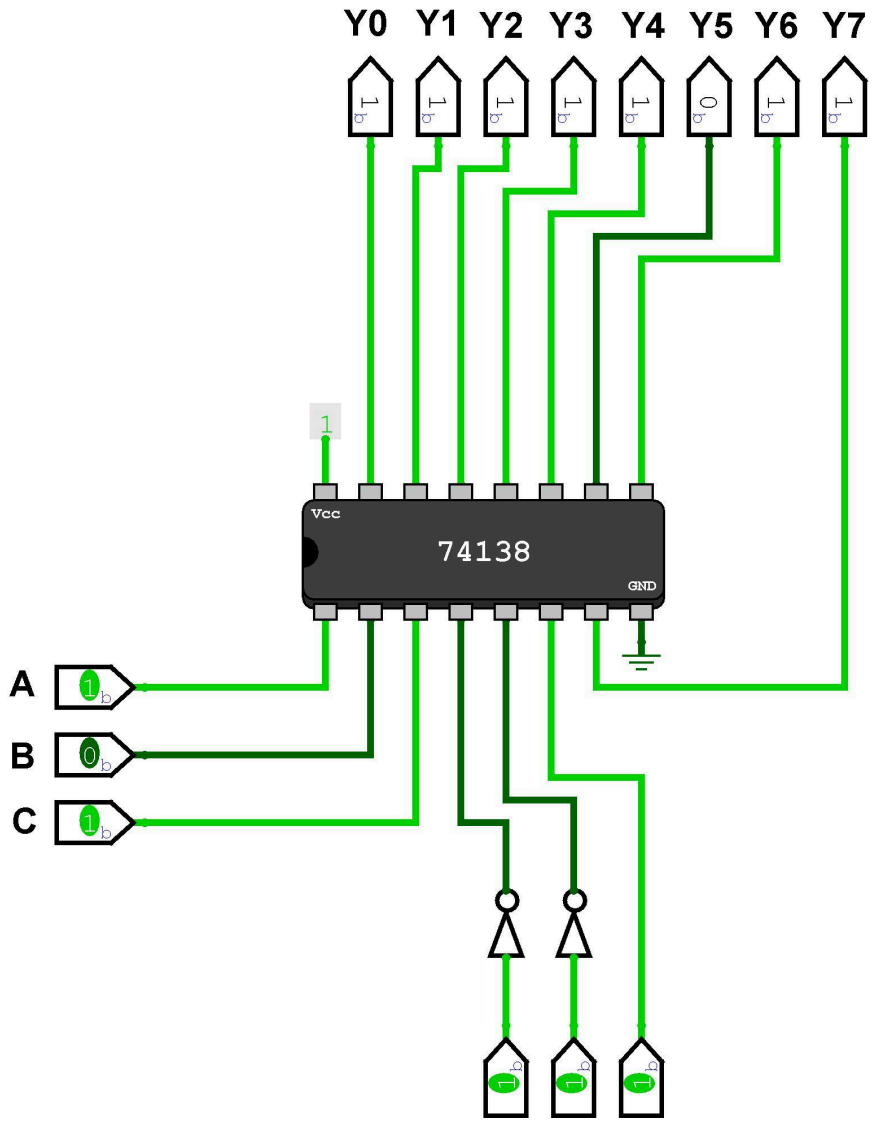


Fig. Simulation of Job 3(*Implementation of a 3-8 line decoder*).