North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	03
Experiment Title:	Universal Gates
Course Code:	**CSE231L**
Section:	**17**
Course Name:	**Digital Logic Design Lab**
Lab Group #:	02
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Objectives

- Get introduced to the concepts of Universal Gates
- Simulating basic logic gates and boolean functions using universal gates and verifying using their respective truth tables.

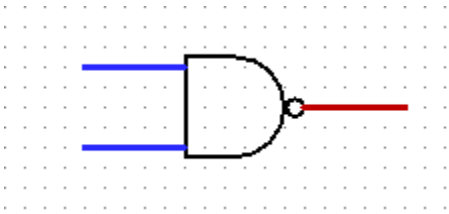
Equipment List

- Trainer Board
- 2 x IC 7400 Quadruple 2-input NAND gates
- 2 x IC 7402 Quadruple 2-input NOR gates

Theory

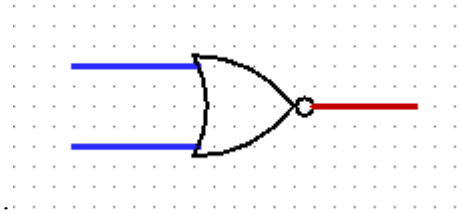
Universal Gates are defined as those gates that can be used to replicate the boolean operation of all the logic gates, using the gate itself only. Of all the available logic gates, only the NAND and NOR gates are found to be the Universal Gates. Therefore, with the use of only NAND or NOR gates, logic gates such as AND, OR, NOT, XNOR, XOR can be constructed.

NAND gate: A NAND gate accepts two inputs A and B, performing AND operation on them (AB) and the output is delivered by inverting (AB); $\overline{AB}$.

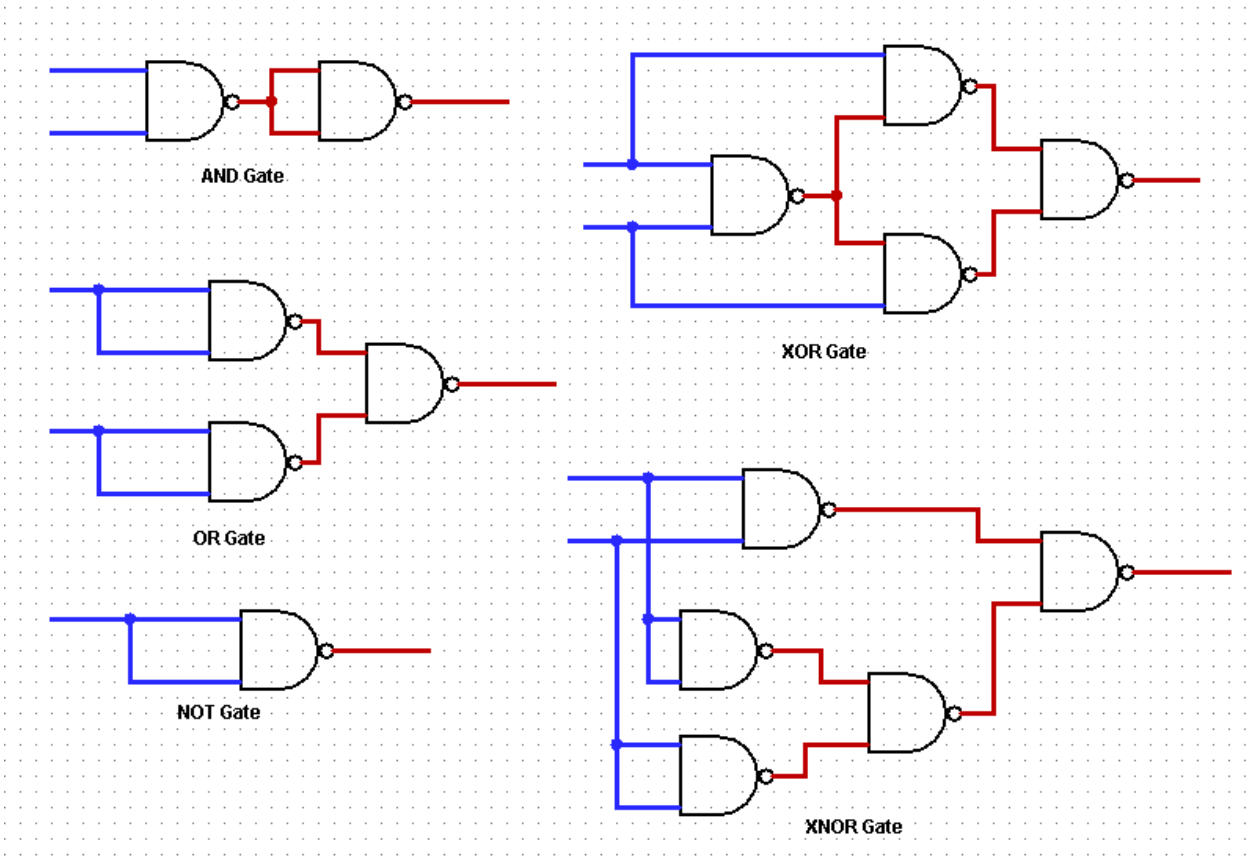


NAND gate

NOR gate: A NOR gate accepts two inputs A and B, performing OR operation on them (A + B) and the output is delivered by inverting (A + B); $\overline{A + B}$



NOR Gate



Logic Gates using NAND Gate

Circuit Diagram:

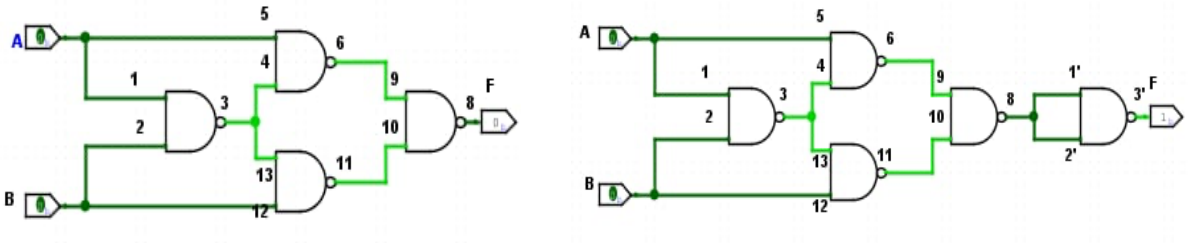
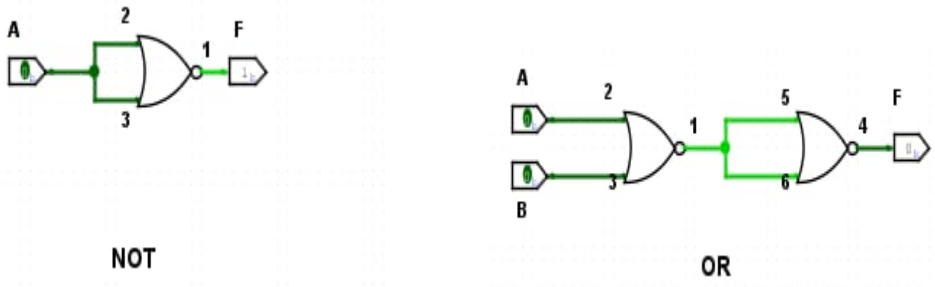


Figure D1:Implementation of XOR and XNOR using NAND gates



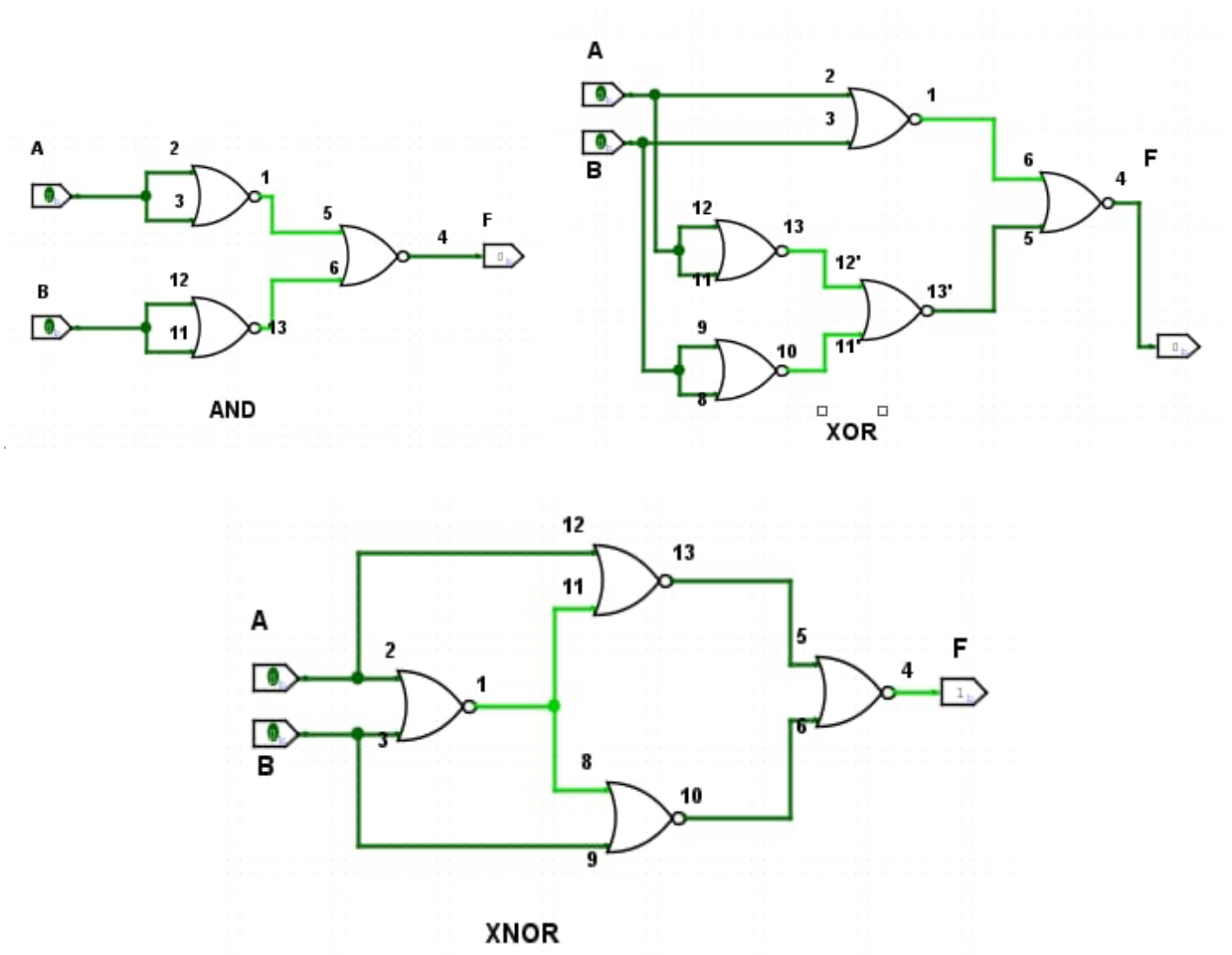


Figure D2:Implementation of NOT, AND, OR, XOR and XNOR using NOR gates.

Data Table & Equation

$A\,B\,C$	$I_1 = A\,C$	$I_2 = B\,\overline{C}$	$F = I_1 + I_2$
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	1	1
0 1 1	0	0	0
1 0 0	0	0	0
1 0 1	1	0	1
1 1 0	0	1	1
1 1 1	1	0	1

Table D1: Truth table of combinational circuit in Figure B2

Minterms and Maxterms

Input Reference	A B C	F	Max term
0	0 0 0	0	$A + B + C$
1	0 0 1	0	$A + B + \overline{C}$
2	0 1 0	1	$A + \overline{B} + C$
3	0 1 1	0	$A + \overline{B} + \overline{C}$
4	1 0 0	0	$\overline{A} + B + C$
5	1 0 1	1	$\overline{A} + B + \overline{C}$
6	1 1 0	1	$\overline{A} + \overline{B} + C$
7	1 1 1	1	$\overline{A} + \overline{B} + \overline{C}$

2nd Canonical Form	F = Π (0,1,3,4)	F = $(A + B + C)(A + B + \overline{C})(A + \overline{B} + \overline{C})(\overline{A} + B + C)$

Minimization

$\therefore F = (A + B + C)(A + B + \overline{C})(A + \overline{B} + \overline{C})(\overline{A} + B + C)$

$\therefore (A + B + C)(A + B + \overline{C})$
$= A + B$
$\therefore (A + \overline{B} + \overline{C})(\overline{A} + B + C)$
$= B\overline{C} + \overline{A}\,\overline{B} + AC$

$\therefore F = (A + B + C)(A + B + \overline{C})(A + \overline{B} + \overline{C})(\overline{A} + B + C)$
$\Rightarrow F = (A + B)(B\overline{C} + \overline{A}\,\overline{B} + AC)$
$\Rightarrow F = AB\overline{C} + A\overline{A}\,\overline{B} + AAC + BB\overline{C} + \overline{A}\,\overline{B}B + ABC$
$\Rightarrow F = AB\overline{C} + AC + B\overline{C} + ABC$
$\Rightarrow F = AC + B\overline{C}$

Discussion

The objective behind performing this experiment was to understand the functionality and importance of universal gates (NAND and NOR) in constructing any logic circuit. We have learned how universal gates can be used to implement all the basic logic gates (NOT, AND, OR) as well as Exclusive gates (XOR, XNOR). The circuits were implemented using these gates and verified through truth tables.

At first, we implemented all the basic logic gates and exclusive gates using only the NAND gates. Then, the process was repeated using the NOR gates. After this, a combinational circuit was constructed that consists of several basic logic gates, using NAND gates. By observing the output, we found that our NAND-only combinational circuit successfully replicated the output without compromising any functionality. We further confirmed this equivalence using the truth table and simulating the circuit on Logisim. The experimental results aligned with the expected values and simulated results, demonstrating that the universal gates can indeed replicate the functions of other gates.

In conclusion, this experiment reinforced the concept of universal gates that these gates are capable of constructing any other logic gate or combinational circuits. No significant problems were encountered while performing the experiment. However, careful pin mapping and circuit design were crucial to ensure correct connections and outputs. Proper verification using truth tables helped in identifying and rectifying any minor wiring issues.

Simulation:

Simulation of the logic circuit in Fig B.2 using only NAND gates for the input ABC = 000

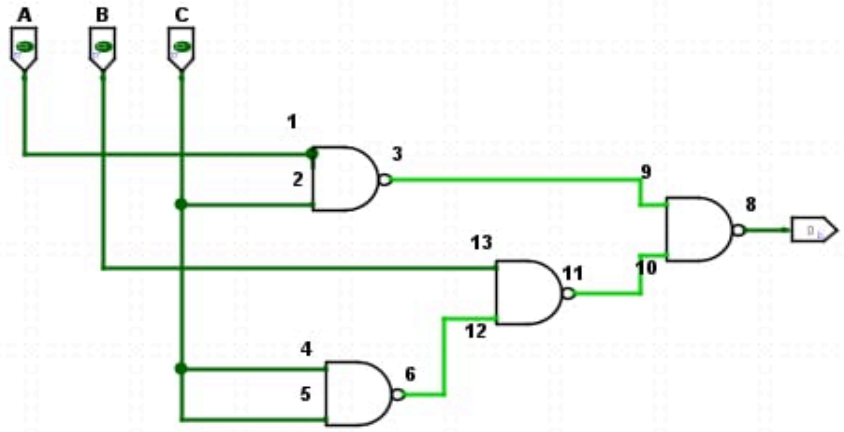
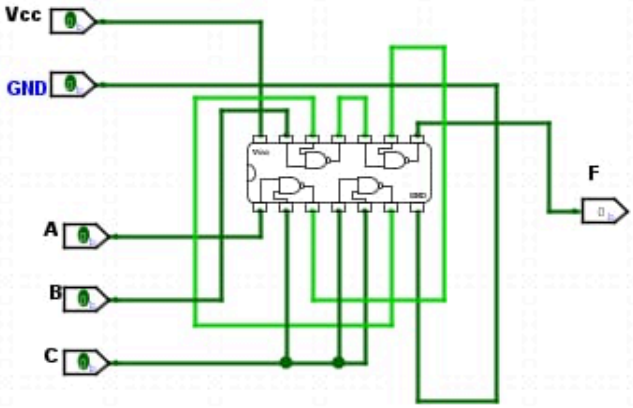


Figure D3: Universal(NAND) gate implementation of the circuit of figure B2



Simulation of the logic circuit in Fig B.2 using only NOR gates for the input ABC = 000

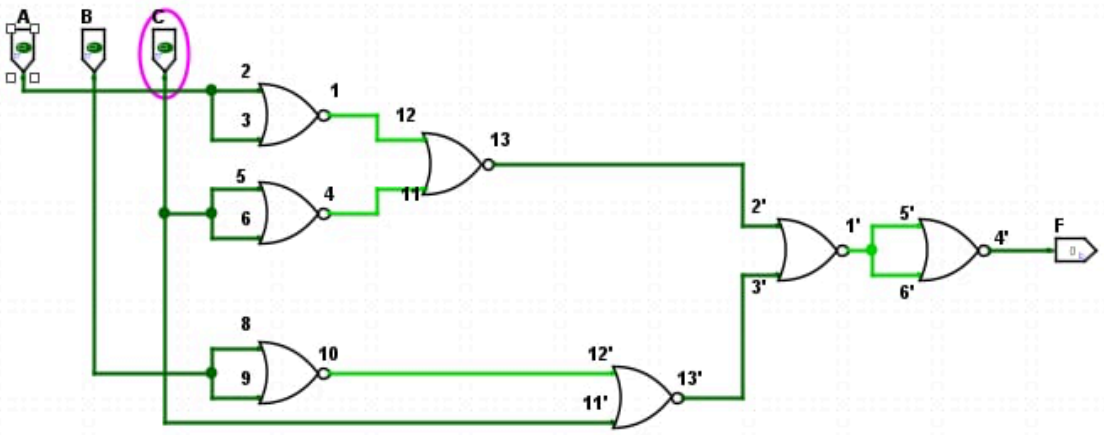


Figure D3: Universal(NOR) gate implementation of the circuit of figure B2