North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	02
Experiment Title:	Combinational Logic Design
Course Code:	**CSE231L**
Section:	**17**
Course Name:	**Digital Logic Design Lab**
Lab Group #:	02
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Objectives

- Familiarize with the analysis of combinational logic networks.
- Learn the implementation of networks using the two canonical forms.
- Devise combinational circuits using universal logic.
- Acquaint with basic binary arithmetic circuits –the half and full adders.

Equipment List

- Trainer Board
- 1 x IC 7411 Triple 3-input AND gates
- 1 x IC 7432 Quadruple 2-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)

Theory

Combinational Logic Design Analysis: Combinational logic circuits have outputs that depend only on the current inputs, without memory or feedback elements.
Steps to Analyze:
1. Identify the inputs and outputs.
2. Derive the truth table that defines the relationship between inputs and outputs.
3. Derive the Canonical Forms of the Boolean Expression.
4. Implement the simplified function using basic logic gates.

Canonical Forms: Any Boolean function expressed as a sum of minterms or as a product of maxterms is said to be in its canonical form. To convert from one canonical form to another, interchange the symbols Σ and Π then list the index numbers excluded from the original form. To convert from one canonical form to its dual, interchange the symbols Σ and Π, and list the index numbers from
the original form
Sum of Products (SOP): A Boolean function expressed as a sum (OR) of minterms.
Product of Sums (POS): A Boolean function expressed as a product (AND) of max terms.

Steps to Convert:
Derive the truth table.
1. For SOP, write the min terms for each output 1.
2. For POS, write the max terms for each output 0.

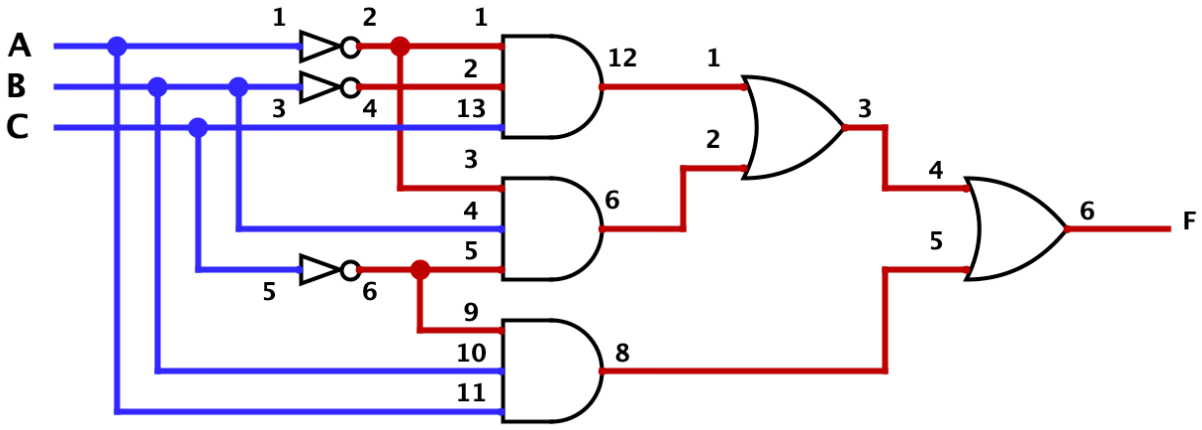
Minterm: A minterm is a product (AND) term in a Boolean expression where each variable appears exactly once. Each literal may be with or without the bar i.e. complimented. It corresponds to a row in the truth table where the output is 1.

Maxterm: A maxterm is a sum (OR) term where each variable appears once. Each literal may be with or without the bar i.e. complimented. It corresponds to a row in the truth table where the output is 0.

De Morgan's theorem: The complement of the product of all the terms is equal to the sum of the complement of each term or the complement of the sum of all terms is equal to the product of the complement of each term.

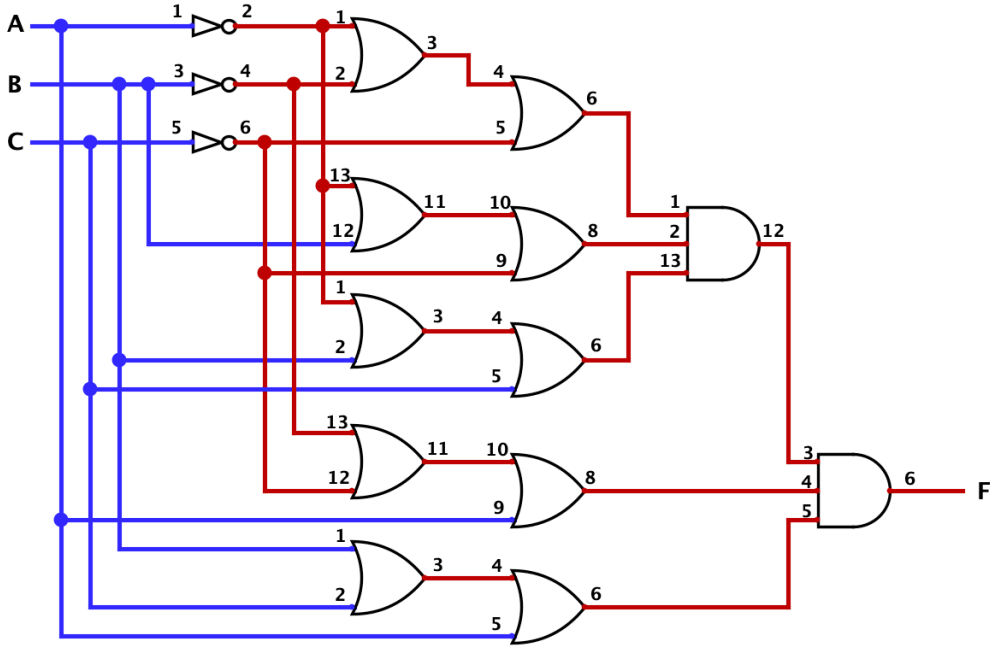
$\overline{A \,.\, B} = \overline{A} + \overline{B}$ $\quad$ $\overline{A + B} = \overline{A} \,.\, \overline{B}$

Circuit Diagram



$F = \overline{A}\,\overline{B}\,C + \overline{A}\,B\overline{C} + A\,B\,\overline{C}$

Figure: C.2 1st Canonical Form



F =

$(A + B + C)(A + \overline{B} + \overline{C})(\overline{A} + B + C)(\overline{A} + B + \overline{C})(\overline{A} + \overline{B} + \overline{C})$

Figure: C.2 2nd Canonical Form

Data Table & Equation

Input Reference	A B C	F	Min term	Max term
0	0 0 0	0	$\overline{A}\,\overline{B}\,\overline{C}$	$A + B + C$
1	0 0 1	1	$\overline{A}\,\overline{B}\,C$	$A + B + \overline{C}$
2	0 1 0	1	$\overline{A}\,B\overline{C}$	$A + \overline{B} + C$
3	0 1 1	0	$\overline{A}\,B\,C$	$A + \overline{B} + \overline{C}$
4	1 0 0	0	$A\,\overline{B}\,\overline{C}$	$\overline{A} + B + C$
5	1 0 1	0	$A\,\overline{B}\,C$	$\overline{A} + B + \overline{C}$
6	1 1 0	1	$A\,B\,\overline{C}$	$\overline{A} + \overline{B} + C$
7	1 1 1	0	$A\,B\,C$	$\overline{A} + \overline{B} + \overline{C}$

Table C.1

	Shorthand Notation	Function
1st Canonical Form	F = Σ (1,2,6) in	F = $\overline{A}\,\overline{B}\,C + \overline{A}\,B\overline{C} + A\,B\,\overline{C}$
2nd Canonical Form	F = Π (0,3,4,5,7)	F = $(A + B + C)(A + \overline{B} + \overline{C})(\overline{A} + B + C)$ $(\overline{A} + B + \overline{C})(\overline{A} + \overline{B} + \overline{C})$

Table C.2

Discussion

For this experiment “Combinational Logic Design,” our goal was to apply the theoretical understanding of minterms, maxterms, and canonical forms that was acquired from lessons. Its primary purpose is to make a Boolean function with the minimum number of logic gates.

We first converted the given logic function into the Sum of Products (SOP) form using minterms and the Product of Sums(POS) using maxterms, respectively. For implementing the circuit, we have used integrated circuits that included the 7411 Triple 3-input AND gates, 7432 Quadruple 2-input OR gates and 7404 Hex Inverters or NOT gates on the breadboard. In order to prevent wiring mistakes, we first simulated the logic in Logisim.

We organized the circuit into sections based on each integrated circuit (IC), which helped us avoid miswiring. By checking the input and output at each stage, we made sure everything was

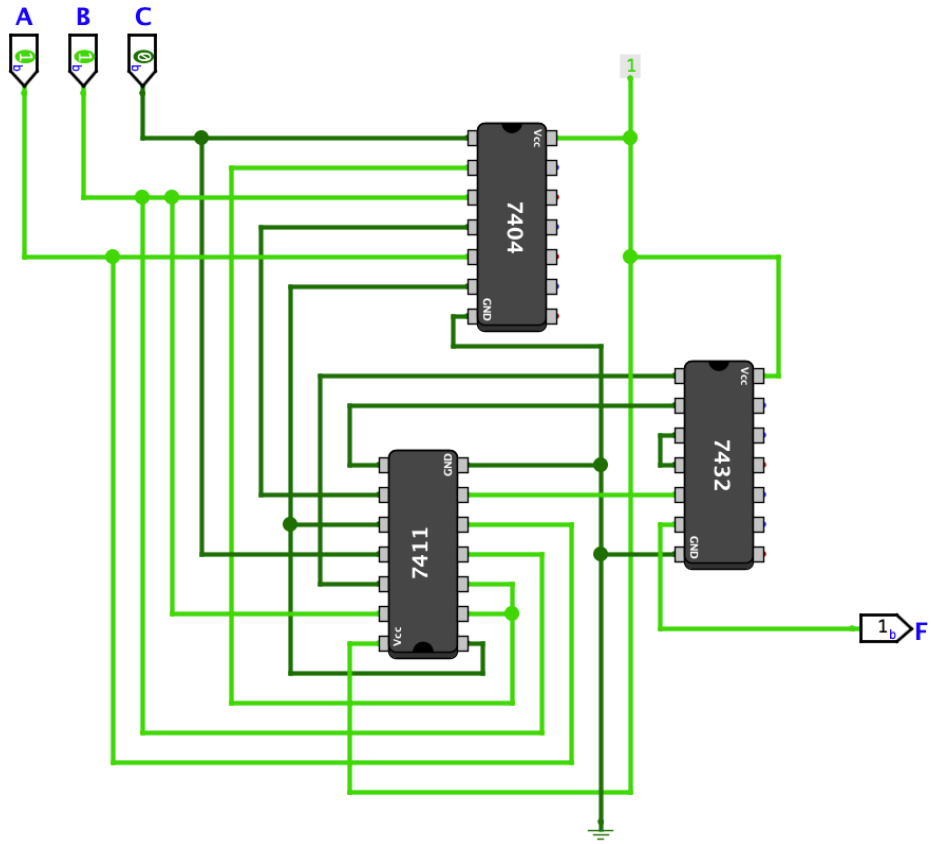
connected correctly before moving on. The final circuit came together smoothly, with all team members playing a role in the design and testing.

When we reviewed the results, we found that our circuit's outputs were the same as the values from the truth table. There were no incorrect output signals, which showed that our implementation was correct. The successful operation of the circuit confirmed the theoretical principles of combinational logic.

Summarizing, it is possible to state that this experiment was useful for gaining practical experience in using the concepts of canonical forms and basic logic gates. The theoretical design and the implemented circuit were on par in every respect, thus proving the efficiency of the design we have made on paper.

Logisim Simulation

Simulation of the logic circuit in Fig C.2 1st Canonical Form for the input ABC = 110



Simulation of the logic circuit in Fig C.2 2nd Canonical Form for the input ABC = 110