North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No: 7

Experiment Title: Introduction to Flip-flop and Registers

Course Code: **CSE231L**

Section: **17**

Course Name: **Digital Logic Design Lab**

Lab Group #: 02

Written By:

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Objectives:

- Learn about the concept of states in digital logic and how Flip-Flop circuits can be used to store state information.

- Understand the internal logic of J-K Flip-Flops and implement one using basic logic gates.

- Understand the relationship between J-K, T and D Flip-Flops and observe the characteristics of all three.

- Implement a shift register using D Flip-Flops and analyze its operation.

Equipment List:

1.Trainer Board

2. 1 x IC 7402 2-input NOR gates + 1 x IC 7411

3.input AND gates

4. 1 x IC 7404 Hex Inverter (NOT gates)

5.2 x IC 7474 (D Flip-Flop)

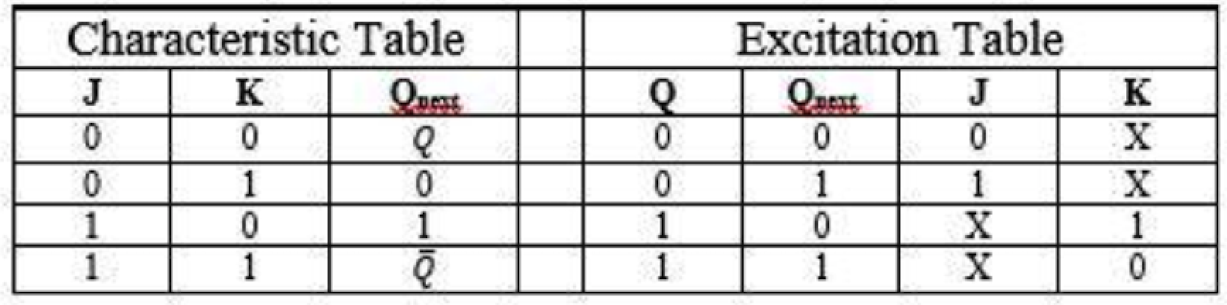
Theory:

Flip-Flops: Digital logic circuits can be divided into two types: combinational logic, whose output signals are dependent only on its present input signals, and sequential logic, whose outputs are a function of both the current inputs and the past history of inputs. In sequential logic, information from past inputs is stored in electronic memory elements, such as flip-flops and latches. The stored contents of these memory elements, at a given point in time, is collectively referred to as the circuit's "state" and contains all the information about the past to which the circuit has access.

A flip-flop is a binary storage device that has two stable states and is capable of storing one bit of information.In a stable state, the output of a flip-flop is either 0 or 1. The output can only change when a clock pulse is supplied to the flip-flop. The value that is stored in a flip-flop when the clock pulse occurs is determined by the inputs to the flip-flop at that time or the values presently stored in the flip-flop (or both). The new value is stored (i.e., the flip-flop is updated) when a pulse of the clock signal occurs.

JK, D ("Data" or "Delay") and T ("Toggle') are three common types of flip-flops used in digital logic circuits.In case of the JK flip-flop (J=Set, K-Reset), the combination J = 1, K = 0 is a command to set the flip-flop (i.e., make the output, Q = 1); the combination J = 0, K = 1 is a command to reset the flip-flop (Q = 0); and the combination J = K = 1 is a command to toggle the flip-flop, ie., change its output to the logical complement of its current value. Setting J = K = 0 maintains the current state.

Since the output of a flip-flop may depend on more than its current inputs, a standard truth table is not enough to summarize its operations. Generally, we use two types of tables to express the behavior of flip-flops. The first one is a State Transition Table or a Characteristic Table which shows the state the flip-flop will move to, based on the current state and other inputs. It's similar to a truth table. The second one, called the Excitation Table, shows the minimum inputs that are necessary to generate a particular next state (in other words, to "excite" it to the next state) when the current state is known. Table B.l shows the Characteristic Table and Excitation table for the JK flip-flop.



Characteristic Table				Excitation Table			
J	K	Q_{next}		Q	Q_{next}	J	K
0	0	Q		0	0	0	X
0	1	0		0	1	1	X
1	0	1		1	0	X	1
1	1	$\bar{Q}$		1	1	X	0

A register that is capable of shifting its binary information either to its right or its left is called a shift register.The logical configuration of a shift register consists of a chain of flip-flops connected in cascade, with the output of one flip flop connected to the input of the next flip-flop. All flip-flops receive a common pulse which causes the shift from one stage to the next.

Circuit Diagram:

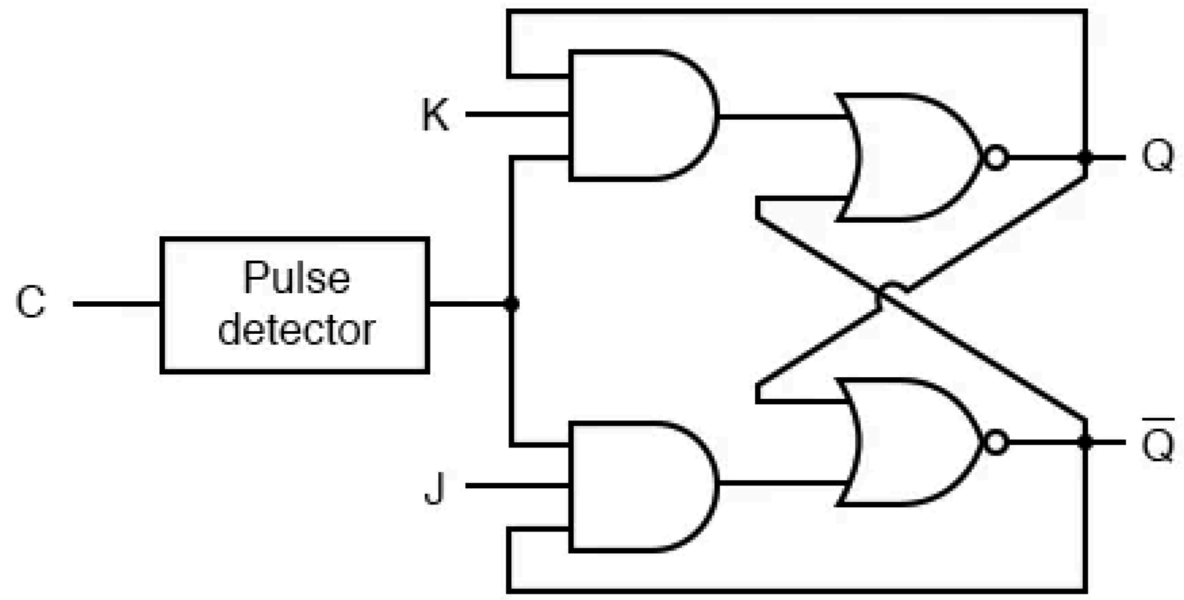


Figure F.1: JK Flip-Flop implemented using AND & NOR gates.

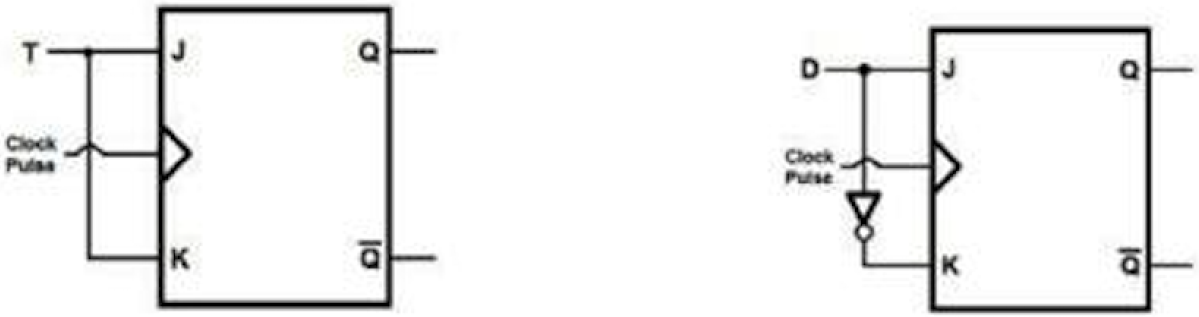


Figure F.2: Tand D flip-flop constructed using JK flip-flop.

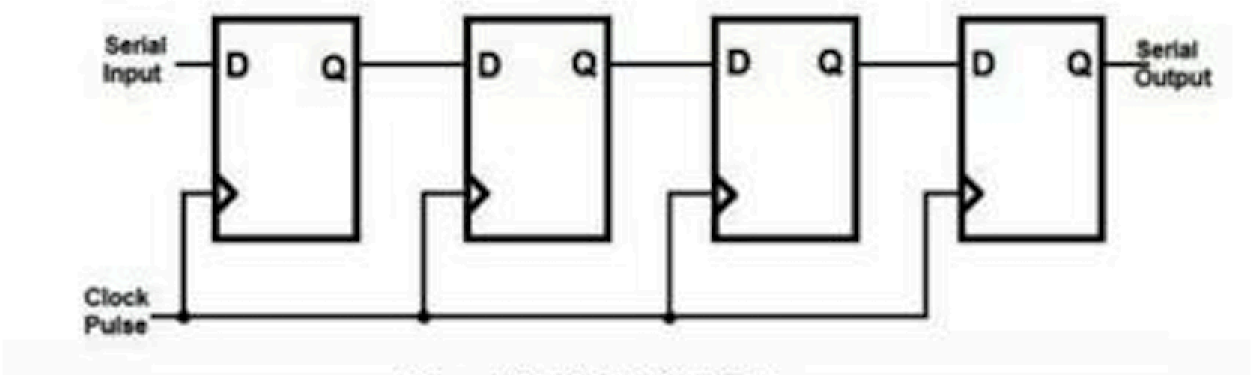


Figure F.3: Right Shift Register.

Data Table & Equation:

J	K	Q(n)	Q'(n)
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	1	0
1	0	1	0
1	1	1	0

Table-1

Table-2.1

T	Q
0	No Change
1	Toggle

D	Q
0	0
1	1

Table-2.2

States	Input	Output
Initial State	X	XXXX
T1	1	1XXX
T2	0	01XX
T3	1	101X
T4	0	0101

Table-3

Question/Answer

Discussion

To build the circuits correctly, we first tested them using Logisim. We carefully followed the wire and pin connections from the simulation to create the physical circuits. If any issues arose, we used the simulation results to help troubleshoot and resolve them. Initially, we didn't achieve the desired output due to some issues with the wire connections. These connection problems caused unexpected outputs, but after several attempts and careful adjustments, we were able to obtain the correct results.

This experiment taught us a lot about the characteristics and behavior of JK, T, and D flip-flops. By observing their operation, we recognized the importance of these flip-flops in digital logic. Additionally, we constructed a JK flip-flop using basic logic gates. We now understand the fundamental relationships between these three types of flip-flops and their differences. This experiment was distinct from others, and it was enjoyable to build. After completing these experiments, we can now quickly build synchronous sequential circuits. We successfully completed all the experiments, achieving the desired outcomes in the end.

Data Sheet

Logisim Simulation

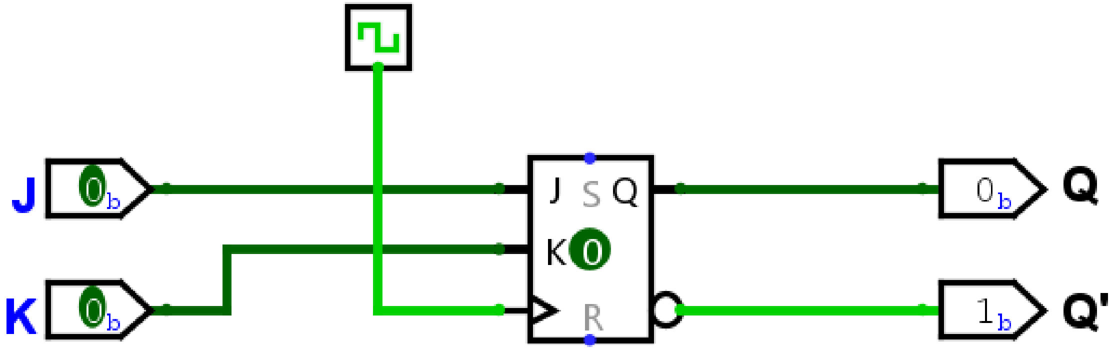


Fig : Implementation of JK flipflop

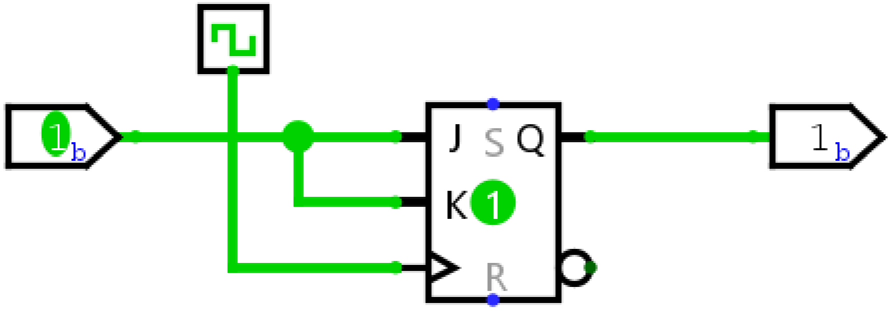


Fig: Implementation T flip flop of using JK flip flop

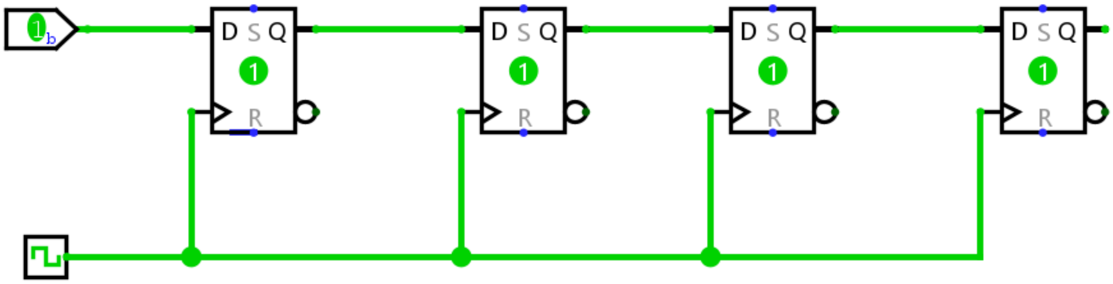


Fig: Shift register

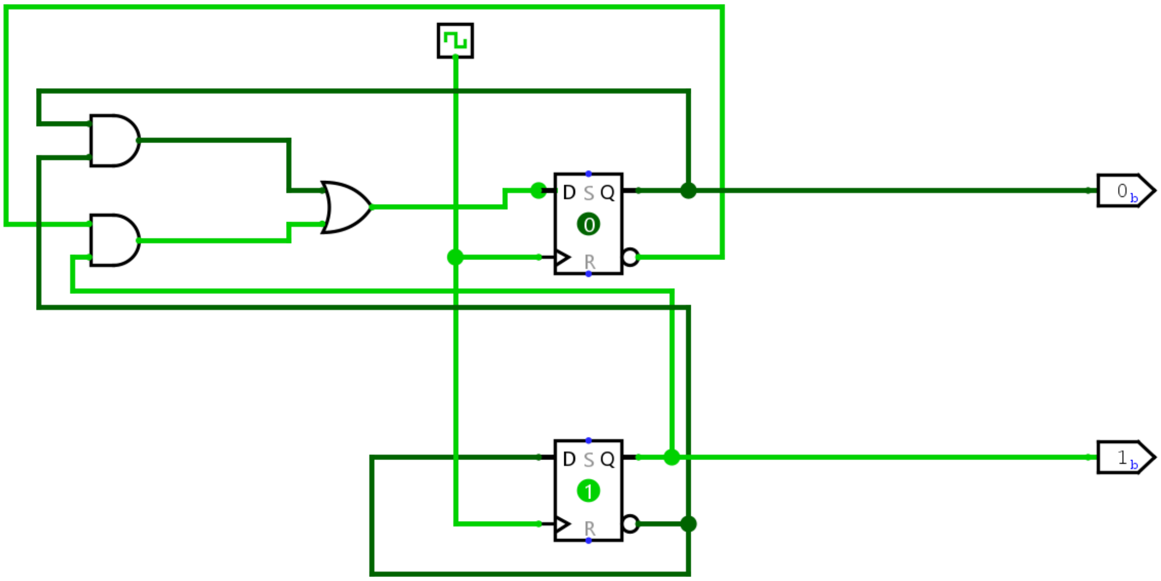


Fig: 2 bit counter using D flip flop

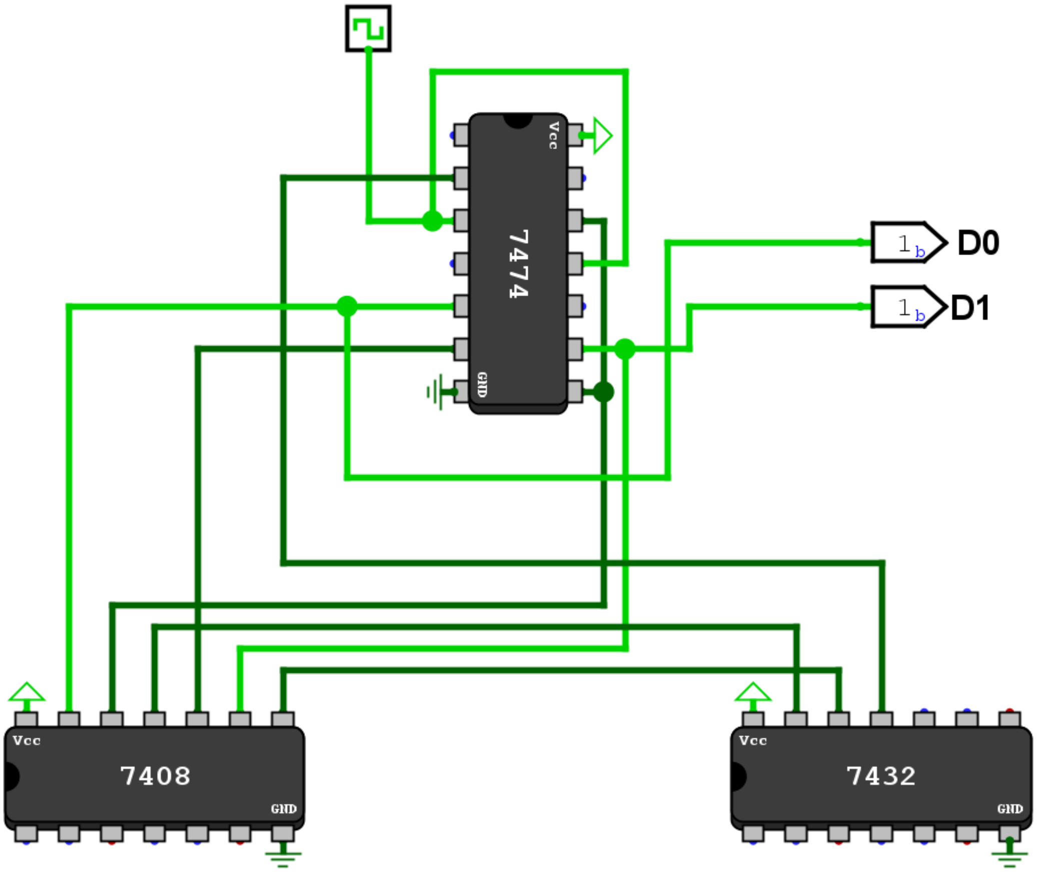


Fig: 2 bit counter using D flip flop