1. A computer system has an MM consisting of 16 MB 32-bit words. It also has an 8 KB cache. Assume that the computer uses a byte-addressable mechanism. Determine the number of bits in each field of the address in each of the following organizations:

    a. Direct mapping with block size of one word.
    b. Direct mapping with a block size of eight words.
    c. Associative mapping with a block size of eight words.
    d. Set-associative mapping with a set size of four block and a block size of one word.

2. Assuming a cache of 4K blocks, a four-word block size, and a 32-bit address, find the total number of sets and the total number of tag bits for caches that are direct mapped, two-way and four-way set associative, and fully associative.

3. Intel's Pentium 4 processor uses a two-level cache organization. Cache L1 represents an 8 KB data cache. This is a four-way set-associative. The block size is 64 bytes. Consider the following example (tailored after the L1 Pentium cache).
    - Cache organization: Set-associative
    - Main Memory size: 16 MB
    - Cache L1 size: 8 KB
    - Number of blocks per set: 4
    - CPU addressing: Byte addressable

    Cache L2 is organized as an eight-way set-associative cache having a 256 KB total size and 128-byte block size.
    Determine the number of bits in each field of the address of each cache.

4. The PowerPC cache is divided into data and instruction caches, called Harvard Organization. Both the instruction and the data caches are organized as 16 KB four-way set-associative. The following table summarizes the PowerPC 604 cache basic characteristics.
    - Cache organization: Set-associative.
    - Block size: 32 bytes.
    - Main memory size: 4 GB (M = 128 Mega blocks).
    - Cache size 16 KB (N = 512 blocks).
    - Number of blocks per set: 4.
    - Number of cache sets (S) 128 sets.

    Determine the number of bits in each field of the address.

5. A magnetic HDD has 16 heads, 684 cylinders, 18 sectors/track. Determine the capacity.