CMOS VLSI Design
MOS Transistor and Logic

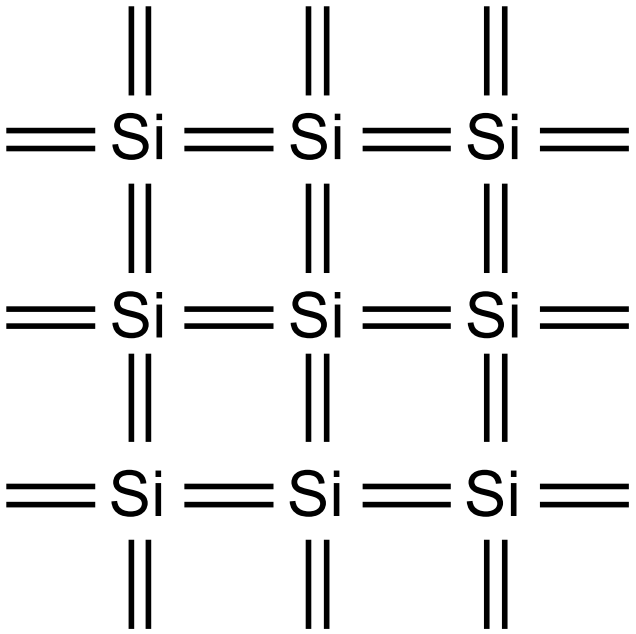
Introduction

- Integrated circuits: many transistors on one chip.
- *Very Large Scale Integration* (VLSI): very many

  >10K gates in a chip
- *Complementary Metal Oxide Semiconductor* (CMOS)
  - Fast, cheap, low power transistors
- Today: How to build your own simple CMOS chip
  - CMOS transistors
  - Building logic gates from transistors
  - Transistor layout and fabrication
- Rest of the course: How to build a good CMOS chip

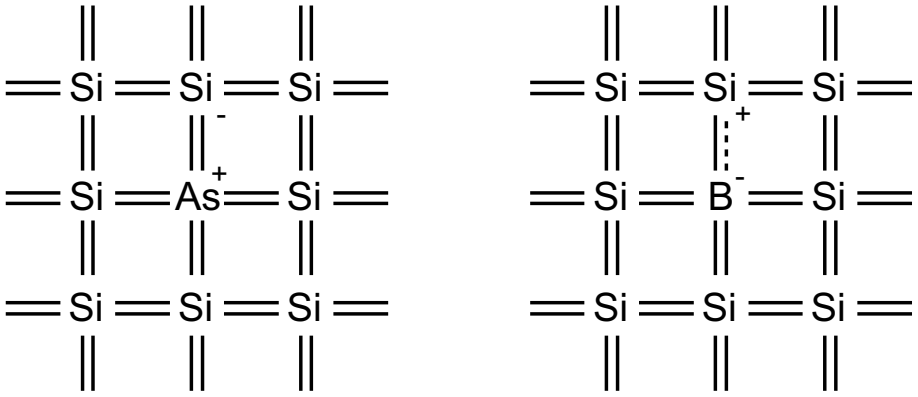
Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors



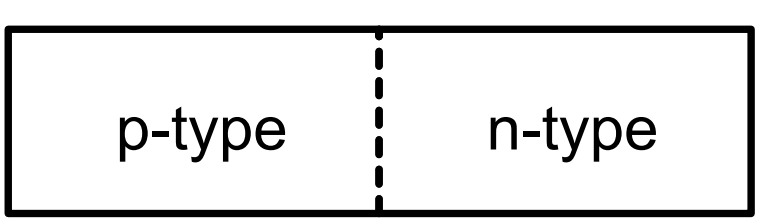
Dopants

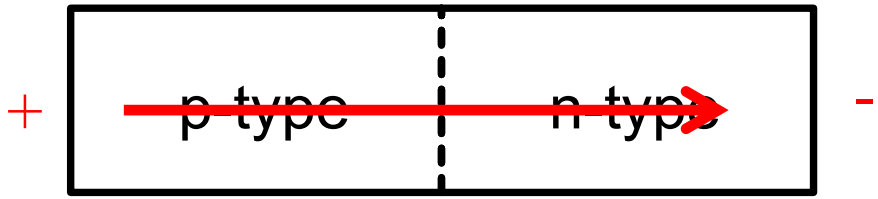
- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



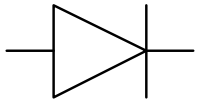
p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
- Current flows only in one direction

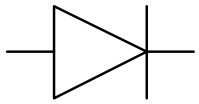




anode cathode

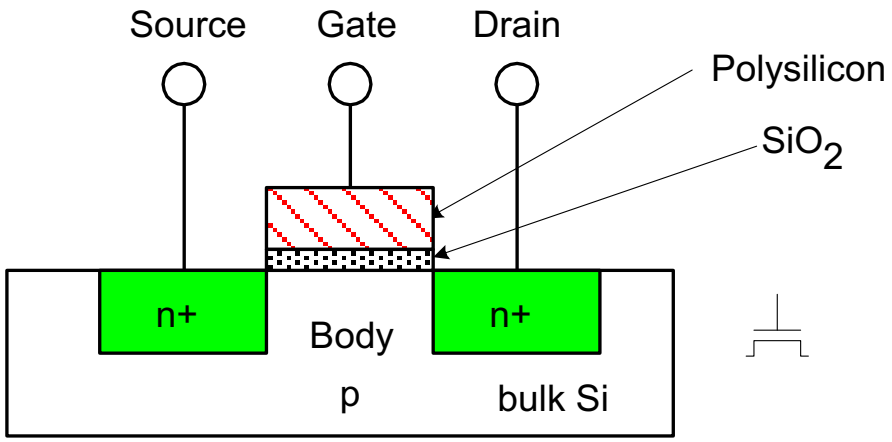


anode cathode



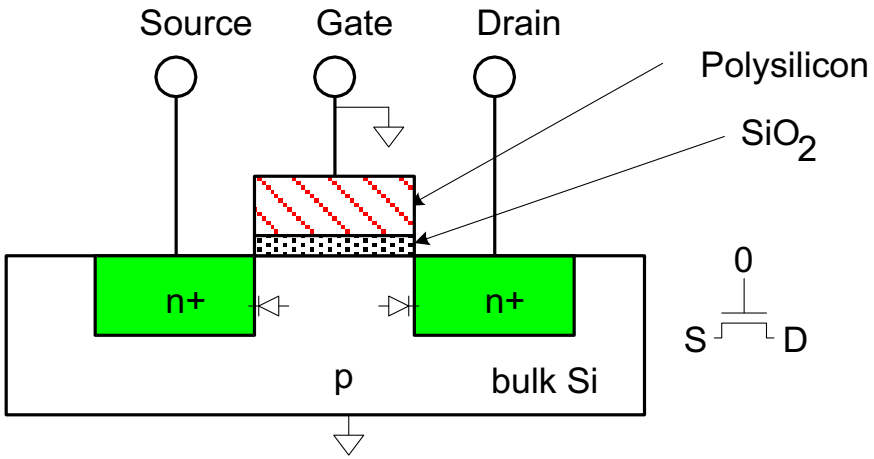
nMOS Transistor

- Four terminals: gate, source, drain, body
- Source and drain: n type
  - n+ mean it is heavily doped
- Body: p type
- Gate is used to control the transistor



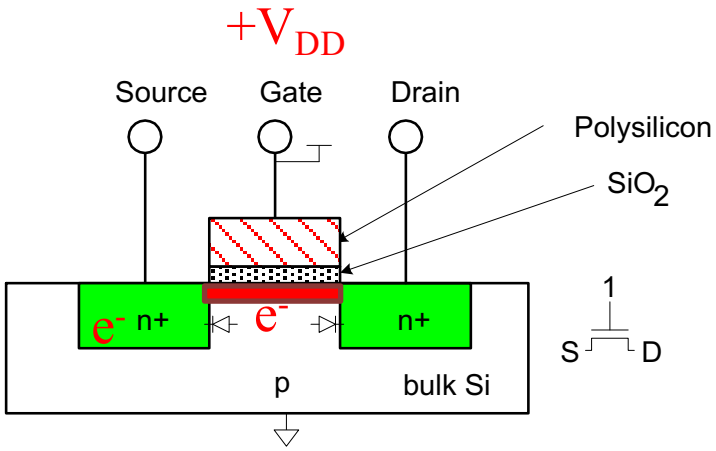
nMOS Operation (V_G=0V)

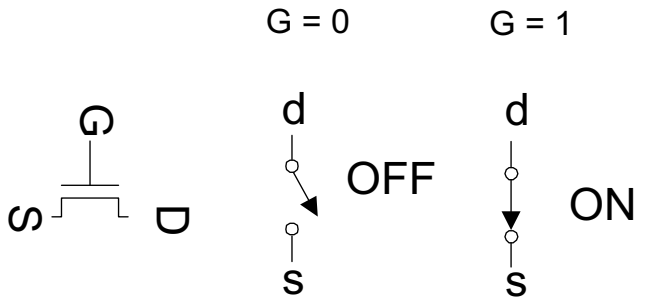
- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage (V_G=0V):
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



nMOS Operation (V_G=VDD)

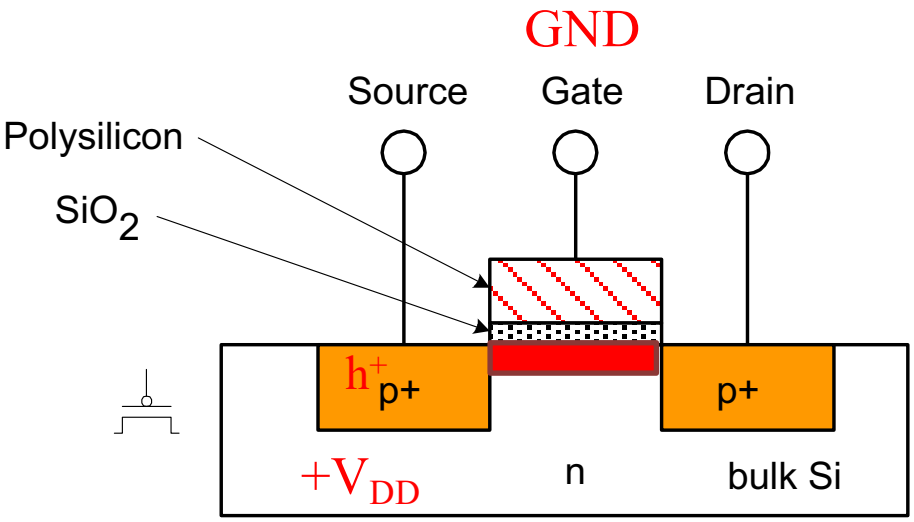
- When the gate is at a high voltage (V_G=V_{DD}):
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON

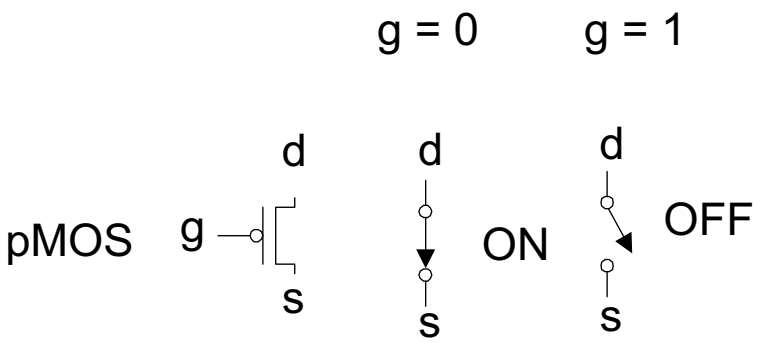




pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



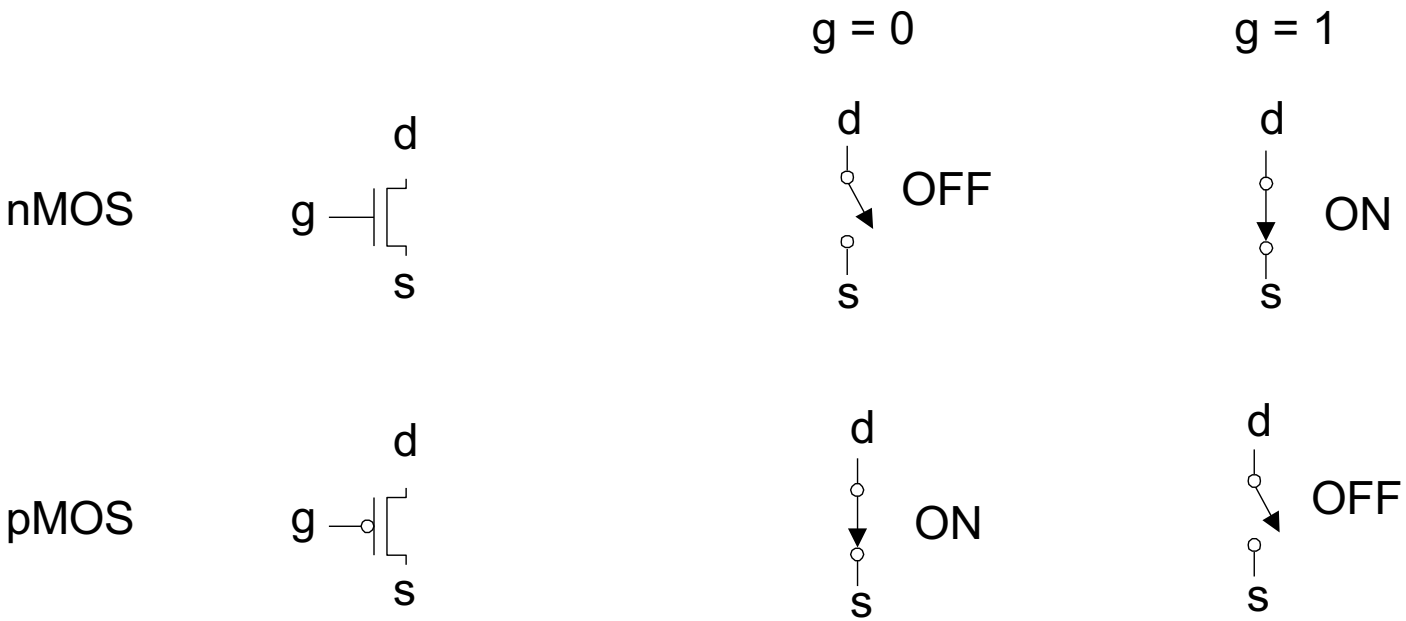


Power Supply Voltage

- GND = 0 V
- In 1980's, V_{DD} = 5V
- V_{DD} has decreased in modern processes
  - High V_{DD} would damage modern tiny transistors
  - Lower V_{DD} saves power
- V_{DD} = 3.3, 2.5, 1.8, 1.5, 1.2, 1.0, …

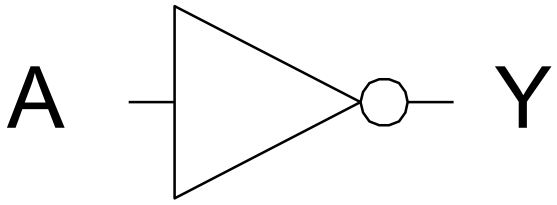
Summary: Transistors as Switches

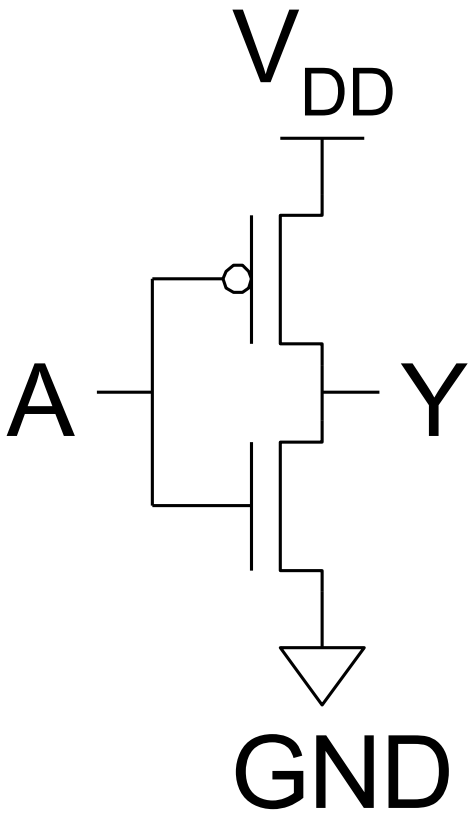
- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain



CMOS Inverter

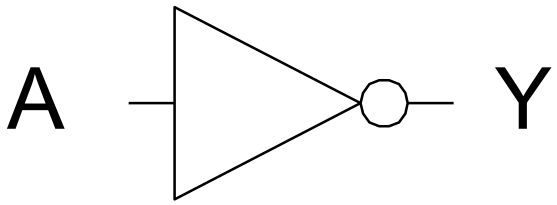
A	Y
0	
1	

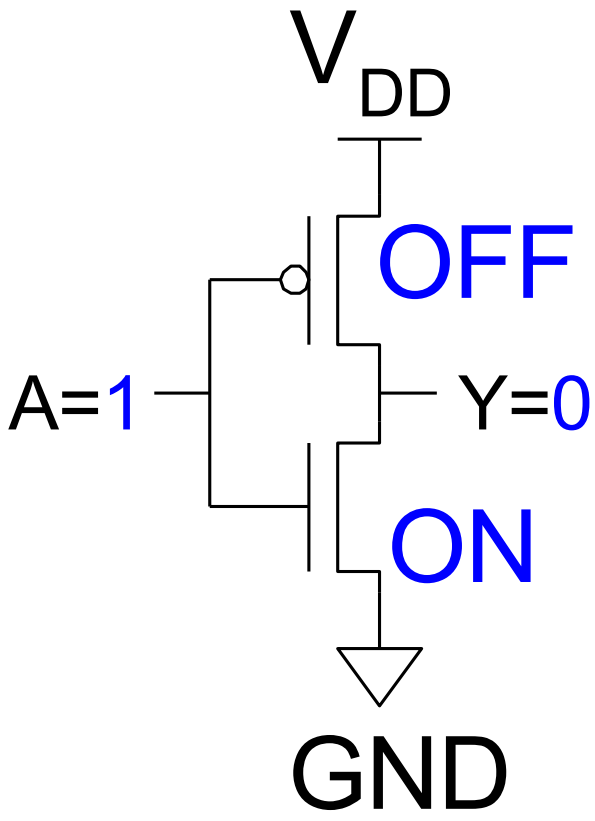




CMOS Inverter

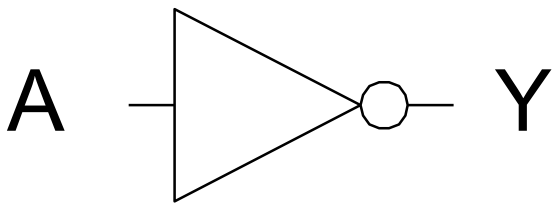
A	Y
0	
1	**0**

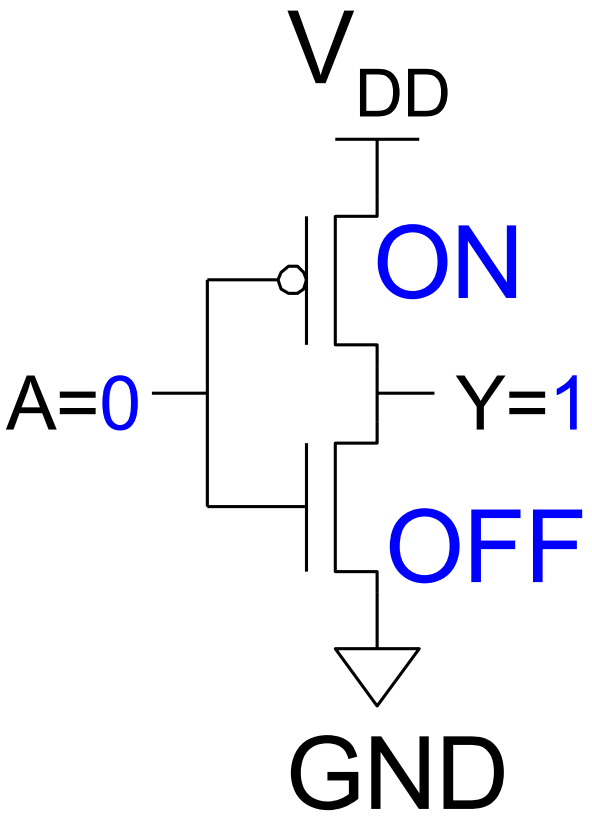




CMOS Inverter

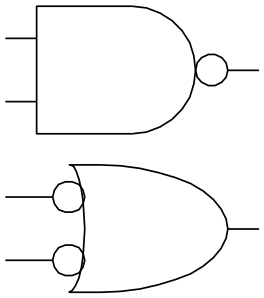
A	Y
0	**1**
1	0

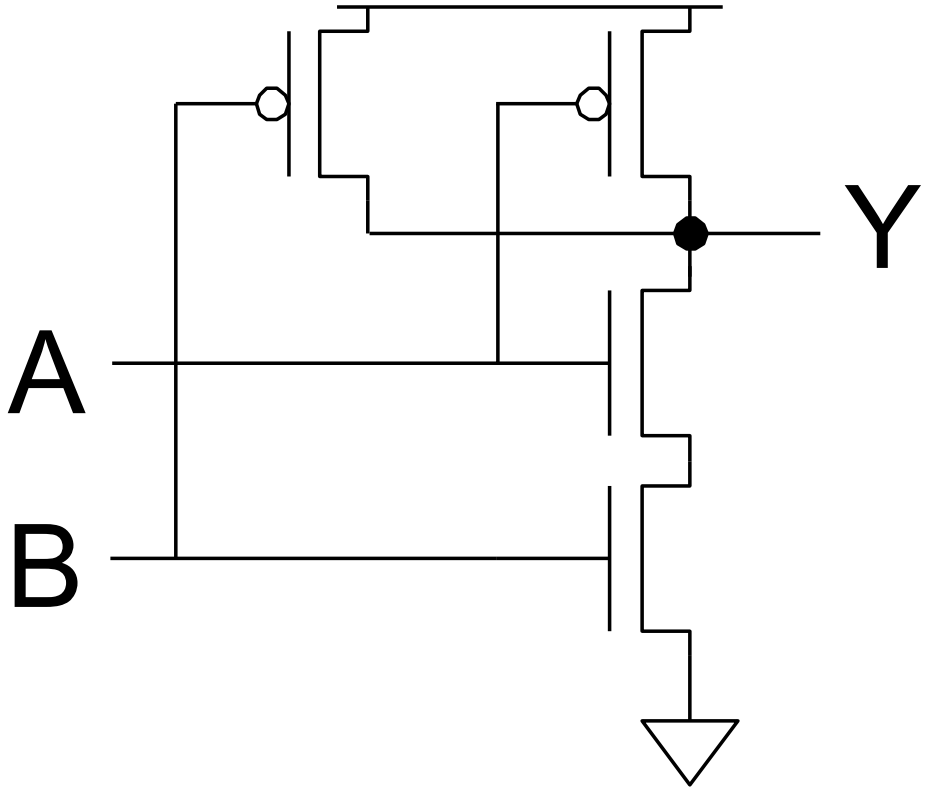




CMOS NAND Gate

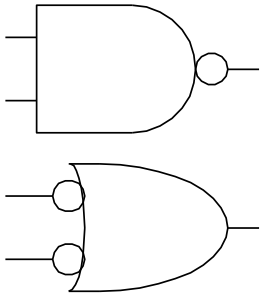
A	B	Y
0	0	
0	1	
1	0	
1	1	

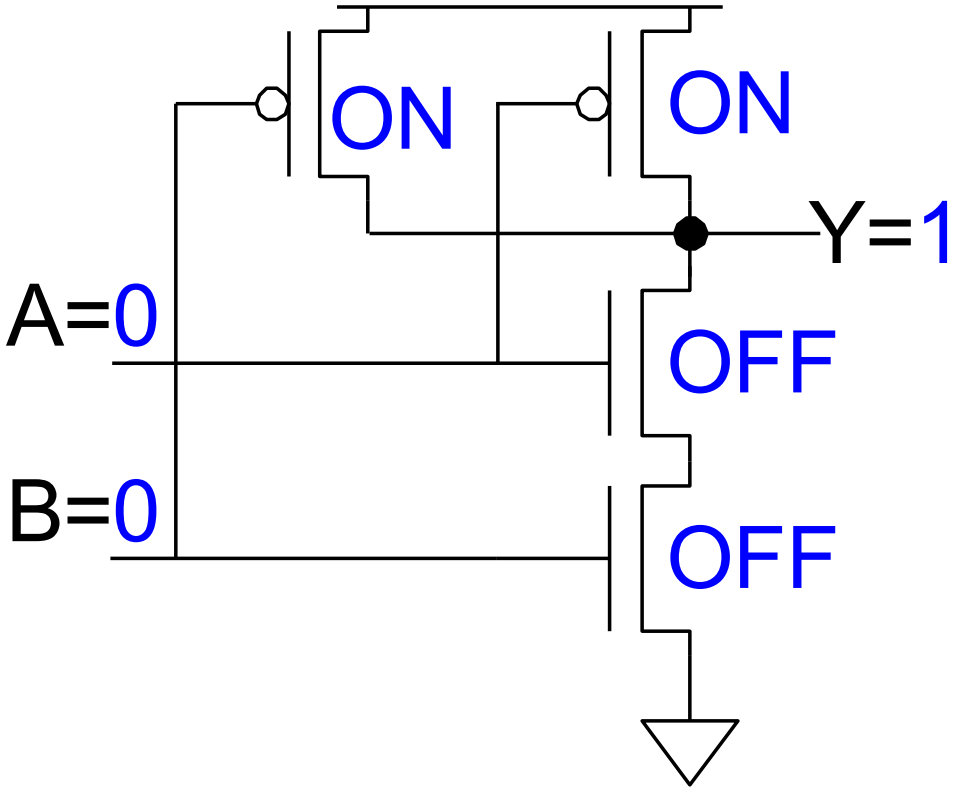




CMOS NAND Gate

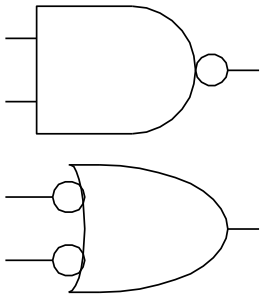
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

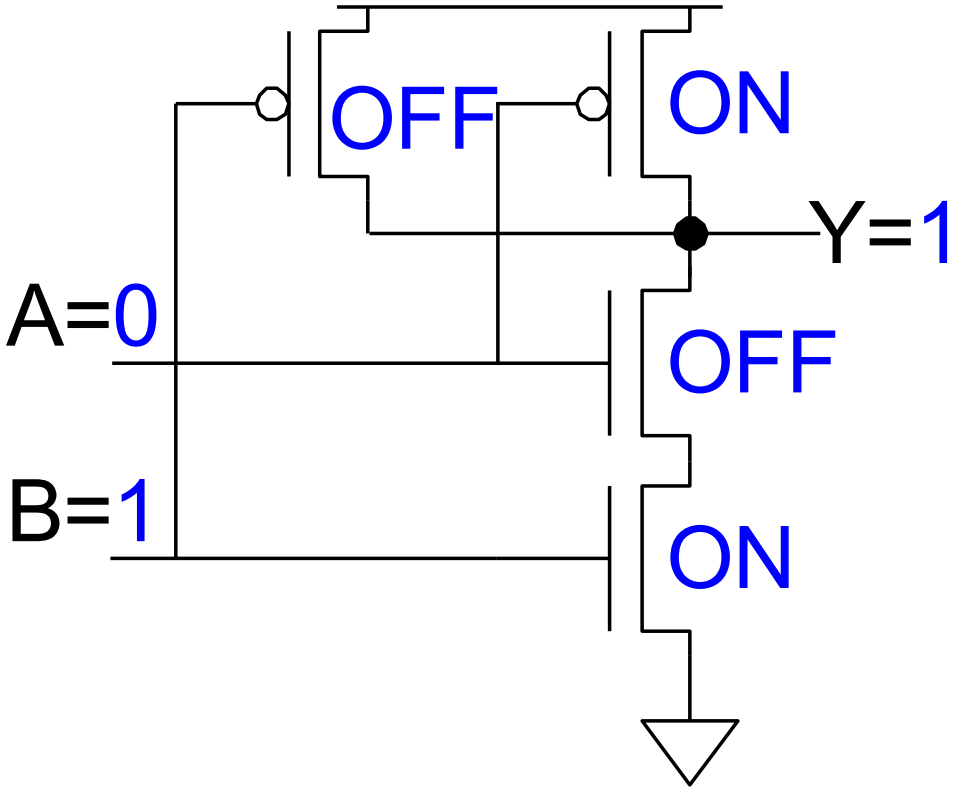




CMOS NAND Gate

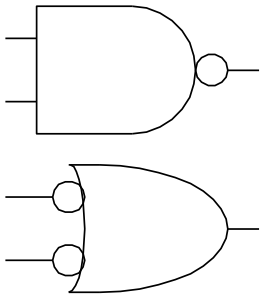
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

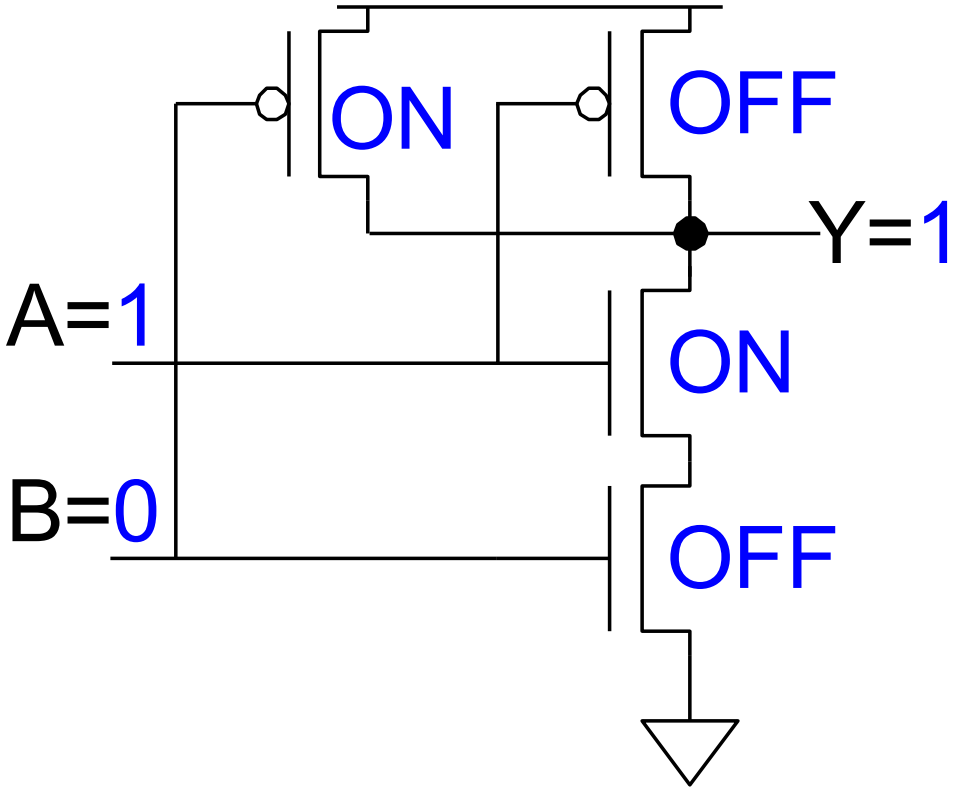




CMOS NAND Gate

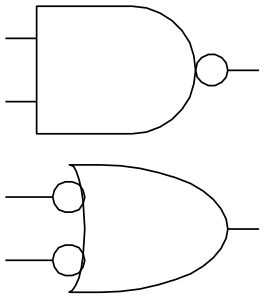
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

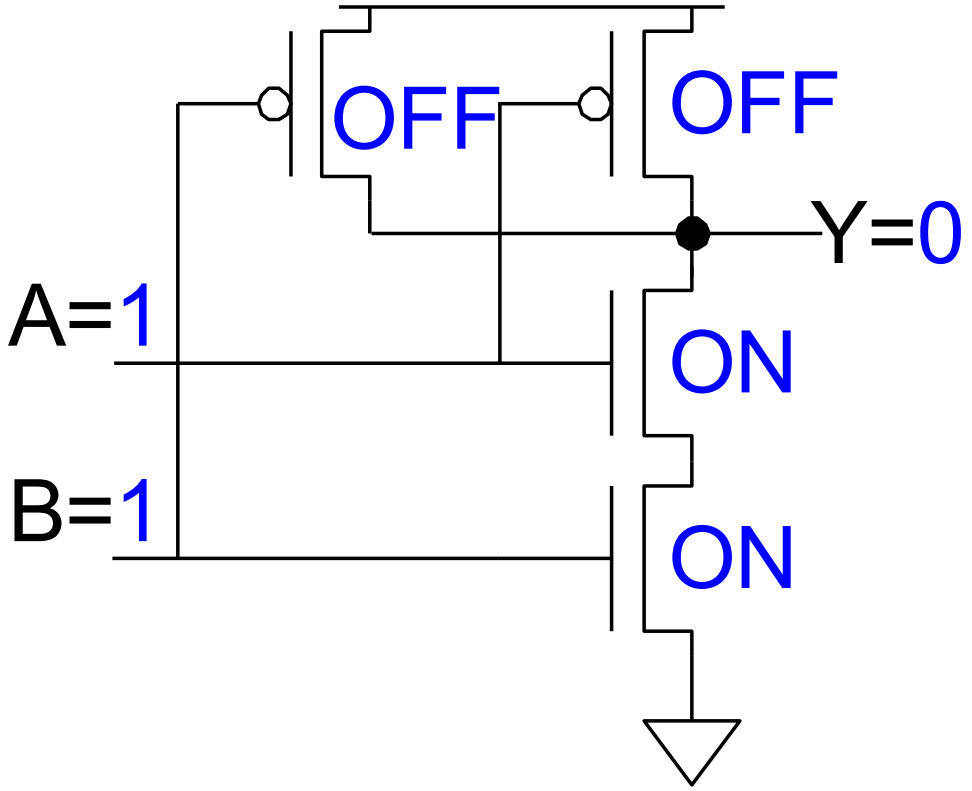




CMOS NAND Gate

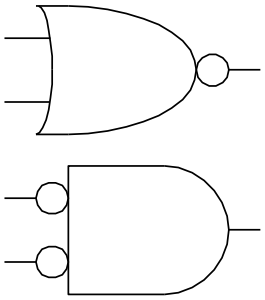
A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

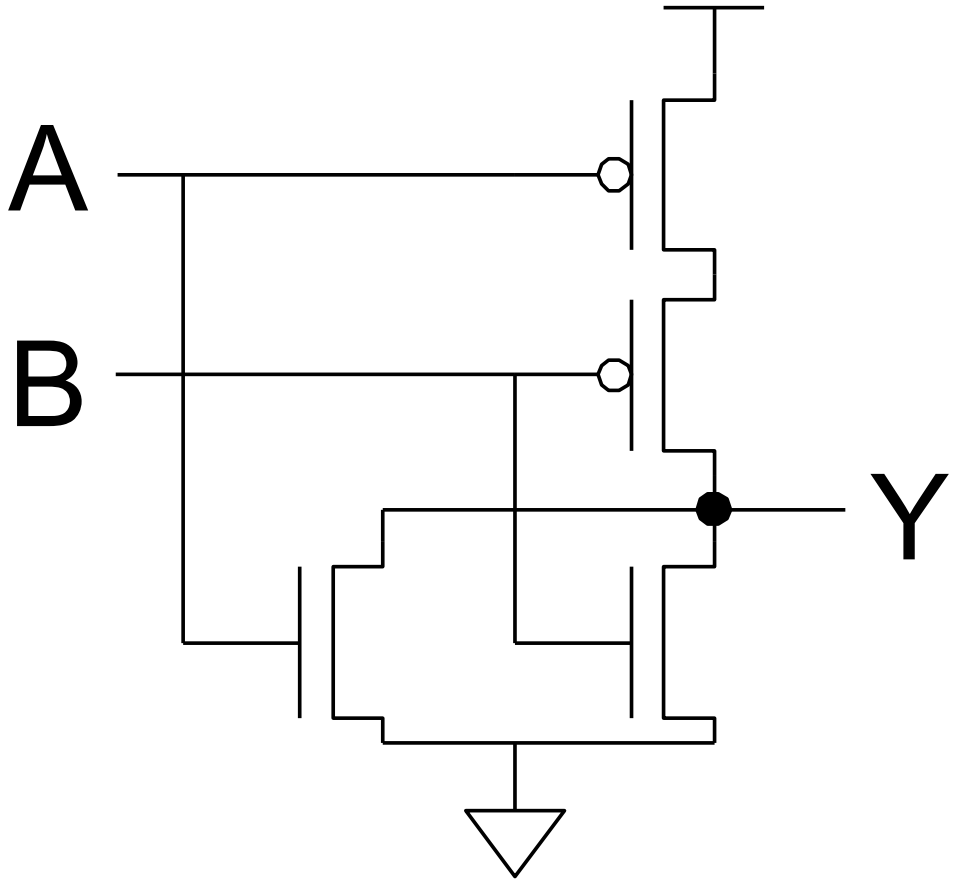




CMOS NOR Gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0





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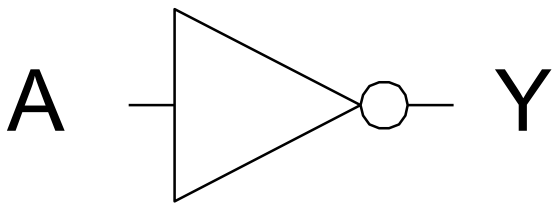
3-input NAND Gate

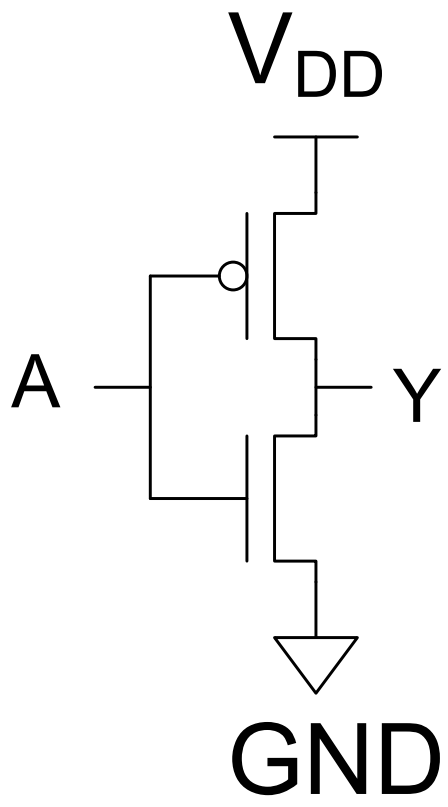
- Y pulls low if ALL inputs are 1
- Y pulls high if ANY input is 0

CMOS Logic Gate Design

Review CMOS Inverter

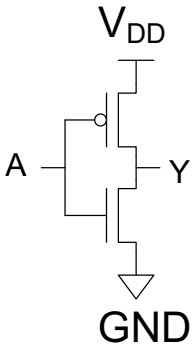
A	Y
0	**1**
1	0

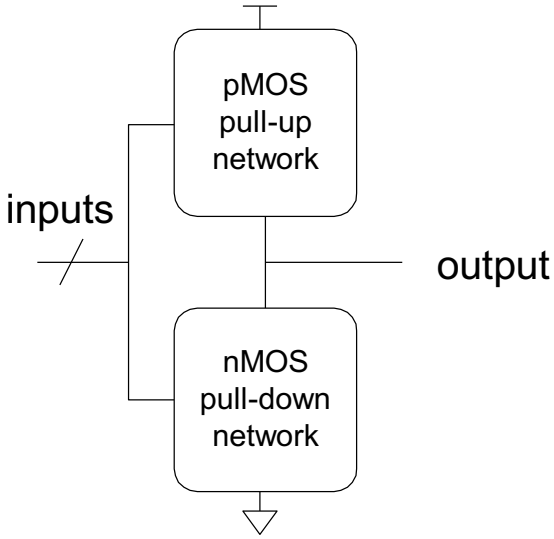




Complementary CMOS

- Complementary CMOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*

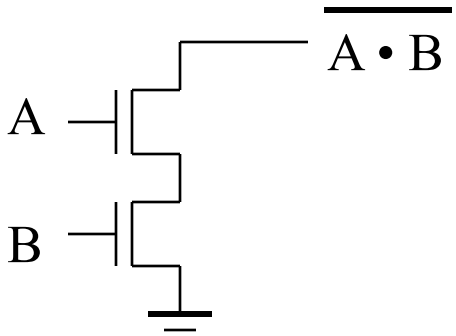




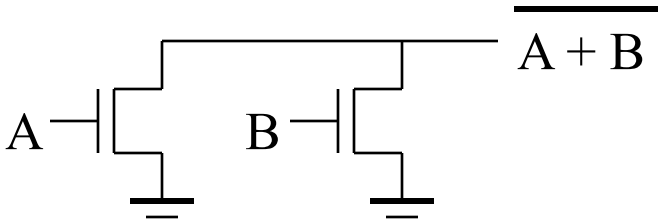
	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

Construction of PDN

- NMOS devices in series implement a NAND function

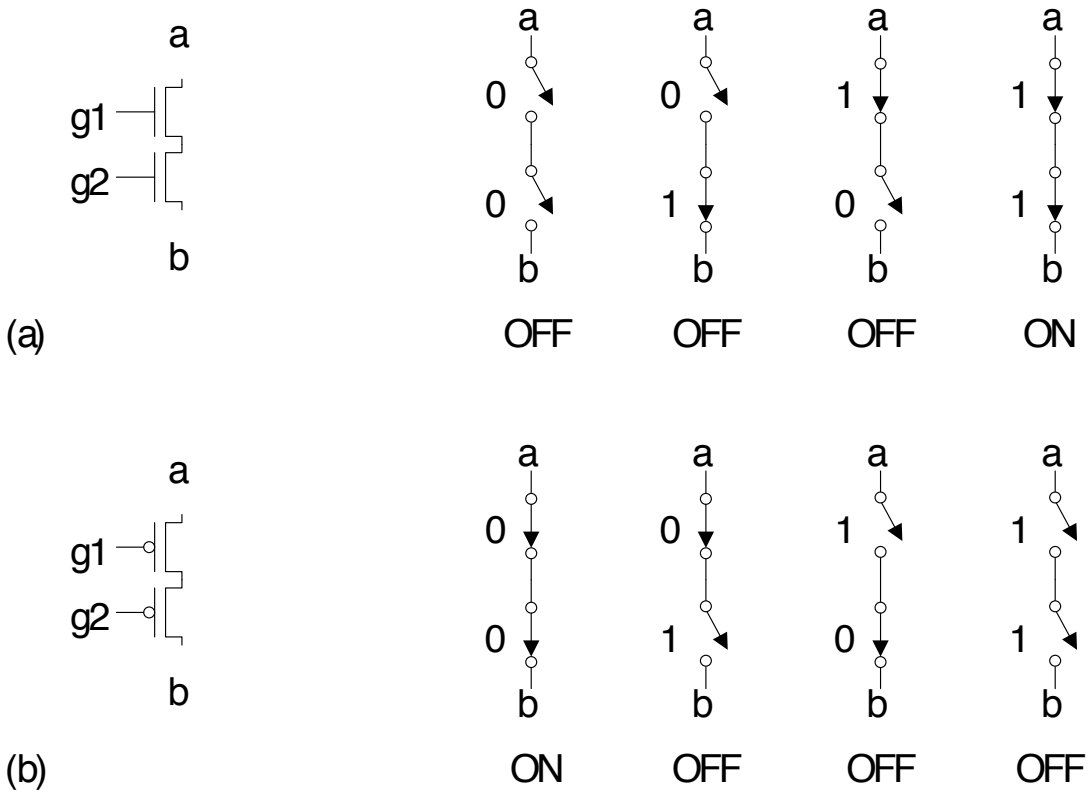


- NMOS devices in parallel implement a NOR function



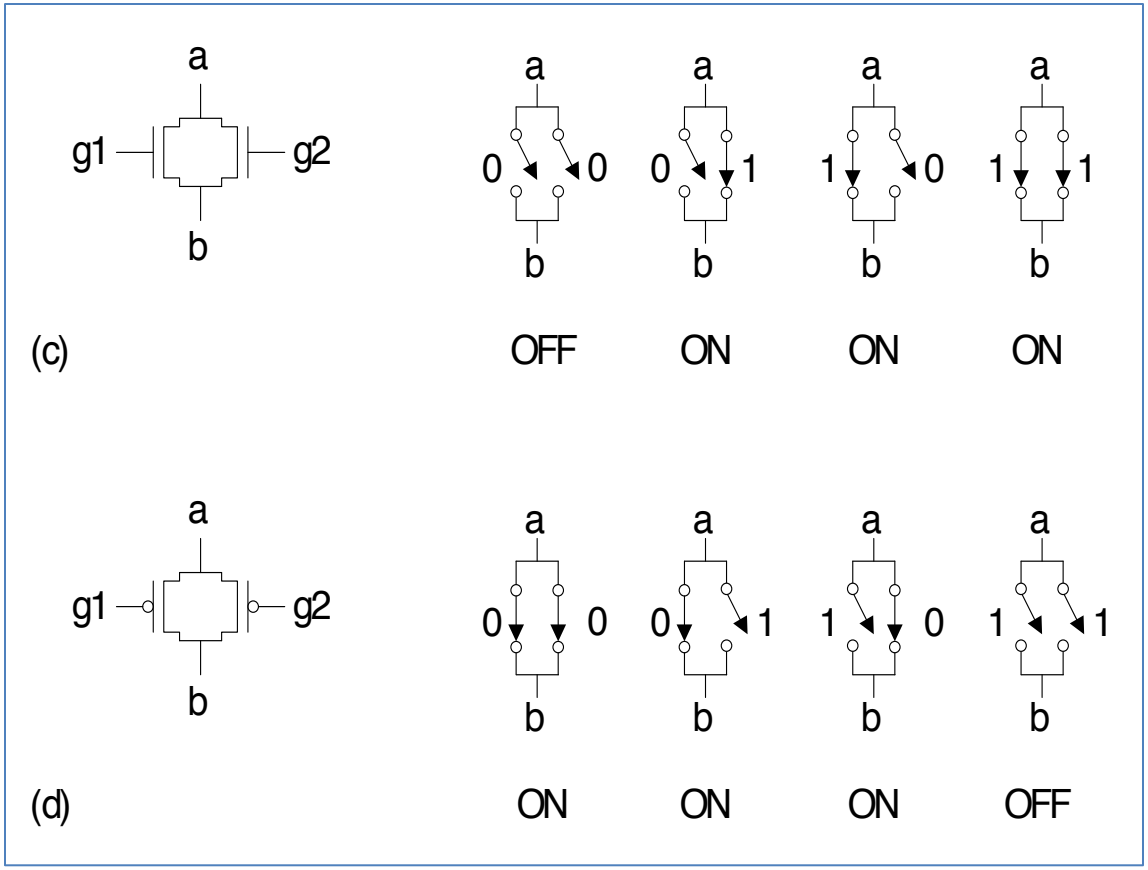
Series and Parallel (1)

- *Series*: both must be ON to be conductive
- *Parallel*: either can be ON to be conductive



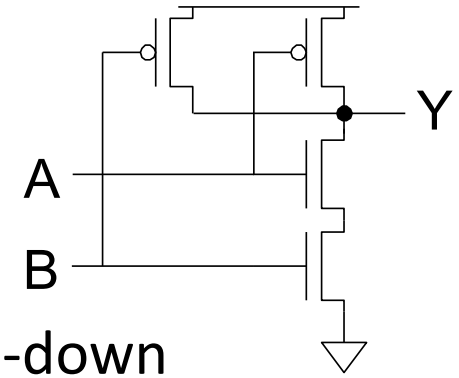
Series and Parallel (2)

- *Series*: both must be ON to be conductive
- *Parallel*: either can be ON to be conductive



Conduction Complement

- Complementary CMOS gates always produce 0 or 1
- Ex: NAND gate
  - Series nMOS: Y=0 when both inputs are 1
  - Thus Y=1 when either input is 0
  - Requires parallel pMOS



- Rule of *Conduction Complements*
  - Pull-up network is complement of pull-down
  - Parallel -> series, series -> parallel

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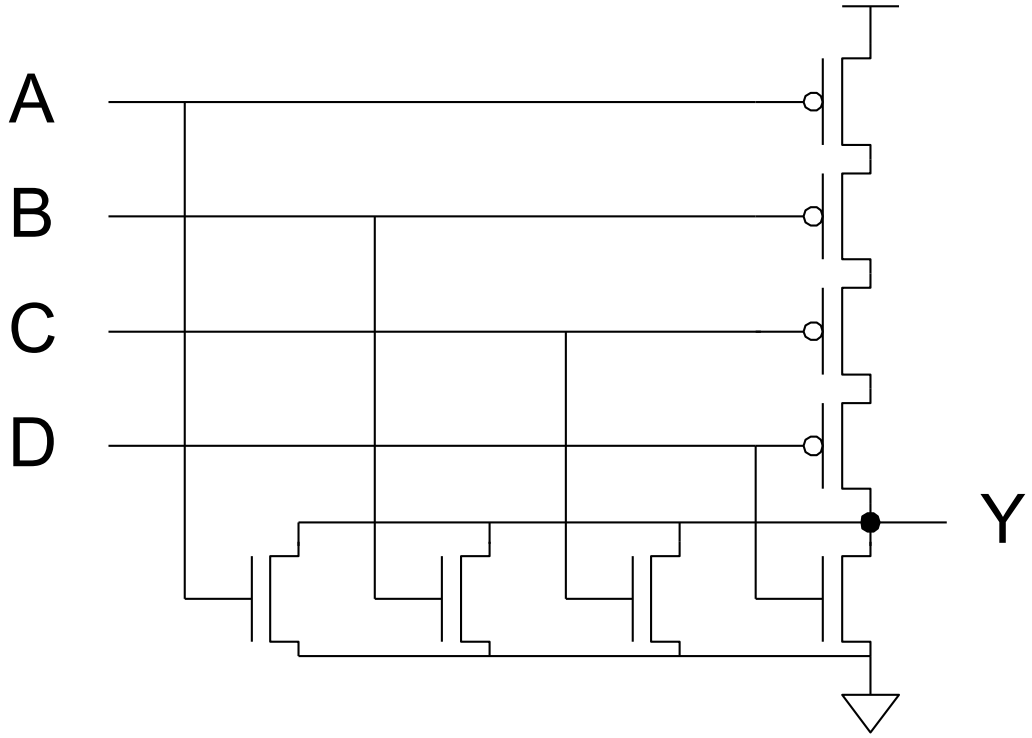
4-input CMOS NOR gate

- Activity:
  - Sketch a 4-input CMOS NOR gate

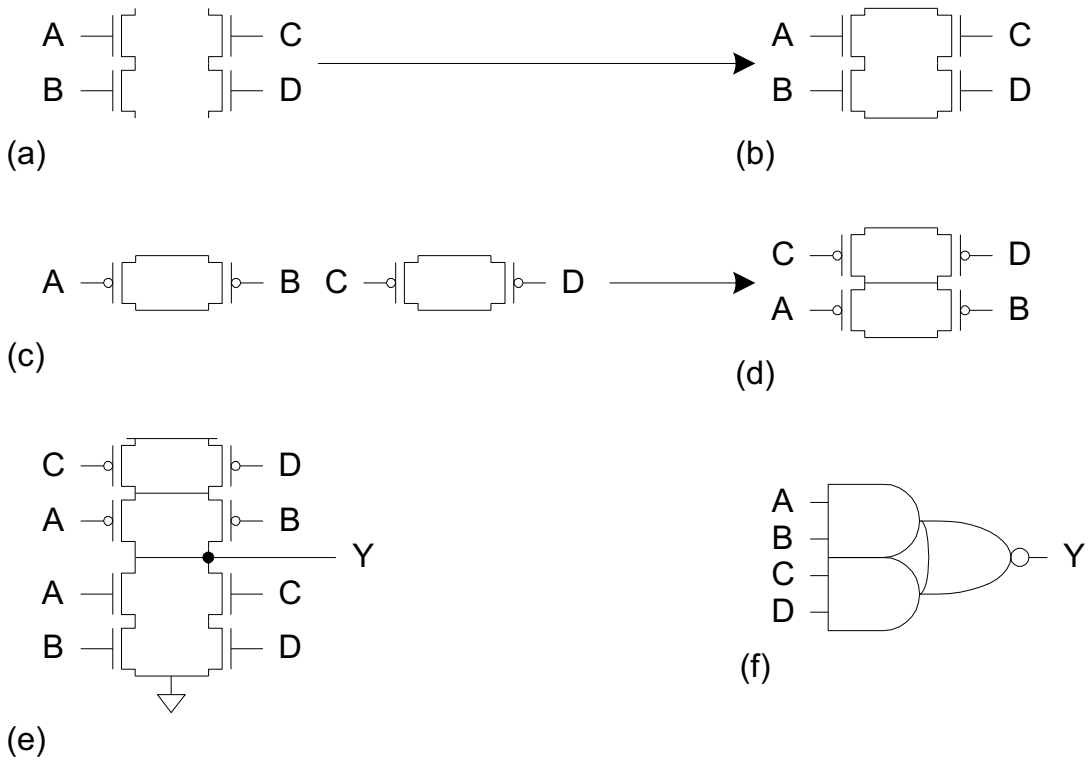
4-input CMOS NOR gate

- Activity:
  - Sketch a 4-input CMOS NOR gate



Compound Gates

- *Compound gates* can do any inverting function
- Ex: AND-OR-INVERT, AOI22 $Y = \overline{A \cdot B + C \cdot D}$



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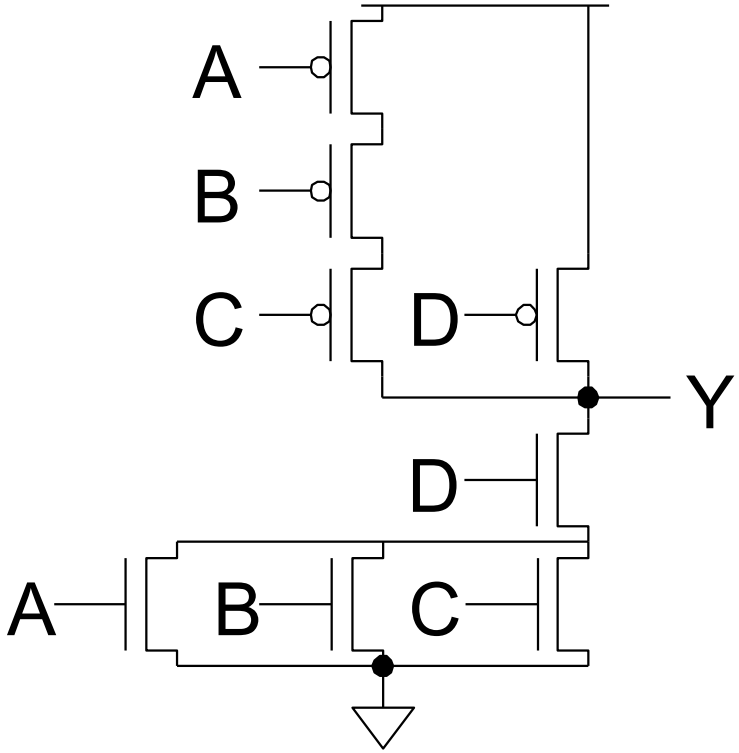
Example: O3AI

- $Y = \overline{(A + B + C) \cdot D}$

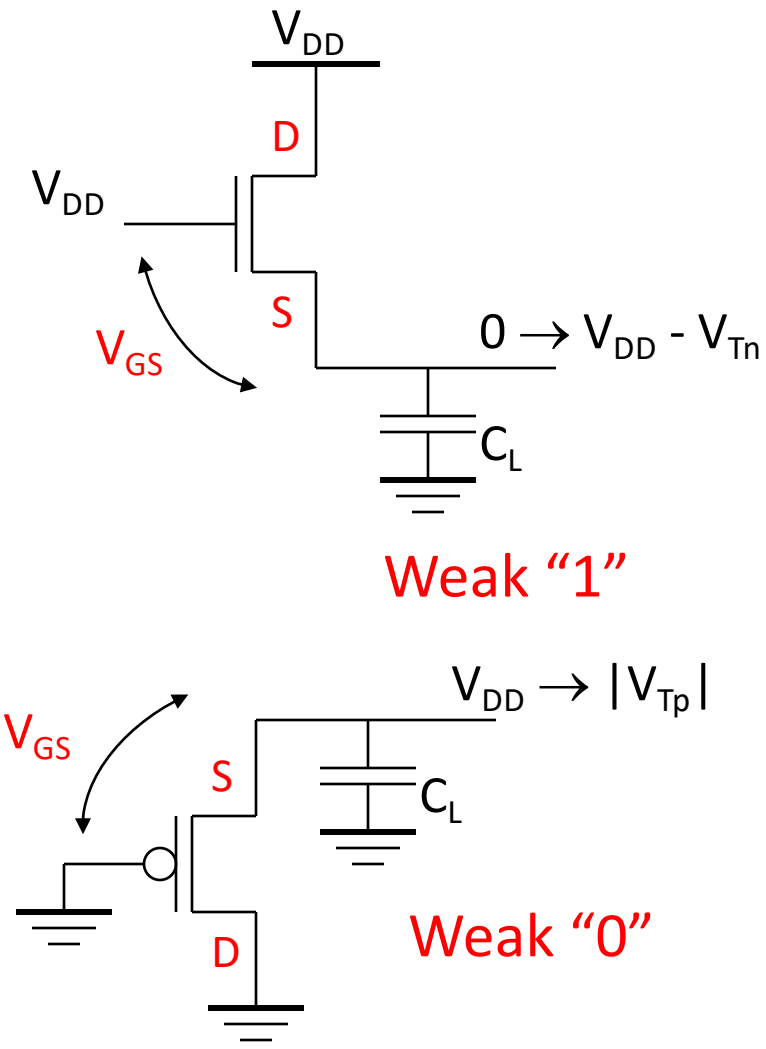
Example: O3AI

- $Y = \overline{(A + B + C) \cdot D}$



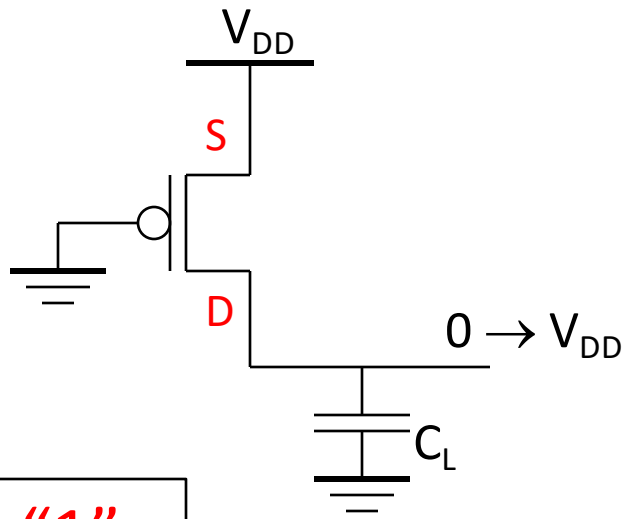
Signal Strength

- *Strength* of signal: How close it approximates ideal voltage source
- V_{DD} and GND rails are strongest 1 and 0
- nMOS pass strong 0
  - But degraded or weak 1
- pMOS pass strong 1
  - But degraded or weak 0
- Thus nMOS are best for pull-down network, pMOS are best for pull-up

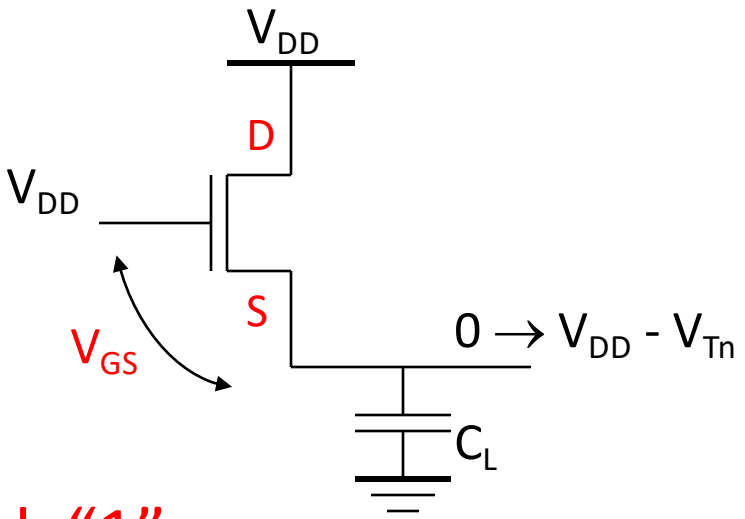


Review: Threshold Drops

PUN

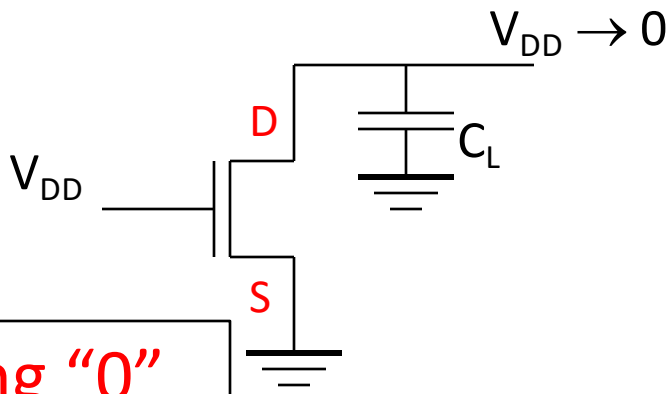


Strong "1"

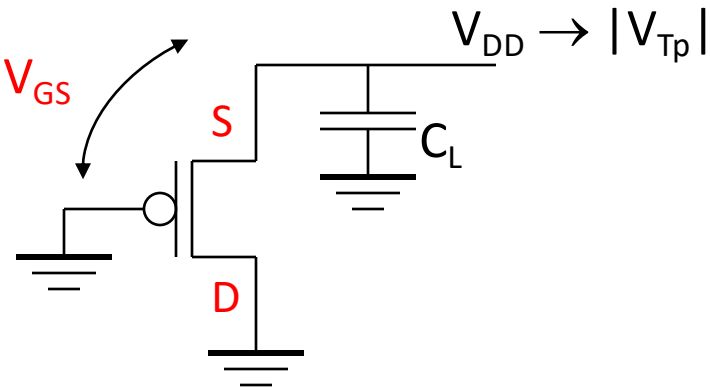


Weak "1"

PDN



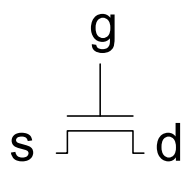
Strong "0"

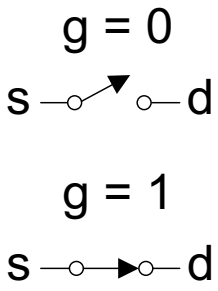


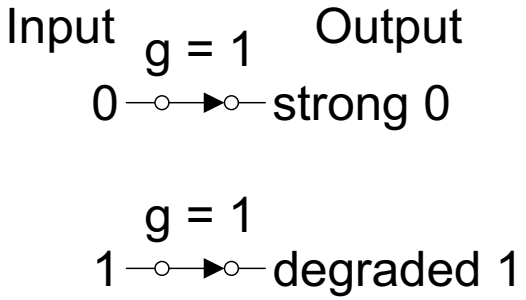
Weak "0"

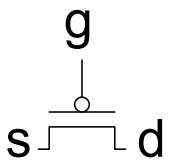
Pass Transistors

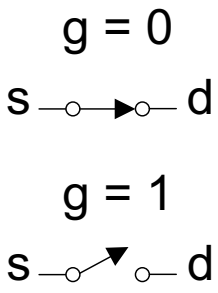
- Input is from the source
- Transistors can be used as switches

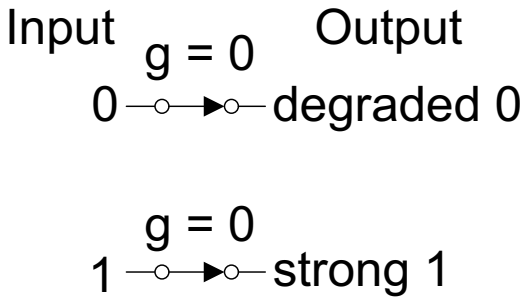






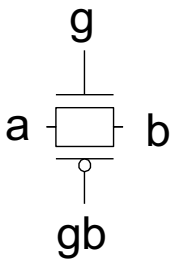


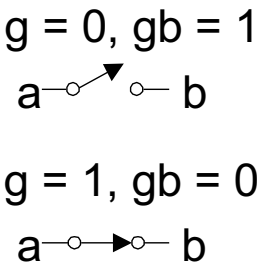


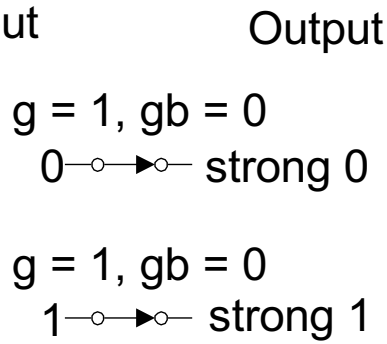


Transmission Gates

- Pass transistors produce degraded outputs
- *Transmission gates* pass both strong 0 and 1

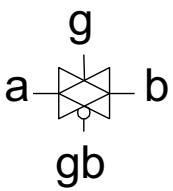


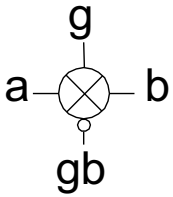


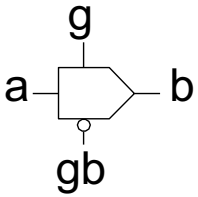


nMOS pass strong 0

pMOS pass strong 1





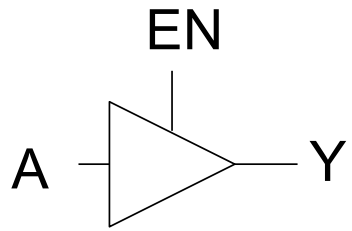


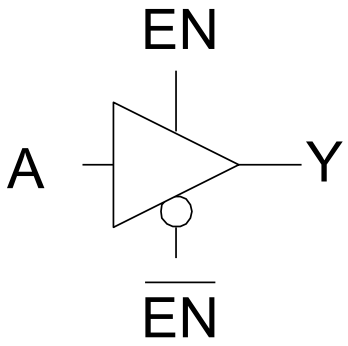
Symbol of Transmission Gates

Tristate buffer

- *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	
0	1	
1	0	
1	1	

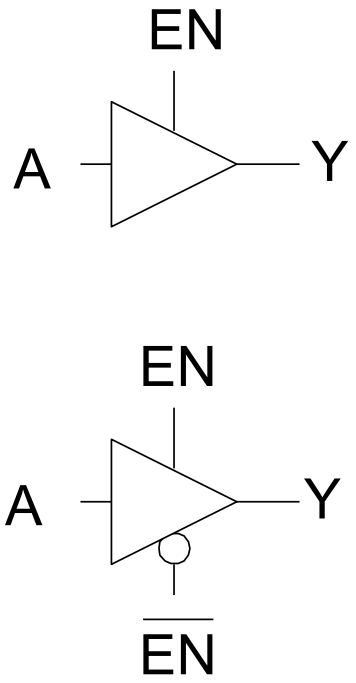




Tristate buffer

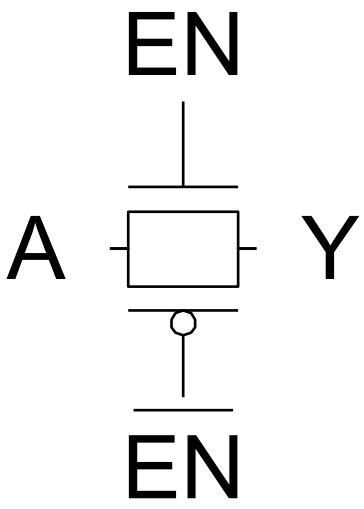
- *Tristate buffer* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1



Nonrestoring Tristate

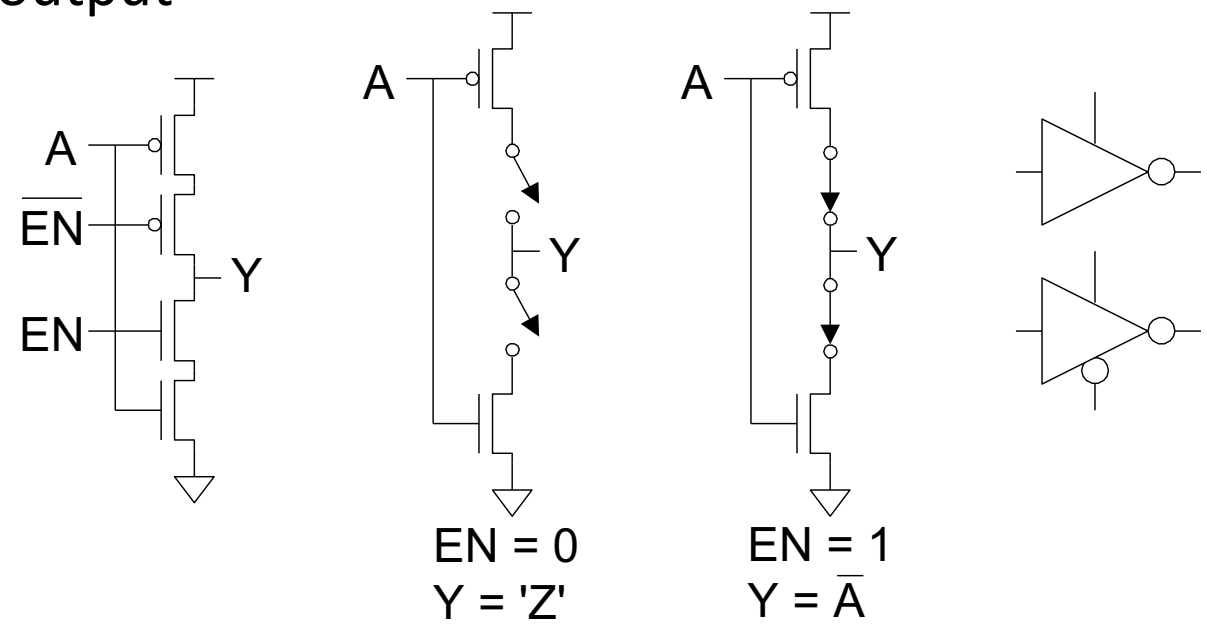
- Transmission gate acts as tristate buffer
  - Only two transistors
  - But *nonrestoring*
    - Noise on A is passed on to Y



EN	A	Y
0	0	Z
0	1	Z
1	0	0
1	1	1

Tristate Inverter

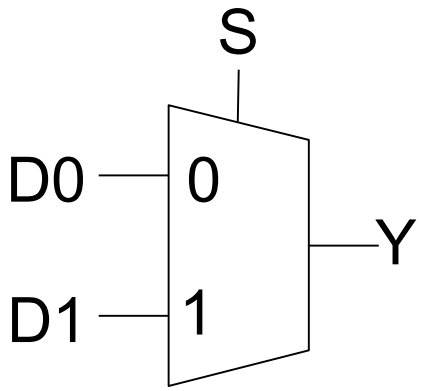
- Tristate inverter that produces restored output
  - Restored output: output is strongly driven and noise in the input is not passed to output
  - Violates conduction complement rule because we want a Z output



Multiplexers

- 2:1 multiplexer chooses between two inputs

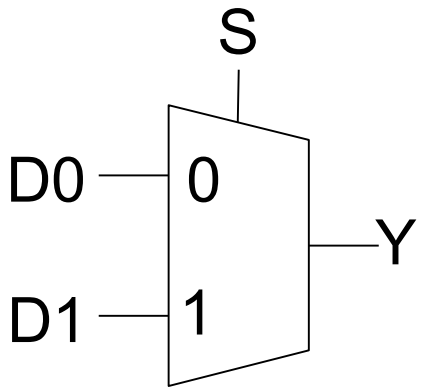
S	D1	D0	Y
0	X	0	
0	X	1	
1	0	X	
1	1	X	



Multiplexers

- 2:1 multiplexer chooses between two inputs

S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1



Gate-Level Mux Design

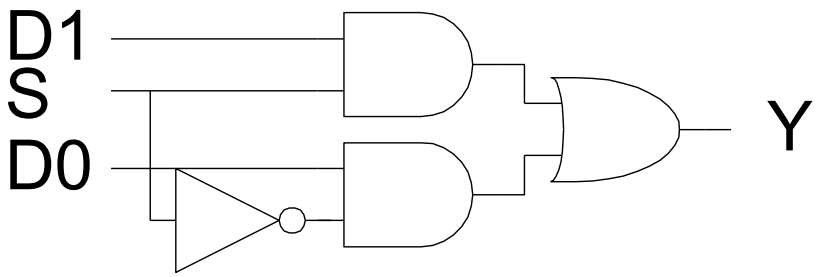
- How many transistors are needed?

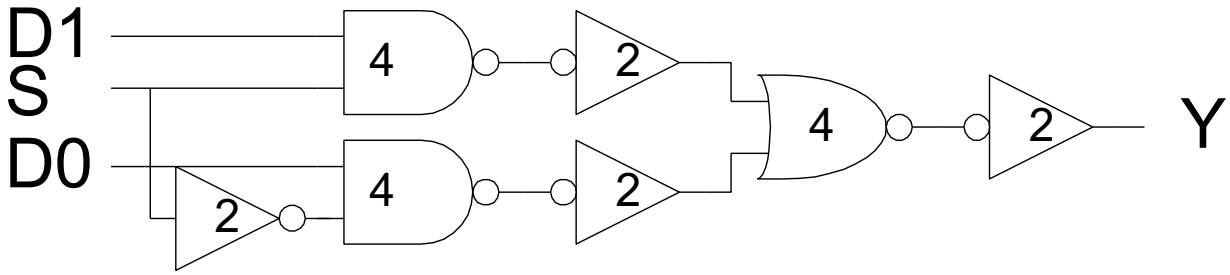
$$Y = SD_1 + \overline{S}D_0$$

Gate-Level Mux Design

- How many transistors are needed? 20

$$Y = SD_1 + \overline{S}D_0$$





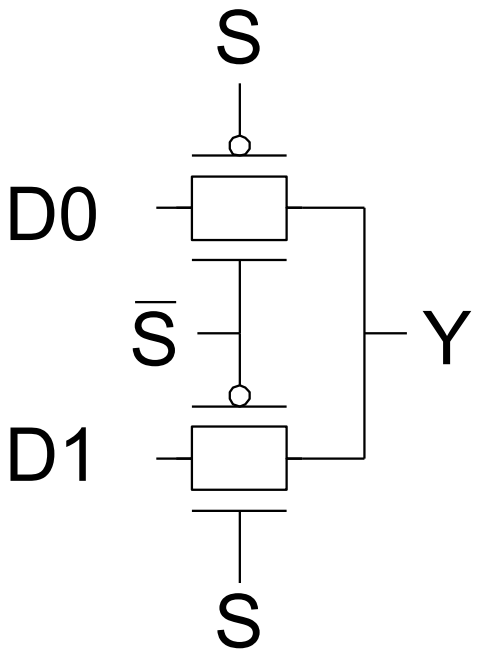
Transmission Gate Mux

- Nonrestoring mux uses two transmission gates

Transmission Gate Mux

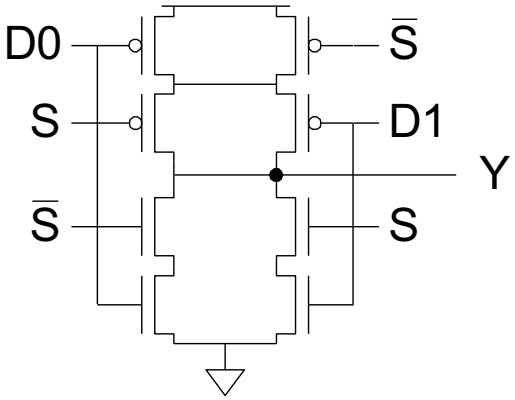
- Nonrestoring mux uses two transmission gates

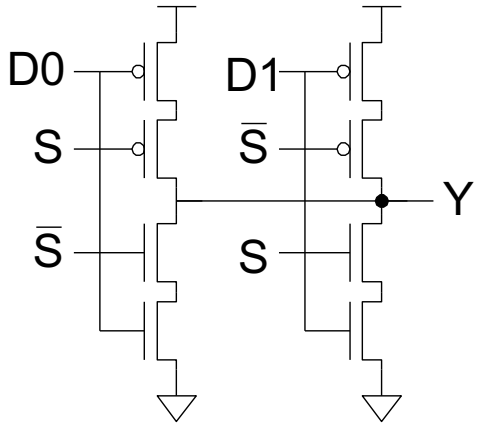
Only 4 transistors

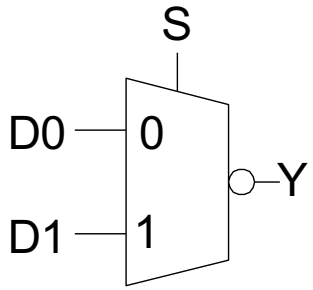


Inverting Mux

- Inverting multiplexer
  - Use compound AOI22
  - Or pair of tristate inverters
  - Essentially the same thing
- Noninverting multiplexer adds an inverter

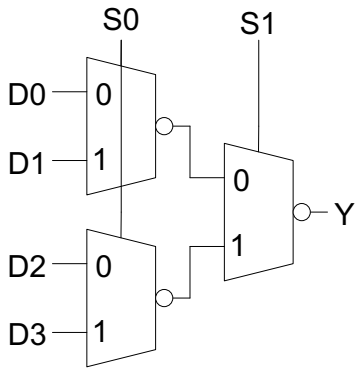


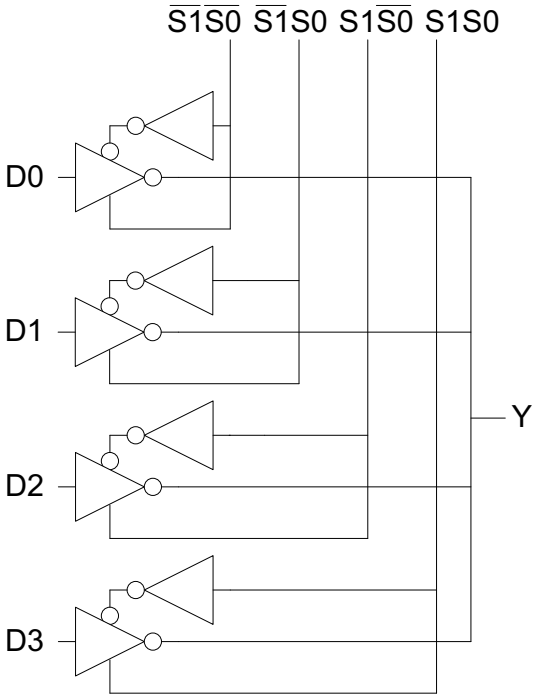




4:1 Multiplexer

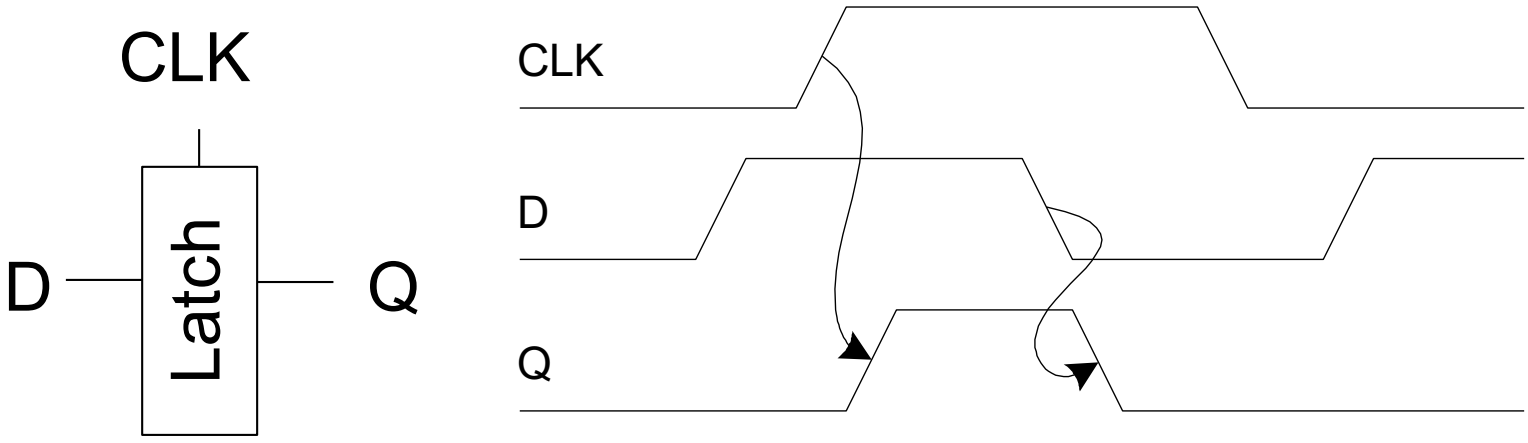
- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes
  - Or four tristates





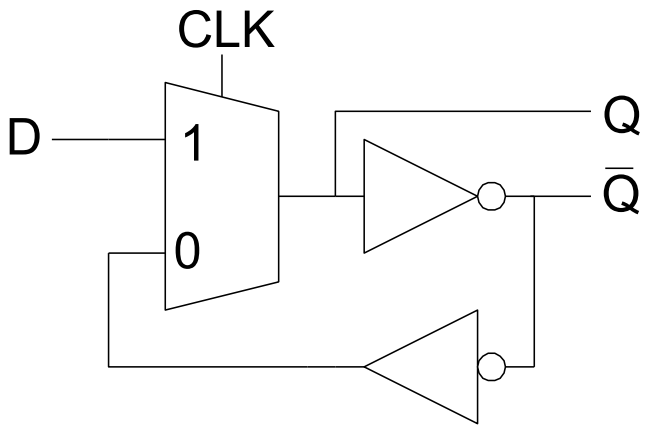
D Latch

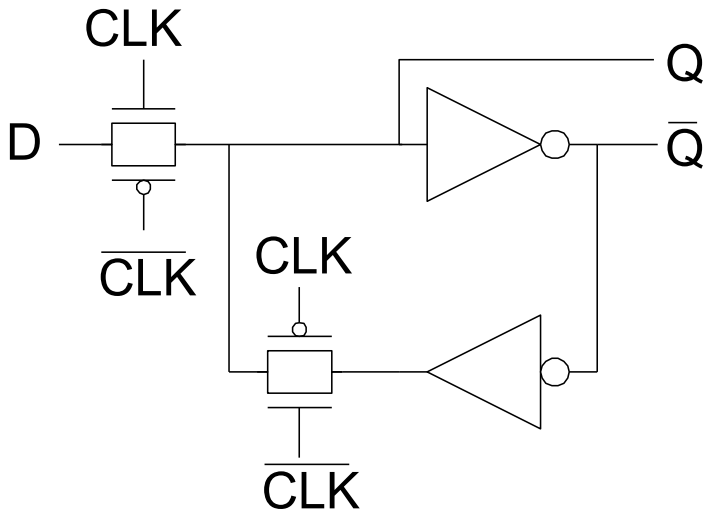
- When CLK = 1, latch is *transparent*
  - D flows through to Q like a buffer
- When CLK = 0, the latch is *opaque*
  - Q holds its old value independent of D
- a.k.a. *transparent latch* or *level-sensitive latch*



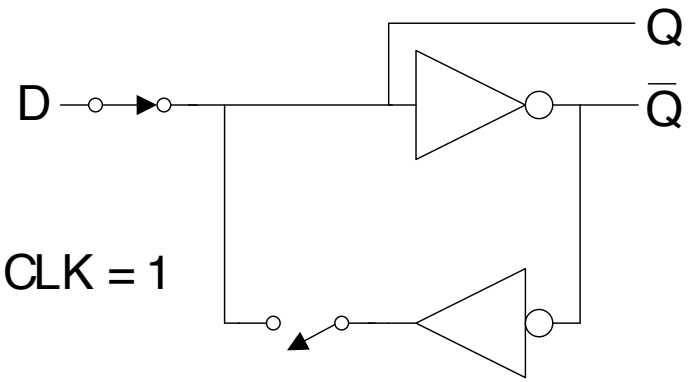
D Latch Design

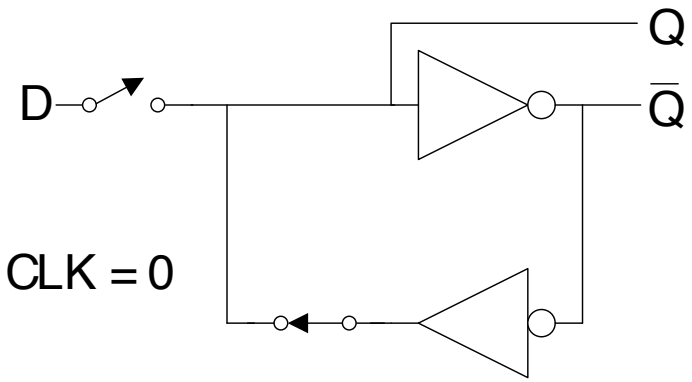
- Multiplexer chooses D or old Q
- See the D operation in the next slide

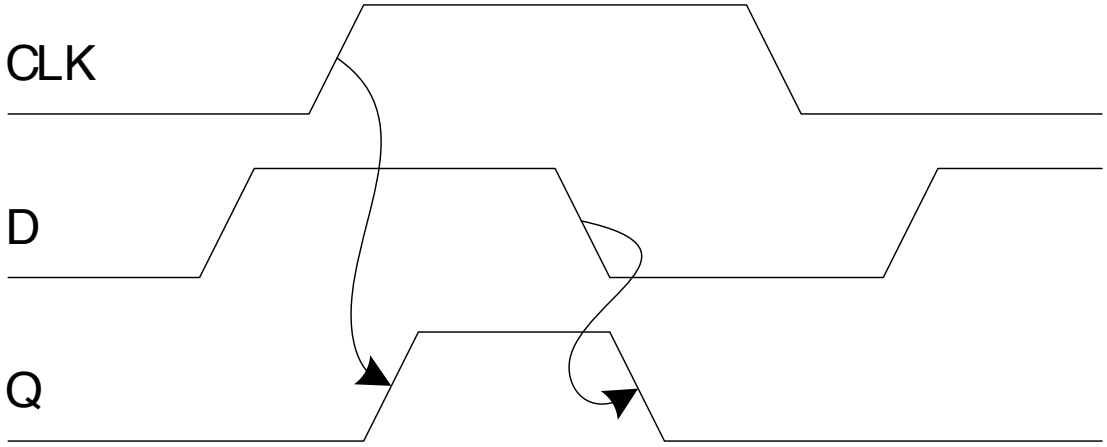


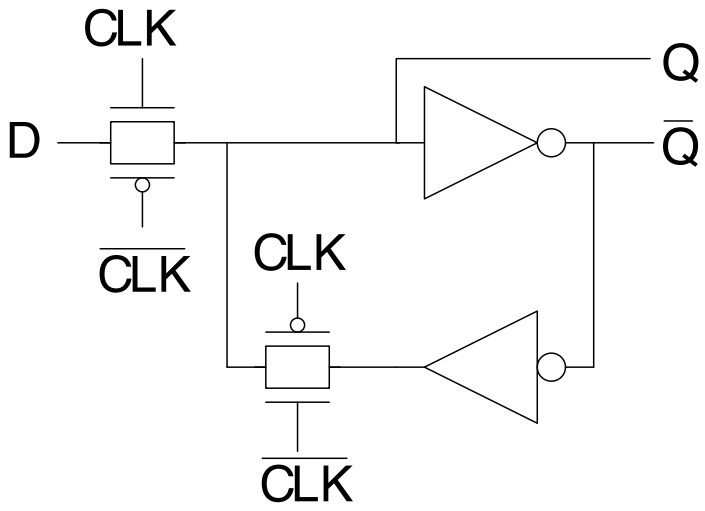


D Latch Operation



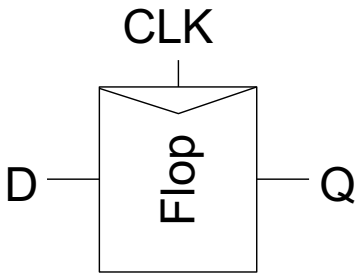


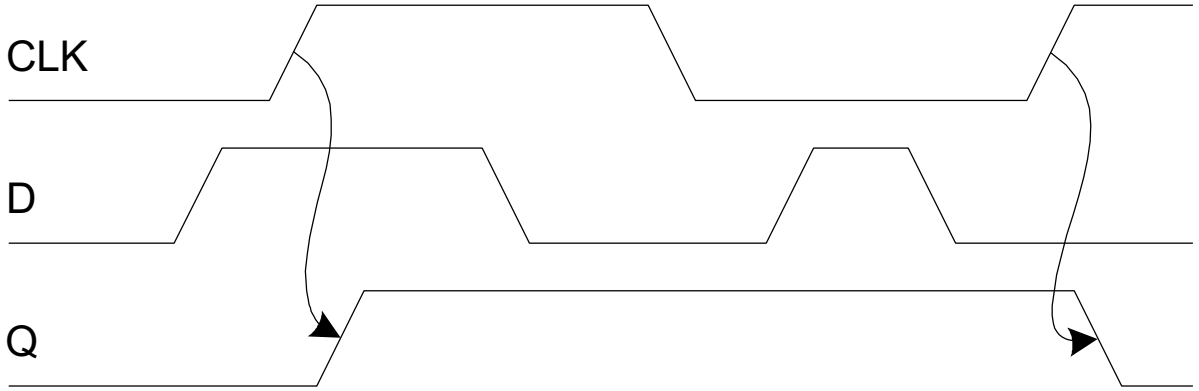




D Flip-flop

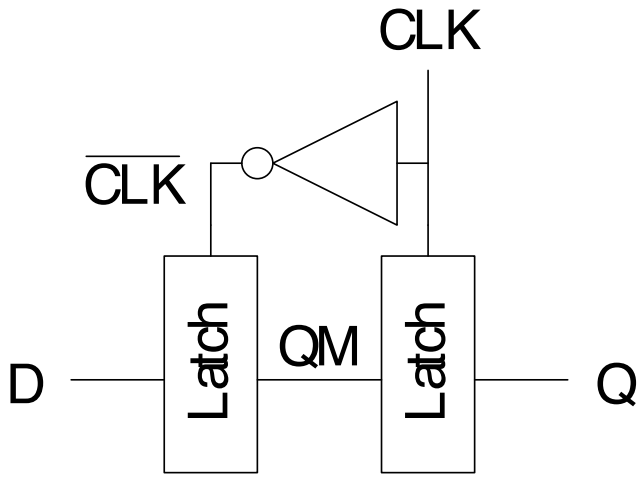
- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. *positive edge-triggered flip-flop*

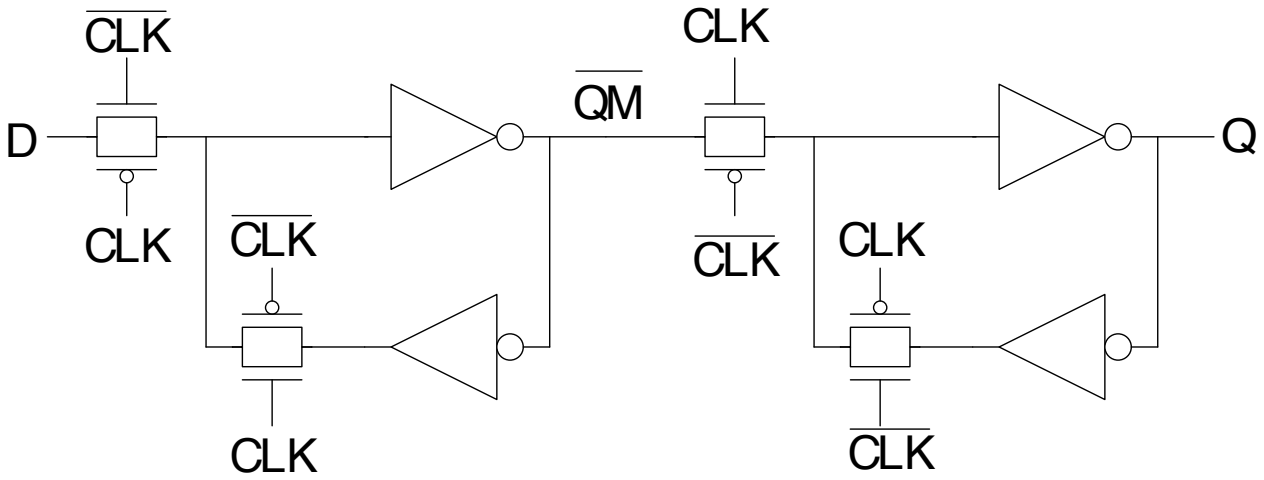




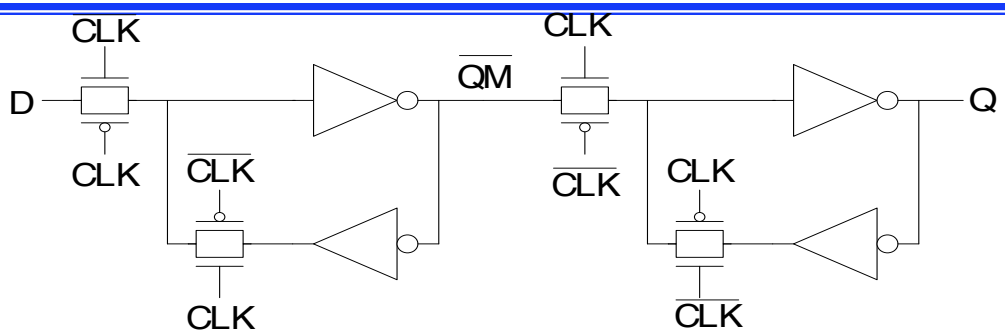
D Flip-flop Design

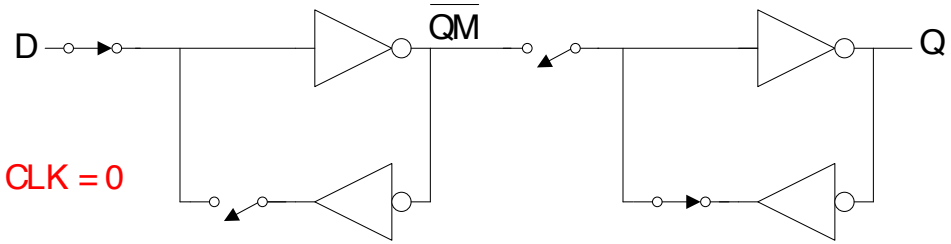
- Built from master and slave D latches

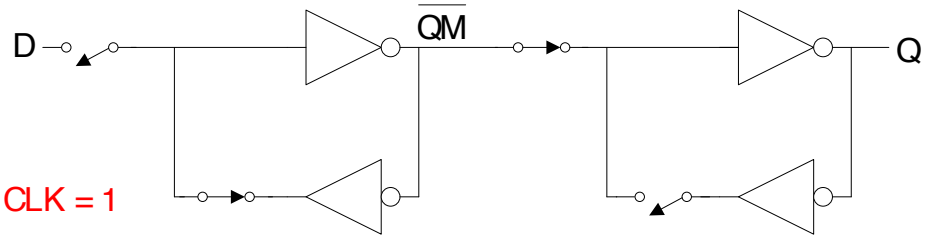


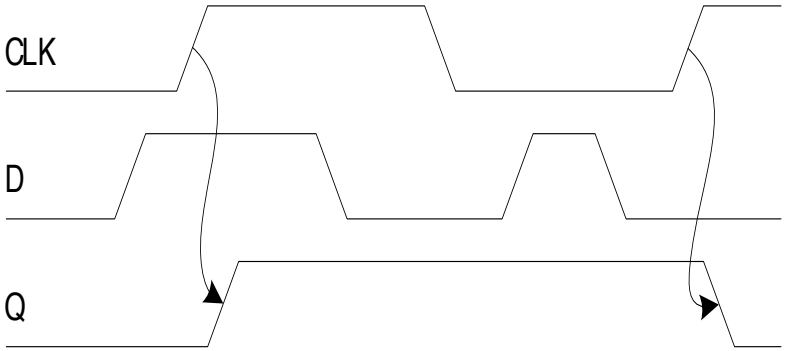


D Flip-flop Operation









Summary

- MOS Transistors are stack of gate, oxide, silicon
- Can be viewed as electrically controlled switches
- Build logic gates and flip-flops out of switches

- Now you know everything necessary to start designing schematics and layout for a simple chip!

Backup slides