Deep learning IC Design

Course Administration

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Course Website:

http://moodle.ncku.edu.tw

announces and slides will be posted here

submit your homework there

Topics Covered

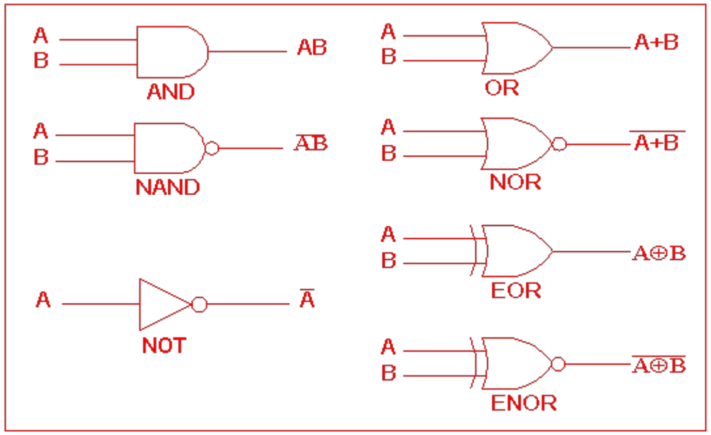
- Verilog
- Combinational
- Sequential Circuit Design
- Finite State Design
- Data Path Design
- Synthesizable Verilog
- VLSI Design Flow (EDA Design Flow)
- Arithmetic Circuit
- FPGA + Pynq + Vivado
- Deep Learning Background
- Survey of DNN Development Resource
- DNN Inference Background
- DNN Hardware
- Roofline Model
- DNN Memory Access Model
- Case Study

Textbook & Materials

- Verilog
  - Verilog HDL, by Samir Palnitkar
  - Digital Design: With an Introduction to Verilog HDL
- Tutorial on HW Architectures for Deep Neural Networks
  - http://eyeriss.mit.edu/tutorial.html
- VLSI
  - Integrated Circuit Design, fourth edition, by N. Weste, and David Harris
- Pynq: http://www.pynq.io
- Selected Paper

Prerequisite

- Introduction to Digital System (F720900)
  - Logic Gates and Gate-Level Minimization
  - Combinational Logic and Synchronous Sequential Logic



- Programming Language: Python
- Personal Computer (Laptop is preferred)

Tentative Grading

- Homework and Lab Assignment (35 %)
- Midterm Exams (30 %)
- Class Participation (Attendance and In-class quick test, 15%)
- Paper Presentation (10%)
- Project (10%)
- Percentage of each part may change slightly

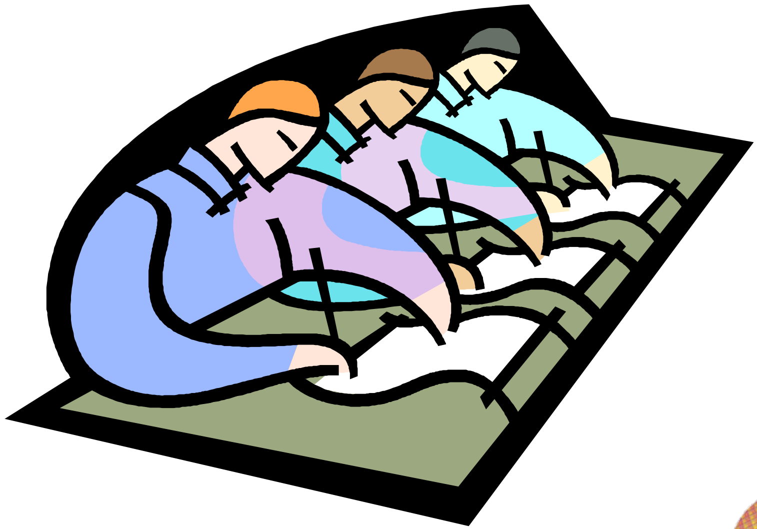
- 35

Note for Homework and Lab Assignment

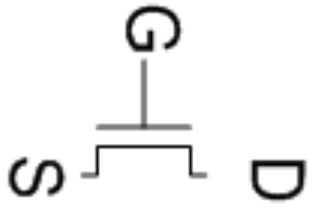
- Grading for each homework
    - Report: You need to carefully explain your codes and results in you results. If your explanation is unclear, you will lose points
- Honesty is the best policy. If you copy your homework from someone, both will get zero points for your homework. In addition, both will lose points of your final grade for each violation.

In-class quick test

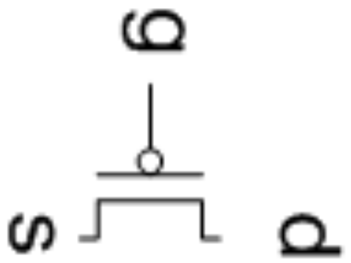
- In-class quick test is a very simple test.
- Will be announced in a few days before. Test what you have learn.
- Normally take less than 20 minutes.
  - If you can’t do anything, you will get 40 points
- Cover what I taught in the previous class



Recap of basic MOS transistors and logic gates

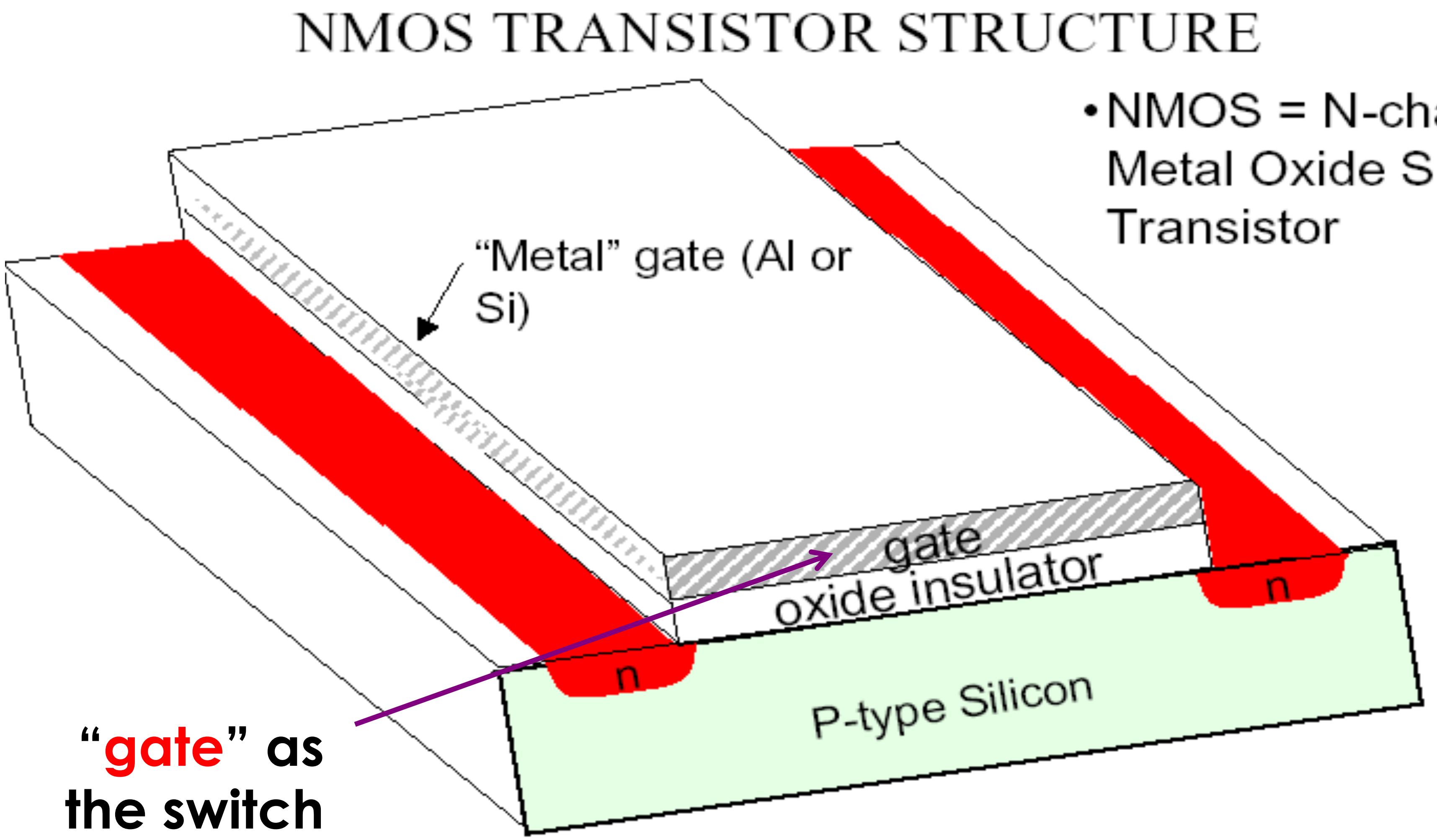


NMOS



PMOS

Electric Switch

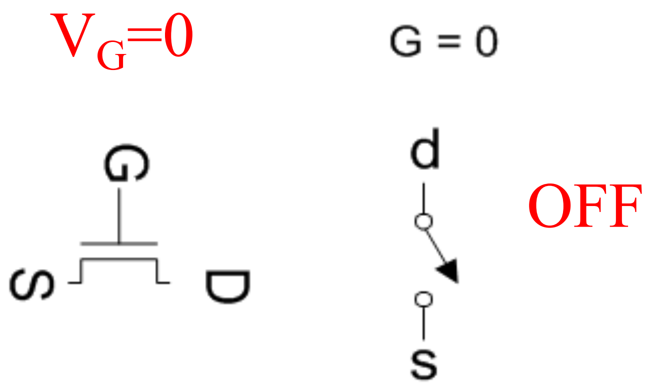


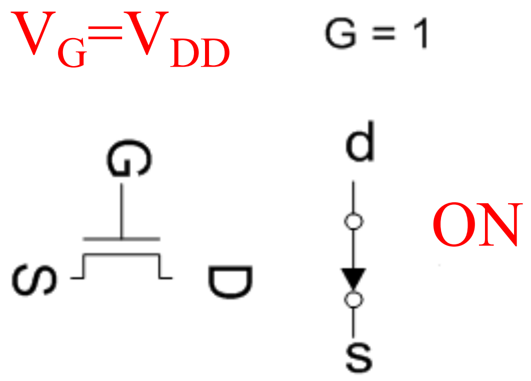
- NMOS = N-channel Metal Oxide Silicon Transistor

"gate" as the switch

nMOS transistor

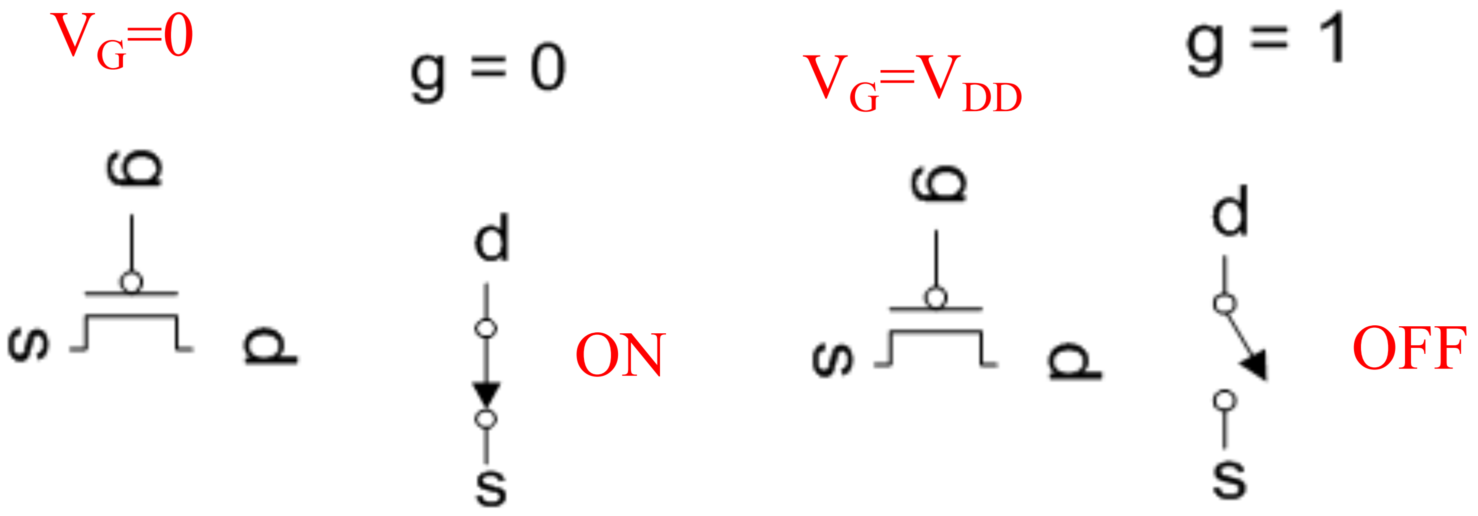
- When the gate is at a low voltage (V_G=0):
  - No channel, transistor is off
- When the gate is at a high voltage (V_G=V_{DD}):
  - Positive voltage inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON





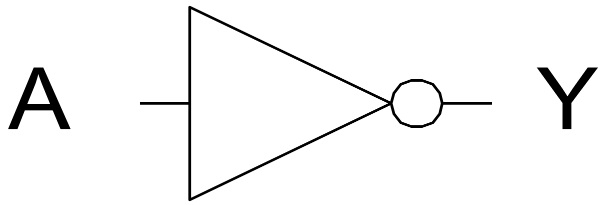
pMOS Transistor

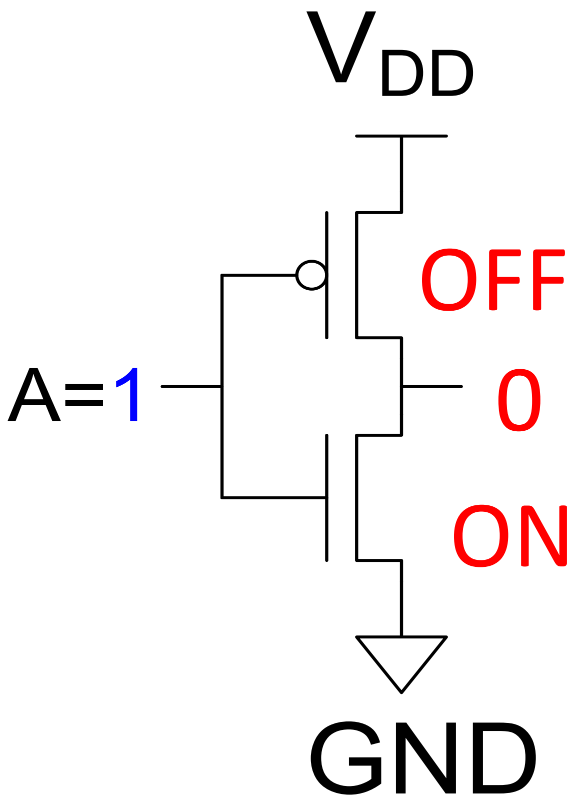
- Similar, but doping and voltages reversed
  - Input (V_G) at low voltage: transistor ON
  - Input (V_G) at high voltage: transistor OFF
  - Bubble indicates inverted behavior



CMOS Inverter

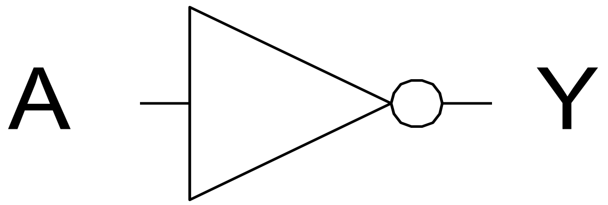
A	Y
0	
1	0

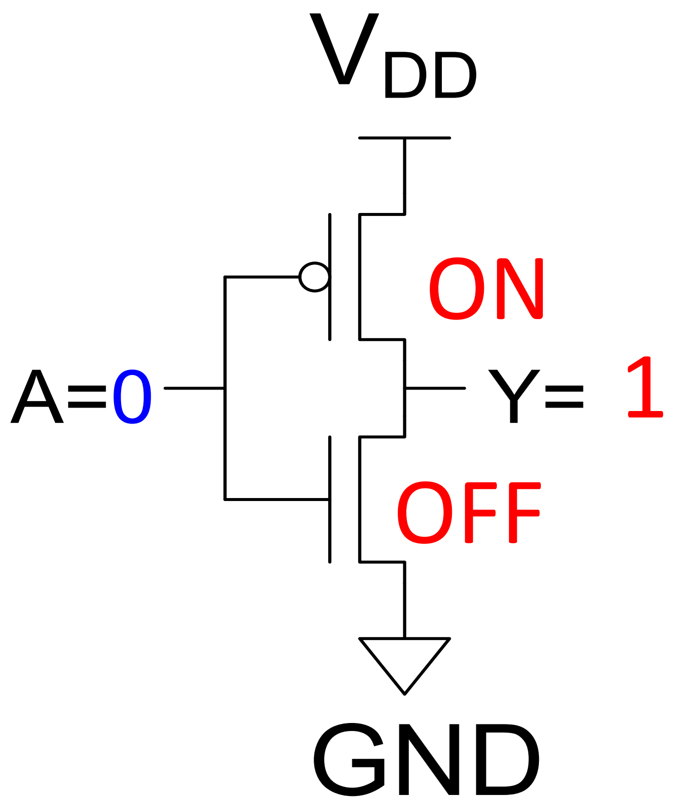




CMOS Inverter

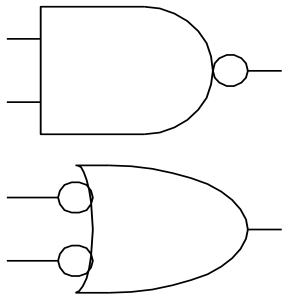
A	Y
0	**1**
1	0

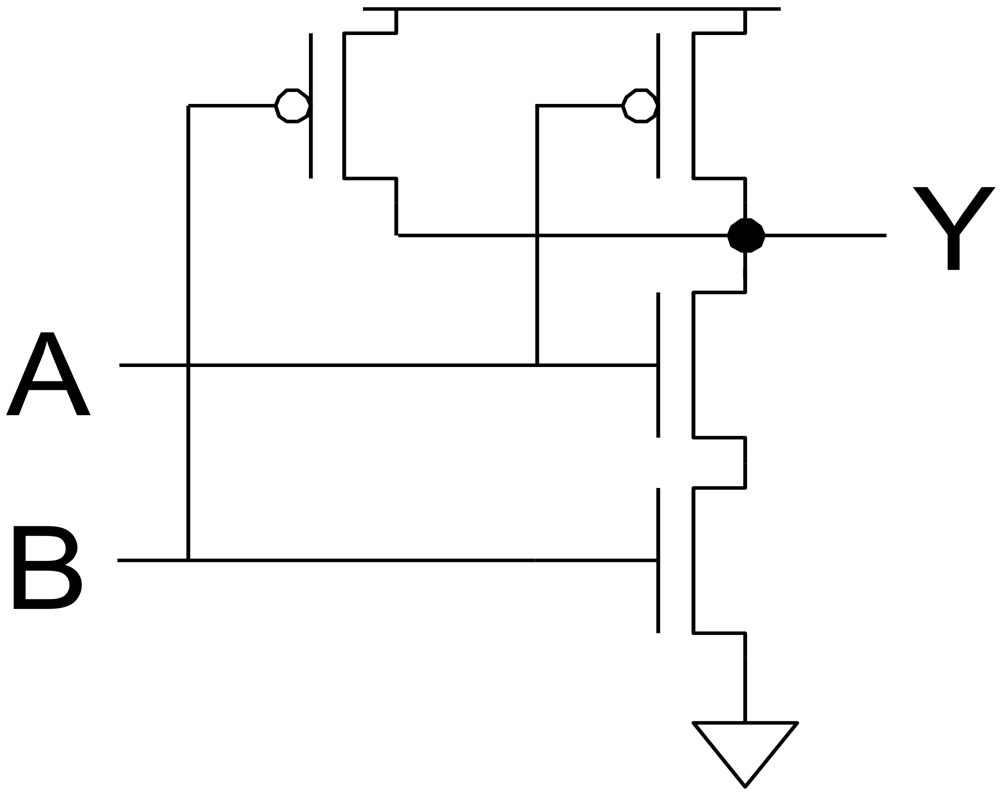




CMOS NAND Gate-1

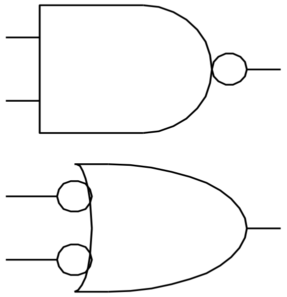
A	B	Y
0	0	
0	1	
1	0	
1	1	

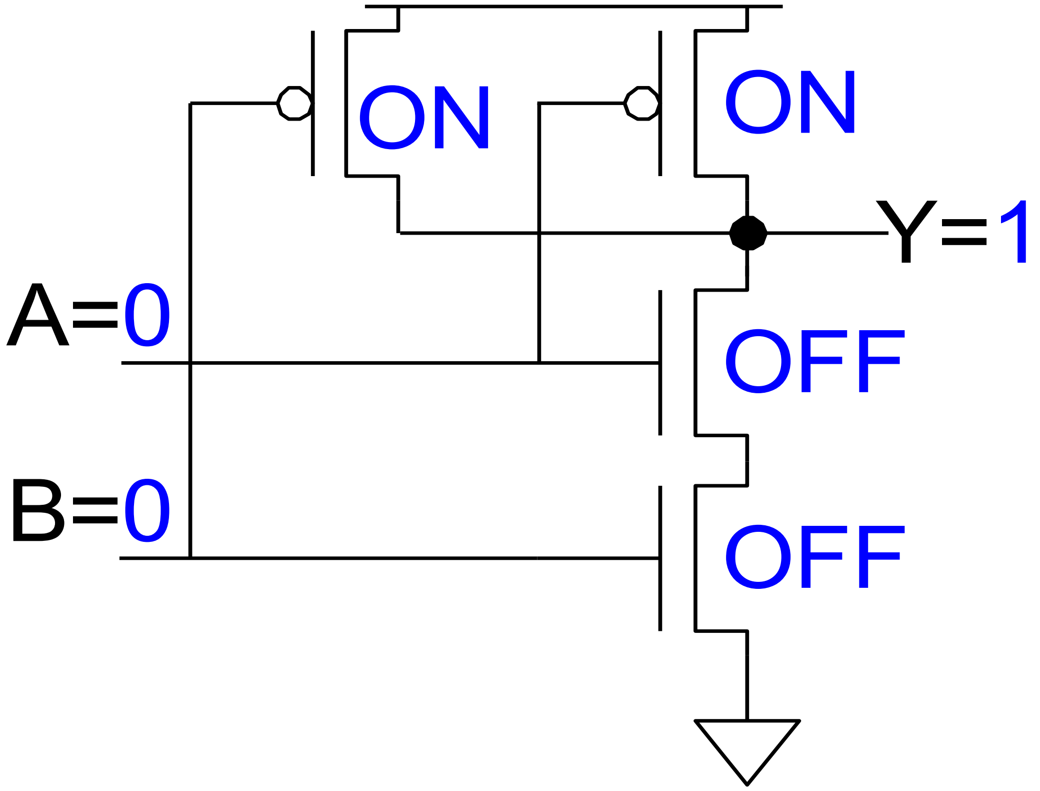




CMOS NAND Gate-2

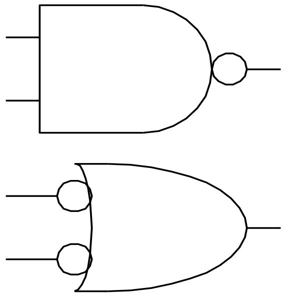
A	B	Y
0	**0**	**1**
0	1	
1	0	
1	1	

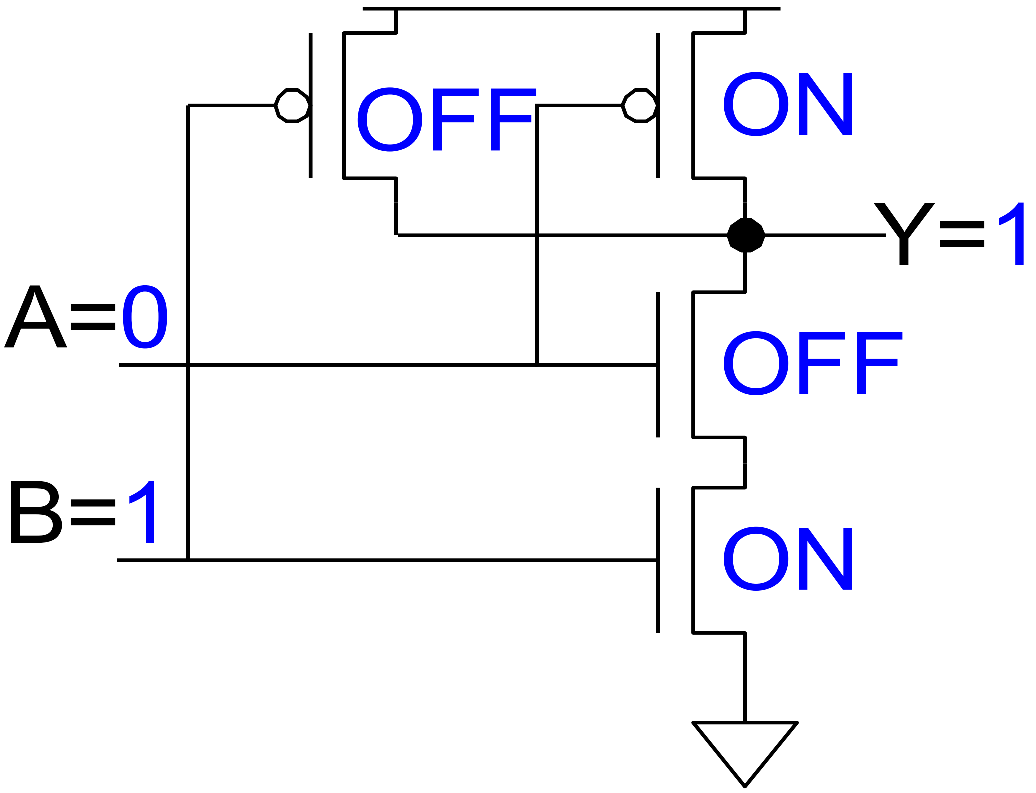




CMOS NAND Gate-3

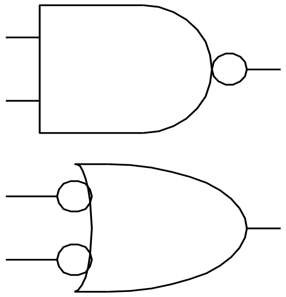
A	B	Y
0	0	1
0	**1**	**1**
1	0	
1	1	

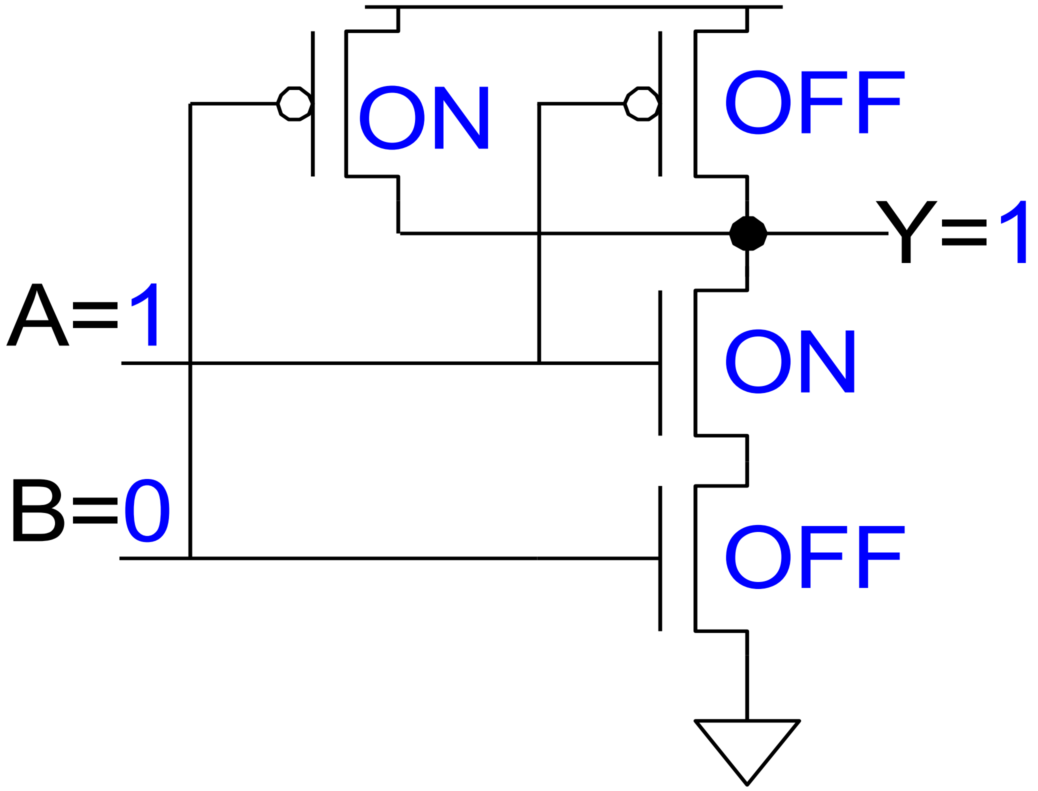




CMOS NAND Gate-4

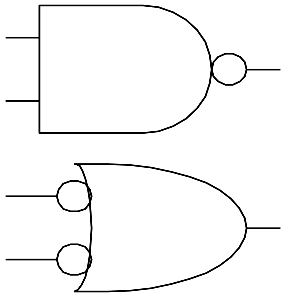
A	B	Y
0	0	1
0	1	1
1	**0**	**1**
1	1	

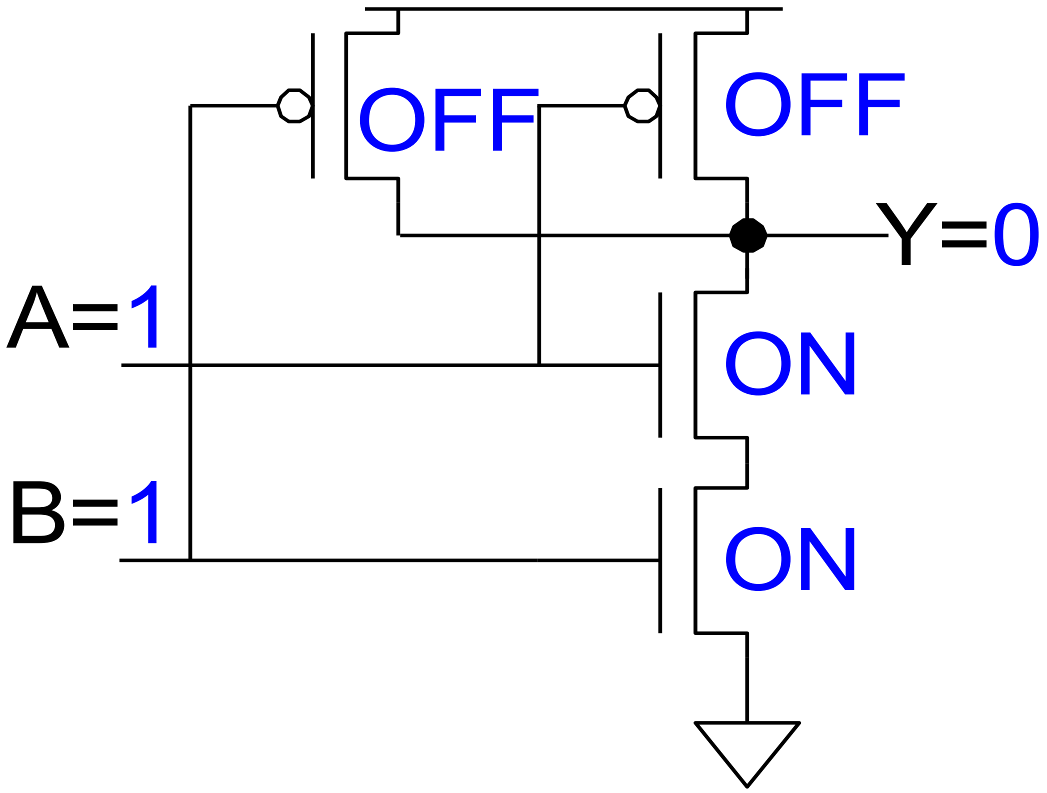




CMOS NAND Gate-5

A	B	Y
0	0	1
0	1	1
1	0	1
1	**1**	**0**

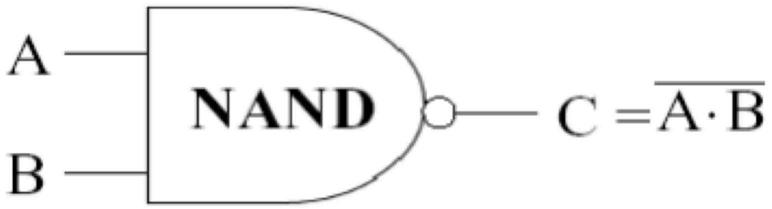


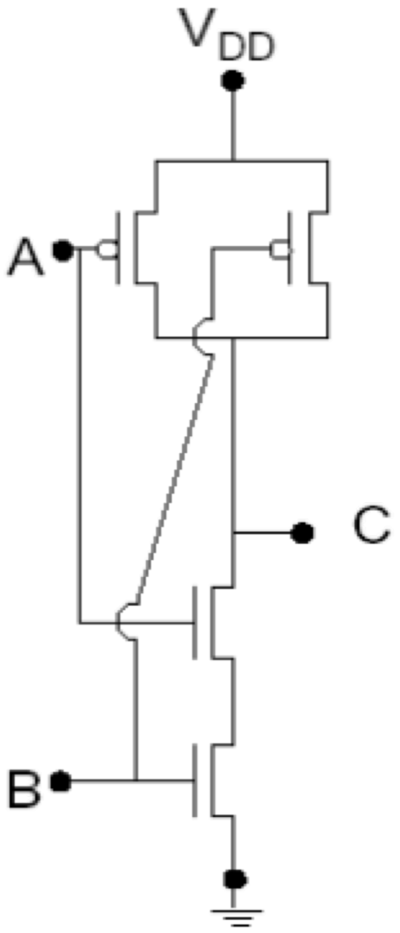


Use Switch to build Gates

- CMOS NAND:

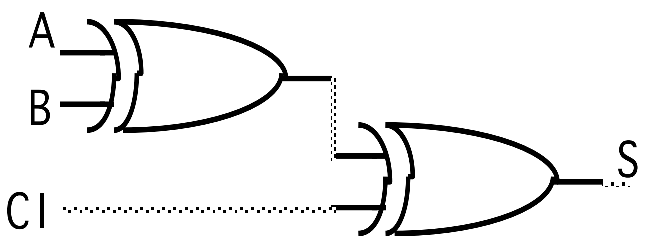
A	B	A B	C= $\overline{A\,B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

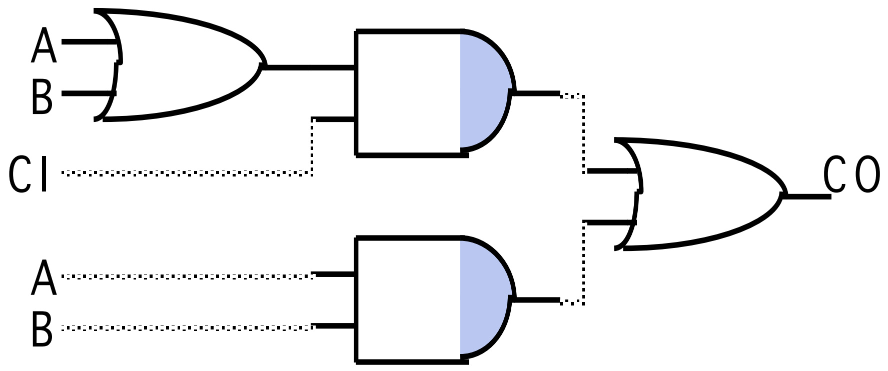




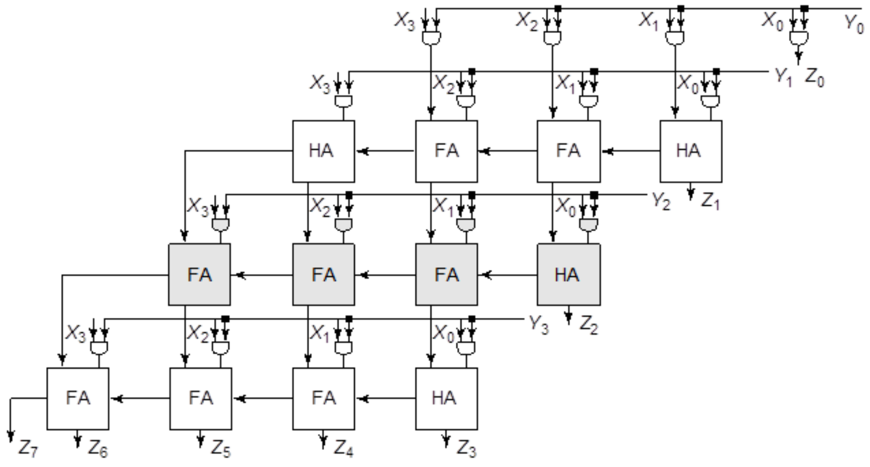
Use gates to build logic blocks

- Full Adder

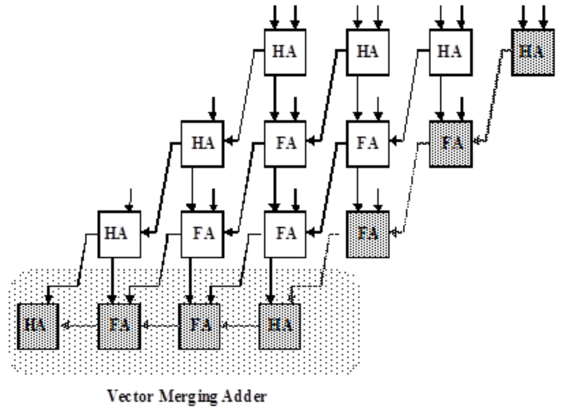




The Array Multiplier



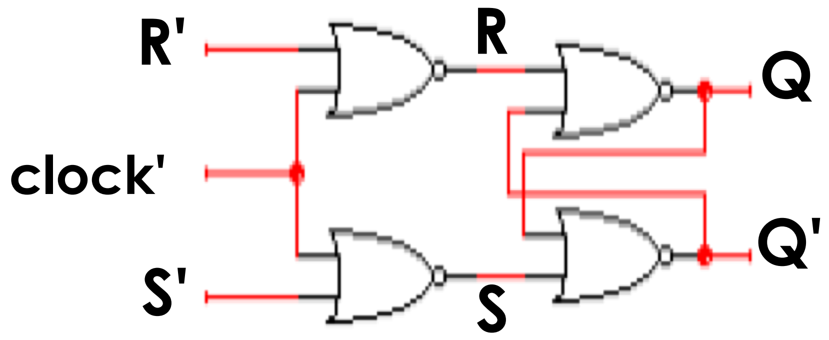
Carry-Save Multiplier



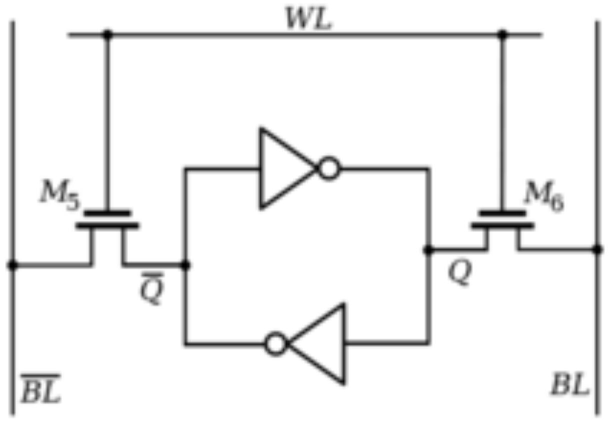
$$t_{mult} = (N-1)t_{carry} + (N-1)t_{and} + t_{merge}$$

Use gates to build memory element

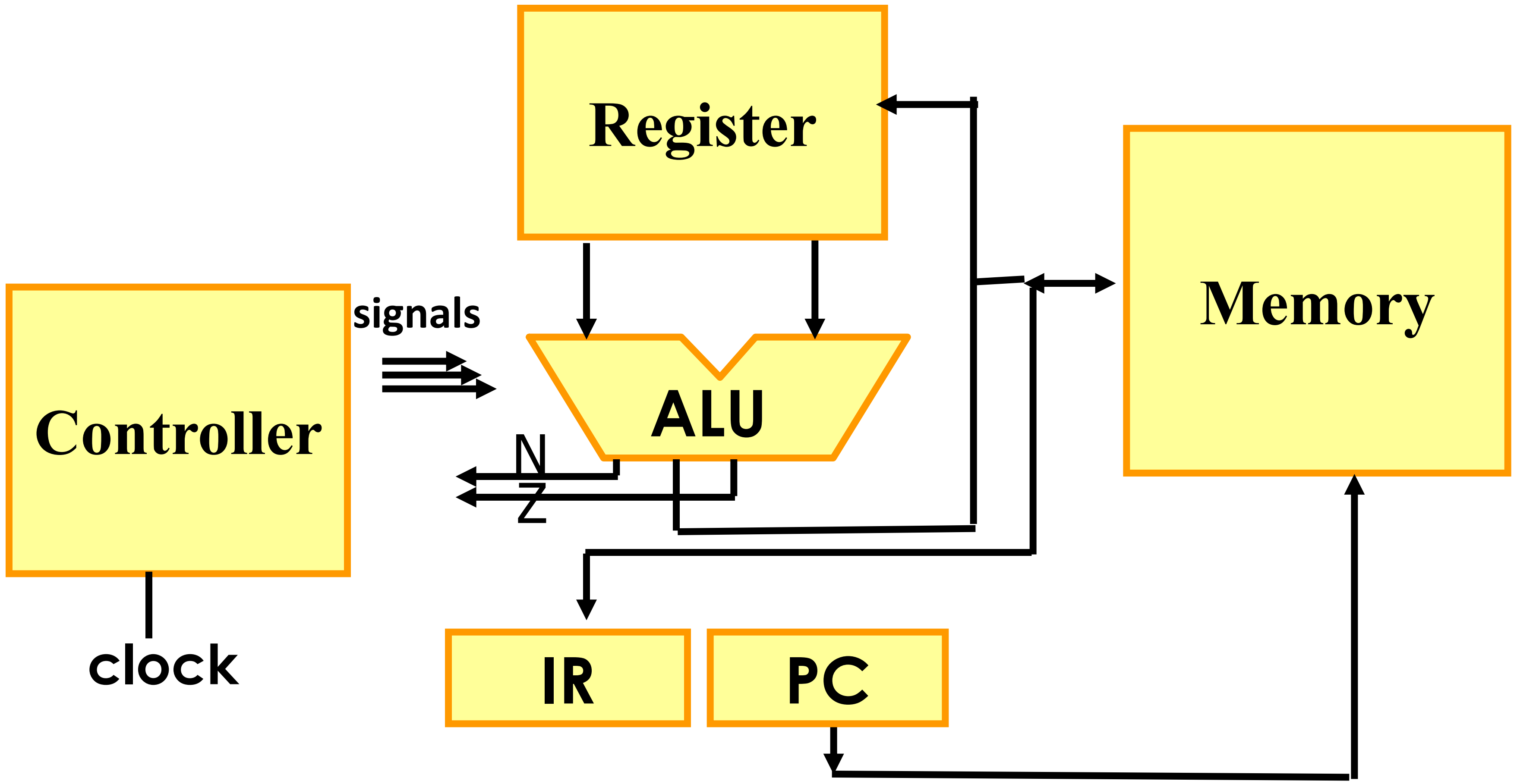
- Circuit to store 1-bit data
  - SR Latch



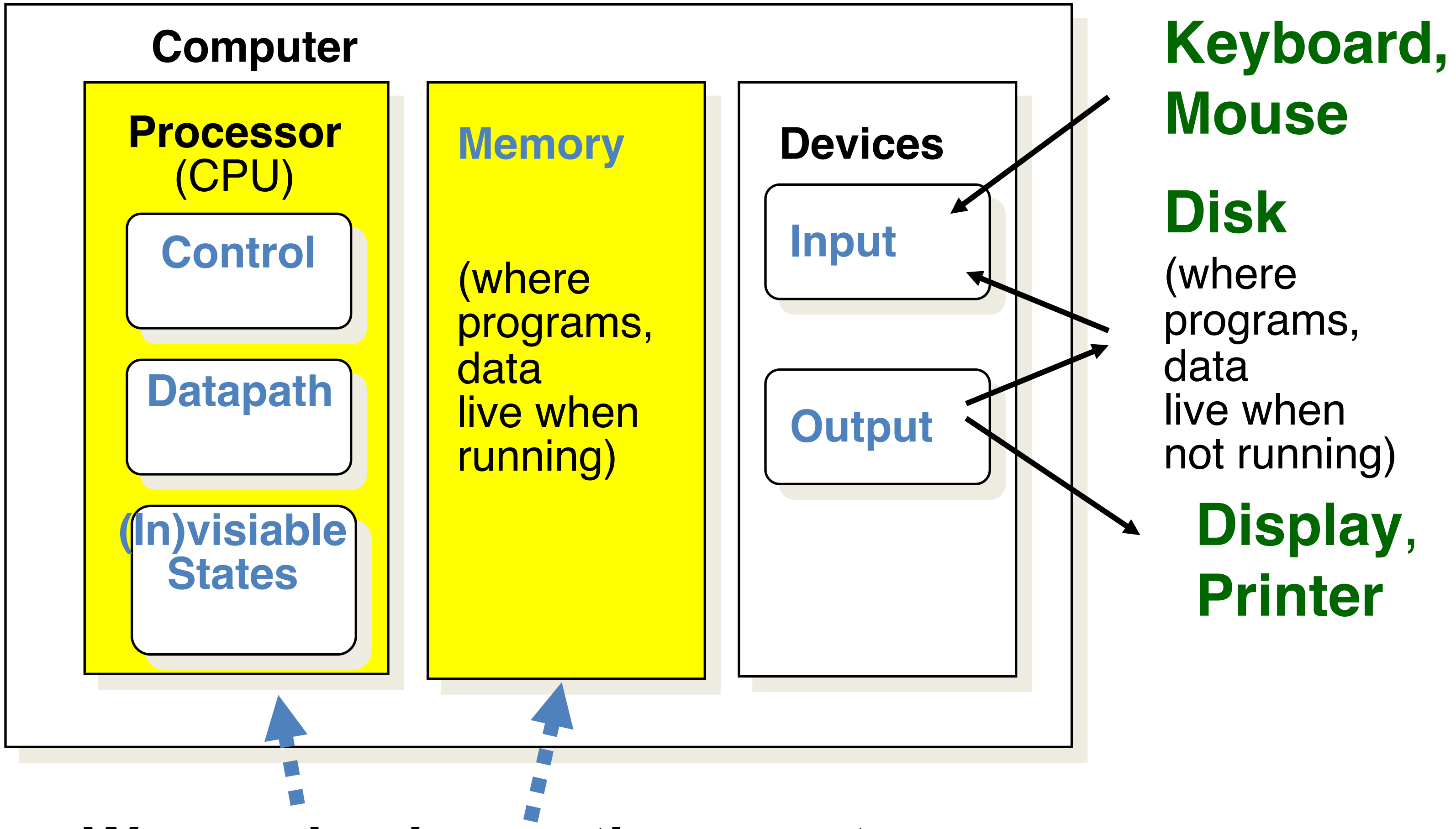
  - SRAM cell



Use logic blocks to build a CPU



Basic Organization of a Computer



We emphasize on these parts

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