2020 Digital IC Design Homework 2: Divider

NAME	Nguyen Vu Le Minh
Student ID	P76087099

Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Gate-level simulation time	2,686,986 (ns)

(your pre-sim result)

```
#       65524 data is correct
#       65525 data is correct
#       65526 data is correct
#       65527 data is correct
#       65528 data is correct
#       65529 data is correct
#       65530 data is correct
#       65531 data is correct
#       65532 data is correct
#       65533 data is correct
#       65534 data is correct
#       65535 data is correct
#       65536 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
```

(your post-sim result)

```
#       65524 data is correct
#       65525 data is correct
#       65526 data is correct
#       65527 data is correct
#       65528 data is correct
#       65529 data is correct
#       65530 data is correct
#       65531 data is correct
#       65532 data is correct
#       65533 data is correct
#       65534 data is correct
#       65535 data is correct
#       65536 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
```

Synthesis Result

Total logic elements	161 / 68,416 (< 1 %)
Total memory bit	0 / 1,152,000 (0 %)
Embedded multiplier 9-bit element	0 / 300 (0 %)

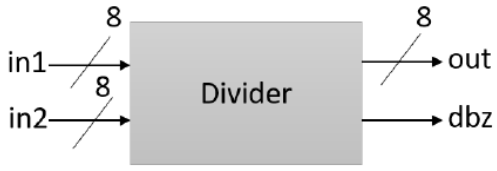
(your flow summary)

Flow Summary

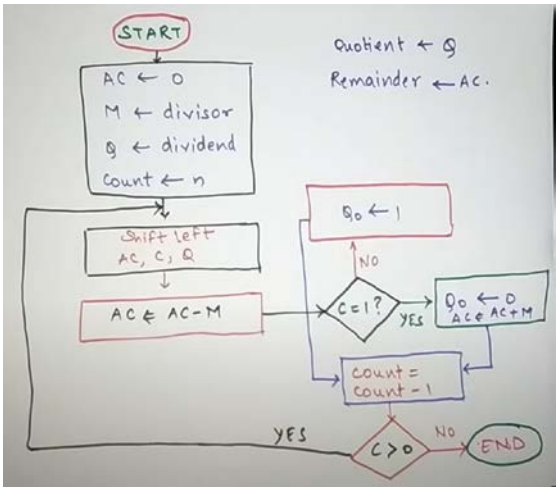
Flow Status	Successful - Sat Apr 11 23:33:51 2020
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	div
Top-level Entity Name	div
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	161 / 68,416 (< 1 %)
Total combinational functions	161 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	25 / 622 (4 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

The divider is a device that can be used to perform division. It can be usually classified into the signed divider or unsigned divider. In my design, I implement an 8-bit unsigned divider with combination both dataflow and behavior description.



First, my input includes in1, in2. The input in1 and in2 which are 8-bit binary, representation for dividend and divisor respectively. Besides, there are 2 output values that are out and dbz in my design. For dbz output, it's set as 1 when encounter divided-by-zero.



According to block overview and flowchart, I designed division with a temporary register, called as AC 8-bit binary. I also have a carry bit to memo overflow bit. In Full_Division function, the division is done by just left shift, subtract and adder operation. I implemented until quotient is 0 and it maybe maximum is 8 times because input is 8-bit.

I also edit the Clock Cycle is 41 in Test_bench file to decrease gate-level simulation time in post-sim.

```
`timescale 1ns / 10ps
`define CYCLE 41 // can be modified
module div_tb;
parameter width = 8;
```

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*