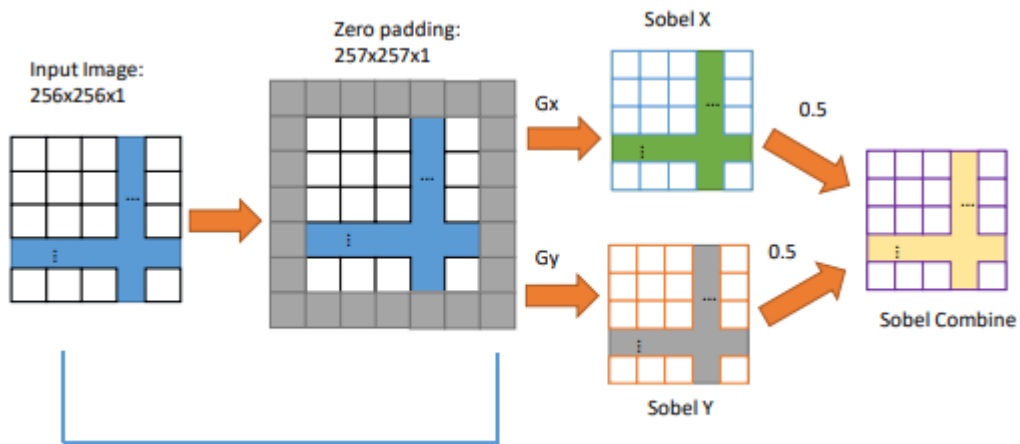


2020 Digital IC Design Homework 5: Sobel

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Simulation Result					
Functional simulation	A	Gate-level simulation	B	Gate-level simulation time	15729010867 (ps)
<pre>----- S U M M A R Y ----- : : Congratulations! Sobel X data have been generated successfully! The result is PASS!! : Congratulations! Sobel Y data have been generated successfully! The result is PASS!! : Congratulations! Sobel combine data have been generated successfully! The result is PASS!! : : ----- : : ** Note: \$finish : P:/2. Study/Semester 2/Digital IC DESIGN/Homework/HW5/00_Functional/ : Time: 13107500 ns Iteration: 0 Instance: /testfixture : : </pre>			<pre> : Congratulations! Sobel X data have been generated successfully! The result is PASS!! : Congratulations! Sobel Y data have been generated successfully! The result is PASS!! : FAIL!!! There are 11198 errors! in Sobel combine : ----- : : ** Note: \$finish : P:/2. Study/Semester 2/Digital IC DESIGN/Homework/HW5/03_GateLe : Time: 15729010867 ps Iteration: 0 Instance: /testfixture : : </pre>		
Synthesis Result					
Total logic elements			981 / 68,416 (1 %)		
Total memory bit			0 / 1,152,000 (0 %)		
Embedded multiplier 9-bit element			0 / 300 (0 %)		
<div><div>Flow Summary</div><div><div>Flow Status</div><div>Quartus II Version</div><div>Revision Name</div><div>Top-level Entity Name</div><div>Family</div><div>Device</div><div>Timing Models</div><div>Met timing requirements</div><div>Total logic elements</div><div>Total combinational functions</div><div>Dedicated logic registers</div><div>Total registers</div><div>Total pins</div><div>Total virtual pins</div><div>Total memory bits</div><div>Embedded Multiplier 9-bit elements</div><div>Total PLLs</div></div><div><div>Successful - Wed Jun 24 18:13:21 2020</div><div>10.0 Build 262 08/18/2010 SP 1 SJ Full Version</div><div>SOBEL</div><div>SOBEL</div><div>Cyclone II</div><div>EP2C70F896C8</div><div>Final</div><div>N/A</div><div>981 / 68,416 (1 %)</div><div>981 / 68,416 (1 %)</div><div>71 / 68,416 (< 1 %)</div><div>71</div><div>81 / 622 (13 %)</div><div>0</div><div>0 / 1,152,000 (0 %)</div><div>0 / 300 (0 %)</div><div>0 / 4 (0 %)</div></div></div>					
Description of your design					
<p>Sobel operator is one of the operators in image processing, also known as Sobel Federman operator or Sobe filter, which is often used to do edge detection in the field of image processing and computer vision. It performs a 2-D spatial gradient measurement on an image. Sobel is a discrete differentiation operator and it is used to compute an approximate absolute gradient magnitude at each pixel of an image for edge detection. In my homework, I implement an image edge detection system, use Gx and Gy to convolve the image to obtain the sobel_X image and sobel_Y image,</p>					

and then add sobel_X image and sobel_Y image together and divide by 2 for the output image of sobel_Combine.



The data in tb is zero padding image data.

In my circuit, I use csel to read or write results to memory, and separate stage to calculate Sobel_X, Sobel_Y and Sobel_Combine. After that I will write my result to memory to check with testbench.

After the calculation of Sobel_X, Sobel_Y, Sobel_Combine are finished, the busy signal set to 0 to done operation.

In the Quatus synthesis, I set period time is 50 in Sobel.sdc file

```
create_clock -period 50 [get_ports clk]
```

In the gate level processing, I set Cycle is 24.0 that is minimum value to operation my design and I receive runtime is 15729010867 (ps)

```
`timescale 1ns/10ps
`define CYCLE      24.0          // Modify your clock
`define End_CYCLE 1000000000    // Modify
`define PAT        "img.dat"
`define L0_EXP0    "img_X.dat"
`define L0_EXP1    "img_Y.dat"
`define L0_EXP2    "img_Combine.dat"
```

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (gate-level simulation time in ns)*