HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
FACULTY OF COMPUTER SCIENCE AND ENGINEERING

LSI LOGIC DESIGN

LAB 2 - SYNTHESIS

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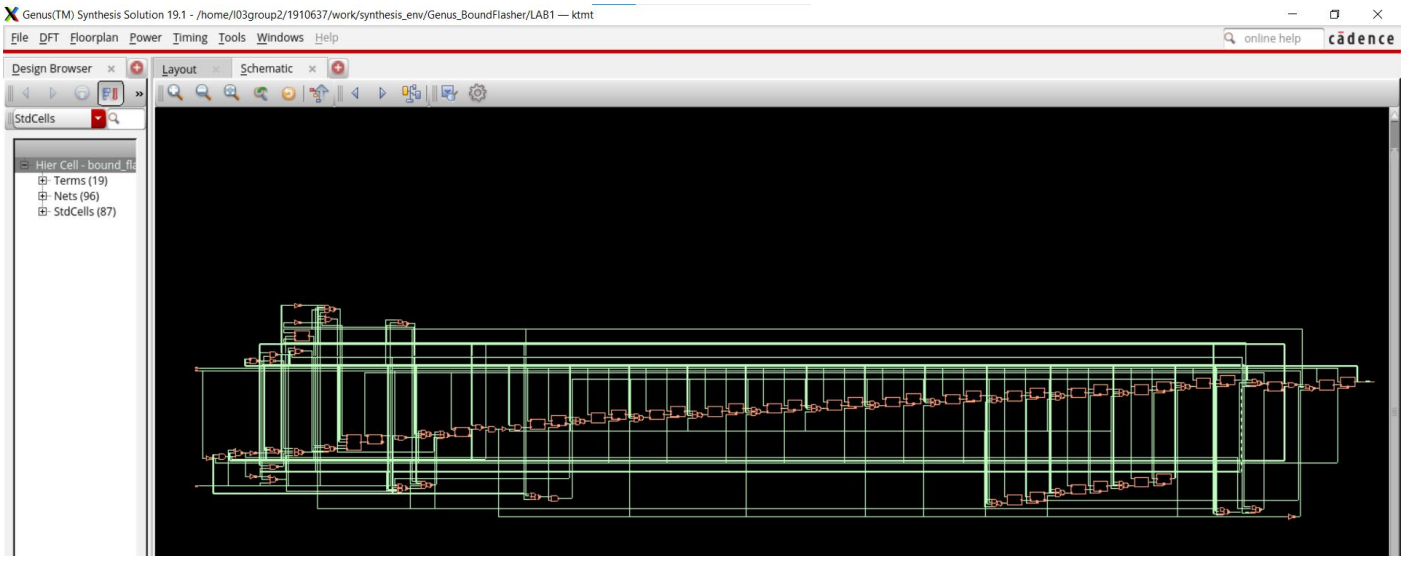
The Result and report is stored in this github link:
--> Link Github: [Lab2_Synthesis_L01Group4]

☞NETLIST:



☞MAXIMUM DESIGN FREQUENCY:

- We know that in order to find maximum design frequency -> we need to find mim period.

- Therefore, we modify the period in the file **bound_flasher_gate.sdc** in folder **constraints:**

```
3. 10.28.8.71 (l01group4)

# set the current design
current_design bound_flasher
create_clock -name "clk" -add -period 0.62 -waveform {0.0 0.31} [get_ports clock]

set_input_delay -clock [get_clocks clk] -add_delay 0.31 [get_ports flick]
set_input_delay -clock [get_clocks clk] -add_delay 0.31 [get_ports reset]
set_output_delay -clock [get_clocks clk] -add_delay 0.31 [get_ports led_out]

set_max_fanout 15.000 [current_design]
set_max_transition 1.2 [current_design]
~
```

=> We finally found the min period -> max design frequency.
This result can be found in file final_qor.rpt.

```
Clock Period
-------------
clk    620.0


  Cost    Critical         Violating
 Group   Path Slack  TNS     Paths
-----------------------------------
clk           0.1   0.0         0
default    No paths   0.0
-----------------------------------
Total                0.0         0
```