**HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY**

**FACULTY OF COMPUTER SCIENCE AND ENGINEERING**

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**LSI LOGIC DESIGN**

**LAB 2 - SYNTHESIS**

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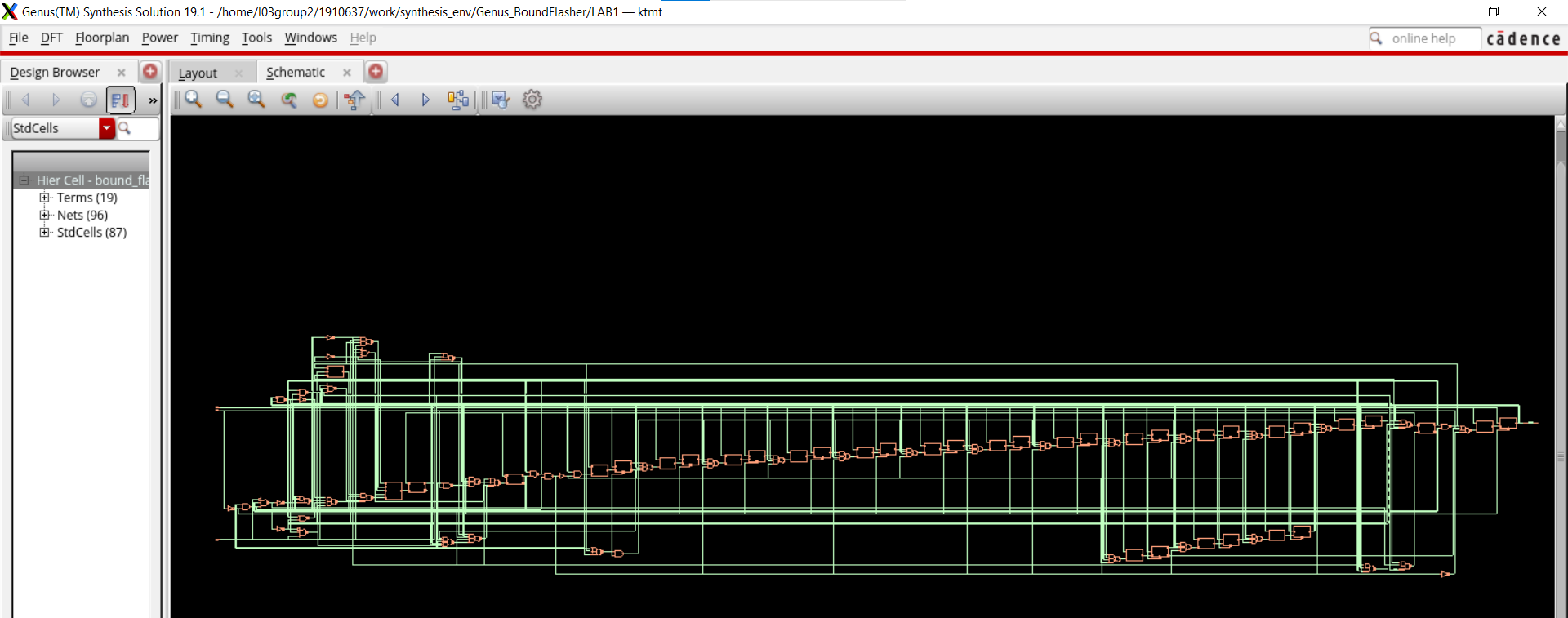
Lê Thanh Tiến - 1912196

*- 03/2023 -*

**The Result and report is stored in this github link:**

**-->** Link Github**: [Lab2\_Synthesis\_L01Group4](https://github.com/minhtritran2308/LSI/tree/master/Lab02_Synthesis)**

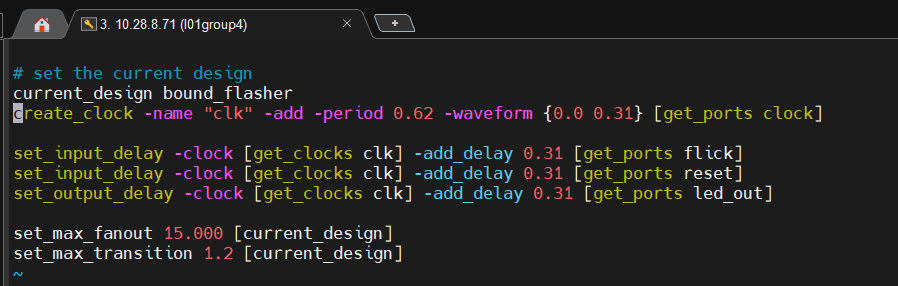
**☞NETLIST:**



**☞MAXIMUM DESIGN FREQUENCY:**

- We know that in order to find maximum design frequency -> we need to find mim period.

- Therefore, we modify the period in the file **bound\_flasher\_gate.sdc** in folder **constraints:**



**=>** We finally found the min period -> max design frequency.

**This result can be found in file final\_qor.rpt.**

