

Báo cáo tuần 3

A, Full adder

1. Đặc tả chức năng

- Bảng chân lý

Inputs			Outputs	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Sum

Cin \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$\begin{aligned} \text{Sum} &= \overline{A} \cdot \overline{B} \cdot C_{in} + \overline{A} \cdot B \cdot C_{in} + A \cdot \overline{B} \cdot C_{in} + A \cdot B \cdot C_{in} \\ &= C_{in} (\overline{A} \cdot \overline{B} + \overline{A} \cdot B + A \cdot \overline{B} + A \cdot B) \\ &= C_{in} (\overline{A} \cdot (\overline{B} + B) + A \cdot (\overline{B} + B)) \\ &= C_{in} (\overline{A} + A) \\ &= C_{in} \end{aligned}$$

Carry

Cin \ AB	00	01	11	10
0	0	0	0	0
1	0	1	1	1

$$\begin{aligned} \text{Carry} &= \overline{A} \cdot B \cdot C_{in} + A \cdot \overline{B} \cdot C_{in} + A \cdot B \cdot C_{in} \\ &= C_{in} (\overline{A} \cdot B + A \cdot \overline{B} + A \cdot B) \\ &= C_{in} (A \oplus B + A \cdot B) \\ &= C_{in} (A \oplus B) \end{aligned}$$

2. Mô tả mạch bằng ModelSim

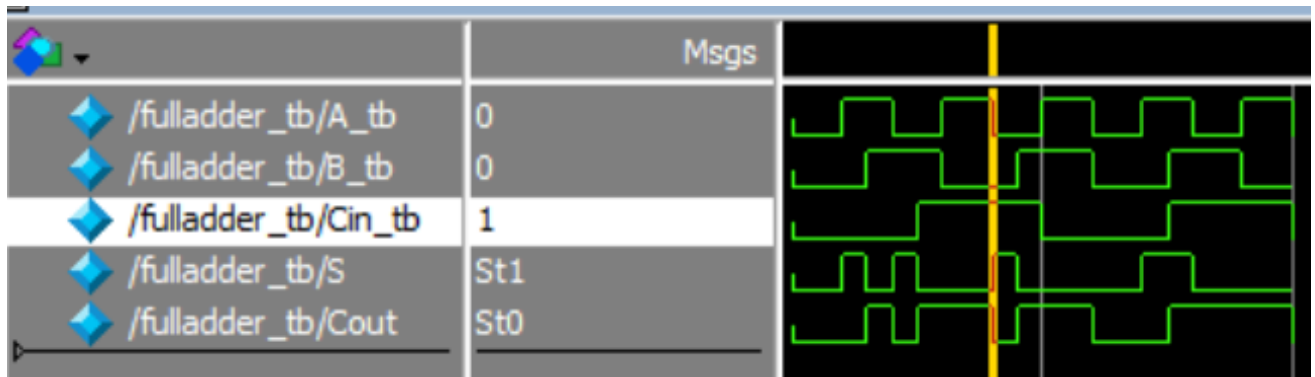
- Full_adder.sv

```
module fulladder (  
    input A, B, Cin,  
    output S, Cout  
);  
  
    assign S = A ^ B ^ Cin;  
    assign Cout = (A & B) | Cin & (A ^ B);  
endmodule
```

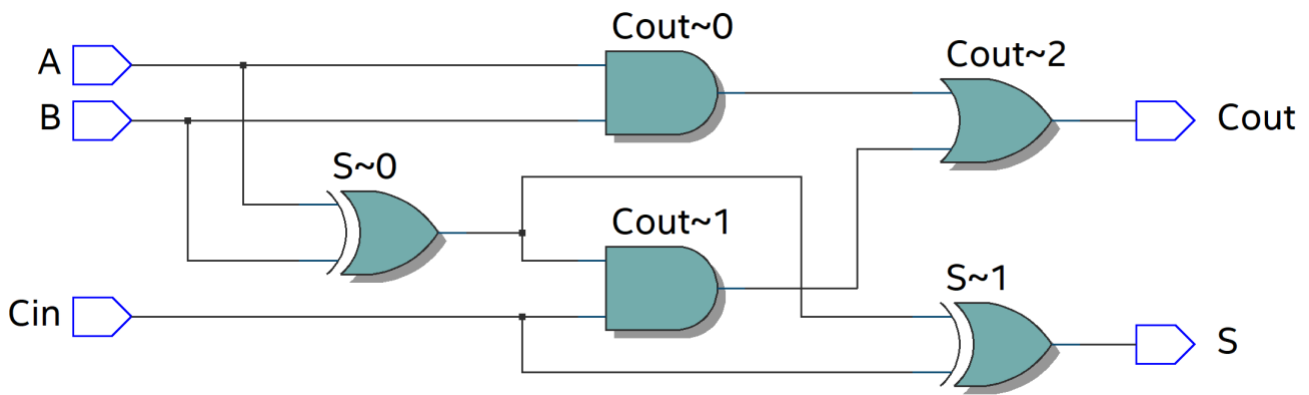
- Full_adder_tb.sv

```
`timescale 1ns/1ns  
  
module fulladder_tb;  
    reg A_tb, B_tb, Cin_tb;  
    wire S, Cout;  
  
    fulladder uut (  
        .A(A_tb),  
        .B(B_tb),  
        .Cin(Cin_tb),  
        .S(S),  
        .Cout(Cout)  
    );  
  
    always begin  
        A_tb = 0;  
        #10 A_tb = 1;  
        #10;  
    end  
  
    always begin  
        B_tb = 0;  
        #15 B_tb = 1;  
        #15;  
    end  
  
    always begin  
        Cin_tb = 0;  
        #25 Cin_tb = 1;  
        #25;  
    end  
  
    initial begin  
        #200;  
        $finish;  
    end  
endmodule
```

3. Mô tả hành vi

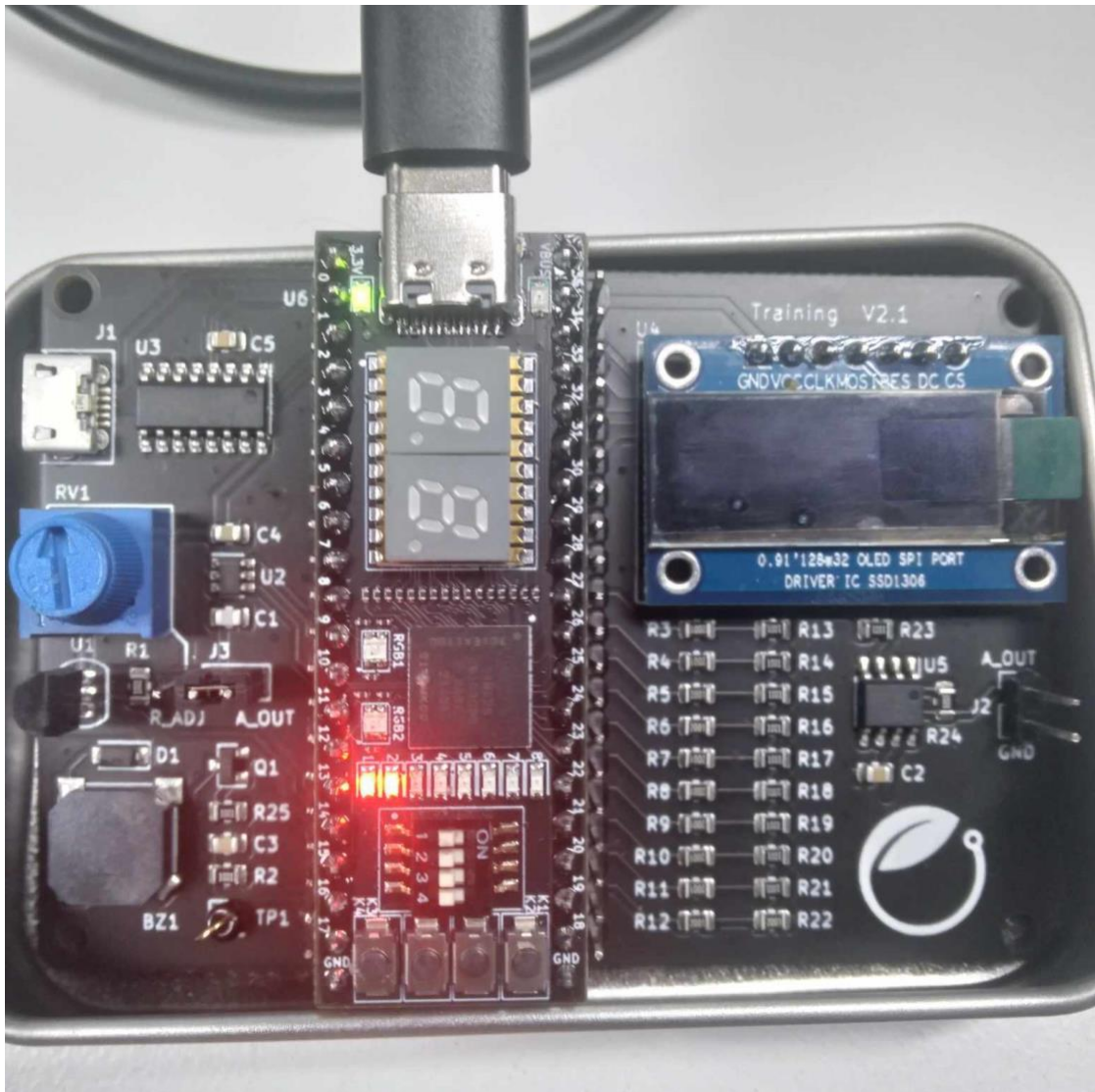


4. Chạy trên Quartus



5. Chạy kiểm thử trên Board mạch

Named: "							
	Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in	A	Input	PIN_J12	6	B6_N0	PIN_P8	2.5 V (default)
in	B	Input	PIN_H11	6	B6_N0	PIN_R3	2.5 V (default)
in	Cin	Input	PIN_H12	6	B6_N0	PIN_L8	2.5 V (default)
out	Cout	Output	PIN_N14	5	B5_N0	PIN_N1	2.5 V (default)
out	S	Output	PIN_N15	5	B5_N0	PIN_P4	2.5 V (default)



- Giải thích:
 - +) Đặt A là Switch 1
 - +) Đặt B là Switch 2
 - +) Đặt Cin là Switch 3
 - +) Đặt S là LED 1
 - +) Đặt Cout là LED 2
- Khi đặt $A = 0, B = 0, Cin = 0$ thì $S = 0$ (LED 1 sáng), $Cout = 0$ (LED 2 sáng)

B. Full Subtractor

1. Đặc tả chức năng
- Bảng chân lý

Inputs			Output	
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Difference

Bin	0	1
AB		
00	0	1
01	1	0
11	0	1
10	1	0

$$\begin{aligned}
 D_{\text{diff}} &= \overline{A}B \cdot \text{Bin} + \overline{A}B \cdot \overline{\text{Bin}} + A \cdot B \cdot \text{Bin} \\
 &\quad + A \cdot B \cdot \overline{\text{Bin}} \\
 &= \text{Bin} (\overline{A}B + AB) + \overline{\text{Bin}} (\overline{A}B + AB) \\
 &= \text{Bin} (A \oplus B) + \overline{\text{Bin}} (A \oplus B) \\
 &= \text{Bin} \oplus A \oplus B
 \end{aligned}$$

Borrow

Bin	0	1
AB		
00	0	1
01	1	1
11	0	1
10	0	0

$$\begin{aligned}
 B_{\text{out}} &= \overline{A}B + \overline{A}B \cdot \text{Bin} + AB \cdot \text{Bin} \\
 &= \overline{A}B + \text{Bin} (\overline{A}B + AB) \\
 &= \overline{A}B + \text{Bin} (A \oplus B)
 \end{aligned}$$

2. Mô tả mạch bằng ModelSim

- Full_subtractor.sv

```
module full_subtractor (  
    input a,  
    input b,  
    input bin,  
    output d,  
    output bout  
);  
  
    assign d = a ^ b ^ bin;  
    assign bout = (~a & b) | (bin & (~a ^ b));  
endmodule
```

- Full_subtractor_tb.sv


```

`timescale 1ns/1ns

module full_subtractor_tb;
    reg a_tb, b_tb, bin_tb;
    wire d, bout;
    full_subtractor uut (
        .a(a_tb),
        .b(b_tb),
        .bin(bin_tb),
        .d(d),
        .bout(bout)
    );
    always begin
        a_tb = 0;
        #10 a_tb = 1;
        #10;
    end

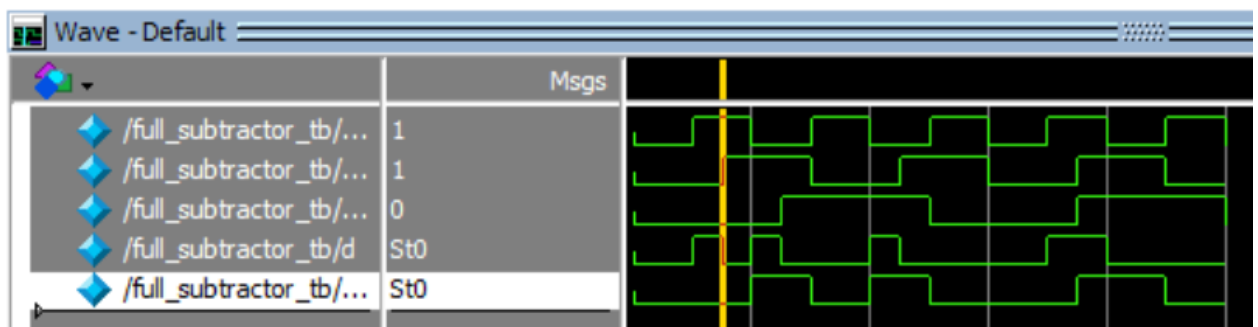
    always begin
        b_tb = 0;
        #15 b_tb = 1;
        #15;
    end

    always begin
        bin_tb = 0;
        #25 bin_tb = 1;
        #25;
    end

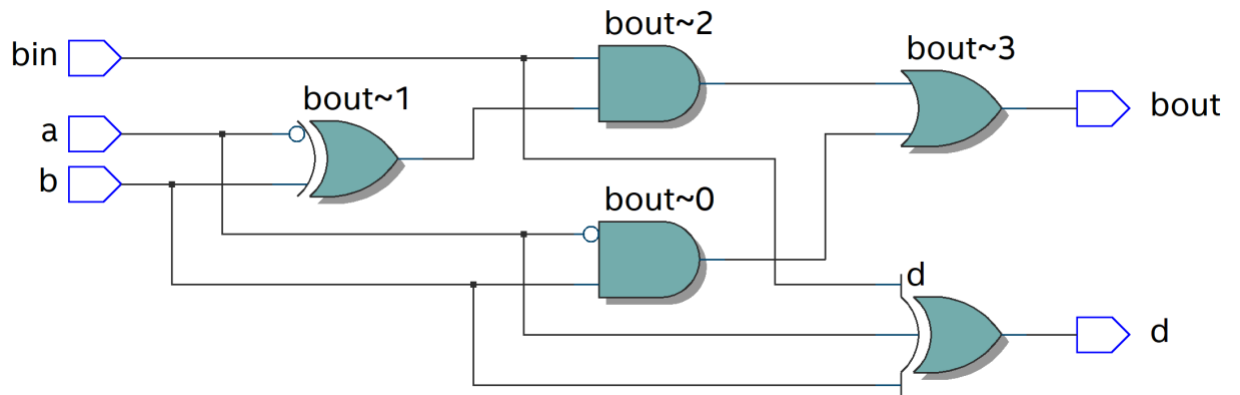
    initial begin
        #200;
        $finish;
    end
endmodule

```

3. Mô tả hành vi



4. Chạy trên Quartus



5. Chạy kiểm thử trên Board mạch

Named: * Edit: PIN_N15							
Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	
<input type="checkbox"/> a	Input	PIN_J12	6	B6_N0	PIN_R3	2.5 V (default)	
<input type="checkbox"/> b	Input	PIN_H11	6	B6_N0	PIN_L8	2.5 V (default)	
<input type="checkbox"/> bin	Input	PIN_H12	6	B6_N0	PIN_P8	2.5 V (default)	
<input type="checkbox"/> bout	Output	PIN_N14	5	B5_N0	PIN_N1	2.5 V (default)	
<input type="checkbox"/> d	Output	PIN_N15	5	B5_N0	PIN_P4	2.5 V (default)	

C. NAND

1. Đặc tả chức năng

- Bảng chân lý

Inputs			Output
A	B	C	N
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

- Công thức: $N = \overline{ABC}$

2. Mô tả mạch bằng ModelSim

- NAND.sv

```

module NAND (
    input a, b, c,
    output n
);
    assign n = ~(a & b & c);
endmodule

```

- NAND_tb.sv

```

`timescale 1ns/1ns

module NAND_tb;
    reg a_tb, b_tb, c_tb;
    wire n;
    NAND uut (
        .a(a_tb),
        .b(b_tb),
        .c(c_tb),
        .n(n)
    );
    always begin
        a_tb = 0;
        #10 a_tb = 1;
        #10;
    end

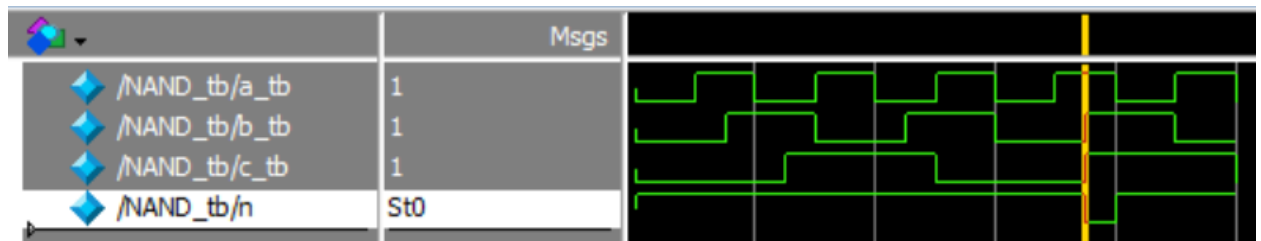
    always begin
        b_tb = 0;
        #15 b_tb = 1;
        #15;
    end

    always begin
        c_tb = 0;
        #25 c_tb = 1;
        #25;
    end

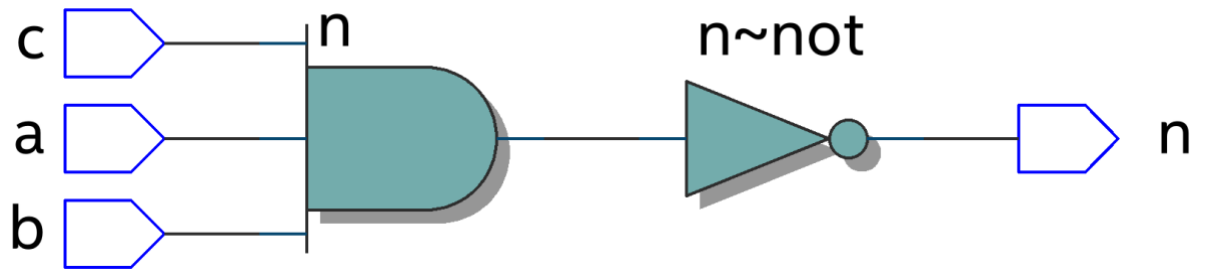
    initial begin
        #200;
        $finish;
    end
end
endmodule

```

3. Mô tả hành vi



4. Chạy trên Quartus



5. Kiểm thử trên Board mạch

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in a	Input	PIN_J12	6	B6_N0	PIN_R7	2.5 V (default)
in b	Input	PIN_H11	6	B6_N0	PIN_A5	2.5 V (default)
in c	Input	PIN_H12	6	B6_N0	PIN_P8	2.5 V (default)
out n	Output	PIN_N15	5	B5_N0	PIN_K4	2.5 V (default)
<<new node>>						

D . Bộ ghép kênh 2:1

- Đặc tả chức năng
- Bảng chân lý

Inputs			Output
A	X1	X2	Y
0	X1	X2	X1
1	X1	X2	X2

- Công thức : $Y = \bar{A} X_1 + A X_2$

2. Mô tả mạch bằng ModelSim

- Mul_2_1.sv

```

module Mul_2_1 (
    input a, x1, x2,
    output y
);

    assign y = (~a & x1) | (a & x2);
endmodule
  
```

- Mul_2_1_tb.sv

```
`timescale 1ns/1ns

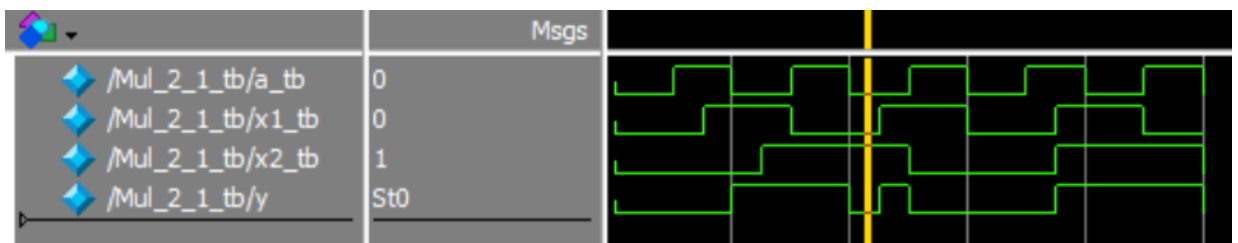
module Mul_2_1_tb;
    reg a_tb, x1_tb, x2_tb;
    wire y;
    Mul_2_1 uut (
        .a(a_tb),
        .x1(x1_tb),
        .x2(x2_tb),
        .y(y)
    );
    always begin
        a_tb = 0;
        #10 a_tb = 1;
        #10;
    end

    always begin
        x1_tb = 0;
        #15 x1_tb = 1;
        #15;
    end

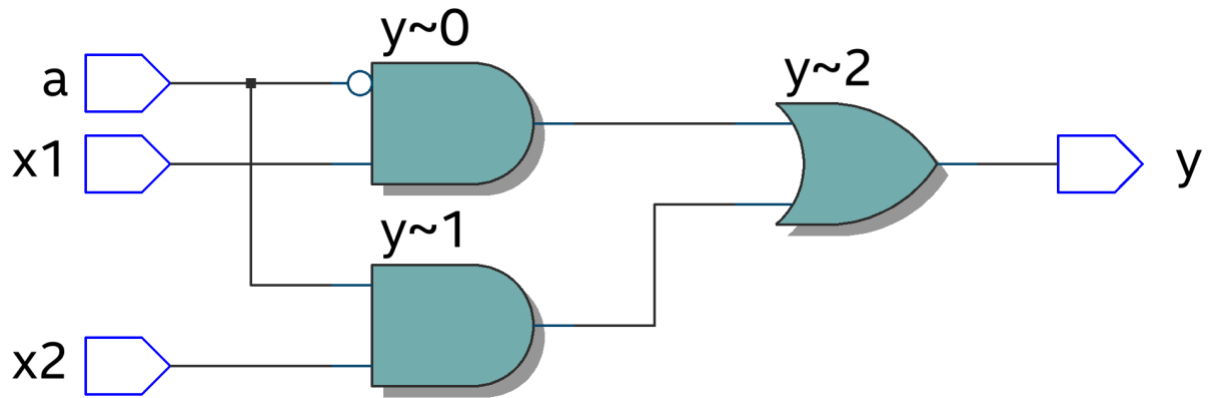
    always begin
        x2_tb = 0;
        #25 x2_tb = 1;
        #25;
    end

    initial begin
        #200;
        $finish;
    end
endmodule
```

3. Mô tả hành vi



4. Chạy trên Quartus



5. Chạy kiểm thử trên Board mạch

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
in a	Input	PIN_J12	6	B6_N0	PIN_P8	2.5 V (default)
in x1	Input	PIN_J9	5	B5_N0	PIN_A5	2.5 V (default)
in x2	Input	PIN_K14	5	B5_N0	PIN_R7	2.5 V (default)
out y	Output	PIN_N15	5	B5_N0	PIN_K4	2.5 V (default)

E . Bộ ghép kênh 4:1

1. Đặc tả chức năng

- Bảng chân lý

Inputs						Output
A	B	X0	X1	X2	X3	Y
0	0	X0	X1	X2	X3	X0
0	1	X0	X1	X2	X3	X1
1	0	X0	X1	X2	X3	X2
1	1	X0	X1	X2	X3	X3

- Công thức

$$Y = \overline{A}\overline{B}X_0 + \overline{A}BX_1 + A\overline{B}X_2 + ABX_3$$

2. Mô tả mạch bằng ModelSim

- Mul_4_1.sv

```

module Mul_4_1 (
    input a, b, x0, x1, x2, x3,
    output y
);

    assign y = (~(a & b) & x0) | ((~b & a) & x1) | ((~a & b) & x2) | ((a & b) & x3);

endmodule

```

- Mul_4_1_tb.sv

```

`timescale 1ns/1ns

module Mul_4_1_tb;
    reg a_tb, b_tb, x0_tb, x1_tb, x2_tb, x3_tb;
    wire y;
    Mul_4_1 uut (
        .a(a_tb),
        .b(b_tb),
        .x0(x0_tb),
        .x1(x1_tb),
        .x2(x2_tb),
        .x3(x3_tb),
        .y(y)
    );
    always begin
        a_tb = 0;
        #10 a_tb = 1;
        #10;
    end

    always begin
        b_tb = 0;
        #15 b_tb = 1;
        #15;
    end

    always begin
        x0_tb = 0;
        #25 x0_tb = 1;
        #25;
    end

    always begin
        x1_tb = 0;
        #30 x1_tb = 1;
        #25;
    end

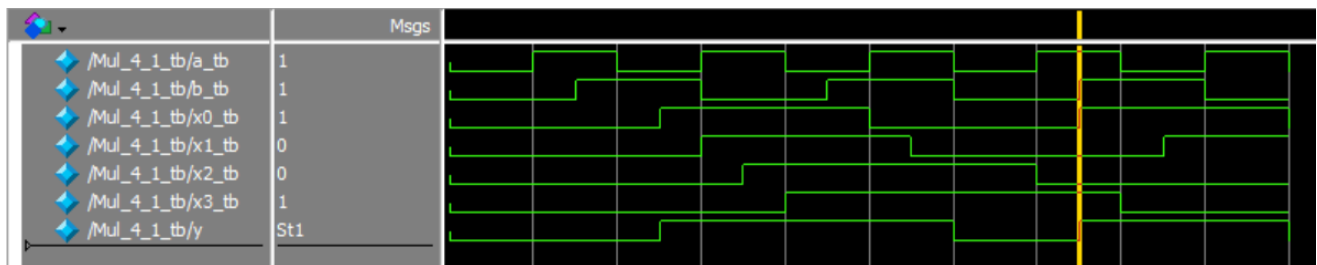
    always begin
        x2_tb = 0;
        #35 x2_tb = 1;
        #35;
    end

    always begin
        x3_tb = 0;
        #40 x3_tb = 1;
        #40;
    end

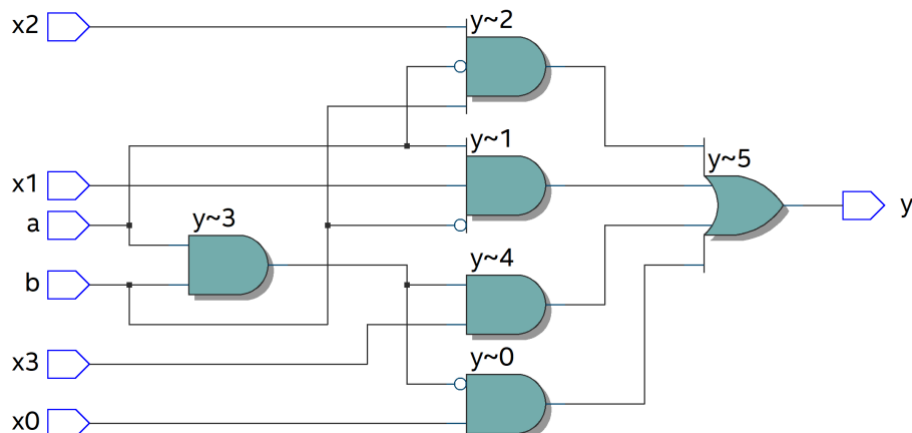
    initial begin
        #200;
        $finish;
    end
endmodule

```








3. Mô tả hành vi



4. Chạy trên Quartus



5. Chạy kiểm thử trên Board mạch

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
 a	Input	PIN_J12	6	B6_N0	PIN_P1	2.5 V (default)
 b	Input	PIN_H11	6	B6_N0	PIN_M5	2.5 V (default)
 x0	Input	PIN_J9	5	B5_N0	PIN_L7	2.5 V (default)
 x1	Input	PIN_K14	5	B5_N0	PIN_P4	2.5 V (default)
 x2	Input	PIN_J11	5	B5_N0	PIN_R3	2.5 V (default)
 x3	Input	PIN_J14	5	B5_N0	PIN_M4	2.5 V (default)
 y	Output	PIN_N15	5	B5_N0	PIN_P2	2.5 V (default)