Digital (Design) logic and Computer Organisation

CIA - 5

Design a 5 bit +ve edge trigger MOD 13 counter.

Answer:

5 bit +ve edge trigger MOD 13 counter
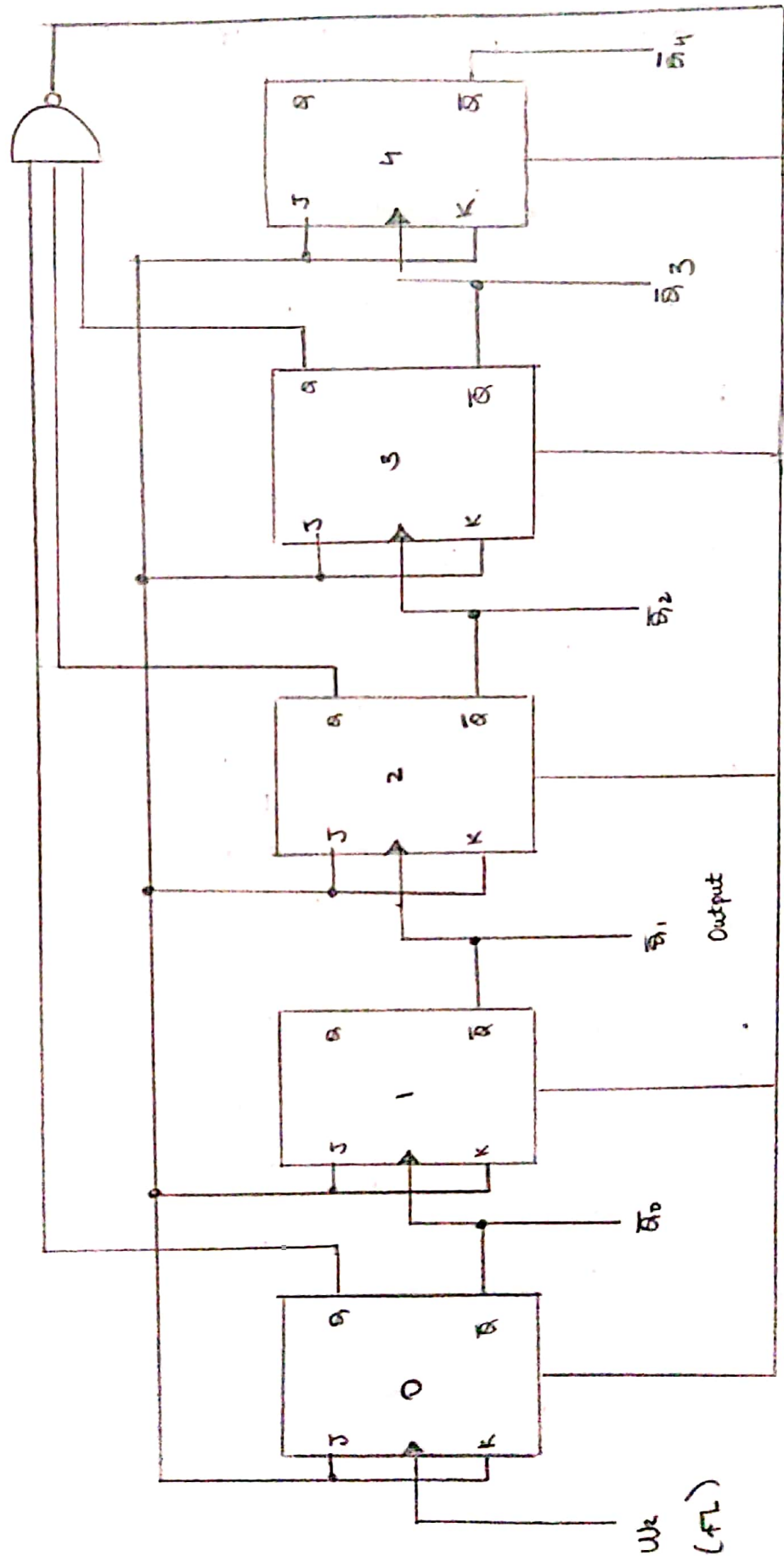
Truthtable :

| Clk | $Q_4$ | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|-----|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0 | 0 | 1 | 0 | 1 |
| 6 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0 | 0 | 1 | 1 | 1 |
| 8 | 0 | 1 | 0 | 0 | 0 |
| 9 | 0 | 1 | 0 | 0 | 1 |
| 10 | 0 | 1 | 0 | 1 | 0 |
| 11 | 0 | 1 | 0 | 1 | 1 |
| 12 | 0 | 1 | 1 | 0 | 0 |

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Reset value : $Q_0 = Q_2 = Q_3 = 1$

Block diagram 5 bit Positive edge Jwigger Mod 13 counter

Timing Diagram: