C

1. ADD R1,R2,R3

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	11	x	x	x	x	x
2	11	x	0	0	x	x
3	11	0	0	0	x	x
4	11	0	0	0	x	0
5	11	0	0	0	1	0

2. ADDI R3,IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	0	0	1	x	x
4	10	0	0	1	x	0
5	10	0	0	1	1	0

3. SUB R1,R2,R3

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	11	x	x	x	x	x
2	11	x	0	0	x	x
3	11	1	0	0	x	x
4	11	1	0	0	x	0
5	11	1	0	0	1	0

4. SUBI R1,IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	1	0	1	x	x
4	10	1	0	1	x	0
5	10	1	0	1	1	0

5. AND R1,R2,R3

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	11	x	x	x	x	x
2	11	x	0	0	x	x
3	11	101	0	0	x	x
4	11	101	0	0	x	0

5	11	101	0	0	1	0

6. ANDI R1,IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	101	0	1	x	x
4	10	101	0	1	x	0
5	10	101	0	1	1	0

7. OR R1,R2,R3

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	11	x	x	x	x	x
2	11	x	0	0	x	x
3	11	111	0	0	x	x
4	11	111	0	0	x	0
5	11	111	0	0	1	0

8. OR R1,IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	111	0	1	x	x
4	10	111	0	1	x	0
5	10	111	0	1	1	0

9. XOR R1,R2,R3

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	11	x	x	x	x	x
2	11	x	0	0	x	x
3	11	1000	0	0	x	x
4	11	1000	0	0	x	0
5	11	1000	0	0	1	0

10. XORI R1,IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB

1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	1000	0	1	x	x
4	10	1000	0	1	x	0
5	10	1000	0	1	1	0

11. NOT R1

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	x	x	x
3	10	110	0	x	x	x
4	10	110	0	x	x	0
5	10	110	0	x	1	0

12. SLA R1,R2

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	x	x	x
3	10	11	0	x	x	x
4	10	11	0	x	x	0
5	10	11	0	x	1	0

13. SLAI R1,IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	11	0	1	x	x
4	10	11	0	1	x	0
5	10	11	0	1	1	0

14. SRA R1,R2

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	x	x	x
3	10	1001	0	x	x	x
4	10	1001	0	x	x	0
5	10	1001	0	x	1	0

15. SRAI R1,IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	1001	0	1	x	x
4	10	1001	0	1	x	0
5	10	1001	0	1	1	0

16. SRL R1,R2

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	x	x	x
3	10	100	0	x	x	x
4	10	100	0	x	x	0
5	10	100	0	x	1	0

17. SRLI R1,IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	100	0	1	x	x
4	10	100	0	1	x	0
5	10	100	0	1	1	0

18. LD R1,SHAMT(R2)

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	0	0	1	x	x
4	10	0	0	1	x	1
5	10	0	0	1	1	1

19. ST R1,SHAMT(R2)

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	11	x	x	x	x	x
2	11	x	0	1	x	x
3	11	0	0	1	x	x
4	11	0	0	1	x	x
5	11	0	0	1	0	x

20. LDSP SP,SHAMT(R2)

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	0	0	1	x	x
4	10	0	0	1	x	x
5	10	0	0	1	1	x

21. STSP SP,SHAMT(R2)

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	1	x	x
3	10	0	0	1	x	x
4	10	0	0	1	x	x
5	10	0	0	1	0	x

22. BR IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	0	x	x	x	x	x
2	0	x	x	x	x	x
3	0	x	x	x	x	x
4	0	x	x	x	x	x
5	0	x	x	x	0	x

23. BMI R1, IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	x	x	x
3	10	10	0	x	x	x
4	10	10	0	x	x	x
5	10	10	0	x	0	x

24. BPL R1, IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	x	x	x

3	10	10	0	x	x	x
4	10	10	0	x	x	x
5	10	10	0	x	0	x

25. BZ R1, IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	10	x	x	x	x	x
2	10	x	0	x	x	x
3	10	10	0	x	x	x
4	10	10	0	x	x	x
5	10	10	0	x	0	x

26. PUSH R1

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	1	x	x	x	x	x
2	1	x	1	x	x	x
3	1	x	1	x	x	x
4	1	x	1	x	x	x
5	1	x	1	x	0	x

27. POP R1

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	0	x	x	x	x	x
2	0	x	1	1	x	x
3	0	0	1	1	x	x
4	0	0	1	1	x	1
5	0	0	1	1	1	1

28. CALL IMM

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	0	x	x	x	x	x
2	0	x	1	x	x	x
3	0	x	1	x	x	x
4	0	x	1	x	x	x
5	0	x	1	x	0	x

29. RET

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	0	x	x	x	x	x
2	0	x	1	1	x	x
3	0	0	1	1	x	x
4	0	0	1	1	x	x
5	0	0	1	1	0	x

30. MOVE R1,R2

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	11	x	x	x	x	x
2	11	x	0	0	x	x
3	11	0	0	0	x	x
4	11	0	0	0	x	0
5	11	0	0	0	1	0

31. HALT

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	0	x	x	x	x	x
2	0	x	x	x	x	x
3	0	x	x	x	x	x
4	0	x	x	x	x	x
5	0	x	x	x	0	x

32. NOP

	Readreg	ALUop	MUXA1	MUXA2	Wreg	MUXWB
1	0	x	x	x	x	x
2	0	x	x	x	x	x
3	0	x	x	x	x	x
4	0	x	x	x	x	x
5	0	x	x	x	0	x

ONTROL SIGNALS

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0

0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch

x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
10	0	x	0
10	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
1	0	0	0
1	0	0	0

RWMem	LoadSP	MUXMemWrite	branch
x	11	x	0
x	11	x	0
x	11	x	0
10	11	x	0
10	11	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
1	0	1	0
1	0	1	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	1
x	0	x	1
x	0	x	1
0	0	x	1
0	0	x	1

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	10
x	0	x	10
x	0	x	10
0	0	x	10
0	0	x	10

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	10
x	0	x	10

x	0	x	10
0	0	x	10
0	0	x	10

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	10
x	0	x	10
x	0	x	10
0	0	x	10
0	0	x	10

RWMem	LoadSP	MUXMemWrite	branch
x	10	x	0
x	10	x	0
x	10	x	0
1	10	0	0
1	10	0	0

RWMem	LoadSP	MUXMemWrite	branch
x	1	x	0
x	1	x	0
x	1	x	0
10	1	x	0
10	1	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	10	x	11
x	10	x	11
x	10	x	11
1	10	1	11
1	10	1	11

RWMem	LoadSP	MUXMemWrite	branch
x	1	x	100
x	1	x	100
x	1	x	100
10	1	x	100
10	1	x	100

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	101
x	0	x	101
x	0	x	101
0	0	x	101
0	0	x	101

RWMem	LoadSP	MUXMemWrite	branch
x	0	x	0
x	0	x	0
x	0	x	0
0	0	x	0
0	0	x	0