提 纲

1 开源芯片的缘起

2 RISC-V开源芯片

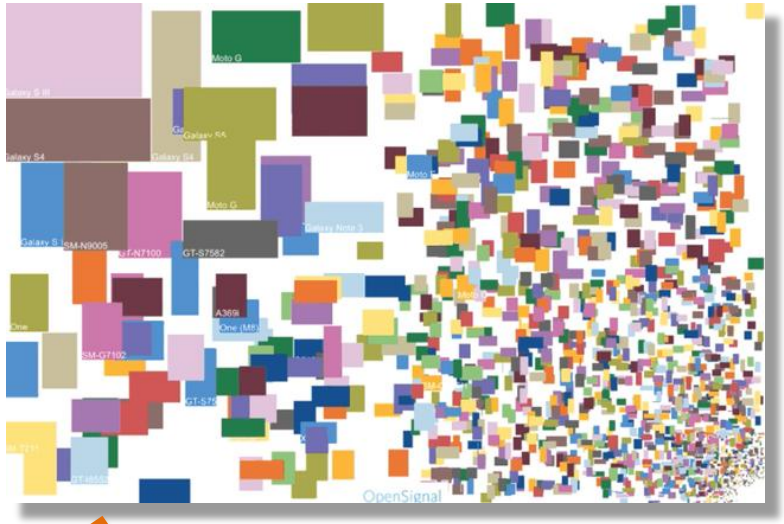
3 Chisel硬件语言

4 敏捷开发的愿景

芯片的软硬件协同开发

领域专用体系结构

处理器芯片碎片化需求



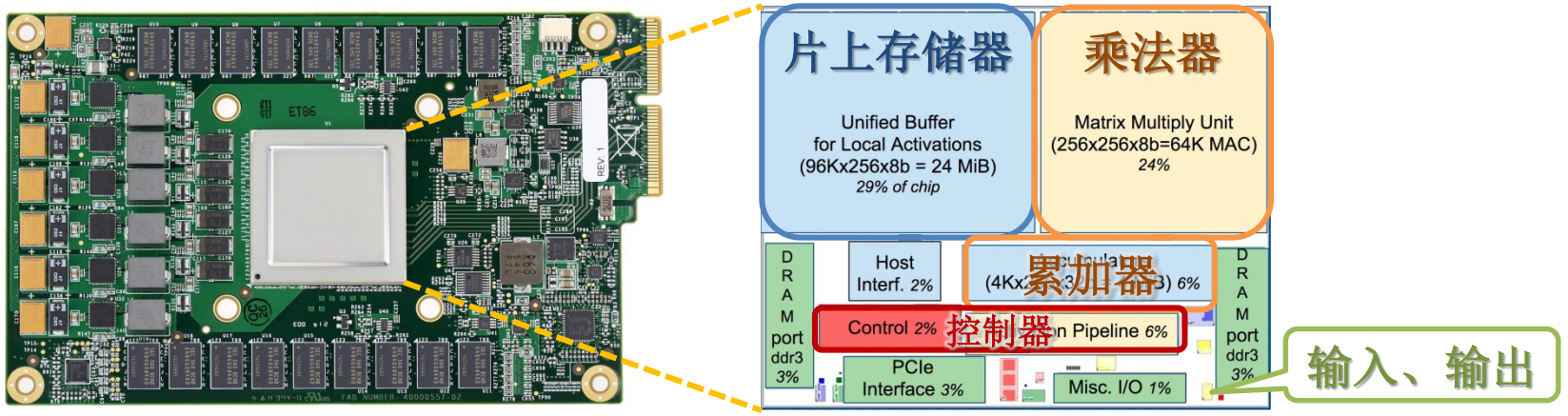
RISC-V

开源软硬件深度融合

开源硬件 + 开源软件

迫切需要在芯片研发初期快速开展软硬件敏捷协同设计与验证

Google: Tensor Processing Unit (TPU)



- **TPU instructions follow the CISC tradition**
  - It has about a dozen instructions overall
- TPU does NOT use stored program
  - Simply executes instructions sent from the host server via PCI Express interface
  - TPU is a co-processor for CPU; no OS on TPU
- The average clock cycles per instruction (CPI) of these CISC instructions is typically 10 to 20 (clk freq = 700 MHz)
  - MatrixMultiply instruction, 12 bytes in length

Opcode & Flags	Uni Buf Addr	Accu Addr	Length
3 bytes	3 bytes	2 bytes	4 bytes

Norman P. Jouppi et al., In-Datacenter Performance Analysis of a Tensor Processing Unit, in ISCA 2017

Tesla: Full Self-Driving Chip

- FSD Chip Specification
  - 14nm FinFET CMOS
  - 6 Billion Transistors
  - 12-core 2.2GHz ARM Cortex-A72 CPU
  - 1GHz 600 GLOPS GPU
  - 72 TOPS 2GHz Neural Network Processors

CISC-like ISA

SMALL INSTRUCTION SET

DMA Read

DMA Write

Convolution

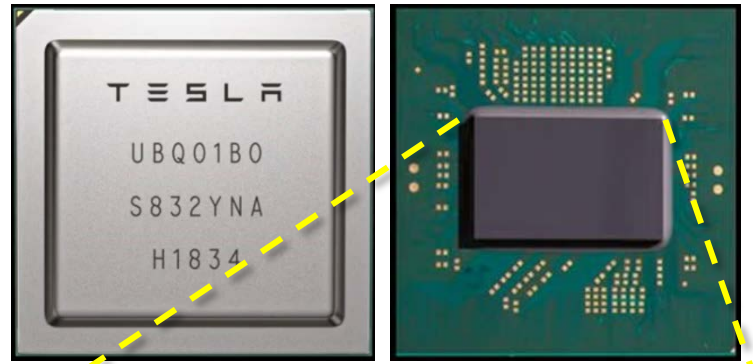
Deconvolution

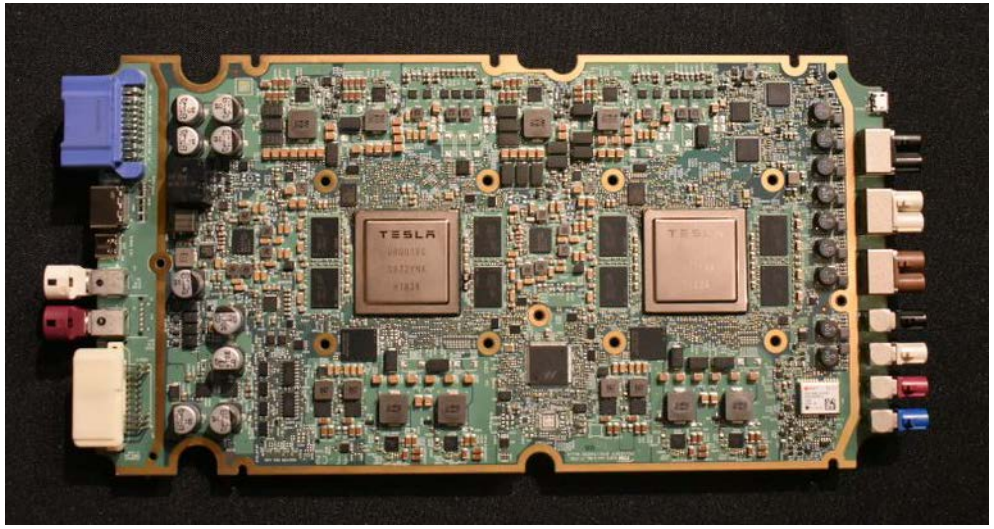
Inner-product

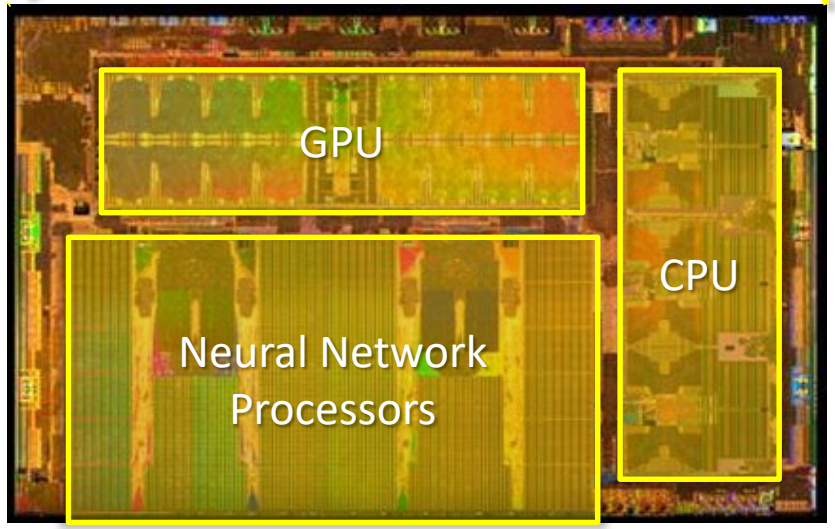
Scale

Eltwise

Stop



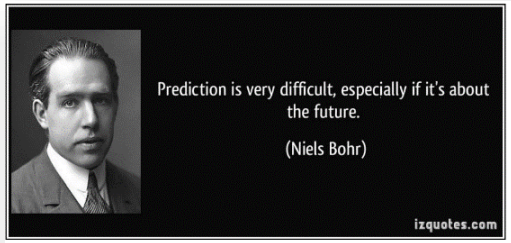


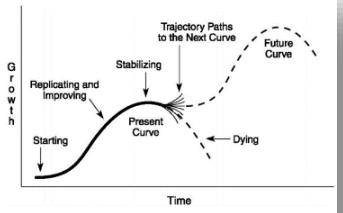


Source: Tesla Autonomy Day, April 22, 2019

Architecture 2030 @ ISCA'16

arch2030.cs.washington.edu





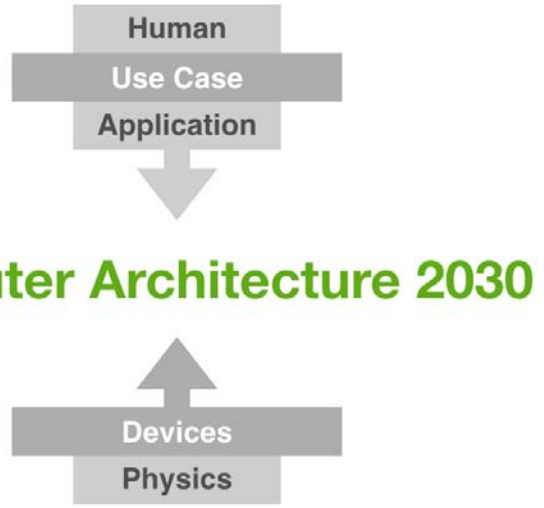
Architecture 2030 @ ISCA'16

Luis Ceze, Tom Wenisch

Mark Hill
(CCC liaison, mentor)

Big themes

- Making HW as easy to design/write as SW, open sourcing
- New devices/better exploitation of physics/biology
- Post-ISA era
- Post-Dennard/Post-Moore
- Vertical integration (systems companies)
- von Neuman is dead, long live von Neumann



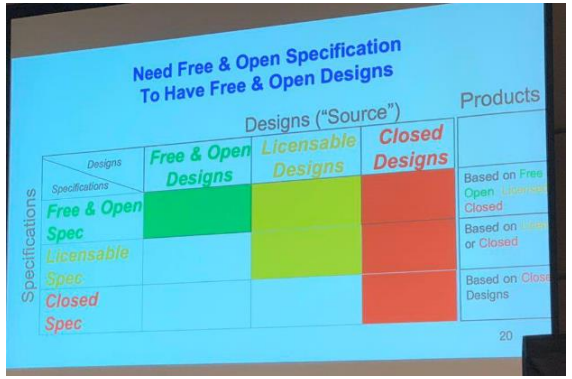
- **开源硬件(芯片)**
- 让开发硬件像开发软件那么容易，成为备受关注的**重大主题（Big themes）**

SIGARCH Visioning Workshop @ ISCA'19

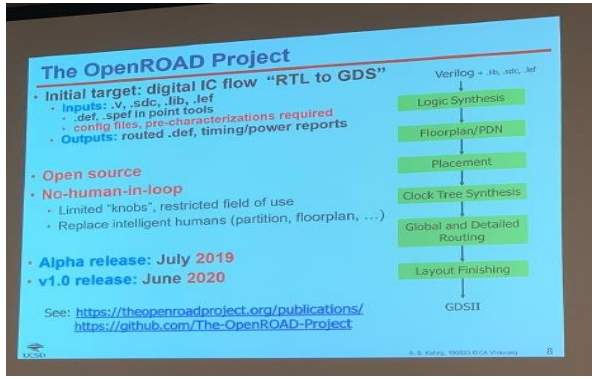
https://sites.google.com/view/agile-and-open-hardware

开源芯片内涵广泛，不仅仅只是RISC-V！

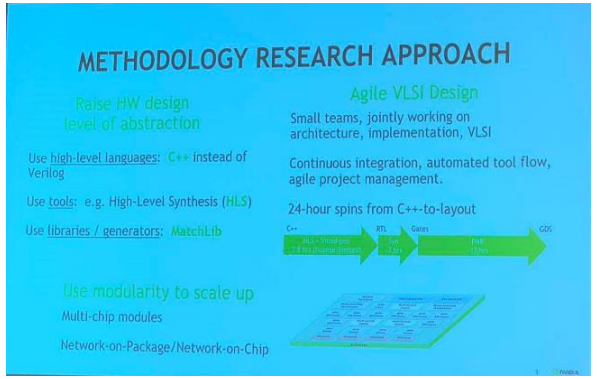
开放开源指令集与设计 (UC Berkeley/Google)



开源EDA工具链 (UCSD)

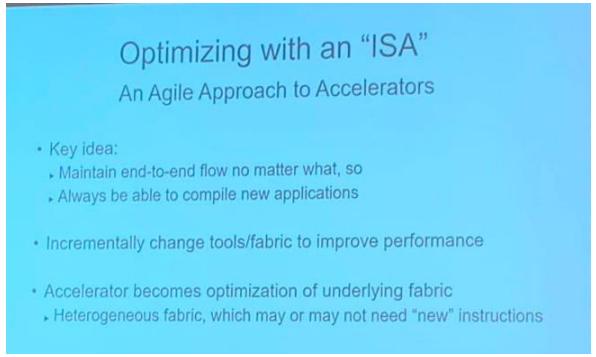


抽象硬件/设计流程 (MIT/Nvidia)

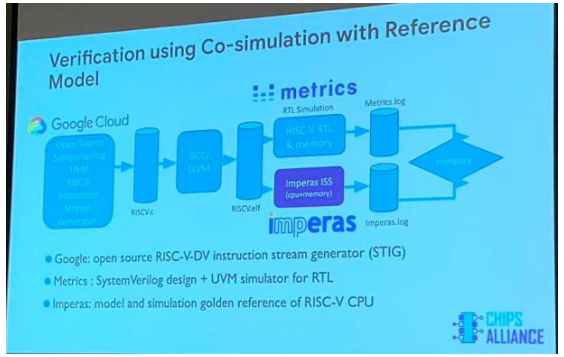


高层次综合 (UCLA)

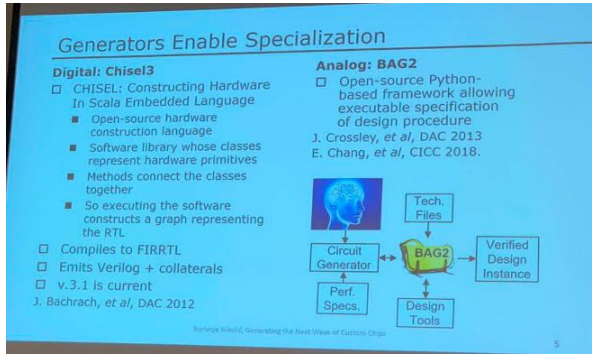
加速器敏捷设计与DSL (MIT/Stanford)



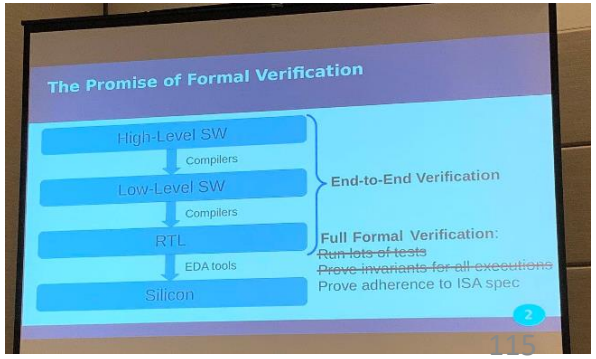
高效模拟与验证方法 (Google)



硬件代码自动生成 (UC Berkeley)



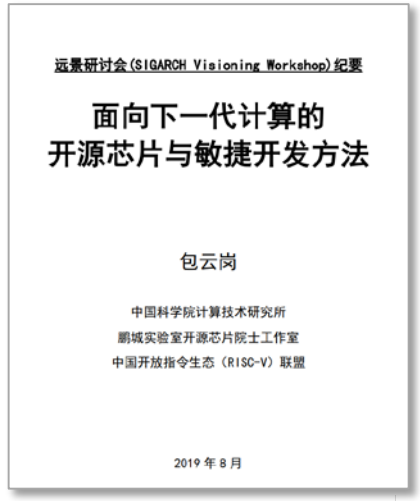
端到端形式化验证 (MIT)



SIGARCH Visioning Workshop @ ISCA'19

- **11个报告**（美国10个，中国仅1个）
  - **大学：** Berkeley/MIT/Stanford/UCLA/UCSD
  - **企业：** Nvidia、Google
  - **政府机构：** DARPA

美国各界积极投入，
中国任重道远！


远景研讨会(SIGARCH Visioning Workshop)纪要

面向下一代计算的
开源芯片与敏捷开发方法

包云岗

中国科学院计算技术研究所
鹏城实验室开源芯片院士工作室
中国开放指令生态（RISC-V）联盟

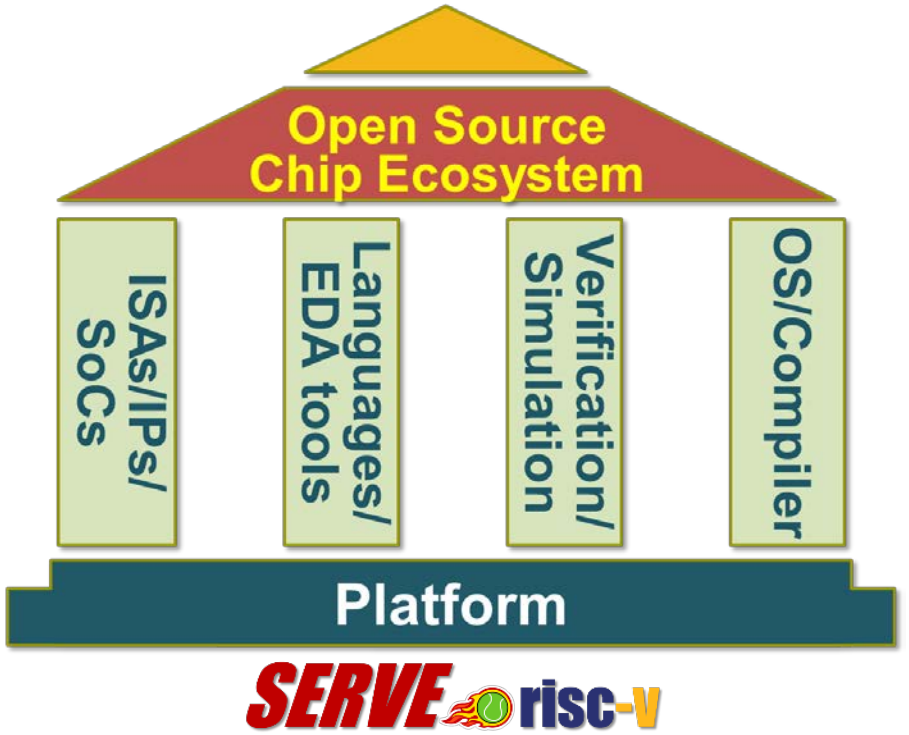
2019 年 8 月

- 9:05 am - 9:35 am, **David Patterson, UC Berkeley/Google,** *A New Golden Age for Computer Architecture*
- 9:35 am - 10:05 am, **Vivienne Sze, MIT,** *Domain-Specific Architectures for AI and Robotics: Opportunities and Challenges*
- 10:05 am - 10:35 am, **Serge Leef, DARPA,** *Automatic Implementation of Secure Silicon*
- 10:35 am - 11:05 am, **Andrew Kahng, UCSD,** *Bringing Design Technology and Architecture Closer Together: What Open Source Might Enable*
- 11:30 am - 12:00 pm, **Yungang Bao, Chinese Academy of Sciences,** *The Four Steps to An Open-Source Chip Design Ecosystem*
- 12:00 pm - 12:30 pm, **Richard Ho, Google,** *Building A Sustainable Open-Source Hardware Ecosystem*
- 2:00 pm - 2:30 pm, **Mark Horowitz, Stanford,** *AHA! – Agile HArdware*
- 2:30 pm - 3:00 pm, **Jason Cong, UCLA,** *Democratize Customizable Computing*
- 3:00 pm - 3:30 pm, **Brucek Khailany, NVIDIA,** *Machine-Learning-Assisted Agile VLSI Design for Machine Learning*
- 4:00 pm - 4:30 pm, **Borivoje Nikolić, UC Berkeley,** *Generating the Next Wave of Custom Chips*
- 4:30 pm - 5:00 pm, **Adam Chlipala, MIT,** *Strong Formal Verification Across a Hardware-Software Stack with RISC-V*

结 语

这是一个打破开源芯片死结的时代

这是一个打造开源芯片生态的时代



OS2ATC 2019 – CPU Tutorial

RISC-V开源处理器及Chisel硬件敏捷开发语言入门

谢 谢！

张　科、余子濠、陈欲晓

crva@ict.ac.cn

RV教程群

CRVA联盟

中国科学院计算技术研究所
Institute of Computing Technology, Chinese Academy of Sciences

鹏城实验室
Peng Cheng Laboratory

中国开放指令生态(RISC-V)联盟
China RISC-V Alliance