Power Transistor Tester

# Background

The idea is to create an automated tester for power transistors.

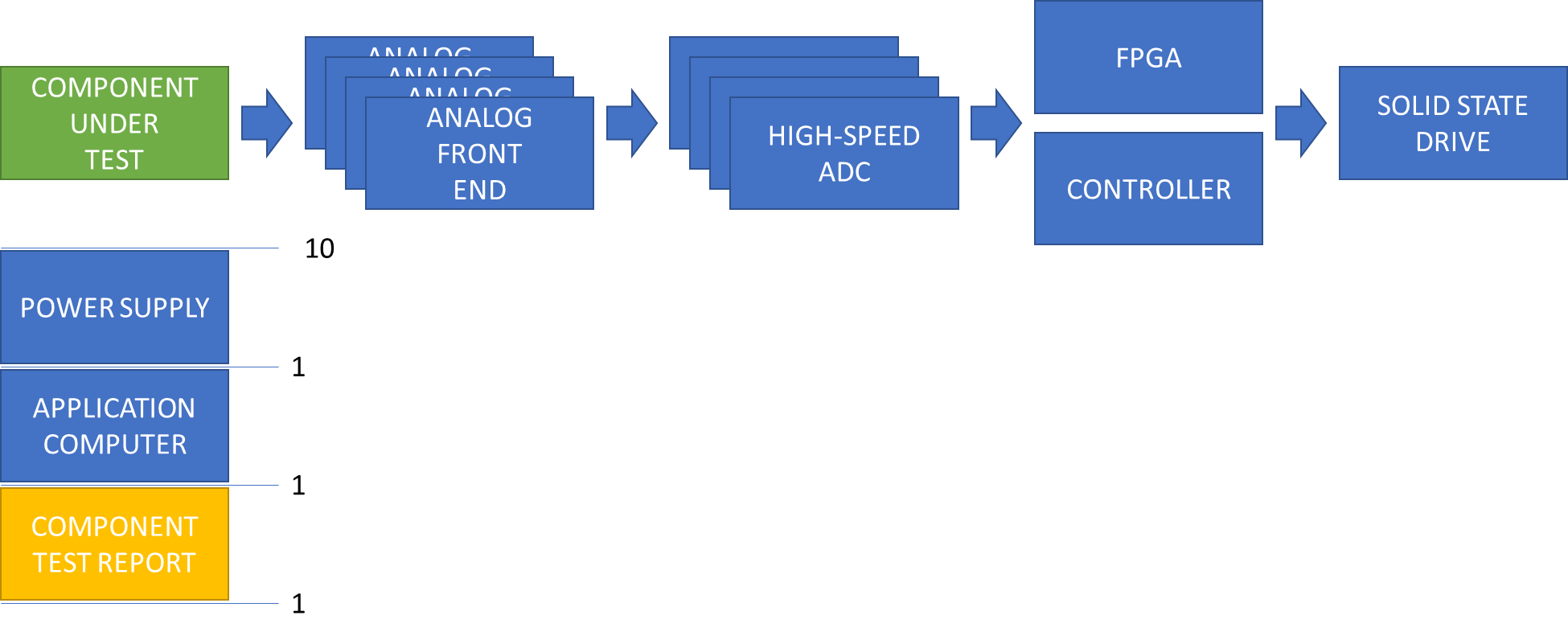
# Introduction

Numerous manufacturers of power transistors may be advertising components that do not perform with the advertised ratings. Companies that use power transistors in critical applications are likely to be interested in purchasing an automated test system (ATS) for qualifying such components.

The automated test system (ATS) will have the following features:

* Run a test program.
* Collect test results.
* Generate a test report.
* Submit the test report.

# Block Diagram



# Test Description

Each of the ten (10) components will be tested in four (4) phases.

1. Burn-In
2. Nominal Performance
3. Maximum Performance
4. Stress-Out

The fourth phase, Stress-Out, will ramp up performance stresses until each component fails.

After each component fails, each FPGA will analyze all of the data from each test cycle it observed and create a report for the application computer.

The application computer will analyze the reports of each of the ten (10) components and create a final report.

# Theory of Operation

By using precision resistors for R1, R2 and R3 and controlling the power supply voltage and control signal and measuring the voltage at each transistor terminal, it is possible to analyze the transconductance characteristics. Control the P1-2 (V+) voltage and P1-4 voltage by setting one and sweeping the other. “Set one. Sweep the other.” “Set A. Sweep B.” “Set. Sweep.” Limit the sweep based on the current flowing through P1-2 (V+) and P1-4 pins. The maximum current-limit setting will be 300A.

Need to design new miniPCB boards to handle 300A.

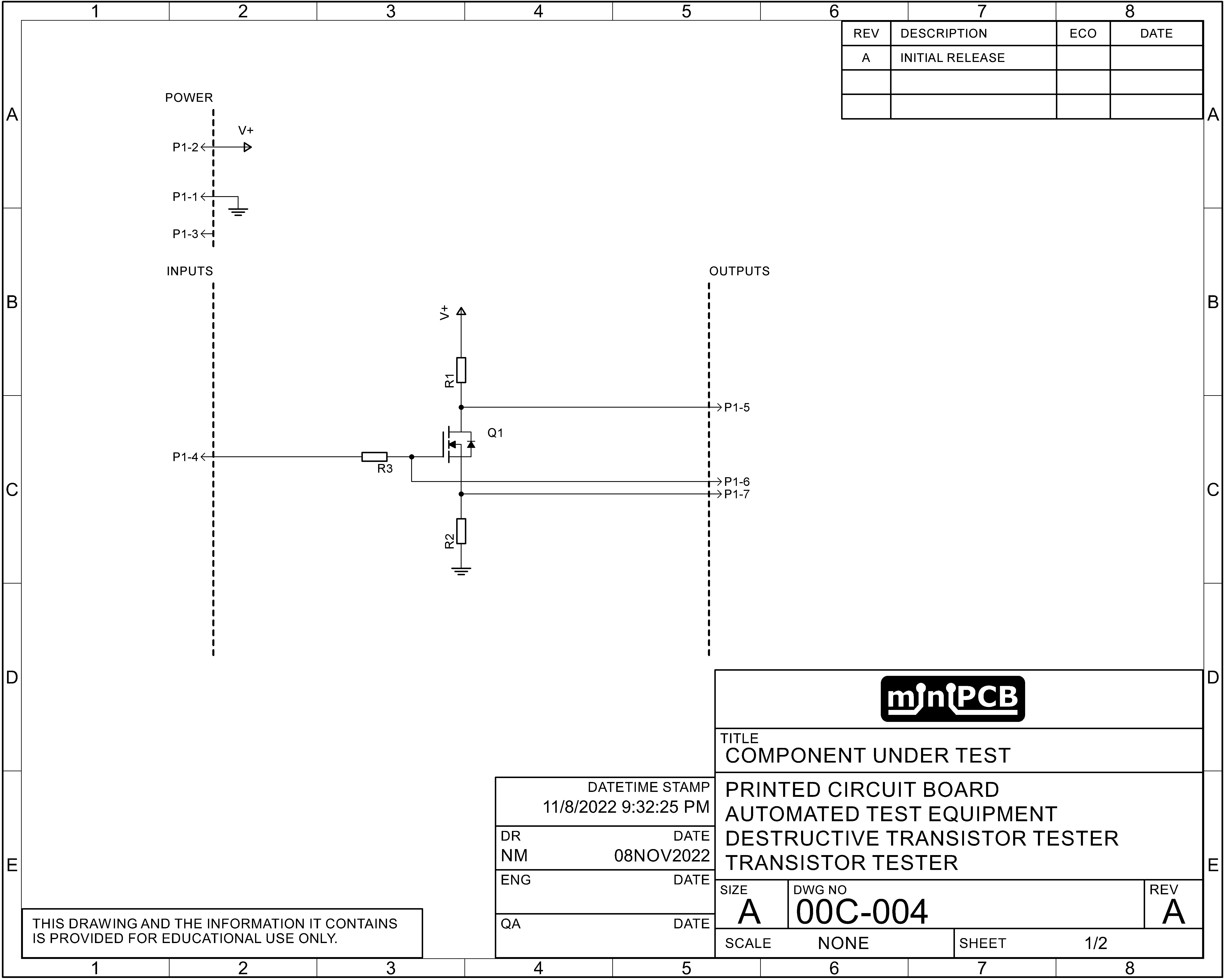
Need to acquire/design a tester capable of controlling the 300A current limit.

By measuring the heat leaving the component and temperatures at each terminal, it is possible to analyze power dissipation characteristics.

By using multiple ADC channels on the drain pin, where each ADC channel has a different gain setting, a high resolution of Vds can be achieved.

By giving each FPGA individual access to an SSD, nearly unlimited data can be recorded throughout the test.

# Schematic: Component Under Test



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| miniPCB™ | A picture containing drawing  Description automatically generated™ | Icon  Description automatically generated™ |

# Revision History

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| --- | --- | --- | --- |
| REV | DESCRIPTION | ECO | DATE |
| A | Initial Release | N/A | 08NOV2022 |
| B | Added information after watching IMSAI Guy #1312 Transistor Curve Tracer Basics (YouTube video). | N/A | 17NOV2022 |