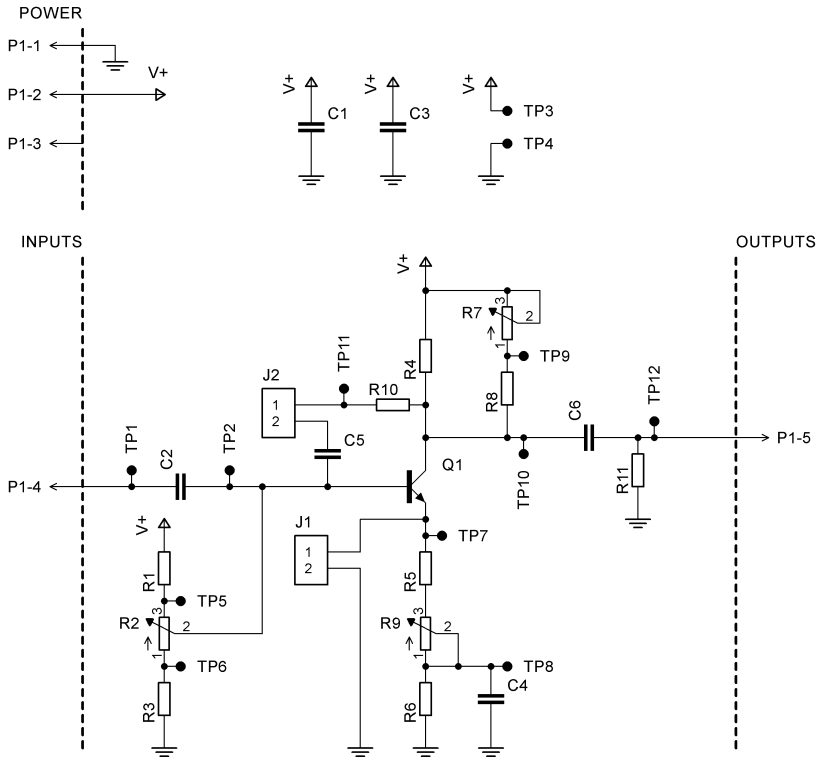
Common Emitter (Source) Amplifier

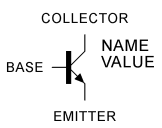
NOTES:



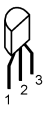
PART: NPN BIPOLAR JUNCTION TRANSISTOR

FOOTPRINT: TO92	EXAMPLE PART: 2N3904

SCHEMATIC SYMBOL



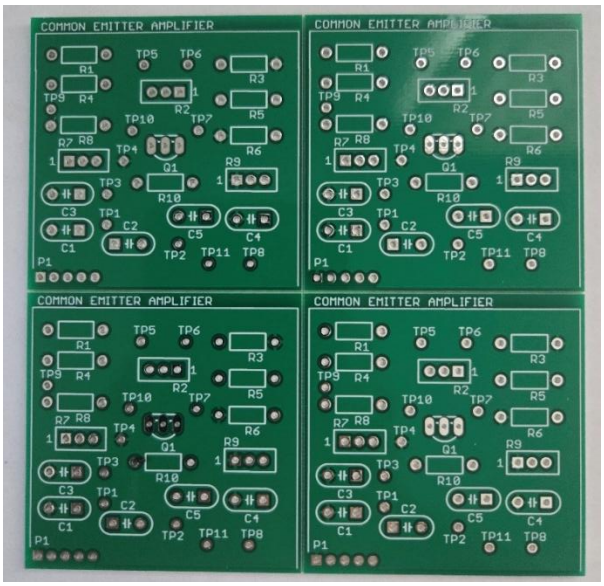
PINOUT



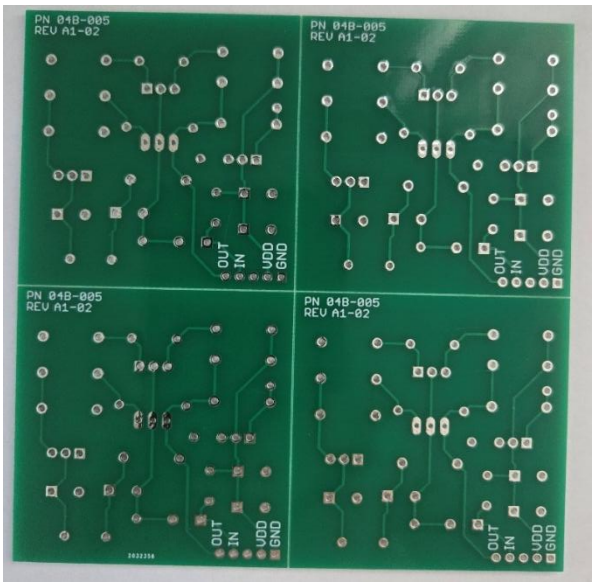
PIN	DESCRIPTION
1	EMITTER
2	BASE
3	COLLECTOR

TITLE: COMMON EMITTER AMPLIFIER

SIZE	DWG NO	REV
A	04B-005	A1-04
SAVED 6/20/2025 7:36:55 AM		SHEET 1/2



Front Side



Back Side

miniPCB Part Number

PART NO	TITLE	PIECES PER PANEL
04B-005	Common Emitter Amplifier	4

miniPCB Revision History

REV	DESCRIPTION	DATE
A1-01	Initial Release	
A1-02	Updated PCB outline and removed logo.	
A1-03	Added AC coupling capacitor, C6. Added load resistor, R11. Added TP12.	
A1-04	Moved R9 in circuit.	20JUN2025

Circuit Description

This miniPCB implements a single-stage common emitter amplifier designed around a discrete NPN bipolar junction transistor (Q1), with optional substitution for an N-channel JFET or MOSFET. The amplifier may be used to demonstrate voltage gain, phase inversion, and the effects of feedback and biasing techniques.

Power Supply Conditioning

Capacitors C1 and C3 serve as power rail decoupling and filtering elements, suppressing high-frequency noise and stabilizing the DC supply voltage. Test points TP3 (V+) and TP4 (GND) are provided for measuring supply and ground reference levels.

Input Coupling and Biasing

The AC input signal is capacitively coupled to the amplifier via C2, which blocks DC offset from the signal source, ensuring proper biasing of the transistor base.

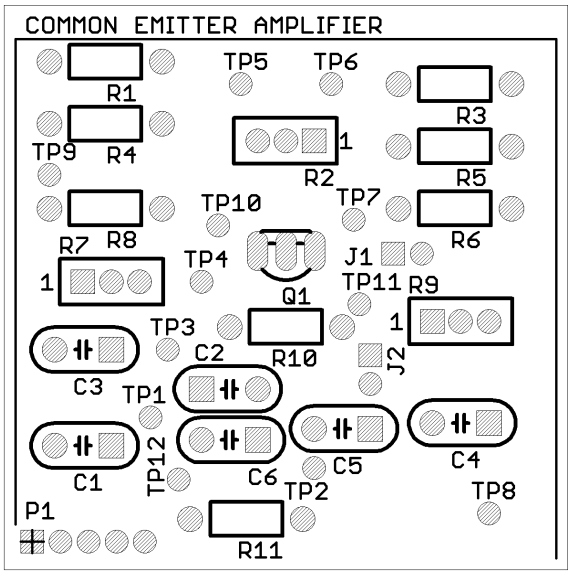


Figure 1 - Single Board, Component Outlines

Test points TP1 and TP2 allow voltage measurements across this input coupling capacitor.

Biasing of the transistor base is achieved through a resistor divider network consisting of R1, R2, and R3, with R2 implemented as a multiturn potentiometer for fine adjustment of the base voltage and operating point. This sets the quiescent collector current and ensures linear amplifier operation in the active region.

Test points TP5 and TP6 monitor voltages at key nodes within this bias network.

Feedback Network

A resistive-capacitive feedback loop composed of R10 and C5 connects the transistor's collector to its base. This provides frequency-dependent negative feedback that stabilizes gain, reduces distortion, and improves bandwidth. TP11 allows direct access to a point within this feedback path for analysis. Jumper J2 allows the feedback network to be removed from the circuit.

Collector Network and Output

The collector load consists of R4, R7, and R8, with R7 as a multiturn potentiometer to adjust gain or output bias. These resistors determine the voltage drop across the collector and directly affect the voltage gain. TP9 and TP10 are used to probe the collector and output signal path.

Emitter Network and Stability

The emitter is grounded through a multi-resistor network consisting of R5, R6, and R9 (with R9 being adjustable). These resistors set the emitter current and provide thermal stability through negative feedback.

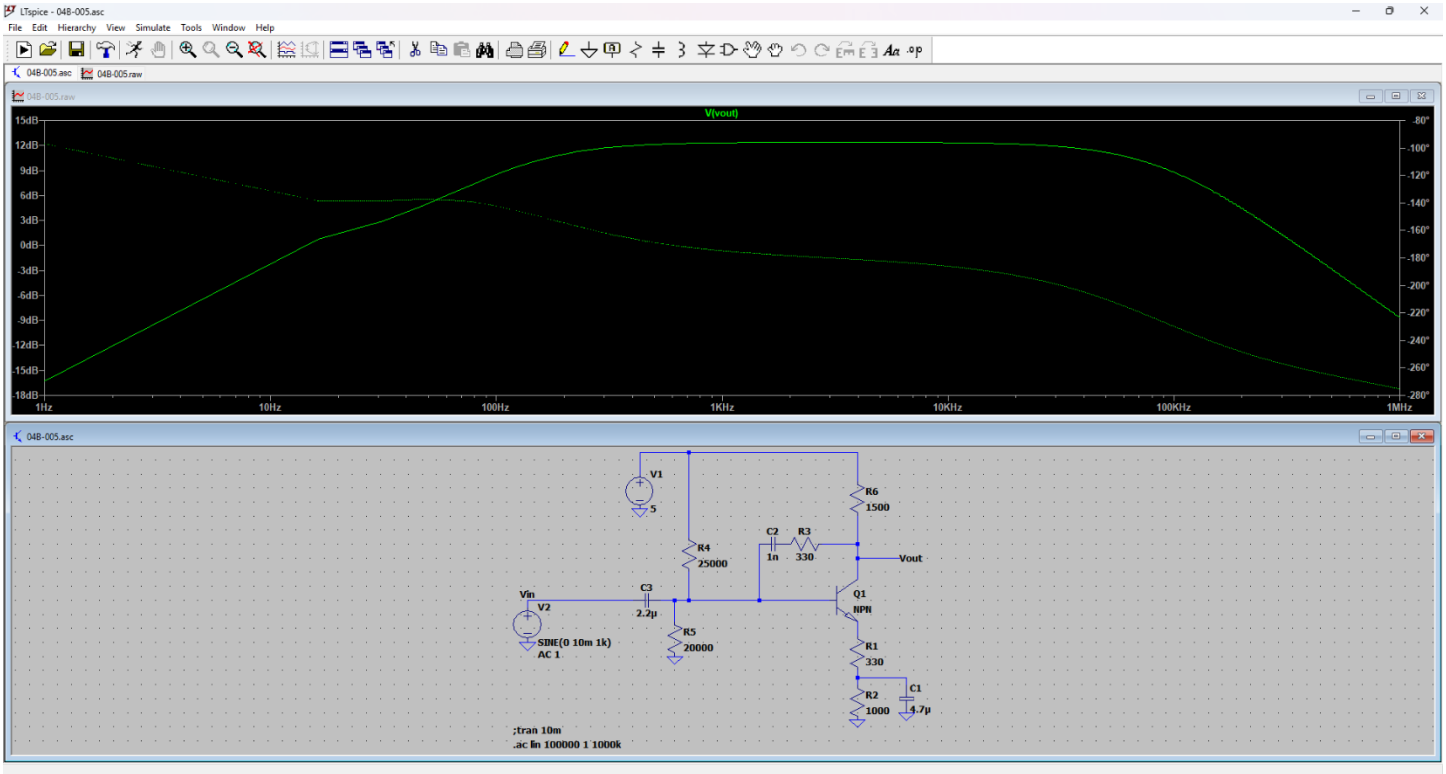
The AC bypass capacitor C4 is placed in parallel with part of the emitter resistance to increase gain at higher frequencies by reducing AC degeneration. TP7 and TP8 enable measurement of the emitter voltage and overall emitter network behavior. Jumper J1 allows the emitter network to be removed from the circuit.

Transistor Configuration

Q1 serves as the active amplifying device in the common emitter configuration. In the provided schematic, Q1 is a general-purpose NPN BJT. However, the board layout and biasing are designed to accommodate equivalent N-channel field-effect transistors (JFETs or MOSFETs) for experimentation with different semiconductor technologies.

Simulation in LTspice

LTspice was used to verify that selected component values produced reasonable amplifier behavior before assembling physical boards. The simulation helped confirm that the circuit was biased correctly, the signal was amplified, and the overall configuration functioned as expected with a voltage gain slightly greater than 4. While the analysis wasn't exhaustive, the simulation served as a practical check to ensure the design was sound and worth building.



Parts List

REF DES	PART TYPE	VALUE / DESCRIPTION
C1	CAPACITOR	4.7uF
C2	CAPACITOR	2.2uF
C3	CAPACITOR	0.1uF
C4	CAPACITOR	4.7uF
C5	CAPACITOR	1nF
C6	CAPACITOR	2.2uF
J1	JUMPER	0.1” HEADER PINS WITH JUMPER
J2	JUMPER	0.1” HEADER PINS WITH JUMPER
R1	RESISTOR	10kΩ
R2	RESISTOR	25kΩ
R3	RESISTOR	10kΩ
R4	RESISTOR	3.3kΩ
R5	RESISTOR	330Ω
R6	RESISTOR	1.5kΩ
R7	RESISTOR	2kΩ
R8	RESISTOR	3.3kΩ
R9	RESISTOR	2kΩ
R10	RESISTOR	330Ω
R11	RESISTOR	10kΩ
Q1	TRANSISTOR	2N3904
TP1-TP12	TEST POINT	KEYSTONE ELECTRONICS SERIES 5000
P1	HEADER PINS	5POS, 2.54mm PITCH, RA

Parts List (Form)

REF DES	PART TYPE	VALUE / DESCRIPTION
C1	CAPACITOR	
C2	CAPACITOR	
C3	CAPACITOR	
C4	CAPACITOR	
C5	CAPACITOR	
C6	CAPACITOR	
J1	JUMPER	0.1” HEADER PINS WITH JUMPER
J2	JUMPER	0.1” HEADER PINS WITH JUMPER
R1	RESISTOR	
R2	RESISTOR	
R3	RESISTOR	
R4	RESISTOR	
R5	RESISTOR	
R6	RESISTOR	
R7	RESISTOR	
R8	RESISTOR	
R9	RESISTOR	
R10	RESISTOR	
R11	RESISTOR	
Q1	TRANSISTOR	
TP1-TP12	TEST POINT	KEYSTONE ELECTRONICS SERIES 5000
P1	HEADER PINS	5POS, 2.54mm PITCH, RA

Build

NEED TO ADD

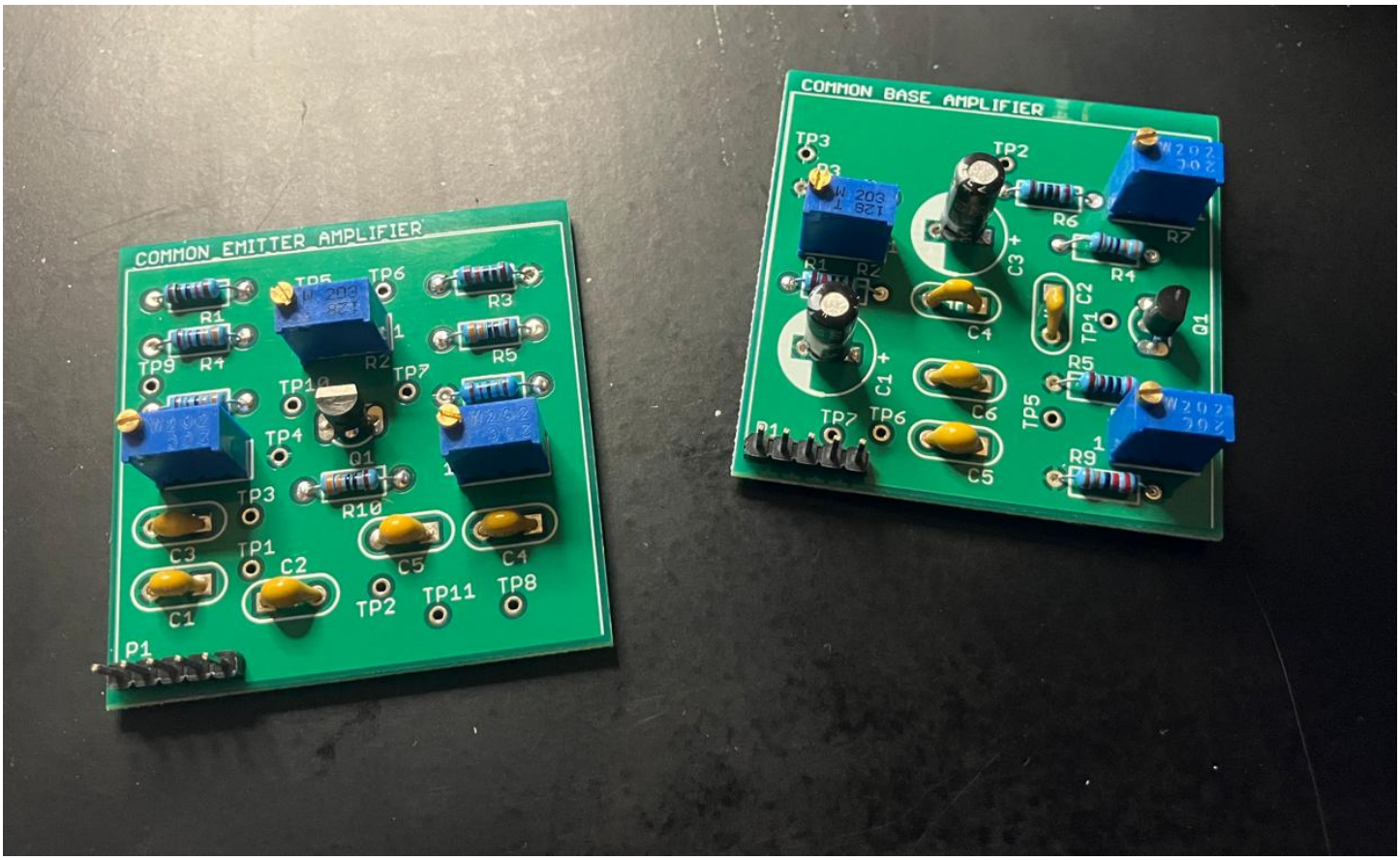
Testing

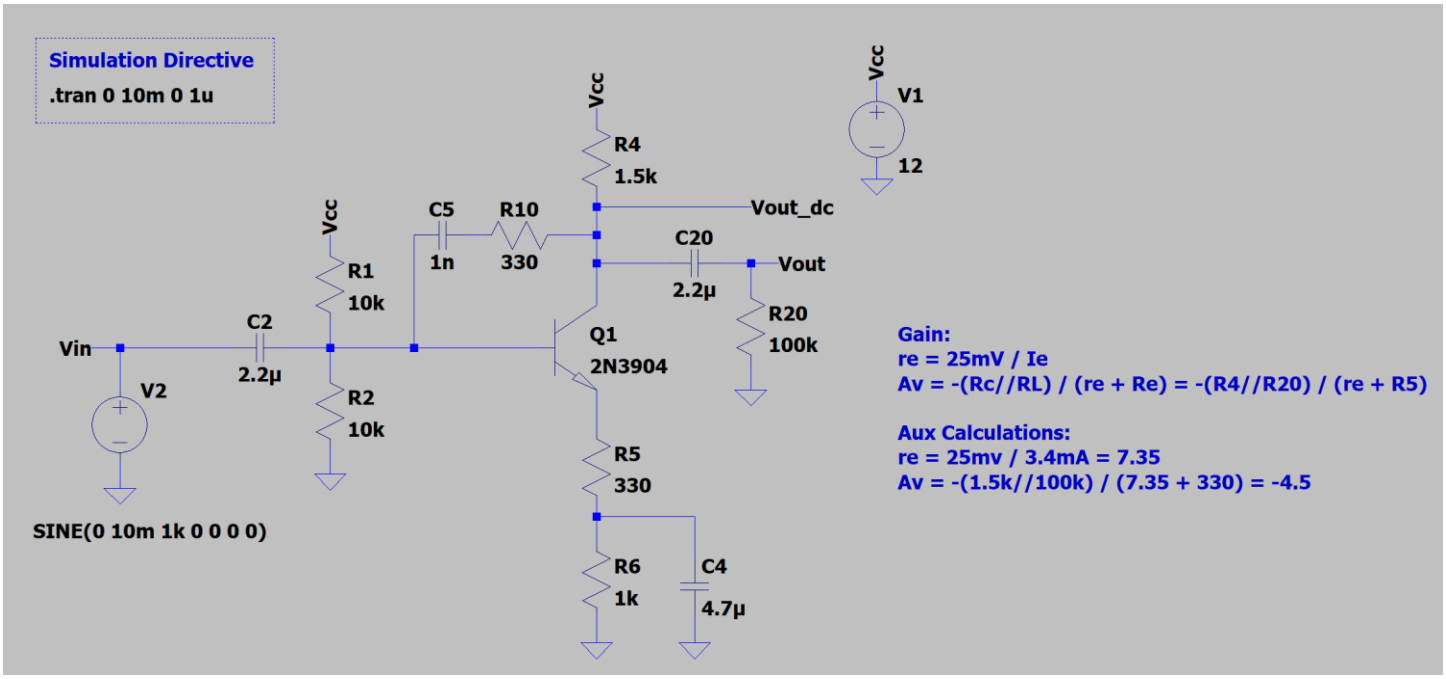
NEED TO ADD

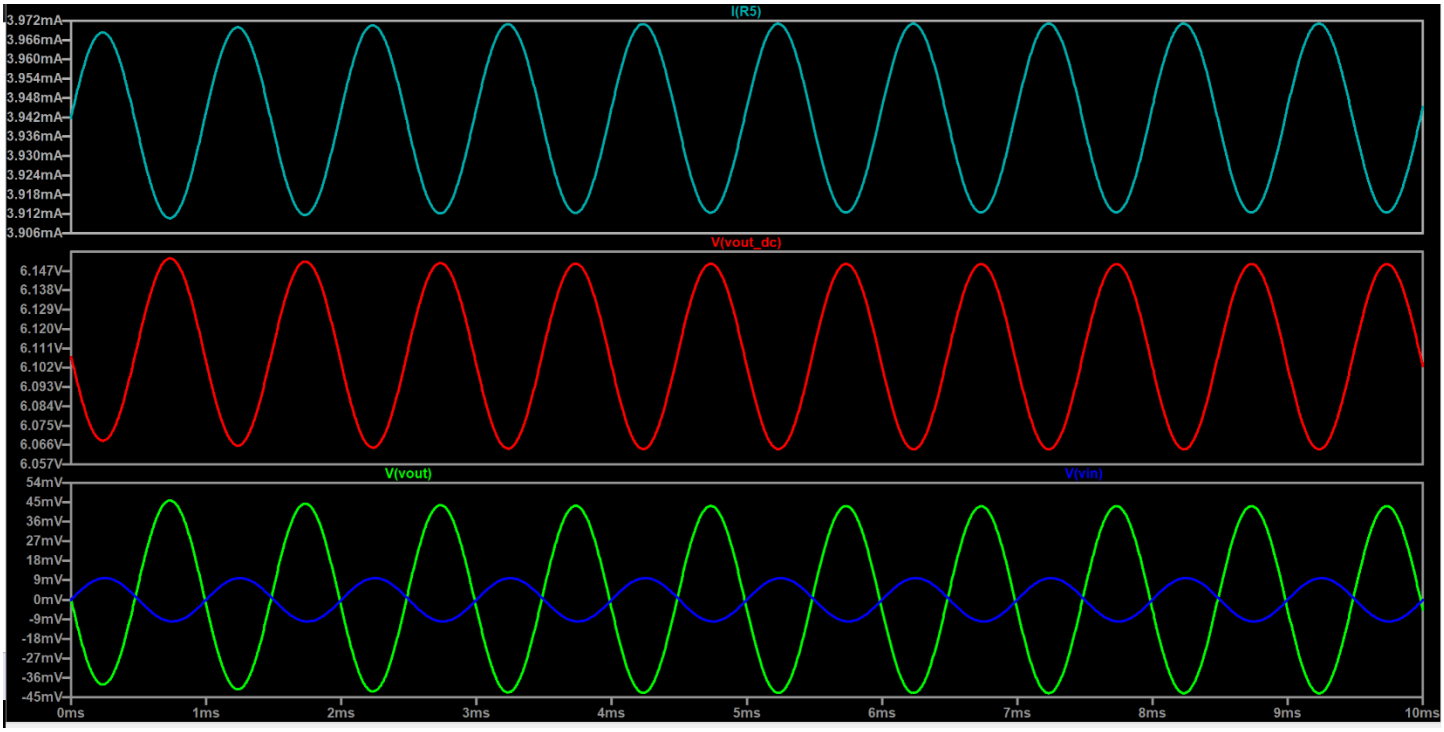
Industry Feedback

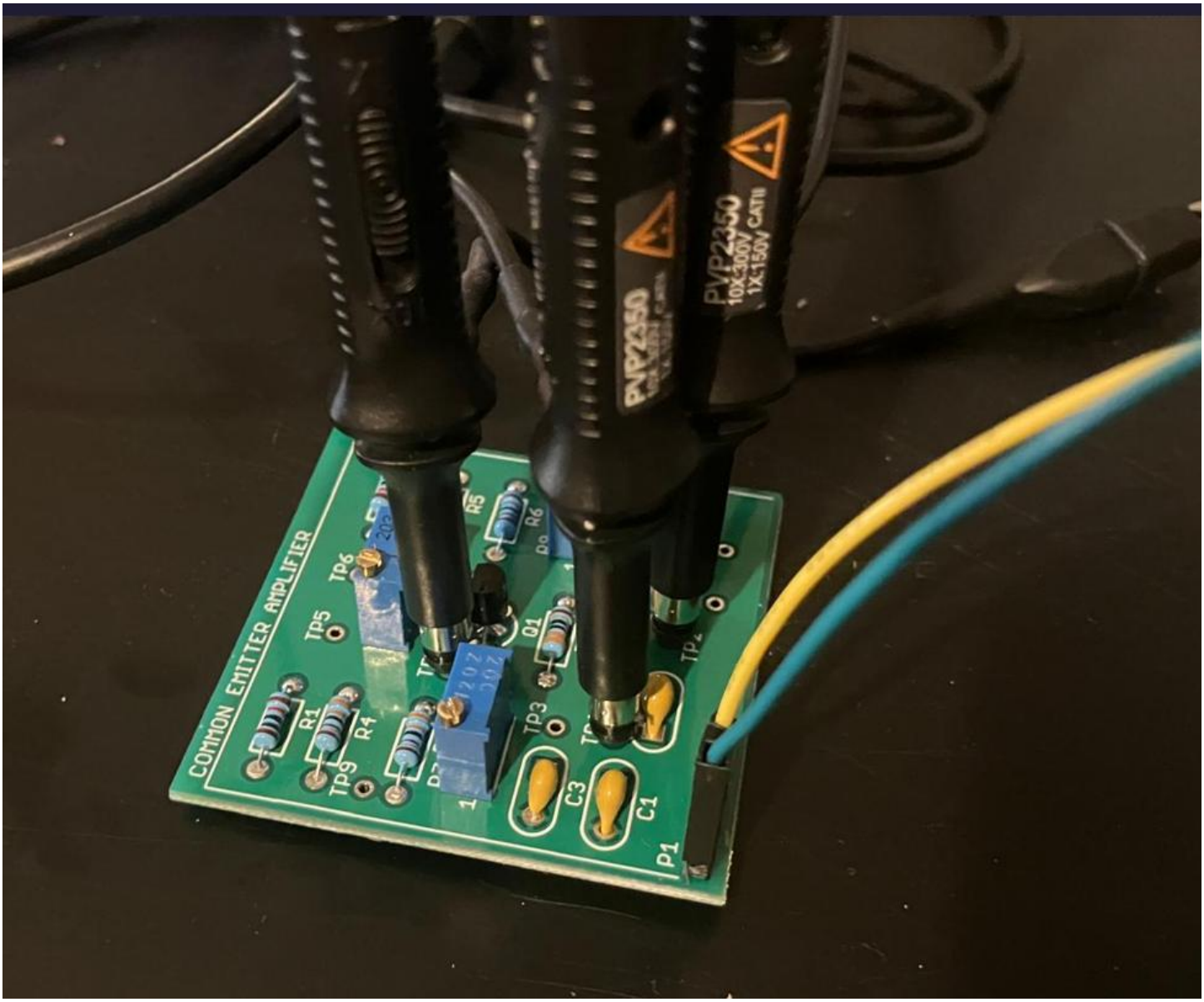
University of Denver, Goncalo, 15JUN2025

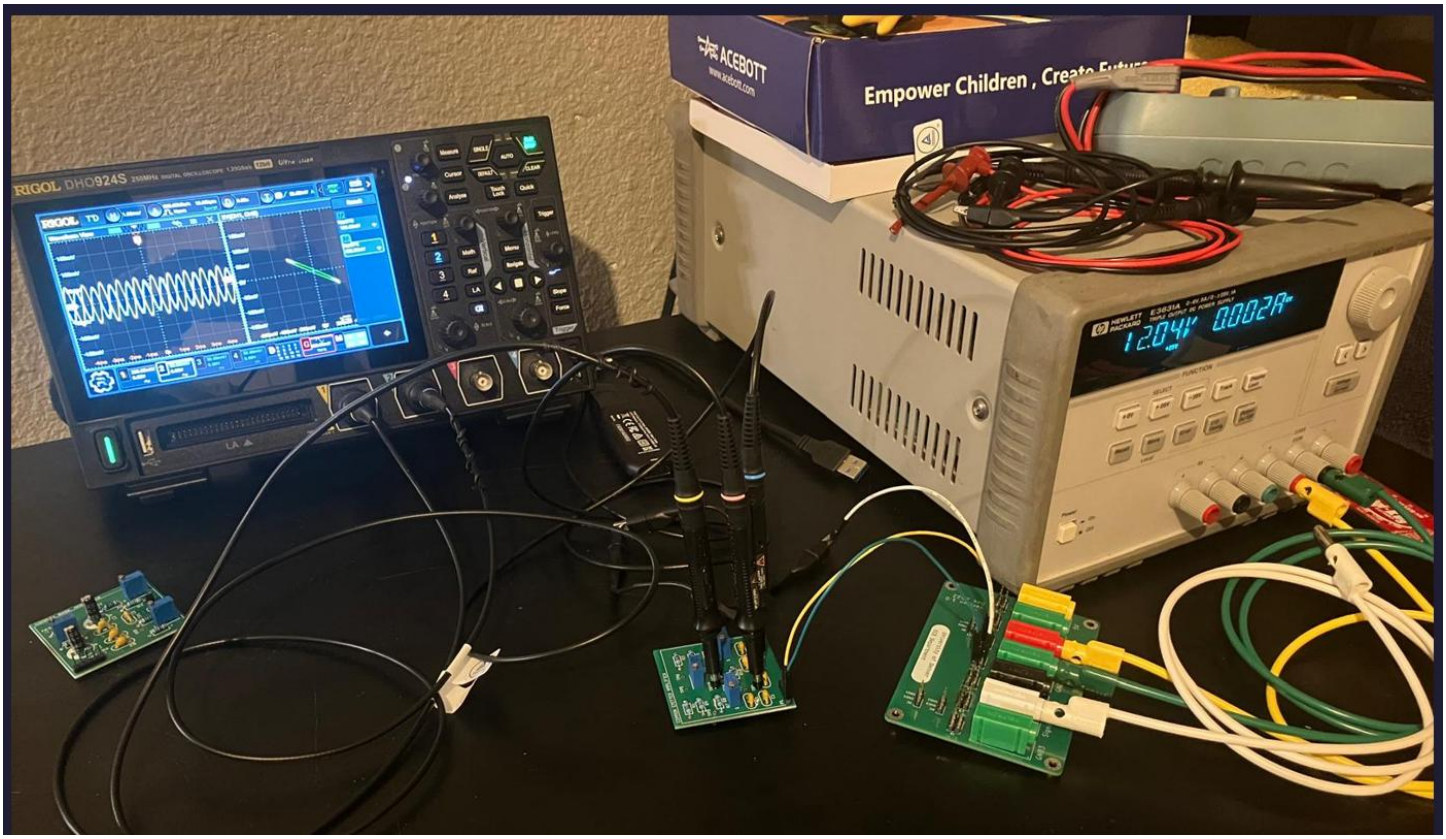
The feedback provided by Goncalo directly affected changes made to Rev A1-03.

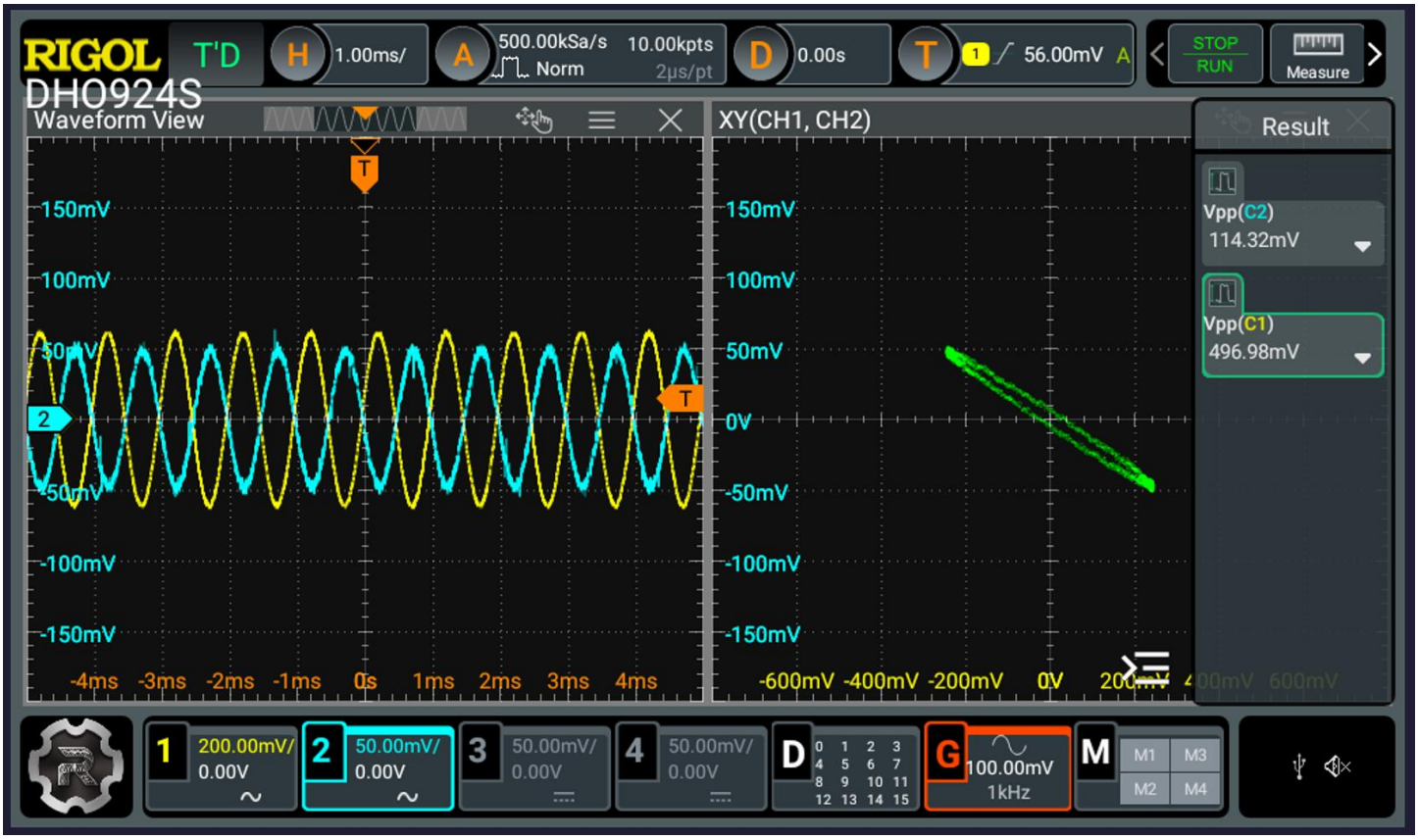


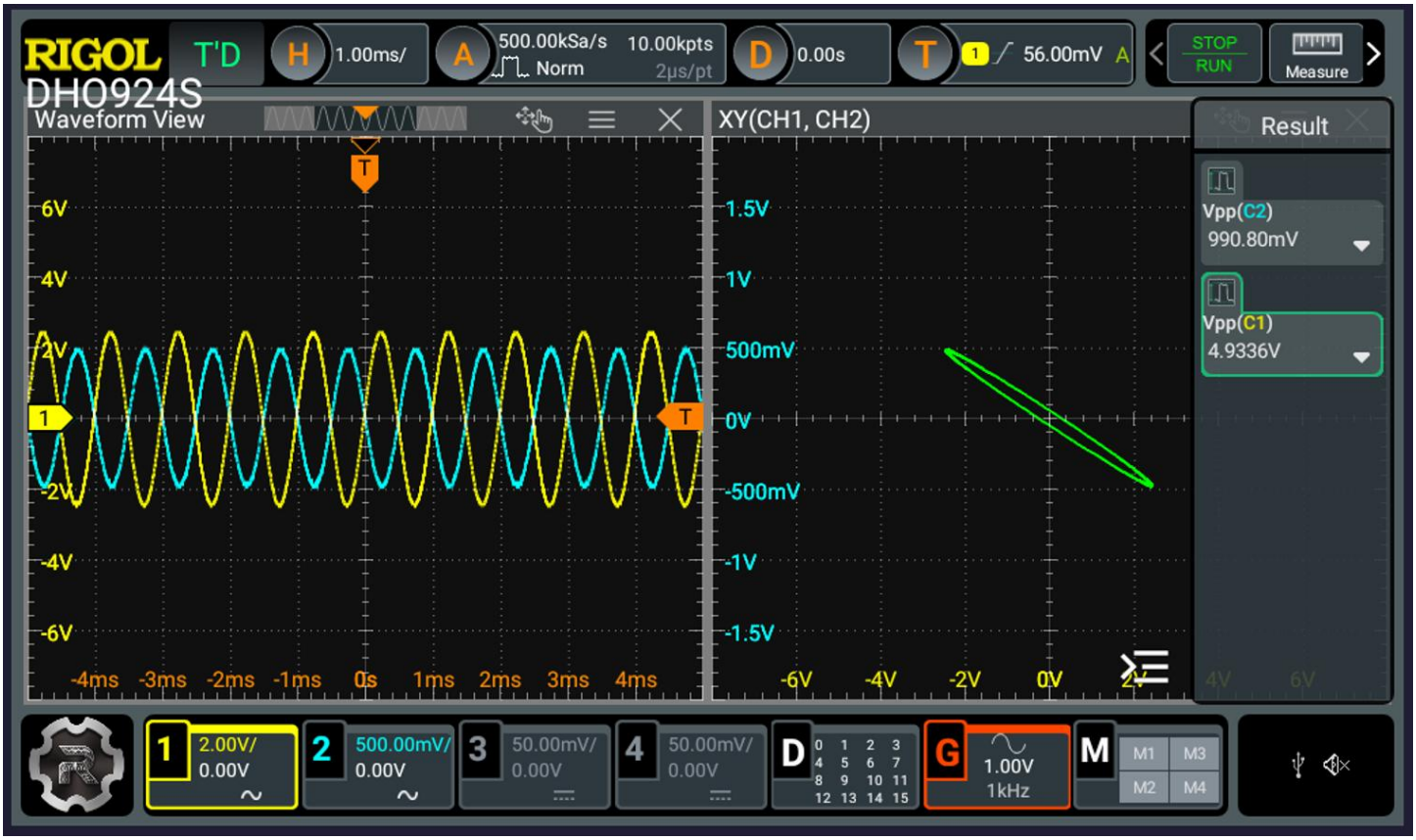

Simulation Directive
.tran 0 10m 0 1u
Vcc
V1
12
R4
1.5k
Vcc
C5
1n
R10
330
Vout_dc
C20
2.2µ
Vout
R1
10k
R20
100k
C2
2.2µ
Vin
Q1
2N3904
V2
R2
10k
R5
330
R6
1k
C4
4.7µ
SINE(0 10m 1k 0 0 0 0)
Gain:
re = 25mV / Ie
Av = -(Rc//RL) / (re + Re) = -(R4//R20) / (re + R5)
Aux Calculations:
re = 25mv / 3.4mA = 7.35
Av = -(1.5k//100k) / (7.35 + 330) = -4.5

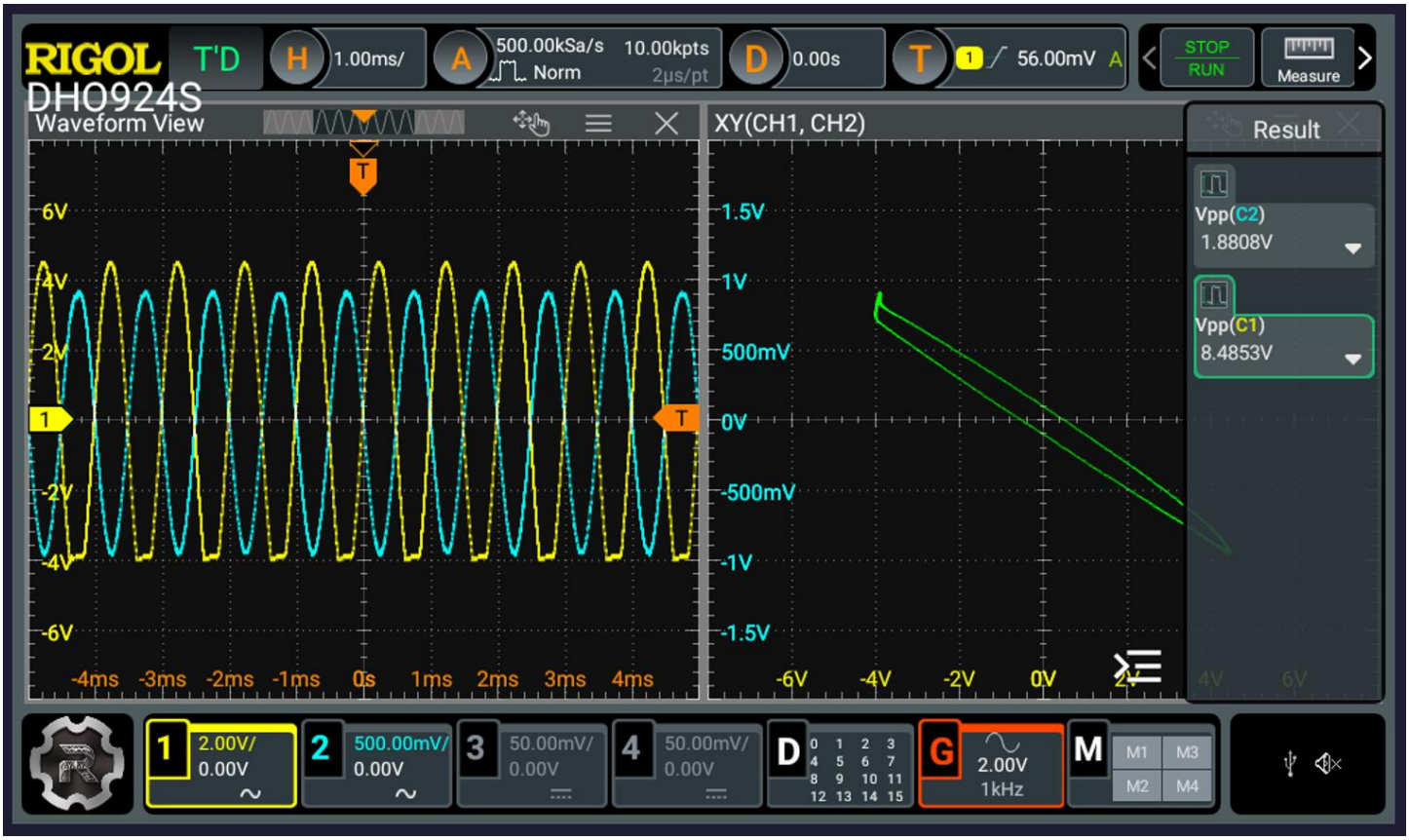

I(R5)
3.972mA
3.966mA
3.960mA
3.954mA
3.948mA
3.942mA
3.936mA
3.930mA
3.924mA
3.918mA
3.912mA
3.906mA
V(vout_dc)
6.147V
6.138V
6.129V
6.120V
6.111V
6.102V
6.093V
6.084V
6.075V
6.066V
6.057V
V(vout)
V(vin)
54mV
45mV
36mV
27mV
18mV
9mV
0mV
-9mV
-18mV
-27mV
-36mV
-45mV
0ms
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms


COMMON EMITTER AMPLIFIER
R1
R4
R5
R6
Q1
TP3
TP5
TP6
TP9
C3
C1
P1
PVP2350
10X-300V
1X-150V CAT II


ACEBOTT
Empower Children , Create Future
RIGOL DHO924S


RIGOL
DHO924S
T'D
H 1.00ms/
A 500.00kSa/s Norm
10.00kpts 2µs/pt
D 0.00s
T 56.00mV A
STOP RUN
Measure
Waveform View
XY(CH1, CH2)
Result
Vpp(C2)
114.32mV
Vpp(C1)
496.98mV
150mV
100mV
50mV
0V
-50mV
-100mV
-150mV
-4ms -3ms -2ms -1ms 0s 1ms 2ms 3ms 4ms
-600mV -400mV -200mV 0V
1 200.00mV/ 0.00V
2 50.00mV/ 0.00V
3 50.00mV/ 0.00V
4 50.00mV/ 0.00V
D
G 100.00mV 1kHz
M
M1 M3 M2 M4


RIGOL
DHO924S
T'D
H 1.00ms/
A 500.00kSa/s 10.00kpts Norm 2µs/pt
D 0.00s
T 1 56.00mV A
STOP RUN
Measure
Waveform View
XY(CH1, CH2)
Result
Vpp(C2)
990.80mV
Vpp(C1)
4.9336V
6V
4V
2V
-2V
-4V
-6V
-4ms -3ms -2ms -1ms 0s 1ms 2ms 3ms 4ms
1.5V
1V
500mV
0V
-500mV
-1V
-1.5V
-6V -4V -2V 0V 2V
4V 6V
1 2.00V/ 0.00V
2 500.00mV/ 0.00V
3 50.00mV/ 0.00V
4 50.00mV/ 0.00V
D 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
G 1.00V 1kHz
M M1 M3 M2 M4


RIGOL
DHO924S
T'D
H 1.00ms/
A 500.00kSa/s 10.00kpts Norm 2µs/pt
D 0.00s
T 1 56.00mV A
STOP RUN
Measure
Waveform View
XY(CH1, CH2)
Result
Vpp(C2)
1.8808V
Vpp(C1)
8.4853V
6V
4V
2V
-2V
-4V
-6V
-4ms -3ms -2ms -1ms 0s 1ms 2ms 3ms 4ms
1.5V
1V
500mV
0V
-500mV
-1V
-1.5V
-6V -4V -2V 0V 2V
4V 6V
1 2.00V/ 0.00V
2 500.00mV/ 0.00V
3 50.00mV/ 0.00V
4 50.00mV/ 0.00V
D 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
G 2.00V 1kHz
M M1 M3 M2 M4

References

- https://www.minipcb.com/04B/04B-005.html
- https://www.youtube.com/@minipcb

Revision History

REV	DESCRIPTION	DATE
A	Initial Release	