An Analog-Assisted Digital LDO with 0.37mV Output Ripple and 5500x Load Current Range in 180nm CMOS

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***Abstract*—This paper presents an analog-assisted digital low dropout regulator (LDO) by adopting a delta sigma modulator (DSM) and a finite impulse response (FIR) filter for reduced output ripple. By employing a dual-mode gain-controlled voltage detector (GCVD) and a gear-shift algorithm, reduced recovery time is achieved. An exponential-ratio array (ERA) is designed to expand the load current range. A charge pump (CP) LDO as an analog-assisted loop enhances transient performance. The proposed digital LDO is implemented in 180nm CMOS. For an output voltage of 0.9V, a maximum load current of 100mA and 5500× load current range are achieved with an input voltage of 1V. The undershooting voltage is 78mV when the load current changes from 10mA to 100mA, and the output ripple is 0.37mV.**

Keywords—low dropout regulator (LDO), digital LDO, gear-shift algorithm, delta sigma modulator (DSM), finite impulse response (FIR) filter, charge pump (CP) LDO

I. Introduction

The low dropout regulator (LDO) plays an important role as the core of supply voltage management circuits in the system-on-chip (SoC) design. With advanced CMOS technology, digital LDOs have attracted widespread attention by offering low-voltage operation and process scalability compared to analog LDOs. However, the conventional digital LDO based on a bidirectional shift register [1] faces the trade-off among transient response speed, output current resolution, and power consumption. In this paper, we propose a dual-loop digital LDO with a dead-zone charge pump (CP) LDO [2] as an analog-assisted loop to speed up transient response. In addition, we adopt a delta sigma modulator (DSM) and an FIR filter in the main digital loop to reduce the output ripple.

II. Architecture

Fig. 1 shows the system architecture of the proposed digital LDO, consisting of a main digital loop in parallel with an analog-assisted loop. The main digital loop is composed of a gain-controlled voltage detector (GCVD), a gear-shift algorithm, an accumulator, a DSM, an FIR filter, an exponential-ratio array (ERA) power transistors and a power transistors array for FIR filter. The analog-assisted loop is based on a dead-zone CP LDO.

Firstly, in order to reduce the circuit recovery time and output ripple, the GCVD with dual-mode operation of the transient mode and the steady mode is designed in the digital LDO. The GCVD consists of three synchronous comparators, a decoder and a multiplier, where the reference voltage for each comparator is generated by a resistor ladder with a high reference voltage V_{REFH} and a low reference voltage V_{REFL}. The decoder increases the loop gain by putting a boosted weight on higher and lower quantization bits. Furthermore, the multiplier provides a variable gain of 2^m, where m is the gear of the gear-shift algorithm. And the gear m depends on the accumulator output. When a voltage undershooting or overshooting appears, the gear-shift algorithm is triggered by the CP LDO. If the difference of the accumulator output for every N cycles is smaller than a threshold, m is decremented by 1. After several cycles, m is decreased to 0, which means the digital LDO is settled. The gear-shift algorithm with multiple automatic gears enables the digital LDO to achieve fast recovery in the transient mode and the minimum output ripple in the steady mode.

Secondly, the DSM and the FIR filter are designed in the main digital loop. The DSM enables the digital LDO to achieve high resolution with oversampling. Also, its noise shaping property pushes quantization noise to high frequencies. The FIR filter consisting of a series of delay units suppresses the quantization noise in high frequencies, resulting in the reduced output ripple of the digital LDO.

Thirdly, the ERA is designed for PMOS power transistors instead of using same-sized transistors. When there is a heavy load, the current resolution of each power transistor is relaxed under the same output ripple. In the ERA, the transistor size is increased exponentially with the base of 1.02, which

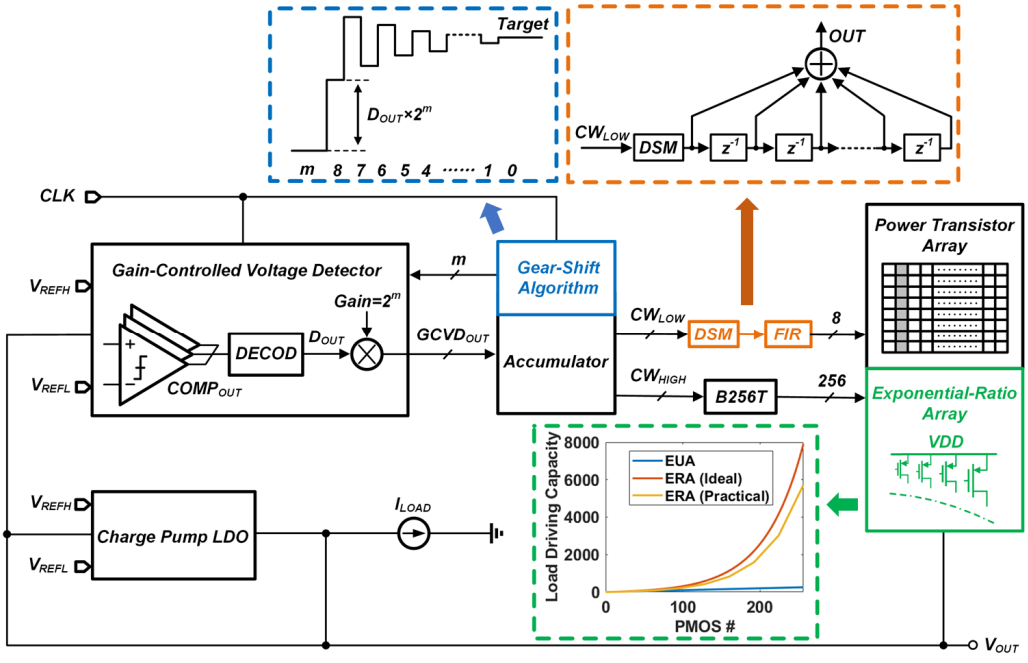

Fig. 1. System architecture of proposed digital LDO.

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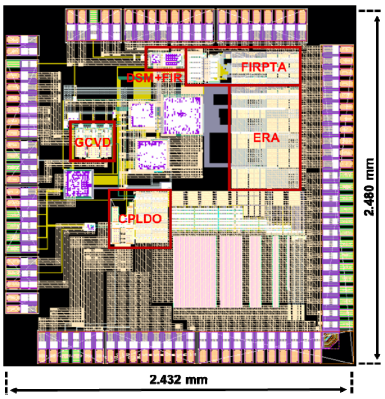
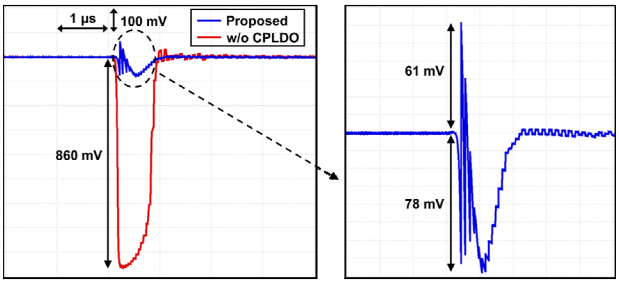
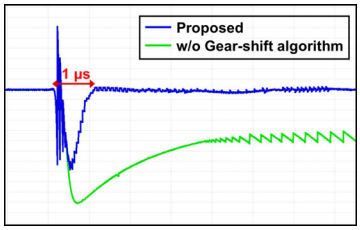


Fig. 2. Layout of proposed digital LDO.



(a)



(b)

Fig. 3. Simulated load transient response: (a) Undershooting voltage, and (b) Recovery time.

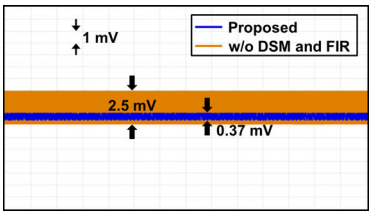


Fig. 4. Simulated steady-state output voltage.

substantially expands the load current range of the digital LDO [3].

Lastly, the dead-zone CP LDO with inverter-based asynchronous comparators is applied as an analog-assisted loop. A voltage undershooting is observed at the output when the load current has a jump. If the undershooting exceeds V_{REFL} of the analog-assisted loop, the comparator is triggered, and the CP LDO is turned on. The CP LDO improves the transient response speed, thus reducing the undershooting voltage.

III. Simulation Results

The proposed digital LDO was implemented in 180nm CMOS. The chip area including pads and load circuits for testing is 2.480mm × 2.432mm with an active area of 0.911 mm^2. The chip layout is shown in Fig. 2.

TABLE I. Performance Comparison

	This Work	[5]	[4]	[2]
Process	180nm	65nm	180nm	65nm
V_{IN} (V)	1-1.8	0.5-1	0.7-1.8	0.6-1.2
V_{OUT}(V)	0.9-1.7	0.4-0.95	0.6-1.7	0.5-1.1
Load Range	0.018mA-100mA (5500×)	0.03mA-15mA (512×)	N.A.	0.02mA-100mA (5000×)
F_S (MHz)	20	10	10	5
C_{TOTAL} (pF)	11.6	100	30	26
Recovery Time (µs)	1	3	6	2
ΔV_{OUT} (mV)	78	105	106	95
ΔI_{LOAD} (mA)	90	10	90	90
I_Q (µA)	248	3.2	6.3	28.5
FOM* (fs)	27.7	230	2.0	8.69
V_{RIPPLE} (mV)	0.37	3	10.5	5

* $FOM = \frac{C_{TOTAL} \cdot \Delta V_{OUT}}{\Delta I_{LOAD}} \times \frac{I_Q}{\Delta I_{LOAD}}$

The proposed digital LDO works at 1V supply with an output voltage of 0.9V. The simulated load transient response with 90mA current change is shown in Fig. 3. Thanks to the CP LDO, the proposed digital LDO achieves the undershooting voltage of 78mV, compared with 860mV for the digital LDO without CP LDO. Moreover, the proposed digital LDO with the gear-shift algorithm achieves the recovery time of 1µs, which is much reduced compared to the digital LDO without gear-shift algorithm. Fig. 4 shows the zoom-in steady-state output voltage. The proposed digital LDO achieves 0.37mV output ripple, compared with 2.5mV for the digital LDO without DSM and FIR filter. Table I summarizes the simulated performance of the proposed digital LDO in comparison with the state-of-the-art works. Even though the I_Q is 248µA, most of the current is consumed by the high frequency DSM and FIR filter to achieve a sub-1mV output ripple.

IV. Conclusion

A digital LDO with an analog-assisted loop has been proposed in this paper. The ERA achieves a 5500× load current range with 100mA maximum current. By applying the gear-shift algorithm, the recovery time is reduced to 1µs. Thanks to the DSM and FIR filter, the output ripple is only 0.37mV. Additionally, a FOM of 27.7fs is achieved.

Acknowledgment

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