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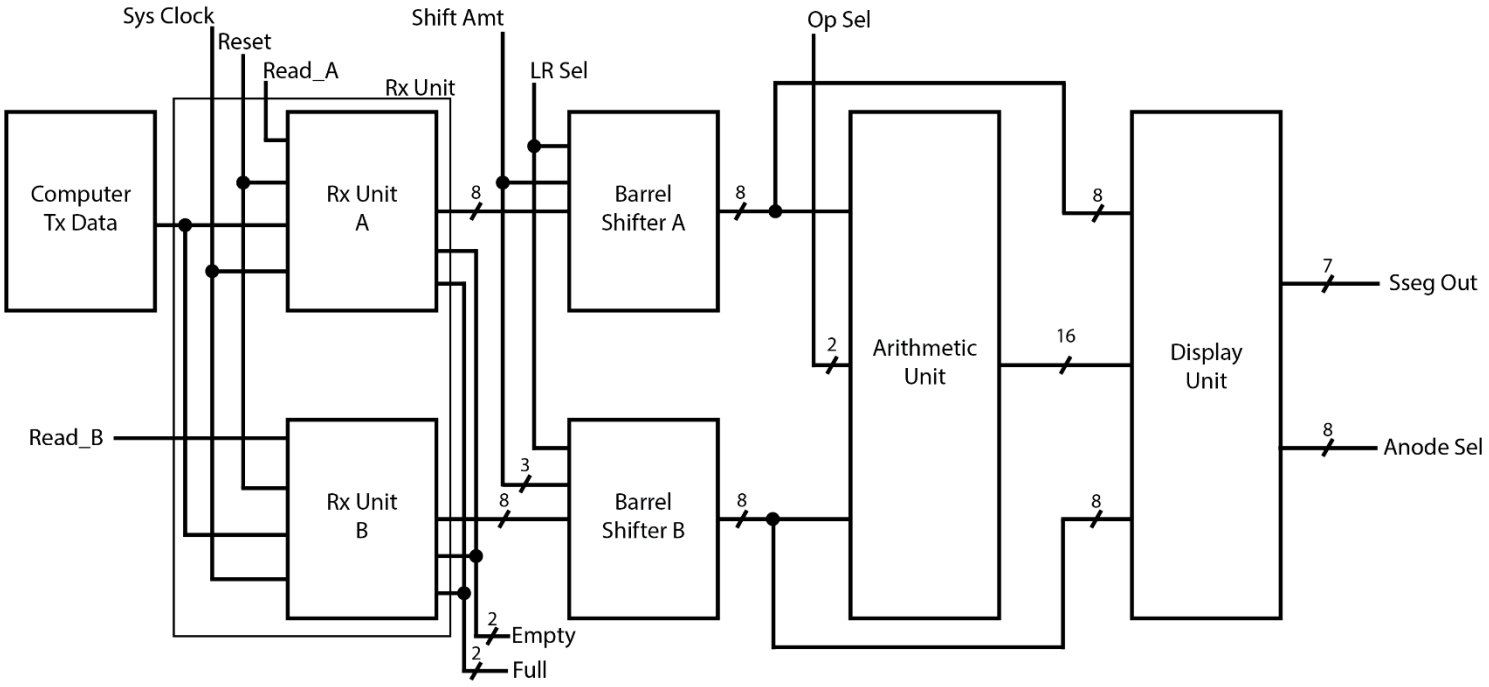
ECE 4304 – 01

Lab 7: UART System

Architecture:

The objective of this lab was to take in data via UART from a computer and output that data onto the board's sseg displays. Before displaying the data, it is first passed through a fifo, barrel shifter, and an arithmetic unit. The control signals sent to the board are how much to shift the data, the direction to shift, and what operation to perform. The board also indicates whether either of the two fifos are full or empty via LEDs. The system hardware architecture is shown below.



Tricks of the Code:

In order to read from a FIFO one at a time the buttons must be debounced or else the FIFO will empty immediately. Each FIFO has their own debounced button for independent reading.

```
DB_COMP_A: debounce_unit
  port map (
    i_db_clk => i_top_clk,
    i_db_rst => i_top_rst,
    i_db_btn => i_top_inst(7),
    o_db_new => temp_db_btn(1)
    );

DB_COMP_B: debounce_unit
  port map (
    i_db_clk => i_top_clk,
    i_db_rst => i_top_rst,
    i_db_btn => i_top_inst(6),
    o_db_new => temp_db_btn(0)
    );
```

Since there is only one Tx unit but two FIFO buffers, a mux is used to write one at a time. Once the first buffer is full, then the second FIFO will be written to until full.

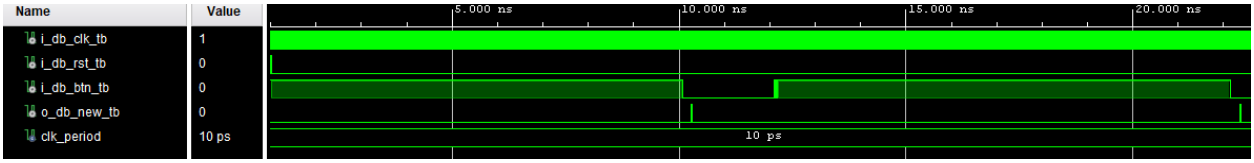
```
begin
  if(rising_edge(i_rx_clk)) then
    if (temp_full_a = '1') then
      temp_data_b <= i_rx_data;
    else
      temp_data_a <= i_rx_data;
    end if;
  end if;
end process;
```

The display unit is capable of displaying both the FIFO data and the arithmetic operation output.

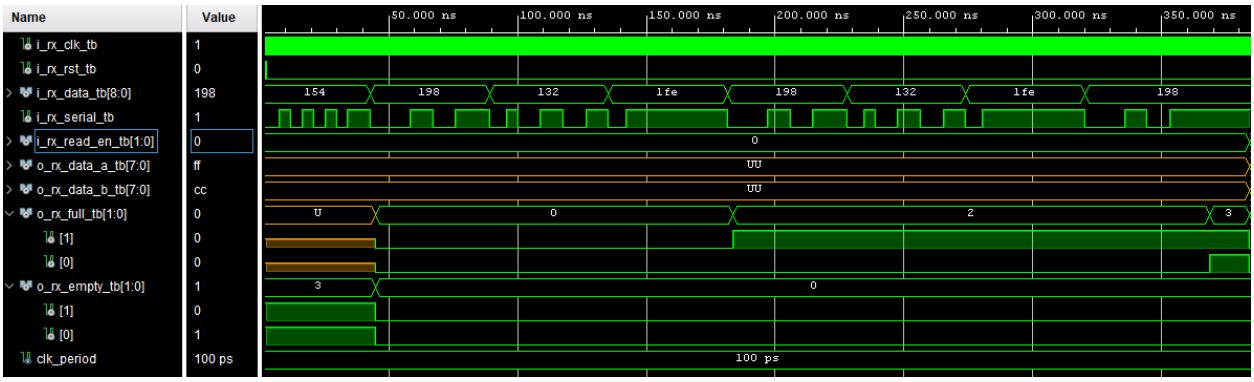
```
DISP_COMP: display_unit
  port map(
    i_disp_clk => i_top_clk,
    i_disp_rst => i_top_rst,
    i_disp_bs_a => temp_data_a_new,
    i_disp_bs_b => temp_data_b_new,
    i_disp_au => temp_data_au,
    o_disp_sseg => o_top_sseg,
    o_disp_an => o_top_an,
    o_disp_dp => o_top_dp
    );
```

Testbench:

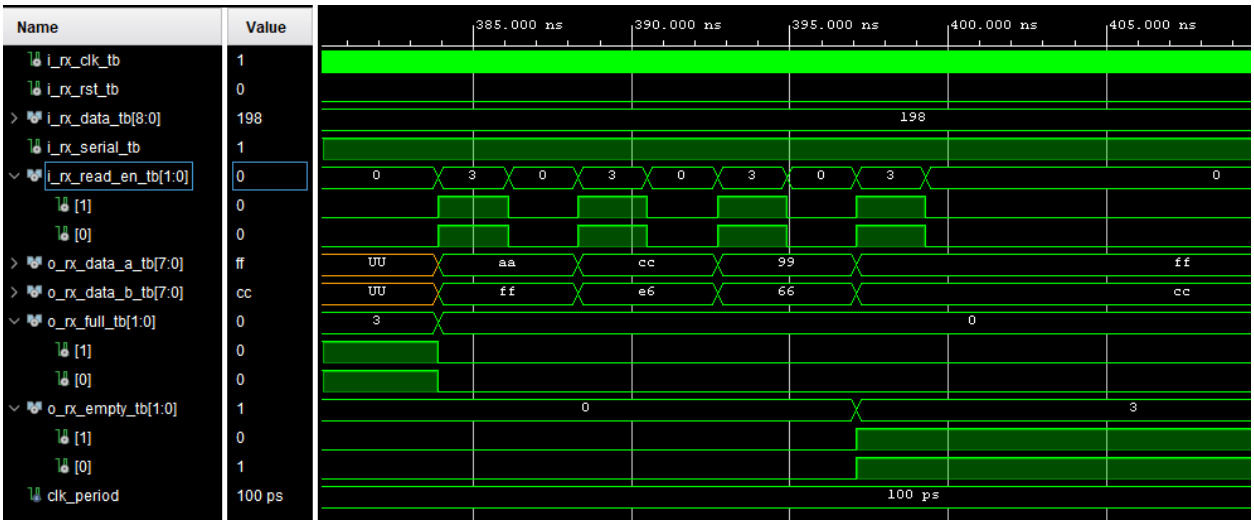
Debouncing Circuit



Rx Unit Filling FIFO



Rx Unit Emptying FIFO



Area/Resources:

Entire System

✓ synth_1	constrs_1	synth_design Complete!								445	212	0.0	0	0
✓ impl_1	constrs_1	write_bitstream Complete!	5.955	0.000	0.191	0.000	0.000	0.120	0	430	212	0.0	0	0

1 Barrel Shifter

✓ synth_1	constrs_1	synth_design Complete!								24	0	0.0	0	0
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	4.734	0	24	0	0.0	0	0

1 Debouncing circuit

✓ synth_1	constrs_1	synth_design Complete!								17	21	0.0	0	0
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	0.331	0	17	21	0.0	0	0

Rx Unit

✓ synth_1	constrs_1	synth_design Complete!								103	88	0.0	0	0
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	2.454	0	102	88	0.0	0	0

Arithmetic Unit

✓ synth_1	constrs_1	synth_design Complete!								186	65	0.0	0	0
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	9.386	0	185	65	0.0	0	0

Display Unit

✓ synth_1	constrs_1	synth_design Complete!								68	17	0.0	0	0
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	5.799	0	68	17	0.0	0	0