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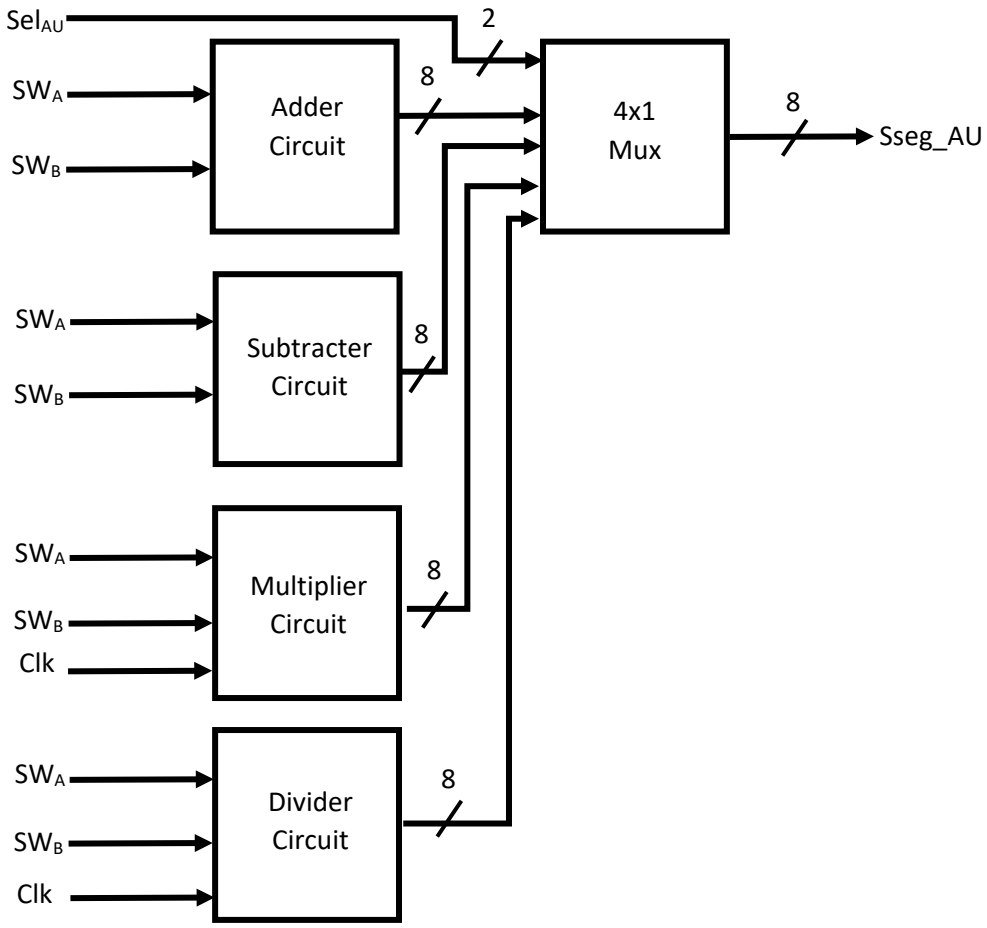
ECE 4304 – 01

Lab 5: Arithmetic Unit

Architecture:

The objective of this lab is to take in two 4 bit values and then output the result. The result comes from the arithmetic unit which can perform addition, subtraction, multiplication, and division. Two other outputs are the input switches which can be either in hex or bcd. There are 4 total instruction bits: 2 for the AU, 1 for the A value, and 1 for the B value. The main diagram can be found in the "Lab5_Diagram.png." Below is the construction of the arithmetic unit.



Tricks of the code:

The adder circuit also doubles as a subtractor.

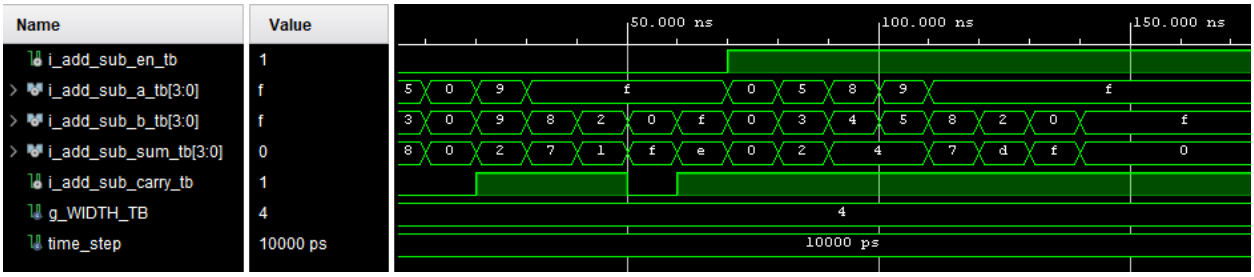
```
entity add_sub is
  generic (g_WIDTH_AS: integer := 4);
  port (
    i_add_sub_sel   : in  std_logic;
    i_add_sub_a     : in  std_logic_vector(g_WIDTH_AS - 1 downto 0);
    i_add_sub_b     : in  std_logic_vector(g_WIDTH_AS - 1 downto 0);
    o_add_sub_sum   : out std_logic_vector(g_WIDTH_AS - 1 downto 0);
    o_add_sub_carry : out std_logic
    );
end add_sub;
```

Splitting up the data via a register helps with data flow and timing.

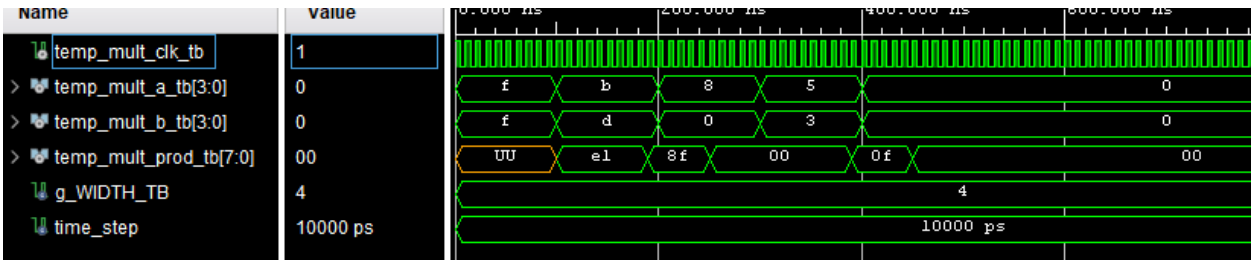
```
REG_COMP: data_register
  generic map (g_WIDTH_REG => g_WIDTH_A)
  port map (
    i_reg_clk  => i_port_a_clk,
    i_reg_data => temp_BCD,
    o_reg_data => o_port_a_data
    );
```

Testbench:

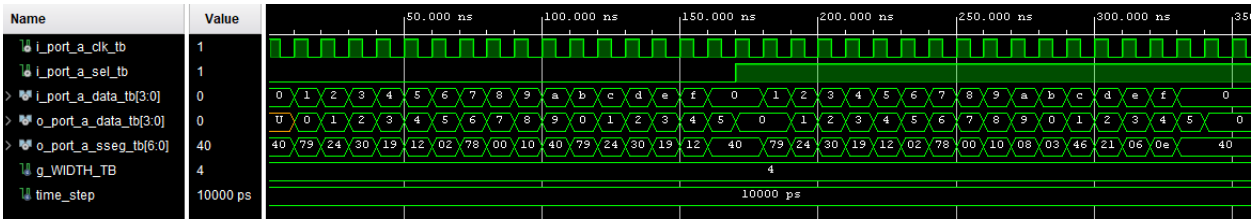
Adder Subtractor Circuit



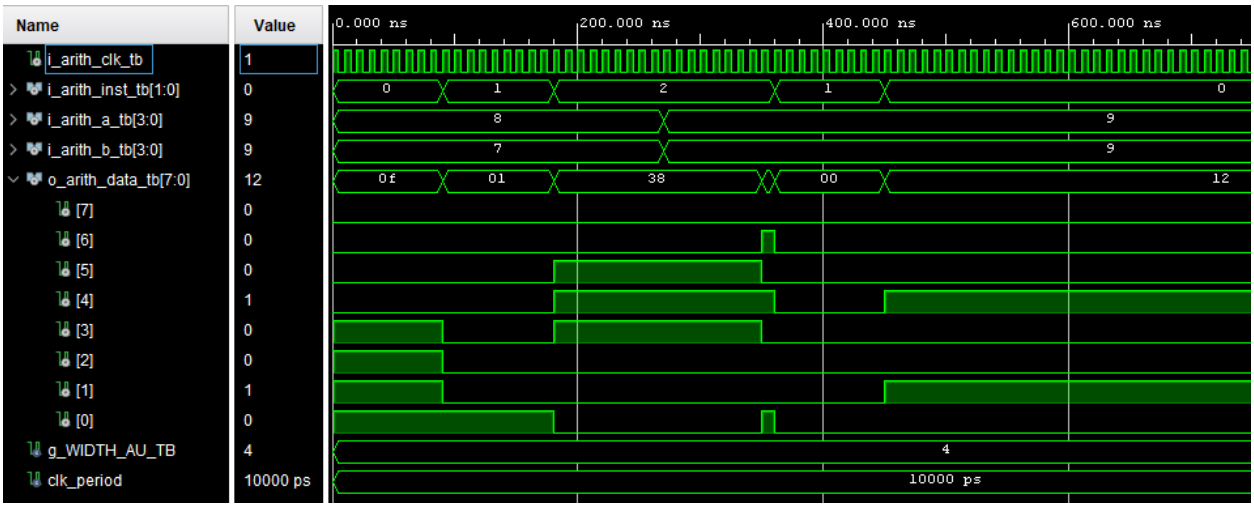
Multiplier Circuit



Port A/B Output Circuit



Arithmetic Unit Circuit



Area/Resources:

Without Divider Circuit

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
synth_1	constrs_1	synth_design Complete!								63	53	0.0	0	0
impl_1	constrs_1	write_bitstream Complete!	6.654	0.000	0.178	0.000	0.000	0.112	0	61	53	0.0	0	0

With Divider Circuit

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
synth_1	constrs_1	Synthesis Out-of-date								90	61	0.0	0	0
impl_1	constrs_1	write_bitstream Complete!	5.893	0.000	0.161	0.000	0.000	0.112	0	86	61	0.0	0	0