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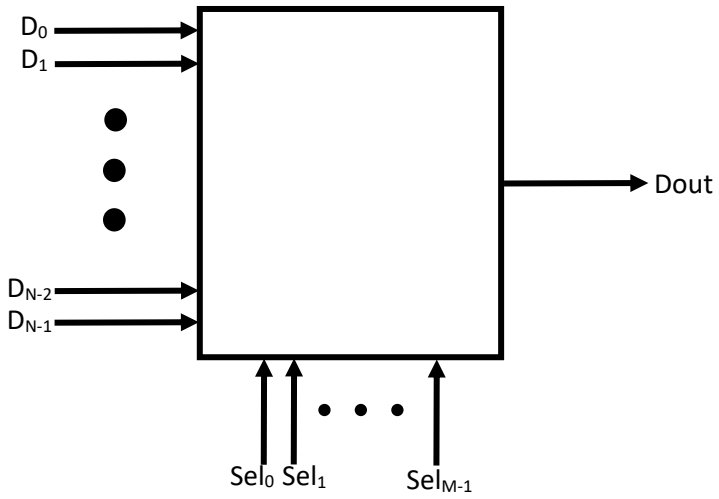
ECE 4304 – 01

Lab 1: Network of Multiplexers

Architecture:

The objective was to create a reconfigurable multiplexer from 4x1 up to Nx1, made up from a network of 2x1 multiplexers with M amount of select bits ($M = \log_2(N)$).



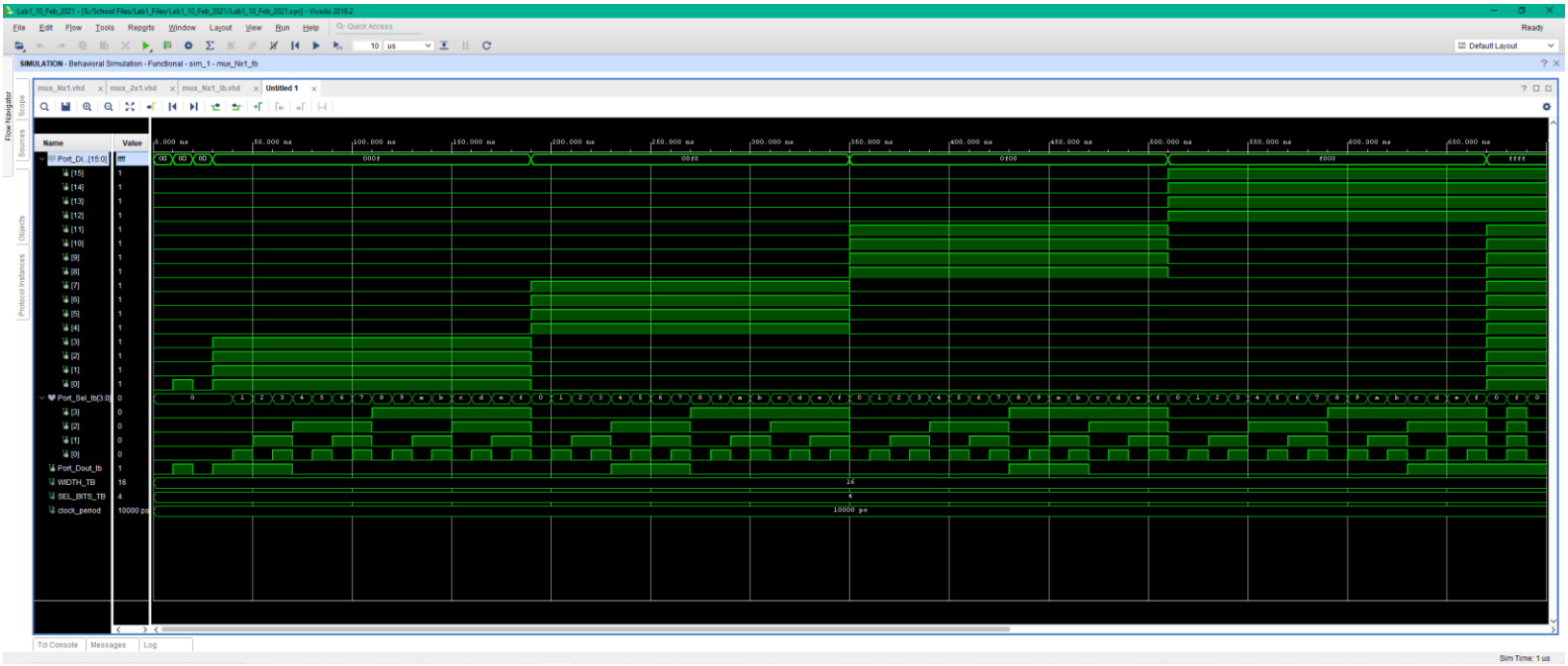
Tricks of the code:

The use of a nested for generate loop is utilized to aid in creating a properly connected network of 2x1 multiplexers for any variation. The first loop generates the select bits from 0 to M-1. The second loop generates the appropriate amount of multiplexers based on what select bit, or level, it is on. For example if creating an 8x1 mux the first level will generate 0-3, the second 4-5, and the last 6 so it creates a total of 7 muxes.

```
GEN_MUX_LEVELS: for i in 0 to SEL_BITS-1 generate
    MUX_PER_LEVEL: for j in WIDTH - 2**(SEL_BITS - i) to WIDTH - 2**(SEL_BITS - i - 1) - 1 generate
```

Testbench:

The input/output text files are added to github but excluded from this report. The output waveform below shows a functioning 16x1 multiplexer with 4 select bits. It first leaves select as 0 but changes the 0 input bit from 0 to 1 and back. The output value follows exactly the same. Then the following simulation starts at 000F and shifts by 4, where the following would be 00F0, it shifts after the select goes from 0-15 each time to ensure only the bits which are 1 will ever output a 1. The last input is FFFF and if the select is 0 or F the output is still 1, which is expected.



Area/Resources:

For a 16x1 Multiplexer

Tcl Console | Messages | Log | Reports | **Design Runs**

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
✓ synth_1	constrs_1	synth_design Complete!								4	0	0.0	0	0
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	1.950	0	4	0	0.0	0	0

For a 32x1 Multiplexer

Tcl Console | Messages | Log | Reports | **Design Runs**

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
✓ synth_1	constrs_1	synth_design Complete!								9	0	0.0	0	0
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	2.351	0	9	0	0.0	0	0

For a 64x1 Multiplexer

Tcl Console | Messages | Log | Reports | **Design Runs**

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
✓ synth_1	constrs_1	synth_design Complete!								17	0	0.0	0	0
✓ impl_1	constrs_1	route_design Complete!	NA	NA	NA	NA	NA	2.846	0	17	0	0.0	0	0