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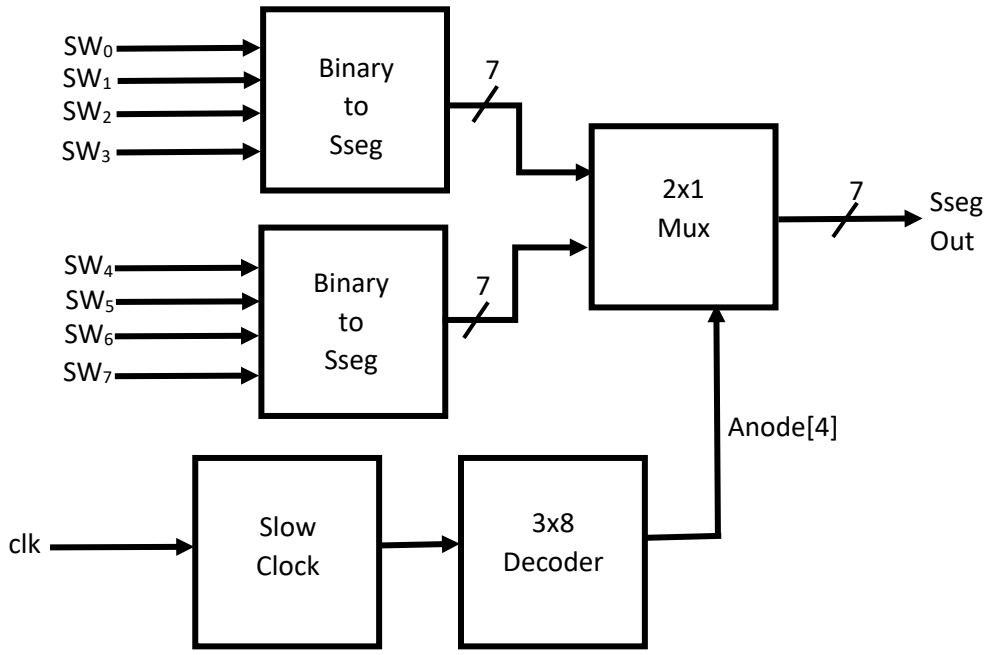
ECE 4304 – 01

Lab 3: Using Seven Segment Displays

Architecture:

The objective of this lab is to use two seven segment displays each with their own bcd input switches. This can be accomplished by instantiating two binary-to-sseg converters where it takes in the bcd input and outputs the respective seven segment representation. The output of these two converters can be tied to a multiplexer so only one set of data is displayed at a time while also alternating through the anodes. Due to the timing constraints of the displays, the internal 100MHz clock must be slowed down to allow ample time for the data to pass.



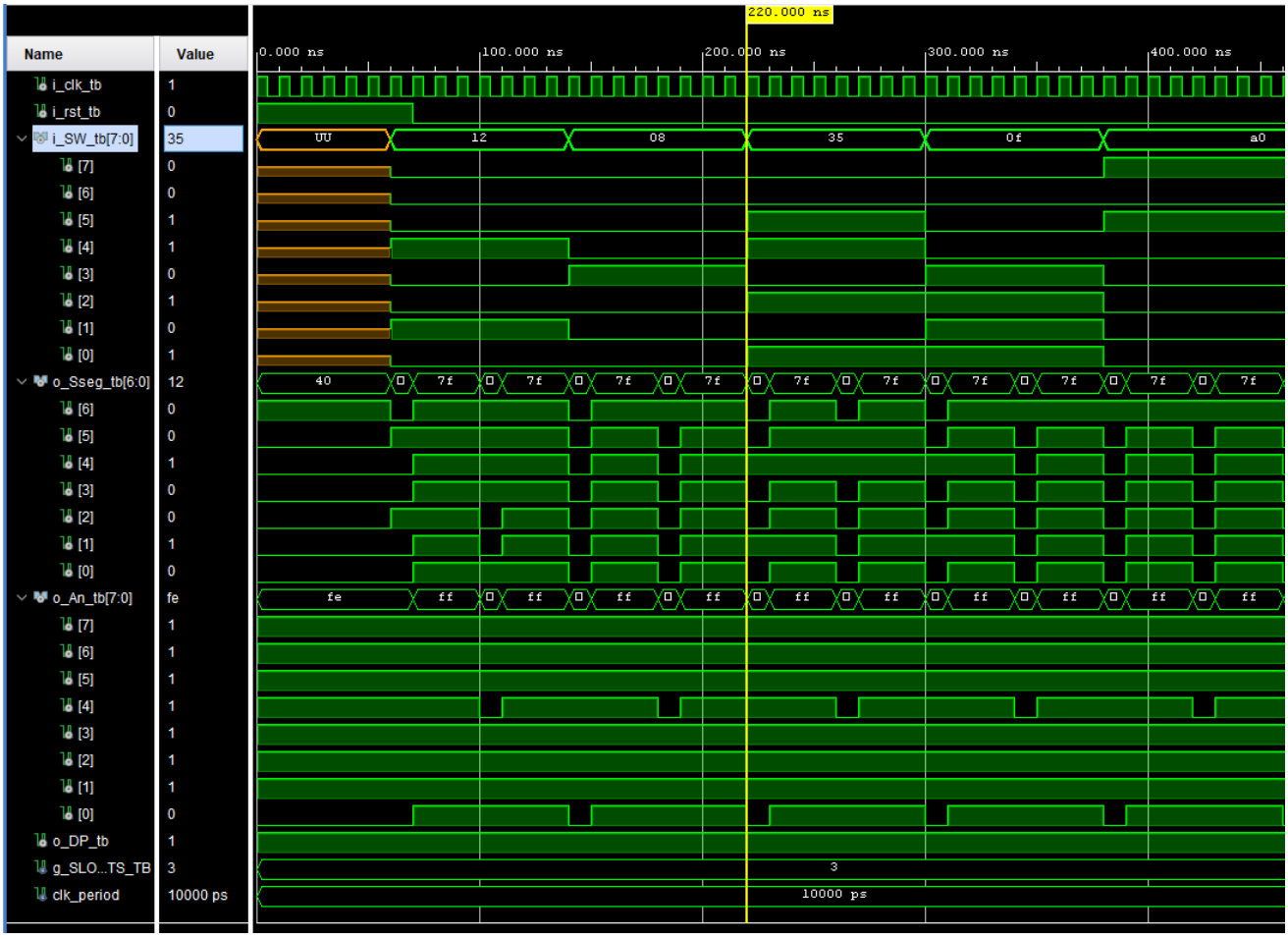
Tricks of the code:

Most of the code is straight forward such as the decoder and the mux. The slow clock is simply a counter with a large amount of bits to count to. The converter from binary to bcd can be seen below where it is only valid from 0 to 9 and anything above that should be added with 6 so that there is a carry out value while the current digit remains valid.

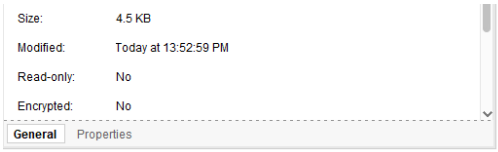
```
begin
    if i_Binary > x"9" then -- If th
        v_Binary := i_Binary + 6;
    elsif i_Binary <= x"9" then --If
        v_Binary := i_Binary;
    else -- If no condition is met t
        v_Binary := (others => '0');
    end if;
```

Testbench:

The testbench covers the standard usage as well as a few corner cases. It can be seen that the anodes are driven low on both 0 and 4 where it enables those seven segment locations. When the enables are driven low the data that is in the switch value is outputted in the sseg format. In the last two switch value inputs the entity is tested to see what occurs when an invalid bcd is passed. As expected, if 15 in binary is given, the output will be 5. If a 10 is given the output will be a 0.



Area/Resources:



Resource	Utilization	Available	Utilization %
LUT	16	63400	0.03
FF	18	126800	0.01
IO	26	210	12.38
BUFG	1	32	3.13

Tcl Console | Messages | Log | Reports | Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed	Run Strategy
synth_1	constrs_1	synth_design Complete!								16	18	0.0	0	0	2/24/21, 1:53 PM	00:00:26	Vivado Synthesis Default
impl_1	constrs_1	write_bitstream Complete!	7.443	0.000	0.324	0.000	0.000	0.105	0	16	18	0.0	0	0	2/24/21, 1:54 PM	00:01:04	Vivado Implementation D