Peter Anthony

Michael Cavins

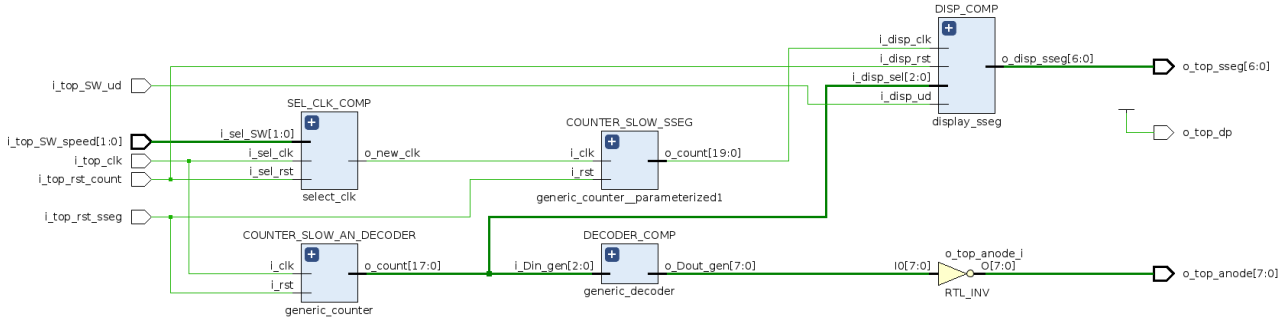
Andres Colon

ECE 4304 – 01

Lab 4: Seven-Segment BCD counter

Architecture:

The objective of this lab was to display a counter where it counts from 00,000,000 to 99,999,999 and then resets based on the direction in which to count in. The speed at which the counter counts at can be varied based on 2 switches which gives a total of 4 counter options. The reset for the ssegs and for the counter are independent to each other.

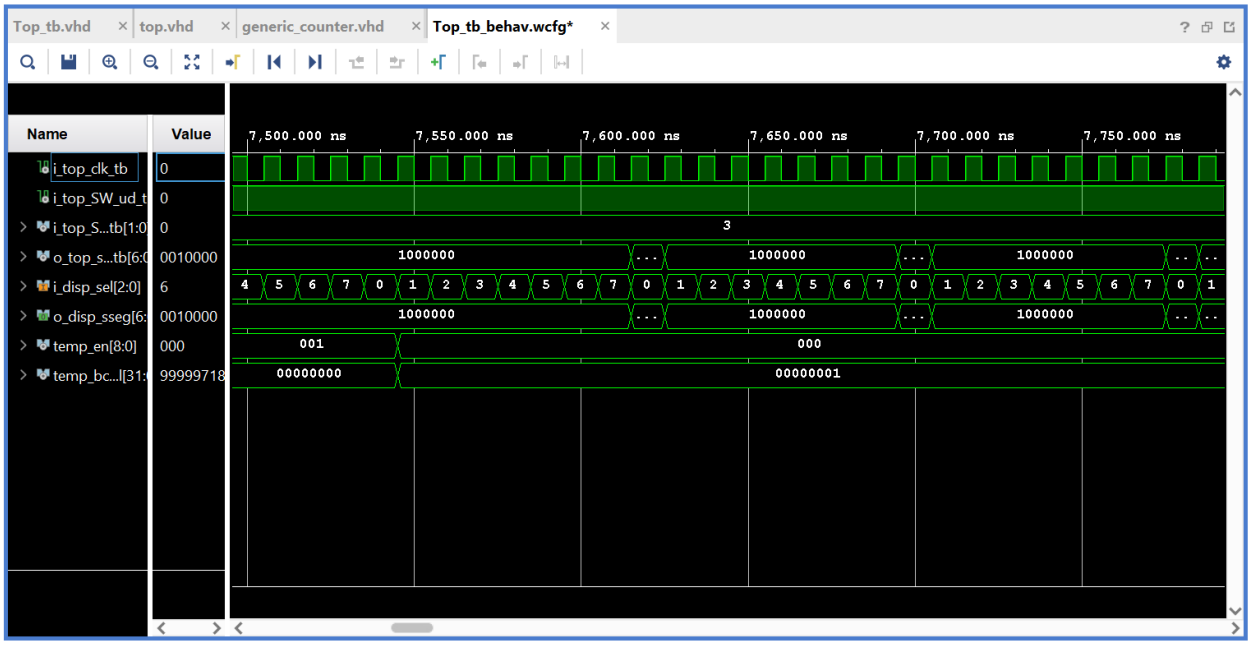


Tricks of the code:

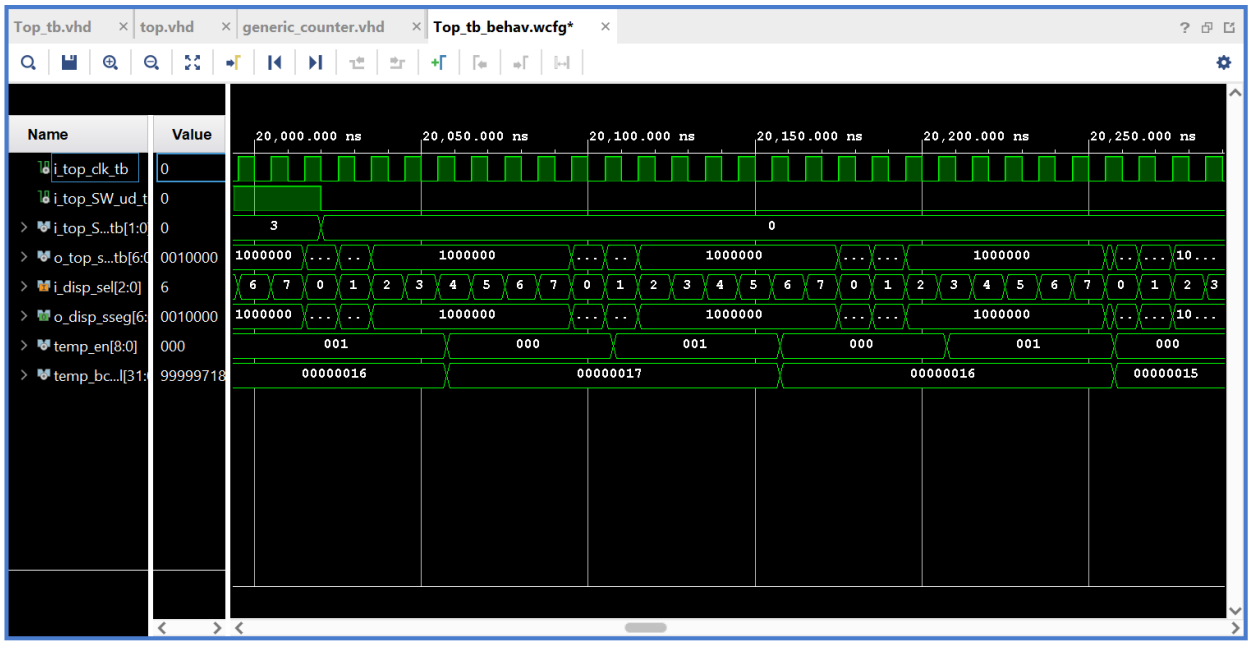
The main trick to this counter is that the clock speed can be changed if desired by making use of the pll. The outputs of each of the pll are used along lock to create a stable clock. The clocks are then multiplexed which can be changed by two switches on the board.

```
PLL_CLK_COMP: clk_wiz_0
port map(
    i_clk_sys  => i_sel_clk,        -- Map the top clock with the input for the pll
    reset      => i_sel_rst,        -- Map the top reset with the input for the pll
    o_pll_10   => temp_pll_clk_10,  -- Output the 10MHz clock
    o_pll_50   => temp_pll_clk_50,  -- Output the 50MHz clock
    o_pll_100  => temp_pll_clk_100, -- Output the 100MHz clock
    o_pll_200  => temp_pll_clk_200, -- Output the 200MHz clock
    locked     => temp_pll_lock     -- Output the current locked value
    );

--  utilizes lock from pll clock to make sure only stable clocks are being used
stable_clk_10  <= temp_pll_clk_10 and temp_pll_lock;
stable_clk_50  <= temp_pll_clk_50 and temp_pll_lock;
stable_clk_100 <= temp_pll_clk_100 and temp_pll_lock;
stable_clk_200 <= temp_pll_clk_200 and temp_pll_lock;

-- Concatenate all stable clocks so it can be formatted for the multiplexer
temp_clk_in    <= stable_clk_10 & stable_clk_50 & stable_clk_100 & stable_clk_200;

-- Creates a 4x1 multiplexer with each data set size of 1 bit
MUX_4x1: generic_mux_Nx1
    generic map(g_WIDTH_MUX_DATA => 1, g_MUX_INPUTS => 4)
    port map(
        i_mux_sel  => i_sel_SW,        -- Map the top select switches for the multiplexer
        i_mux_data => temp_clk_in,     -- Input the newly formatted clock data
        o_mux_data => temp_current_clk -- output the selected clock
        );
```

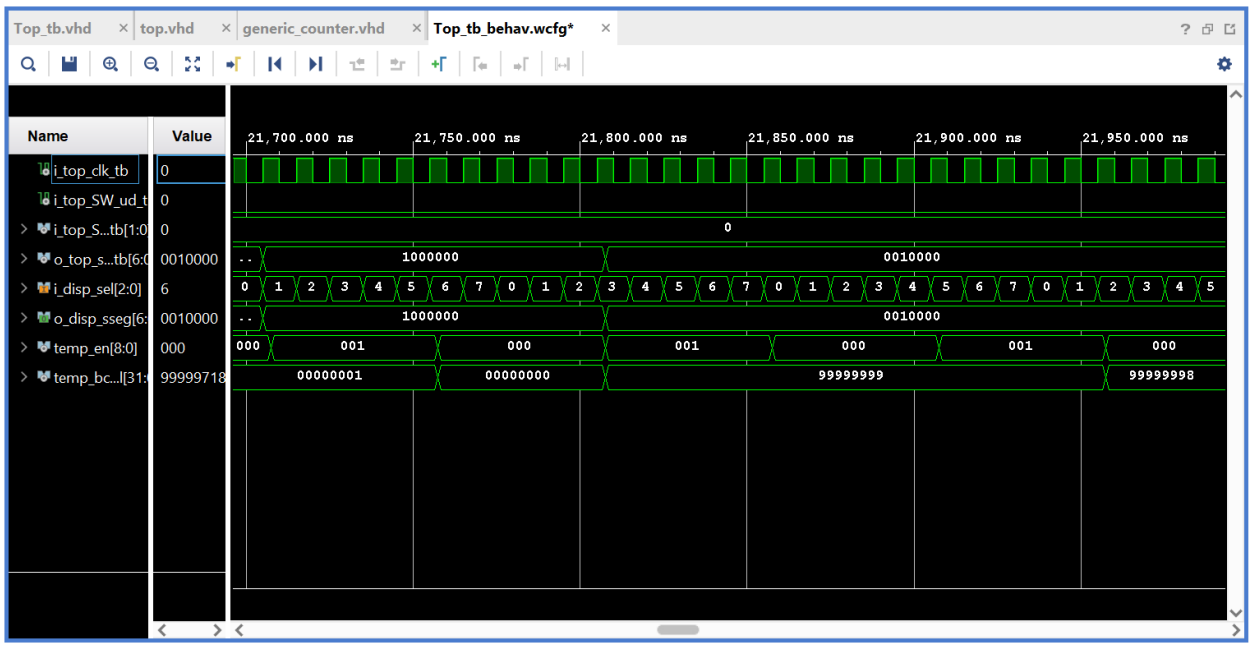
Testbench:



Counter is set to count up.



Counter is set to count down.



Corner case for when BCD counter counts backwards from 0.

Area/Resources:

Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	129	63400	0.20
FF	94	126800	0.07
IO	22	210	10.48
BUFG	5	32	15.63
PLL	1	6	16.67

Power

Total On-Chip Power:	**0.233 W**
Junction Temperature:	**26.1 °C**
Thermal Margin:	58.9 °C (12.8 W)
Effective ϑJA:	4.6 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

RC | Methodology | Power | Timing | **Utilization**

Hierarchy

Name	Slice LUTs (63400)	Slice Registers (126800)	F7 Muxes (31700)	Slice (15850)	LUT as Logic (63400)	Bonded IOB (210)	BUFGCTRL (32)	PLLE2_ADV (6)
top	129	102	22	55	129	22	5	1
COUNTER_SLOW_AN_DECODER (generic_counter)	5	18	0	7	5	0	0	0
COUNTER_SLOW_SSEG (generic_counter__parameterized1)	1	20	0	5	1	0	0	0
DISP_COMP (display_sseg)	121	64	22	41	121	0	0	0
SEL_CLK_COMP (select_clk)	2	0	0	2	2	0	5	1