Peter Anthony

Michael Cavins

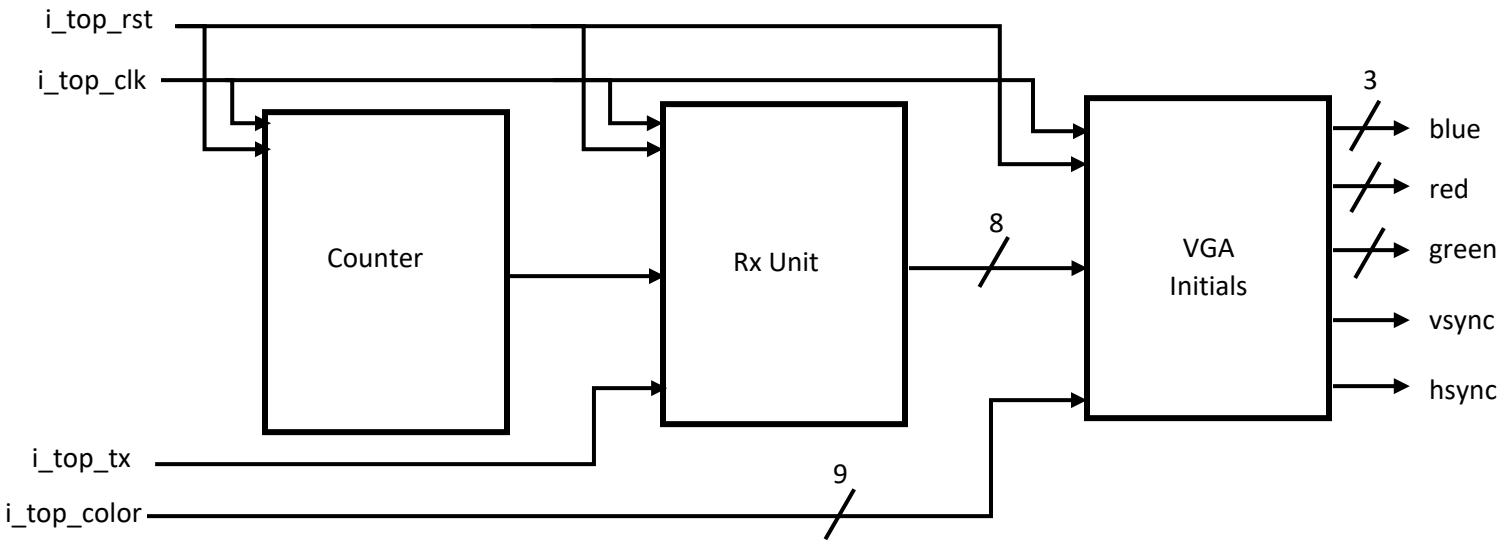
Andres Colon

ECE 4304 – 01

Lab 8: VGA System

Architecture:

The objective of this lab was to create a system that takes in UART data and switch data to control both the color and location of the icon on the VGA display. The current designed system uses one counter, one Rx fifo buffer, and one VGA control unit. The counter is used to control the reading of the fifo so it is not always reading. The Rx unit is used in order to take in the serial data from the UART terminal port and store it in a fifo buffer. The VGA control unit is what determines the logic for the image used as well as creating a proper VGA display output.



Tricks of the Code:

By using a counter with an output tick there is a limit on when to read the fifo. This gives enough time for the UART data to be sent to the fifo before being read prematurely. The read data is what is sent to control the location of the VGA sprite/image.

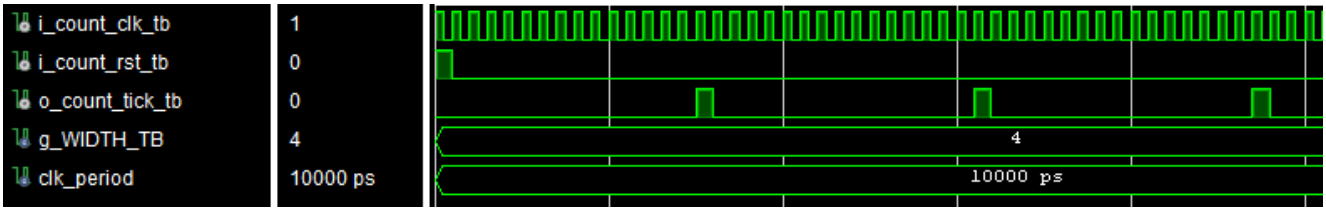
```
COUNT_COMP: generic_counter
  generic map(g_WIDTH_COUNTER => 7)
  port map(
    i_count_clk  => i_top_clk,
    i_count_rst  => i_top_rst,
    o_count_tick => s_enable
    );

RX_COMP: UART_RX
  generic map (g_CLKS_PER_BIT => rx_clks_per_bit)
  port map (
    i_Clk        => i_top_clk,
    i_reset      => i_top_rst,
    i_RX_Serial  => i_top_tx,
    ReadEn       => s_enable,
    DATAOUT_FIFO => s_rx_data,
    Empty        => open,
    Full         => open
    );
```

Within the output color process, creating an offset based on the switch input allows for the variation in VGA color.

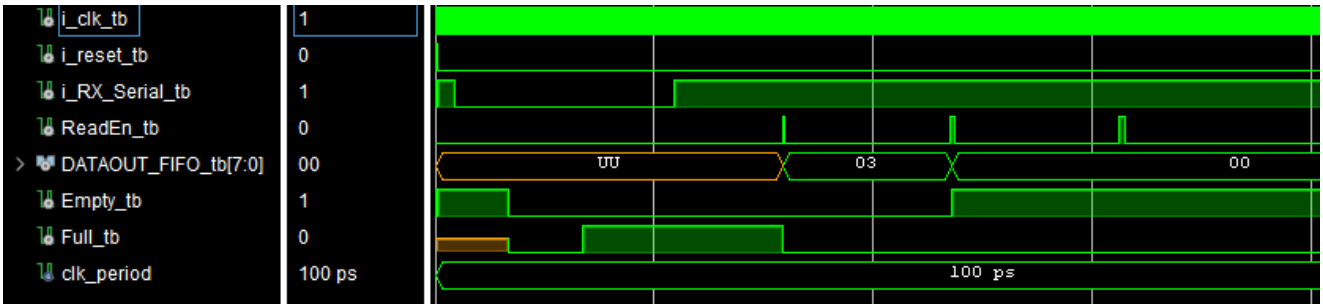
```
R <= M(conv_integer(rom_pix - SW(2 downto 0)));
G <= M(conv_integer(rom_pix - SW(5 downto 3)));
B <= M(conv_integer(rom_pix - SW(8 downto 6)));
```

Testbench:

Counter



Rx Unit



Area/Resources:

Top Design

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
✓ **synth_1** (active)	**constrs_1**	**synth_design Complete!**								**141**	**77**	**0.0**	**0**	**0**
✓ impl_1	constrs_1	write_bitstream Complete!	8.064	0.000	0.103	0.000	0.000	0.224	0	140	83	0.0	0	0