

HYBRID SWITCHED-CAPACITOR CIRCUITS  
AND MAGNETICS CO-DESIGN FOR VERTICAL  
POWER DELIVERY

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# Abstract

The increasing demands of high-performance computing, driven by widespread adoption of artificial intelligence, necessitate power electronics that are energy efficient, have high power densities, and respond quickly to load transients. Power architectures must leverage advances in semiconductors, passive components, and heterogeneous integration for high density, efficiency, and speed. Vertical power delivery is a promising approach to improving end-to-end efficiency in power conversion for high density loads by reducing interconnect resistance, electromagnetic interference, and converter area.

This thesis introduces the challenges of vertical power delivery for microprocessor applications, which require high efficiency, power density, and control bandwidth. These metrics are crucial for thermal performance, power and signal integrity, and packaging. A *vertical stacked heterogeneous packaging model* is proposed for vertical-stacked converters, optimizing the function of the capacitor, switch, and magnetics layers, exploiting their scaling laws for compact packaging.

Next, a hybrid switched-capacitor magnetics architecture is introduced that addresses the necessary tradeoffs for vertical power delivery – the *Linearly-Extendable Group-Operated Point-of-Load (LEGO-PoL) architecture* – together with multiple critical techniques to achieve high performance. The LEGO-PoL architecture uses a hybrid switched-capacitor topology together with coupled magnetics and vertical-stacked packaging to deliver high output currents within a small area with low height and high efficiency. Two LEGO-PoL prototypes are built and tested to validate the architecture for vertical power delivery. The first LEGO-PoL prototype has a height of 16.65 mm and delivers 450 A of current for 48-V-to-1-V conversion with 88.4% peak efficiency and 294 W/in<sup>3</sup> power density. The second prototype, *Mini-LEGO*, re-designs the converter with a height of 8.4 mm and a peak efficiency of 84.1%, trading off some efficiency for a significant improvement in power density to 1390 W/in<sup>3</sup>.

Lastly, by merging and coupling multiple magnetic components into one, benefits in size reduction, performance improvement, and control bandwidth are achieved. This thesis quantifies the benefits of coupled magnetics and introduces geometries and optimization methods for vertical power delivery coupled inductors. Three inductors are fabricated to demonstrate the magnetics design methodology for vertical coupled inductors at frequencies of 1 MHz, 1.5 MHz, and 2 MHz. The pinwheel coupled inductor design presented for 2 MHz underscores the vision for vertical magnetics with power-via interconnects that deliver high current with low profile and low impedance.

The LEGO-PoL architecture and the development of vertical coupled magnetics pave the way for vertical power delivery as a promising approach to resolving the tradeoffs of performance, size, and speed, and meeting the growing energy demands of future high power density applications.

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# Chapter 1

## Introduction

### 1.1 Power Electronics for High-Density Loads

Power electronics converters enable efficient conversion of electrical energy between different forms, voltages, and currents. For high-density loads where a large amount of power needs to be delivered within a constrained area and volume, such as the emerging data center industry, LED arrays, modular battery storage systems, and high power lasers, power electronics are required that can deliver a concentrated amount of power with high performance. These converters need to be ultra dense with good efficiency, thermal performance, and reliability.

The computing industry is a good example of a high-density load that illustrates the need for advancements in power electronics. A new era of human history, the “information age,” has been enabled by the proliferation of computing devices that can solve extremely complicated problems with ease. Recently, artificial intelligence and cloud computing have propelled the microprocessor industry to new heights, and high performance chips designed for these applications are consuming power on the order of kilowatts, and upwards of 1000 A of current within a few square centimeters of chip area [1].

Power electronics for high-density loads face a fundamental challenge: how does a converter deliver extreme amounts of current to increasingly smaller areas and volumes while maintaining efficiency and with fast response times to load variations? Traditional power supplies employing conventional architectures use simple architectures with multiple individualized components and are sized for a specific application. They lack innovations on the architectural side that can synergistically combine functionalities of different components to break trade-offs and achieve mutual benefits, and they lack the modularity and scalability required for high-density load systems often composed of multiple parallel units.

To address these problems and re-think power electronics design, holistic innovations are required in architectures, materials, devices, and packages. **While the remainder of this thesis focuses specifically on microprocessor power delivery as a demonstrative example, the theories and methods developed in this thesis are widely applicable to a variety of applications where a concentrated amount of power is delivered in a small area with high efficiency, density, and speed, such as LED drivers and radio frequency envelope trackers.**

Two driving concepts that focus this thesis on answering the question posed above are discussed in this introduction. The first regards the scaling laws of the three fundamental building blocks of power electronics: 1) capacitors, 2) semiconductor devices, and 3) magnetics. By understanding how to extract the optimum performance and size of each of these components, architectures can be developed to exploit these scaling trends. The second concept is scalability. Scalability is the property of an architecture to modularly expand or contract for different power ratings and applications without the need to re-design an entirely new architecture. Architectures that leverage scalability as a way to enhance the overall operation can achieve a good mid-

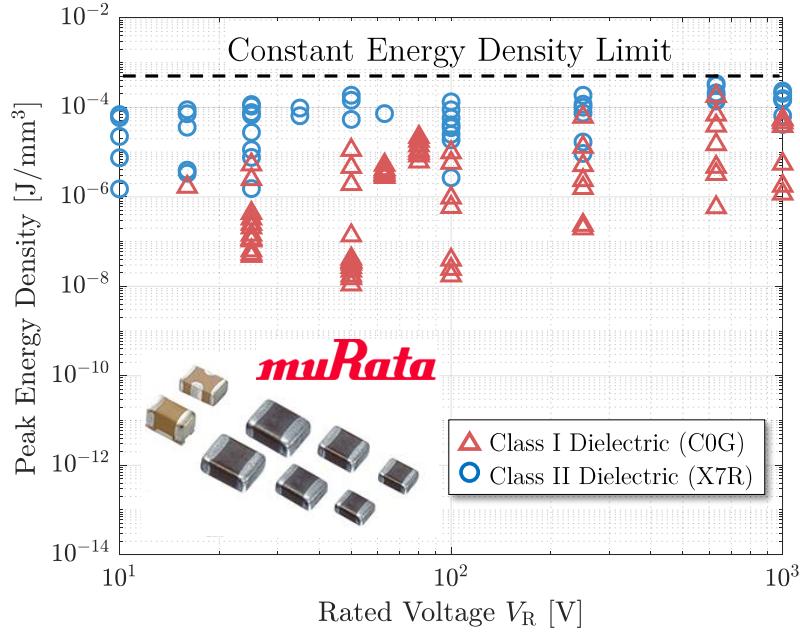


Figure 1.1: Plot of the capacitor energy density of multilayer ceramic capacitors sampled from Murata’s database and re-plotted from data provided in [2]. Regardless of the size and voltage rating, there is a constant energy density limit for capacitors. Capacitors are relatively indifferent to scaling in either of these parameters.

idle ground towards designing power converters that are customized to exploit scaling laws while maintaining the flexibility to power a wide variety of loads.

### 1.1.1 Power Component Scaling Laws

#### Capacitors

Capacitors are one of the two major passive components in power electronics circuits. They have many important functions in a circuit, including filtering, blocking dc voltages, and forming resonant second-order circuits along with magnetic components.

Capacitors store energy in an electric field between two parallel plates. The peak energy density of a capacitor is equal to  $\epsilon E_c^2 = \frac{1}{2}CV_R^2$ , where  $\epsilon$  is the dielectric constant of the material between the two parallel plates,  $E_c$  is the critical electric field of the dielectric before it breaks down,  $C$  is the capacitance of the capacitor, and  $V_R^2$  is the rated breakdown voltage of the capacitor.

Capacitors are extremely energy dense. Figure 1.1 plots the energy density of a sampled database of capacitors from Murata, re-plotted from [2]. Different sizes of capacitors and different voltage rated capacitors are shown. It can be observed that regardless of the voltage or capacitor size, there is a constant energy density limit. If one capacitor with capacitance of  $C$  and voltage rating  $V$  is replaced with three smaller capacitors with a smaller voltage rating of  $\frac{1}{3}V$  and a capacitance  $3C$ , a similar total volume will be occupied [3].

In summary, capacitors are *indifferent* to scaling their voltage rating and their dimensions. In practice, implementing large capacitors with small granular capacitors may offer increased flexibility in design, such as in switched-capacitor energy buffer circuits [4].

## Semiconductor Devices

Semiconductor devices are at the heart of power electronics. In switched mode power supplies, semiconductor devices are able to modulate their state from on, where current is conducted, to off, where voltage is blocked. Currently, silicon devices (MOSFETs, IGBTs, and diodes) are the most commonly used in power electronics circuits. As emerging applications demand higher blocking voltages (dc grid infrastructure) and higher frequencies (high-density loads where higher frequency can enable smaller size), wide-bandgap materials (WBG) such as silicon carbide (SiC) and gallium nitride (GaN) developing to address these concerns. Figure 1.2a illustrates the landscape of power semiconductor devices. GaN devices exhibit good performance at higher switching frequencies as a result of their high electron mobility, while SiC devices excel in high power applications with their high thermal conductivity and robustness at high temperatures [5, 6].

The higher bandgap of GaN and SiC also enables a higher critical electric field, which results in a shorter channel length needed for the same breakdown voltage as

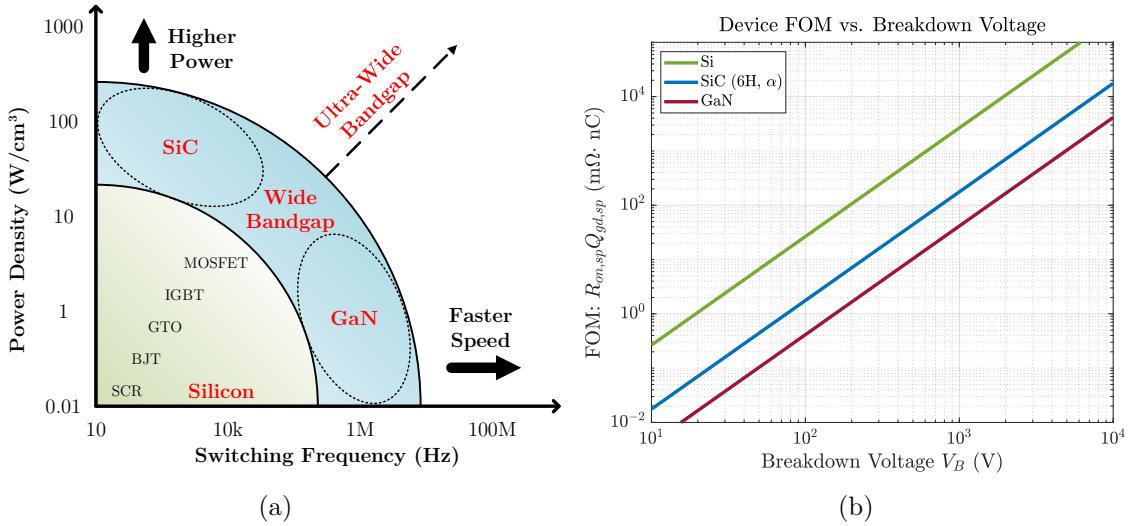


Figure 1.2: (a) Power semiconductor device application range depending on switching frequency and target power level. (b) Plot of the figure-of-merit  $R_{on,sp}Q_{gd,sp}$  vs. breakdown voltage for Si, SiC, and GaN devices [7]. As  $V_B$  increases, the FOM quadratically increases.

a silicon device. As a result of the shorter channel length, WBG devices have lower on-resistance ( $R_{on}$ ) than silicon devices, and occupy smaller packages. In order to quantify the performance of power semiconductor devices, a figure-of-merit (FOM) is defined. The theoretical minimum losses of a power semiconductor switch in a typical switched-mode power supply, introduced in [7], can be calculated as:

$$P_{loss,min} = \left( 2I_{rms} \sqrt{\frac{V_D I_D f}{I_g}} \right) \cdot \sqrt{R_{on,sp} Q_{gd,sp}}. \quad (1.1)$$

Here,  $I_{rms}$  is the root-mean-square (rms) current through the switch,  $I_D$  is the switch turn-on/turn-off current,  $I_g$  is the average gate current,  $V_D$  is the drain-to-source blocking voltage, and  $f$  is the switching frequency. The loss is directly proportional to the square root of two device parameters present in the equation, the on-resistance  $R_{on,sp}$  and the gate-to-drain charge  $Q_{gd,sp}$ . Thus, a suitable FOM to use to evaluate devices is  $R_{on,sp}Q_{gd,sp}$  [8, 9].

Figure 1.2b plots the FOM for Si, SiC, and GaN. The advantage of SiC and GaN over Si is apparent in the FOM. However, for all devices, the plot shows that as the

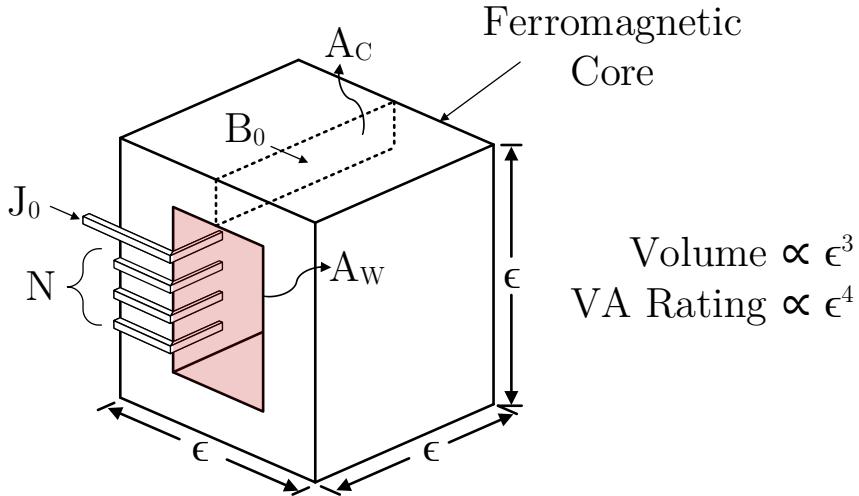


Figure 1.3: An example magnetic inductor component with dimensions  $\epsilon \times \epsilon \times \epsilon$ . The volume scales with  $\epsilon^3$ , while the power rating scales with  $\epsilon^4$ .

breakdown voltage of the device increases, the FOM increases quadratically. Since  $R_{on,sp}Q_{gd,sp} \propto V_B^2$  and  $V_D \propto V_B$ ,  $P_{loss,min} \propto V_B^{3/2}$ . If one large switch blocking voltage  $V_B$  is replaced by  $n$  switches in series, each blocking  $V_B/n$ , the theoretical minimum loss will be reduced by a factor of  $1/\sqrt{n}$ .

Therefore, *smaller power semiconductor devices are better*. Advantages arise when the blocking voltage across a switch can be distributed across many smaller switches. These smaller switches have better FOM, lower parasitics, and reduced overall resistance as a result. As a result of reduced parasitics, smaller switches can also operate at higher frequencies, which can help to further reduce the passive component size [10].

## Magnetics

Magnetic components are the second major passive component in power electronics converters. Magnetic components store energy in a magnetic field, and function as inductors and transformers to provide voltage conversion, filtering, isolation, as well as forming second-order circuits with capacitors. A typical inductor is implemented using a current-carrying conductor and a ferromagnetic “core” that guides the magnetic flux through a low reluctance path. Figure 1.3 shows an example inductor, with

a current density  $J_0$  through a winding with  $N$  turns. The core cross sectional area is  $A_c$ , the flux density in the core is  $B_0$ , and the “window” area in the center of the core is  $A_w$ .

The power density of this inductor depends on the maximum voltage and current ratings of the inductors. The maximum voltage depends on the flux density limit  $B_0$  within the cross-sectional area of the core  $A_c$ , which determines the flux linked by the winding  $\Phi = B_0 A_c$ . The voltage in a winding is proportional to the product of the number of turns  $N$ , the frequency  $f$ , and the flux linked by the winding. The maximum current rating for this inductor is determined by  $\frac{J_0 A_w}{N}$  [11]. The VA power rating is given by

$$\text{VA Rating} = V \cdot I = (N f B_0 A_c) \left( \frac{J_0 A_w}{N} \right) = f(B_0 J_0)(A_c A_w) \quad (1.2)$$

To understand how this scales with size, a linear dimension  $\epsilon$  is defined, and  $A_c A_w \propto \epsilon^4$ . Thus, the VA rating scales with  $\epsilon^4$ , while the overall inductor box volume scales with  $\epsilon^3$ . This means that the power density increases as the linear dimension  $\epsilon$  increases. There is a fundamental advantage to larger-scale magnetics. This opens up opportunities to integrate the functionality of many magnetic components into one large component that handles high VA, as opposed to using many small magnetic components handling small VA. To conclude, *larger magnetics are better* than smaller magnetics.

### 1.1.2 Architecture Scalability

The microprocessor industry has been shifting towards multi-core processors, where chiplet-based architectures that combine multiple smaller chips together are becoming the norm. Much like the scalability of chiplet systems, the scalability of the converters that power them is an important characteristic. Scalability in this context refers to the

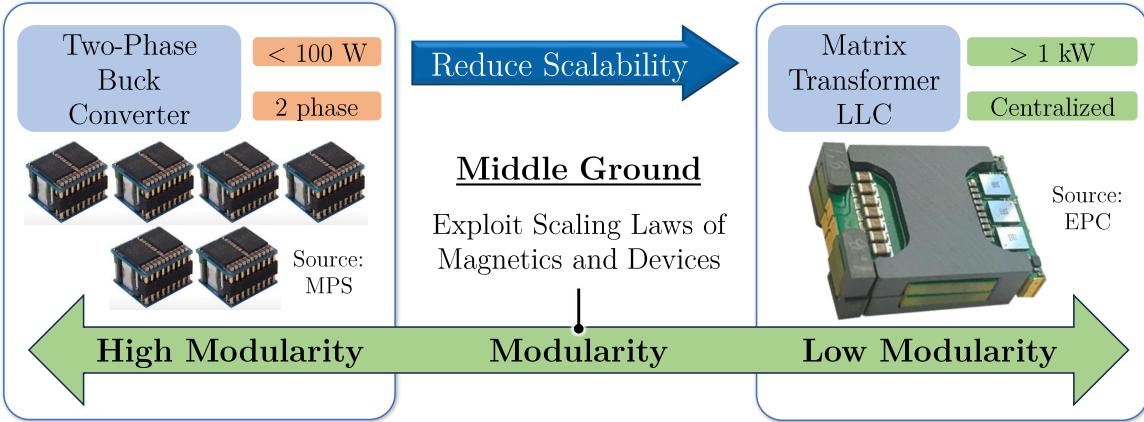


Figure 1.4: Scalability spectrum for power electronics converters. On one end, a converter such as the two-phase buck converter (MPS MPC22163-130 [12]) is designed to process low power and can easily be paralleled to scale to higher power levels. As scalability reduces, on the other end of the spectrum is a converter such as the matrix transformer LLC (EPC 9159 [13]) which handles over 1 kW of power. In the middle lies a point where the scaling laws of magnetics and devices can be exploited while maintaining flexibility to scale the converter for multi-core and chiplet architectures.

flexibility of a power architecture to modularly adjust to different power ratings and application requirements without necessitating a complete redesign. This property is beneficial in addressing the diverse and dynamic power needs of modern computing systems.

At one end of the scalability spectrum, power converters can be designed to be highly modular. The converters on this side of the spectrum process a relatively low amount of power across a few phases, employing a “one size fits all” approach. Such architectures, exemplified by the two-phase buck converter as depicted in Figure 1.4, allow for multiple identical modules to be paralleled, adapting to meet various power level demands. This high modularity ensures that designers can cater to low-power applications under 100 W with the same basic architecture used for more demanding applications.

Progressing toward lower modularity, power converters like the matrix transformer LLC adopt a centralized approach to power conversion, handling high power levels exceeding 1 kW in with a single converter. These converters are less modular but

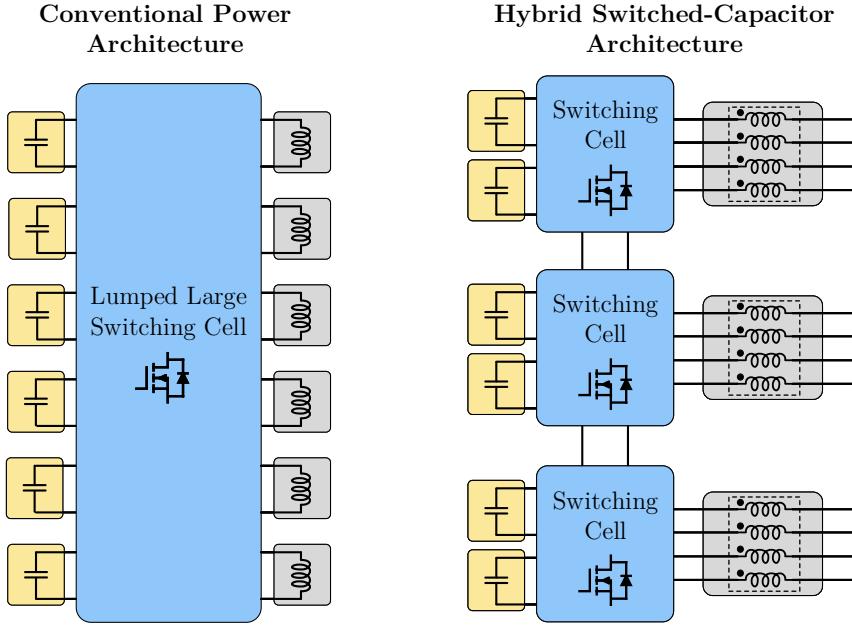


Figure 1.5: The hybrid switched-capacitor architecture developed in this dissertation compared against a conventional power converter architecture. This architecture utilizes power components appropriately to enable high density while supporting scalability.

are designed to efficiently manage large power quantities, making them suitable for high-power applications.

Between these two extremes lies a middle ground – a hybrid approach that seeks to balance scalability with the benefits derived from the scaling laws of magnetics and devices. This approach aims to merge magnetic components and reduce device blocking voltages to maintain scalability for chiplet applications while still allowing the power architecture to be tailored to specific performance criteria.

Scalability is an essential feature of contemporary power delivery architectures, allowing for versatility in design and application. As this thesis unfolds, it will further examine specific VPD architectures and magnetic designs, continuing to highlight the importance of scalable solutions in power electronics. The discussions to come will build upon this scalable framework, showcasing how it can be applied to create highly efficient and adaptable power delivery systems for future microprocessors.

Hybrid switched-capacitor circuits are a prime example. This architecture is able to use low voltage rating devices, merge the functionality of multiple magnetic components into one, while exploiting architectural features to easily extend to provide power for multiple different voltage rails as needed. Figure 1.5 shows the concept of the hybrid switched-capacitor architecture. This architecture moves power electronics in the direction of using each power component to its full potential. Capacitors are leveraged for their high energy density; blocking voltages across devices are decreased and multiple smaller switches are used to improve performance and speed; the functionality of multiple magnetic components are integrated into larger-scale magnetics. The architecture is modular, guaranteeing symmetrical voltage and current through each submodule. This thesis will develop the hybrid-switched capacitor architecture together with novel coupled magnetics for vertical power delivery to high-density power electronics.

## 1.2 Contributions and Thesis Organization

Designing power electronics for high-density loads to exploit component scaling laws while maintaining scalability requires innovations in the approach to converter design. By re-thinking how each component interacts with each other and how to best optimize and utilize a fixed volume to construct these components such that they serve as greater than the sum of their parts, power converters can be designed to push the front of efficiency, density, and speed. This thesis is split into three parts that explore a new vision for power converter design.

Chapter 2 introduces a new power delivery scheme for high-density loads. It discusses vertical power delivery (VPD), which expands the design of power converters from a 2D layout to a 3D volume. The contributions of this chapter are summarized as:

- A comprehensive overview and discussion on the benefits and challenges of VPD for board-level power converters with power levels of 100-1000 W.
- The introduction of a *vertically stacked heterogeneous packaging model for in-packaging vertical stacked power converters*, with broader applications to 3D stacked power management integrated circuits.
- The qualities required of a power architecture consisting of capacitors, switches, and magnetics that work with the packaging model to fully realize the benefits of VPD in the specific application of microprocessor power delivery.

Chapter 3 focuses on the power conversion architectures that are most suited for the vision presented in Chapter 2. Contributions of this chapter include:

- A systematic categorization of power converter architectures suitable for 48-V voltage regulator modules (VRMs) based on their power conversion stages, energy transfer mechanism, operation mechanism, and regulation capability.
- The formulation of a new hybrid switched-capacitor architecture called the *linear-extendable group-operated point-of-load (LEGO-PoL) architecture*. The operation mechanisms are analyzed. The architecture is modular, leveraging switched-capacitor and switched-inductor techniques and merging the operation of the two stages to achieve benefits in density, efficiency, and speed.
- The LEGO-PoL architecture splits the high input voltage stress and high output current stress with automatic voltage balancing and current sharing among submodules. The operation of this automatic balancing mechanism is analyzed in detail.
- A vertical stacked LEGO-PoL prototype is designed, built, and tested. It uses a 3D vertical stacking approach as per the model presented in Chapter 2. The

system height is 16.65 mm. It achieves a peak efficiency of 88.4% for 48-V-to-1-V conversion, and uses air cooling to deliver 450 A and immersion liquid cooling to deliver 780 A. The power density with air cooling is 294 W/in<sup>3</sup>.

- A second prototype, optimized to exploit the full potential of the LEGO-PoL architecture for high density and low height, is designed, built, and tested. The Mini-LEGO architecture leverages optimizations in all aspects of the original LEGO-PoL design to trade off performance in efficiency for benefits in density. It achieves a peak efficiency of 84.1% for 48-V-to-1-V conversion, and uses air cooling to deliver 240 A with a height of 8.4 mm. The power density is improved to 1390 W/in<sup>3</sup>.
- A detailed comparison between the vertical stacked LEGO-PoL prototypes and other lateral power delivery converters for the same target application of 48-V VRMs. The Mini-LEGO converter exhibits extremely high density and pushes the pareto front of efficiency and density to new territory.

Chapter 4 details a design methodology for vertical magnetic components suitable for VPD. Contributions of this chapter are:

- Introducing the benefits and ways to model parallel coupled magnetic structures. Models are classified and used to derive a compact set of equations that explain the benefits of parallel coupled magnetics in extending the ripple reduction benefits achieved by interleaving power converters into the individual phases themselves.
- A systematic optimization routine using the developed equations and models that link the physical geometry of a structure to the electrical performance of the magnetic component. This optimization routine determines how to allocate the available 3D volume towards ferrite material, air, or copper to minimize losses and satisfy designer-specified constraints.

- A characterization methodology for vertical coupled inductors is proposed and detailed. This method can be used to accurately measure the inductance parameters of a fabricated vertical coupled inductor, taking into account the leakage inductance contributed by the remainder of the vertical stacked system.
- The design and fabrication of a 1 MHz four-phase vertical coupled inductor for the initial vertical stacked LEGO-PoL prototype. This inductor has a footprint of 12 mm × 13 mm, a height of 5.25 mm, and is capable of delivering 65 A per phase with a winding resistance of 0.09 mΩ.
- The design and fabrication of a 1.5 MHz four-phase vertical coupled inductor, re-designed for Mini-LEGO and optimized for thinner height. This inductor has an area of 9 mm × 9 mm with a height of 2.5 mm. It delivers 20 A per phase, with a coupling factor that results in the inductor having a transient performance similar to a 10 nH inductor while having a steady-state ripple performance similar to a 65 nH inductor. It has a resistance of 0.18 mΩ.
- A fully re-designed vertical magnetic structure called the *pinwheel coupled inductor* designed for frequencies of 2 MHz and beyond. This structure realizes the power-via-magnetics concept introduced in Chapter 2, with current-carrying conductors that are realized as vertical interconnects. The magnetic core is designed to wrap around these conductors to guide the magnetic flux to achieve parallel coupling. A pinwheel inductor is fabricated with dimensions of 8 mm × 8 mm × 1.8 mm and tested with a four-phase buck converter. The inductor delivers 25 A per phase with a resistance of 0.09 mΩ and is benchmarked against other multiphase coupled inductor solutions for VRMs.

Chapter 5 concludes this thesis and summarizes the progress made towards the vision outlayed for vertical power delivery. Future topics of work required to fully realize this vision are discussed. The proposed hybrid switched-capacitor and mag-

## *1. Introduction*

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netics design architecture opens up opportunities for future power converters that are highly compact and scalable for a variety of different applications requiring a large amount of power to be delivered in a small area.

# Chapter 2

## Design Considerations for Vertical Power Delivery

### 2.1 Background

The requirements of high-density loads such as microprocessor systems continually require higher power to be delivered with increasing spacial constraints. Traditional power delivery methods distribute components across the surface of printed circuit boards (PCBs) and deliver high power laterally across the PCB to the load. An example of this is shown in Figure 2.1. The microprocessor, in this case a graphics processing unit (GPU), is placed on a printed circuit board that handles the power delivery. The GPU is placed in the center of the board, and power delivery components – semiconductor devices, capacitors, and magnetics – surround the GPU and deliver the required high currents and low voltages. Although effective at previous power levels, lateral power delivery is becoming less suitable as power levels increase due to the extensive physical space it requires and inefficiencies resulting from the power delivery network (PDN).

Vertical power delivery (VPD) is emerging as a paradigm shift to overcome these challenges. VPD stacks power delivery components vertically, delivering power in a

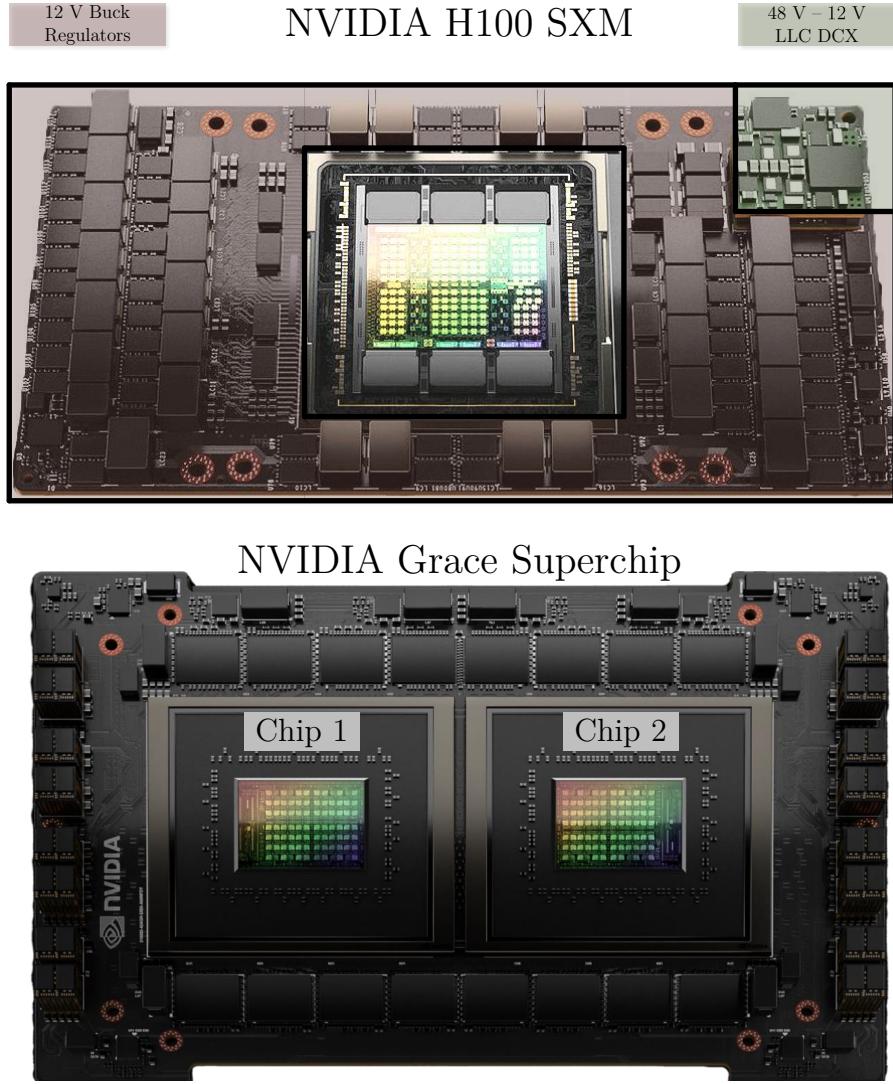


Figure 2.1: Picture of an NVIDIA H100 SXM board (top), housing a 4 nm Hopper GPU and 80 GB of memory [14]. Surrounding the GPU are power delivery components that deliver power laterally to the GPU. The 48 V input voltage is stepped down by the converter highlighted in green, which converts 48 V to an unregulated 12 V bus. The buck regulators highlighted in red each step down 12 V to a regulated voltage required by the GPU. Each delivers a fraction of the required output current to the GPU. The NVIDIA Grace Superchip (bottom) places two chips on the same board, with high speed communication between the two chips [15].

different plane than the board housing the microprocessor. This approach can offer many benefits for power delivery, such as reduced PDN resistance by minimizing the length of the power interconnects, increasing the power density, improving signal integrity, and enabling greater modularity and scalability. The shift towards VPD is

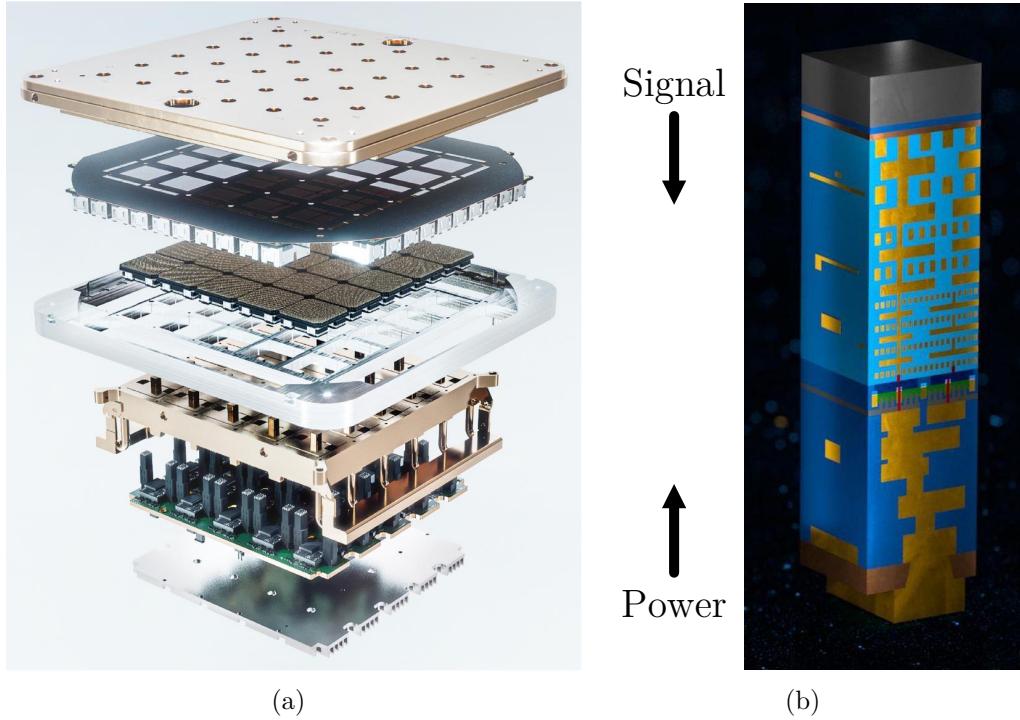


Figure 2.2: (a) Tesla Dojo [16], an example of packaging level vertical power delivery, where power is vertically delivered to a supercomputing platform. (b) Intel PowerVia [17], an example of a 3D power integrated circuit (IC) using backside power delivery, which delivers power to transistors on the backside, separating the PDN from the signal routing.

apparent not only on the PCB level, but in the system packaging level and the chip level. Figure 2.2 highlights Tesla Dojo [16], a new supercomputing platform that uses vertical packaging with innovative thermal solutions for a highly dense solution, as well as Intel PowerVia [17], a new backside power delivery architecture for future chip architectures.

Despite its advantages, VPD introduces new challenges to power electronics design, particularly in system integration and thermal management. Vertically stacking power components into a compact volume as opposed to on a planar area and increasing the power density exacerbates the thermal management challenge as the reduced space limits air flow and paths for heat dissipation. New cooling technologies such as

liquid cooling and heat pipes, along with architectures that enable balanced thermal dissipation, are essential for vertically integrated systems.

These challenges demonstrate the need for new architectures and packaging methods for VPD. To address these challenges, this chapter introduces the vision of a new vertically stacked heterogeneous (VSH) packaging model for VPD. This model organizes power delivery into multiple distinct layers, each comprised of the major power delivery components – semiconductor devices, capacitors, or magnetics. Each layer is designed optimally for its function. This configuration maximizes volume utilization to improve power density and facilitate compact integration. By symmetrically distributing the high voltage input stress and high current output stress evenly throughout the package, thermal management is simplified. Architectures and magnetics that guarantee these symmetrical properties are further developed in the remainder of this dissertation.

## 2.2 Motivation for Vertical Power Delivery

The push towards VPD specifically in the field of microprocessor power delivery is motivated by a need to manage the growing power requirements within an increasingly constrained area and volume. High power applications, such as data centers which comprise of multiple server racks, as well as dense 3D power integrated circuits (ICs), have been integrating more power-intensive functionalities into smaller and smaller form factors. The more power per server rack, or the more power per IC, the more computing workload that can be accommodated in less space.

One of the major advantages of VPD is its ability to support higher power density loads. By opening the  $z$ -dimension for power converter design, area densities of power converters can greatly increase, from the order of  $0.01 - 0.1 \text{ A/mm}^2$  to upwards of  $1 \text{ A/mm}^2$  [40]. Figure 2.3 plots the area densities of a survey of voltage regulator modules (VRMs) that are designed for microprocessor power delivery. The plot shows

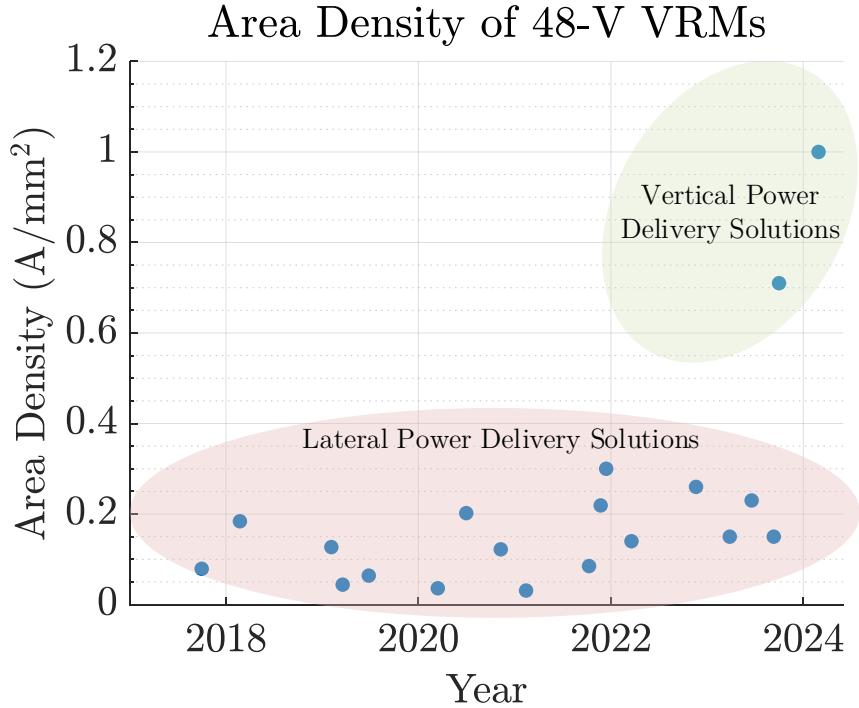


Figure 2.3: Survey of the area density of voltage regulator modules (VRMs) with 48 V input [18–39]. Emerging VPD solutions greatly improve upon the area density of traditional lateral power delivery approaches.

that vertically packaged VRMs are able to achieve area densities that are a factor of ten greater than their counterparts that employ lateral power delivery.

For PCB-level power conversion, heavy current is distributed laterally through the multi-level packaging PDN through the package to the point-of-load (PoL) converters on the die. These long, high current PDN traces suffer from high  $I^2R$  loss and can induce electromagnetic interference (EMI) which impacts overall system performance. Significant power savings can be attained by shortening the long lateral distance between the output of the power converter and on-chip PoLs. Figure 2.4 demonstrates how in-packaging VPD, whereby the VRM is now co-packaged underneath the microprocessor, can greatly reduce the interconnect resistance. By placing the VRM directly underneath the motherboard, shorter vertical interconnects deliver the high output current to the microprocessor while freeing up motherboard area. Typical PDNs, with resistances on the order of  $500 \mu\Omega$  (which would result in 500 W

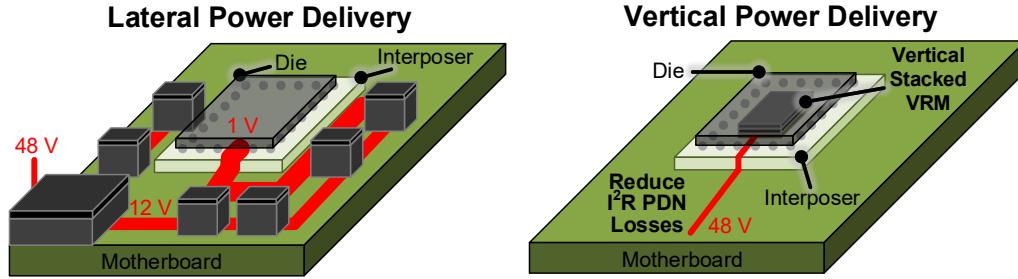


Figure 2.4: Lateral power delivery vs. vertical power delivery architectures. In-packing vertical power delivery enables high current area density while reducing the high current and high resistance PDN traces improving overall system efficiency.

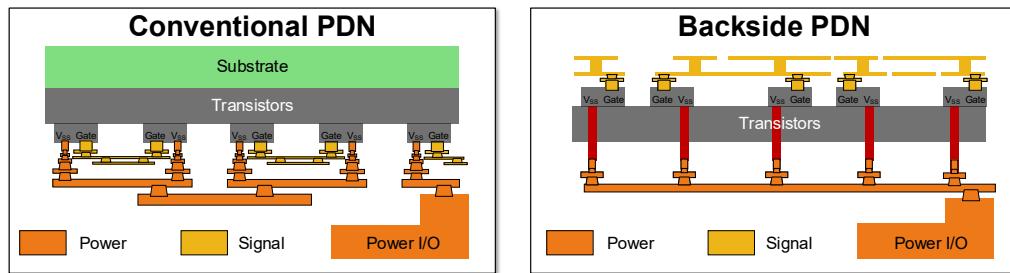


Figure 2.5: Backside power delivery for ICs. Power and signal are separated, and power is routed vertically to the transistors with advanced interconnects such as nTSVs. Together with in-packaging VPD for VRMs, a vertical power delivery architecture can reduce the overall PDN resistance by over 100 times that of conventional lateral power delivery.

of loss at 1000 A) can be reduced by a factor of 100 to  $5 \mu\Omega$ , decreasing the  $I^2R$  losses by a factor of 100 – or facilitating a hundred-fold increase in the power delivery capability for the same PDN loss [41].

In-packaging VPD, coupled with improving the interconnect density from the VRM to the microprocessor, can greatly reduce the PDN resistance. Advanced vertical interconnect technologies, such as  $\mu$ -bumps, nTSVs, and Cu-Cu direct bonding, have recently been demonstrated as a promising alternative to the traditional solder-based ball grid arrays (BGAs) and flip-chip bumps [42, 43]. Both in-packaging VPD and backside power delivery, as shown in Figure 2.5, reduce the overall PDN both from the VRM to the die as well as on the die level to the transistors, and together represent the ultimate vision of high density power delivery.

Backside power delivery and freeing up motherboard area enhances the overall signal integrity as well. VPD reduces the potential for signal degradation that can occur over long transmission routes. The close proximity of the power conductors to the microprocessor reduces the parasitic inductances and capacitances between the VRM and the processor. These parasitics can create resonances and introduce ringing in the presence of highly dynamic loads with high  $\frac{di}{dt}$  transients. The reduction in PDN resistance and parasitics enables slew rates upwards of  $> 5 \text{ A/ns}$  and a reduction of bypass capacitance due to the reduction in  $IR$  drop [44]. By freeing up top-side motherboard area, opportunities arise to include more high-speed signal routing from the processor to other elements such as co-packaged optics or communication links.

By leveraging strategic placement of components within an in-package VRM, noise-generating components can be shielded within the package from the external system. VPD inherently minimizes the areas exposed to electromagnetic interference (EMI) generated by the voltage regulator. In lateral power delivery systems, high frequency radiated EMI is caused by common-mode currents that flow on the input and output paths [45]. Switching semiconductor devices also radiate EMI. In-packaging VPD reduces the length of the common-mode current paths, lessening the radiation from these noise propagation paths. The design of VPD systems allows for better control of the EMI paths. By strategically positioning high-frequency switching devices within the VPD stack, shielding solutions can be included that encompass multiple layers and help to reduce EMI from these noise sources.

In summary, the benefits of VPD for high density loads are as follows:

1. Improving the power density of high-density load systems.
2. Reducing the PDN resistance and losses, greatly improving the overall system efficiency and improving the power handling capability.

3. Enhancing signal integrity and improving processor-to-processor communication.
4. Mitigating electromagnetic interference from high common-mode current paths.

While VPD has the potential to provide performance-enhancing and space-efficient benefits, the next section will discuss practical challenges that are associated with VPD, such as system integration difficulties and thermal management requirements that arise with high density power delivery converters.

## **2.3 Challenges of Vertical Power Delivery**

While VPD brings many advantages such as higher power densities, lower PDN impedance, and better utilization of resources for signal and power paths, challenges arise that need to be properly mitigated for these benefits to be realized.

### **2.3.1 Thermal Management**

One of the major complexities introduced as power converters transition from 2D planar configurations to high-density 3D cube-like systems is thermal management. While high density layouts maximize space utilization, heat generation is now concentrated within a significantly smaller volume. As mentioned in the previous section, vertical power delivery leads to lower overall system loss due to reduced  $I^2R$  conduction losses in the PDN. Overall, the entire system will exhibit less heat generation than a comparable lateral power delivery solution with planar configured power converters [39]. However, the concentration of heat generation in higher density hot spots necessitates unique cooling solutions as the densities approach around 2-3 A/mm<sup>2</sup> [46, 47].

A simple comparative example can be used to demonstrate the thermal management challenge. For a microprocessor load, assume two power delivery solutions:

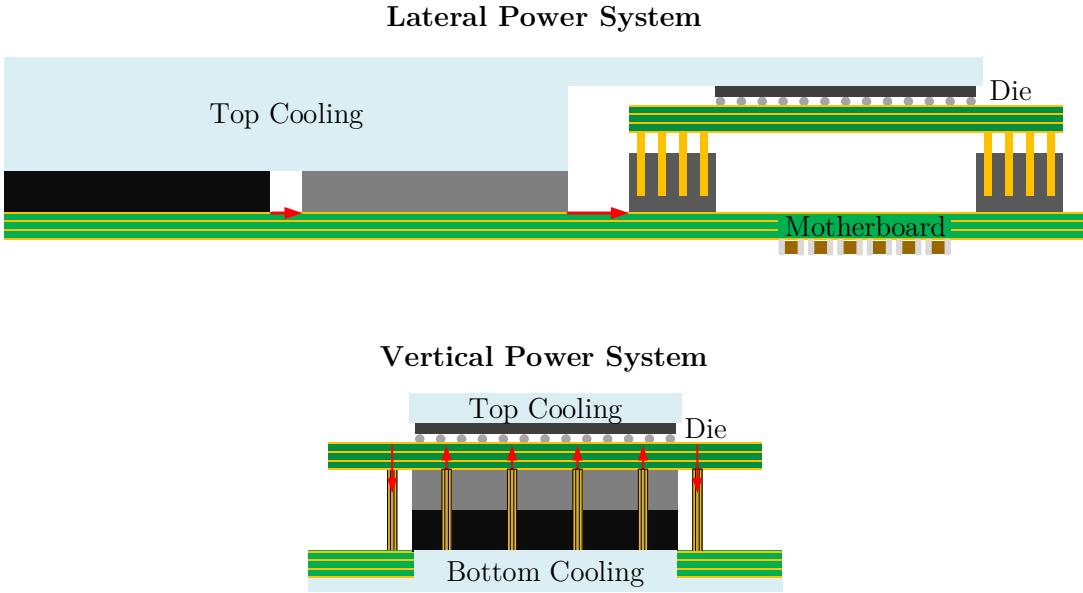


Figure 2.6: Comparison of cooling mechanisms of a lateral power delivery solution and a vertical power delivery solution. The lateral solution has more surface area exposed to make contact with the heat sink compared to the vertical solution. The vertical system will have higher internal temperatures that must be managed.

- Vertical power delivery configuration: two constituent layers are stacked, each with an area of  $A$  and a height of  $h$ . The entire system has a height of  $2h$  and an area of  $A$ .
- Lateral power delivery configuration: this system is comprised of the same layers as the VPD system, but arranged in a planar configuration such that the overall area is  $2A$  and the height is  $h$ .

Figure 2.6 illustrates these two solutions. The most common thermal solution for removing heat is to use top side and bottom side heat sinks. In the vertical system depicted, the heat generated is confined to a smaller volume with less surface area per unit power to dissipate the heat as compared to the lateral system. The lateral system, with its larger surface area three times that of the VPD system, inherently has more effective heat dissipation as more of the heat-generating components make contact with the heat sinks. Despite having similar cooling infrastructure, the vertical

system will have higher internal temperatures as the heat sinks cannot manage the denser heat flux as effectively.

However, careful thermal design of the vertical power stack can ultimately result in reduced thermal stress on the interconnects between the microprocessor and the PCB. In VPD, the top side cooling is primarily for the microprocessor, while the bottom side cooling is the main way of removing the heat from the power converter. This dual-sided approach optimizes the thermal management of the power circuitry and the microprocessor load. One technique to conduct heat from the middle of the vertical stack, farthest away from the heat sink, towards the heat sink is to introduce heat pipes. Heat pipes can rapidly transfer heat from warmer middle layers of the stack to the cooler outer edges [48]. Heat pipes contain fluid that vaporizes when it absorbs heat. The vapor travels through the pipe to the cold interface where it condenses back to a liquid and releases the heat. The thermal conductivity of heat pipes is one to two orders of magnitude higher than copper, allowing them to remove large amounts of heat with small form factors. A combination of well designed copper conduction paths between vertical stacked layers and heat pipes can help to deliver heat to the cooler outer edges and increase the temperature uniformity of the stack.

For high heat flux scenarios where the cooling capacity of heat pipes is exceeded, microchannel liquid cooling systems can further increase the heat dissipation. Instead of using phase-change liquids, microchannel cooling circulates a liquid coolant through designed channels either within or adjacent to heat-generating components. Microchannels require careful co-design with the power converter to be integrated within the entire vertical stack. This technique is increasing in prevalence in the design of 3D ICs and is directly applicable to board-level VPD as well. Figure 2.7 shows how the implementation of both heat pipe cooling and microchannel cooling can be implemented in vertical stacked converters for in-packaging VPD [47]. Thermal interface materials, such as gap fillers or thermal putty, can offer another way

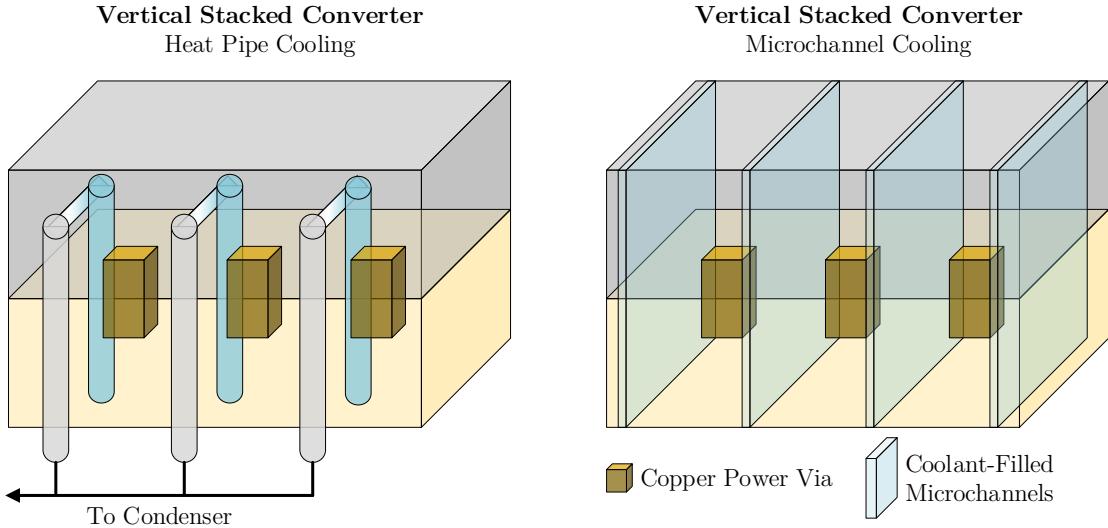


Figure 2.7: Demonstration of heat pipe cooling and microchannel cooling for vertical stacked converters. Power vias carry current between the stacked power layers, and advanced cooling solutions are used to extract heat from the inside of the stack towards the cooler outer edge.

to fill in any air gaps between the vertically stacked layers to help conduct heat from the inside to the outside.

### 2.3.2 Signal Integrity

While signal integrity was mentioned as an advantage in Section 2.2, since the long common-mode current traces on the motherboard are eliminated, vertical power delivery introduces signal integrity and EMI concerns within the dense converter package itself. These concerns are further accentuated with the push towards higher switching frequencies in vertical stacked converters to enable a reduction of passive component size so that the converter can fit the limited 3D volume available for in-packaging VPD. The high density of components in VPD systems makes it more difficult to isolate noise-generating elements from high-frequency signal paths.

Architecture and magnetics design is integral to ensuring low EMI and high signal integrity in vertical stacked converters. On the architecture side, high frequency current loops should be identified and techniques such as reducing the loop area,

embedding high frequency components within the PCB, and differential signal routing to cancel fields should be employed. Architectures that can switch at high frequency with full soft-switching, which reduces high frequency switching noise, or architectures that can switch the high blocking voltage devices at low frequencies, are advantageous for vertical power delivery. Chapter 3 presents the architectural innovations of this dissertation that enable in-packaging VPD.

Magnetic structures should be designed with well-contained flux paths and reduced magnetic flux. Certain magnetic structures, such as solenoid inductors, radiate significant magnetic flux to the air around the component. In addition, air-core magnetics, lacking magnetic cores with higher permeability than air, have flux paths that occupy significant volume beyond the magnetic windings. Designing a magnetic structure that contains magnetic flux within the magnetic core can reduce radiated noise. In addition, magnetic coupling techniques can be leveraged to fundamentally reduce the energy storage within the magnetic field for the same amount of power transferred when compared with magnetic structures without coupling. This energy storage reduction leads to mutual advantages in size reduction, improved dynamic performance, and reduced levels of magnetic flux. Chapter 4 analyzes in details the benefits of magnetic coupling and develops a design methodology for magnetic components suitable for in-packaging VPD converters.

In advance of developing the specific innovations in architectures and magnetics, the following section introduces a generalized packaging vision for in-packaging vertical stacked power converters.

## **2.4 Packaging Vision for Vertical Power Delivery**

This section introduces a structured vertically stacked heterogeneous (VSH) architecture and vision for in-packaging VPD converters that optimizes the role of each constituent component in the stack.

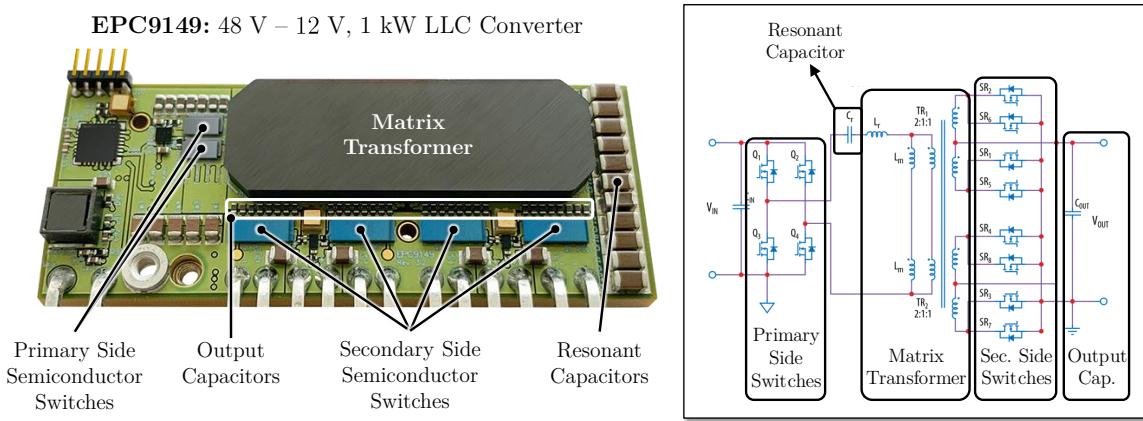


Figure 2.8: Picture and schematic of a 48-V-to-12-V 1 kW LLC converter from EPC [49]. The EPC9149 converter uses lateral power delivery, distributing and scattering the power components on the PCB with high impedance power flow paths.

Figure 2.8 shows an annotated picture of the EPC9149 48-V-to-12-V 1 kW LLC power converter [49]. This converter is designed to function as the first stage of a full 48-V-to-1-V system, processing the entire power meant for the microprocessor load and outputting an intermediate 12 V bus voltage that is then sent to a regulated converter for further voltage step down. This architecture is used as a demonstration of a typical lateral power delivery converter. The main constituent parts: the primary side switches, the matrix transformer, the resonant capacitor, the secondary side switches, and the output capacitors, are distributed along the board and non-optimal, high impedance power flow paths connect the scattered elements together. The converter is customized with a matrix transformer for the specific application, hindering the scalability.

Figure 2.9 shows the block diagram of a scalable and modular architecture suitable for in-packaging vertical stacked converters. The system is comprised of  $N$  submodules, each processing a fraction of the input voltage  $V_{in}/N$  and delivering a fraction of the output current  $I_{out}/N$ . This system is scalable, and can be extended and sized based on the input voltage and output current specifications. With each submodule processing an equal amount of power, this results in a uniform heat distribution

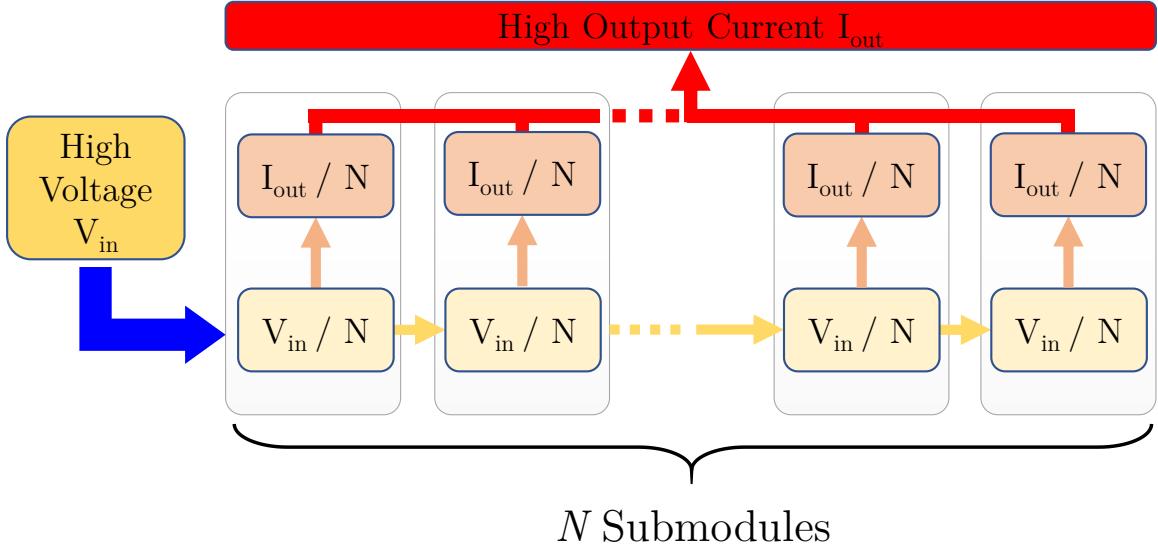


Figure 2.9: Block diagram of a VPD-suitable architecture. The architecture is composed of multiple submodules. The submodules are arranged to split the high input voltage stress and high output current stress uniformly throughout the converter, balancing the thermal stress evenly throughout the converter package.

throughout the system. Such an architecture is advantageous for VPD where thermal management is a challenge. By splitting the high voltage uniformly, each switch can be sized smaller, better utilizing the available device area with lower on-resistance devices.

To implement vertical power delivery using this modular approach, a structured VSH packaging model is developed. Figure 2.10 introduces this model, with three layers as an example. It splits up the three major power components – capacitors, switches, and magnetics – each into their own layer. Each layer is vertically stacked on top of each other, with capacitors at the bottom to utilize their higher energy density to interface with the input voltage and magnetics on the top to act as a current source and deliver the high output current in the load. The function of each layer is explained in detail:

- 1. Bottom Layer – Capacitors:** Positioned at the bottom of the vertical stack, capacitors are essential in splitting up the input voltage into multiple smaller

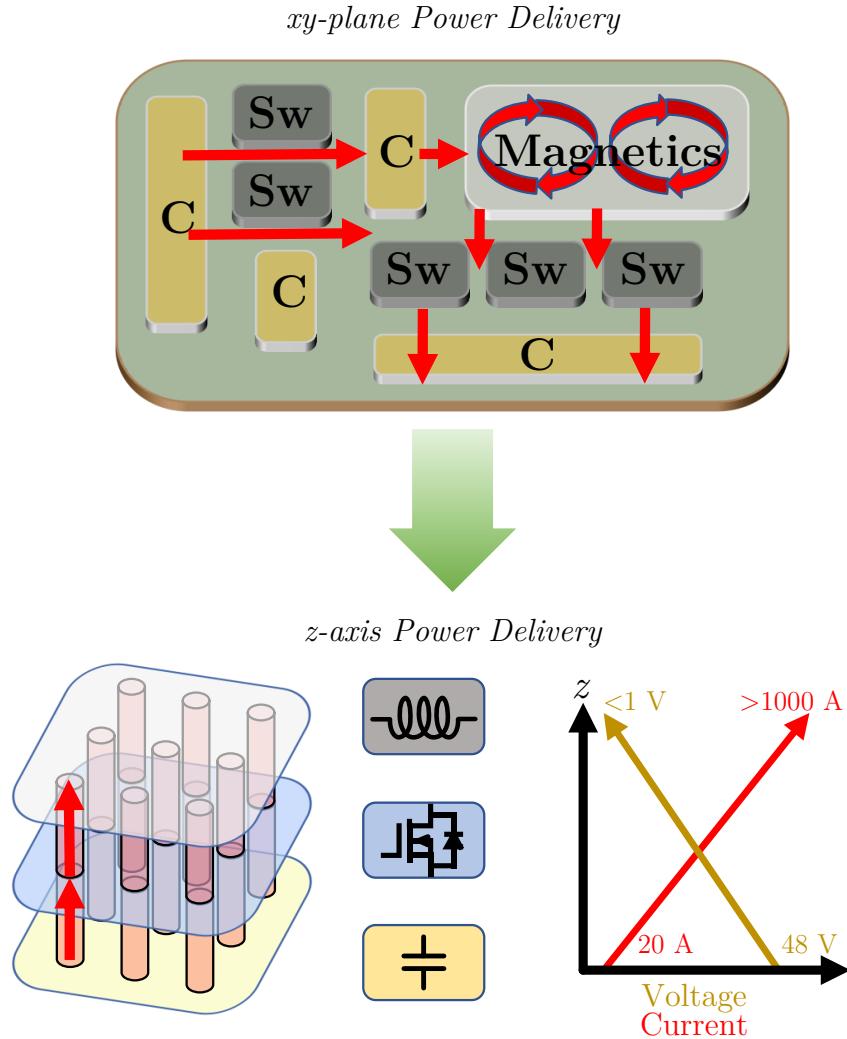


Figure 2.10: Block diagram depiction of the lateral power delivery converter of Figure 2.8 (top). The three-layer packaging model (bottom) presents a vertical stacked power converter architecture with capacitors on the bottom, switches in the middle, and magnetics at the top. Each layer is connected by distributed and symmetric vertical interconnects.

domains. As explained in Chapter 1, capacitors have a high energy density and are indifferent in regards to size when it comes to their energy storage. Capacitors are distributed and connected to switching cells that turn on and off such that energy is shuffled between the power source and the capacitors to maintain relatively stable dc voltages across each capacitor. Multiple ceramic

capacitors can be placed in parallel in this layer with low height, resulting in low equivalent series resistance and equivalent series inductance.

2. **Middle Layer – Switches:** Switches, implemented as power semiconductor devices such as silicon or gallium nitride MOSFETs, comprise the middle layer. These switches interface with the capacitors on the bottom layer, creating a switching network in such a way that certain capacitors charge up during one switching phase and release energy in another switching phase. The switches also must interface with the magnetic layer, providing a pulsed power source as input that the magnetic layer works to filter in order to extract the average value of the pulse, thereby stepping down the voltage in an ideally lossless manner. As switches are the main heat source, ensuring that each switch sees balanced voltage and current stress is essential to distributing the thermal stress evenly across this layer. Cooling solutions must be employed to bring the heat away from the middle and out towards the bottom and top of the vertical stack.
3. **Top Layer – Magnetics:** The top layer of the vertical stacked converter contains the magnetics. This component functions as a current source in the converter. It delivers the large output current to the microprocessor, and is positioned the closest to the load as a result. It can slew the current up or down in response to a fast dynamic load transient. The current through the inductor can also be used throughout the circuit as a way to shuffle energy between capacitors in a more efficient manner. The magnetic layer plays an essential role in filtering the output power to provide a clean output voltage with low ripple and noise to the microprocessor. This layer must be carefully optimized to fully utilize the limited 3D volume available to provide large amounts of power while minimizing losses – and as a result, minimizing heat generation.

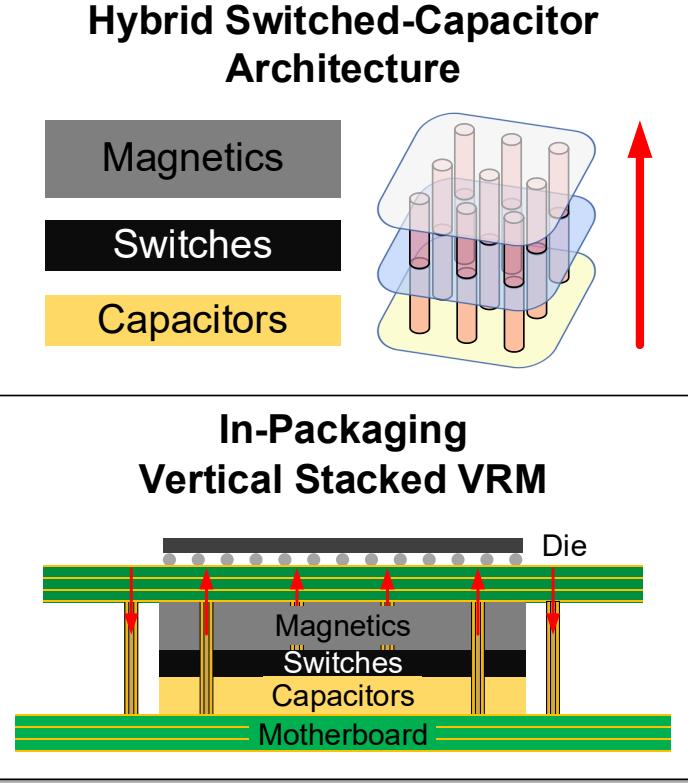


Figure 2.11: Three-layer packaging of a vertical stacked hybrid-switched capacitor converter. The converter is split into its constituent parts of capacitors, switches, and magnetics. Vertical power interconnects deliver power between the layers to the microprocessor.

Each submodule of the VPD architecture presented in Figure 2.9 consists of a vertical stack of these three layers. Each vertical stack contains vertical power interconnects, that connect the capacitor layer, switches, and magnetics layer together. The magnetics layer vertical power interconnects together with a magnetic core to connect to the board housing the microprocessor. By combining these smaller 3D vertical stacks with short lateral interconnects between them, a configurable and modular vertical stacked converter can be developed that is suitable for a given target application.

Figure 2.11 highlights an example of an in-packaging vertical stacked VRM that adheres to this design vision. A hybrid-switched capacitor architecture, which utilizes both capacitors and magnetics along with a switching network to step down voltage,

is split into its constituent components and arranged along the three-layer packaging model. Vertical power-via interconnects are distributed evenly along the vertical stack in the  $x$  and  $y$  plane to deliver power in the  $z$  axis to the microprocessor.

The VSH packaging model, combined with the proper circuit topology and optimized vertical magnetics, is designed to leverage the inherent benefits of VPD in a high density 3D form factor with low interconnect resistance while mitigating challenges that arise such as thermal management. Each layer, as well as the interconnection between the layers, is designed to reduce system parasitics and large high-frequency loops to mitigate EMI concerns. The following sections of this dissertation explore specific circuits and magnetic designs that fit well into the vision presented here for in-packaging vertical stacked power converters.

## 2.5 Summary

This chapter introduces and explains the role of VPD in high-density microprocessor systems. The traditional lateral power delivery architecture is examined. Lateral power delivery occupies a large amount of area on the motherboards and uses lengthy high-impedance interconnects to deliver power to the microprocessor. The low density and high loss associated with lateral power delivery pose problems to future microprocessor systems where the current consumption only continues to grow.

Motivated by improving the overall system efficiency, density, and speed, VPD offers many advantages to remedy the problems of traditional lateral power delivery solutions. VPD can improve on the area density of lateral solutions by utilizing 3D stacking, freeing up area on the motherboard for improved signal integrity and chip-to-chip communication. It greatly reduces the interconnect lengths from the voltage regulator to the processor, significantly improving the end-to-end system efficiency and reducing PDN losses.

In order to leverage the advantages of VPD, challenges that arise as a result of vertical stacking need to be mitigated. The main challenges that arise are thermal management and signal integrity within the vertical stack. As the density of a VPD solution increases, and less surface area is exposed to the ambient air for heat extraction, innovative thermal solutions such as microchannels or heat pipes are increasingly required to cool the system. Thermal co-design is needed to ensure that the performance and reliability of VPD converters matches that of their lateral counterparts. While VPD removes the high common-mode current traces on the motherboard, helping overall signal integrity, vertical stacking introduces the risk of larger high-frequency loops and places noise-generating semiconductor devices closer to other components. Architectures for VPD must be designed to mitigate these EMI effects.

A generalized VSH packaging model is introduced for a modular and extendable in-packaging vertical stacked power converters to exploit the advantages of VPD for microprocessor systems. An example three-layer package is introduced, composed of capacitors at the bottom, switches in the middle, and magnetics on top. Each separate layer is designed to optimize its functionality and interaction with other layers. The capacitor layer at the bottom interfaces with the high voltage and splits it into smaller voltage domains with high efficiency and density; the switch layer in the middle manages the power flow and includes integrated cooling technologies to handle heat effectively; and the magnetics layer at the top provides the current source needed throughout the package to distribute energy between capacitors and the load.

This chapter lays out the vision for power converters suitable for VPD. The subsequent chapters detail the specific architectures and magnetics that can best fit this presented vision, and summarize the work that has been done thus far in implementing and realizing in-packaging vertical stacked power converters with VPD for high-density loads.

## Related Publications

1. Y. Elasser and M. Chen, “Power-Via-Magnetics with Pinwheel Coupled Inductors for Ultra-Thin Vertical Power Delivery,” *IEEE Transactions on Power Electronics*, 2024, under review. [50]

# Chapter 3

## Linear Extendable Group Operated Architecture for Vertical Power Delivery

### 3.1 Background and Motivation

As the energy consumption of microprocessors continues to grow, increased attention has been placed on designing efficient and dense voltage regulator modules (VRMs) to provide power to these loads. The microprocessor industry has been driven by Moore's Law, which is an empirical observation that the transistor count on individual chips tends to roughly double within a two year span while the power density of these chips remains the same. However, the scaling laws that enabled Moore's Law, known as Dennard scaling [51], broke down around 2005 and resulting performance improvements achieved by frequency increases have tapered off, as observed in Figure 3.1a. Efforts have instead shifted to multi-core processors as the main mechanism of increasing chip transistor count, which has resulted in increased power consumption and chip die areas (highlighted in Figure 3.1b).

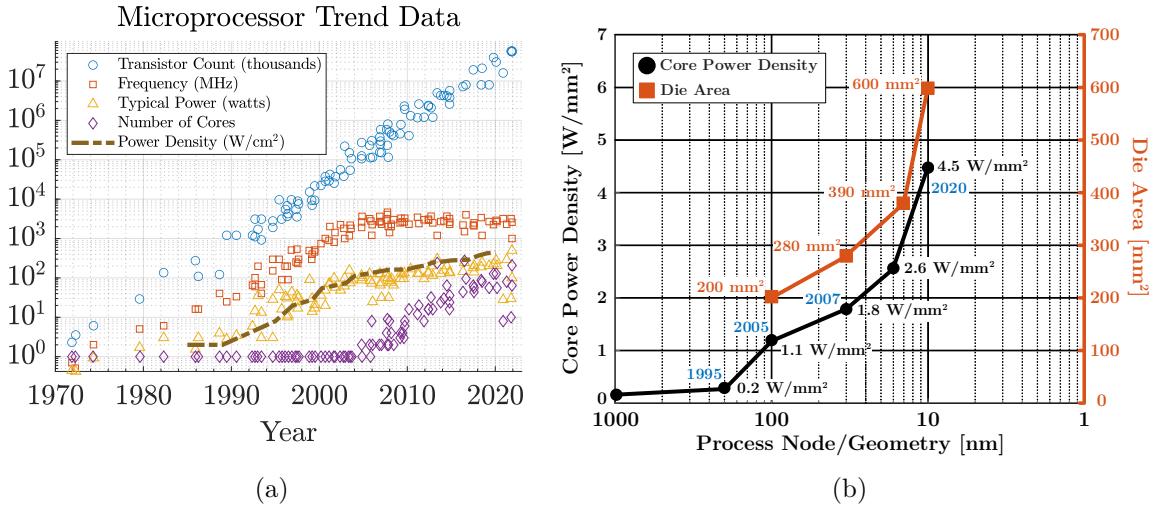


Figure 3.1: (a) Microprocessor trend data over the past 50 years (reproduced with data from [52]). (b) The breakdown of Dennard scaling (reproduced with data from [53, 54]). Microprocessors consume higher power per square millimeter in an increasingly larger die area, requiring very efficient and miniaturized power delivery from high voltage.

As the operating voltages of microprocessors has continued to decrease in tandem with these trends, the increasing power consumption has placed stringent requirements on VRMs to deliver these lower voltages ( $\leq 1$  V) and higher currents ( $\geq 100$  A) from a higher input voltage supply (40 V – 60 V) [1, 55, 56]. Delivering power from a nominal 48 V supply, instead of the traditional 12 V power delivery architecture, increases the power delivery capacity and reduces the power distribution losses by reducing the current delivered to the server rack [57]. A VRM on the motherboard is then tasked with stepping down 48 V to a well-regulated low voltage required at the point-of-load (PoL) while delivering high output current. The VRM must also be able to dynamically respond to any changes in power demanded from the microprocessor while still keeping the output voltage at the required level.

Various architectures for 48-V VRMs have been proposed. Each architecture has different trade-offs with regards to the key metrics of size, efficiency, and speed. Improving the density of VRMs can enable opportunities to co-package the VRM within the processor package and leverage vertical power delivery to greatly reduce

the interconnect length between the VRM and processor, improving overall system efficiency. This frees up motherboard area for chip-to-chip interconnects improving overall signal integrity, which makes co-packaging an extremely attractive solution for future microprocessor systems. By improving efficiency, less thermal resources are required for cooling the system.

In order to evaluate proposed architectures along these metrics, this chapter presents a categorization method to organize VRMs and better understand their trade-offs. These architectures can be organized by their number of power conversion stages, the mechanism by which they transfer energy from input to output, their operation waveforms, and how they perform regulation. While single-stage architectures offer low component count and smaller size, they suffer from limited control bandwidth and often use bulky magnetic components to achieve a high voltage conversion ratio [24, 58, 59]. Multi-stage architectures, using a fixed voltage conversion ratio switched-capacitor (SC) circuit as a dc transformer (DCX) and a magnetics-based regulation stage to interface with the microprocessor, can mitigate these trade-offs.

This chapter introduces and develops a new multi-stage VRM architecture called the linear-extendable group-operated point-of-load (LEGO-PoL) architecture, as shown in Figure 3.2. The LEGO-PoL architecture decouples the voltage stress, current stress, and dynamic requirements and addresses each of these design challenges separately with switched-capacitor and coupled inductor techniques. The input voltage is stepped down to a virtual intermediate bus voltage by a set of series-stacked SC units. Each submodule has its own virtual intermediate bus voltage [33]. This virtual intermediate bus voltage is a dc voltage, but may have significant ripple depending on the effective capacitance of the flying capacitors, the operating power, and the switching frequency. This virtual intermediate bus voltage serves as the input voltage the current-source switched-inductor stage. Multiple switched-inductor units are connected in parallel at the output to deliver high output current.

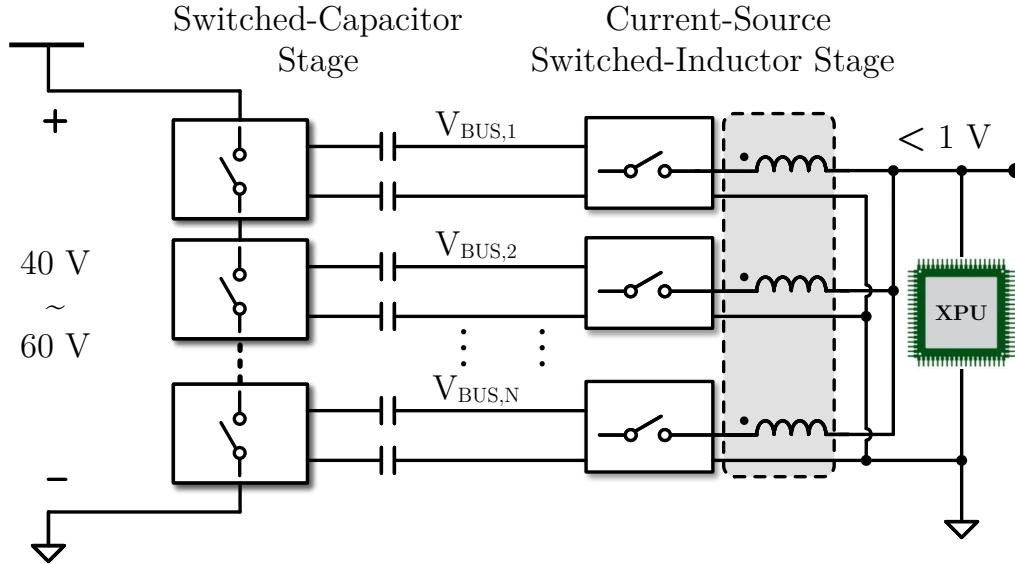


Figure 3.2: Overview of the Linear-Extendable Group-Operated Point-of-Load (LEGO-PoL) architecture. Series-stacked switched-capacitor units step down the high input voltage into multiple lower intermediate bus voltages, which serve as the input to a switched-inductor stage to perform voltage regulation. The switched-inductor units are configured in parallel to deliver high output current to the processor.

The operation of the SC stage and switched-inductor stage are merged. Instead of a large decoupling capacitor between the two stages, as commonly exists in intermediate-bus two-stage architectures, a small capacitance is used instead to filter the high-frequency ripple generated by the second stage. This allows the inductors in the multiphase buck stage to act as a current source, charging and discharging the flying capacitors to achieve soft charging. This soft charging mechanism enables usage of much lower flying capacitor values while maintaining high efficiency [60]. The switched-inductor stage can operate at a higher switching frequency than the SC stage to achieve faster dynamic performance at the processor interface.

The LEGO-PoL architecture is well suited to perform in-packaging vertical power delivery. The capacitors in the first stage interface with the high voltage input, while switches in the middle route energy between the capacitors acting as voltage sources and the inductors acting as current sources to the processor. This capacitor-switches-magnetics configuration is leveraged to design and build a vertical stacked LEGO-PoL

prototype. This prototype is designed to deliver 450 A of output current with forced air cooling (and is rated to 780 A with liquid cooling), and has a power stage area of 767 mm<sup>2</sup> and a height of 16.65 mm. The peak efficiency, including the gate driving loss, is 88.4% and the full load efficiency is 84.1%. This preliminary prototype verifies the suitability of the LEGO-PoL architecture for vertical packaging, however, is too tall to effectively co-package with the processor. The overall system density is further hampered when including the gate drive circuitry into the overall system area, which nearly doubles the area from 767 mm<sup>2</sup> to 1510 mm<sup>2</sup> and reduces the power density to 294 W/in<sup>3</sup>.

In order to exploit the full potential of the LEGO-PoL architecture for high power density and in-packaging vertical power delivery, a design iteration on the original LEGO-PoL prototype was conducted, resulting in the development of Mini-LEGO. The new hardware prototype achieves significantly smaller area and lower height, enabled by (1) improved device implementation, (2) optimized gate drive circuitry, (3) optimized magnetics, (4) higher switching frequency, and (5) compact packaging. Mini-LEGO reduces the height of the 48-V VRM from 16.65 mm to 8.4 mm as compared to the first iteration LEGO-PoL design. It has a current area density of 0.71 A/mm<sup>2</sup> and achieves a power density of 1390 W/in<sup>3</sup> including all gate drive circuitry. The peak efficiency including the gate driving loss is 84.1%. Mini-LEGO trades off energy efficiency to realize improvements in power density and control bandwidth. The miniaturized size and thickness allows the VRM to be packaged much closer to the microprocessor where abundant cooling resources are available, which helps to mitigate the challenges of thermal management due to lower efficiency.

The remainder of this chapter is structured as follows: Section 3.2 introduces the key metrics for evaluating architectures for VRMs and presents a categorization methodology for organizing architectures and evaluating how they perform in each key metric. Section 3.3 introduces the LEGO-PoL architecture as a hybrid

switched-capacitor architecture that is well-suited for efficient, dense, and high bandwidth VRMs, explains its operating principles, and analyzes the mechanism of how it achieves automatic current sharing and voltage balancing. Section 3.4 details the development of the first iteration vertical stacked LEGO-PoL hardware prototype and presents experimental results. Section 3.5 focuses on the second design iteration Mini-LEGO design, explains how it improves upon the previous design, and presents its experimental results. Section 3.6 analyzes and discusses how Mini-LEGO performs compared to the first iteration LEGO-PoL design as well as a representative selection of other 48-V VRM designs from academia and industry. Lastly, section 3.7 concludes this chapter.

## 3.2 Architectures for Voltage Regulator Modules

Many different approaches for microprocessor power delivery have been explored in previous literature. Architectures for VRMs can be categorized based on certain defining features detailed in this subsection. When designing a VRM, three main metrics, each with connected trade-offs, are of key consideration:

1. **Size:** The system area ( $x \times y$ ) and height ( $z$ ) are critical constraints set by the end application for the VRM. Power density (units: W/in<sup>3</sup>) and current area density (units: A/mm<sup>2</sup>) are important benchmarking metrics dependent on the size of the VRM and its power handling capability.
2. **Efficiency:** The overall VRM efficiency curve measures how much loss is present throughout the entire output load curve. Depending on the application, certain points of the load curve (e.g. thermal design points) are of more significance than others and high efficiency at these operating conditions is crucial. The VRM loss ties together with the overall thermal solution required to cool the VRM.

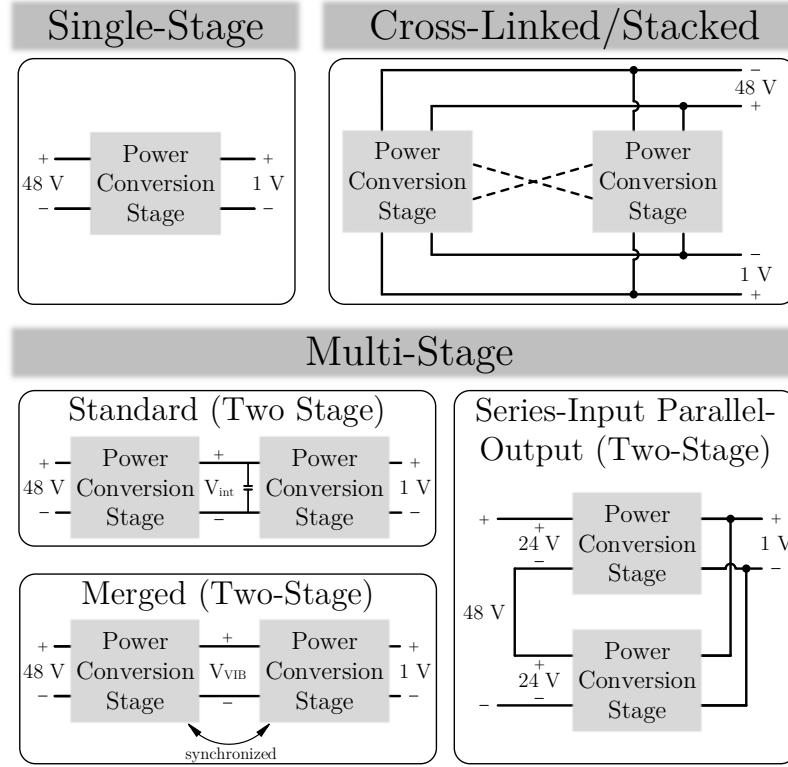


Figure 3.3: Power conversion stages are the building blocks of VRM architectures. Architectures can be either single-stage, multi-stage, or cross-linked/stacked.

**3. Control Bandwidth:** The speed at which the VRM responds to changes in the output power demand depends on the output filter of the VRM (output inductance and output capacitance) as well as the switching frequency. More and more stringent transient requirements are being placed on VRMs. Dynamic voltage and frequency scaling (DVFS) is commonly needed in modern microprocessors.

All of the evaluation criteria for how a VRM performs for a set application can generally be grouped into these three major categories. Different architectures offer ways to trade off performance in one of these metrics to achieve benefits in the others. To classify a given architecture and understand its strengths and weaknesses in regards to the above metrics, **four major design choices** are used to categorize an architecture:

**1. Arrangement of Power Conversion Stages:** A “stage” is defined as a building block in the architecture that can be represented as a two-port network with a dc voltage at the input and dc voltage at the output. Each stage typically comprises one major power conversion mechanism. These dc voltages can have significant ac ripple superimposed on them. VRM architectures can be classified in terms of their stages as follows:

- *Single-Stage:* Architectures that consist of only one power conversion stage.
- *Multi-Stage:* Architectures that consist of two or more power conversion stages. A specific subset of multi-stage architectures, referred to as “merged multi-stage,” have multiple stages that require synchronized operation between them for proper operation. Another subset is the “series-input parallel-output” (SIPo) arrangement, in which the inputs of multiple stages are configured in series and their outputs are configured in parallel.
- *Cross-Linked or Stacked:* Architectures that consist of multiple power conversion stages that are interlinked in such a way that the operation of these different stages must be coordinated.

These classifications are illustrated in Fig. 3.3. Each stage is represented as a black-box two-port network.

**2. Energy Transfer Mechanism:** Each power conversion stage within an architecture can be classified by their primary energy storage component:

- *Capacitor-Based:* Stages that primarily utilize capacitors as the energy storage element, known as “switched-capacitor” circuits. These circuits leverage the high energy density of capacitors to achieve high power densities. Certain techniques, such as soft-switching and soft-charging (detailed

more in Section 3.3) use small magnetic components to enable higher efficiencies.

- *Magnetics-Based:* Stages that use either transformers or inductors as the primary energy storage element. Transformers can provide high voltage conversion ratios, and magnetics-based designs offer high efficiency. Energy densities of magnetic components are lower than capacitors, limiting the power density of these solutions. Magnetic materials for VRMs need to operate at high frequencies with high permeabilities and low losses.

### **3. Operation Mechanism:**

- *Pulse-Width-Modulation (PWM):* PWM topologies process energy as pulsed square waves, and are more widely used with more mature control solutions.
- *Resonant:* Resonant topologies process energy with sinusoidal or piecewise sinusoidal waveforms. These topologies offer opportunities to achieve soft-switching, which leads to higher efficiency at higher switching frequencies.

### **4. Regulation:** Stages that can maintain a desired output voltage or current level throughout any variations in input or output conditions are capable of performing regulation. There are two types of regulation that a stage can perform:

- *Voltage Source Output:* These stages can dynamically change the output voltage in response to changes in the input or the output to either maintain a constant output voltage or adjust the output voltage to a desired level.

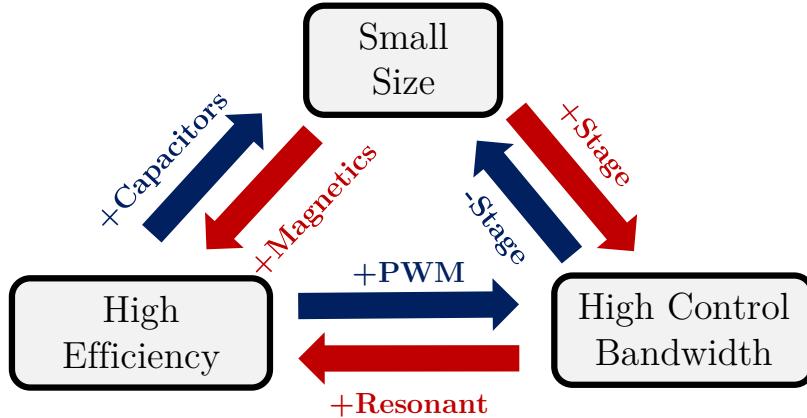


Figure 3.4: Architecture selection chart based on which performance factor – small size, high efficiency, and/or high control bandwidth – is more important for a given application.

- *Current Source Output:* These stages are able to maintain a constant current output and rapidly adjust the output current to keep the voltage ripple due to a transient event small.

Sometimes there is no clear distinction between voltage source output and current source output. The main power conversion mechanism, capacitor-based or inductor-based, determines the core state variable that is controlled in the power electronics system.

Depending on the application, some design factors are more significant than others. The architecture classifications detailed can be leveraged to optimize a design for one performance factor over another. Figure 3.4 summarizes the trade-offs present when designing an architecture for 48-V VRMs.

The arrangement and number of power conversion stages has a strong correlation on the trade-off between the power density and the control bandwidth. Lower number of power conversion stages generally leads to a lower component count design, and this can lead to higher power density and lower overall system size. Multi-stage designs, on the other hand, enable different stages to operate at different frequencies, which creates opportunities to increase the control bandwidth without greatly increasing

the overall system loss. Merged multi-stage and SIPO architectures can partially counteract the increase in size due to multiple stages – such an approach in the LEGO-PoL architecture is described more in detail in the following section.

The energy transfer mechanism impacts the trade-off between the efficiency and power density. Magnetic-based stages generally have higher efficiency, at the expense of power density owing to their bulkiness. Increasing the switching frequency is one method of miniaturizing the size of magnetic components, however, the loss mechanisms of magnetic components progressively worsen as the frequency continues to go up. The performance metrics of magnetic components improve as their size increases, making small and efficient power inductors rare [11]. Capacitor-based stages are much smaller in size, as the energy density of capacitors is much higher than that of magnetic components. The efficiency of capacitor-based architectures can improve if larger size capacitors are used, but this comes at the expense of power density. Utilizing small magnetic components in capacitor-dominant stages enables soft-switching and soft-charging opportunities that can greatly increase the efficiency.

Lastly, the operation mechanism impacts the trade-off between efficiency and control bandwidth. Resonant stages can achieve high efficiency as a result of soft-switching. This allows resonant converters to switch at high frequencies. However, this comes at the expense of more complex control methods for precise regulation. PWM stages, on the other hand, have mature control solutions that have been well studied.

### **3.3 Hybrid Switched-Capacitor Linear-Extendable Group-Operated Point-of-Load (LEGO-PoL) Architecture**

This section presents the key concepts of hybrid switched-capacitor circuits and introduces the LEGO-PoL architecture and its operation mechanisms.

### 3.3.1 Hybrid Switched-Capacitor Operation Mechanisms

As mentioned in the discussion on multi-stage architectures in Section 3.2, capacitor-based multi-stage architectures can offer high control bandwidth and leverage capacitor energy density to keep the size small. In these architectures, while the first stage is typically a capacitor-based stage, the second stage is a magnetics-based stage to perform voltage regulation. The capacitor-based SC stage functions as a DCX, with a fixed voltage conversion ratio leveraging the high energy density of capacitors to step down the high input voltage and feed a lower input voltage to the magnetics-based regulation stage. However, the SC stages suffers from a common limitation in capacitor-based circuits referred to as “hard-charging,” whereby capacitors of different voltage levels are connected directly in parallel, resulting in large energy dissipation and larger loss ( $\frac{1}{2}C\Delta V^2$  dissipated across the parasitic resistance between the capacitors). Without introducing additional circuit elements, the only ways to mitigate this effect are to either use large capacitance values or higher frequencies to reduce the voltage ripple. Larger capacitors increase the system size, while higher frequencies can increase the losses and result in lower system efficiency. “Soft-charging,” on the other hand, uses magnetic components which function as a current source to shuffle the charge between capacitors with a well-defined current. This avoids the large current spikes and charge redistribution loss present under hard-charging.

The two main approaches to achieving soft-charging are resonant soft charging or merged multi-stage soft charging, as shown in Figure 3.5. Resonant soft-charging uses small inductors in series with flying capacitors in the SC stage to form a resonant tank. By switching the SC stage at the resonant frequency of the *LC* tank, a sinusoidal current is used to charge and discharge the flying capacitors, avoiding the problematic large current spikes. Switching the converter at the zero-crossing points of the sinusoidal current creates opportunities for soft-switching (where the devices are turned on or off at a point where there is zero voltage across or zero

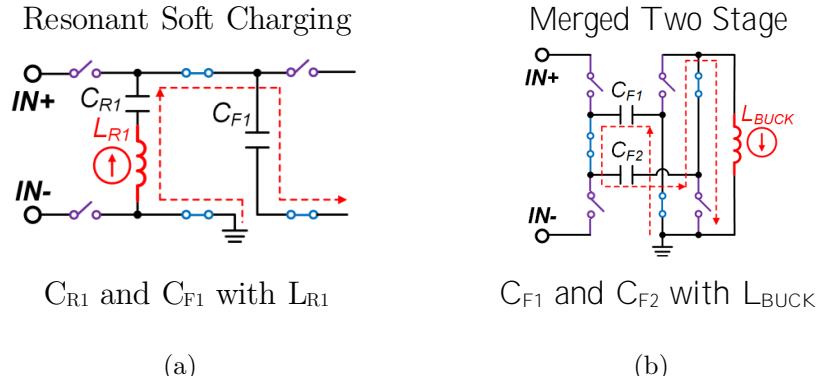


Figure 3.5: (a) Resonant soft charging, where  $C_{R1}$  and  $L_{R1}$  form a resonant tank. (b) Merged two-stage soft charging, where the inductor in the buck stage  $L_{BUCK}$  soft charges  $C_{F1}$  and  $C_{F2}$ .

current through the switch) which can greatly reduce the overall system switching losses. While advantageous from an efficiency standpoint, the resonant approach has drawbacks that hamper its performance on other metrics. Magnetics tend to be the bulkiest component in a power converter, and the resonant approach requires inductors in the SC stage as well as magnetics in the second stage, increasing system size and complicating the system packaging. Switching frequency of the SC stage is limited to the resonant frequency, which requires capacitances which are well controlled under different temperatures and dc bias voltages, reducing design flexibility and increasing cost. Resonant SC converters also require large decoupling capacitors between the two stages, which further reduces the system density.

The second approach to achieving soft-charging is by merging the stages together. By merging the multiple stages, these architectures can obtain soft-charging by using the magnetic components in the second stage to prevent the connection of capacitors of different voltage levels directly in parallel [60, 61]. To achieve this, the large decoupling capacitor between the stages is removed, effectively coupling the operation of the stages. Compared to the resonant approach, merged multi-stage architectures can reuse the magnetics in the regulation stage and eliminate the need for inductors in

the SC stage. These architectures obtain high efficiency and power density, counteracting the trade-off of capacitor-based architectures between efficiency and size. The LEGO-PoL architecture, detailed in the following subsection, uses a merged two-stage approach, with a SIPO structure to achieve high efficiency, high density, and high control bandwidth.

### 3.3.2 LEGO-PoL Architecture

Figure 3.6 shows the key principles of the merged two-stage LEGO-PoL architecture with  $N$  submodules. One LEGO-PoL submodule comprises two building blocks: a 2:1 SC unit and an  $M$ -phase buck unit. The 2:1 SC unit operates with fixed complementary 50% duty cycles ( $\phi_1$  and  $\phi_2$ ). It is operated at a low frequency to reduce switching losses and achieve high efficiency. Each SC unit contains two flying capacitors. The buck unit consists of  $M$  phases, and makes use of interleaving operation to split the submodule output current across multiple phases. It operates at a higher switching frequency for high control bandwidth. This enables the buck unit to effectively reject the voltage ripple present on the intermediate bus, which is present as there is no large dc decoupling capacitor between the two stages. The two stages are functionally merged, and the buck units act as current sources to soft-charge the flying capacitors.

The LEGO-PoL architecture is highly modular and scalable. The number of submodules can be extended to cover a wider operation range in both the voltage and current domains. With buck units as the output stage, the LEGO-PoL architecture can leverage state-of-the-art voltage-mode or current-mode control techniques that have been developed for buck-based VRMs. The  $N$  series-connected 2:1 SC units split the input voltage into  $N$  voltage domains, each equal to  $\frac{V_{IN}}{N}$ . The  $N$  parallel-connected  $M$ -phase buck units divide the output current into  $N$  current paths. Each individual phase of the buck units delivers  $\frac{1}{M \times N}$  of the output current. The dc value

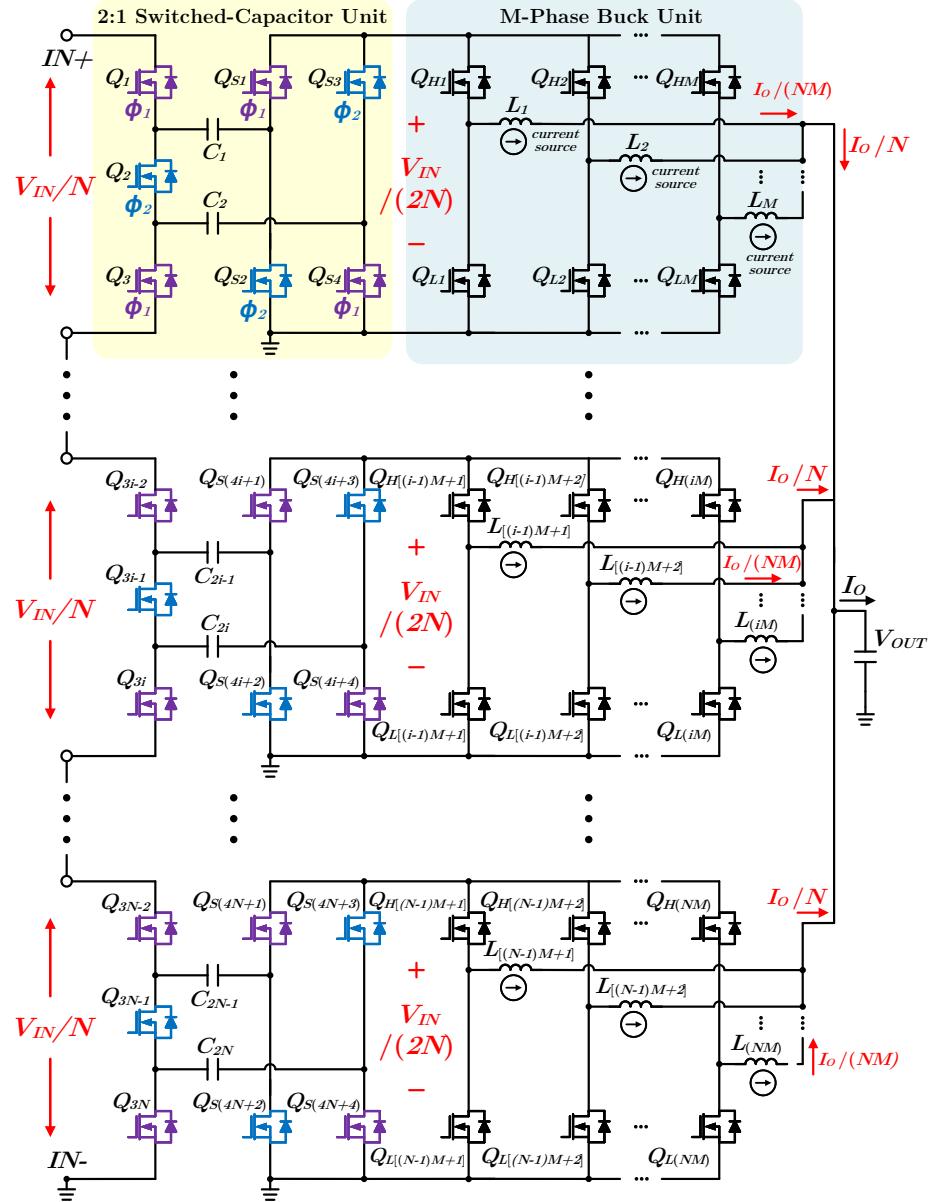


Figure 3.6:  $N$ -submodules of the merged two-stage LEGO-PoL architecture. One LEGO-PoL submodule comprises one 2:1 SC unit and one  $M$ -phase buck unit.  $N$  submodules are connected with their inputs in series and outputs in parallel. The LEGO-PoL architecture can be linearly extended for different input voltage and output current specifications.

of the virtual intermediate bus voltage is equal to  $\frac{V_{IN}}{2N}$ . By equally distributing the high input voltage stress and high output current stress into each submodule, the architecture can utilize lower rated semiconductor devices with uniformly distributed heat dissipation across the submodules.

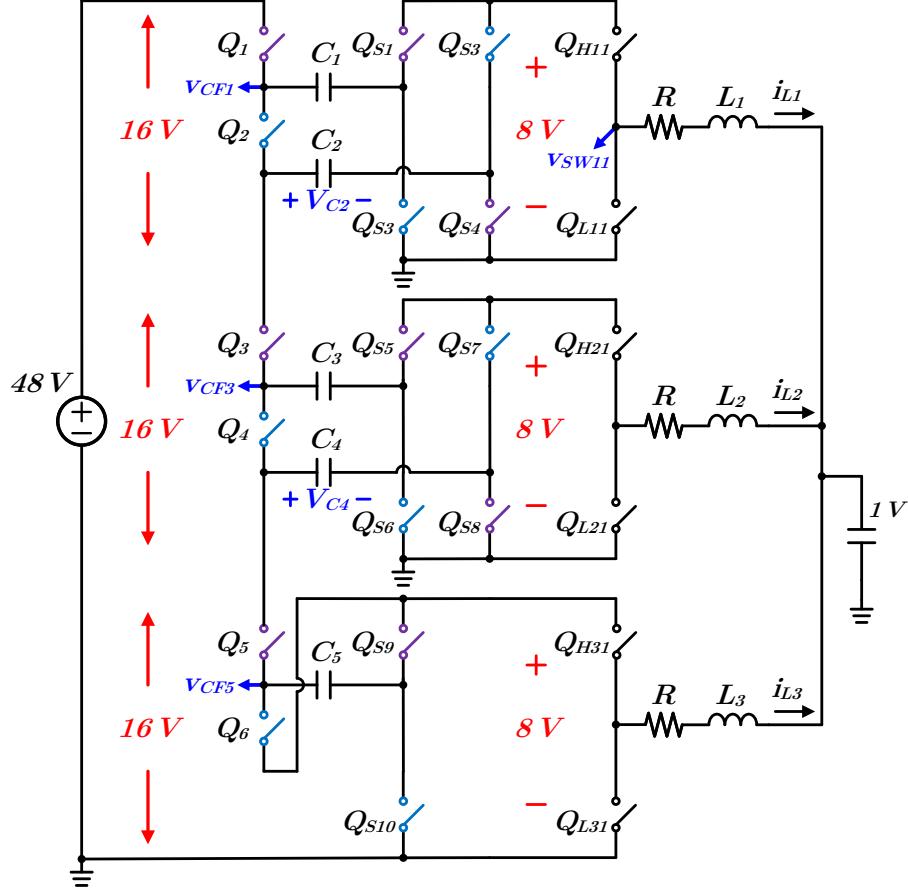


Figure 3.7: Schematic of a three submodule LEGO-PoL converter with 48 V input voltage and 1 V output voltage for investigating the operation mechanisms. Single phase buck units are used to simplify the analysis. The switches with purple color are controlled by a PWM signal  $\phi_1$ , while the switches with blue color are controlled by a PWM signal  $\phi_2$ . The resistance  $R$  represents a lumped resistance encompassing all of the parasitic resistance in a submodule.

The LEGO-PoL architecture decouples the voltage stress, current stress, and dynamic requirements and addresses these design challenges. This section presents the soft switching, soft charging, current sharing, and voltage balancing mechanisms in detail.

### Operation Mechanisms of the LEGO-PoL Architecture

Figures 3.7 and 3.8 show a topology and operational waveforms of a LEGO-PoL converter comprising three ( $N = 3$ ) 2:1 SC units and three single-phase ( $M = 1$ )

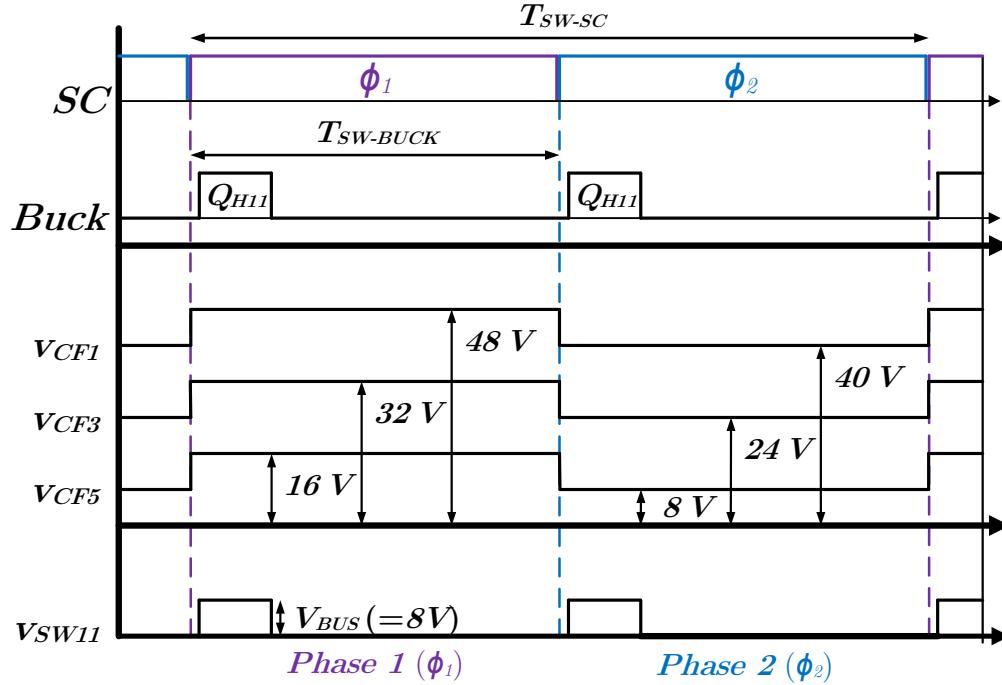


Figure 3.8: Operational waveforms of the LEGO-PoL converter shown in Figure 3.7.

buck units to illustrate the operation mechanisms. The SC units in Figure 3.7 are simplified from Figure 3.6. The series-connected switches in Figure 3.6, such as  $Q_3$  and  $Q_{3i-2}$ , can be merged as one switch,  $Q_3$  in Figure 3.7. One switch ( $Q_{3N}$ ), one capacitor ( $C_{2N}$ ), and two synchronous rectifier switches ( $Q_{S(4N+3)}$  and  $Q_{S(4N+4)}$ ) in the third 2:1 SC unit can be removed because the voltage across  $C_{2N}$  is zero. Switch  $Q_6$  is connected to the output of the third 2:1 SC unit.

### Soft Switching and Soft Charging

The LEGO-PoL architecture leverages the merged two-stage concept presented in [61, 62]. There are two options for implementing merged two-stage operations. The first is when the LEGO-PoL converter is designed with a very low parasitic inductance (e.g.,  $\ll 1$  nH) along the current path between the SC stage and the buck stage. In this option, the capacitors of the SC stage are used as the input capacitors of the buck stage, and the decoupling capacitor between the two stages is eliminated. Buck

inductor currents can only conduct through each SC unit when the high-side buck switches ( $Q_{Hx}$ ) are turned on. Zero-current-switching is achieved in the SC units by coordinating the switching sequences of the SC units and buck units. The key principle is to change the state of the SC units during the free-wheeling state of the buck units, when all of the high-side switches in the buck units are turned off. (Figure 3.8). The capacitors of the SC units are always charged and discharged by the buck stage which acts as a current source. Figure 3.9 highlights the principles of soft charging operation during phase 1 and phase 2. The capacitors are always charged and discharged by a current source, eliminating the large current spikes and associated charge redistribution loss with hard charging operation.

The second possible design option is when the LEGO-PoL converter does not have a low enough parasitic inductance (e.g.,  $>1$  nH). In this option, a capacitor between two stages is used. This capacitor is large enough to filter the high frequency pulsating current from the buck stage, and is small enough to maintain low charge sharing loss. The current flowing in the SC units is the input current of the buck units, filtered by the parasitic inductance and filter capacitance. This design option is implemented in the developed prototypes detailed in the following sections. The design of this filter capacitor is further discussed in Section 3.4.1.

In contrast to the resonant hybrid switched-capacitor converter, which achieves soft charging operation by placing an inductor between two capacitors, the LEGO-PoL architecture utilizes the inductors in the buck stage to achieve soft charging. The selection of the switching frequencies of the SC units and buck units are not limited by resonant operation. In both LEGO-PoL design options, the two stages are merged. The large decoupling capacitor present in a traditional two stage architecture is either completely eliminated (option 1) or replaced with a small filter capacitance (option 2). The charge sharing loss is greatly reduced over hard charging operation in both design options.

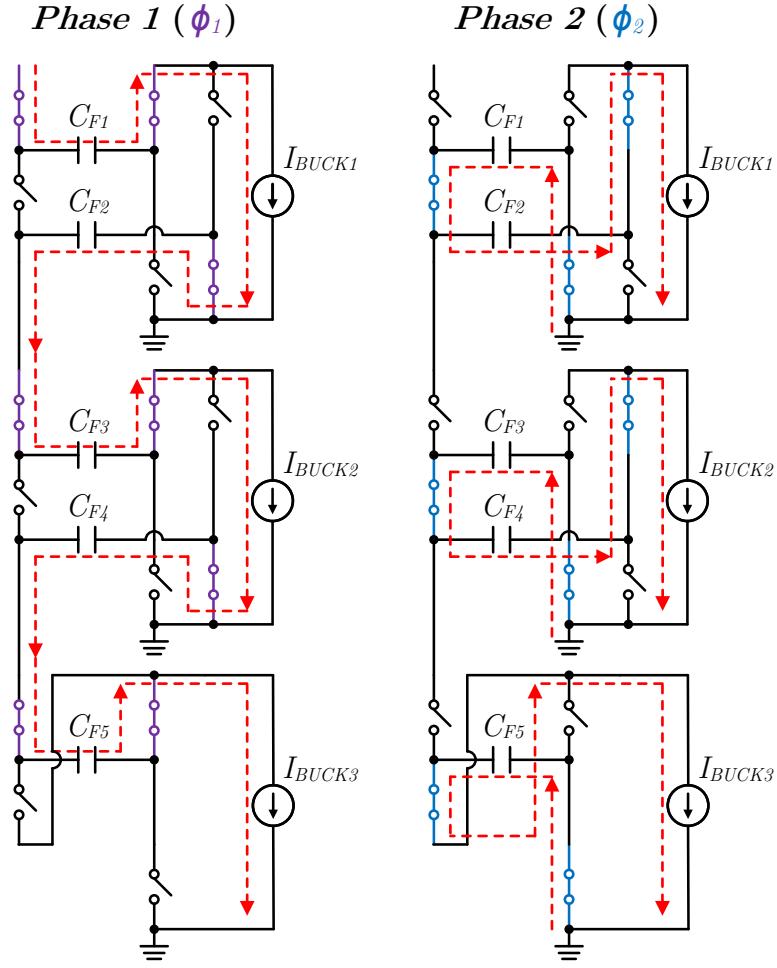


Figure 3.9: Current paths during phase 1 and phase 2 for the LEGO-PoL converter shown in Figure 3.7.

### Automatic Current Sharing and Voltage Balancing

The automatic current sharing and voltage balancing mechanism of the LEGO-PoL architecture can be explained by analyzing the current flow in the two switching phases in Figure 3.7. In each switching cycle, capacitors  $C_2$  and  $C_4$  are charged by one current source in  $\phi_1$ , and discharged by another current source in  $\phi_2$ . Due to the charge balancing requirements of the switched capacitors, the two current sources have to be equal, leading to current sharing between two adjacent modules, and sequentially current sharing to all modules. For example,  $C_2$  is discharged by  $i_{L_2}$  in  $\phi_1$ , and charged by  $i_{L_1}$  in  $\phi_2$ .  $C_3$  is charged by  $i_{L_2}$  in  $\phi_1$ , and discharged by  $i_{L_2}$  in

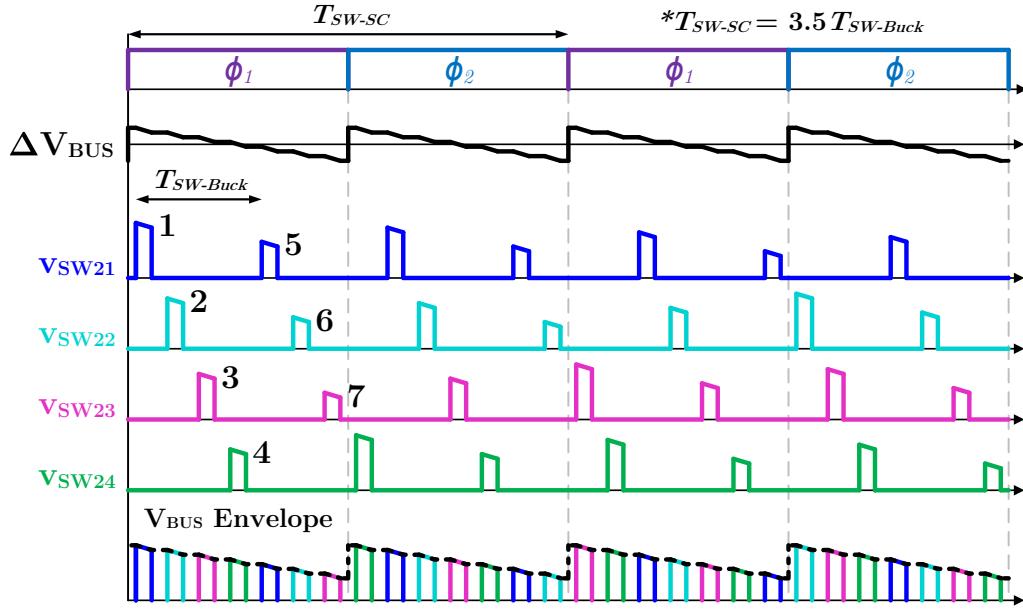


Figure 3.10: An example of passive phase current balancing of the LEGO-PoL converter. Phase rotation enables each buck switch node to have the same average input voltage.

$\phi_2$ . As analyzed in detail in Section 3.3.3, the charge balance requirement of  $C_2$  and  $C_3$  in one switching period forces  $i_{L_1}$  to be equal to  $i_{L_2}$  in steady state operation. Benefiting from a similar SC mechanism, the automatic current sharing leads to automatic voltage balancing between the series stacked switched capacitors. With these features, the LEGO-PoL architecture can handle a very high output current.

### Passive Phase Current Balancing

The LEGO-PoL architecture automatically balances the current between each submodule. The current through each individual phase of a given buck unit can be balanced by coordinating the selection of the switching frequencies of the SC stage and buck stage. Since the LEGO-PoL architecture either removes the large dc decoupling capacitor between the two stages or replaces it with a significantly smaller filter capacitor, the virtual intermediate bus voltages ( $V_{BUS}$ ) contain a higher ripple. This may cause phase current mismatch in a buck unit if certain phases are always

seeing higher input voltage while other phases are always seeing lower voltage. There are a few methods to balance the phase currents in the presence of this ripple, including active current mode control. The duty ratios of the buck unit switches can be actively modulated to compensate for the input voltage ripple and balance phase currents. Another way is to use a passive phase rotating scheme to balance the current as depicted in Figure 3.10. When the buck switching frequency is chosen as

$$f_{\text{Buck}} = \frac{2k+1}{2} f_{\text{SC}}, \quad k = 1, 2, 3, \dots \quad (3.1)$$

where  $f_{\text{Buck}}$  and  $f_{\text{SC}}$  are the switching frequencies of the buck stage and SC stage, respectively, an odd number (seven, in the example of Figure 3.10) of buck switching occurrences happen during a half switching cycle of the SC stage. This results in rotating through the different buck switches, each taking a turn as the one turned on at the highest  $V_{\text{BUS}}$  ripple, and resulting in identical average input voltage across all buck switch nodes.

### Summary of LEGO-PoL Architecture

The following list summarizes the advantages of the LEGO-PoL architecture, and compares the features of this architecture over other commonly used VRM solutions:

- Different from a traditional intermediate bus converter architecture with a transformer-based first stage [63], the front-end of the LEGO-PoL architecture leverages the advantages of switched-capacitor-based solutions over transformer-based solutions [64]. It scales well to high-frequency operation and is not limited by the availability of high-performance magnetic materials in the MHz range.
- Compared to other switched-capacitor or resonant-switched-capacitor two-stage solutions [65], the LEGO-PoL architecture can greatly reduce both the size of

the flying capacitance required in the first stage and the decoupling capacitance on the intermediate bus, while offering automatic voltage balancing and current sharing as needed in high power applications.

- Compared to other single-stage or merged two-stage solutions with a switched-capacitor front-end followed by a buck-derived unit, where all switches are synchronously operated with one common clock [24, 36, 38], the LEGO-PoL architecture allows for different switched-capacitor units to operate at different frequencies to better balance the trade-off between device utilization, efficiency, and control bandwidth.

### 3.3.3 Analysis of Automatic Current Sharing and Voltage Balancing

This subsection analyzes the automatic current sharing and voltage balancing mechanism in the LEGO-PoL architecture. A large signal average analysis is performed to illustrate the principle of the automatic current sharing and voltage balancing mechanisms. In the three submodule system depicted in Figure 3.7, assume the duty ratio of the buck converter (i.e., the duty ratio of high side switches) is  $D$ ,  $L_x$  is connected with a series resistance  $R$  which encompasses the parasitic resistance of an entire submodule, the large-signal average current of  $L_x$  is  $i_x$ , the large-signal average voltage of  $C_y$  is  $v_{C_y}$ , where  $x \in \{1, 2, 3\}$  and  $y \in \{2, 4\}$ . The large-signal average models are:

$$\begin{aligned} L_1 \frac{di_{L_1}}{dt} &= \langle v_{L_1} \rangle = \frac{1}{2}(V_{in} - v_{C_2})D - v_o - i_{L_1}R, \\ L_2 \frac{di_{L_2}}{dt} &= \langle v_{L_2} \rangle = \frac{1}{2}(v_{C_2} - v_{C_4})D - v_o - i_{L_2}R, \\ L_3 \frac{di_{L_3}}{dt} &= \langle v_{L_3} \rangle = \frac{1}{2}v_{C_4}D - v_o - i_{L_3}R. \end{aligned} \quad (3.2)$$

$$\begin{aligned} C_2 \frac{dv_{C_2}}{dt} &= \langle i_{C_2} \rangle = \frac{1}{2}(Di_{L_1} - Di_{L_2}), \\ C_4 \frac{dv_{C_4}}{dt} &= \langle i_{C_2} \rangle = \frac{1}{2}(Di_{L_2} - Di_{L_3}). \end{aligned} \quad (3.3)$$

Note  $v_{C_1}$ ,  $v_{C_3}$ , and  $v_{C_5}$  are canceled out in (3.3), and do not impact the large-signal dynamics. The charge balance requirement of capacitor  $C_2$  and  $C_4$  leads to the automatic current sharing mechanism among  $L_1$ ,  $L_2$ , and  $L_3$ . Assuming that  $L_1 = L_2 = L_3 = L$  and  $C_2 = C_4 = C$ , the second-order differential equations for the current of the three submodule LEGO-PoL system can be obtained from (3.2):

$$\begin{aligned} \ddot{\mathbf{X}} + \frac{R}{L}\dot{\mathbf{X}} + \frac{D^2}{4LC}\mathbf{M}\mathbf{X} &= 0, \\ \ddot{\mathbf{X}} = \begin{bmatrix} \frac{d^2i_{L_1}}{dt^2} \\ \frac{d^2i_{L_2}}{dt^2} \\ \frac{d^2i_{L_3}}{dt^2} \end{bmatrix}, \quad \dot{\mathbf{X}} = \begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \\ \frac{di_{L_3}}{dt} \end{bmatrix}, \quad \mathbf{X} = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_3} \end{bmatrix}, \\ \mathbf{M} = \begin{bmatrix} 1 & -1 & 0 \\ -1 & 2 & -1 \\ 0 & -1 & 1 \end{bmatrix}, \quad (3.4) \\ \mathbf{Q}^{-1} = \frac{1}{6} \begin{bmatrix} 2 & 2 & 2 \\ -3 & 0 & 3 \\ 1 & -2 & 1 \end{bmatrix}, \quad \mathbf{\Lambda} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 3 \end{bmatrix}. \end{aligned}$$

Note  $\mathbf{M}$  is a real symmetric matrix.  $\mathbf{M}$  can be diagonalized as  $\mathbf{M} = \mathbf{Q}\mathbf{\Lambda}\mathbf{Q}^{-1}$  where  $\mathbf{Q}$  is a matrix composed of eigenvectors ( $\mathbf{e}_1$ ,  $\mathbf{e}_2$ , and  $\mathbf{e}_3$ ), and  $\mathbf{\Lambda}$  is a diagonal matrix composed of eigenvalues ( $\lambda_1$ ,  $\lambda_2$ , and  $\lambda_3$ ) of  $\mathbf{M}$ . (3.4) can be rewritten as (3.5) by

denoting  $\mathbf{Y} = \mathbf{Q}^{-1}\mathbf{X}$ :

$$\begin{aligned} \ddot{\mathbf{Y}} + \frac{R}{L}\dot{\mathbf{Y}} + \frac{D^2}{4LC}\boldsymbol{\Lambda}\mathbf{Y} &= 0, \\ \frac{d^2y_1}{dt^2} + \frac{R}{L}\frac{dy_1}{dt} + \frac{D^2}{4LC}(\lambda_1 y_1) &= 0, \\ \frac{d^2y_2}{dt^2} + \frac{R}{L}\frac{dy_2}{dt} + \frac{D^2}{4LC}(\lambda_2 y_2) &= 0, \\ \frac{d^2y_3}{dt^2} + \frac{R}{L}\frac{dy_3}{dt} + \frac{D^2}{4LC}(\lambda_3 y_3) &= 0. \end{aligned} \quad (3.5)$$

Since  $i_{L_1} - i_{L_3}$  is linearly proportional to  $y_2$ , the second-order differential equation describing  $i_{L_1} - i_{L_3}$  is:

$$\frac{d^2(i_{L_1} - i_{L_3})}{dt^2} + \frac{R}{L}\frac{d(i_{L_1} - i_{L_3})}{dt} + \frac{D^2}{4LC}(i_{L_1} - i_{L_3}) = 0. \quad (3.6)$$

This second-order differential equation describes the large-signal dynamics of the current difference between  $i_{L_1}$  and  $i_{L_3}$ . The natural frequency  $\omega_n$  of this second order oscillation system is  $\frac{D}{2\sqrt{LC}}$ . The damping ratio  $\zeta$  is  $\frac{R}{D}\sqrt{\frac{C}{L}}$ . The decay rate  $\alpha$  is  $\frac{R}{2L}$ , the quality factor  $Q$  is  $\frac{D}{2R}\sqrt{\frac{L}{C}}$ . The current difference will respond to perturbations like a second-order system, and gradually decay to zero in periodic steady state. As  $i_{L_1}$  and  $i_{L_3}$  converge, based on (3.4), since  $y_3$  is proportional to  $i_{L_1} - 2i_{L_2} + i_{L_3}$ , and  $y_3$  damps to zero, all currents are equal in steady state. The current sharing mechanism of the LEGO-PoL converter is very similar to that of the series-capacitor buck converter [66]. As the current differences between inductors are zero, the average voltages of  $C_2$  and  $C_4$ ,  $v_{C_2}$  and  $v_{C_4}$ , reach  $\frac{2V_{in}}{3}$  and  $\frac{V_{in}}{3}$ , respectively, because the average voltage across all switch nodes needs to be equal.  $v_{C_1}$ ,  $v_{C_3}$ , and  $v_{C_5}$  are set by the switched capacitor mechanism due to the presence of the small filtering capacitor  $C_{filter}$ . This guarantees automatic voltage balancing of the LEGO-PoL architecture.

Figure 3.11 compares the large-signal average model against SPICE simulation results. The model is derived with  $V_{in} = 48$  V,  $D = 0.2$ ,  $L_x = 1$   $\mu$ H,  $C_y = 45$   $\mu$ F,

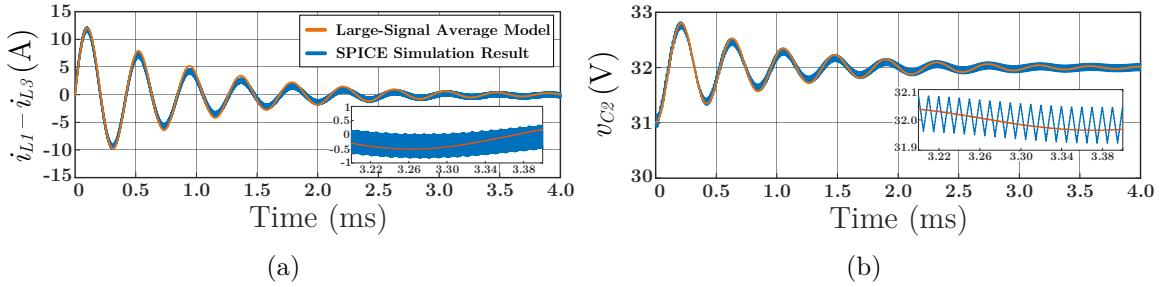


Figure 3.11: Large-signal average model and SPICE simulated transient response of the automatic current sharing dynamics for the three submodule design in Figure 3.7. As described in (3.5),  $v_{C_1}$ ,  $v_{C_3}$ , and  $v_{C_5}$  have no impact on the transient dynamics. Their dc values are set by the switched capacitor mechanism due to the existence of  $C_{\text{filter}}$ .

and  $R = 2 \text{ m}\Omega$ . The initial conditions of this simulation are  $i_{L_1}(0) = i_{L_2}(0) = i_{L_3}(0) = 0 \text{ A}$ ,  $v_{C_2}(0) = 31 \text{ V}$ , and  $v_{C_4}(0) = 15 \text{ V}$ . In periodic steady state, the large signal current  $i_{L_1} = i_{L_3}$ , and  $\frac{di_{L_1}}{dt} = \frac{di_{L_3}}{dt} = 0$ . This mechanism holds the large-signal average of  $v_{C_2}$  at  $\frac{2}{3}V_{in}$  and the transient dynamics of the capacitor voltage follows a similar second-order transient dynamic (similar damping ratio and  $Q$ ) as  $i_{L_1} - i_{L_3}$  and gradually damps to  $\frac{2}{3}V_{in}$  following the same oscillation.  $V_{C_2}$  will be automatically maintained at  $\frac{2}{3}V_{in}$  in this example implementation.

This analysis can be extended and generalized for a LEGO-PoL converter with  $N$  submodules. Assuming that  $L_1 = L_2 = \dots = L_N = L$  with series resistance  $R_1 = R_2 = \dots = R_N = R$ ,  $C_2 = C_4 = \dots = C_{2(N-1)} = C$ , and the duty ratio of all high side switches in all buck units is  $D$ , the large-signal average model of the system

is:

$$\ddot{\mathbf{X}} + \frac{R}{L} \dot{\mathbf{X}} + \frac{D^2}{4LC} \mathbf{M} \mathbf{X} = 0, \quad (3.7)$$

$$\ddot{\mathbf{X}} = \begin{bmatrix} \frac{d^2 i_{L_1}}{dt^2} \\ \frac{d^2 i_{L_2}}{dt^2} \\ \vdots \\ \frac{d^2 i_{L_N}}{dt^2} \end{bmatrix}, \quad \dot{\mathbf{X}} = \begin{bmatrix} \frac{di_{L_1}}{dt} \\ \frac{di_{L_2}}{dt} \\ \vdots \\ \frac{di_{L_N}}{dt} \end{bmatrix}, \quad \mathbf{X} = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ \vdots \\ i_{L_N} \end{bmatrix},$$

$$\mathbf{M} = \begin{bmatrix} 1 & -1 & 0 & 0 & \cdots & 0 \\ -1 & 2 & -1 & 0 & \cdots & 0 \\ 0 & -1 & 2 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \cdots & \vdots \\ 0 & 0 & \cdots & -1 & 2 & -1 \\ 0 & 0 & \cdots & 0 & -1 & 1 \end{bmatrix}.$$

$$\mathbf{X}^T \cdot \mathbf{M} \cdot \mathbf{X} = \sum_{k=1}^{N-1} (x_{k+1} - x_k)^2 \geq 0 \quad (3.8)$$

$\mathbf{M}$  is a  $N \times N$  real symmetric matrix, so it can be diagonalized as  $\mathbf{M} = \mathbf{Q} \Lambda \mathbf{Q}^{-1}$ , where  $\mathbf{Q} = [\mathbf{e}_1, \mathbf{e}_2, \dots, \mathbf{e}_N]$  and  $\Lambda$  is the diagonal matrix consisting of eigenvalues  $(\lambda_1, \lambda_2, \dots, \lambda_N)$ . For any non-zero  $\mathbf{x} = [x_1, x_2, \dots, x_N]^T$ ,  $\mathbf{M}$  satisfies (3.8), so  $\mathbf{M}$  is positive semidefinite, i.e.  $\lambda_k \geq 0$ , where  $k \in \{1, 2, \dots, N\}$ . The rank of  $\mathbf{M}$  is  $N - 1$ , so there exists one and only one zero eigenvalue. Assuming  $\lambda_1 = 0$ , the corresponding eigenvector  $\mathbf{e}_1$  is  $[1, 1, \dots, 1]^T$ . Denoting  $\mathbf{Y} = \mathbf{Q}^{-1} \mathbf{X}$ , then (3.7) can be rewritten as (3.9) with explicit solutions:

$$\begin{cases} \frac{d^2 y_1}{dt^2} + \frac{R}{L} \frac{dy_1}{dt} = 0, & k = 1 \\ \frac{d^2 y_k}{dt^2} + \frac{R}{L} \frac{dy_k}{dt} + \left(\frac{D^2 \lambda_k}{4LC}\right) y_k = 0, & k = \{2, 3, \dots, N\} \end{cases} \quad (3.9)$$

The general solutions for (3.9) are:

$$\begin{cases} y_1(t) = K_{11}e^{(-2\alpha t)} + K_{12}, & k = 1 \\ y_{k(k \geq 2)}(t) = K_{k1}e^{(-\alpha + \beta_k)t} + K_{k2}e^{(-\alpha - \beta_k)t}, \end{cases} \quad (3.10)$$

where  $K_1$ ,  $K_2$ ,  $K_{k1}$  and  $K_{k2}$  are constant coefficients,  $\alpha = \frac{R}{2L}$ ,  $\beta_k = \frac{1}{2}\sqrt{(\frac{R}{L})^2 - \frac{D^2\lambda_k}{LC}}$ .

There are three cases for the solution of  $y_{k(k \geq 2)}(t)$ : two different real roots, repeated roots, and complex roots. In all three cases, since  $\alpha$  is positive,  $y_1(t)$  damps to  $K_{12}$  and  $y_{k(k \geq 2)}(t)$  damps to zero as  $t \rightarrow \infty$ . Therefore, in periodic steady state, the large signal inductor currents of the LEGO-PoL architecture with  $N$  submodules and total system output current  $I_O$  will settle to the same constant value  $K_{12} = \frac{I_O}{N}$ :

$$\begin{bmatrix} i_{L1} \\ i_{L2} \\ \vdots \\ i_{LN} \end{bmatrix} = \mathbf{Q} \mathbf{Y} = [\mathbf{e}_1, \mathbf{e}_2, \dots, \mathbf{e}_N] \begin{bmatrix} K_{12} \\ 0 \\ \vdots \\ 0 \end{bmatrix} = \begin{bmatrix} K_{12} \\ K_{12} \\ \vdots \\ K_{12} \end{bmatrix}. \quad (3.11)$$

Similarly, the average capacitor voltages  $V_{C_2}, V_{C_4}, \dots, V_{C_{2(N-1)}}$  damp to a balanced voltage:

$$\begin{bmatrix} V_{C_2} \\ V_{C_4} \\ \vdots \\ V_{C_{2(N-1)}} \end{bmatrix} = \frac{V_{in}}{N} \begin{bmatrix} N-1 \\ N-2 \\ \vdots \\ 1 \end{bmatrix}. \quad (3.12)$$

The voltages of other capacitors are then balanced by the switched capacitor mechanism due to the existence of  $C_{filter}$ . The charge balancing mechanism of the series capacitors guarantees automatic current sharing and automatic voltage balancing for the LEGO-PoL architecture with  $N$  submodules. This property enables

the extendability of the LEGO-PoL architecture to higher or lower submodule counts based on the specific application.

## 3.4 Vertical Stacked LEGO-PoL Converter Design

To validate the suitability of the LEGO-PoL architecture for vertical power delivery, a vertical stacked LEGO-PoL converter is designed, built, and tested [25]. The designed LEGO-PoL converter consists of three submodules, as shown in Figure 3.12. The first stage steps down the input voltage, nominally 48 V (with a range of 40 V to 60 V), to three virtual intermediate bus voltages centered around 8 V, which is then stepped down further by the multiphase buck stage. The converter is designed to achieve a rated output current of 450 A during air-cooled operation and 780 A during liquid-cooled operation. This section details the design methodology for the SC front end, the multiphase buck stage back end, and the considerations required for the virtual intermediate bus as a result of merged multi-stage operation.

### 3.4.1 Switched-Capacitor Stage

Three series-stacked 2:1 SC units split the 48 V input voltage into smaller 16 V voltage domains to enable the utilization of low voltage rating devices with low on-resistance. The voltage stresses on the active switches are either  $V_{BUS}$  or  $2V_{BUS}$ , as the voltage blocked by the switches is always clamped by the flying capacitors. As the maximum voltage rating across any given device is equal to 16 V for an input voltage of 48 V (18 V when considering a maximum input voltage of 60 V), 30 V silicon MOSFETs are used to implement each switch. Without a pre-charging circuit to charge up the flying capacitors to their nominal dc values before start-up, the top switch  $Q_1$  may be required to block the entire input voltage, and for safe operation should be rated for 60 V. However, this was not implemented for the designed prototype.

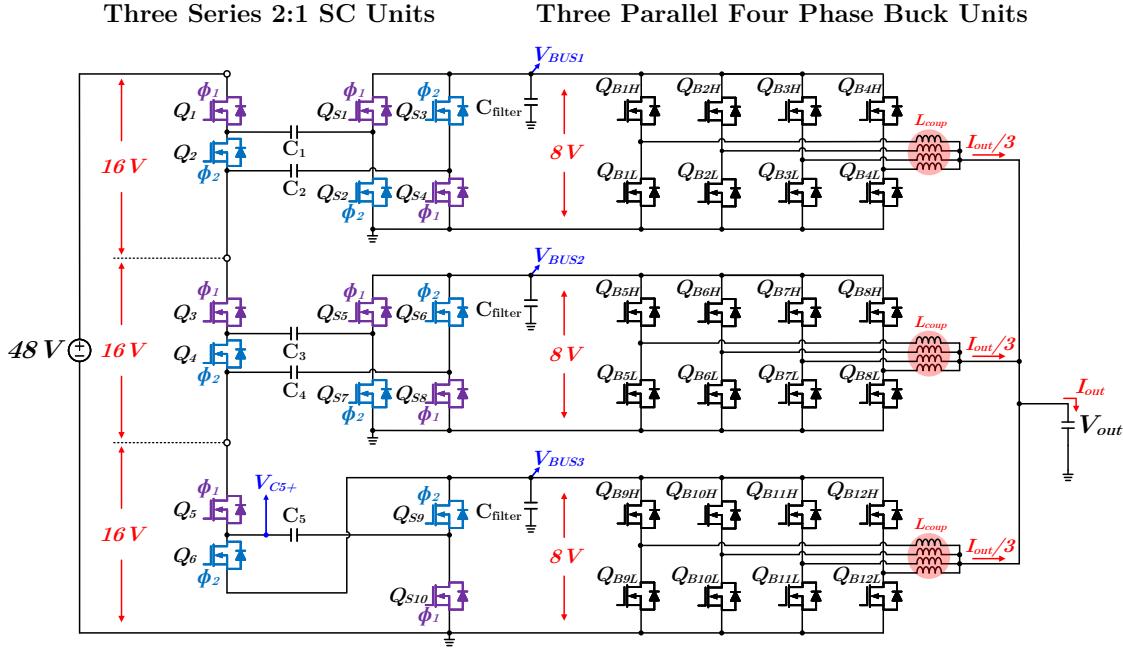


Figure 3.12: Circuit schematic of a three submodule LEGO-PoL converter. The input voltage of 48 V is split into three 8 V virtual intermediate bus voltages, and three parallel configured four-phase buck converters regulate the output voltage. Each buck unit delivers one-third of the total output current.

After selecting the appropriate switches, the next major design decision for the SC stage is sizing the flying capacitors. One of the key merits of the LEGO-PoL architecture as opposed to other SC architectures, specifically the resonant SC architecture [65], is that the values of the flying capacitors do not need to be precisely controlled. In many resonant SC designs, the capacitors need to be carefully selected because the capacitance value determines the soft charging, soft switching, and resonant operation. Capacitance drifting and degradation may have a significant impact on the system performance. In the LEGO-PoL converter,  $C_1 - C_5$  are flying capacitors which charge up to and hold a set dc value. The value of the flying capacitors impacts the voltage ripple across the capacitors, which in turn impacts the voltage ripple across the virtual intermediate bus as these flying capacitors are effectively reused as the input capacitors for the multiphase buck stage. As such, the

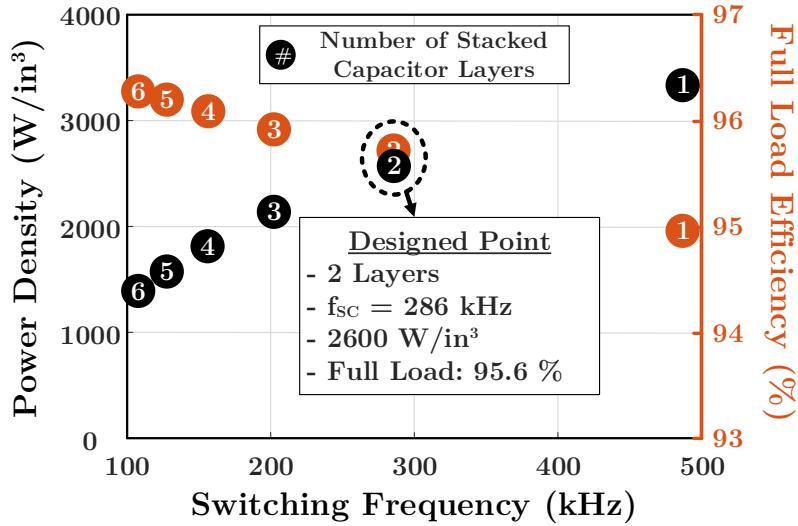


Figure 3.13: For a fixed maximum virtual intermediate bus voltage ripple of 3 V, increasing the number of stacked capacitor layers in the switched-capacitor stage improves the efficiency while reducing the power density. Two stacked capacitor layers are used for the vertical stacked LEGO-PoL prototype.

LEGO-PoL architecture can tolerate capacitance variations that result from dc bias, temperature variation, and/or capacitance degradation.

The capacitance of the flying capacitors is selected to optimize the power density, efficiency, and virtual intermediate bus voltage ripple. The maximum bus voltage ripple occurs at the full load output current, and a 3 V maximum intermediate bus voltage ripple is specified for this application, or a maximum of 40% ripple. In regards to the PCB layout of the SC stage, the power stage area is set by the layout and placement of the switches, which are placed on the top side of the PCB. The bottom side is used for placing the flying capacitors. The capacitance can be increased by vertically stacking layers of capacitors, increasing the overall height while maintaining a fixed area. A trade-off exists between higher capacitor size, which generally results in higher efficiency (due to lower capacitor equivalent series resistance and lower charge sharing loss), and the overall system power density. Height is a crucial metric in regards to evaluating the suitability of a converter for in-packaging vertical power delivery. Figure 3.13 illustrates this trade-off and the selection of the capacitor size.

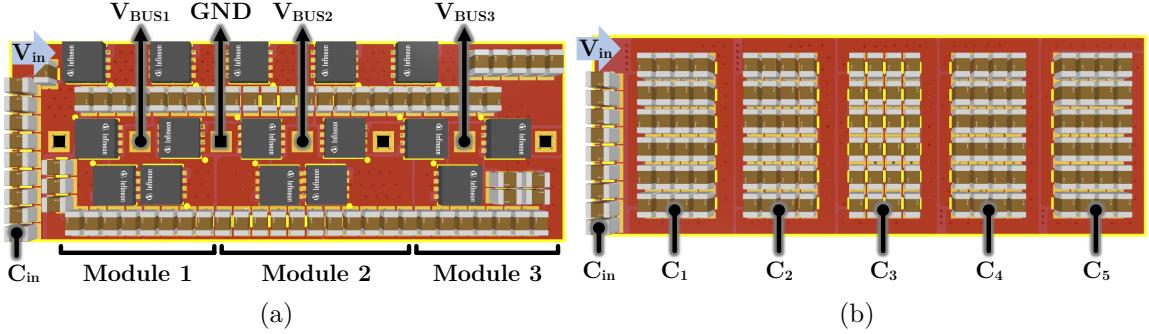


Figure 3.14: Component placement of the SC printed circuit board for the vertical stacked LEGO-PoL converter: (a) top side, where the switches are located; (b) bottom side, which houses the flying capacitors.

For a fixed full load virtual intermediate bus voltage ripple of 3 V, the full load efficiency and system power density is shown for varying numbers of stacked capacitor layers. For the vertical stacked LEGO-PoL prototype, two layers of 0805 ceramic capacitors are stacked with a switching frequency of 286 kHz resulting in a calculated 2600 W/in<sup>3</sup> power density and 95.6% full load efficiency.

Figures 3.14a and 3.14b show the component placement of the SC stage. The total power stage area is 767 mm<sup>2</sup>. On the top layer, MOSFETs and capacitors are placed as close as possible to reduce parasitics. Then, the remaining space is filled with copper traces and capacitors. On the bottom layer, the capacitors are fully modularized to optimize the current path and reduce the PCB conduction loss.

The final part of designing the SC stage is to design a gate drive circuit in order to drive all of the switches in the circuit. Various techniques for implementing gate drive circuits for SC circuits and flying capacitor multi-level converters have been explored [67, 68]. In the switched-tank converter, which uses a resonant Dickson SC topology [69], a charge-pump gate drive circuit is used to generate the bias power for each gate driver integrated circuit (IC) [65]. The SC stage in the vertical stacked LEGO-PoL converter is a Dickson switched-capacitor non-resonant topology, and a similar gate driving method can be adapted.

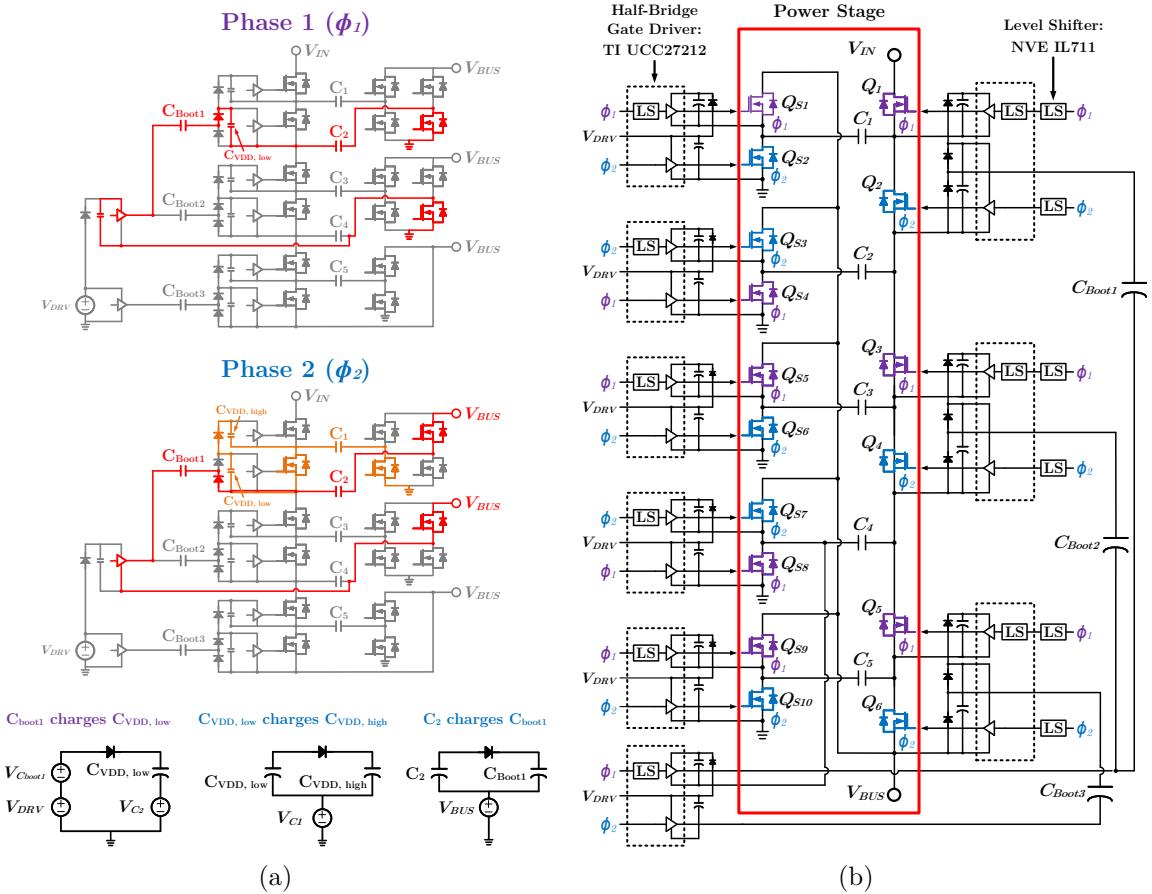


Figure 3.15: (a) Charging mechanism of the bootstrap capacitor and isolated gate driver power supply capacitors highlighted for the first submodule of the SC stage. The equivalent sub-circuits shown below demonstrate how the bootstrap capacitor charges the low side channel power supply capacitor  $C_{VDD, low}$  during phase  $\phi_1$ , which then charges the high side power supply capacitor  $C_{VDD, high}$  during phase  $\phi_2$ . The flying capacitor  $C_2$  charges the bootstrap capacitor during phase  $\phi_2$ . (b) Block diagram of the gate drive implementation for the vertical stacked LEGO-PoL prototype.

The SC stage consists of six floating switches (where the source of the switch is not ground-referenced) and ten ground-referenced switches. For the floating switches, a bootstrapping method is used to provide a floating power supply to the gate driver ICs used to drive these switches. Figure 3.15a illustrates the operation principles of the gate drive circuitry, including the charging process of the bootstrap capacitors. Focusing on  $C_{Boot1}$  as an example, the operation principles of the bootstrap circuit during periodic steady-state include the following:

1. During phase 1 ( $\Phi_1$ ),  $C_{\text{Boot}_1}$  charges the  $V_{DD}$  capacitor of the low side channel of the gate driver IC, denoted  $C_{V_{DD,\text{low}}}$ . The low side channel is off during  $\Phi_1$ .
2. During phase 2 ( $\Phi_2$ ), the bootstrap capacitor is charged by the flying capacitor  $C_2$  until  $V_{C_{\text{Boot}_1}} = V_{C_2}$ .
3. During  $\Phi_2$ , as the bootstrap capacitor is being charged,  $C_{V_{DD,\text{low}}}$  charges up  $C_{V_{DD,\text{high}}}$ .

This charging mechanism holds for  $C_{\text{Boot}_2}$  as well. The last of the six floating switches has its drain connected to the positive terminal of  $C_5$  (as denoted in Fig. 3.12) and its source connected to  $V_{BUS}$ . Thus,  $C_{\text{Boot}_3}$  has a slightly different charging mechanism, and charges during  $\Phi_1$  through the filter capacitors present across  $V_{BUS}$  and ground. The low-side channel of the charge pump is driven by  $\Phi_2$ , used to charge  $C_{\text{Boot}_3}$ , and the high-side channel, which is used to charge the bootstrap capacitors the other two submodules, is driven by  $\Phi_1$ . This gate drive strategy is widely applicable to other switched-tank or Dickson-derived circuits.

### 3.4.2 Multiphase Buck Stage

Three parallel-connected four-phase buck units equally share the full load output current. The peak virtual intermediate bus voltage is 9.5 V (nominally 8 V, with a maximum peak-to-peak voltage ripple of 3 V). The LEGO-PoL architecture enables the multiphase buck stage to switch at a higher frequency than the SC stage due to the reduced voltage stress. In this design, the multiphase buck stage switches at 1 MHz. This reduced stress enables the use of low-voltage high-current semiconductor devices and small magnetics. State-of-the-art control strategies for multiphase buck converters can be adopted. In a traditional multiphase buck converter design, the controller needs to balance the current of all phases. Due to automatic current sharing as described in Section 3.3.3, the controller only needs to balance the current of

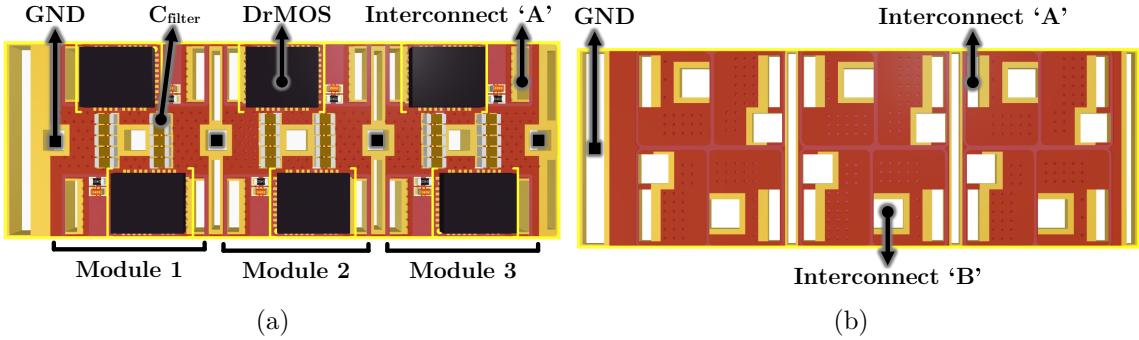


Figure 3.16: Component placement of the switched-capacitor printed circuit board for the vertical stacked LEGO-PoL converter: (a) top side, where the switches are located; (b) bottom side, which houses the flying capacitors.

the four phases within each submodule. This unique feature allows the LEGO-PoL architecture to be scaled to high current without adding significant control complexity, a key advantage of this architecture compared to traditional two-stage intermediate bus architectures with numerous parallel units that require active control for current balancing.

Figure 3.16a shows the component placement of the buck stage. Two 5 mm × 6 mm DrMOS devices are placed on the top and two are placed on the bottom per submodule. Each phase is designed to have the same PCB pattern from the input node to each of the coupled inductor interconnect nodes to minimize the phase current mismatch. Filter capacitors, discussed in Section 3.4.3, are placed in the center of the board to filter the high frequency current.

Figure 3.16b shows the PCB layout of the interposer board. The interposer board decouples the design constraints of the multiphase buck stage and the magnetics. Interconnect ‘A’ is for the buck PCB connection, while interconnect ‘B’ is for the designed inductor. The interposer board is a four-layer PCB; each layer is 2 oz copper, and the overall board thickness is 0.8 mm. Further details on the magnetics design for the vertical stacked LEGO-PoL converter are presented in Section 4.4.

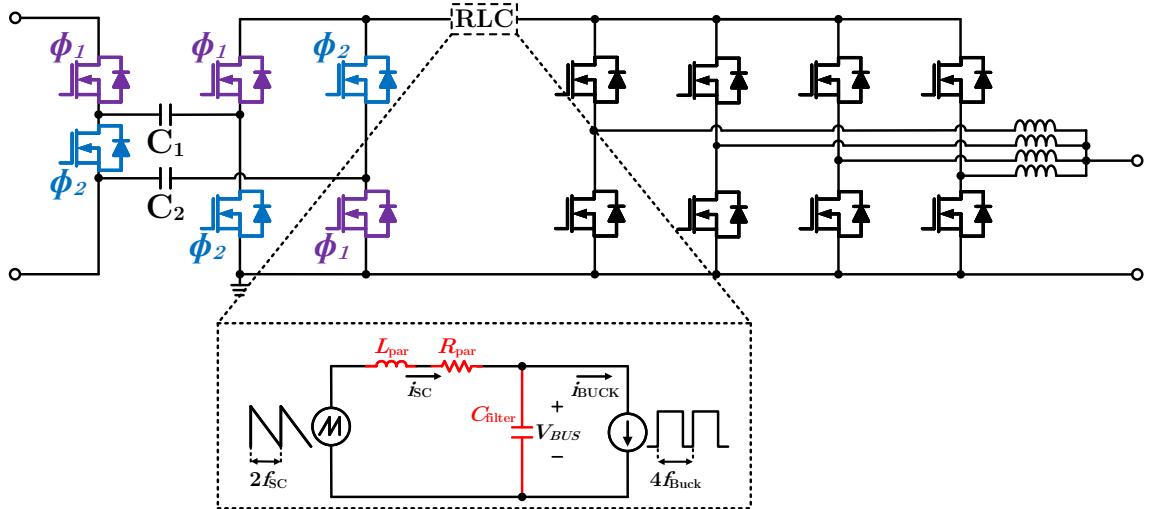


Figure 3.17: One submodule of the LEGO-PoL converter, showing the presence of an RLC circuit between the two stages composed of the parasitic resistance of the SC stage, the parasitic inductance between the two stages, and a filter capacitor. The SC stage can be modeled as a sawtooth voltage with a frequency of  $2f_{SC}$  and the buck stage can be modeled as a pulsed current source with frequency of  $4f_{Buck}$ .

### 3.4.3 Virtual Intermediate Bus Filter

As the multiphase buck stage switches at a high frequency, a small parasitic inductance between the two stages can cause current ringing and increase the current stress on the devices in the SC stage. Figure 3.17 shows an equivalent RLC circuit of one submodule of the LEGO-PoL converter. The SC stage is modeled as a sawtooth voltage source whose frequency is twice of that of the SC stage switching frequency ( $2f_{SC}$ ). The buck unit is modeled as a pulse wave current source with four times the switching frequency of the buck stage ( $4f_{buck}$ ).  $L_{par}$  and  $R_{par}$  are the lumped parasitic inductance and resistance along the current paths in the SC stage.  $C_{filter}$  is a small input capacitor for the buck stage to smooth the high frequency current. The input current of the four-phase buck units ( $i_{buck}$ ) is clamped by the inductor current, while the current going through the SC units ( $i_{SC}$ ) is determined by the RLC filter and has ringing. This issue commonly exists in merged-two-stage designs [61, 62].

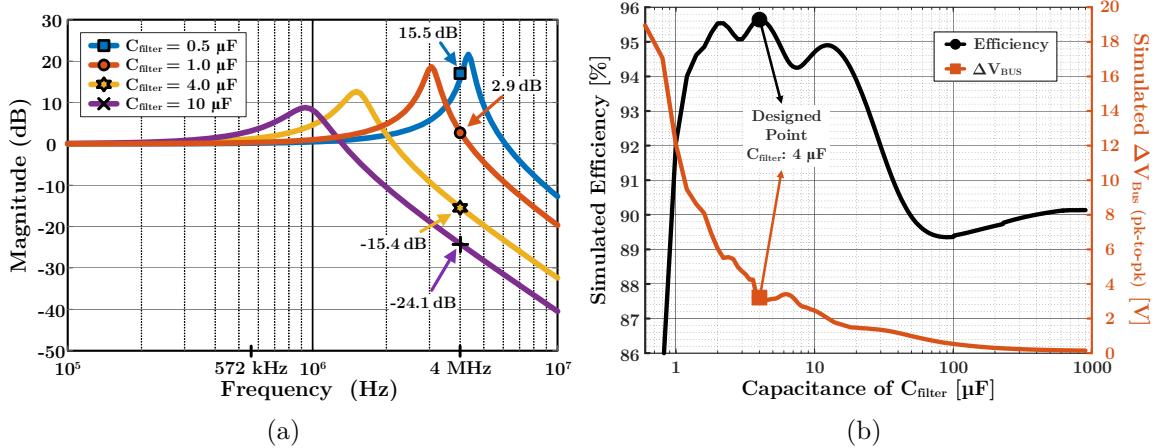


Figure 3.18: (a) Bode plot of the RLC circuit frequency response with different values of  $C_{\text{filter}}$ . The filter needs to reject the 4 MHz buck unit current ripple. (b) Simulated SC stage efficiency and virtual intermediate bus voltage ripple for varying values of  $C_{\text{filter}}$  at full load (780 A with liquid cooling).

$L_{\text{par}}$  contributes to filtering and larger values are beneficial, but layouts that deliberately increase  $L_{\text{par}}$  often increase resistance and require extra space. Here,  $L_{\text{par}}$  is determined by the practical value achieved in the system assembly.  $R_{\text{par}}$  is minimized to improve efficiency, and thus  $C_{\text{filter}}$  is the only design parameter for the filter. The cutoff frequency of the RLC filter is

$$f_o = \frac{1}{2\pi\sqrt{L_{\text{par}}C_{\text{filter}}}}. \quad (3.13)$$

The switches of the SC stage, interconnects between the SC stage, and PCB traces are all sources of parasitic inductance and resistance. For the vertical stacked LEGO-PoL converter, the calculated parasitic inductance is 2.7 nH and parasitic resistance is 6.1 mΩ. The buck switching frequency  $f_{\text{Buck}}$  is 1 MHz.

Figure 3.18a shows a Bode plot of the magnitude response of the RLC filter, considering the buck switched current as the input and the current  $i_{\text{SC}}$  as the output. The response is plotted for various values of  $C_{\text{filter}}$ . A small filter capacitance of  $0.5 \mu\text{F}$  amplifies the high frequency 4 MHz current, which can cause increased losses. As the

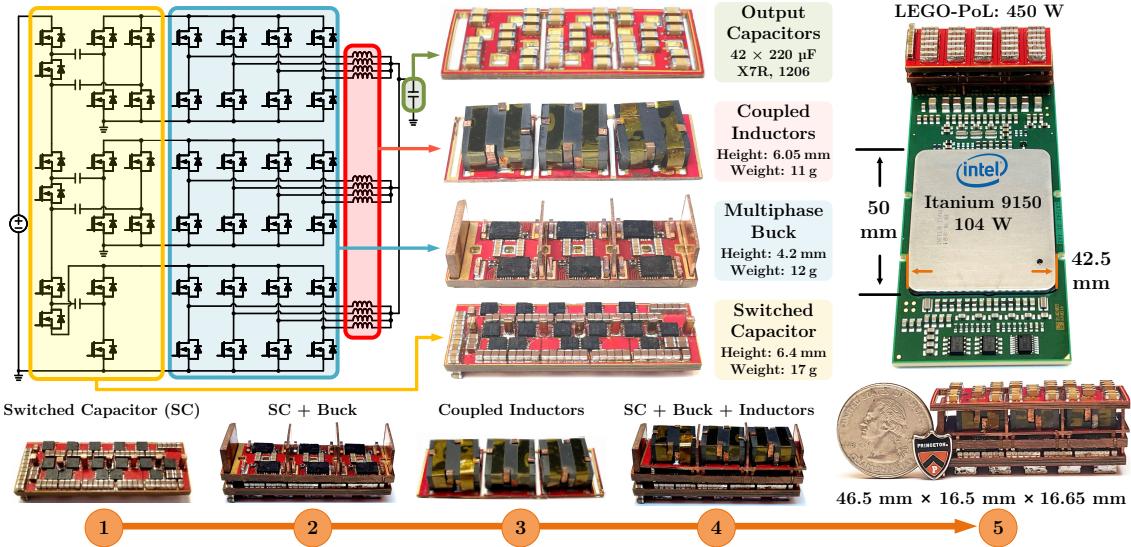


Figure 3.19: Assembly procedure for the vertical stacked LEGO-PoL converter. The SC stage and multiphase buck stage are implemented as two PCBs, vertically stacked on each other and connected with copper rod interconnects. The coupled inductors are placed on an interposer and stacked on top of the multiphase buck stage. The final power stage dimensions are  $46.5 \text{ mm} \times 16.5 \text{ mm} \times 16.65 \text{ mm}$ .

filter capacitance increases, the filter is able to adequately damp the current ringing.

Figure 3.18b shows the simulated efficiency and intermediate bus voltage ripple of the LEGO-PoL design, simulated and calculated with Powersim. The simulated efficiency of the switched-capacitor stage at full load has multiple resonant peaks.

As  $C_{\text{filter}}$  increases (in the range of hundreds of  $\mu\text{F}$ ), the two stages effectively become more and more decoupled. The architecture loses the benefits achieved from merged operation, namely soft charging of the flying capacitors, and the efficiency of the SC stage suffers as a result. This added charge sharing loss in addition to the larger filter capacitor size is detrimental to the system efficiency and density. To balance between this trade-off of charge sharing loss and achieving adequate filtering, sizing the filter capacitor to be roughly 5-15% of the value of the flying capacitors generally results in sufficient filtering while maintaining low charge sharing loss. In this design,  $C_{\text{filter}}$  is selected as  $4.0 \mu\text{F}$  to achieve a high efficiency (95.6%).

### 3.4.4 System Assembly

A vertical stacked LEGO-PoL converter is fabricated and tested. The input voltage range is from 40 V to 60 V, and the output voltage range is from 0.8 V to 1.5 V. Figure 3.19 shows the structure and assembly procedure of the prototype. Three submodules were used, as per the schematic in Fig. 3.12. The multiphase buck stage is stacked vertically on the SC stage and connected with vertical copper rod interconnects. The coupled inductors are assembled on the interposer board, which connects to the multiphase buck board.

Table 3.1 lists the key power stage components of this design. The switches in the SC units are implemented as silicon MOSFETs. The switches in the multiphase buck units are implemented as low voltage DrMOS devices. Each DrMOS device consists of two switches, in a half-bridge configuration, as well as the gate driving circuitry required for these two switches. Twelve DrMOS devices are used, three per submodule, to implement the 24 switches in the multiphase buck stage. The same type of ceramic capacitors were used for  $C_1 - C_5$ . Due to different bias voltages, the derated capacitance of each flying capacitor varies. For the filter capacitance,  $24 \times 0.22 \mu\text{F}$  0603 size capacitors per module are used and the effective  $C_{\text{filter}}$  is  $4.0 \mu\text{F}$  at 8 V bias voltage and 4 MHz effective frequency due to four-phase interleaving. The power stage has an area of  $46.5 \text{ mm} \times 16.5 \text{ mm} = 767 \text{ mm}^2$  and a height of 16.65 mm.

### 3.4.5 Experimental Verification

Figure 3.20 shows the experimental setup to characterize the performance of the vertical stacked LEGO-PoL converter. All of the necessary equipment is placed in a standard 1U server rack setup. Five Agilent 34401A digital multimeters are used to take automated measurements of the input voltage, input current, output voltage, output current, and DrMOS junction temperature. Rideon RSN-50 and Rideon RSC-1000 current shunts are used for input and output current measurement. A BK

Table 3.1: Bill-of-Materials for the Vertical Stacked LEGO-PoL Converter

Semiconductor Devices	Symbol	Part Number	
SC Stage Switches	$Q_1 - Q_5$ $Q_{S1} - Q_{S10}$	Infineon BSZ010NE2LS5	
Buck Stage Switches	$Q_{B1} - Q_{B12}$	Infineon TDA21472 DrMOS	
Capacitors	Bias Voltage	Quantity	Effective Size
C <sub>1</sub>	40 V	59 × 0805 X7R 50 V 4.7 μF	47.2 μF
C <sub>2</sub>	32 V	57 × 0805 X7R 50 V 4.7 μF	62.7 μF
C <sub>3</sub>	24 V	58 × 0805 X7R 50 V 4.7 μF	82.0 μF
C <sub>4</sub>	16 V	59 × 0805 X7R 50 V 4.7 μF	140 μF
C <sub>5</sub>	8 V	68 × 0805 X7R 50 V 4.7 μF	257 μF
C <sub>filter</sub>	8 V	24 × 0603 X7R 25 V 4.7 μF	4.0 μF

Precision 9117 dc power source and two electronic loads, a Chroma 63103A 240 A load and a Chroma 63203 600 A load, are used. Two 36 CFM fans are used for the air cooling. Liquid cooling with circulated mineral oil, flowing at a speed of 9 L/min, is used to further increase the output current to 780 A. The waveforms henceforth presented are captured under liquid cooling, with an output voltage of 1 V and output current of 780 A.

Figure 3.21a shows the measured waveforms of the SC stage at a 48 V input voltage, 1 V output voltage, and an output current of 780 A. The input voltage is shown on top, and the differential voltage across C<sub>2</sub> and C<sub>4</sub>, as well as the leftmost node voltage of C<sub>5</sub> (denoted  $V_{C5+}$  on the schematic of Fig. 3.12), are shown below the input voltage.

Figure 3.21b shows the waveforms of the intermediate bus voltages of each module at the same operating condition as above. The dc value of each of the three bus voltages is very close, further verifying the voltage balancing of the LEGO-PoL converter. Due to the different dc bias voltage of the flying capacitors, as listed in Table 3.1, each module has a different intermediate bus voltage ripple. Module #1 has the highest



Figure 3.20: Picture of the experimental setup. Digital multimeters are used to take automated measurements of the input and output power via the BenchVue software. An interface PCB is used to connect the device under test to the dc power source and the electronic loads, as well as house shunts for measuring the input and output current.

voltage ripple due to the higher bias voltage resulting in lower effective capacitance for  $C_1$  and  $C_2$ , and module #3 has the lowest voltage ripple.

Figure 3.22a shows the switch node voltages of each of the four phases of the second buck module. The envelope of the switch nodes is equal to  $V_{BUS2}$ , which is the input voltage of the buck unit. The four phases are interleaved, with a duty cycle of 15.7% at 1 V/780 A output. The switching frequency is 1 MHz. Figure 3.22b shows

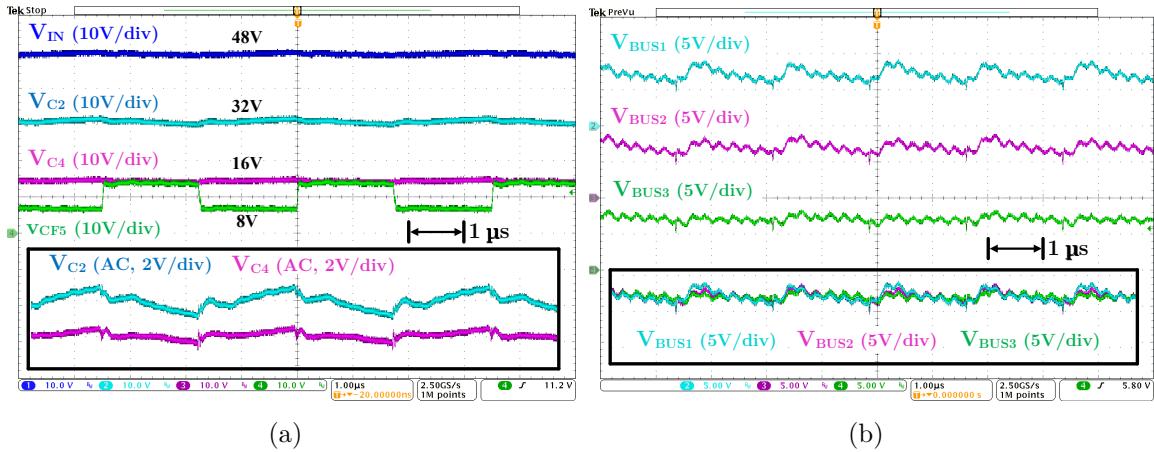


Figure 3.21: (a) Measured waveforms of the SC stage at 48 V input, 1 V/780 A output. The series-stacked SC modules evenly split 48 V input voltage into three 16 V voltage domains. C<sub>2</sub> has a higher voltage ripple than C<sub>4</sub> due to higher dc bias voltage. (b) Measured waveforms of three bus voltages at 48 V input, 1 V/780 A output. The three virtual intermediate bus voltages are automatically balanced.

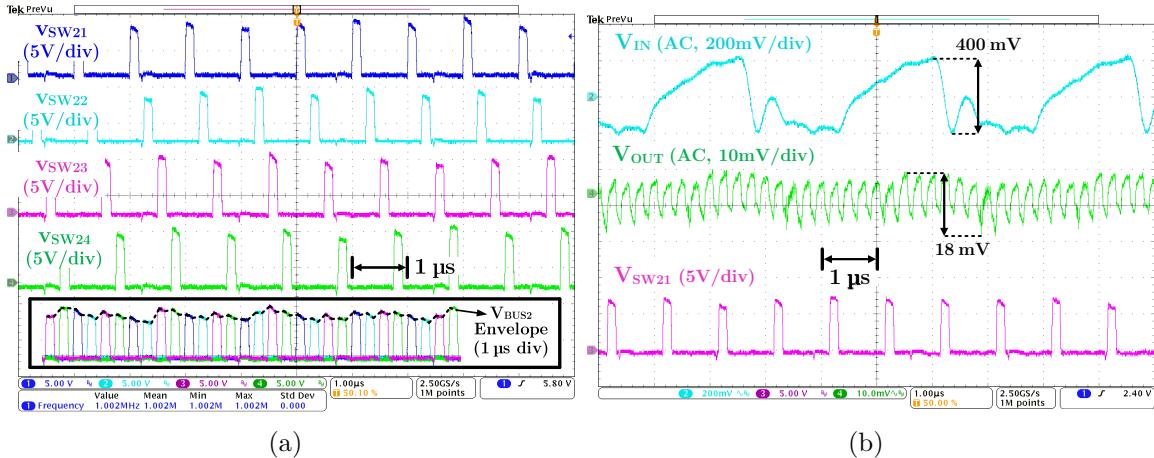


Figure 3.22: (a) Measured waveforms of switch nodes of a four-phase buck module at 48 V input, 1 V/780 A output. The four phases are interleaved. The envelope of the switch nodes is equal to the virtual intermediate bus voltage. (b) Measured voltage ripples at 48 V input, 1 V/780 A output.

the input and output voltage ripple waveforms at 48 V input and 1 V/780 A output. The steady state output voltage ripple is 18 mV with 5.75 mF output capacitance. The input capacitor voltage ripple is 400 mV. The frequency of the output voltage ripple is 4 MHz, as a result of four-phase interleaving, which effectively multiplies the frequency of input and output voltage and current ripples by the number of phases.

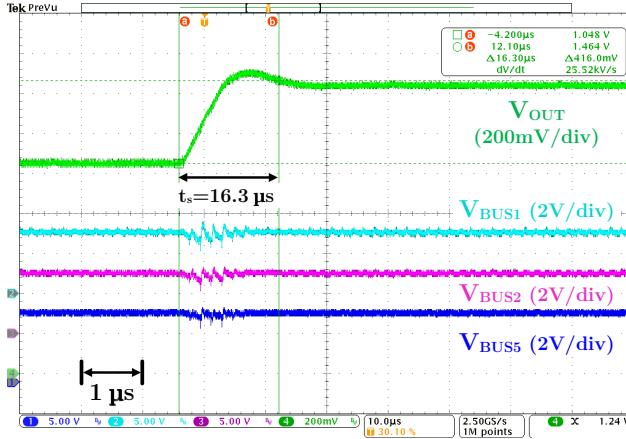
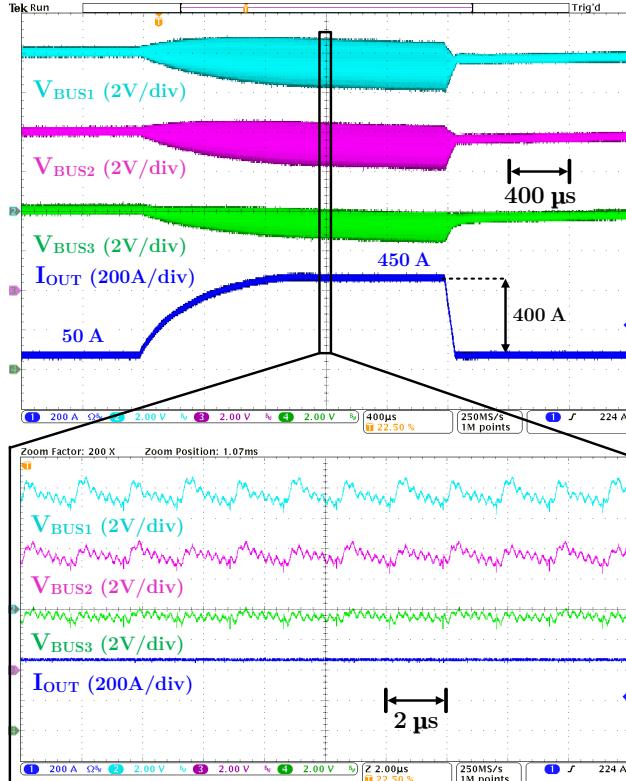


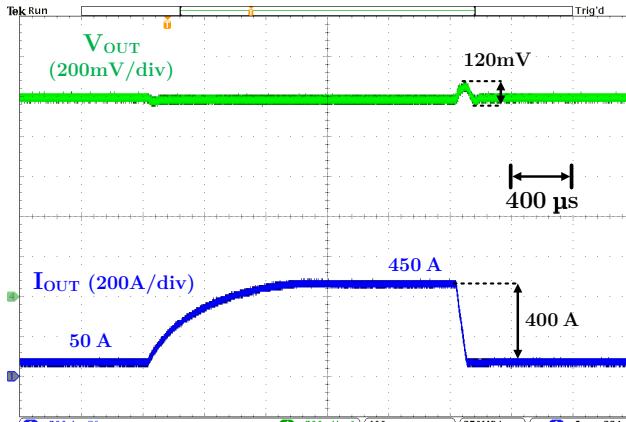
Figure 3.23: Measured transient waveforms with an open-loop buck duty ratio step from 15% to 20% at 150 A. The output voltage steps from 1.048 V to 1.464 V within  $16.3 \mu s$ .

To evaluate the dynamic performance of the vertical stacked LEGO-PoL converter, both open-loop and simple closed-loop tests are conducted. Figure 3.23 shows the output voltage and virtual intermediate bus voltage waveforms in response to a buck switch duty ratio change from 15% to 20% at an output load current of 150 A. The output voltage settles to within 2% of its expected value in  $16.3 \mu s$ . The virtual intermediate bus voltages remain stable, with increased ripple during the transition as the output capacitors are being charged to the new output voltage level. The SC stage of the LEGO-PoL converter operates as a dc transformer like a traditional hybrid SC stage.

Figure 3.24 shows a closed-loop transient test for a 50% load step. A classic voltage-mode feedback PI controller is used for this experiment [70]. The three virtual intermediate bus voltages and output voltage in response to an output current load step between 50 A and 450 A are measured. The merged two-stage operation maintains stable intermediate bus voltage without a large decoupling capacitor, with expected ripple due to the increase in output load current. Due to the limited controller bandwidth, a 120 mV peak-to-peak voltage excursion is observed during the transient. Advanced control methods, such as current mode control, can significantly



(a)



(b)

Figure 3.24: Measured transient waveforms with a load current step between 50 A and 450 A (50% load step of the full load output current). (a) Three intermediate bus voltages. (b) Output voltage. A classic voltage-mode digital PI feedback loop was implemented in a microcontroller (TMS320F28388D) for this test. The total output capacitance is 5.75 mF.

improve the transient performance [71]. Demonstration of extreme control performance of the LEGO-PoL architecture is beyond the scope of this dissertation.

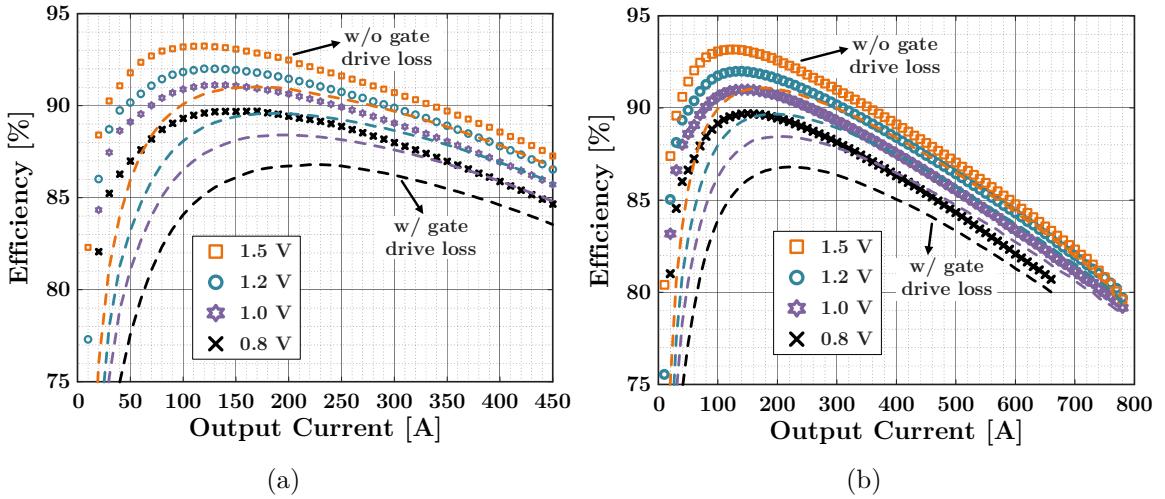


Figure 3.25: Measured efficiency at 48 V input and different output voltages with (a) air cooling and (b) liquid cooling. The efficiency is shown with and without gate drive loss. The DrMOS junction temperature is kept below 100°C throughout its operation.

### 3.4.6 Converter Performance

Figure 3.25a and 3.25b summarize the system efficiency of the vertical stacked LEGO-PoL converter with air cooling and liquid cooling. Measurements are taken at four different output voltage conditions: 0.8 V, 1.0 V, 1.2 V, and 1.5 V. The input and output voltages are measured right at the input and output capacitors. The measurement data for the 0.8 V condition with liquid cooling stops at 660 A due to the voltage drop between the converter output and electronic load. The data for the other three conditions are provided across the full operating range in 10 A intervals. In all conditions, the SC switching frequency is 286 kHz and the buck switching frequency is 1 MHz. The converter achieves a peak efficiency of 88.4% at  $V_{\text{out}} = 1.0$  V and  $I_{\text{out}} = 160$  A including the gate drive loss. The gate drive loss of the prototype is measured as 5.02 W (switched-capacitor stage: 2.02 W, buck stage: 3 W). The maximum power rating of the converter in air cooling is 450 A with the DrMOS junction temperature kept below 100 °C, and the efficiency is 84.8%. At 780 A with liquid

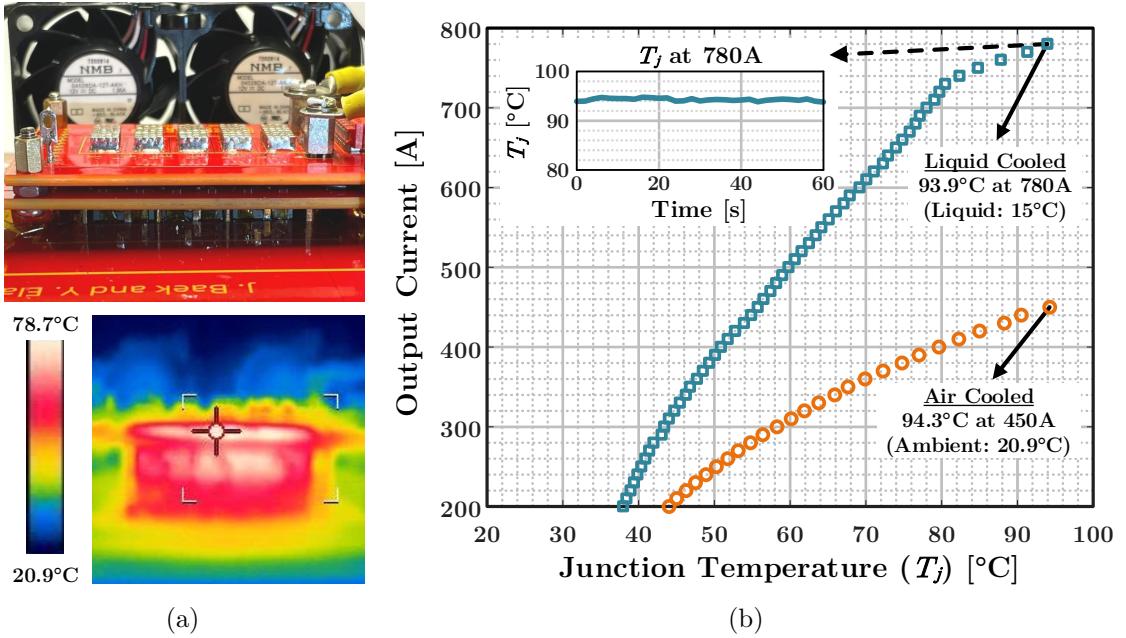


Figure 3.26: (a) Thermal image of the vertical stacked LEGO-PoL converter. The thermal image was measured at 20.9°C ambient temperature with two 36 CFM fans. (b) Measured DrMOS junction temperature (from  $T_j$  sensing pin) with air cooling and liquid cooling. The junction temperature is stable at 780 A output current with liquid cooling.

cooling, the efficiency of the converter is 78.7% at  $V_{\text{out}} = 1.0$  V including gate drive loss.

With air cooling, the maximum output current of the system is 450 A. Figure 3.26a shows a thermal image of the converter at  $V_{\text{out}} = 1.5$  V and  $I_{\text{out}} = 450$  A. Two 36 CFM fans are used, and the PCBs reach a temperature of 78.7°C. Figure 3.26b shows a graph of the DrMOS junction temperature (using the built-in temperature sensing pin) for both the air cooled and liquid cooled operation at  $V_{\text{out}} = 1.5$  V. The junction temperature reaches 94.3°C at  $I_{\text{out}} = 450$  A. The junction temperature of the DrMOS reaches 93.9°C at  $I_{\text{out}} = 780$  A in liquid cooling.

A detailed theoretical loss breakdown is provided in Fig. 3.27 for the 1.0 V and 1.5 V output voltage conditions. The loss breakdown takes into account the experimentally measured duty ratio of the buck stage and junction temperature of DrMOS in Fig. 3.26b. Losses from the SC stage include loss from the MOSFETs, the flying

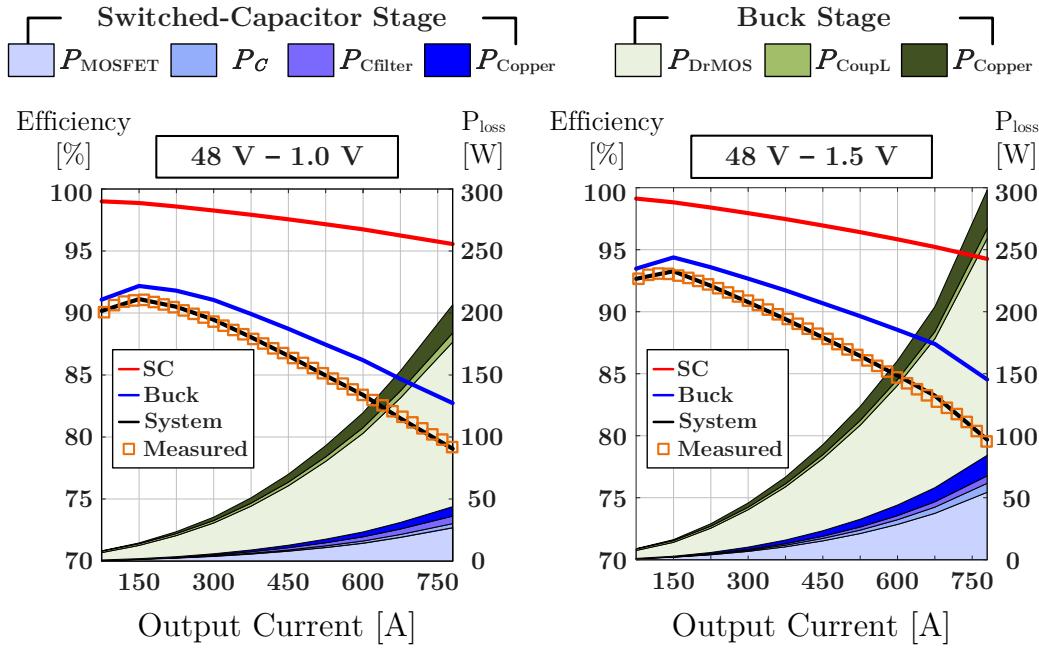


Figure 3.27: Loss breakdown and calculated efficiencies of the SC stage, buck stage, and total system at 1.0 V and 1.5 V output voltage conditions.  $P_{\text{MOSFET}}$ ,  $P_C$ ,  $P_{C_{\text{filter}}}$ , and  $P_{\text{Copper}}$  are the loss of MOSFETs, flying capacitors, filter capacitors, and copper traces including connectors and PCB traces in the SC stage.  $P_{\text{DrMOS}}$ ,  $P_{\text{CoupL}}$ , and  $P_{\text{Copper}}$  are the loss of DrMOS, coupled inductors, and copper traces in the buck stage.

capacitors, the filter capacitors, and the copper traces. Losses from the buck stage include loss from the DrMOS, the coupled inductor (both core loss and conduction loss), and the copper traces. The DrMOS switching and conduction loss dominates the loss of the overall system due to its high switching frequency operation and high output current. The SC stage maintains high efficiency (above 95.5%) throughout the entire load range for the 1 V output voltage condition. The overall system efficiency curve mirrors the shape of the buck efficiency curve, with a larger slope as the load current increases due to increased conduction loss. The converter achieves peak efficiency at around 20% of its fully rated power for the liquid cooling case, dominated by the efficiency curves of the buck stage.

Table 3.2: Summary of Vertical Stacked LEGO-PoL Converter Performance

Year	Note	At Peak Efficiency			At Full Load Efficiency				Switching Frequency <sup>‡</sup>
		Output Current	Efficiency	Power Density <sup>†</sup>	Output Current	Efficiency	Power Density <sup>†</sup>	Area Density	
2022	Vertical Stacked LEGO-PoL*	190 A	88.4%	124 W/in <sup>3</sup>	450 A	84.8%	294 W/in <sup>3</sup>	0.3 A/mm <sup>2</sup>	1000 kHz

\* Numbers presented include gate drive losses and are presented for air cooling only.

† The power density is calculated with the box volume (maximum length × width × height) of the prototype, including the gate drive circuitry.

‡ The switching frequency of the voltage regulation stage, which strongly influences the transient dynamics of the voltage regulator.

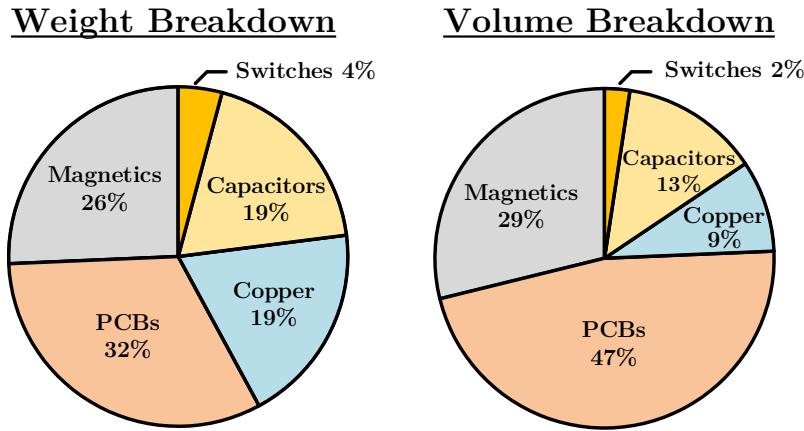


Figure 3.28: Weight and volume breakdown of the vertical stacked LEGO-PoL prototype. The total weight of the prototype is 40 g, and the total component volume is 0.52 in<sup>3</sup>. The switches only contribute to 4% of the weight and 2% of the volume; capacitors and magnetics each occupy about one quarter of the volume, and the PCBs and copper contribute about one-half of the weight and volume.

### 3.4.7 Discussion

Table 3.2 summarizes the performance of the vertical stacked LEGO-PoL prototype. The numbers are presented for air cooling, and include the gate drive size and losses. When including the gate drive size in the vertical stacked LEGO-PoL prototype, as discussed in Section 3.4.1, the total area increases from 767 mm<sup>2</sup> to 1510 mm<sup>2</sup>. This greatly hinders the current area density and power density of the prototype. The area density is 0.3 A/mm<sup>2</sup> and the power density at 1 V and 450 A is 294 W/in<sup>3</sup>.

The presented prototype achieves its peak efficiency at around 20% of its thermal design power (TDP) under liquid cooling and 30% under air cooling. Depending on

the application, different microprocessors (e.g., CPUs, GPUs, TPUs) need performance optimized at different fractions of the TDP, leading to different design trade-offs. Different priorities among efficiency, density, and transient performance also lead to different tradeoffs. Challenges and pathways to achieving over  $4.5 \text{ W/mm}^2$  area density – matching that of a state-of-the-art of the silicon core – while maintaining a high efficiency across the entire operation range, include:

1. Performance of the available DrMOS devices. The devices used limit current area density, efficiency, and switching frequency. Better low-voltage power devices, whether based on silicon or wide-bandgap semiconductors, are expected to be instrumental in overcoming all three of these limitations.
2. Reducing the height of the LEGO-PoL prototype. The height in this prototype is limited by the vertical coupled inductors and capacitors. Switching at a higher frequency, enabled by better switches, optimizing the magnetics design with a priority on reducing thickness, and more advanced capacitor technologies can further reduce the height and weight of the system.
3. The thermal performance of the converter. The current throughput of the prototype is limited by the thermal rating of the switches. Better cooling technology, and semiconductor devices that can work at higher temperatures (such as GaN devices), are promising techniques to improve the power density and improve the system efficiency at full load.
4. Reducing the volume of the passive components. In the prototype, passive components (capacitors and magnetics) contribute an order of magnitude more volume and weight than the semiconductor devices. As shown in Fig. 3.28, semiconductor devices only contribute 4% of the system weight and 2% of the system volume. Devices that can efficiently switch at a higher frequency can further reduce the passive component sizes.

5. Packaging techniques to interconnect the circuit elements and route the high current. Printed circuit boards (PCBs) and copper interconnects occupy a large percentage of the system weight and volume. Advanced packaging techniques are needed to further reduce the size and improve the current density.

After analysis of the performance of the vertical stacked LEGO-PoL prototype, tall height and poor density remain the major bottlenecks hindering in-package vertical power delivery. The next section focuses on work done to develop a new prototype – Mini-LEGO – that fully exploits the potential of the LEGO-PoL architecture for extreme power density, by trading off efficiency to achieve compact size.

### **3.5 Mini-LEGO Design and Optimization**

As detailed in the previous section, the LEGO-PoL architecture, and its preliminary vertical stacked implementation, performs vertical power delivery for 48-V-to-1-V, achieving a current density of  $1 \text{ A/mm}^2$  and a power density of  $1000 \text{ W/in}^3$  for 48-V-to-1-V conversion with liquid cooling and without including the gate drive circuitry. When including the gate drive circuitry and only using air cooling, the density numbers drop to  $0.3 \text{ A/mm}^2$  and  $294 \text{ W/in}^3$ . Its height is 16.65 mm, which is too tall to enable in-packaging vertical power delivery. Figure 3.29 demonstrates how in-packaging vertical power delivery is performed with a vertical stacked LEGO-PoL converter. By co-packaging the VRM with an LGA socket, it can be placed directly underneath the CPU and leverage the benefits of vertical power delivery.

This section presents a new 48-V VRM design – Mini-LEGO – which is significantly smaller and thinner than the vertical stacked LEGO-PoL implementation. A side-by-side comparison of the power stages of both converters is shown in Figure 3.30. The significantly reduced size is enabled by (1) improved device implementation, (2)

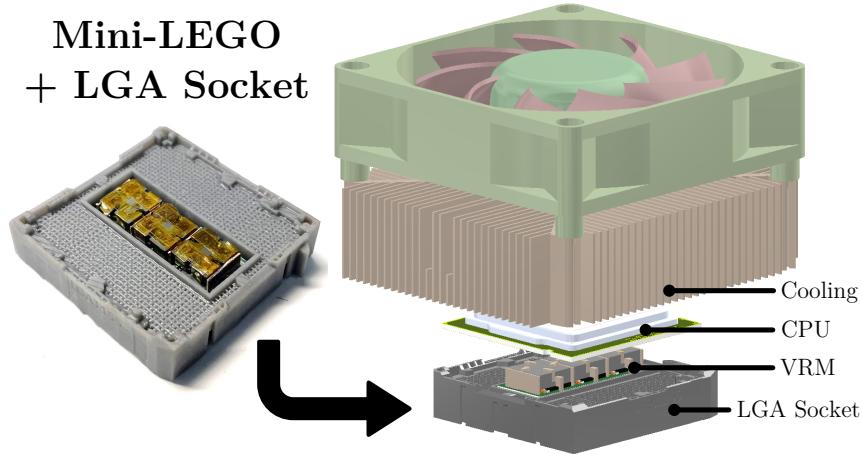


Figure 3.29: VRM placed within a modified land-grid array (LGA) socket (Intel LGA1155) for CPUs. Co-packaging the VRM inside the LGA socket can leverage the cooling resources of the CPU and perform point-of-load power delivery. The VRM must have small enough area and thin enough height.



Figure 3.30: Side-by-side comparison of the Mini-LEGO prototype presented in this section (2024), the vertical stacked LEGO-PoL prototype (2022), and a United States quarter. The volume of the 240 A Mini-LEGO is 22.5% of the 450 A vertical stacked LEGO-PoL. The height is reduced from 16.65 mm to 8.4 mm, and the total area (power stage and gate drive) is reduced from 1510 mm<sup>2</sup> to 336 mm<sup>2</sup>.

optimized gate drive circuitry, (3) optimized magnetics, (4) higher switching frequency, and (5) compact packaging.

### 3.5.1 Switched-Capacitor Stage and Gate Drive Design

The primary design targets for the Mini-LEGO converter are high power density and low height, which guide the design philosophy and component selection. Figure 3.31 shows how each switch of the LEGO-PoL topology is implemented in Mini-

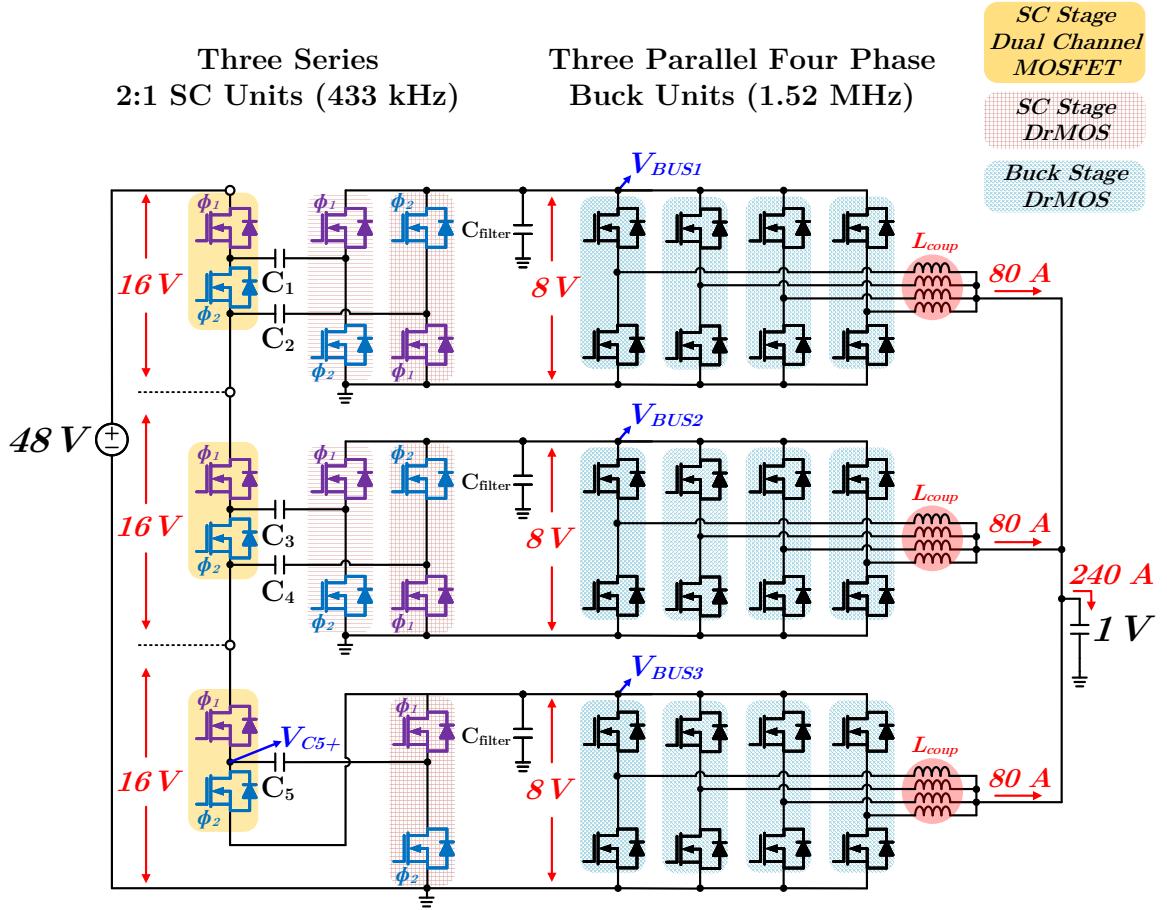


Figure 3.31: Circuit topology and implementation of the 48-V-to-1-V, 240-A Mini-LEGO design. Each buck phase delivers 20 A of peak current. The floating switches in the SC stage are implemented as dual-channel silicon MOSFETs, and the SC synchronous rectifier switches as well as the buck stage switches are implemented as DrMOS (integrated driver and two power MOSFETs). Three dual-channel MOSFETs, five rectification DrMOS devices, and 12 buck DrMOS devices are used, totaling 20 devices by discrete component count.

LEGO. Figure 3.32a shows the top side layout of the SC stage, where all switches are placed. Instead of implementing the ten ground-referenced synchronous rectifier switches as discrete MOSFETs with separate gate driver ICs, as was done in the previous vertical stacked LEGO-PoL implementation, Mini-LEGO uses DrMOS devices, which comprise of an integrated driver and two power MOSFETs (highlighted red in Figure 3.31). The footprint of the DrMOS devices chosen (onsemi FDMF3039) is 3.5 mm × 4.5 mm. For the floating switches, dual-channel symmetric

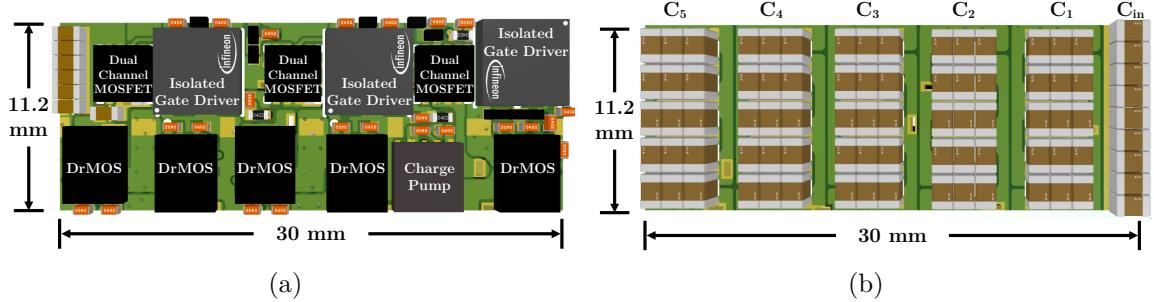


Figure 3.32: (a) PCB layout of the top side of the SC stage. The power stage and all gate-drive circuitry is included within an area of 336 mm<sup>2</sup>. (b) PCB layout of the bottom side of the SC stage, containing the flying capacitors and input capacitors.

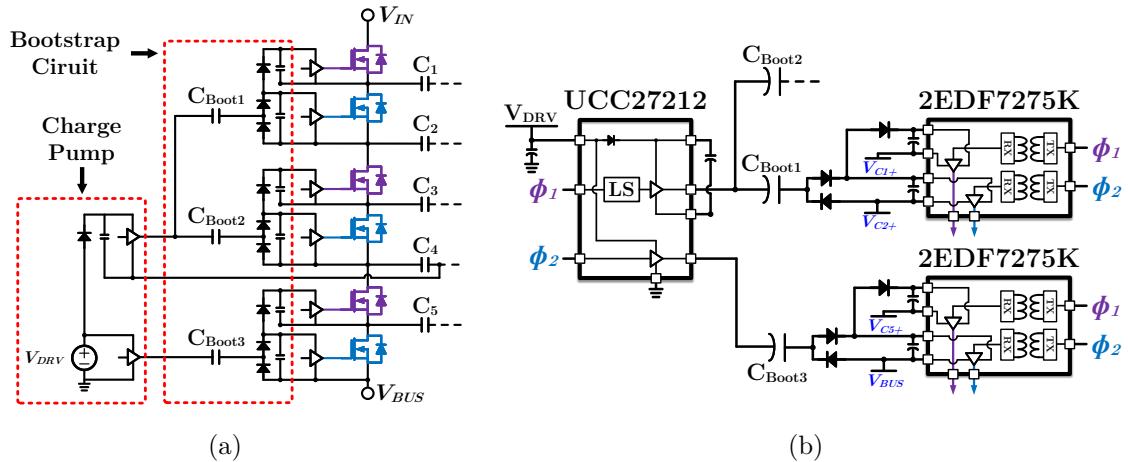


Figure 3.33: (a) Circuit schematic of the gate drive for the floating switches of the SC stage. (b) Implementation of the charge pump, bootstrapping circuit, and gate drivers. An isolated gate driver IC (2EDF7275K from Infineon) is used to drive each of the floating dual-channel MOSFETs.

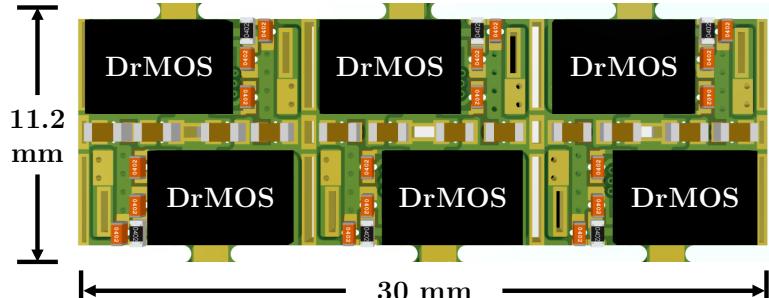
MOSFETs (onsemi NTTFD2D8N03P1E), configured as half-bridges, are used. Two power MOSFETs are integrated in one package within the standard footprint area of 3.3 mm × 3.3 mm. The gate drive circuitry for the floating switches is placed in the remaining area.

The bottom side layout of the SC stage is shown in Fig. 3.32b. Each of the five flying capacitors consists of fifteen 50 V, 4.7  $\mu$ F, 0805 MLCCs. A row of input capacitors is placed on the bottom side as well. The overall dimensions of the power stage and gate drive circuitry are 30 mm × 11.2 mm, resulting in an area of 336 mm<sup>2</sup>.

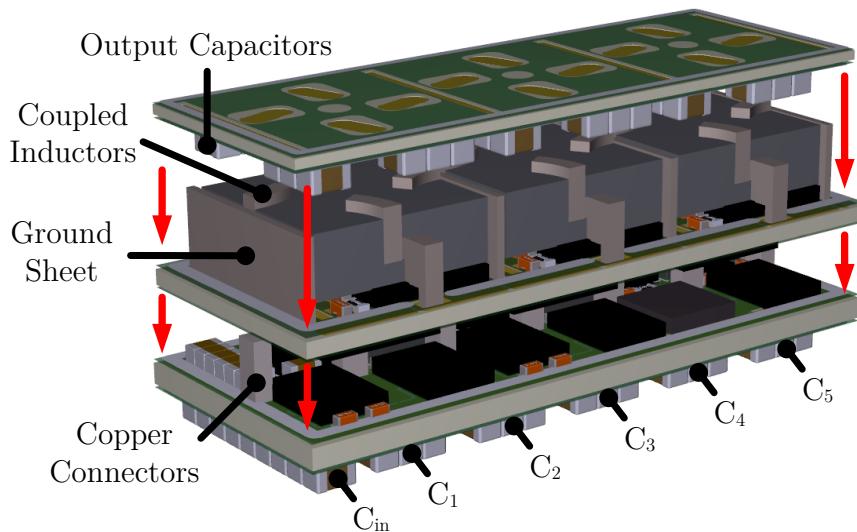
Figure 3.33a shows the power stage and gate drive circuit implementation for the SC stage floating switches. The gate drive circuit implementation is highlighted specifically in Fig. 3.33b. Similarly to the previous LEGO-PoL prototype, a bootstrapping circuit is used to provide a power supply to the floating gate driver ICs. The gate drive circuit comprises a charge pump implemented with a half-bridge gate driver IC (4 mm × 4 mm) and three isolated gate driver ICs (5 mm × 5 mm), and is highly modular and scalable. Since an isolated gate driver IC (Infineon 2EDF7275K) is used, a separate level shifter is not needed for the PWM control signals. The isolated gate driver ICs are placed directly adjacent to the dual channel MOSFETs that they drive. The charge pump is placed next to the ground referenced DrMOS devices, and close to  $C_4$ , as  $V_{SS}$  for the high-side channel of the charge pump is  $V_{C4-}$  (shown in Figure 3.33a). The gate drive circuitry occupies approximately 111 mm<sup>2</sup> of the area on the SC board, roughly 1/3 of the overall area.

### 3.5.2 System Assembly

Figure 3.34a shows the layout of the multiphase buck stage, which has the same area as the SC stage. The top and bottom side are identical in terms of component placement. The board is divided into three submodules. Four DrMOS devices (Reed Semiconductor RS86900), capable of handling up to 45 A, are used per submodule. Copper rods from the SC stage vertically deliver power to the multiphase buck stage. Four pads are present per submodule to connect to the windings of the vertical coupled inductor, which sits directly on top of the DrMOS devices. This allows for an interposer-less connection between the inductors and the multiphase buck board, which further reduces the system height compared to the original vertical stacked LEGO-PoL design which uses an interposer. The interstage filter capacitors are placed between the vertical copper connectors, resulting in a short parasitic in-



(a)



(b)

Figure 3.34: (a) PCB layout of the top side of the multiphase buck board. The bottom side has identical component placement. Four pads are present on the top side to connect to the four-phase coupled inductor. (b) Altium 3D rendering of multi-board assembly process.

ductance loop between the two stages. Eight 0603 X7R 25 V MLCCs are used per submodule, and the de-rated filter capacitance value for each submodule is  $1.03 \mu\text{F}$ .

Figure 3.34b shows a 3D rendering of the full Mini-LEGO system assembly. Copper sheet connectors are used for the current return path. The full assembly uses four copper ground sheets, with three coupled inductors in between them. Design of the coupled inductor for Mini-LEGO is discussed in Section 4.5. The output capacitors are placed vertically above the coupled inductors on a separate board, embedding

Table 3.3: Bill-of-Materials for the Mini-LEGO Converter

Semiconductor Devices	Symbol	Part Number	
SC Stage Floating Switches	$Q_{D1} - Q_{D3}$	onsemi NTTFD2D8N03P1E (30 V)	
SC Stage Synchronous Rectifiers	$Q_{SR1} - Q_{SR5}$	onsemi FDMF3039 DrMOS (30 A)	
Buck Stage Switches	$Q_{B1} - Q_{B12}$	Reed Semiconductor RS86900 DrMOS	
Isolated Gate Driver	-	Infineon 2EDF7275K	
Charge Pump	-	Texas Instruments UCC27212	
Capacitors	Bias Voltage	Quantity	Effective Size
C <sub>1</sub>	40 V	16 × 0805 X7R 50 V 4.7 $\mu$ F	12.8 $\mu$ F
C <sub>2</sub>	32 V	15 × 0805 X7R 50 V 4.7 $\mu$ F	15.8 $\mu$ F
C <sub>3</sub>	24 V	15 × 0805 X7R 50 V 4.7 $\mu$ F	21.5 $\mu$ F
C <sub>4</sub>	16 V	15 × 0805 X7R 50 V 4.7 $\mu$ F	35.6 $\mu$ F
C <sub>5</sub>	8 V	15 × 0805 X7R 50 V 4.7 $\mu$ F	56.8 $\mu$ F
C <sub>filter</sub>	8 V	1 × 0603 X7R 25 V 1 $\mu$ F 4 × 0603 X7R 25 V 100 nF 3 × 0603 X7R 25 V 22 nF	1.03 $\mu$ F

them within the overall converter package. The key component specifications are summarized in Table 3.3.

### 3.5.3 Experimental Verification

The Mini-LEGO prototype is assembled and tested at an input voltage of 48 V up to a maximum output current of 240 A. The assembly procedure is shown in detail in pictured in Figure 3.35, along with an overall system height breakdown and a comparison to the vertical stacked LEGO-PoL prototype in Section 3.4. The Mini-LEGO converter is mounted on an output and control motherboard that interfaces with the input power source, electronic loads, and the microcontroller, as shown in Figure 3.36. The same test bench in Figure 3.20 is used for testing Mini-LEGO.

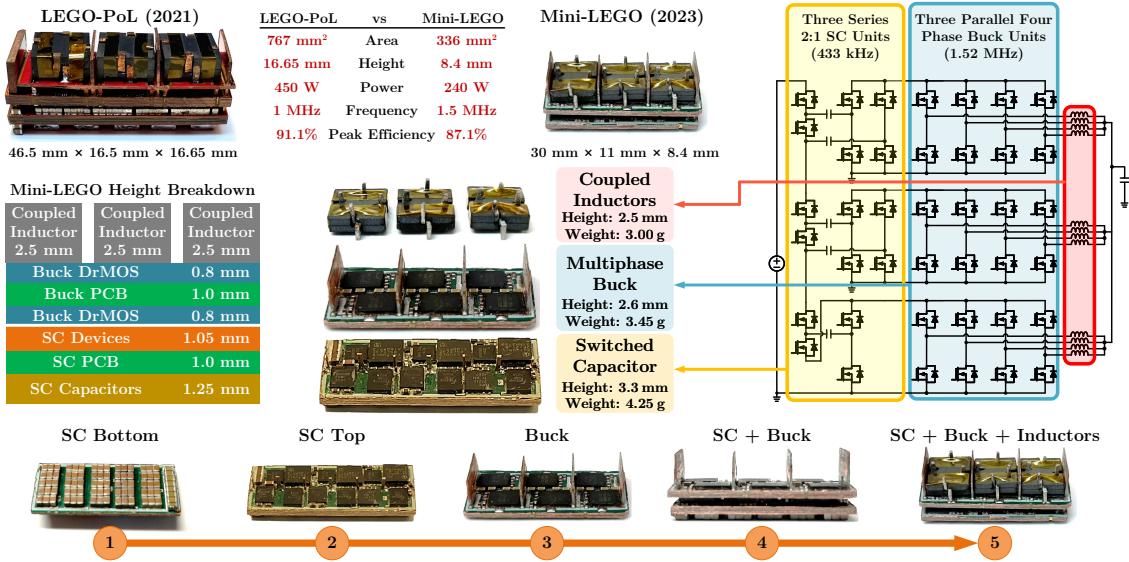


Figure 3.35: Assembly procedure of the Mini-LEGO converter (bottom); simplified schematic highlighting the SC stage, buck stage, and coupled inductors (right); zoomed-in images of each stage and inductors (middle); height breakdown of the Mini-LEGO prototype (left); comparison between the Mini-LEGO converter and the vertical stacked LEGO-PoL prototype (top). The power stage area of the Mini-LEGO prototype is  $30 \text{ mm} \times 11.2 \text{ mm} = 336 \text{ mm}^2$ . The height of the prototype is 8.4 mm. The current density is  $0.71 \text{ A/mm}^2$  at 240 A and the power density is  $1390 \text{ W/in}^3$  at 1 V and 240 A.

Figure 3.37a shows the key waveforms of the SC stage at an output voltage of 1 V and an output current of 240 A. The flying capacitors  $C_1 - C_5$  charge up to 40 V, 32 V, 24 V, 16 V, and 8 V, respectively. The ac coupled waveforms of the voltage across  $C_2$  and  $C_4$  show that, since  $C_2$  is biased at a higher dc voltage, the lower effective capacitance results in a higher ripple. The triangular shape of the voltage ripple show that the capacitors are being soft-charged by the coupled inductors in the multiphase buck stage.

The SC stage outputs three virtual intermediate bus voltages that are automatically balanced to a dc voltage level of 8 V, as can be seen in Fig. 3.37b.  $V_{\text{BUS}1}$  has the highest ripple voltage as  $C_1$  has the lowest effective capacitance. At the full load current of 240 A, the peak-to-peak ripple voltage is 2.4 V. The ripple frequency of

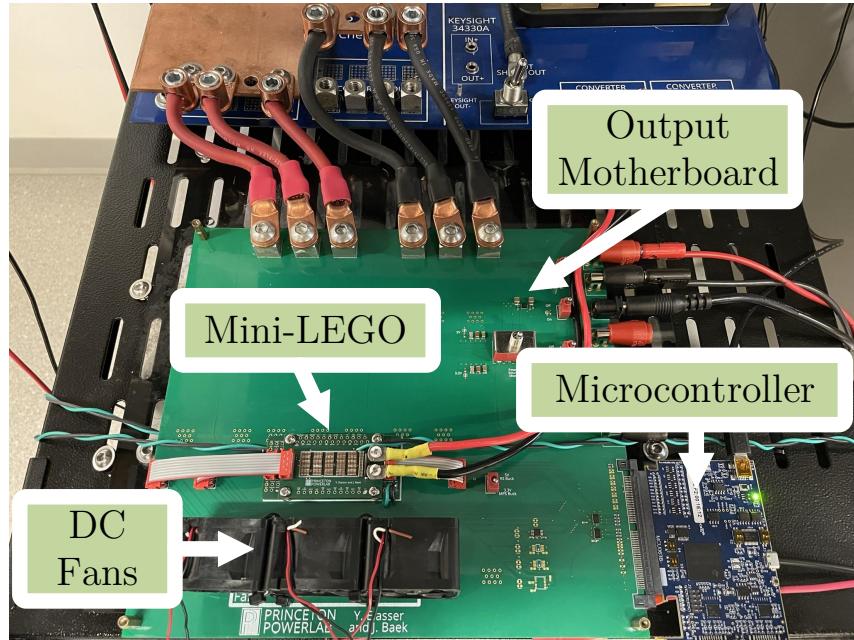


Figure 3.36: Picture of the Mini-LEGO converter assembled on to the output and control motherboard. This board houses the control circuitry and microcontroller, as well as routing the input power to the converter and output power to the electronic loads. Forced air cooling is used, with three 36 CFM dc fans placed on the motherboard as well.

the virtual intermediate bus voltages is 865.8 kHz, twice the switching frequency of the SC stage (432.9 kHz).

Figure 3.38a shows the four switch node voltages from the second multiphase buck submodule. Each phase switches at 1.515 MHz. The four phases are interleaved, with a  $90^\circ$  phase shift between each of the phases. The envelope of the switch node voltages approximately follows  $V_{BUS2}$ , which is the input voltage for the second multiphase buck submodule.

The same transient tests that were conducted for the vertical stacked LEGO-PoL converter were repeated for Mini-LEGO. The first, shown in Fig. 3.38b, was an open-loop duty cycle transient, where the duty cycle of the twelve PWM signals of the multiphase buck stage were stepped from 15% to 20%. The output voltage settles to its new voltage level within 12  $\mu$ s. During the transient, the ripple on the virtual intermediate bus voltages increase as the output capacitors are being charged. The

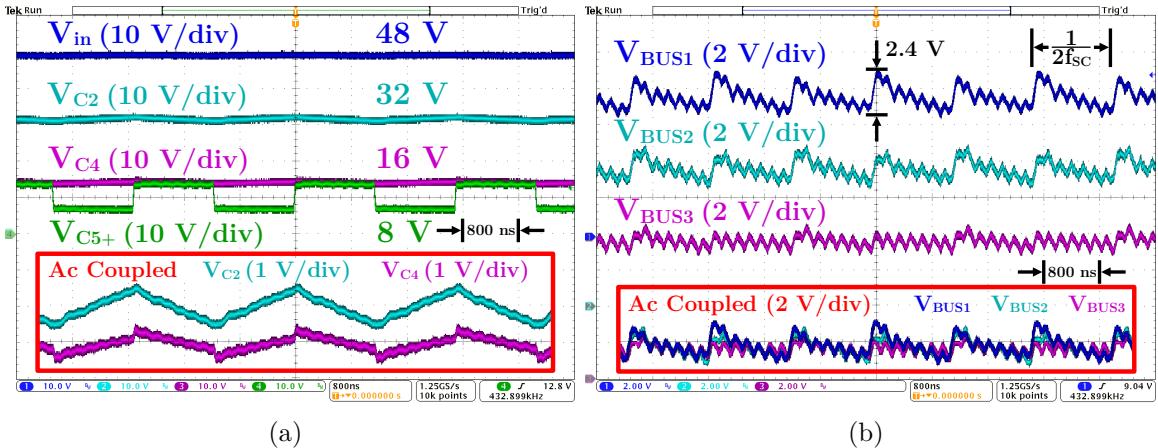


Figure 3.37: (a) Measured waveforms of the input voltage, differential voltages across  $C_2$  and  $C_4$ , and switch node voltage  $V_{C5+}$  (labelled on Fig. 3.31) during 48 V to 1 V operation at an output current of 240 A. The SC stage is switching at 432.9 kHz. The ac coupled waveforms of  $V_{C2}$  and  $V_{C4}$  highlight that the flying capacitors are being soft-charged by the inductor current in the multiphase buck stage. (b) Measured waveforms of the three virtual intermediate bus voltages during 48 V to 1 V operation at an output current of 240 A.  $V_{BUS1}$  has the highest peak-to-peak voltage ripple at 2.4 V, since flying capacitors  $C_1$  and  $C_2$  have the lowest effective capacitance. The ripple frequency of the intermediate bus voltage is equal to twice the switching frequency of the SC stage (432.9 kHz). All three intermediate bus voltages are balanced at 8 V.

speed at which the output voltage changes to its new level depends on the output  $LC$  filter. Using a coupled inductor greatly reduces the effective inductance seen during a transient as compared to a discrete inductor with the same steady-state ripple current.

A voltage-mode control method was implemented using a TMS320F28388D microcontroller to test the system under closed-loop operation. While demonstrating transient performance in response to an extreme load current transient ( $\geq 1 \text{ A/ns}$ ) is beyond the scope of this dissertation, a load current transient from 50 A to 200 A to 50 A (a jump of 150 A, equal to 62.5% of the full load current) was performed. Figure 3.39a shows the intermediate bus voltages, which remain stable, with increased ripple as the load current increases. Figure 3.39b shows the output voltage, which exhibits a 100 mV voltage spike as the load current steps down at a slew rate of 5 A/ $\mu\text{s}$ .

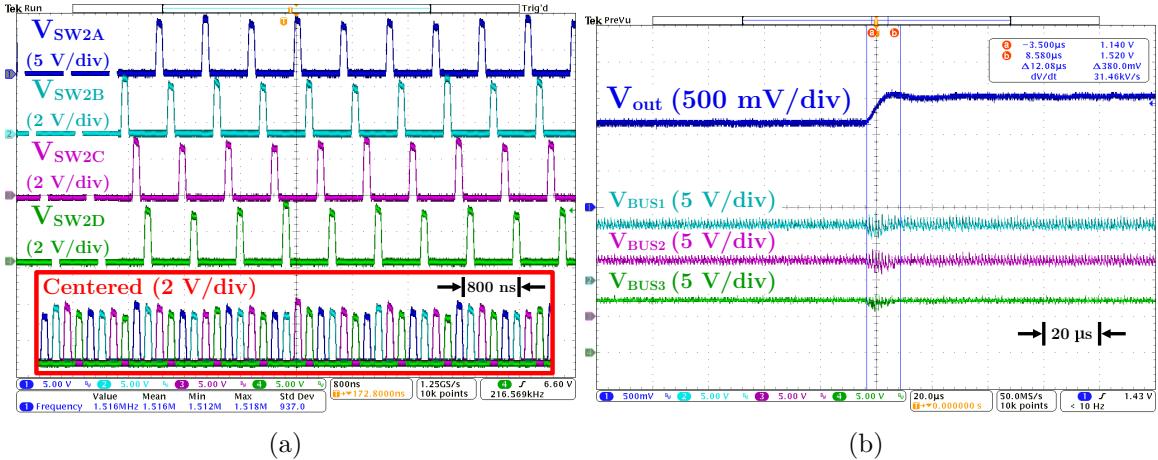


Figure 3.38: (a) Measured waveforms of the switch node voltages in the second submodule of the multiphase buck stage ( $f_s = 1.515$  MHz) during 48 V to 1 V operation at an output current of 240 A. The input voltage of the second submodule of the multiphase buck stage is equal to  $V_{BUS2}$ . (b) Measured waveforms of the output voltage and three virtual intermediate bus voltages in response to an open-loop duty cycle transient from 15% to 20% during 48 V to 1 V operation at an output current of 120 A. The output voltage changes from 1.14 V to within 2% of the new output voltage of 1.5 V within 12  $\mu$ s. The output capacitance is 2.5 mF.

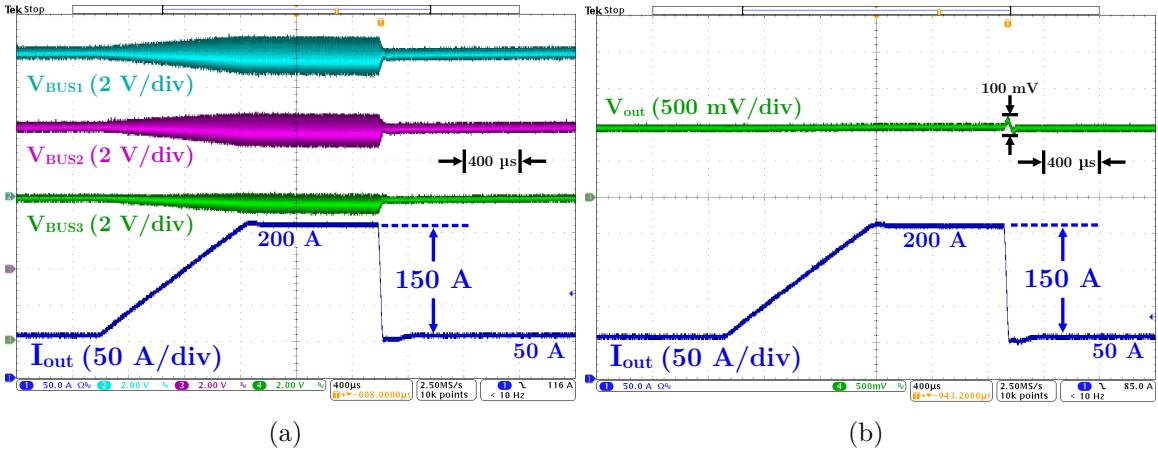


Figure 3.39: Measured waveforms during a load current transient from 50 A to 200 A to 50 A (62.5% load step) of (a) the three intermediate bus voltages, and (b) the output voltage during 48 V to 1 V operation. A voltage-mode control method was implemented using a TMS320F28388D microcontroller. The output capacitance is 2.5 mF.

More advanced control techniques, such as current-mode control, can be used to improve the closed-loop control bandwidth and improve the transient performance [72].

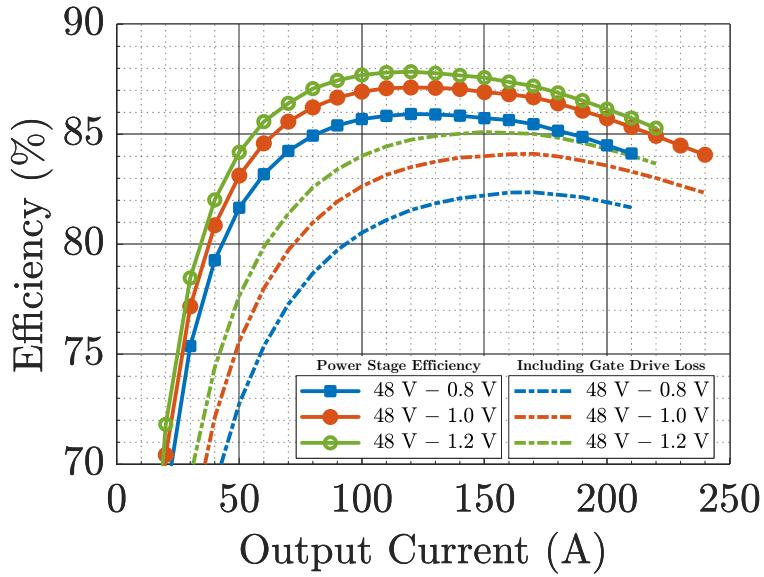


Figure 3.40: Measured efficiency of the Mini-LEGO converter with and without gate driving losses during 48 V to 0.8 V, 1.0 V, and 1.2 V conversion. For 48 V to 1 V, including the gate drive loss, the Mini-LEGO converter achieves a peak efficiency of 84.1% at 120 A and a full load efficiency of 82.3% at 240 A.

### 3.5.4 Converter Performance

Figure 3.40 summarizes the efficiency of the Mini-LEGO converter with 48 V input and output voltages of 0.8 V, 1.0 V, and 1.2 V, with the SC stage switching at 432.9 kHz, and the multiphase buck stage switching at 1.515 MHz. The efficiency is presented with and without the gate drive losses included. Gate drive losses consist of the power consumed by the SC isolated gate drivers for the floating switches, powered by an auxiliary 10 V supply, and the power consumed by the SC and multiphase-buck DrMOS devices, powered by an auxiliary 5 V supply. The input voltage and output voltage were measured across the input and output capacitors. The data was measured in 10 A intervals. For the 1.0 V and 1.2 V tests, the full load current was determined by the point at which the multiphase buck stage DrMOS junction temperatures were less than or equal to 100 °C. For the 0.8 V curve, the data stops at 210 A due to the voltage drop between the converter and the electronic load used

which limits the amount of current from the electronic load. At an output voltage of 1.0 V, the converter achieves a peak efficiency of 87.1% at 120 A, and a full load efficiency of 84.1% at 240 A, without the gate driving losses. Including the buck stage gate driving losses of 4.5 W and the SC stage gate driving losses of 1.4 W, the peak efficiency at 1.0 V is 84.1% at 170 A and the full load efficiency is 82.3% at 240 A.

To understand the cooling mechanisms of the Mini-LEGO converter prototype, thermal simulations were conducted to determine what the target power density of the converter would be based on the cooling resources available. For the experimental setup of Figure 3.20, the decision to use forced air cooling was made, using an output motherboard that was sized to interface with all of the measurement equipment. These two factors – cooling and interface – impact the thermal performance of a converter designed for vertical power delivery and must be considered during the overall system design. The availability of liquid cooling resources, or the heat dissipation of loads that are placed directly on the same motherboard as the converter, will change the design considerations required for optimal thermal performance.

Figure 3.41 shows the results of a thermal simulation using ANSYS Icepak 3D, which was performed at full load ( $V_{out} = 1$  V,  $I_{out} = 240$  A, and  $P_{loss} = 45$  W) for the Mini-LEGO converter pictured in Figure 3.36. The DrMOS devices in the buck stage, DrMOS devices in the switched-capacitor stage, and dual-channel MOSFETs in the switched-capacitor stage are modeled as a two-resistor thermal network, using the values provided in the datasheets for junction-to-case resistance ( $R_{jc}$ ) and junction-to-board resistance ( $R_{jb}$ ). The temperature distribution is shown, with an expected buck stage DrMOS temperature of 95.4 °C. A second simulation using a small motherboard was conducted. With reduced cooling capability from the motherboard, the DrMOS junction temperature increases by 7.4 °C to 103 °C.

Junction temperature data from the multiphase buck stage DrMOS devices is plotted in Fig. 3.42a during a 48 V to 1 V operation test. At each output current

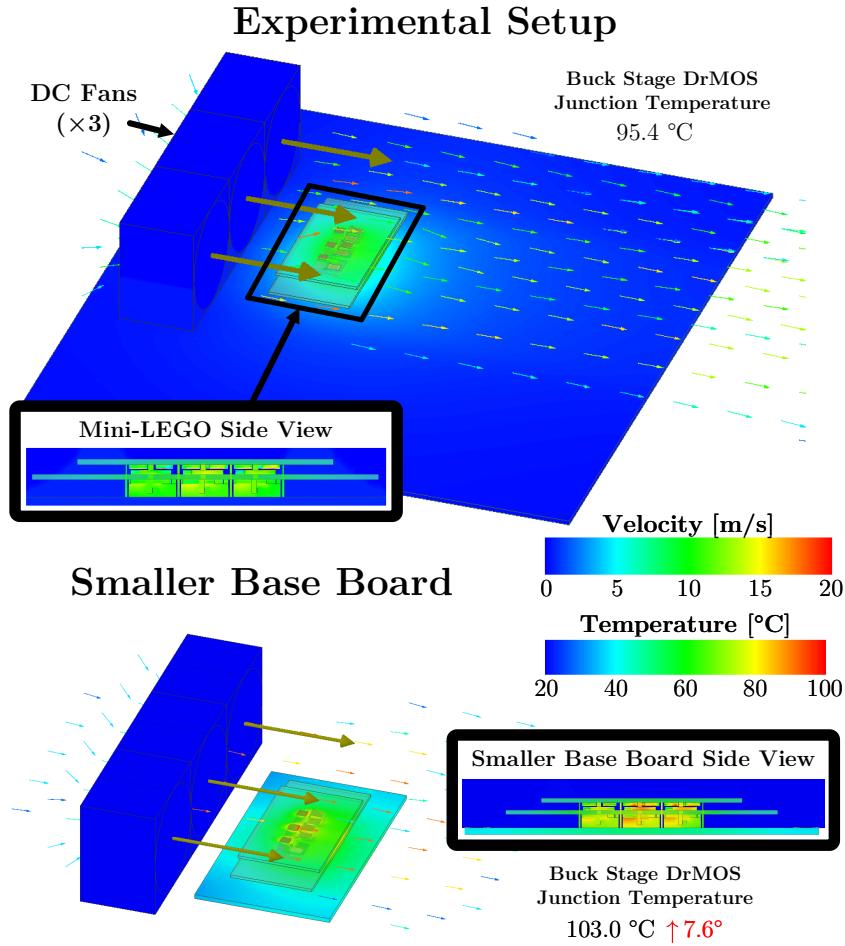


Figure 3.41: ANSYS Icepak 3D thermal simulation of the Mini-LEGO converter connected to the output motherboard shown in Fig. 3.36 (top) and a smaller output motherboard (bottom). The thermal simulation is done for the Mini-LEGO operating at an output voltage of 1 V and output current of 240 A, with 45 W of loss. The buck stage DrMOS junction temperature is 95.4 °C with the larger output motherboard and increases to 103 °C with the smaller output motherboard. The enlarged PCB for carrying high current also behaves as a cooling channel for removing heat.

level, the converter was left operating for five minutes before the current is increased to the next higher level. The temperature is plotted at the end of each interval. The junction temperature is also plotted over the full five-minute interval for the full load operating point. At full load, the DrMOS junction temperature is approximately 100 °C, which matches well with the ANSYS Icepak 3D simulation of Fig. 3.41. Figure 3.42b shows the fan setup and a captured thermal image at 240 A. Three 36 cubic feet per minute (CFM) fans are placed 2 cm away from the converter. The

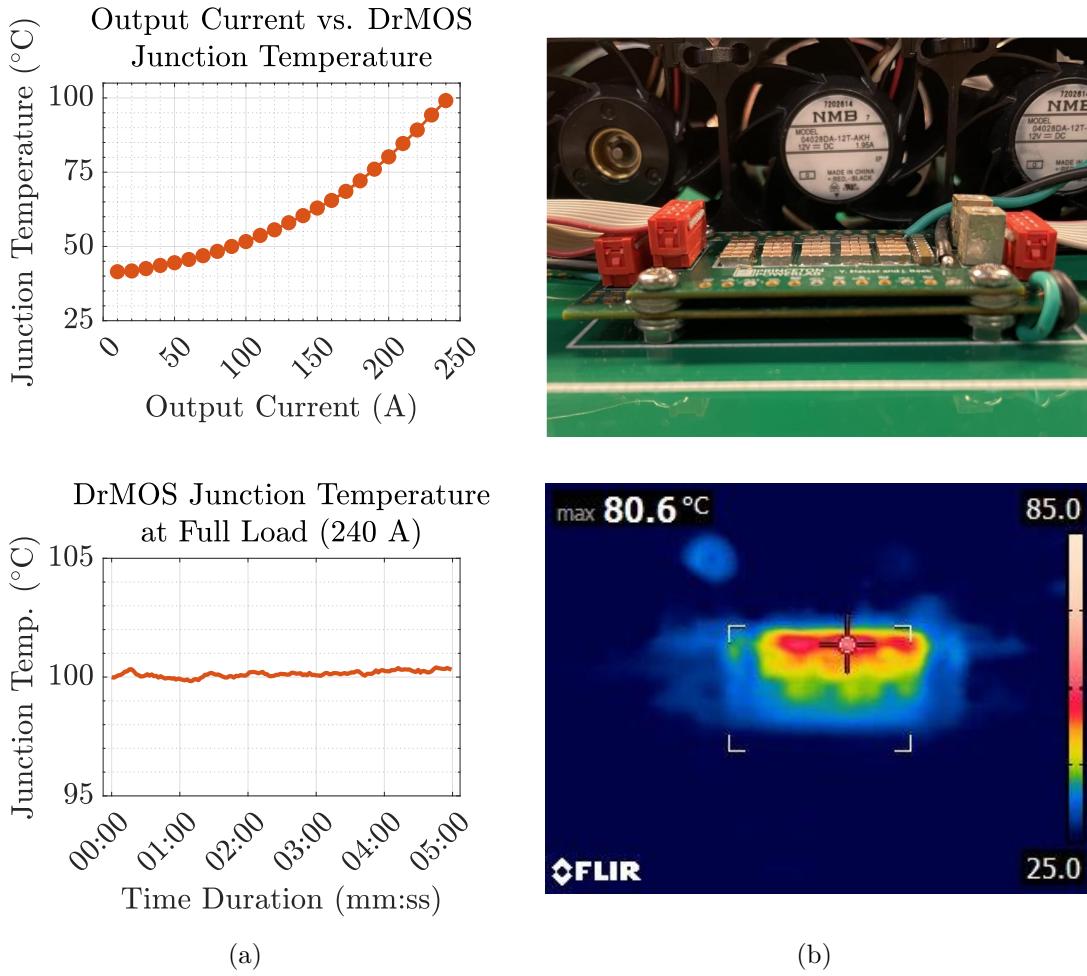


Figure 3.42: (a) Plot of the output load current vs. DrMOS junction temperature for the Mini-LEGO converter during the 48 V to 1 V operation test (top). The temperature reported is the temperature at the end of a five minute interval where the converter is left running at the specified load current. The bottom plot shows the junction temperature at the full load operating point during the duration of the five minute time interval. (b) Side view image and corresponding thermal image of the Mini-LEGO converter at the full load operating point of 240 A.

thermal image taken from the side view shows the PCBs reaching roughly 81 °C during full load operation.

A theoretical loss breakdown is presented in Fig. 3.43. The calculations use experimentally measured duty ratios and junction temperatures to account for the temperature impact on switch resistance values. In the SC stage, the loss comes from the dual-channel MOSFETs and synchronous rectifier DrMOS devices, the PCB copper

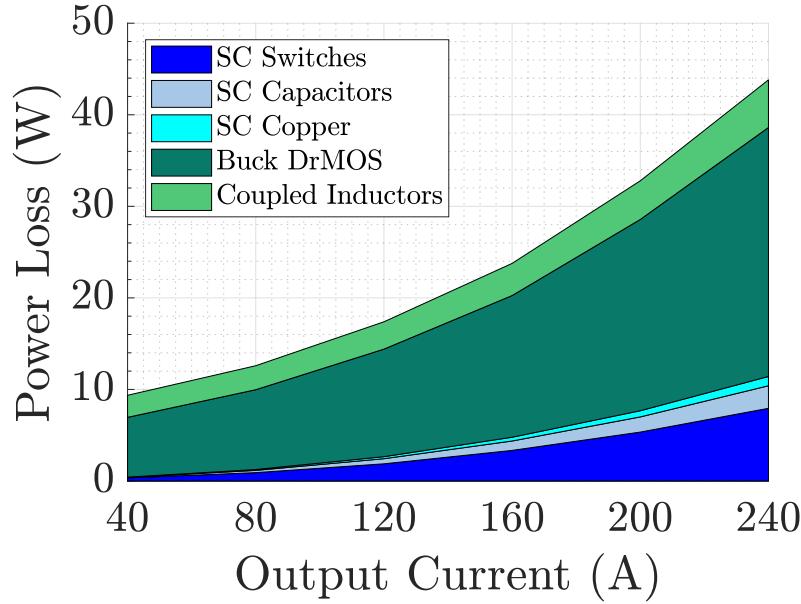


Figure 3.43: Calculated loss breakdown of the Mini-LEGO converter during 48 V to 1 V operation. The SC stage loss is split into switching and conduction losses due to the switches, energy and conduction losses due to the capacitors, and loss due to the PCB and vertical copper connectors. In the multiphase buck stage, the loss is divided into the device switching and conduction losses and the winding and core losses from the coupled inductors.

and vertical copper rods that connect the two stages together, and both the flying and filter capacitors. In the buck stage, the loss comes from the DrMOS devices and the coupled inductor. At 120 A, the peak efficiency point, the converter has 17.8 W of loss, with 15 W coming from the multiphase buck stage. Most of the loss comes from the buck stage DrMOS devices, which are switching at a high frequency. At 240 A, there is 45 W of loss, with around 10 W from the SC stage and 35 W from the multiphase buck stage. The efficiency of the SC stage at full load is 95.5%, and the efficiency of the multiphase buck stage is 88.1%.

### 3.6 Performance Evaluation and Benchmarking

The Mini-LEGO converter was benchmarked against state-of-the-art 48-V-to-1-V voltage regulator modules from both academia and industry, as presented in Ta-

Table 3.4: Performance Comparison of 48 V-to-1 V Point-of-Load VRMs

Year	Note	At Peak Efficiency			At Full Load Efficiency				Switching Frequency <sup>‡</sup>
		Output Current	Efficiency	Power Density <sup>†</sup>	Output Current	Efficiency	Power Density <sup>†</sup>	Area Density	
2024	Mini-LEGO	160 A	84.1%	929 W/in <sup>3</sup>	240 A	82.3%	1390 W/in <sup>3</sup>	0.71 A/mm <sup>2</sup>	1515 kHz
2022	Vertical Stacked LEGO-PoL	190 A	88.4%	124 W/in <sup>3</sup>	450 A	84.8%	294 W/in <sup>3</sup>	0.30 A/mm <sup>2</sup>	1000 kHz
2020	Sigma [23] <sup>*</sup>	50 A	94.0%	256 W/in <sup>3</sup>	80 A	92.5%	410 W/in <sup>3</sup>	0.13 A/mm <sup>2</sup>	600 kHz
2020	Vicor [20, 21]	120 A	90.1%	224 W/in <sup>3</sup>	214 A	≈87%¶	400 W/in <sup>3</sup>	0.20 A/mm <sup>2</sup>	1025 kHz
2021	On-Chip [31]	1.5 A	90.2%	37 W/in <sup>3</sup>	8 A	76.0%	198 W/in <sup>3</sup>	0.03 A/mm <sup>2</sup>	2500 kHz
2021	ADI [19]	30 A	90.8%	53 W/in <sup>3</sup>	50 A	88.1%	89 W/in <sup>3</sup>	0.06 A/mm <sup>2</sup>	350 kHz
2021	24 V VIB [33]	144 A	93.3%	75 W/in <sup>3</sup>	450 A	88.1%	232 W/in <sup>3</sup>	0.16 A/mm <sup>2</sup>	417 kHz
2022	SDIH [32] <sup>§</sup>	50 A	81.4%	285 W/in <sup>3</sup>	116 A	73.2%	663 W/in <sup>3</sup>	0.15 A/mm <sup>2</sup>	750 kHz
2022	Dickson <sup>2</sup> [35]	100 A	91.6%	133 W/in <sup>3</sup>	270 A	87.7%	360 W/in <sup>3</sup>	0.14 A/mm <sup>2</sup>	280 kHz
2023	MSC-PoL [38]	80 A	91.1%	221 W/in <sup>3</sup>	220 A	85.8%	607 W/in <sup>3</sup>	0.26 A/mm <sup>2</sup>	500 kHz
2023	Sw. Bus [36]	380 A	92.4%	192 W/in <sup>3</sup>	1200 A	87.5%	607 W/in <sup>3</sup>	0.23 A/mm <sup>2</sup>	200 kHz
2023	MHB-CDR [37]	40 A	93.1%	345 W/in <sup>3</sup>	120 A	87.8%	1037 W/in <sup>3</sup>	0.15 A/mm <sup>2</sup>	600 kHz

<sup>†</sup> The power density is calculated with the box volume (maximum length × width × height) of the prototype, including the gate drive circuitry.

<sup>‡</sup> The switching frequency of the voltage regulation stage, which strongly influence the transient dynamics of the voltage regulator.

\* The gate drive loss is not included in the efficiency of the Sigma converter.

¶ The full load efficiency (Vicor) 48-V-to-1-V solution is not available and an estimate is presented here for comparison purposes.

§ The efficiency (SDIH) including the gate drive losses is calculated using the average gate drive energy per switching cycle provided in [32].

|| The efficiency and density (MHB-CDR) is reported for 48 V to 1.8 V conversion.

ble 3.4 and Figure 3.44. The top section compares the Mini-LEGO against the first iteration vertical stacked LEGO-PoL prototype. The Mini-LEGO switches at 1.5 times the frequency, and improves on both the power density and the current area density, by trading off a 4.3% peak efficiency and a 2.5% full load efficiency. This implementation includes all of the gate drive circuitry within the power stage area.

The Mini-LEGO converter is able to achieve extremely high power density and current area density compared to existing state-of-the-art designs. In terms of regulation stage switching frequency, it switches at the highest frequency of the discrete implementations considered; its switching frequency is only exceeded by fully integrated solutions such as the one presented in [31]. The peak efficiency of the Mini-LEGO is lower than most other designs. However, due to the low maximum phase

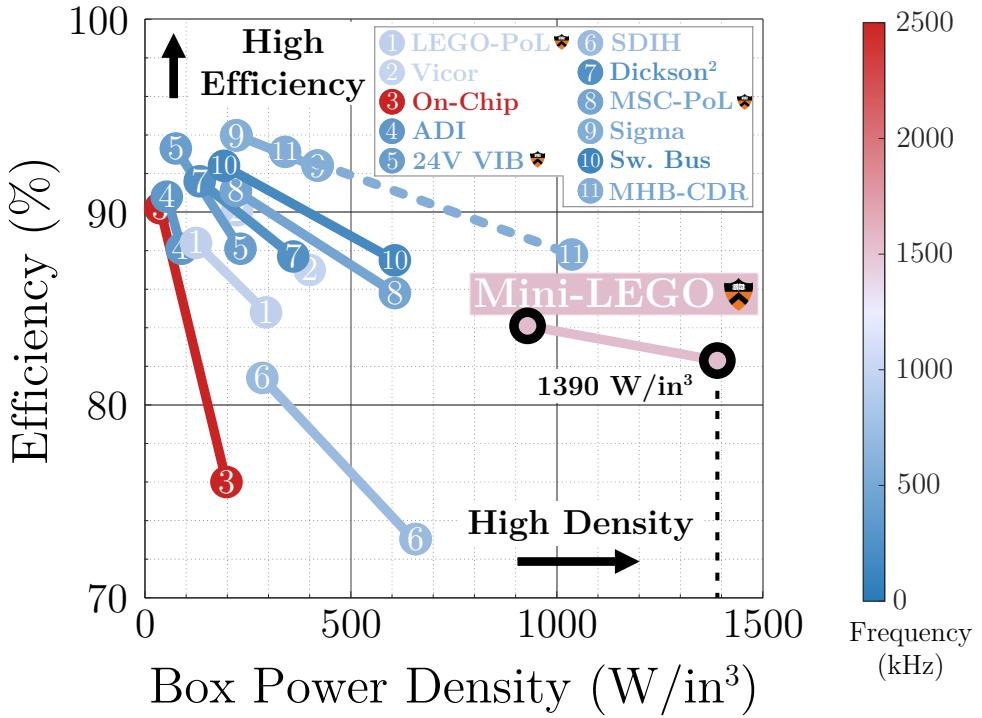


Figure 3.44: Plot of the peak efficiency and box power density at the peak efficiency point, as well as the full load efficiency and box power density at the full load efficiency point, connected with a line, for all of the 48-V-to-1-V converters presented in Table 3.4. All designs plotted include the gate driving size and all include the gate driving losses, with the exception of “⑨ Sigma”. The line for “⑪ MHB-CDR” is dashed as the density and efficiency are reported for 48-V-to-1.8-V conversion. The Mini-LEGO achieves unprecedented power density at both the peak and full load efficiency points, achieving a 1390 W/in<sup>3</sup> density at 240 A of output current with 84.1% efficiency. The Mini-LEGO converter was optimized to achieve the highest density with the highest switching frequency while sacrificing efficiency, given sufficient cooling capability near microprocessors.

current, the full load efficiency is comparable to other designs despite the lower peak efficiency. Better magnetic materials more suitable to the 1–10 MHz range can help to reduce the fixed losses present in the multiphase buck stage to obtain higher peak efficiency. While the latest DrMOS devices are suitable for switching frequencies up to 2 MHz, their performance past 1 MHz still limits the overall system efficiency at higher switching frequencies.

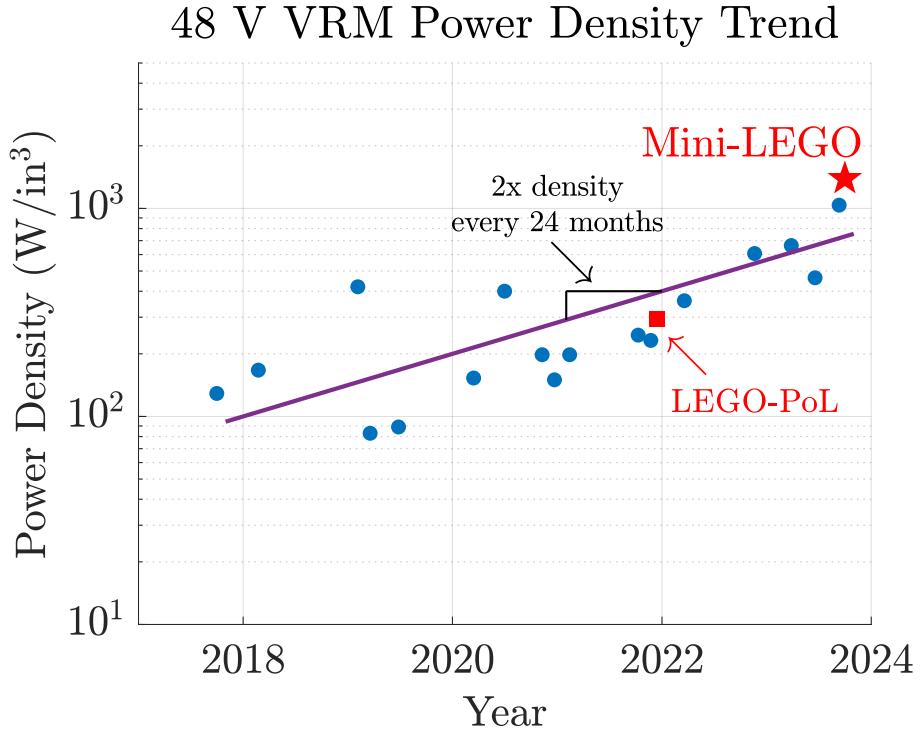


Figure 3.45: Trend of the power density (in W/in<sup>3</sup>) of various 48 V to 1 V CPU VRMs. The date represents either the date of publication in a journal, the date presented in a conference, or the date of release of the initial datasheet revision [18–38]. The Mini-LEGO design significantly improves on the power density of the LEGO-PoL design after 24 months of circuit-magnetics co-optimization.

The DrMOS devices used in the multiphase buck stage were optimized for 1 MHz, which placed limitations on how fast the devices could switch before performance significantly degraded. In regards to the overall system height, further opportunities to reduce the passive component size will present themselves with devices that can maintain acceptable performance at 2 MHz and beyond. The coupled inductor still occupies roughly 30% of the height, similar to the initial vertical stacked LEGO-PoL design.

Figure 3.45 shows a plot of the power densities of 48 V VRMs that have been designed over the last six years. Designs from both academia and industry are plotted based on the date in which the design was published in a journal or the date of release of the initial datasheet revision [18–38]. Fitting a trend line to the data

highlights that designers have been roughly doubling the power densities of 48 V VRMs every two years – analogous to the empirical observation of Moore’s Law which observed a doubling in the number of transistors in an integrated circuit every 18-24 months. The Mini-LEGO converter continues this trend, and achieves a two times reduction in height and two times reduction in area over the original LEGO-PoL design in approximately 24 months. As semiconductor device technology continues to improve and support higher frequency operation, particularly with the advent of wide-bandgap gallium nitride (GaN) power devices, this, along with continued development of magnetic materials for higher frequency operation, enables designers to continue to further reduce passive component sizes and increase power densities [73]. Circuits-magnetics co-design to maximize the benefits of magnetic components in a topology while shrinking their size is essential to furthering this trend.

### **3.7 Chapter Summary**

This chapter presents a linear-extendable group-operated architecture for high density microprocessor power delivery. Proposed architectural solutions to solve the challenges of delivering power from a high input voltage to a low voltage, high current load with high power density, high efficiency, and high control bandwidth are examined. A specific subset of architectures known as hybrid switched-capacitor circuits can leverage capacitor energy transfer for higher density, with techniques such as soft charging to improve the efficiency and two-stage operation to improve the control bandwidth. Merging the operation of a switched-capacitor and switched-inductor stage enables dual frequency operation and allows hybrid switched-capacitor converters to de-couple the trade offs of density, efficiency, and speed and address each separately.

A specific hybrid switched-capacitor called the LEGO-PoL architecture is introduced and analyzed. This architecture is highly modular, consisting of submodules

made up of a 2:1 switched-capacitor unit and a multiphase buck unit. The operation of the two units are merged together, eliminating the bulky decoupling capacitor between the two stages and replacing it with a much smaller filter capacitor. The coupled operation allows the magnetics in the second stage to be utilized as a current source to charge and discharge the flying capacitors in the first stage, eliminating charge transfer losses between the flying capacitors, which both improves efficiency and enables size reduction. By linearly extending these submodules, configuring their inputs in series and outputs in parallel, this architecture can be configured to suit a wide range of input voltages and output currents. To enable this modularity, the mechanism of automatic current sharing and voltage balancing between submodules is analyzed in detail.

To verify the suitability of the LEGO-PoL architecture for vertical power delivery, an initial prototype was designed, built, and tested. This prototype had a power stage area of 767 mm<sup>2</sup> without the gate drive circuitry, 1510 mm<sup>2</sup> with the gate drive circuitry, and a height of 16.65 mm. The buck regulation stage switched at 1 MHz with four-phase interleaving. The converter had a full load current of 450 A with forced air cooling and 780 A with liquid cooling. The efficiency including the gate drive losses for 48-V-to-1-V was 88.4% at its peak and 84.8% at 450 A with air cooling, resulting in a density of 294 W/in<sup>3</sup>.

Due to the limitations of the first LEGO-PoL prototype in regards to height and size, which prevented its feasibility to perform in-packaging vertical power delivery, a second design iteration was performed and a new design – Mini-LEGO – was built and tested. This prototype reduced the area to 336 mm<sup>2</sup>, including all gate drive circuitry, and halved the height to 8.4 mm. Efficiency from the previous prototype was traded off for gains in both density and control bandwidth. The Mini-LEGO increased the buck switching frequency to 1.5 MHz. The peak efficiency is 84.1% for 48-V-to-1-V and the full load efficiency at 240 A is 82.3%. The resulting power den-

sity is 1390 W/in<sup>3</sup>, a five-fold increase over the first iteration LEGO-PoL prototype. The Mini-LEGO converter boasts one of the highest power density numbers when compared against other 48-V-to-1-V VRMs, and its thin height pushes the vision of in-packaging vertical power delivery for high density microprocessor loads.

## Related Publications

1. J. Baek, P. Wang, Y. Elasser, Y. Chen, S. Jiang, and M. Chen, “A Merged-Two-Stage LEGO-PoL Converter with Coupled Inductors for Vertical Power Delivery,” in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 490-497, 2020 [74]
2. Y. Elasser, J. Baek, and M. Chen, “A Merged-Two-Stage LEGO-PoL Converter with Coupled Inductors for Vertical Power Delivery,” in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 916-923, 2020 [75]
3. J. Baek, Y. Elasser, and M. Chen, “3D LEGO-PoL: A 93.3% Efficient 48V-1.5V 450A Merged-Two-Stage Hybrid Switched-Capacitor Converter with 3D Vertical Coupled Inductors,” in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1321–1327, 2021 [76]
4. Y. Elasser, J. Baek, K. Radhakrishnan, H. Gan, J. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, C. R. Sullivan, and M. Chen, “Vertical Stacked 48V-1V LEGO-PoL CPU Voltage Regulator with 1A/mm<sup>2</sup> Current Density,” in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1259–1266, 2022. [77]
5. J. Baek, Y. Elasser, K. Radhakrishnan, H. Gan, J. P. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, C. R. Sullivan, and M. Chen, “Vertical Stacked LEGO-PoL CPU Voltage Regulator,” *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6305–6322, 2022. [25]
6. Y. Elasser, J. Baek, K. Radhakrishnan, H. Gan, J. P. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, V. De, C. R. Sullivan, and M. Chen, “Mini-LEGO CPU Voltage Regulator,” *IEEE Transactions on Power Electronics*, vol. 39, no. 3, pp. 3391–3410, 2024. [78]

7. Y. Elasser, H. Li, P. Wang, J. Baek, K. Radhakrishnan, S. Jiang, H. Gan, X. Zhang, D. Giuliano, and M. Chen, “Circuits and magnetics co-design for ultra-thin vertical power delivery: A snapshot review,” *MRS Advances*, vol. 9, pp. 12–24, 2024. [40]

# Chapter 4

## Design Methodology for High-Current Low-Profile Vertical Coupled Magnetics

### 4.1 Background and Motivation

Magnetics play a critical role in delivering high amounts of current to high density loads. Magnetic components provide filtering of pulsed power waveforms, voltage conversion and regulation, and serve as current sources throughout the switching mode power supply topologies. While magnetics are essential for high performance power electronics, they are often the bottleneck in improving the density of a converter. Of the three building blocks of power converters – semiconductor devices, capacitors, and magnetics – magnetic components are often the bulkiest. In addition, larger inductors generally have greater power handling capability as compared to multiple smaller inductors, posing the question of how to effectively deliver large amounts of current to high density loads with high density for vertical power delivery [11].

Designing vertical magnetics that can enable the advantages of vertical power delivery has yet to be fully explored. This chapter focuses on developing a new

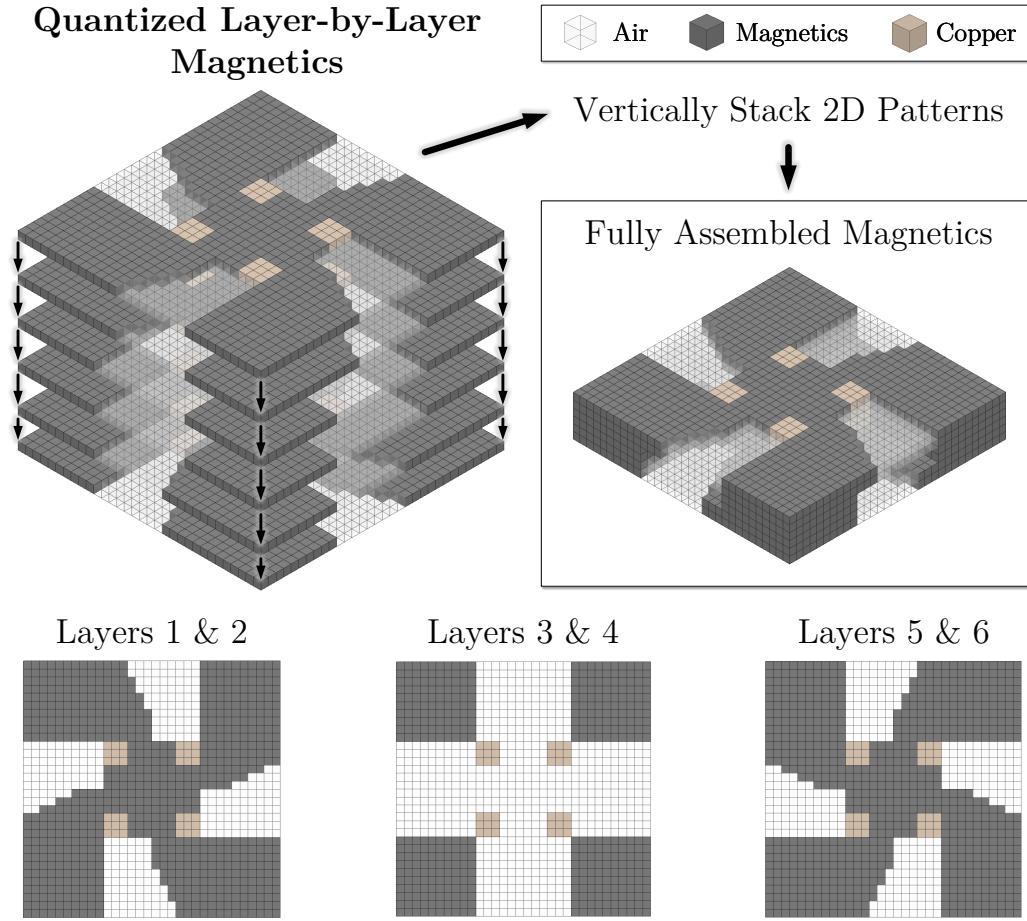


Figure 4.1: The vision of quantized magnetics design for vertical power delivery. A fixed and constrained 3D volume is divided into smaller unit cubes. An optimization routine determines whether to allocate each individual unit cube as air, ferrite, or copper, building a magnetic structure layer by layer to achieve the desired inductance and winding resistance. The layers are vertically stacked to assemble the final magnetic structure for manufacturing.

methodology for designing magnetic components in a limited cubic area to achieve desired functionality while ensuring robust operation. This vision is demonstrated in Figure 4.1. The design of a magnetic component is broken down into its constituent parts – flux carrying, flux blocking, current carrying, and current blocking (omitted from the example in Figure 4.1). The flux carrying magnetic material is used to provide magnetic flux with a permeability greater than that of air, which can be used to guide the flux into well-defined paths and achieve inductance. By strategically

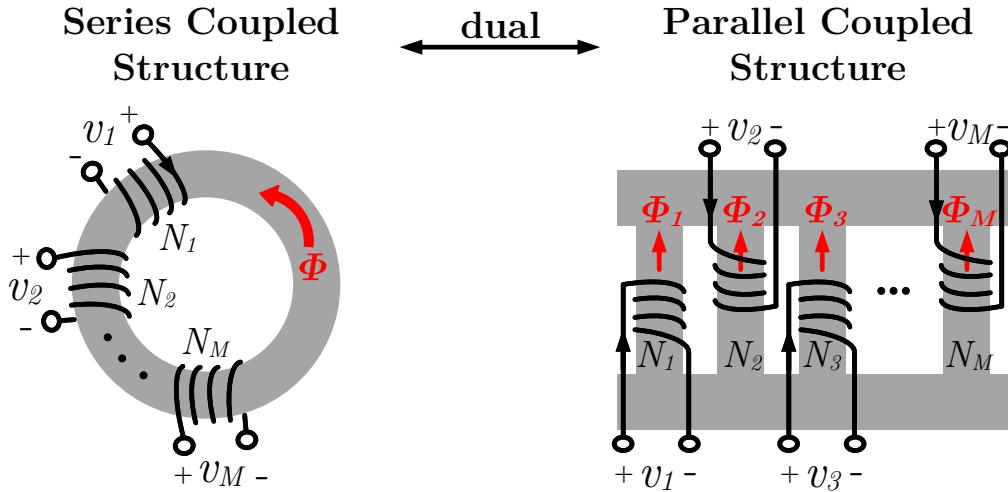


Figure 4.2: Two major categories of multiwinding magnetic structures: series coupled magnetic structure, where multiple windings share the same flux path; parallel coupled magnetic structure, where each the flux from each winding merges at specific points in the structure.

placing flux blocking air gaps in certain parts of the magnetic component, a high reluctance path can be created in certain regions where it is not advantageous for flux to traverse through. The current carrying material (depicted as copper) serves as the conductor to deliver the current through the magnetic component, inducing the magnetic flux. A constrained volume can be segmented and quantized into multiple smaller unit cubes: the goal of the optimization routine is to effectively allocate each unit cube to one of these building blocks to satisfy the constraints and design targets of the end application.

To design magnetic components that can deliver large power in small area and height, this chapter also explores integration of multiple magnetic components into one by leveraging magnetic coupling. Magnetic coupling is present in two forms, series coupling and parallel coupling, highlighted in Figure 4.2. Series coupling, used in magnetic transformers, combines multiple windings into one core with a shared flux path, and can be used for voltage conversion by modulating the number of turns on each winding. For the application of high density loads, where the high load current

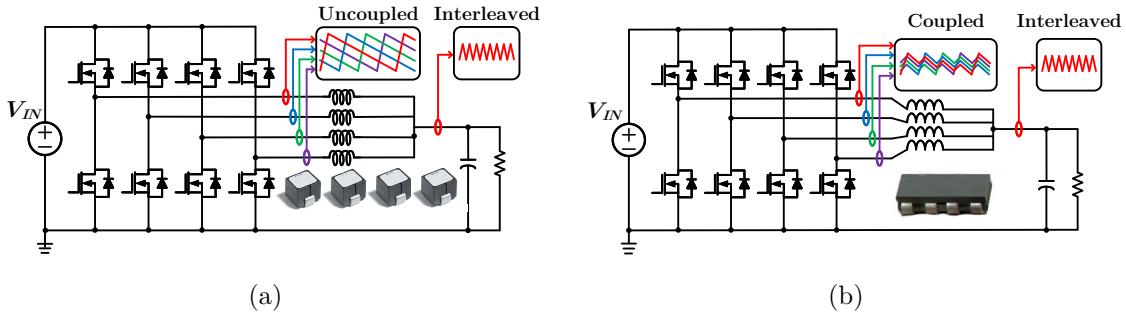


Figure 4.3: An example four-phase interleaved buck converter with (a) four discrete inductors; (b) one four-phase coupled inductor. By interleaving the phases at the output, the output current ripple is reduced and its effective frequency is multiplied. Coupling the inductors together extends the benefits achieved by interleaving into the individual phases themselves.

is often distributed into multiple smaller phases that each deliver a fraction of the output current, parallel magnetic coupling is promising as a way to combine magnetic components into one. By creating points at which the flux from multiple different windings merge, the parallel coupled magnetic structure can shuffle the energy from one phase into the other coupled phases, which can greatly reduce the  $\frac{1}{2}LI^2$  energy that the magnetic core has to store. Multiple inductors can be merged onto one core and can be made smaller than if they were separated, with a low effective inductance in regards to common mode energy storage, while still maintaining a high inductance in differential mode steady state interleaved operation.

Parallel magnetic coupling for VRMs has been thoroughly explored throughout the last two decades as a promising technology for PoL power delivery [79,80]. Figure 4.3a shows the circuit schematic of a four-phase buck converter, implemented with discrete inductors. By interleaving each of the phases 90° from each other, the overall output current ripple can be reduced, however, the current ripple reduction does not extend to the individual phases themselves. A high inductance is needed to maintain a sufficiently low per-phase current ripple. By inversely coupling the inductors using a single magnetic core as in Fig. 4.3b, the current ripple cancellation achieved at the output can be extended into the individual phases themselves. This offers efficiency

benefits in reducing the ac rms current through the copper traces and semiconductor devices. In addition, as this ripple reduction is achieved through coupling, a lower effective inductance is needed when compared to the discrete case, which results in faster transient response when compared to the discrete case for the same per-phase current ripple.

This chapter first presents ways to model parallel coupled inductors. After reviewing the available models and their pros and cons, the models are unified and summarized in Section 4.2 as a way to understand the electrical performance of magnetic components. With a way to model coupled inductors, an optimization routine is developed and detailed for vertical coupled magnetic components in Section 4.3. This optimization routine is used to design and fabricate three vertical coupled inductor designs for different applications, operating at different switching frequencies. The first design presented in Section 4.4 is a 1 MHz four-phase coupled inductor, designed for the initial vertical stacked LEGO prototype in Section 3.4. This design has a height of 5.25 mm and targets 65 A of per-phase current in a 12 mm × 13 mm footprint. In the Mini-LEGO re-design discussed in Section 3.5, a new coupled inductor structure is designed at 1.5 MHz and presented in Section 4.5. The Mini-LEGO inductor has a height of 2.5 mm and delivers 20 A per phase with an area of 8 mm × 8 mm. Lastly, a novel magnetic structure called the pinwheel coupled inductor structure is designed for 2 MHz operation in Section 4.6. This inductor structure pushes towards the vision layed out in Figure 4.1, where the 3D volume is optimized to create a structure whereby the ferrite material is contorted around the winding, resulting in a magnetic structure with ultra-low-resistance and a low profile of 1.8 mm.

## 4.2 Modeling and Analysis of Multiphase Coupled Inductors

This section focuses on the modeling and analysis of parallel multiphase coupled inductors and their operation mechanisms. Figure 4.4 shows an example geometry of

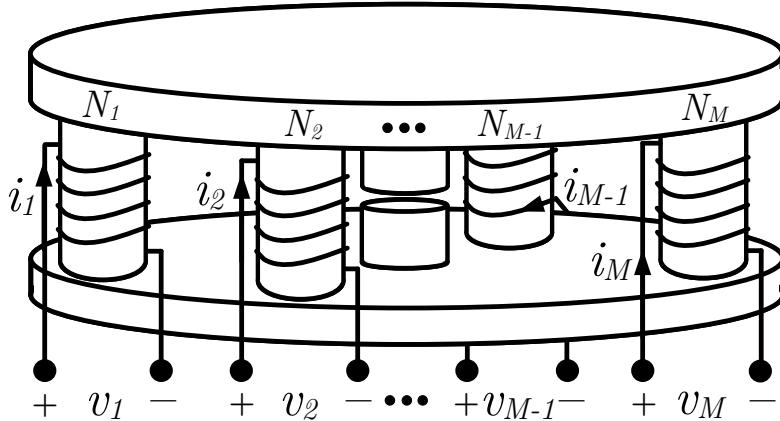


Figure 4.4: A symmetric multiphase coupled inductor with  $M$  windings. This structure has  $M$  outer legs and one center leg. Each winding in this example has  $N$  turns ( $N_1 = N_2 = \dots = N_M = N$ ).

a multiphase coupled inductor with  $M$  outer legs and one leg in the center. This is a parallel coupled multiwinding structure with symmetric geometry. Each of the outer legs is encircled by an  $N$ -turn winding. A center leg is present with an air gap. This air gap incorporates an additional path for the magnetic flux, and by controlling the height of the air gap, the amount of flux through the center leg can be modulated.

#### 4.2.1 Models for Coupled Inductors

Models for coupled inductor structures can generally be categorized into *math-based models* and *physics-based models*. The math-based models, including models such as the inductance matrix model, multiwinding transformer model, and extended cantilever model, focus on the mathematical coupling relationship between windings. Information about the core geometry and material properties are not explicitly included in math-based models. Physics-based models represent the physical geometry of the magnetic structure more directly, using a lumped circuit element to correspond to each portion of the magnetic structure. Physics-based models, such as the magnetic circuit model, gyrator-capacitor model, and inductance dual model can offer greater insight to magnetics designers on how the geometrical structures impact the

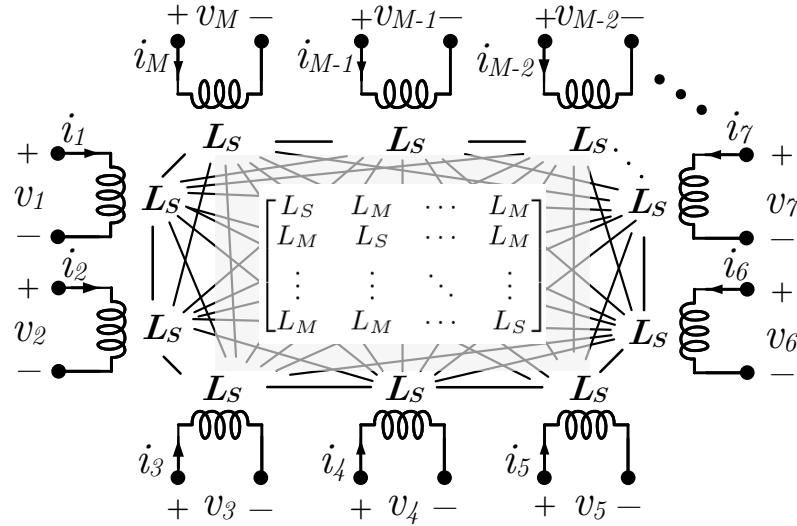


Figure 4.5: Inductance matrix model representation of the structure in Figure 4.4.

magnetic performance. In particular, the inductance dual model offers unique insights into the analysis and design of parallel coupled magnetic structures, particularly for multiphase coupled inductor buck converters.

### Math-Based Models

The voltage and current of an arbitrary multiphase coupled inductor is described by an inductance matrix  $\mathbf{L}$ :

$$\underbrace{\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_M \end{bmatrix}}_{\mathbf{V} \quad (M \times 1)} = \underbrace{\begin{bmatrix} L_{11} & L_{12} & \cdots & L_{1M} \\ L_{21} & L_{22} & \cdots & L_{2M} \\ \vdots & \vdots & \ddots & \vdots \\ L_{M1} & L_{M2} & \cdots & L_{MM} \end{bmatrix}}_{\mathbf{L} \quad (M \times M)} \underbrace{\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \vdots \\ \frac{di_M}{dt} \end{bmatrix}}_{\mathbf{I} \quad (M \times 1)}. \quad (4.1)$$

$\mathbf{V}$  and  $\mathbf{I}$  are the voltages and currents of the  $M$  windings. The inductance matrix  $\mathbf{L}$  is a symmetric  $M \times M$  matrix with positive and negative element values. It describes the mathematical coupling relationship between windings and is applicable to linear multiwinding coupled magnetics, neglecting losses [81–84]. The element values of this

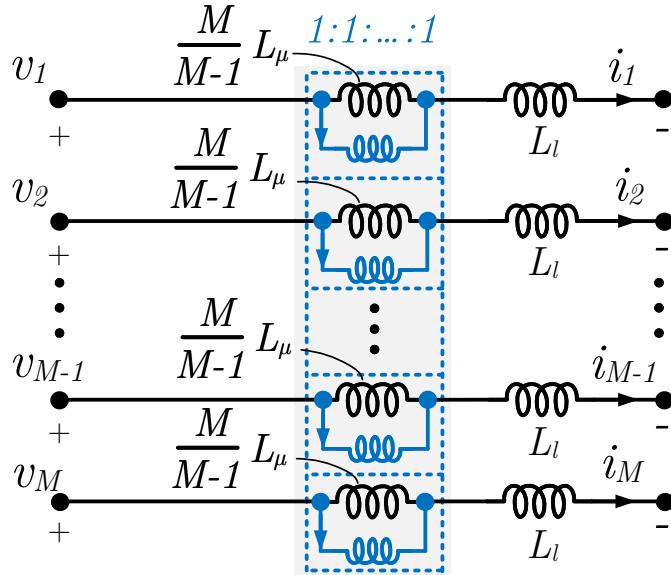


Figure 4.6: Multiwinding transformer model representation of the structure in of the structure in Fig. 4.4. The ideal current equalizing transformer (highlighted in blue) equalizes the current of all of its windings, forcing the sum of the per-turn voltages of all windings to equal zero.

matrix can be identified by finite-element analysis or by experimental measurements.

Figure 4.5 shows the inductance matrix model of the structure in Figure 4.4 represented as a lumped circuit. The self and mutual inductance values are the element values of the inductance matrix. Many SPICE simulation platforms support the use of the inductance matrix model.

This model is generally the standard for all mathematical analysis of coupled inductors, and can easily be extended for deriving more advanced control models such as state-space analysis. For gaining circuit intuition, the multiwinding transformer model can also be helpful [85]. Similarly to the extended cantilever model, only non-coupled inductors and ideal transformers are used. Figure 4.6 shows one example of the multiwinding transformer model using a current equalizing transformer. The turns ratio of the current equalizing transformer is  $\{1 : 1 : \dots : 1\}$  (assuming equal number of turns  $N$  in each physical winding). Each winding of the current equalizing transformer has a magnetizing inductance in parallel with the winding, and a

leakage inductance in series. The magnetizing inductance for each phase is equal to  $\frac{M}{M-1}L_\mu$ , where  $L_\mu$  is defined by analogy to the magnetizing inductance in a two-winding transformer as  $L_\mu = L_S - L_\ell$ .  $L_S$  is the self inductance of each winding, and is equivalent to  $L_S$  in the inductance matrix model. The multiwinding transformer model can also be represented using voltage equalizing transformers [86]. During a common-mode excitation, whereby the voltages at the positive and negative terminals of each phase of the transformer model are equal, zero voltage is seen across the magnetizing inductance. This is due to the multiwinding transformer, which requires all of the transformer voltages to sum to zero, which can only be achieved if the voltage across each winding is zero. Thus, the leakage inductance is the only effective element during a common-mode excitation, and is a very useful parameter to analyze the behavior of a coupled inductor during a transient.

One drawback of math-based models is that the geometry and material property information is not explicitly captured within the model. Limited insight on magnetic structure design is offered. In addition, as the number of phases increases, the complexity of math-based models rapidly increases. Physics-based models offer more direct insight on the relationship between the physical structure and the model, and are discussed next.

## Physics-Based Models

The magnetic circuit model (also referred to as the reluctance model), as shown in Figure 4.7, is one of the most widely used physics-based models for modeling magnetic components [81–84]. Each portion of the magnetic core is modeled as a reluctance. Each winding is modeled as an MMF source driving the reluctance circuit as a voltage source. This model performs well in capturing the geometric information of the magnetic structure, however, it is challenging to simulate as it is not in terms of voltage and current [87]. The gyrator-capacitor model, shown in Figure 4.8a, replaces the

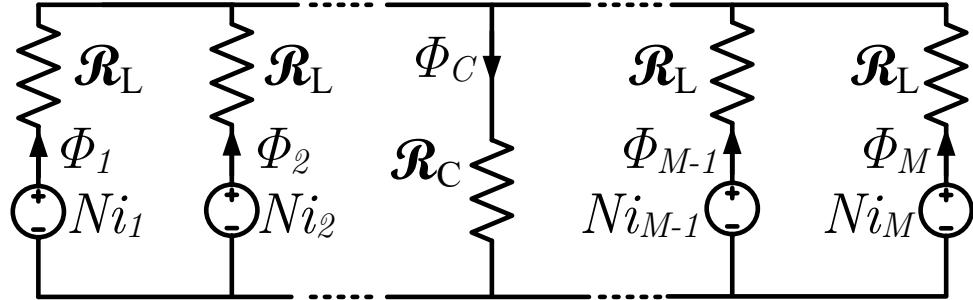


Figure 4.7: Magnetic circuit model of the structure in Figure 4.4. The reluctances of the outer legs are  $\mathcal{R}_L$ , and the reluctance of the center leg is  $\mathcal{R}_C$ , as the structure is fully symmetric.

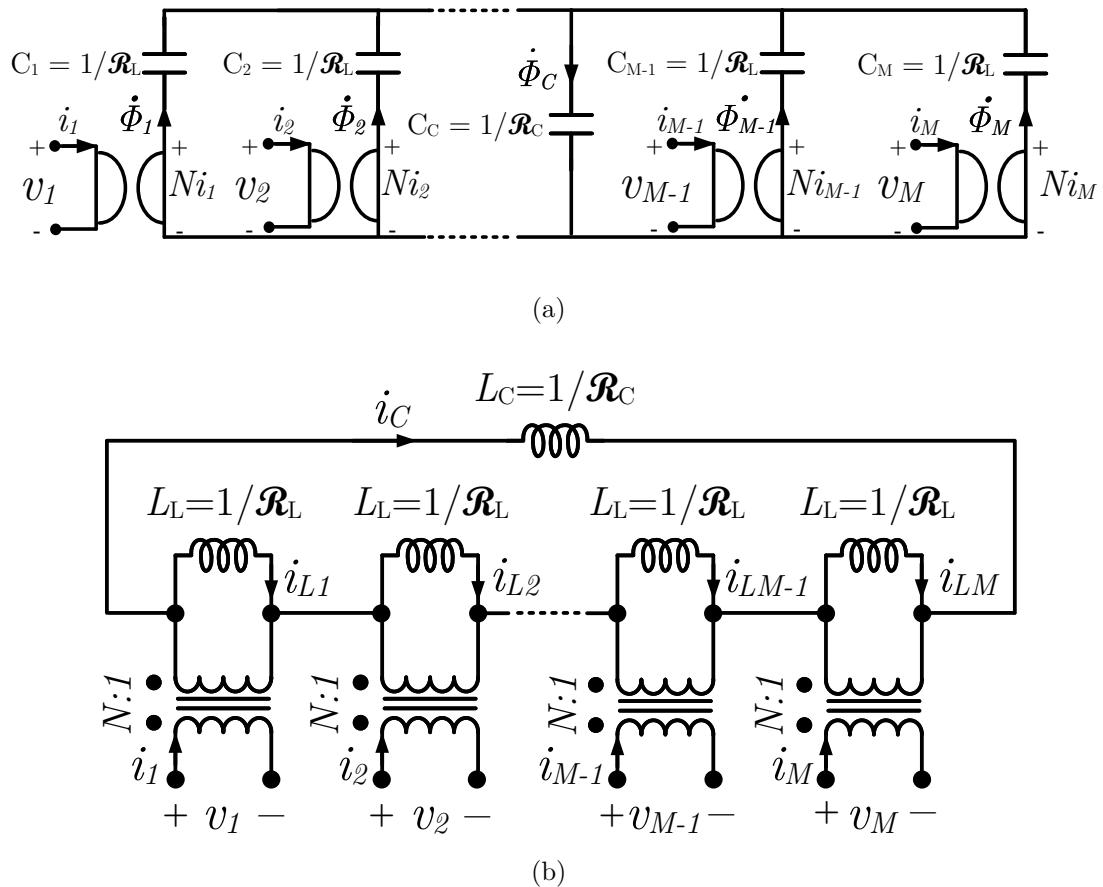


Figure 4.8: (a) Gyrator-capacitor model of the structure in Figure 4.4. The labelled values are capacitances with units of Farads (F). (b) Inductance dual model of the structure in Figure 4.4. This model is derived by taking the topological dual of the gyrator-capacitor model.  $L_L$  and  $L_C$  represent the inductive elements of the outer legs and center legs, respectively.  $i_C$  and  $i_L$  are linearly proportional to  $\Phi_C$  and  $\Phi_L$  in Figure 4.4.

reluctances in the magnetic circuit model with capacitors. The capacitance of each capacitor is equal to the permeance  $\mathcal{P} = 1/\mathcal{R}$  of its corresponding reluctance. The MMF sources are replaced with gyrators, which convert current into voltage [88]. The inductance dual model shown in Figure 4.8b [89–91] is derived by applying topological duality to the gyrator-capacitor model [92]. In the inductance dual model, the elements representing the magnetic core are inductors with inductance values equal to the permeance values  $\mathcal{P} = 1/\mathcal{R}$ , in units of Henries (H). The terminals of the model are ideal transformers with turns ratios equal to the physical turns of the windings.

All models represent the same math and physics, but can be extended in different ways to capture different details. The physics-based models allow for greater understanding of how affecting the geometry of the structure impacts the circuit performance. In particular, the inductance dual model offers various advantages over the other models presented. It allows for easy simulation in any circuit simulation platform, as it consists of discrete inductors and ideal transformers. At the same time, the only parameters the model utilizes are reluctances and number of turns. Any analysis done using the inductance dual model provides insight into how the magnetic geometry impacts inductor performance. In addition, as the number of phases increases, the number of elements in the inductance dual model scales linearly, facilitating easier analysis of designs with a large number of phases.

#### 4.2.2 Analysis of Coupled Inductors in PWM Converters

While a multiphase buck converter achieves current ripple cancellation at the output via phase interleaving, coupling the inductors between phases can extend this ripple reduction through the individual phase currents as well. Analysis of the ripple current cancellation of coupled inductor buck converters using the inductance dual model highlights the key parameters and physical structures that can maximize these benefits.

All of the analysis presented detailing phase current ripple reduction is performed under the assumption of **fixed transient response between non-coupled and coupled cases**. This means that, when a coupled inductor is said to reduce the phase current ripple by a certain factor over non coupled inductors, the value of the non coupled inductor is equal to the leakage inductance  $L_\ell$  of the coupled inductor, as defined in Section 4.2.1 using the multiwinding transformer model. The leakage inductance can be calculated in terms of the reluctances used in the reluctance model formulation of Figure 4.7. The reluctance model can be described in matrix form as follows:

$$N \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_M \end{bmatrix}}_I = \underbrace{\begin{bmatrix} \mathcal{R}_L + \mathcal{R}_C & \mathcal{R}_C & \cdots & \mathcal{R}_C \\ \mathcal{R}_C & \mathcal{R}_L + \mathcal{R}_C & \cdots & \mathcal{R}_C \\ \vdots & \vdots & \ddots & \vdots \\ \mathcal{R}_C & \mathcal{R}_C & \cdots & \mathcal{R}_L + \mathcal{R}_C \end{bmatrix}}_R \underbrace{\begin{bmatrix} \Phi_1 \\ \Phi_2 \\ \vdots \\ \Phi_M \end{bmatrix}}_\Phi. \quad (4.2)$$

Using the matrix of Equation 4.1 with the matrix form of the reluctance model, a link can be established between the physical reluctances and the parameters of the inductance matrix and multiwinding transformer models by taking the time derivative of Equation 4.2.

$$\begin{aligned} \mathbf{V} &= \frac{d\Phi}{dt}, \\ \mathbf{L} &= N^2 \mathbf{R}^{-1}, \\ N \frac{d\mathbf{I}}{dt} &= \mathbf{R} \frac{d\Phi}{dt} = \mathcal{R}_L \frac{d\Phi}{dt} + \mathcal{R}_C \frac{d\Phi_C}{dt} = \frac{\mathcal{R}_L}{N} \mathbf{V} + \frac{\mathcal{R}_C}{N} \sum_{x=1}^M v_x. \end{aligned} \quad (4.3)$$

The self inductance and mutual inductance from the inductance matrix model as well as the leakage inductance from the multiwinding transformer model in terms of reluctances are as follows:

$$L_S = \frac{N^2 (\mathcal{R}_L + (M-1)\mathcal{R}_C)}{\mathcal{R}_L (\mathcal{R}_L + M\mathcal{R}_C)} = L_\mu + L_\ell \quad (4.4)$$

$$L_M = \frac{N^2}{\mathcal{R}_L + M\mathcal{R}_C} = -\frac{1}{M-1} L_\mu \quad (4.5)$$

$$L_\ell = \frac{N^2}{\mathcal{R}_L + M\mathcal{R}_C} = L_S + (M-1)L_M \quad (4.6)$$

In a multiphase buck converter, interleaving of the multiple phases, without taking any coupling into consideration, can reduce the current ripple at the output when compared to a single phase converter. As mentioned above, all analysis will assume a fixed transient response. Thus, to compare a single-phase buck converter with a multiphase buck converter, the single-phase converter is assumed to have an inductance  $L_{1\phi} = L_{M\phi}/M$  where  $L_{M\phi}$  is the inductance of each inductor in the multiphase buck converter. The output ripple current cancellation ratio between a single-phase converter with an output current ripple of  $\Delta i_o^{1\phi}$  and an  $M$ -phase converter with output current ripple  $\Delta i_o^{M\phi}$  is

$$\Gamma \triangleq \frac{\Delta i_o^{M\phi}}{\Delta i_o^{1\phi}} = \frac{(k+1-DM)(DM-k)}{(1-D)DM^2}, \quad (4.7)$$

where  $k$  is an integer index such that  $\frac{k}{M} \leq D \leq \frac{k+1}{M}$  and  $D$  is the duty ratio. By introducing magnetic coupling, the ripple reduction achieved at the output solely due to interleaving  $M$  phases as opposed to using a single-phase converter can now be *extended* to the individual phases themselves. An  $M$ -phase coupled inductor can reduce the phase current ripple as compared to an  $M$ -phase buck converter with non-coupled inductors, whereby the inductance  $L_{M\phi}$  is equal to the leakage inductance  $L_\ell$  of the coupled inductor. Thus, in this scenario, the transient response is fixed: the single-phase converter has one inductor equal to  $L_\ell/M$ ; the  $M$ -phase buck converter

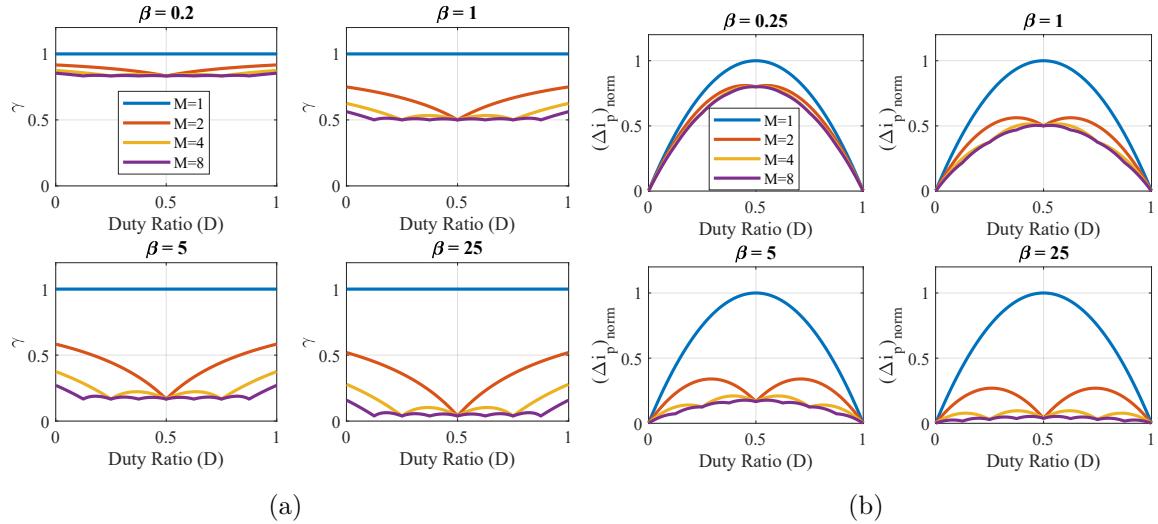


Figure 4.9: (a) Plots of  $\gamma$  vs. duty cycle for different values of  $\beta$  and varying phase count. As coupling increases,  $\gamma$  approaches the value of  $\Gamma$ . (b) Plots of the normalized phase current ripple for different values of  $\beta$  and varying phase count. Increased coupling reduces the per-phase current ripple for fixed transient response.

has  $M$  inductors equal to  $L_\ell$ ; the  $M$ -phase coupled inductor buck converter has an  $M$ -phase coupled inductor with the leakage inductance of each phase equal to  $L_\ell$ .

To quantify how much of the benefit of ripple current cancellation at the output can be extended to the individual phases via coupling, a coupling parameter is defined based on the inductance dual model as  $\beta = \frac{M\mathcal{R}_C}{\mathcal{R}_L}$ . This per-phase current ripple reduction ratio is denoted as  $\gamma$ , and is calculated as follows:

$$\gamma \triangleq \frac{\Delta i_\Phi^{\text{coupled}}}{\Delta i_p^{\text{non-coupled}}} = \frac{1 + \beta\Gamma}{1 + \beta}. \quad (4.8)$$

From this equation, it is shown that as the coupling increases (in other words, for higher values of  $\beta$ ), the phase current ripple reduction approaches the output current ripple reduction. This is demonstrated in Figure 4.9a. As the coupling increases, the value of  $\gamma$  decreases. As  $\beta \rightarrow \infty$ ,  $\gamma \rightarrow \Gamma$  and all of the ripple reduction achieved at the output is observed in the phases themselves. It is also observed that at duty cycles near an integer multiple of  $1/M$ ,  $\gamma \rightarrow \frac{1}{1+\beta}$ . From this, the peak-to-peak current ripple can be calculated

$$\Delta i_{\Phi} = \frac{V_{\text{out}}(1 - D)T}{L_{pss}}, \quad (4.9)$$

where  $L_{pss} = \frac{L_{\ell}}{\gamma}$  is the per-phase steady-state inductance which dictates the current ripple. Figure 4.9b plots the normalized per-phase current ripple,  $\Delta i_{\Phi}/\Delta i_{\Phi}^{\max}$ .  $\Delta i_{\Phi}^{\max}$  is equal to the worst-case phase current ripple, which occurs at  $D = 0.5$  for the single-phase scenario, where the inductance is equal to  $L_{\ell}$ . A lower value of normalized per-phase current ripple indicates a smaller absolute value of the current ripple, which occurs closest to  $D = 0$  and  $D = 1$ .

To design a coupled inductor with high phase current reduction (in other words, a high value of  $L_{pss}$ ),  $\beta$  can be increased by reducing  $\mathcal{R}_L$ . Geometrically, this correlates to using a high permeability material, reducing the length of the side legs, and increasing the cross sectional area of the legs.  $\mathcal{R}_C$  can then be adjusted in order to maintain the appropriate leakage inductance  $L_{\ell}$  to meet the transient requirements. This analysis correlates the physical geometry design directly to the steady-state phase current ripple and transient performance achieved by a designed magnetic geometry. These equations are used in an optimization routine to determine whether a given geometry satisfies the specified constraints on per-phase current ripple and transient speed, while ensuring the magnetic core does not enter saturation for the given operating conditions.

### 4.3 Vertical Coupled Inductor Optimization Procedure

The trade-offs between efficiency, size, and speed of a coupled inductor are all highly correlated. Figure 4.10 organizes the main metrics of a coupled inductor design. In terms of electrical performance, the two key constraints based on the target application of the coupled inductor are the steady-state inductance and the transient, or leakage, inductance. In regards to efficiency, the inductor loss comes from the wind-

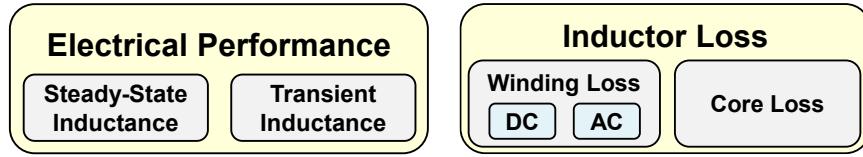


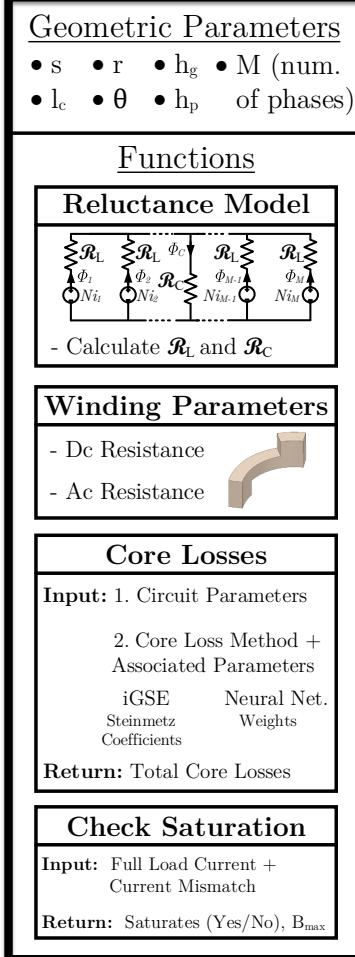
Figure 4.10: Main metrics for coupled inductor optimization. The steady-state inductance, transient inductance, and inductor loss have highly interrelated tradeoffs that need to be balanced depending on the end application.

ings, with loss due to the dc current component and ac current component, as well as losses from the magnetic core.

Each of these parameters in the final inductor design impact the overall efficiency, size, and speed of the system:

1. **Size:** Generally, larger magnetic size, which can manifest itself in larger flux path cross-sectional areas and taller height, results in higher inductance. Larger cross-sectional areas reduce the flux density throughout the core, which can increase the amount of current that a magnetic component is rated for as well as reduce core loss. For vertical power delivery, the goal is to minimize the height as much as possible, while achieving high density ( $\text{A/mm}^2$  and  $\text{W/in}^3$ ) and low loss.
2. **Speed:** A lower inductance increases the slew rate at which the inductor can ramp up or ramp down its current. Faster inductor slew rate can reduce the size of the output capacitors. However, low inductance increases the current ripple, increasing the ac conduction losses. Higher frequencies can be used to improve the control bandwidth, and reduce the current ripple, but the loss mechanisms of magnetic components tend to scale poorly with increasing frequency.
3. **Performance:** Losses in an inductor are composed of static core losses, which are relatively constant throughout the entire load current operation range, and copper losses, which consist of both dc and ac winding losses and scale in proportion to the square of the current. In a fixed 3D volume, reserving more

## Magnetic Geometry



## Optimization Flowchart

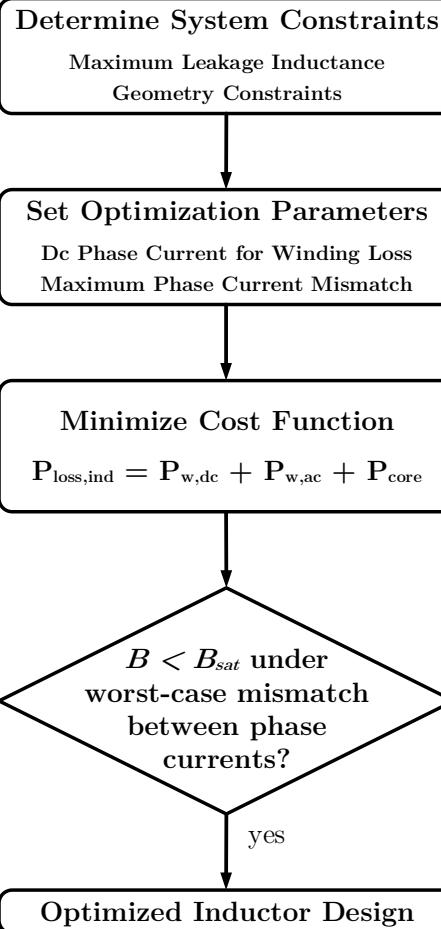


Figure 4.11: Structure and flowchart for the vertical coupled inductor optimization routine. The design of the inductor is constrained by the maximum leakage inductance and the dimension. The optimization goal is the winding loss, core loss, and the core saturation margin against phase current imbalance.

space for copper can reduce winding losses, but can increase the magnetic core losses. The volume needs to be optimally allocated to minimize the overall losses at the load current values of greatest significance. Losses tend to increase with frequency, as previously mentioned.

A systematic optimization for the geometric parameters can help minimize the losses, maximize the power density, and maintain the desired transient response [80].

A generalized optimization framework for multiphase coupled inductors is summarized in Fig. 4.11. Once a magnetic geometry is described with parameters, the inductor loss, ripple current, and transient inductance can be calculated to obtain a design with minimized loss subject to specified constraints. To calculate the winding loss, the following formula is used:

$$P_w = I_{dc}^2 R_{dc} + I_{ac,rms}^2 R_{ac}. \quad (4.10)$$

The power loss per unit volume (in units of kW/m<sup>3</sup>) in the core is usually calculated using Steinmetz's Equation ( $P_v = kf^\alpha \hat{B}^\beta$ ), where  $f$  is the frequency of the excitation (in kHz),  $\hat{B}$  is the peak flux density, and  $k$ ,  $\alpha$ , and  $\beta$  are constants referred to as the Steinmetz coefficients, often provided by the material manufacturer. In coupled inductors, where the current waveforms are irregular piece-wise-linear waveforms, the Steinmetz equation cannot be directly used. The "Generalized Steinmetz Equation" first presented in [93] and later improved in [94] (termed the "improved Generalized Steinmetz Equation," or iGSE) are used to predict the core loss. The only input parameters needed are the Steinmetz coefficients. For each linear time segment, the power loss per unit volume can be calculated as

$$\bar{P}_v = \frac{k_i(\Delta B)^{\beta-\alpha}}{T} \sum_m \left| \frac{B_{m+1} - B_m}{t_{m+1} - t_m} \right|^\alpha (t_{m+1} - t_m), \quad (4.11)$$

where

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos \theta|^\alpha 2^{\beta-\alpha} d\theta}. \quad (4.12)$$

In this dissertation, the iGSE is the method employed to calculate the core losses for optimization. Other core loss calculation methods are applicable, such as machine learning methods that might increase the overall optimization complexity but improve the calculation accuracy [95].

The next step is to set constraints on the magnetic design. Constraints are placed on the overall inductor volume, which defines the 3D cubic area that the magnetic component must fit within. In terms of electrical performance, the operating condition is specified by the input voltage  $V_{in}$ , output voltage  $V_{out}$ , number of phases  $M$ , phase current  $I_\Phi$ , and switching frequency  $f_S$ . The phase current at which the core is optimized for greatly impacts the optimal design. If performance at lighter loads is more significant, inputting a phase current to the optimization routine that is around 30% of the targeted full load current will steer the optimization to reduce the core losses at the expense of dc resistance, which leads to higher winding losses at full load. For designs in which the output current varies significantly during normal operation, one can consider using a weighted average cost function for the winding loss across the entire load range, or adding additional constraints to ensure that any selected design meets the targeted performance at specified load currents for thermal considerations.

With the converter parameters and constraints set, a nonlinear optimization (such as *fmincon* in MATLAB) is conducted to minimize the total inductor loss. A saturation check is placed to ensure that the selected core design does not exhibit saturation under the full load operating condition, setting an upper bound on the maximum tolerable flux equal to 80% of the  $B_{sat}$  value provided by the manufacturer at 100 °C to avoid any reduction in the permeability. A worst-case current mismatch can also be specified as a constraint. For balanced dc currents, where each phase current in the coupled inductor has the same dc value, the dc flux generated by each winding is equal. This results in the best scenario for dc flux cancellation with the lowest flux throughout the core. In the presence of a mismatch between phase currents, certain regions of the core may have higher dc flux than others, which can result in a portion of the core entering saturation. Generally, a tolerance of around 10% mismatch is sufficient to ensure robust operation against current mismatch.



Figure 4.12: Pictures of the designed inductors in this chapter. As the switching frequency increases from 1 MHz to 1.5 MHz to 2 MHz, geometric optimizations are conducted to reduce the magnetic height and enable in-packing vertical power delivery with reduced interconnect length.

This generalized optimization routine is employed in the remainder of this chapter to optimize three vertical coupled inductor structures, each for different applications. Figure 4.12 shows the three inductors designed. As the switching frequency increases, geometry modifications and optimizations enable a reduction in both the height and size of the overall inductor volume, progressing the vision of in-packaging vertical power delivery where every unit cube of volume within the magnetic component is optimized to bring about the desired performance and functionality.

## 4.4 1 MHz Vertical Coupled Inductor

This section details the design and fabrication of a 1 MHz four-phase coupled inductor for the initial vertical stacked LEGO-PoL prototype, detailed in Section 3.4.

### 4.4.1 Inductor Geometry

A four-phase coupled inductor is designed in order to facilitate vertical power delivery in the LEGO-PoL converter while providing a current source to soft charge the flying capacitors. Figure 4.13a shows a parameterized drawing of the top view and side view of a single piece of the designed coupled inductor.

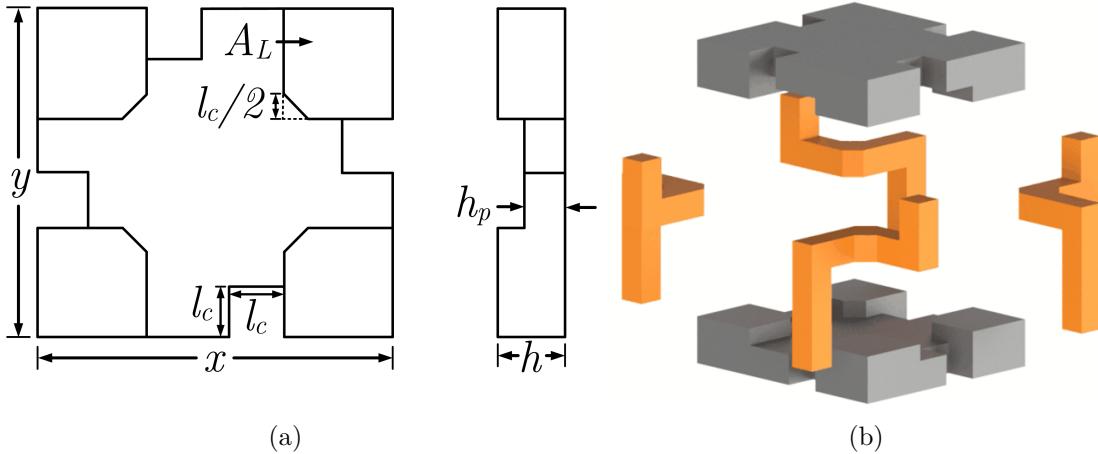


Figure 4.13: (a) Key design parameters for the vertical four phase coupled inductor including:  $x$  – width,  $y$  – length,  $l_c$  – cutout size,  $A_L$  – leg area,  $h$  – core height, and  $h_p$  – plate thickness. (b) Assembly procedure for the full four-phase vertical coupled inductor. Two pieces of this core and four copper windings form a complete EE assembly.

The parameterized dimensions that determine the inductor geometry include:

- $x$  and  $y$ : The length and width of the overall core, which determines the overall footprint and current area density.
- $A_L$ : The cross-sectional area of the corner posts of the inductor. This cross-sectional area determines the reluctance value  $\mathcal{R}_L$  in the reluctance model shown in Figure 4.7.
- $l_c$ : The depth of the cutouts created next to the corner posts. These cutouts are inserted such that the copper winding can be fit to wrap around the corner post while keeping the entire magnetic component contained within a rectangular prism.
- $h_p$ : The “plate height”, or the height of ferrite material other than the corner posts. Flux moves laterally between corner posts through this center region, and this parameter impacts the cross-sectional area of the flux that traverses through the center.

- $h$ : Overall height of the core piece including the height of the corner posts. The air gap in the center in between two core pieces assembled in an EE configuration is equal to  $2(h - h_p)$ .

The coupled inductor is designed as a two piece assembly. Often referred to as an “EE” assembly, two identical core pieces are used, alongside four copper windings, and assembled as depicted in Figure 4.13b. The entire inductor assembly constitutes a rectangular prism, with four terminals on the bottom of the component and four terminals on the top of the component. The four bottom terminals are connected to the separate buck converter phases, while the top terminals are connected to a motherboard which shorts the four terminals together to the output node.

#### 4.4.2 Inductor Design

Table 4.1 summarizes the converter parameters and constraints defined by the vertical stacked LEGO-PoL converter for optimizing the inductor. The volumetric constraints are determined by the power stage layout of the converter, leaving a possible 12 mm × 16 mm area for the inductor. The maximum height of the entire two-piece assembly was constrained to 5.5 mm, with an effort to minimize the height.

The buck converters in the LEGO-PoL prototype take in a nominal 8 V dc input and step down the voltage to 1 V at the output. The coupled inductor is designed for a nominal duty cycle of  $D = 0.125$ . The switching frequency of the buck converter is 1 MHz. The target full-load phase current is 65 A per phase. Due to the high current operation, the target dc resistance is set to be below 0.1 mΩ. The maximum allowable leakage inductance is determined by

Given a 2% transient voltage requirement, a 1 A/ns output current slew rate, and an output capacitance of 6 mF, a leakage inductance  $L_\ell = 25$  nH was selected. Given a 2% transient voltage requirement with an output capacitance of 6 mF and a 1 A/ns output current slew rate, a leakage inductance of  $L_\ell \leq 25$  nH was set as a constraint.

Table 4.1: 1 MHz Inductor Optimization Parameters and Constraints  
**Volumetric Constraints**

Description	Symbol	Value
Length	$x$	$\leq 12 \text{ mm}$
Width	$y$	$\leq 16 \text{ mm}$
Height	$2 \times (h_p + h_g)$	$\leq 5.5 \text{ mm}$

**Electrical Parameters**

Description	Symbol	Value
Input Voltage	$V_{in}$	8 V
Output Voltage	$V_{out}$	1 V
Switching Frequency	$f_s$	1 MHz

**Electrical Constraints**

Description	Symbol	Value
Dc Resistance	$R_{dc}$	$\leq 0.1 \text{ m}\Omega$
Full-Load Phase Current	$I_{out}/4$	65 A
Per-Phase Current Ripple	$\Delta i_\Phi$	$\leq 12 \text{ A}$
Per-Phase Leakage Inductance	$L_\ell$	$\leq 25 \text{ nH}$

The next step in designing the inductor is to select a suitable material. Selecting the proper magnetic material to use is highly application dependent. The primary factors that influence material selection are the frequency range of operation, the maximum peak-to-peak flux density, the saturation flux density of the material, and the relative permeability of the material [96]. The two main classes of magnetic materials that are most suitable for 48-V VRM applications are **MnZn** ferrites and **NiZn** ferrites.

- **MnZn** power ferrites are suitable for low- to medium-power applications in the frequency range of 10 kHz to 5 MHz [97,98]. These materials have high relative permeabilities (500-3000), saturation flux densities in the range of 400-600 mT, and low power loss. Their low electrical resistivity values limit their application at higher switching frequencies.

Table 4.2: Properties of Ferroxcube 3F4 Material

Parameter	Symbol	Value
Relative Permeability	$\mu_r$	900
Saturation Flux Density (100 °C)	$B_{\text{sat}}$	350 mT
Core Loss Constant	$k$	$1.2 \times 10^{-4}$
Frequency Exponent	$\alpha$	1.7
Flux Density Exponent	$\beta$	2.7
Constant for Equation (4.11)	$k_i$	$4.961 \times 10^{-6}$

- **NiZn** ferrites are suitable for high switching frequency ranging from 5 MHz to 500 MHz [99]. They have high values of electrical resistivity, which limits their eddy current losses. Their relative permeabilities, in the range of 10-100, and their saturation flux densities, in the range of 200-400 mT, are lower than MnZn ferrites.

Current 48-V VRM designs switch at frequencies typically ranging from 100 kHz to 2 MHz. As semiconductor device technology improves and devices that can switch at high frequencies while handling high currents with low loss, designers will leverage higher switching frequencies to further miniaturize the capacitors and magnetic components in their systems. For now, MnZn ferrites are the best fit for most 48-V VRM designs. Ferroxcube 3F4 is selected for the 1 MHz vertical coupled inductor.

Table 4.2 summarizes the material properties.

Given the material and the constraints, the optimal values for the remaining free parameters can be determined as per the optimization framework outlined in Section 4.3. A fixed dc current of 20.8 A per phase is used to calculate the winding loss, as this is the thermal design point of the vertical stacked LEGO-PoL converter, roughly 1/3 of the full load current under air cooling. The selected design is summarized in Table 4.3. The selected design has a 12 mm × 13 mm × 5.25 mm geometry, with a side leg area of 16 mm<sup>2</sup>. The thickness of the top and bottom plates is

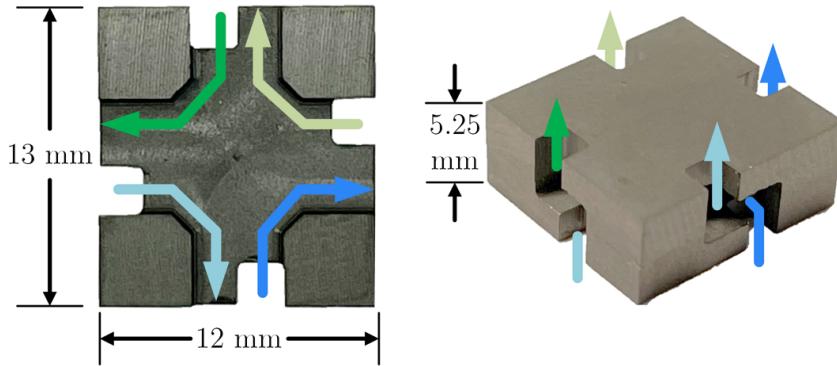


Figure 4.14: Picture of the fabricated inductor design. The windings fit within the footprint of the core and enable vertical power delivery.

Table 4.3: Geometric Parameters of Designed 1 MHz Vertical Coupled Inductor

Description	Symbol	Value
Length	$x$	12 mm
Width	$y$	13 mm
Total Height	$h$	5.25 mm
Plate Height	$h_p$	1.7 mm
Winding Cutout Length	$l_c$	2 mm
Side Leg Area	$A_L$	16 mm <sup>2</sup>

1.7 mm. The resulting calculated reluctances of the core are  $\mathcal{R}_L = 1.02 \times 10^6 \text{ H}^{-1}$  and  $\mathcal{R}_C = 20 \times 10^6 \text{ H}^{-1}$ , and the calculated leakage inductance is  $L_\ell = 12.4 \text{ nH}$ . The coupling coefficient  $\beta$  is 78. The phase current ripple  $\Delta i_\Phi$  is 7.24 A. The dc winding resistance is 0.087 mΩ and the ac winding resistance is 4.8 mΩ. The calculated core loss is 0.242 W. The fabricated optimized core is pictured in Figure 4.14.

A trade-off arises on how to best use the available volume to reduce both core and winding loss. Higher cross-sectional area for the core reduces the flux density and reduces the core loss, but may lead to higher conduction loss in windings. This trade-off can be visualized with the contour plot of Figure 4.15. This plot is shown for the optimal  $x$ ,  $y$ ,  $l_c$ , and  $h_p$  for a coupled inductor subject to the parameters in Table 4.3. At the optimal point, the leg cross-sectional area  $A_L$  and the total height

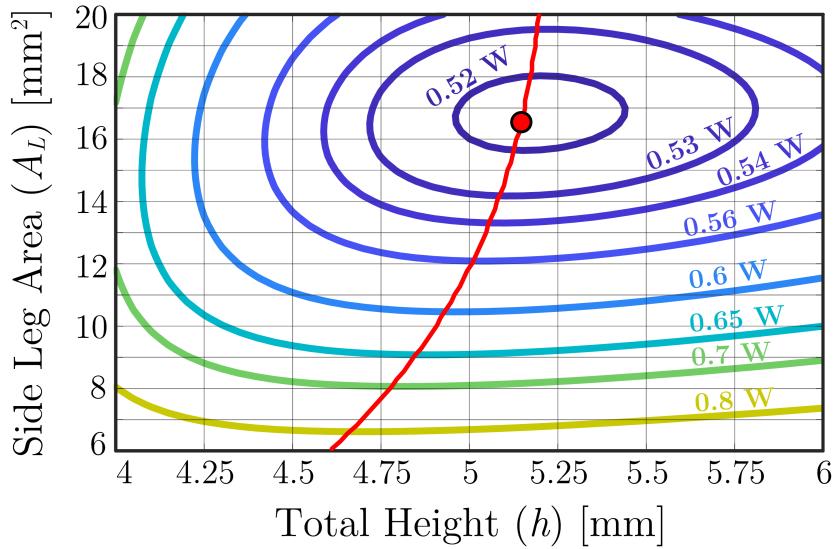


Figure 4.15: Contour plot of the coupled inductor in 4.13 with  $x = 12 \text{ mm}$ ,  $y = 13 \text{ mm}$ ,  $h_p = 1.7 \text{ mm}$ , and  $l_c = 2 \text{ mm}$ . The total height  $h$  is varied from 4 mm to 6 mm and is plotted on the x-axis, and the side leg area  $A_L$  is varied from 6  $\text{mm}^2$  to 20  $\text{mm}^2$  and is plotted on the y-axis. The contours visualize the total inductor loss. The red line indicates the optimal height for each cross-sectional side leg area that minimizes the inductor loss. The optimal design is marked by the red dot.

$h$  of the core are swept to produce a contour of the inductor loss. For a selected cross-sectional side leg area  $A_L$ , the red line represents the optimal height. By increasing the height beyond this point, the benefits achieved in reducing the winding loss are outweighed by the increase in core loss. Likewise, decreasing the height beyond this point increases the winding loss at a rate higher than the core loss is reduced. The optimal design which has the lowest loss has a side leg area  $A_L$  of 16.5  $\text{mm}^2$ , and a total height of 5.15 mm.

#### 4.4.3 Evaluation

The fabricated coupled inductor with dimensions listed in Table 4.3 is shown in Figure 4.16. Four copper windings are milled with computer numerical control (CNC) to fit within the winding cutouts and form a quarter-turn around the corner leg post. Current is delivered from bottom to top and facilitate compact vertical power delivery.

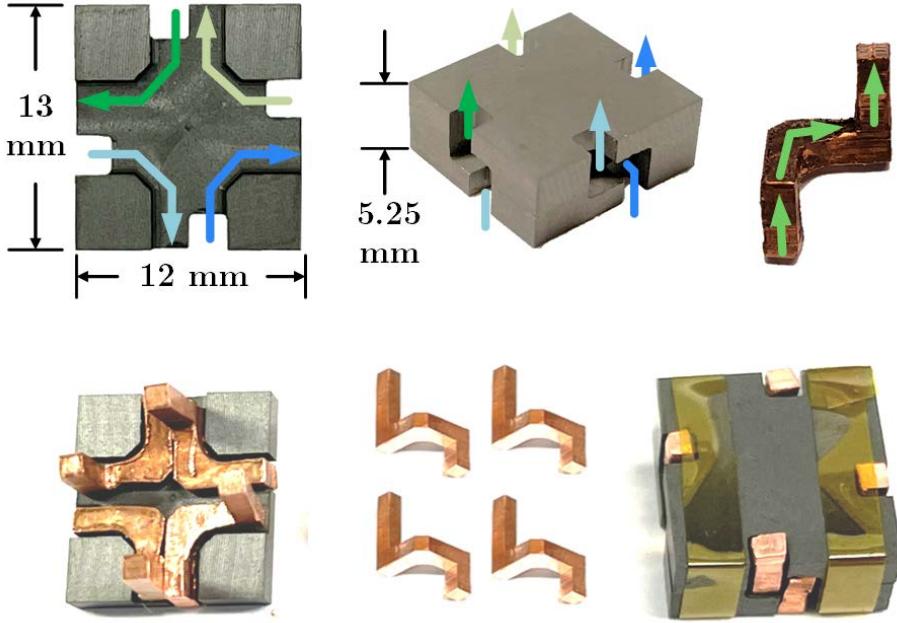


Figure 4.16: Picture of the vertical four-phase coupled inductor magnetic core. Four machined copper windings make a 90° rotation within the core and deliver current from bottom to top. Cutouts in the core shorten the conduction path and facilitate the winding placement within the core.

ery. This coupled inductor is designed to be able to handle a phase current mismatch of 10% of the full load current (65 A per phase) without saturation.

The inductor is characterized using an HP/Agilent 4395A impedance analyzer. In order to extract the values of  $\mathcal{R}_L$  and  $\mathcal{R}_C$ , two impedance measurements are taken. First, an  $N$ -turn winding is configured around one of the side legs. This impedance represents the self inductance  $L_S$  of one winding. Next, by configuring  $N$ -turn windings around each of the side legs and connecting them in parallel at their inputs and outputs, the overall leakage inductance  $L_\ell/M$  can be measured. Based on the measurement results,  $\mathcal{R}_L$  and  $\mathcal{R}_C$  can be experimentally determined using the following equations:

$$\mathcal{R}_L = \frac{N^2(M - 1)}{ML_S - L_\ell}, \quad (4.13)$$

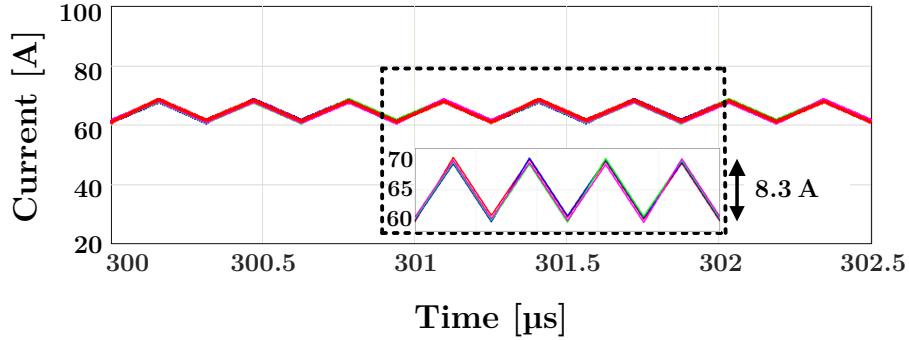


Figure 4.17: Simulation of the four-phase coupled inductor using measured inductance parameters for a four-phase buck converter with  $V_{in} = 8$  V,  $V_{out} = 1$  V,  $I_{\Phi,DC} = 65$  A, and  $f_s = 1$  MHz. The peak-to-peak current ripple is 8.3 A and the effective ripple current frequency is 4 MHz.

$$\mathcal{R}_C = \frac{N^2(L_S - L_\ell)}{ML_\ell(L_S - \frac{L_\ell}{M})}. \quad (4.14)$$

These equations are re-arrangements of Equations (4.4) and (4.6). The measured self inductance is 793.8 nH and the measured overall leakage inductance is 4.36 nH. The resulting measured reluctance values are  $\mathcal{R}_L = 0.95 \times 10^6$  H<sup>-1</sup> and  $\mathcal{R}_C = 14.1 \times 10^6$  H<sup>-1</sup>. From these, the leakage inductance per phase is 17.4 nH and the steady-state inductance is 105 nH at  $D = 0.125$ , which results in a peak-to-peak phase current ripple of 8.3 A at 1 MHz.

Figure 4.17 shows the simulated current waveforms of the four-phase coupled inductor. The simulation was conducted using the measured inductance values to represent the inductor. Each phase carries 65 A of dc current and the four-phase buck converter has an input voltage of 8 V, output voltage of 1 V, and the switching frequency is 1 MHz. The per-phase current ripple is 8.3 A peak-to-peak, matching calculations. One point of observation is that, as compared to a discrete inductor with no coupling, where the inductor current ramps up during the time when the high side switch for its phase is on and ramps down during the remainder of the time within a switching period, the current in each phase of the coupled inductor ramps up

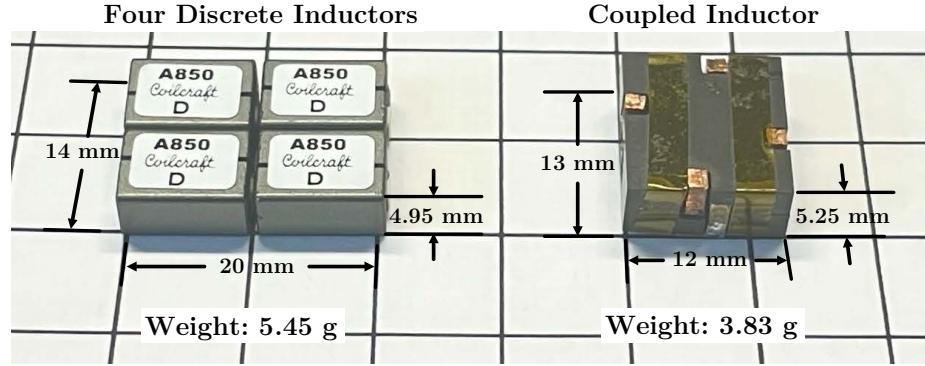


Figure 4.18: Comparison of the coupled inductor with four discrete Coilcraft SLR1050A 85 nH discrete inductors. A comparison of the two solutions is presented in Table 4.4. The coupled inductor has a smaller leakage inductance and overall system transient inductance, lower dc resistance per phase, and lower core loss, while enabling vertical power delivery. The two options have similar phase current ripples. The volume of the three coupled inductors is only 57.7% of that of the twelve discrete inductors, with only 25% of the dc resistance.

Table 4.4: Comparison Between Vertical Coupled Inductor and Four Discrete Inductors

Description	Symbol	Discrete	Coupled
Leakage Inductance	$L_\ell$	85 nH	12.4 nH
Phase dc Resistance	$R_{dc}$	0.39 mΩ	0.09 mΩ
Core Loss	$P_c$	0.53 W	0.15 W
Phase Current Ripple	$\Delta i_p$	10.3 A	8.3 A
Total Volume	V	4.24 cm <sup>3</sup>	2.45 cm <sup>3</sup>

when any of the four phases is turned on. This results in an effective ripple current frequency equal to four times the switching frequency, in this case, 4 MHz.

Figure 4.18 shows a picture of the fully assembled coupled inductor against four Coilcraft SLR1050A 85 nH discrete inductors. These off-the-shelf inductors were chosen for comparison as they have a similar inductance as the steady-state inductance of the coupled inductor, which means the phase current ripple would be approximately the same with both solutions. A side-by-side comparison of the two solutions is presented in Table 4.4. The coupled inductor achieves a much lower leakage inductance

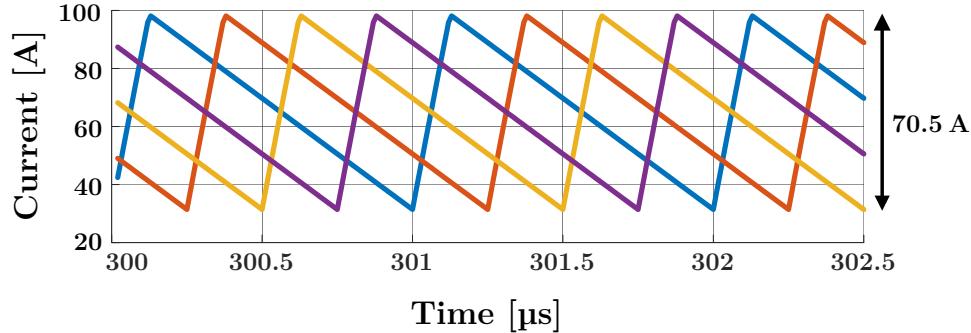


Figure 4.19: To achieve the same transient performance as the four-phase coupled inductor, discrete non-coupled inductors with their value equal to  $L_\ell$ , or 12.4 nH, need to be used. This plot shows the simulated per-phase current ripple with four 12.4 nH discrete inductors; a ripple of 70.5 A peak-to-peak is seen, which would result in large ac conduction losses and significantly lower system efficiency.

while maintaining a similar peak-to-peak phase current ripple as the discrete inductor solution. It also has four times lower dc resistance as well as lower core loss. The volume of the coupled inductor is only 57.7% of that of the four discrete inductors. To achieve the transient current speed using non-coupled discrete inductors, four 12.4 nH discrete inductors must be used. This would yield a 70.5 A peak-to-peak phase current ripple, as simulated and plotted in Figure 4.19.

Table 4.5 summarizes the metrics of the fabricated 1 MHz coupled inductor. This table presents two metrics for inductance and coupling evaluation: inductance density and  $\gamma|_{D=0.25}$ . The inductance density is calculated by taking the sum of the diagonal elements in the inductance matrix of the coupled inductor (in this case,  $L_{S1} + L_{S2} + L_{S3} + L_{S4}$ ) and dividing this by the inductor volume. To evaluate the coupling strength, since this metric varies with duty cycle,  $D = 0.25$  is selected as the point of evaluation for this metric to remain consistent throughout this chapter when evaluating designs. As defined in Equation (4.8), this is evaluated by taking the leakage inductance  $L_\ell$  and dividing it by the steady-state inductance evaluated at  $D = 0.25$ . A lower number indicates less energy storage and higher magnetic coupling.

Table 4.5: Summary of Metrics for 1 MHz Coupled Inductor

Year	Inductor Reference	Size			Inductance		Winding Resistance	Phase Current*	Phase Count	Operation Frequency
		Length	Width	Height	Inductance Density †	$\gamma _{D=0.25}‡$				
2021	1 MHz LEGO-PoL	12 mm	13 mm	5.25 mm	3.86 $\frac{\text{nH}}{\text{mm}^3}$	0.166	0.09 mΩ	65 A	4	1 MHz

† Inductance density is calculated using the sum of the self inductances of all of the phases divided by the overall box volume of the inductor:  $\Sigma_i (L_{S,i}) / l \times w \times h$ .

‡  $\gamma|_{D=0.25}$  is equal to the per-phase leakage inductance over the per-phase steady state inductance evaluated at D=0.25:  $L_\ell / (L_{pss}|_{D=0.25})$ . A lower number indicates higher magnetic coupling.

\* The per-phase current denotes the maximum phase current that was experimentally achieved in the testing of the inductor.

The fabricated four-phase coupled inductor is able to achieve high current rating, while improving upon all three key metrics compared to a discrete inductor solution. It improves in size by reducing the total occupied volume and area; it improves in efficiency by reducing the dc resistance and core losses; it improves the transient performance for the same peak-to-peak phase current ripple by introducing magnetic coupling and reducing the leakage inductance by a factor of 7 compared to the steady-state inductance. However, the fabricated coupled inductor occupies roughly one-third of the volume contributes one-third of the system height in the initial vertical stacked LEGO-PoL prototype. To implement in-packaging vertical power delivery, where the VRM is mounted underneath the processor, the overall system height needs to be reduced. For the Mini-LEGO design, a new inductor design and optimization is needed to reduce the height of the vertical coupled inductor.

## 4.5 1.5 MHz Vertical Coupled Inductor

This section details the design and fabrication of a 1.5 MHz four-phase coupled inductor for the high density Mini-LEGO prototype, detailed in Section 3.5. The height of the coupled inductor in the LEGO-PoL design was 5.25 mm. The Mini-LEGO implementation reduces its height by over half to 2.5 mm through a systematic re-design and optimization.

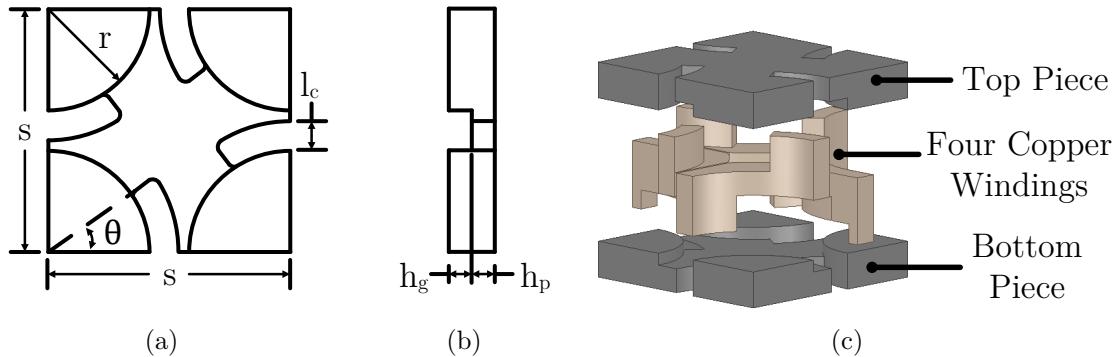


Figure 4.20: (a) Top view and (b) side view of the vertical coupled inductor structure highlighting the geometric parameters used for optimization. (c) Vertical coupled inductor two-piece assembly, illustrating the copper winding positioning between the top and bottom magnetic core pieces.

#### 4.5.1 Inductor Geometry

Figure 4.20a-b shows the novel fully parameterized four-phase vertical coupled inductor structure designed for the Mini-LEGO converter. The structure is designed to be a two-piece assembly, with the windings placed in between the two core pieces as demonstrated in Figure 4.20c. For a design with four phases, such as the one presented in this section, the inductor can be either square or rectangular in shape, with outer legs on each of the four corners. This design can be extended to higher number of phases by changing the shape of the overall inductor.

The primary geometrical change between the Mini-LEGO inductor and the inductor in Section 4.4 is the modification of the winding cutout. The parameter  $\theta$ , which is defined as the angle between the edge of the core and the radial cutout in which the winding is inserted, enables designs that can trade-off between winding resistance and core losses. Figure 4.21 shows the effect of different values of  $\theta$ . For small values of  $\theta$ , the winding makes a quarter-turn around the core leg post, while the flux traverses from the center of the bottom core piece through the individual legs and up to the top core piece. As  $\theta$  increases beyond  $45^\circ$ , the current travels vertically through the winding, while the magnetic core “wraps” around it. Higher

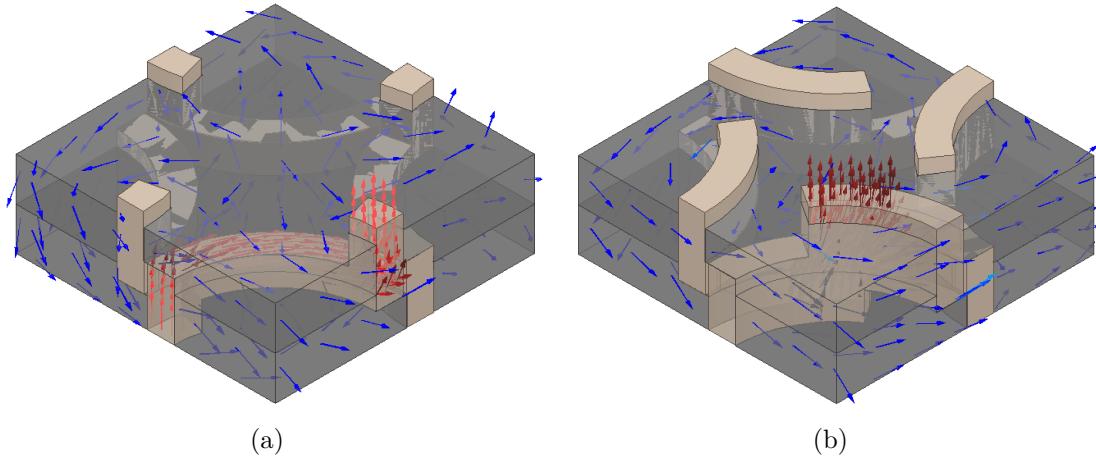


Figure 4.21: Demonstration, using ANSYS Maxwell 3D, of how varying  $\theta$  impacts the current and flux distribution for (a)  $\theta = 15^\circ$  and (b)  $\theta = 57^\circ$ . The blue arrows on the magnetic core pieces show the flux density, and the red arrows on the winding show the current density.

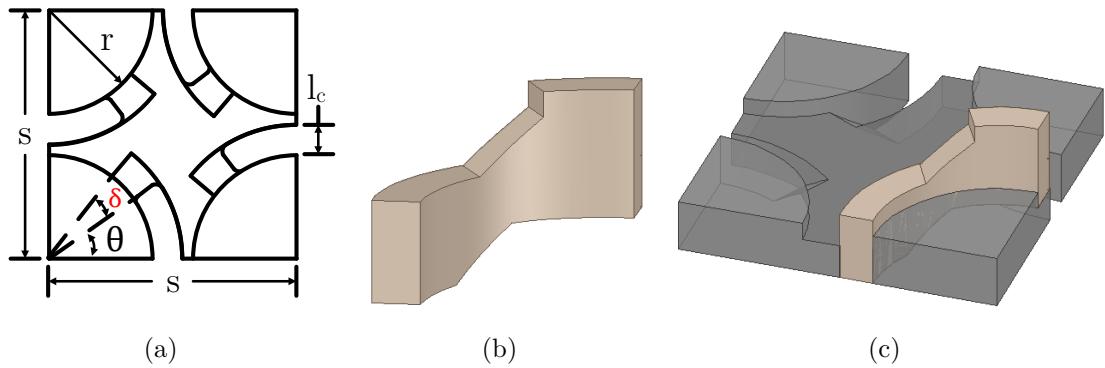


Figure 4.22: (a) Top view of vertical coupled inductor structure with the addition of  $\delta$ . (b) Winding design, with angled copper for continuous conduction path. (c) Winding placement within the magnetic core.

values of  $\theta$  can substantially reduce the dc resistance of the windings. With a fixed cutout size, as in the coupled inductor design presented in Section 4.4, the primary way to reduce the dc resistance is to increase height between the top and bottom core plates, denoted as  $h_g$  in Fig. 4.20b. Adding a parameter in  $\theta$  to effectively shorten the overall winding path increases design flexibility and enables another way to reduce the dc resistance without directly contributing to overall inductor height.

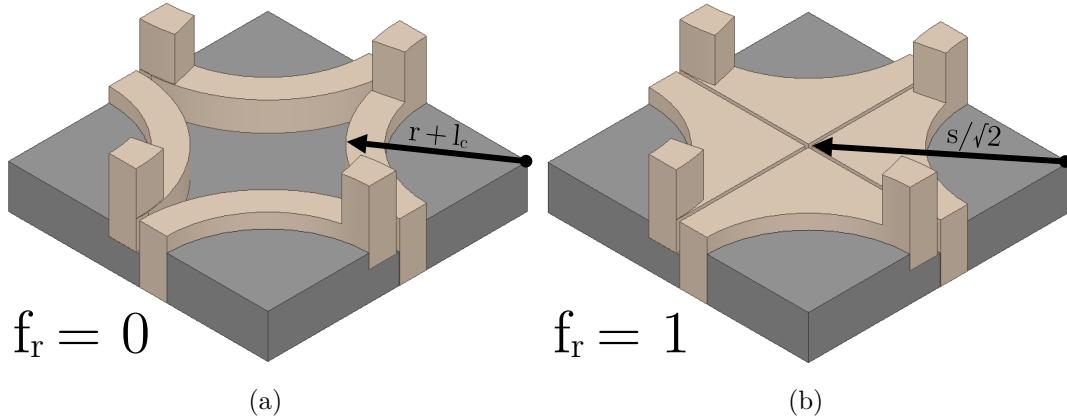


Figure 4.23: The winding fill factor parameter  $f_r$  at (a) its minimum condition of  $f_r = 0$  and (b) its maximum condition at  $f_r = 1$ . The fill factor parameter is independent of the core geometry and can be used to further fine tune the per-phase transient inductance and dc resistance of the coupled inductor after the core is manufactured.

An additional parameter, denoted as  $\delta$ , can be introduced as well to further influence the winding design. Figure 4.22 illustrates this parameter and the effect it can have on the winding design. This parameter defines a chamfer in the cutout, from the bottom to the top of the magnetic core piece (with a height of  $h_p$ ), starting at the end of the cutout and ending at an angle of  $\theta + \delta$ . This results in an angled winding design that removes the sharp 90 degree corners and improves the current density distribution throughout the winding. For the inductors used in the Mini-LEGO converter, this parameter was excluded.

Another additional parameter that modifies the copper winding design as compared to the inductor of Section 4.4 is added. This parameter, denoted as  $f_r$ , or the fill factor ratio, is independent of the magnetic geometry and is a function of the copper winding geometry. Copper blocks the passage of ac flux, and in this geometry, where the copper is placed in the air gap between the top and bottom plates, the presence or absence of copper can confine the ac flux to a certain area. Figure 4.23 illustrates this concept. A fill factor ratio of 0 means the winding does not exceed the radius of  $r + l_c$ , when measured from the corner of the magnetic core. A fill factor ratio of 1

Table 4.6: 1.5 MHz Inductor Optimization Parameters and Constraints  
**Volumetric Constraints**

Description	Symbol	Value
Length	$x$	$\leq 9$ mm
Width	$y$	$\leq 9$ mm
Height	$2 \times (h_p + h_g)$	$\leq 2.5$ mm
<b>Electrical Parameters</b>		
Description	Symbol	Value
Input Voltage	$V_{in}$	8 V
Output Voltage	$V_{out}$	1 V
Switching Frequency	$f_s$	1.5 MHz
<b>Electrical Constraints</b>		
Description	Symbol	Value
Dc Resistance	$R_{dc}$	$\leq 0.2$ mΩ
Full-Load Phase Current	$I_{out}/4$	20 A
Per-Phase Current Ripple	$\Delta i_\Phi$	$\leq 10$ A
Per-Phase Leakage Inductance	$L_\ell$	$\leq 12$ nH

means the winding fills in the remaining area. This parameter can be adjusted after the design is completed to further tune the transient inductance to its desired value.

### 4.5.2 Inductor Design

The parameters for the design are summarized in Table 4.6. DMR53, a MnZn ferrite from Hengdian Group DMEGC Magnetics Co., is used as the magnetic material for this inductor design. The key material parameters are listed in Table 4.7. The provided parameters at 100°C are used for the optimization procedure. Given these fixed parameters, the optimal values for the remaining free parameters can be determined to minimize the inductor loss. Parameters are constrained to ensure the finalized design meets the specified targets. Constraints on the  $x$  and  $y$  dimensions are dictated by the converter layout, which limits both to a maximum of 9 mm. Adding

Table 4.7: Properties of DMR53 Material

Parameter	Symbol	Value
Relative Permeability	$\mu_r$	900
Saturation Flux Density (100 °C)	$B_{\text{sat}}$	460 mT
Core Loss Constant	$k$	$2.07 \times 10^{-10}$
Frequency Exponent	$\alpha$	2.31
Flux Density Exponent	$\beta$	2.68
Constant for Eqn. ((4.11))	$k_i$	$4.856 \times 10^{-12}$

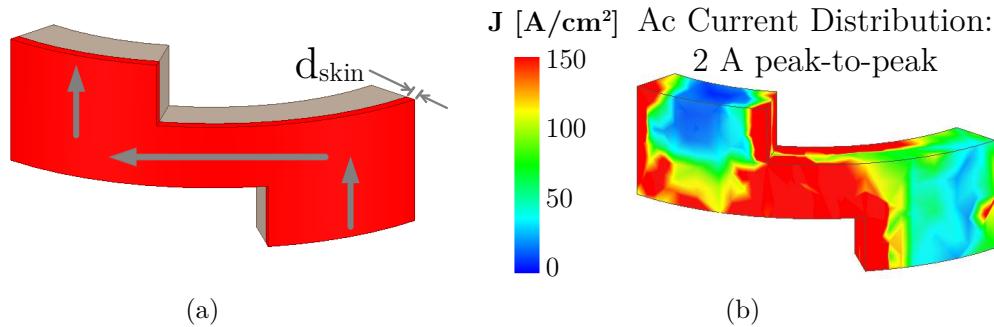


Figure 4.24: (a) Approximation of the ac winding resistance for the vertical coupled inductor structure in Figure 4.20 used in the optimization to compute the ac winding loss. It is assumed that the ac current only flows through the outer surface of the conductor. (b) ANSYS Maxwell 3D Eddy Current simulation of the current density distribution of one of the windings. Each winding is excited with a sinusoidal ac current of 2 A peak-to-peak at a frequency of 1.5 MHz.

a constraint on the maximum total height  $h$  of the inductor of 2.5 mm, or no more than 30% of the overall system height, restricts the design space to include inductors with a volume no larger than 203 mm<sup>3</sup>. Constraints are also added to the electrical properties of the coupled inductor, such as the maximum tolerable phase current ripple or output current ripple as well as the maximum tolerable transient inductance. A constraint was added to this design, which sets the maximum allowable per-phase leakage inductance to 12 nH and the maximum allowable per-phase current ripple to 10 A.

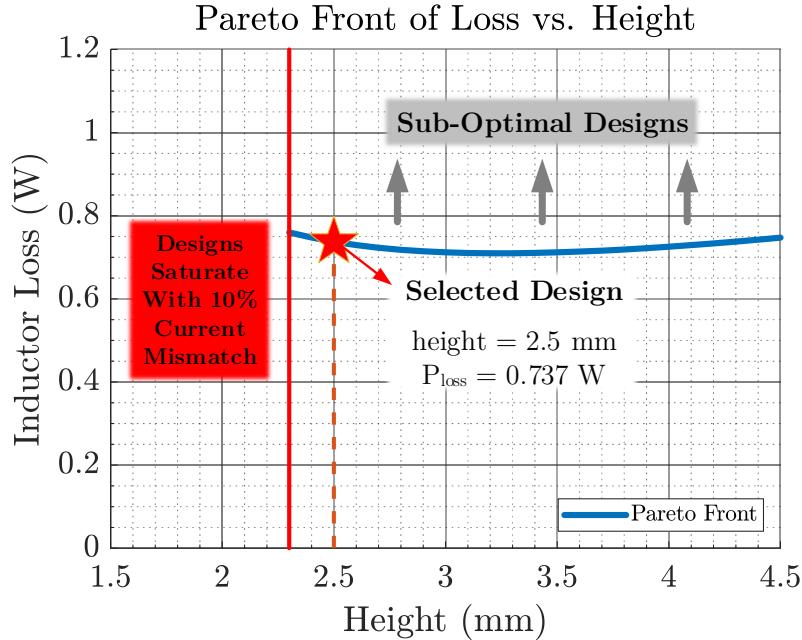


Figure 4.25: Results of the optimization routine for the vertical coupled inductor showing the Pareto front of the inductor loss vs. its height. The optimization is performed at a dc current of 20 A per phase and a switching frequency of 1.5 MHz. The selected height of the vertical coupled inductor for Mini-LEGO is 2.5 mm, resulting in an estimated loss of 0.737 W at full load.

As the Mini-LEGO converter is designed with a primary target of achieving high full load power density, a dc current of 20 A per phase is used to calculate the winding loss, as this is the thermal design point (TDP) of the Mini-LEGO converter. Due to the skin effect and the proximity effect, the ac current will flow on the outer edge of the winding, away from the magnetic material. Figure 4.24a shows how this is modeled. The ac resistance is calculated based on the skin depth for only the outer region of the winding. Figure 4.24b shows the current density from an Eddy Current simulation in ANSYS Maxwell 3D of the coupled inductor with each winding excited with a 2 A peak-to-peak sinusoidal ac current at 1.5 MHz. The current is concentrated primarily on the surface of the winding that is not interfacing with the magnetic material.

With the converter parameters and constraints set, the inductor is optimized to minimize the total loss. A saturation check is placed to ensure that the selected core design does not exhibit saturation under the full load operating condition, setting an

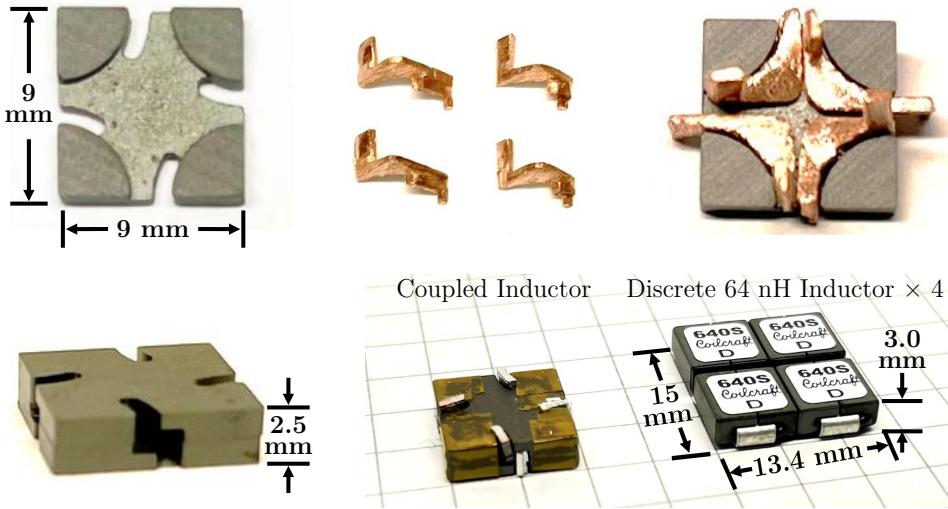


Figure 4.26: Pictures of the designed vertical coupled inductor along with the four copper windings. The windings were milled with a fill factor ratio  $f_r = 1$  (top right), and then later adjusted to the desired fill factor ratio  $f_r = 0$  (top middle). The coupled inductor is pictured next to four discrete 64 nH inductors. For a similar per-phase ripple current, the volume of the coupled inductor is 34% of the volume and has 0.5 mm less height than the four discrete inductors. The coupled inductor has a per-phase transient inductance of 10.3 nH, over six times lower than 64 nH.

upper bound on the maximum tolerable flux equal to 80% of the  $B_{\text{sat}}$  value provided by the manufacturer at 100 °C. Figure 4.25 shows the Pareto front of the coupled inductor loss against the total height of the inductor. Below a height of 2.3 mm, no designs satisfy the constraint of avoiding saturation in the core under a maximum 10% dc current mismatch. At lower heights, the optimization routine attempts to decrease  $\theta$  to reduce the core loss, however, reduced cross-sectional areas throughout the core causes larger core losses and larger overall losses. The minimum loss occurs when the height is 3.2 mm. A height of 2.5 mm was selected as a point that reduces the height while only marginally increasing the overall inductor loss when compared to the loss at 3.2 mm. As the height increases, the winding path increases, and the optimization routine increases  $\theta$  to compensate and reduce the winding resistance. This leads to the loss slightly increasing as the height is further increased.

Table 4.8: Geometric Parameters of Designed 1.5 MHz Vertical Coupled Inductor

Description	Symbol	Value
Length/Width	$s$	9 mm
Post Radius	$r$	3.5 mm
Cutout Length	$l_c$	0.95 mm
Plate Height	$h_p$	0.75 mm
Post Height	$h_g$	0.5 mm
Cutout Angle	$\theta$	33°
Fill Factor	$f_r$	0

Figure 4.26 shows the selected vertical coupled inductor design after optimization. The parameters and dimensions of the inductor are summarized in Table 4.8. Four copper windings are CNC milled and designed to connect with the multiphase buck board for an interposer-less design, with the coupled inductor resting directly on top of the top-side components. The windings were milled with a fill factor ratio  $f_r = 1$  (as shown in the top right of Figure 4.26), and then later adjusted to the desired fill factor ratio  $f_r = 0$ .

The coupled inductor was characterized to measure key inductance values when operating in the full system. Details on the measurement setup as well as extended measurement results are presented in the following section.

### 4.5.3 Coupled Inductor Characterization Methodology

While Section 4.4 discussed taking simple measurements to characterize vertical inductors, this subsection introduces an accurate and comprehensive characterization methodology for vertical coupled inductor converters. As vertical coupled inductors are part of a system that includes the vertical current return paths, the inductor (referred to as the device under test) is fully assembled into a test setup that mimics the real converter operation. Two measurements are taken to fully characterize the

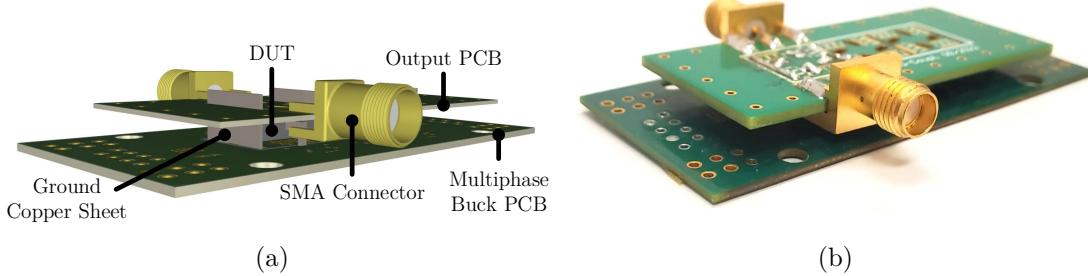


Figure 4.27: (a) Altium 3D Rendering of the test fixture assembly and (b) fully assembled test fixture with DUT in place. The DUT is connected to the multiphase buck board used in the Mini-LEGO converter. An output board is designed and connected to the DUT and ground copper sheets. Two SMA connectors are placed on the output board and used to interface with the vector network analyzer to conduct the measurements.

coupled inductor's electrical performance: the self inductance ( $L_S$ ), and the overall transient inductance ( $L_{otr}$ ). These two measurements are then used to determine the full inductance matrix, and thus the circuit performance of the coupled inductor.

A test fixture was designed to characterize the inductor's performance. Inductances along the winding path, such as the inductance contributed by the PCBs, contribute to the steady-state and transient performance of the inductor. The test fixture is designed to include all of these in the measurement setup. Figure 4.27a shows a rendering of the full assembly of the test fixtures for the DUT. The multiphase buck board (presented in Section 3.5) is placed on the bottom. The DUT is connected to the multiphase buck board in the same manner as it would be during normal converter operation. A new fixture was designed for the output connection, which is placed on top of the DUT and houses two SMA connectors. These connectors interface with a vector network analyzer (VNA) which is used to conduct the inductance measurements. The fully assembled test fixture assembly is shown in Fig. 4.27b.

The self inductance was measured by electrically connecting the switch node, which is connected to the inductor winding, to the ground pad of the DrMOS adjacent

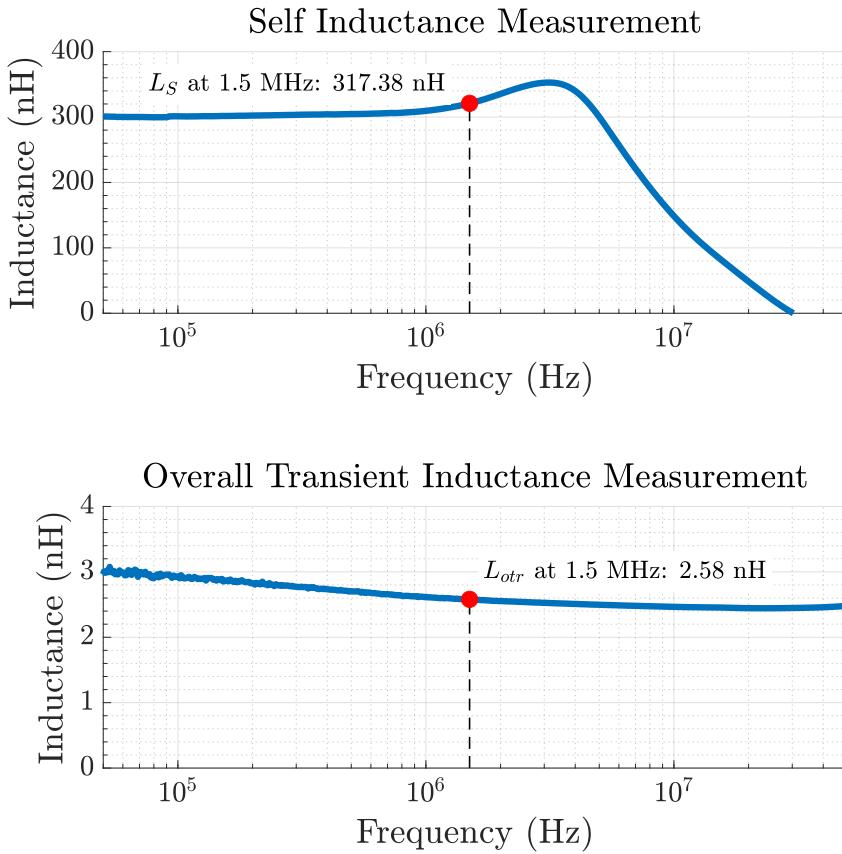


Figure 4.28: Measured data of the self inductance (top) and overall transient inductance (bottom) of the vertical coupled inductor. The self inductance is 317.38 nH at 1.5 MHz, and the overall transient inductance is 2.58 nH at 1.5 MHz. The measurements include parasitic inductances of PCBs and GND copper sheets on paths.

to the switch node to complete the signal path. The overall transient inductance is measured by connecting all four of the switch nodes to their adjacent DrMOS ground pad. This places all four of the phases in parallel, and characterizes the overall transient inductance, which is equivalent to the per-phase transient inductance divided by the number of phases ( $L_{otr} = L_{ptr}/M$ , where  $M$  is the number of phases). The inductance measurements are plotted in Fig. 4.28. The measured self-inductance at 1.5 MHz is 317 nH and the measured overall transient inductance is 2.58 nH. These values can be used to calculate the full inductance matrix of the coupled inductor by rearranging Equation (4.6) as follows, assuming that the inductor is fully symmetric:

$$L_M = \frac{1}{M-1} (M \times L_{otr} - L_S) \quad (4.15)$$

Each phase is assumed to have the same self inductance, based on symmetry. The accuracy of this assumption is limited only by imperfections in construction. The mutual inductances are also approximated to be the same between any two given phases. The full inductance matrix based on measurements of the fabricated coupled inductor is:

$$\mathbf{L} = \begin{bmatrix} 317.38 & -102.35 & -102.35 & -102.35 \\ -102.35 & 317.38 & -102.35 & -102.35 \\ -102.35 & -102.35 & 317.38 & -102.35 \\ -102.35 & -102.35 & -102.35 & 317.38 \end{bmatrix} \text{nH} \quad (4.16)$$

This correlates to the fabricated vertical coupled inductor having a per-phase transient inductance of 10.3 nH and steady-state ripple amplitude in the circuit with a duty cycle of 0.125 equal to that of a non-coupled 63 nH inductor. The copper winding dc resistance was also measured using a milliohm meter at 0.185 mΩ.

#### 4.5.4 Evaluation

The coupled inductor has a per-phase transient inductance ( $L_{ptr}$ ) of 10.3 nH and has the same per-phase current ripple as a 63 nH non-coupled inductor at  $D = 0.125$ , achieving a ripple reduction factor ( $1/\gamma$ ) of over six. Figure 4.29a shows the simulated phase-current waveforms of the designed coupled inductor using the measured parameters compared with the discrete 64 nH inductors. The multiphase buck stage was simulated with  $V_{in} = 8 \text{ V}$ ,  $V_{out} = 1 \text{ V}$ ,  $I_{out} = 40 \text{ A}$ ,  $f_s = 1.5 \text{ MHz}$ , and  $C_{out} = 500 \mu\text{F}$ . The coupled inductor has a phase current ripple of 9.26 A and the discrete inductors have a ripple of 9.1 A during steady-state operation.

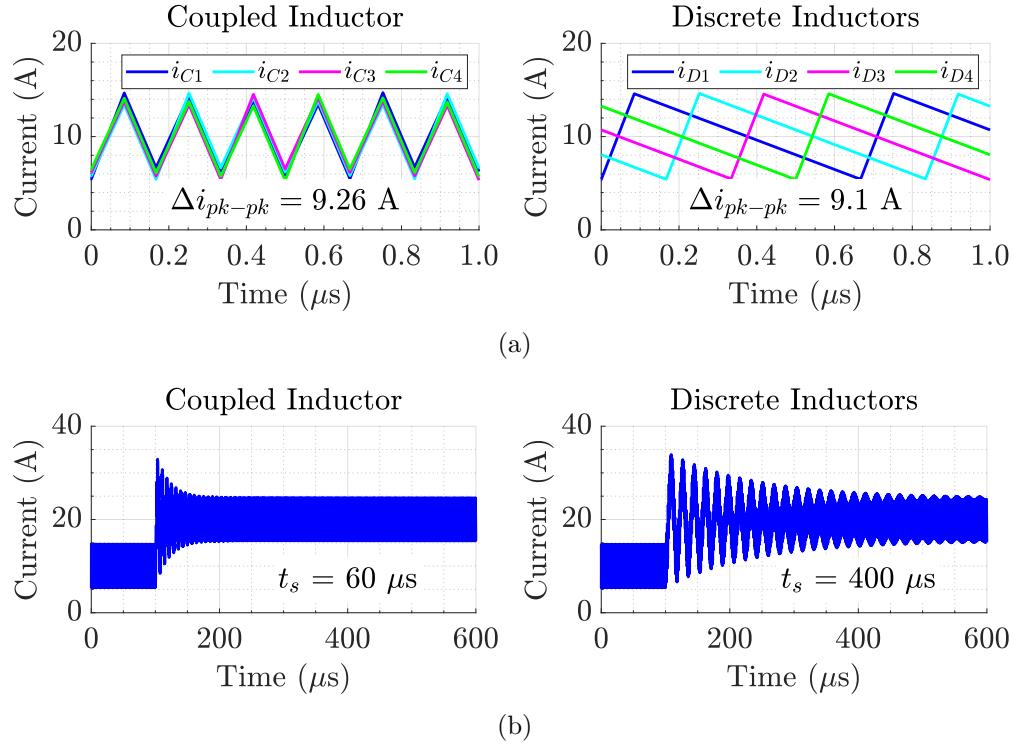


Figure 4.29: Simulation waveforms of the 1.5 MHz coupled inductor using measured values compared with discrete 64 nH inductors. A four-phase buck converter was simulated in open loop with  $V_{in} = 8$  V,  $V_{out} = 1$  V,  $I_{out} = 40$  A,  $f_s = 1.5$  MHz, and  $C_{out} = 500 \mu\text{F}$ . (a) Steady-state phase-current waveforms for the coupled inductor (left) and the discrete inductors (right). The phase-current ripple is similar. (b) One phase-current waveform of the coupled inductor (left) and discrete inductors (right) in response to a load current transient from 40 A to 80 A at  $t = 100 \mu\text{s}$ , which corresponds to a 50% to 100% load transient.

A load current transient from 40 A to 80 A was simulated during open-loop operation, and the phase current transient is plotted in Figure 4.29b. The coupled inductor phase currents settle to within 2% of their new value in approximately 60  $\mu\text{s}$ , around 6 times faster than the discrete inductors which take approximately 400  $\mu\text{s}$ . The designed coupled inductor achieves similar per-phase steady-state ripple as the 64 nH discrete inductors, while reducing the transient inductance by more than a factor of six and occupying only one-third of the volume of four 64 nH discrete inductors.

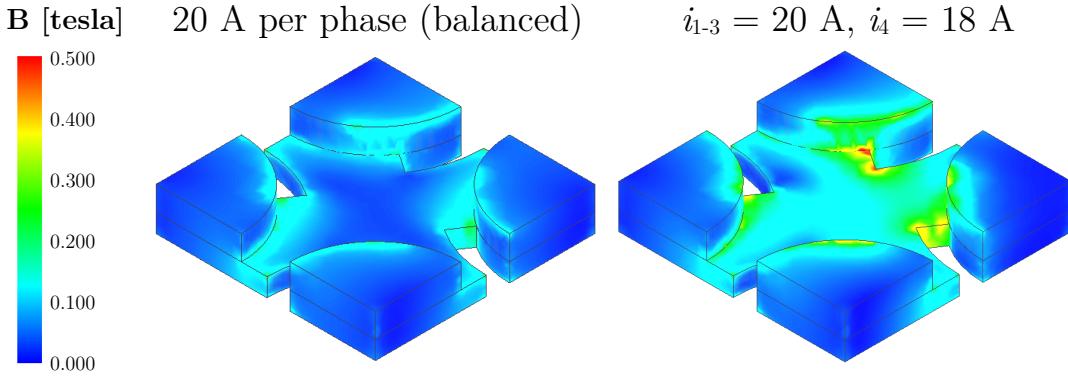


Figure 4.30: Magnetostatic finite-element model simulation (using ANSYS Maxwell 3D) of the designed 1.5 MHz coupled inductor. The simulation was conducted both under balanced dc phase currents equal to 20 A per-phase (left) and a phase current imbalance of 10% (right) where three phases are carrying 20 A of current, while the fourth is carrying 18 A. The peak flux density of the core is 190 mT in the balanced condition and 390 mT in the imbalanced condition.

A magnetostatic finite-element model (FEM) simulation was performed to assess the flux distribution in the coupled inductor core, using ANSYS Maxwell 3D. Figure 4.30 shows the dc flux density distribution during a magnetostatic simulation of the coupled inductor with equal phase currents as well as during a phase current imbalance. During the balanced operation simulation, each winding conducts 20 A, representing the full load operating condition. The maximum flux density in the core is 190 mT, well below the saturation flux density of the DMR53 material (460 mT at 100 °C). When a 10% phase current mismatch is introduced, which is the imbalance that the inductor was designed to handle, the maximum flux density in the core increases to 390 mT. This high flux density is only present in a small volume of the core, and results in a 3% decrease in magnetizing inductance.

The key performance metrics for the fabricated 1.5 MHz coupled inductor are presented in Table 4.9 and compared against the 1 MHz coupled inductor in Section 4.4. The 1.5 MHz Mini-LEGO coupled inductor reduces all of the dimensions compared to the 1 MHz inductor, and reduces the height by over a factor of two. It is able to maintain high inductance density, and greatly improves upon the coupling

Table 4.9: Summary of Metrics for 1.5 MHz Inductor Against 1 MHz Inductor

Year	Inductor Reference	Size			Inductance		Winding Resistance	Phase Current*	Phase Count	Operation Frequency
		Length	Width	Height	Inductance Density †	$\gamma _{D=0.25} \ddagger$				
2021	1 MHz LEGO-PoL	12 mm	13 mm	5.25 mm	3.86 $\frac{\text{nH}}{\text{mm}^3}$	0.166	0.09 mΩ	65 A	4	1 MHz
2023	1.5 MHz Mini-LEGO	9 mm	9 mm	2.5 mm	3.73 $\frac{\text{nH}}{\text{mm}^3}$	0.025	0.185 mΩ	20 A	4	1.5 MHz

† Inductance density is calculated using the sum of the self inductances of all of the phases divided by the overall box volume of the inductor:  $\Sigma_i (L_{S,i}) / l \times w \times h$ .

‡  $\gamma|_{D=0.25}$  is equal to the per-phase leakage inductance over the per-phase steady state inductance evaluated at D=0.25:  $L_\ell / (L_{pss}|_{D=0.25})$ . A lower number indicates higher magnetic coupling.

\* The per-phase current denotes the maximum phase current that was experimentally achieved in the testing of the inductor.

strength which further decreases the leakage inductance from 17.4 nH to 10.3 nH. The resistance of the 1.5 MHz inductor is higher as it was optimized for a full load phase current of 20 A compared to 65 A for the 1 MHz inductor. The optimization routine allocates more volume towards ferrite, and less towards copper, as the conduction losses were considerably lower for the Mini-LEGO application.

Mini-LEGO successfully presents a system with magnetics thin enough to realize in-packaging vertical power delivery. However, the push towards reducing system heights to sub-5 mm and sub-3 mm to develop regulator systems that are co-packaged with thermal solutions has necessitated magnetic components that are even thinner than the one presented in this subsection. The following section discusses geometrical innovations used to reduce the height of magnetic components even further.

## 4.6 2 MHz Pinwheel Inductor

This section presents a magnetics design aimed at pushing forward the possibility of vertical power delivery for VRMs with short vertical interconnects. The vision of quantized magnetics design introduced in Section 4.1 and shown in Figure 4.1 is advanced in this section with the development of the pinwheel coupled inductor geometry.

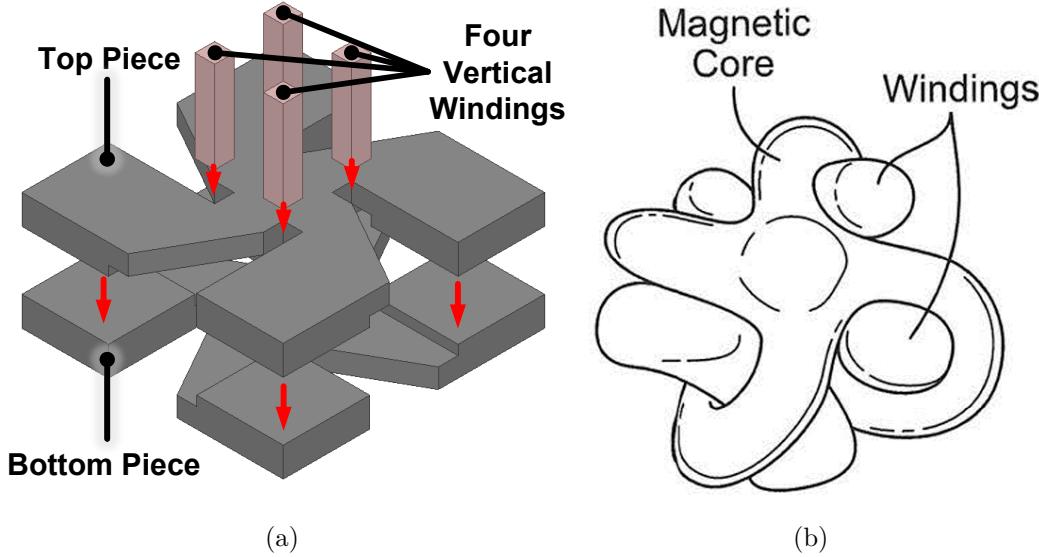


Figure 4.31: (a) Assembly procedure for a four-phase pinwheel inductor. Two identical core pieces are used, with the top piece rotated 180° in the x-axis and placed on top of the bottom piece. Four vertical windings are inserted through the core assembly. (b) Rendering of the concept of pinwheel magnetics. The magnetic core forms a 3D structure that effectively contorts itself around vertical windings to achieve multiphase coupling with low resistance and height.

#### 4.6.1 Pinwheel Inductor Geometry

To realize the concept of power-via-magnetics, the pinwheel inductor geometry is designed such that a magnetic core surrounds vertical, straight-through current-carrying conductors to achieve coupling between multiple phases. The inductor is implemented as a two-piece design, where the top and bottom piece are identical, and the top piece is rotated 180° in the  $x$ -axis and placed on top of the bottom piece as demonstrated in Figure 4.31. In this inductor structure, the core creates a path that traverses around the straight-through vertical winding, guiding the magnetic flux from the center of the top piece to the center of the bottom piece.

The geometry of one piece of the pinwheel inductor is parameterized for optimization as shown in Figure 4.32. These geometric parameters define how much of the overall inductor volume is allocated to ferrite, air, or copper. Looking at a single piece

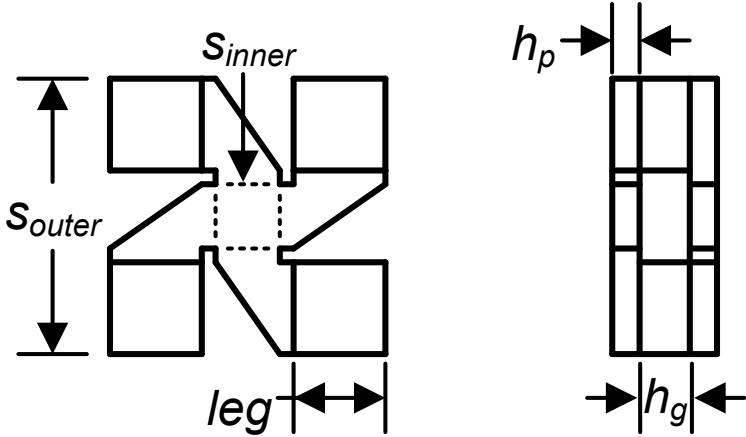


Figure 4.32: Parameterization of the pinwheel inductor. The top view (left) shows the parameters  $s_{inner}$ ,  $s_{outer}$ , and  $leg$  which define the amount of ferrite material allocated to each phase leg and the center area, as well as the copper winding area. The side view (right) shows the parameters in the  $z$ -dimension,  $h_g$  and  $h_p$ , which specify the core plate thickness, middle air gap size, and overall inductor height.

from the top view, the ferrite space is divided into two general regions: the center area, and the leg area. The center area is defined by  $s_{inner}^2$  and is the area of the core where the flux from each of the four phases combines together. The leg area consists of a square post, with an area equal to  $leg^2$ , and an angled piece that connects between the center and the leg post. The square area between the center area and the leg post, defined by  $\frac{(s_{outer}-2\times leg-s_{inner})^2}{2}$ , is the area reserved for the copper winding.

From the side view, looking at the full two piece assembly, the two key parameters are  $h_p$ , which defines the thickness of the core for the center area and leg connector, and  $h_g$ , which sets the height of the air gap in between the two pieces. These parameters define the entire cubic area of the coupled inductor, and are used in an optimization routine to determine the percentage allocation for ferrite, air, and copper.

## 4.6.2 Pinwheel Inductor Design

The pinwheel coupled inductor is optimized using the loss minimization routine of Section 4.3. The calculated loss includes winding losses (dc and ac) and the core losses,

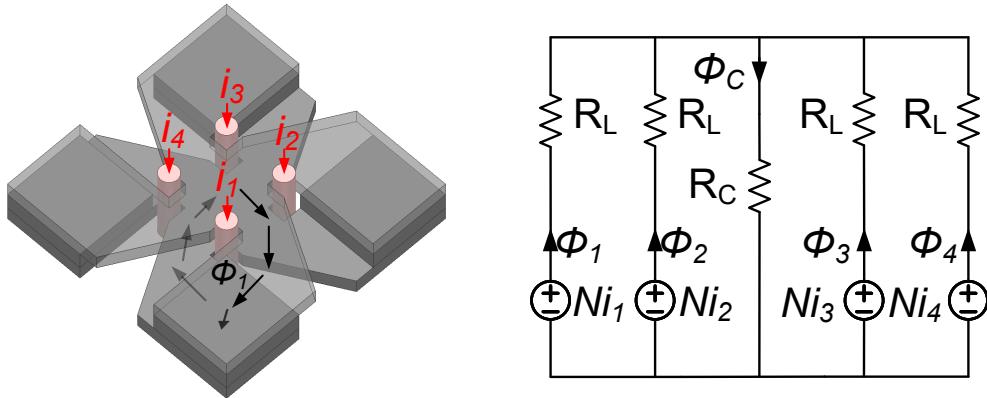


Figure 4.33: Four-phase pinwheel inductor (left) with the flux path of winding 1 shown. The dc flux generated by winding 1 wraps around the winding from the top piece to the bottom piece, with most of the flux continuing to the leg posts of the other three windings, while a small amount of the flux travels through the middle air gap from the bottom piece back to the top piece. The lumped reluctance model (right) captures the geometrical information of the pinwheel inductor with four reluctances representing the leg path and a center reluctance representing the middle air gap.

calculated using the improved Generalized Steinmetz Equation. Figure 4.33 shows the magnetic circuit model for the pinwheel inductor structure of Figure 4.32, which is used to calculate the steady-state per-phase current ripple and leakage inductance. It highlights the flux path of winding 1, illustrating how the flux is guided to wrap around the winding from top to bottom.

The optimization target is to minimize the overall inductor loss while subject to constraints in regards to inductance and efficiency with the lowest height possible. Table 4.10 details the optimization parameters and constraints. DMR53 Mn-Zn ferrite from Hengdian Group DMEGC Magnetics Co. is used as the ferrite material for the optimization, with a relative permeability of 900 and a saturation flux density of 460 mT at 100 °C (Table 4.7 summarizes the material properties). The inductor is designed to be four phases, for a 4 V to 1 V multiphase buck converter with a switching frequency of 2 MHz. Based on Equations (4.7)-(4.9), for an  $M$ -phase coupled inductor, duty cycles of  $k/M$ , where  $k = \{0, 1, \dots, M - 1\}$ , are where the

Table 4.10: 2 MHz Inductor Optimization Parameters and Constraints  
**Volumetric Constraints**

Description	Symbol	Value
Length	$s_{outer}$	$\leq 8 \text{ mm}$
Width	$s_{outer}$	$\leq 8 \text{ mm}$
Height	$2 \times h_p + h_g$	$\leq 2 \text{ mm}$
<b>Electrical Parameters</b>		
Description	Symbol	Value
Input Voltage	$V_{in}$	4 V
Output Voltage	$V_{out}$	1 V
Switching Frequency	$f_s$	2 MHz
<b>Electrical Constraints</b>		
Description	Symbol	Value
Dc Resistance	$R_{dc}$	$\leq 0.1 \text{ m}\Omega$
Full-Load Phase Current	$I_{out}/4$	25 A
Per-Phase Current Ripple	$\Delta i_{p-p,\Phi}$	$\leq 3 \text{ A}$
Per-Phase Leakage Inductance	$L_\ell$	$\leq 30 \text{ nH}$

phase current ripple reduction is at its highest. As such, a four-phase coupled inductor is well suited for operation around  $D = 25\%$ . Hence, the target per-phase current ripple is set to be  $\leq 3 \text{ A}$ , to reduce ac conduction losses and relax the requirements on the output capacitors.

Figure 4.34 shows the pareto front of the four-phase pinwheel inductor design space, fixing the parameter  $s_{outer}$  at 8 mm. For each value of overall inductor height, the pareto front shows the loss of the most optimal inductor design at that point. All of the designs shown satisfy the constraints of Table 4.10. To minimize the height while maintaining low loss, a height of 1.8 mm was identified as the “knee” of the pareto front and selected for fabrication, with a loss of 0.73 W at a full load dc current of 25 A per-phase.

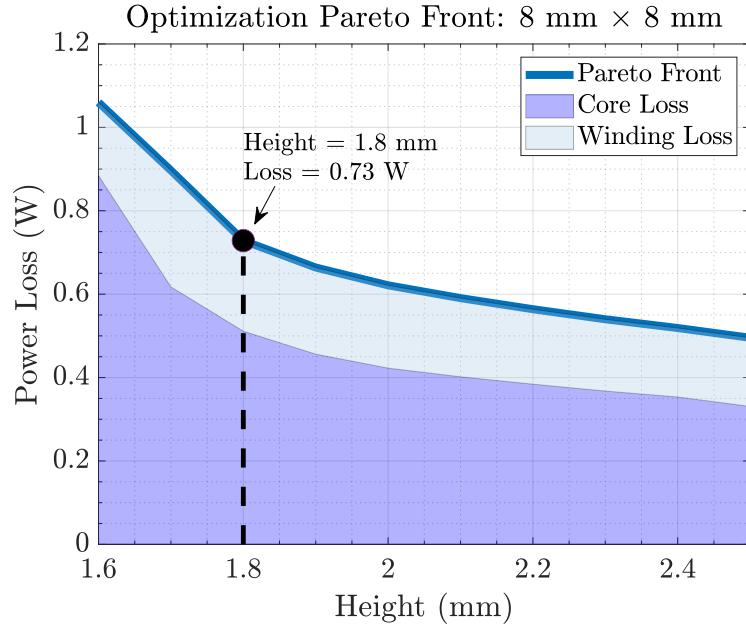


Figure 4.34: Pareto front of the pinwheel coupled inductor optimization. The “knee” of the curve, where the height is minimized while maintaining low loss, is at 1.8 mm. The design at 1.8 mm is selected for fabrication.

Table 4.11: Geometric Parameters of Designed Pinwheel Inductor

Description	Symbol	Value
Outer Side	$s_{\text{outer}}$	8 mm
Inner Side	$s_{\text{inner}}$	1.5 mm
Leg	$\text{leg}$	2.65 mm
Height	$2 \times h_p + h_g$	1.8 mm
Plate Height	$h_p$	0.6 mm
Gap Height	$h_g$	0.6 mm

The geometrical parameters of the optimized pinwheel inductor design are shown in Table 4.11. The total height is 1.8 mm, with one-third of the overall height used for the middle air gap and the remaining two-thirds for the top and bottom core pieces. The design is validated with FEM simulations in ANSYS Maxwell 3D to verify whether the flux density will remain below the saturation flux density. Figure 4.35 shows the flux density under two conditions. The first simulation is conducted with

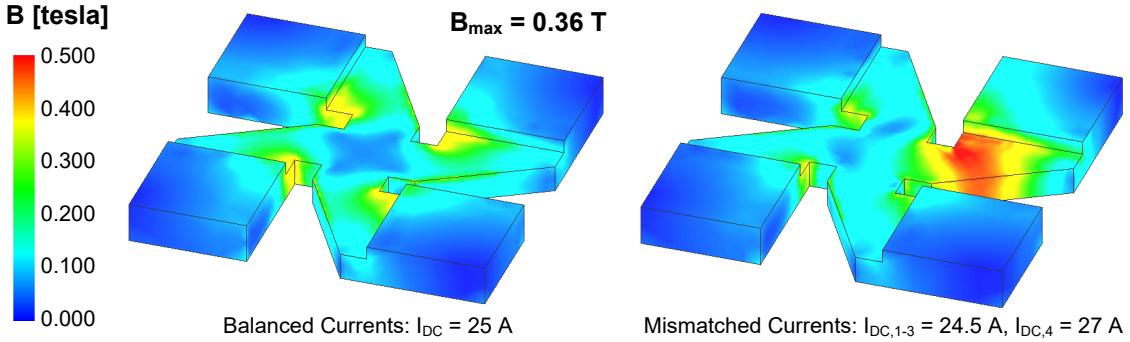


Figure 4.35: ANSYS Maxwell 3D dc flux density distribution with balanced phase currents of 25 A per phase (left) and a dc current mismatch where  $I_{DC,1-3} = 24.5$  A and  $I_{DC,4} = 27$  A (right). The maximum flux density in the core is 360 mT when all phases have balanced currents. For the dc current mismatch condition, the inductance of winding four drops by 20% of its zero dc bias inductance value, still providing sufficient inductance during full load unbalanced operation. The effective central gap length is 0.6 mm.

the current through each winding equal to 25 A. The maximum flux density of 0.36 T is observed in the core at the edges closest to the windings. Balanced currents are ideal for coupled inductors as the dc flux cancellation is equal between phases; however, in the presence of a dc current mismatch, higher dc flux levels are present in the parts of the core closest to the windings with higher current. The second simulation introduces an approximately 10% dc current mismatch, where current  $i_4$  is equal to 27 A while the other three phases are equal to 24.5 A. The self inductance of winding four drops by 20% compared to its zero dc bias value, and still providing sufficient inductance.

### 4.6.3 Experimental Results

A four-phase pinwheel coupled inductor is fabricated as per the design parameters listed in Table 4.11. The fully assembled inductor is assembled onto a test fixture utilizing the four-phase buck voltage regulator and the base motherboard (later introduced) in order to measure the inductance parameters of the inductor using the same characterization method presented in Section 4.5.3. Measurements are taken with an

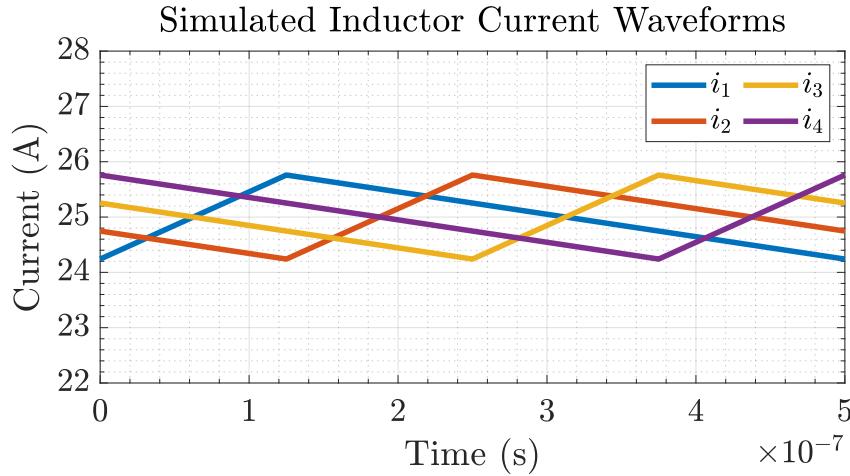


Figure 4.36: Simulated inductor current waveforms using the inductance matrix obtained from Ansys Maxwell 3D for a four-phase buck converter with  $V_{in} = 4$  V,  $V_{out} = 1$  V, and  $f_s = 2$  MHz. The peak-to-peak current ripple is 1.52 A.

Agilent 4395A Network Analyzer of the self inductance and the overall leakage inductance to characterize the inductance matrix of the assembled pinwheel inductor. These measurements include any additional leakage inductance introduced by the vertical ground return paths and the PCB parasitics. The self inductance is 189 nH at 2 MHz and the overall leakage inductance is 6.63 nH at 2 MHz. The inductance matrix for the pinwheel inductor fully assembled in the vertical four-phase buck VRM is

$$\mathbf{L} = \begin{bmatrix} 189 & -54.3 & -54.3 & -54.3 \\ -54.3 & 189 & -54.3 & -54.3 \\ -54.3 & -54.3 & 189 & -54.3 \\ -54.3 & -54.3 & -54.3 & 189 \end{bmatrix} \text{nH.} \quad (4.17)$$

This results in a per-phase steady-state inductance at  $D = 25\%$  of 243 nH and a per-phase leakage inductance of 26 nH. Figure 4.36 shows a simulation waveform of the phase currents in a four-phase buck converter with  $V_{in} = 4$  V,  $V_{out} = 1$  V, and

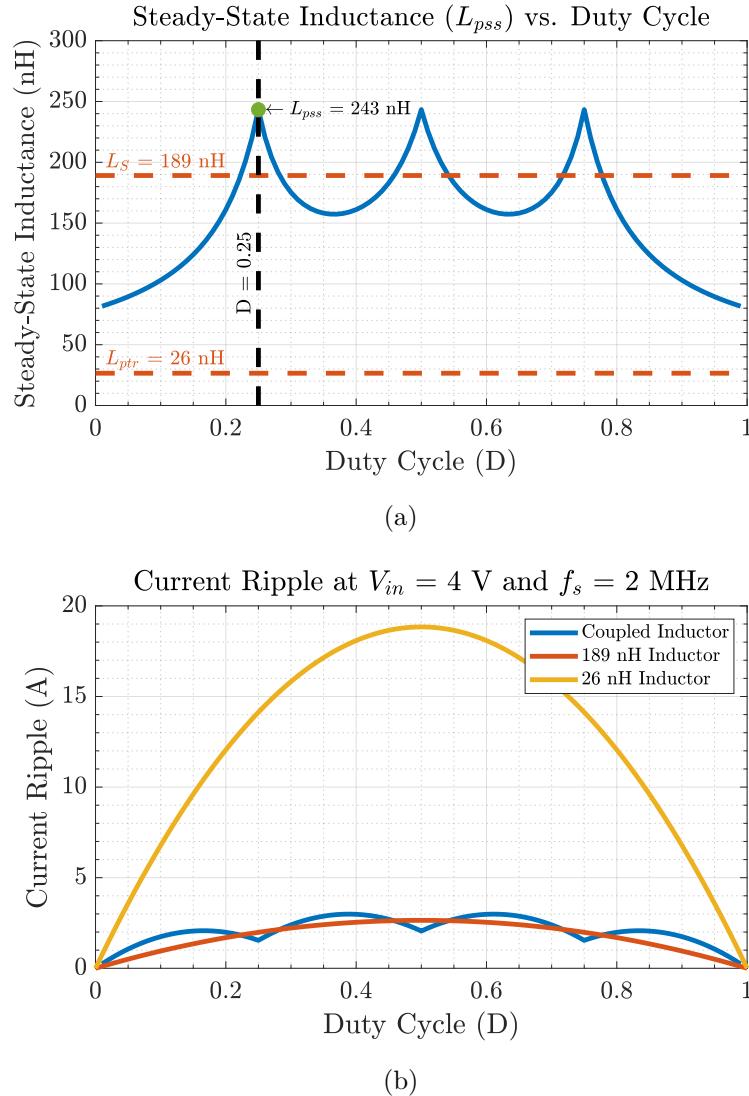


Figure 4.37: (a) Plot of the steady-state inductance ( $L_{pss}$ ) vs. duty cycle for the pinwheel coupled inductor assembly. At  $D = 0.25$ ,  $L_{pss} = 243$  nH, exceeding  $L_S$  by a factor of 1.3 and exceeding  $L_\ell$  by a factor of 7. (b) Plot of the peak-to-peak phase current ripple for the four-phase buck VRM when  $V_{in} = 4$  V and  $f_s = 2$  MHz compared to if four discrete inductors with values  $L_{disc} = L_S$  and  $L_{disc} = L_\ell$  were used. The peak-to-peak phase current ripple at  $D = 0.25$  is 1.52 A for the coupled inductor, 1.98 A for the discrete inductor case where  $L_{disc} = L_S$ , and 14.13 A for the discrete inductor case where  $L_{disc} = L_\ell$ .

$f_s = 2$  MHz using a coupled inductor with the inductance matrix of Equation 4.17.

The peak-to-peak current ripple is 1.52 A.

Figure 4.37a plots the per-phase steady-state inductance and per-phase leakage inductance against the duty ratio. At duty ratios close to 25%, 50%, and 75%,

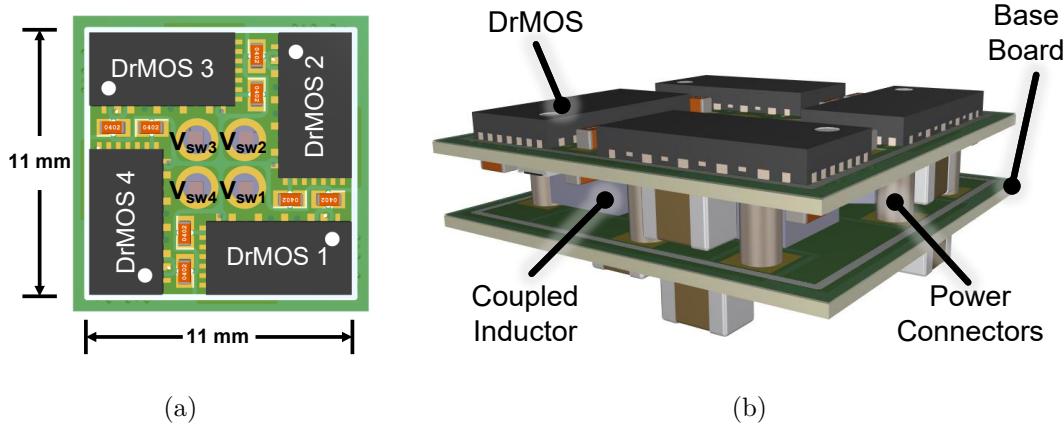


Figure 4.38: (a) Top side view of the four-phase buck VRM power stage. The layout is symmetrical, with each phase consisting of one MP86936 DrMOS and associated bootstrap and input capacitors. The switch node connects to a via in the center of the board for connection to the coupled inductor. (b) 3D view of the four-phase buck VRM power stage system assembly. The coupled inductor is assembled by soldering the four vertical windings to the vias in the buck board as well as to vias in the base board. Power connectors are used for the ground return path and the input power between the base board and buck board.

the steady-state inductance exceeds the self inductance of each winding. Thus, at these points, as further highlighted in Figure 4.37b which shows the peak-to-peak phase current ripple of the inductor when  $V_{in} = 4$  V and  $f_s = 2$  MHz, the phase current ripple is lower than if a discrete inductor with an inductance equal to the self-inductance of 189 nH were used. At this condition, the coupled inductor is able to reduce the peak-to-peak phase current ripple by a factor of 1.3 times over the scenario where  $L_{disc} = L_S = 189$  nH and by a factor of 7 times over the scenario where  $L_{disc} = L_\ell = 26$  nH.

To verify the coupled inductor design, a four-phase buck converter was designed to interface with the inductor and perform vertical power delivery. Figure 4.38a shows the top-side layout of the four-phase buck converter. All four of the semiconductor devices are placed on the top side in a symmetrical fashion. The switch node of each phase is connected to a via, where the inductor winding is connected. Figure 4.38b highlights the assembly process of the four-phase buck converter PCB and coupled

Table 4.12: Bill-of-Materials for the Four-Phase Buck Pinwheel Inductor Verification System

Description	Quantity	Part Number
DrMOS Devices	4	MPS MP86936GRJT-P
Bootstrap Capacitors	4	Kemet 0402 25 V 0.1 $\mu$ F
Input Capacitors	4 8	Kemet 0402 25 V 4.7 $\mu$ F TDK 0805 25 V 22 $\mu$ F
Output Capacitors	12	TDK 0805 6.3 V 100 $\mu$ F

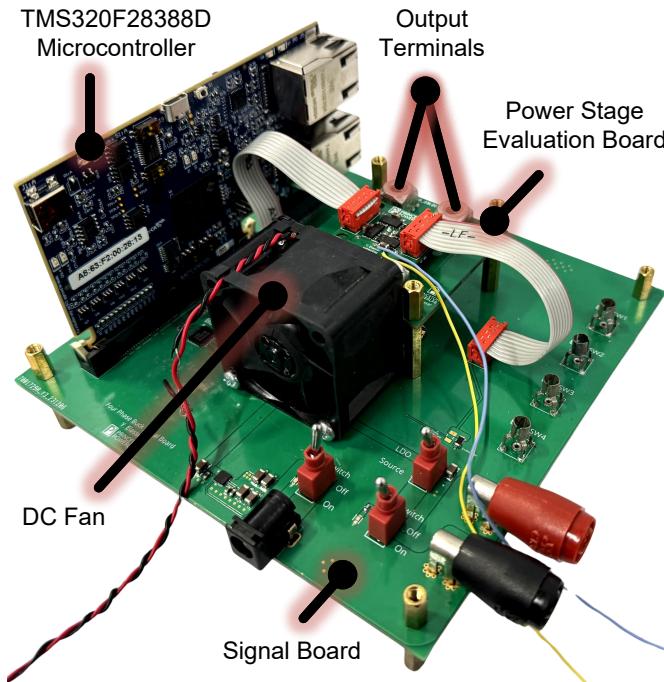


Figure 4.39: Test fixture assembly for the four-phase buck VRM. The power stage evaluation board contains the four-phase buck power stage, including the pinwheel coupled inductor, as well as the base motherboard which houses the input and output power terminals. A TMS320F28388D microcontroller is connected to a signal board, which generates the PWM signals, provides the gate drive power, and houses test points. One 36 CFM dc fan is used for cooling the system.

inductor. A base motherboard is used to connect between the input power source and output electronic load, routing the input power vertically to the four-phase buck PCB and receiving the output power from the inductor. Output capacitors are placed on the bottom side of this base board. The bill-of-materials for the four-phase buck

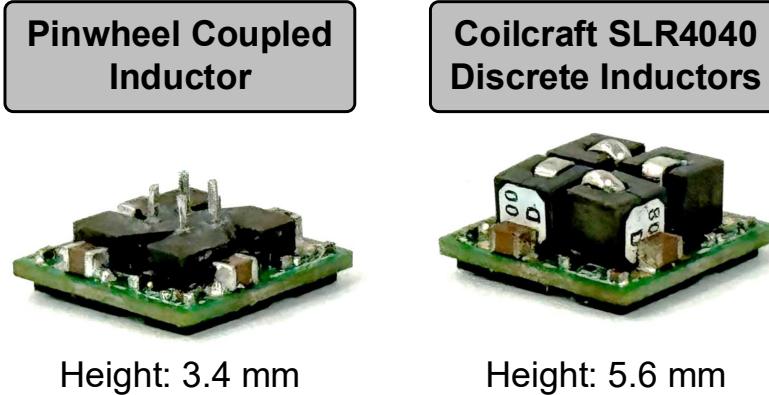


Figure 4.40: Power stage of the four-phase buck VRM of Figure 4.38 assembled with the pinwheel coupled inductor (left) and four Coilcraft SLR4040 discrete inductors (right). The power stage system height with the pinwheel coupled inductor is 3.4 mm, approximately 60% of the height of the system height of 5.6 mm with the discrete inductors.

converter is listed in Table 4.12. MP86936 DrMOS devices are used, with a footprint of  $3 \text{ mm} \times 6 \text{ mm}$ , resulting in an overall power stage area of  $11 \text{ mm} \times 11 \text{ mm}$ . The height of the DrMOS device is 0.8 mm.

The four-phase buck VRM is assembled with the four-phase pinwheel coupled inductor in a test fixture assembly shown in Figure 4.39. A signal board is used to provide the PWM signals, gate drive power, and house test points for probing. Signals are generated using a TMS320F28388D microcontroller from Texas Instruments. The converter is cooled with one 36 CFM dc fan.

To compare the performance of the pinwheel coupled inductor against off-the-shelf discrete inductors, a four-phase buck VRM is assembled with Coilcraft SLR4040 series discrete inductors. These inductors have a dimension of  $4 \text{ mm} \times 4 \text{ mm} \times 4 \text{ mm}$ , resulting in an overall area footprint for four discrete inductors of  $8 \text{ mm} \times 8 \text{ mm}$ , which is the same as the pinwheel coupled inductor. Figure 4.40 shows the power stage assemblies with the pinwheel coupled inductor and the discrete inductors. The pinwheel coupled inductor is 1.8 mm tall, 2.2 mm less than the discrete inductors with a height of 4 mm. The overall system height is 3.4 mm with the pinwheel coupled

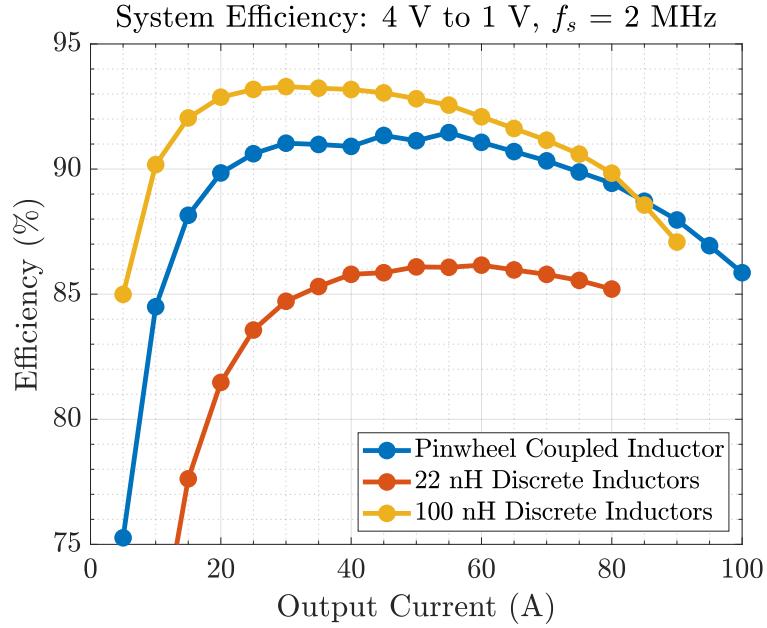


Figure 4.41: System efficiency of the four-phase buck VRM with the pinwheel coupled inductor, four Coilcraft SLR4040 22 nH discrete inductors, and four Coilcraft SLR4040 100 nH discrete inductors. The DrMOS junction temperature is below 100 °C for all points presented. The pinwheel coupled inductor VRM achieves a peak efficiency of 91.5%, significantly higher than the 22 nH discrete inductors with similar transient performance as the coupled inductor, and 1.7% lower than the 100 nH inductors.

inductor, which is approximately 60% of the height of the system height of 5.6 mm with the discrete inductors.

The discrete inductors are available in five different inductance values: 22 nH, 50 nH, 65 nH, 80 nH, and 100 nH. The 22 nH inductors, which are similar in value to the per-phase leakage inductance of the pinwheel coupled inductor, as well as the 100 nH inductors, which have the highest achievable inductance in this package and thus the lowest current ripple, are used to compare against the coupled inductor in terms of efficiency and transient speed.

Figure 4.41 plots the system efficiency for the four-phase buck VRM with  $V_{in} = 4$  V,  $V_{out} = 1$  V, and  $f_s = 2$  MHz. The efficiency is presented excluding the gate drive loss of 0.43 W at  $f_s = 2$  MHz. The converter was run until the junction temperature of the DrMOS devices, which is monitored using the provided junction temperature pin

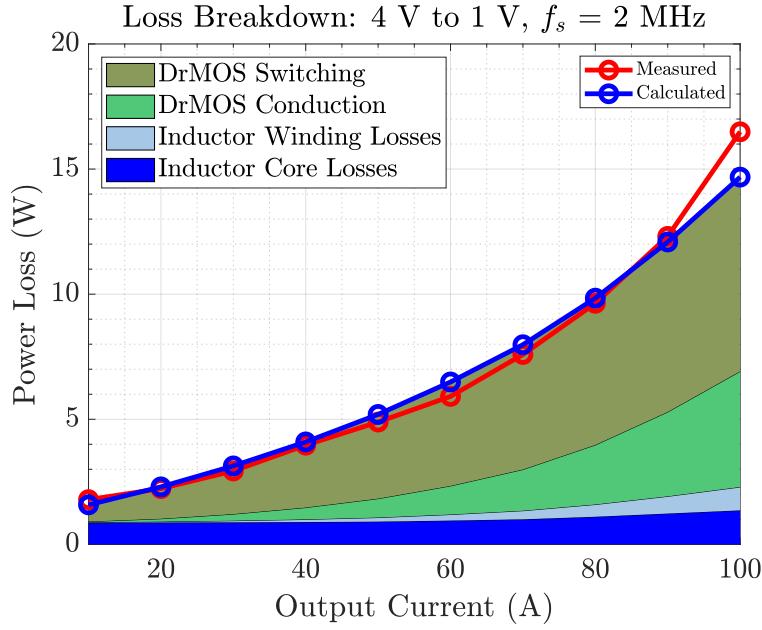


Figure 4.42: Loss breakdown for the four-phase buck VRM with the pinwheel coupled inductor. The measured vs. calculated loss is plotted. The inductor winding conduction losses are the smallest component of the loss due to the low dc resistance. The DrMOS devices dominate the overall system loss.

of the devices, reaches 100 °C. The peak efficiency of the pinwheel coupled inductor VRM is 91.5% at 55 A and the full load efficiency at 100 A is 86%. When using 22 nH discrete inductors, similar in value to the per-phase leakage inductance of the pinwheel coupled inductor, the junction temperature reaches 100 °C at 80 A of current and has a peak efficiency of 86.2% at 60 A and a full load efficiency of 85.2%. Using 100 nH discrete inductors improves the peak efficiency to 93.2% at 40 A, however, these inductors have a saturation current (defined as a 20% drop in the inductance at zero dc bias) of 17 A at 100 °C, resulting in a steeper decline of the efficiency. The full load efficiency is 87% at 90 A.

The loss breakdown for the pinwheel coupled inductor VRM is presented in Figure 4.42. The DrMOS devices contribute the bulk of the losses, with significant switching losses at the 2 MHz frequency. In regards to the coupled inductor, while the conduction losses are kept low due to the short winding path and the low dc

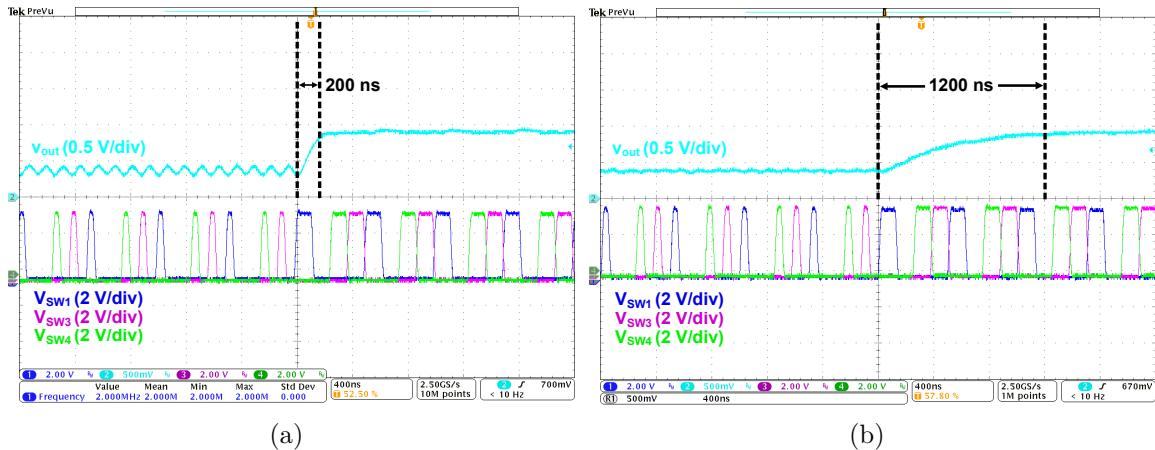


Figure 4.43: Common-mode duty cycle to output voltage transient with a duty cycle step from 10% to 25% at  $V_{in} = 4$  V and  $f_s = 2$  MHz. (a) The pinwheel coupled inductor settles to its new output voltage within 200 ns. (b) The 100 nH discrete inductors take 1200 ns to settle to their new output voltage.

resistance of 0.09 mΩ, the core losses correspond to a drop in the peak efficiency of 1.4% at 55 W. In this instance, the benefits of system height reduction were achieved while increasing the core losses. Core loss models that can quickly and more accurately estimate the loss for a given coupled inductor geometry with non-uniform flux densities are required for future optimization of low-profile coupled magnetics [100].

To evaluate the transient performance of the system, an open loop duty cycle transient is conducted for the pinwheel coupled inductor VRM and the 100 nH discrete inductor VRM. A common-mode duty cycle perturbation  $\tilde{d}$  is applied to all four phases, and the resulting change in the output voltage  $\tilde{v}_o$  is measured. The transfer function  $G_{vd} = \tilde{v}_o/\tilde{d}$  is impacted by the leakage inductance of the coupled inductor, highlighting the ability of the coupled inductor to achieve faster transient performance when compared to the self or steady-state inductance [101, 102].

To measure the output voltage transient, 22 Kemet 0805 10 V 47 nF C0G MLCCs were placed on the base motherboard, totalling 1.13 μF of capacitance. A resistive load of 50 mΩ, implemented as 20 1 Ω 1 W 1% 1206 power resistors, is used. A duty

Table 4.13: Performance Comparison between Pinwheel Coupled and Discrete VRM Implementation (Operating Condition:  $V_{in} = 4$  V,  $V_{out} = 1$  V, and  $f_s = 2$  MHz)

Inductor	Efficiency		Density		$L_\ell$
	Peak	Full Load	Area	Volume	
<b>Pinwheel Coupled</b>	91.5% @ 55 A	86.0% @ 100 A	0.83 A/mm <sup>2</sup>	3760 W/in <sup>3</sup>	26.5 nH
<b>22 nH Discrete</b>	86.2% @ 60 A	85.2% @ 80 A	0.67 A/mm <sup>2</sup>	1930 W/in <sup>3</sup>	22 nH
<b>100 nH Discrete</b>	93.2% @ 40 A	87% @ 90 A	0.75 A/mm <sup>2</sup>	2180 W/in <sup>3</sup>	100 nH

cycle transient is performed from 10% to 25% at  $V_{in} = 4$  V and  $f_s = 2$  MHz, which steps the output power from 0.4 V and 8 A to 1 V and 20 A.

Figure 4.43a shows the experimental waveforms of the output voltage and three of the four switch node voltages for the pinwheel coupled inductor for the duty cycle transient. The output voltage settles to within 2% of its new voltage level in 200 ns. Figure 4.43b shows the same waveforms for the 100 nH discrete inductors, settling to the new output voltage in approximately 1200 ns.

Table 4.13 compares the pinwheel coupled inductor VPD module against the discrete inductor implementations. While each of the solutions has the same area, the coupled inductor is able to handle a larger amount of current per phase than the 100 nH inductors as the dc flux cancellation allows the inductor to avoid saturation, and can handle more current than the 22 nH inductors due to the lower loss at higher load currents. The pinwheel coupled inductor has a peak efficiency 1.7% lower than the 100 nH inductors, but achieves a power density 1.75 times higher and has a per-phase leakage inductance 4 times lower, resulting in significantly faster transient performance.

Table 4.14: Comparison of the Pinwheel Coupled Inductor Against Other Magnetics Solutions for VRMs

Year	Inductor Reference	Size			Inductance		Winding Resistance	Phase Current*	Phase Count	Operation Frequency
		Length	Width	Height	Inductance Density †	$\gamma _{D=0.25}‡$				
2021	1 MHz LEGO-PoL	12 mm	13 mm	5.25 mm	3.86 $\frac{\text{nH}}{\text{mm}^3}$	0.166	0.09 mΩ	65 A	4	1 MHz
2023	1.5 MHz Mini-LEGO	9 mm	9 mm	2.5 mm	3.73 $\frac{\text{nH}}{\text{mm}^3}$	0.025	0.185 mΩ	20 A	4	1.5 MHz
2024	Pinwheel	8 mm	8 mm	1.8 mm	6.56 $\frac{\text{nH}}{\text{mm}^3}$	0.107	0.09 mΩ	25 A	4	2 MHz
2022	Integrated Series Asymmetrical [103]	5.21 mm	3.36 mm	0.54 mm	9.7 $\frac{\text{nH}}{\text{mm}^3}$	0.521	3.1 mΩ	3 A	4	20 MHz
2023	LC Two-Phase [104]	8 mm	14 mm	1.3 mm	0.82 $\frac{\text{nH}}{\text{mm}^3}$	0.580	0.15 mΩ	25 A	2	1.6 MHz
2024	MSC-PoL [38]	28.9 mm	13 mm	3.9 mm	1.67 $\frac{\text{nH}}{\text{mm}^3}$	0.126	0.06 mΩ	28.1 A	4	400 kHz
2024	Switching Bus [36]	18 mm	5 mm	5 mm	4.62 $\frac{\text{nH}}{\text{mm}^3}$	0.331	0.48 mΩ	31.3 A	2	150 kHz
2024	Twisted Core [105]	9.3 mm	8.6 mm	2 mm	0.98 $\frac{\text{nH}}{\text{mm}^3}$	0.436	0.03 mΩ	65 A	2	1.5 MHz

† Inductance density is calculated using the sum of the self inductances of all of the phases divided by the overall box volume of the inductor:  $\Sigma_i (L_{S,i}) / l \times w \times h$ .

‡  $\gamma|_{D=0.25}$  is equal to the per-phase leakage inductance over the per-phase steady state inductance evaluated at D=0.25:  $L_\ell / (L_{pss}|_{D=0.25})$ . A lower number indicates higher magnetic coupling.

\* The per-phase current denotes the maximum phase current that was experimentally achieved in the testing of the inductor.

#### 4.6.4 Inductor Benchmarking

The pinwheel coupled inductor is benchmarked against the 1 MHz inductor of Section 4.4, the 1.5 MHz inductor of Section 4.5, and other state-of-the-art magnetics solutions for VRMs in Table 4.14. The pinwheel coupled inductor is the smallest inductor out of the three presented in this chapter, and has the smallest height with 1.8 mm. Designing for a lower input voltage, along with the pinwheel geometry itself, allowed for a highly dense inductor structure with ultra-low dc resistance. The dc resistance of 0.09 mΩ is the same as the 1 MHz inductor, but designed for a lower current application. The straight-through vertical power-via winding design results in the shortest possible winding path for vertical power delivery.

The pinwheel coupled inductor performs well in all metrics when compared to the landscape of other magnetic solutions. For designs in the frequency range of 100 kHz to 5 MHz, the pinwheel coupled inductor achieves the lowest volume amongst the presented inductor designs and operates at the highest switching frequency. The

inductance density is high, leveraging strong magnetic coupling to obtain a high per-phase steady-state inductance. It achieves a ratio of the per-phase leakage inductance to the per-phase steady-state inductance at 25% duty cycle ( $\gamma|_{D=0.25} = L_{pss}|_{D=0.25} / L_\ell$ ) is 0.107, indicating a per-phase current ripple 10 times lower than it would be if discrete inductors equal to  $L_\ell$  were used. The dc resistance of 0.09 mΩ is amongst the lowest reported, resulting in lower conduction losses for the designed full load current when compared to the design in [105] with a winding resistance of 0.03 mΩ.

## 4.7 Chapter Summary

This chapter presents a framework for the design and fabrication of coupled inductor magnetic components suitable for vertical power delivery. These magnetic components are able to deliver large amounts of power in a small area under stringent 3D volume constraints. Magnetic components are essential for filtering and regulating power delivered to high density loads, and need to be carefully designed and optimized for high performance, speed, and density.

One technique to greatly improve the density of magnetic components is to merge the functionality of multiple discrete inductors into one single magnetic component with shared flux paths. By coupling the magnetic components in a parallel fashion, less energy is stored in the core and benefits can be realized in regards to the trade-off between desiring a large inductance for a low-ripple current source and a small inductance for fast current slew rates in response to a transient event. Models for coupled inductors are reviewed, analyzed, and a set of simple equations are derived to understand the impact of coupling on the per-phase steady-state ripple and the leakage inductance, which is the effective inductance during transient operation.

Using the derived equations, a generalized optimization procedure is developed for vertical coupled inductors. The optimization routine determines exactly how to allocate the volume available for the inductor towards copper, magnetic material, or

air. The optimization routine aims to minimize the loss of the inductor at specified points of interest along the output current load curve while ensuring that the inductor satisfies constraints set on its steady-state and transient performance. Three four-phase vertical coupled inductors, each subject to different constraints and for different applications, are designed using this optimization routine at frequencies of 1 MHz, 1.5 MHz, and 2 MHz.

For the preliminary vertical stacked LEGO-PoL converter presented in Section 3.4, a four-phase 1 MHz coupled inductor is designed and fabricated to carry 65 A per phase at full load. The inductor is 5.25 mm tall, and has a per-phase current ripple of 8.3 A and a leakage inductance of 17.4 nH. While the inductor performed well, the high height was detrimental to in-packaging vertical power delivery. The design of Mini-LEGO (Section 3.5), focusing on low height and high power density, saw the design and optimization of a new four-phase inductor for operation at 1.5 MHz. This inductor modifies the geometry to give the optimization routine more flexibility to balance the trade-off between winding loss and core loss, enabling a low height 2.5 mm tall inductor carrying 20 A per phase. This inductor enables Mini-LEGO to achieve unprecedented power density.

The inductors designed for LEGO-PoL and Mini-LEGO still adhered to a magnetics design philosophy where the windings are designed to revolve around magnetic material to form a turn. Towards the vision of vertical power delivery, a new design called the pinwheel coupled inductor is developed to facilitate power-via-magnetics. In this new structure, the current-carrying conductors are constrained to be vertical, and the magnetic core is designed to form a pinwheel pattern that wraps around the conductor. This structure is optimized and fabricated with a height of 1.8 mm and validated in a four-phase buck converter delivering 25 A per phase. It is benchmarked against comparable non-coupled off-the-shelf inductors as well as other coupled inductor structures for VRMs, and exhibits low dc resistance, high inductance density, and

ultra-thin height. This structure pushes forward the vision of designing low-profile coupled magnetics that can deliver high-currents while utilizing an ever-shrinking 3D volume to its full extent.

## Related Publications

1. Y. Elasser, J. Baek, C. R. Sullivan, and M. Chen, “Modeling and Design of Vertical Multiphase Coupled Inductors with Inductance Dual Model,” in 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), (Phoenix, AZ, USA), pp. 1717–1724, June 2021. [[106](#)]
2. Y. Elasser, J. Baek, K. Radhakrishnan, H. Gan, J. P. Douglas, H. K. Krishnamurthy, X. Li, S. Jiang, V. De, C. R. Sullivan, and M. Chen, “Mini-LEGO CPU Voltage Regulator,” *IEEE Transactions on Power Electronics*, vol. 39, no. 3, pp. 3391–3410, 2024. [[78](#)]
3. Y. Elasser and M. Chen, “Power-Via-Magnetics with Pinwheel Coupled Inductors for Ultra-Thin Vertical Power Delivery,” *IEEE Transactions on Power Electronics*, 2024, under review. [[50](#)]

# Chapter 5

## Conclusion

### 5.1 Conclusion

This dissertation systematically develops methods for hybrid switched-capacitor circuits and magnetics co-design for vertical power delivery to high-density loads. High-density loads, such as microprocessor systems (which are used as the case study for this dissertation), require a large amount of power – specifically high current at low voltages – to be delivered within an ever-decreasing area with low height. They need power electronics that have high densities with good end-to-end efficiency, fast speed, and scalability to easily extend to power multiple voltage rails.

To push power electronics towards these goals, the hybrid switched-capacitor architecture and magnetics leverages the scaling laws of power components. Power converters consist of capacitors, semiconductor devices, and magnetics. Generally, capacitors are the most energy dense passive components, and are indifferent to scaling, while semiconductor devices that are smaller and block lower voltages are preferred and larger-scale magnetic components that process more power are advantageous.

To further improve upon density and efficiency, Chapter 3 of this dissertation explores the advantages and challenges of a new power delivery paradigm called *vertical power delivery*, whereby power converters utilize a 3D system package to deliver

power in the  $z$ -axis as opposed to traditional lateral power delivery with 2D converters where power is routed through the  $xy$ -plane. Vertical power delivery reduces the power delivery network impedance and losses, opens up area adjacent to the processors, and improves overall system integrity. The hybrid switched-capacitor architecture is a suitable fit for vertical power delivery with the adoption of a proposed *three-layer packaging model*, whereby three separate layers consisting of capacitors at the bottom, switches in the middle, and magnetics at the top are vertically stacked to construct a 3D power converter where each layer is optimized for its function and works synergistically with the other layers for mutual advantages.

Focusing specifically on the first two layers of this packaging model, Chapter 3 presents the proposed hybrid switched-capacitor architecture called the *linear-extendable group-operated point-of-load (LEGO-PoL) architecture*. This architecture is configured in a series-input, parallel-output configuration with automatic voltage balancing and current sharing between submodules, allowing for scalability. Capacitors process the high input voltage stress, and a switch network interfaces with the bottom layer capacitors and top layer magnetics to shuffle energy between the input source and the load, stepping down the input voltage and delivering high output current. By merging the operation of the capacitive and inductive energy transfer stages through the switch network, the LEGO-PoL architecture can achieve extremely high density, as well as high efficiency through soft-charging of the capacitors and high bandwidth through magnetics integration. Two prototypes were developed to validate the architecture and vertical stacking packaging model. The first LEGO-PoL prototype is 16.65 mm tall, and achieves a peak efficiency of 88.4% for 48-V-to-1-V conversion, using air cooling to deliver 450 A and immersion liquid cooling to deliver 780 A. The power density with air cooling is 294 W/in<sup>3</sup>. The second prototype, termed Mini-LEGO, fully re-designed the converter to enable ultra-high density. It reduces the height to 8.4 mm, achieves a peak efficiency of

84.1% for 48-V-to-1-V conversion, and uses air cooling to deliver 240 A. The power density is improved to 1390 W/in<sup>3</sup> and the current area density is 0.7 A/mm<sup>2</sup>. Mini-LEGO demonstrates the feasibility of performing in-package vertical power delivery with the hybrid-switched capacitor architecture.

Chapter 4 focuses specifically on the third layer of the packaging model, the magnetic components. These are often the most bulky components in a power converter, so extra effort is placed in re-imagining the way in which these components are designed. As vertical power delivery shifts the design mindset from 2D to 3D, this chapter answers the question of the best way to optimize and develop a magnetic component with a fixed 3D volume for high density with low vertical profile to deliver large amount of current vertically. Methods for integrating multiple magnetic components onto a single magnetic core through parallel coupling are reviewed, modelled, and analyzed to develop a comprehensive optimization routine to design vertical coupled magnetics. Three magnetic components are fabricated and tested. The first is a 1 MHz, four-phase vertical coupled inductor for the first iteration LEGO-PoL prototype with a height of 5.25 mm, delivering 65 A per phase. It achieves a steady-state performance equivalent to that of an 85 nH inductor, and a transient performance equivalent to that of a 17 nH inductor. For Mini-LEGO, a four-phase inductor operating at 1.5 MHz is fabricated with a reduced height of 2.5 mm delivering 20 A per phase. It increases the coupling strength, such that it has the steady-state performance of a 65 nH inductor and the transient performance of a 10 nH inductor. Lastly, a new vertical coupled inductor structure, the *pinwheel coupled inductor*, is developed, which uses vertical power-via interconnects with the magnetic core guiding the flux around the conductors. This inductor is designed to operate at above 2 MHz, and a four-phase pinwheel inductor with 1.8 mm is built and tested in a four-phase buck vertical power module. The magnetics design methodology presented in this chapter is widely applicable to design power components with high density and volumetric

restrictions, and goes hand-in-hand with designing power converters to satisfy the requirements of future loads.

## 5.2 Future Work

This thesis presents and begins to develop a vision for what power converters will look like when designed for vertical power delivery, strategically utilizing the available 3D volume for optimal performance. While packaging models, architectures, and magnetics are explored in this thesis towards this vision, future work that builds upon the foundation presented here includes, but is not limited to:

- Circuits-magnetics-thermal co-design. While emphasis on this thesis is placed on circuits and magnetics co-design, as alluded to in Section 2.3, thermal management will become an increasing challenge as area densities begin to exceed  $1 \text{ A/mm}^2$ . Incorporating thermal models into the magnetics optimization routines and PCB design methodology will be important to developing complete vertical stacked power converter packages.
- Leveraging artificial intelligence for power electronics optimization. The optimization routine presented in Section 4.3 uses iterative methods to calculate the highly non-linear hysteresis losses in the magnetics. As one of the optimization targets is to minimize the loss, the accuracy of this loss calculation impacts the overall optimization result greatly. In the future, optimization routines that can leverage machine learning from data can improve the accuracy of magnetics design and accurately predict system performance.
- Advanced packaging methods that connect the vertical layers together. Currently, PCB technology limits the height and system integration. Eschewing PCB technology completely for other technologies with better thermal and elec-

trical performance can increase the level of integration and improve the overall density.

- Exploring power management integrated circuits with future process-level transistors for extreme proximity to the load. By distributing some of the switch network to highly integrated circuits, parasitics can be further reduced and density can be further improved.
- A detailed examination of EMI in vertical stacked converters. Modeling and mitigation techniques for EMI in vertical converters is important to ensuring the power and signal integrity of the entire 3D package.

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