Mandeep Singh

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●https://github.com/mink007 ● https://www.sabzimatic.com
● Google Scholar

Founder

Open for consultation roles on Semiconductor Design Automation using Artificial Intelligence. Also open for Principal Engineer Roles.

Skills

- Python/R/Ruby/Perl/Tcl Shell scripting
- Circuit/Physical Design Automation
- Design of Experiments
- Unix/Linux OS
- Git/Design Sync/Synchronicity
- Machine Learning/CNN/Reinforcement Learning
- Matlab/Simulink
- C/C++
- High Performance Computing/Distributed computing/Multi-threading

Professional Experience

NSA Affiliate - 11/2023 to 03/2024
Engineering and Physical Sciences Researcher position.
To perpetually protect American Semiconductor Technology $15 Billion Intel-Microsoft foundry partnership dated Feb 21st, 2024. Fought by Mandeep Singh in SCOTUS 21-739 Question #8 and also at 8 hour non-stop NSA security interview for the people of Hillsboro, Intel Corporation and American semiconductor technology.

Founder and Inventor 06/2020 – Present
Sabzimatic, Hillsboro, OR

- Design and implement cooking robot for cloud/smart kitchen from concept to final product. Job responsibilities include but not limited to design, develop, test and iterate in software, firmware, electronic, electrical and mechanical research and engineering aspects. Implement design from safety, ease of use, easy to assemble perspective.

- Firmware development include coding in C/C++ and integration of temperature sensors, depth sensors, camera, stepper motors and LCD Touch screen (GUI Development) over SPI, UART, I2C and USB interfaces.

- Collaborate with domestic and international vendors for part manufacturing and procurement.

Patents pending. As of April 16th 2024 Korean International Search Report on Patentability granted all claims as inventive steps. Link to prototype videos

Staff CAD R&D/EDA Tools Software Engineer: 02/2023 – 10/2023
Intel Corp, Hillsboro, OR

- Presented on Reinforcement Learning starter algorithms on TD Programmers day for knowledge share.

- Proposed and explained on white board how to pull-in PDK kit schedule by mid single digit weeks with high quality. This is **invention disclosure**. It is state of the art in semiconductors to pull-in pdk kit schedule by mid single digit weeks.
- Developed 3D transistor models for field-solver to extract capacitance on advanced node - Intel18A.
- Directed EDA vendor tools for bugs and feature enhancements to improve quality and productivity.
- Wrote flows in python to better debug capacitance delta among field-solver tools. Write layers in gds from text format. Convert geometry from one field-solver tool to another.
- Wrote automation in python which generates field solver profile for multiple skews with single command thus improving quality and eliminating multiple steps.

STANFORD UNIVERSITY, Stanford, CA
Graduate Certification in Artificial Intelligence, 6/2019 - 06/2020 CGPA – 3.5

- Convolutional Neural Networks for Visual Computing – CS231N
  - Emotion recognition in Audio & Video using Deep Neural Networks. (link to paper).
- Probabilistic Graphical Models – CS228
  - Markov random fields, Bayesian Networks representation, inference & learning.
- Principles of Robotic Autonomy I – AA274A
  - Filters(Bayesian, KF, EKF, Particle) for SLAM. Camera calibration, path planning, trajectory optimization. (link to project).
- Decision making under Uncertainty -AA228
  - Bayesian Networks, Reinforcement Learning, MDP – (link to project, link to project).
- Data Mining and Analysis – STATS202
  - PANSS Score predictor and Assessment Classifier (link to project)
    - Unsupervised learning, Linear regression, Support Vector Machines, Random forest, Bagging, Boosting, Classification, data transformation, R programming language.

Design Automation Engineer 6/2017 –10/2019
Intel Corporation, Hillsboro, OR
Skills: Placement & Routing Algorithms, Tcl, Perl, DRC, LVS, Reliability verification, Timing, Extraction, Design Sync, ICV, StarRC.

- Worked on fullchip auto-router. Using in-house EDA tool tcl based APIs and functions.
- Developed taper script which shrinks the trunk route for power saving. Saved 2% power consumption at partition level.
- Optimized over-the-hierarchy generation flow/algorithm on mega FUB(Functional Unit Block). Reduced throughput time down to 25 hours from 6.5 days (~85% improvement). Implemented distributed computing and explored enabling multi-threading in the EDA tool flow.
- Implemented via-optimizer based on via wires widths table lookup approach.
- Create DRC auto fixer based on customer request.
- Support GDS/Oasis/NDM generation tool for 14/10/7nm technologies.
- ROM and Datapath functional unit blocks owner for advanced node.
- Full placement and route, timing, extraction, power, Reliability Verification and LVS/DRC ownership and implementation for advanced node projects.
- Wrote script in python and tcl that reads in the layout file, launches NDiff/PDiff DFM(fill) flow with target density and runs icv density checker flow. The script iterates over a range of target densities.

CAD Engineer 7/2011–5/2017
Intel Corporation, Hillsboro, OR

Skills : Project management, High Performance Computing, Multi-threading, Data Analysis, Ruby, Perl, Shell, Yaml, Automation, Algorithms/flows, LVS, DRC, Density, Calibre, ICV, ICC.

- Earned 4 Department Level Awards. Identify problems and gaps, define automation requirements and implement automation in production.
- Owned PreOPC, PostOPC Calibre & Density modules for all tapeout process nodes. Owned support of CalibreViewer tool qualifications and maintenance.
- Chaired and lead the Drawn & Mask Density Working Group. Responsible for generating densities on all layers, for all designs and all technology nodes. Configure CAD flows, qualify new CAD tool versions/OS versions/unix environment changes. Define CAD tool enhancements for advance tech nodes to clear road blocks and getfaster execution.
- Integrated the drawn density CAD tool into mask data generation production line for **all designs across all advanced technology nodes**. Reduced **24 hours** of manual setup time for **multi die products**. Eliminated errors which crop up due to manual setup. Defined CAD tool enhancements required for integration.
- Demonstrated proof of concept to **dynamically generate** CAD flows used to generate mask density per design. Proposed automation eliminates manual flow setup per mask.
- Wrote ruby script that searches for log files with duplicate runs i.e. overlapping execution times for high volume manufacturing. Enabled the automation in **Jenkins** to run as cron job and sends email periodically.
- Wrote ruby script that queries database for released masks and checks for corresponding mask density data has been released or not and display on a **webpage** for users to check. Webpage gets updated weekly through launch trigger using crontab in unix.
- Qualified Intel in house design density CAD tool for advanced/upcoming technologies. Deployed the tool for High Volume manufacturing of **all design tapeins**. Improved throughput time by **> 50%.**
- Set and execute design of experiments to analyze CAD tools suitable for Litho-DFM for HVM production line.Analyzed ICV & Calibre runtime and memory consumption on Litho-DFM flow on 10nm Server Chip. Configured ICV & Calibre tool to run with best possible tool switches for best throughput time & optimal memory usage. Configured tools in master and slave configuration using ruby scripting.
- Wrote **calibre svrf** to extract certain cell locations in full-chip layout for all designs and all tech nodes. Automation eliminated 6 hours of manual setup of laser tools which cuts the die on a wafer.
- Install, deploy new CAD tools into production environment.
- Guide junior engineers and train new hires on the tapeout process tools and methodology.
- Implemented & enabled regression automation for asic & fill integration flow for templates, diering & halo process kits released by Intel Custom Foundry.
- Chaired diering kit release meetings which tracks the status of development/fixes that needs to go in a given kit version.

Marvell Technology Group, Santa Clara, CA

Product Test Engineering Internship, 3/2011 to 5/2011

Skills learned: ATE, Evaluation Board, C, Visual Basic, Batch Scripting, Hardware testplan, Robotic Handler

- Developed Test Plan for one of Marvell's Wireless product.
- Implemented the test plan using batch scripting and C program which controls the handler and evaluation board.
- Involved in interfacing digital multimeter within the C program which takes current reading through the chip.

Academics

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SAN JOSE STATE UNIVERSITY, San Jose, CA

Master of Science in Electrical Engineering, 1/2009 - 5/2011 **CGPA – 3.92**

- **Major:** Analog/Mixed-Signal IC Design
- **Courses:** Linear System Theory, Probability Theory, Signal Processing.
- **Master's Project:**8-bit Current-Mode algorithmic ADC for Quadratic Integrate and Fire circuit(link).
  - Characterized the NMOS and PMOS using gm-id method and Spectre model of TSMC 0.25um pdk.
  - Designed ideal ADC and DAC using VerilogA to find INL, DNL, SNDR, SFDR and ENOB.
  - Designed beta multiplier circuit (current mirror) to generate reference voltages.
  - Achieved SNDR of 40.8dB, SFDR of 51.7dB and ENOB of 6.48 with power dissipation of 8.6mW.
  - Designed 8-bit parallel to serial converter(serializer) that interfaces the output of designed ADC to QIF block.
  - Matched post layout (DRC, LVS, extraction) simulation results with expected results.
- **Grad School Projects:**

1) Wireless channel estimation using USRP based on software defined radios.
2) Full-Custom design & layout of pipelined 4-bit multiplier using 4 phase clocking and dynamic logic.
   a. Achieved operating frequency of 8Ghz using ASU 45nm technology. (link)
   b. Matched post layout (DRC, LVS, extraction) simulation results with expected results.
3) Variable Gain Amplifier design and layout (physical design) for QPSK receiver. (link)
   a. Achieved efficient power transmission by implementing constant return loss circuitry for various gain stages. Designed using 90nm tech with operating frequency of 4GHz.
4) Designed two stage single ended operational trans-conductance amplifier (OTA).(link)
   a. Achieved 60dB gain, 10MHz bandwidth, 0.4 nV/s slew rate and 4ns settling time with phase margin of 63.1 degree. The technology used was gpdk90nm.
5) Designed and analyzed, using Verilog, unsigned 8-bit multiplier.(link)
   a. Verification done using ModelSim and Synthesis was done using Design Analyzer.

THAPAR UNIVERSITY, Patiala, Punjab.

B.E in Electronics & Communication Engineering **CGPA – 8.83**