Attention Please: Under the technology license agreement between MStar and Dolby/SRS/BBE, MStar is obliged not to provide samples that incorporate Dolby/SRS/BBE technology to any third party who is not a qualified licensee of Dolby/SRS/BBE respectively.

FEATURES

- Single display LCD TV controller with PC & multimedia display functions
- Input supports up to UXGA & 1080P
- Panel supports up to UXGA(1600x1200) / WSXGA+(1680x1050)
- TV decoder with comb filter
- Multi-standard TV sound demodulator and decoder
- 10-bit triple-ADC for TV and RGB/YPbPr
- 10-bit video data processing
- Integrated DVI/HDCP/HDMI compliant receiver
- High-quality dual scaling engines & dual 3-D video de-interlacers
- 3-D video noise reduction
- MStarACE-3 picture/color processing engine
- Embedded On-Screen Display (OSD) controller engine
- Built-in MCU supports PWM & GPIO
- Built-in dual-link 8/10-bit LVDS transmitter
- 5-volt tolerant inputs
- Low EMI and power saving features
- 216-pin LQFP

■ NTSC/PAL/SECAM Video Decoder
- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- 3-D Comb filter for NTSC/PAL
- 5 configurable CVBS & Y/C S-video inputs
- Supports Teletext level-1.5, WSS, VPS, Closed-caption, and V-chip
- CVBS video output

■ Video IF for Multi-Standard Analog TV
- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

■ Multi-Standard TV Sound Decoding/Processing
- Supports BTSC/NICAM/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- Support MP3 decode
- Programmable delay for audio/video synchronization
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, and P/G EQ
- Optional advanced surround available (Dolby[1], SRS[2], BBE[3].. etc) **Note**

■ Digital Audio Interface
- I²S digital audio input & output
- S/PDIF digital audio output
- HDMI audio channel processing capability
- Audio Line-In L/R x4
- Audio Line-Out L/R x4
- Built-in audio DAC L/R x4
- Built-in audio ADC L/R x1
- SIF audio input

■ Analog RGB Compliant Input Ports
- Two analog ports support up to UXGA
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

■ DVI/HDCP/HDMI Compliant Input Port
- Two DVI/HDMI input ports with built-in switch
- Supports TMDS clock up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver
- High Definition Multimedia Interface (HDMI) 1.3 compliant receiver with CEC support
- Long-cable tolerant robust receiving
- Support HDTV up to 1080P

[1] **Trademark of Dolby Laboratories**
[2] **Trademark of SRS Labs, Inc.**
[3] **Registered trademark of BBE Sound, Inc.**

- Auto-Configuration/Auto-Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
  - Sync detection for H/V Sync
- High-Performance Scaling Engines
  - Fully programmable shrink/zoom capabilities
  - Nonlinear video scaling supports various modes including Panorama
- Video Processing & Conversion
  - 3-D motion adaptive video de-interlacer
  - Edge-oriented adaptive algorithm for smooth low-angle edges
  - Automatic 3:2 pull-down & 2:2 pull-down detection and recovery
  - MStar 3rd Generation Advanced Color Engine (MStarACE-3) automatic picture enhancement gives:
    - Brilliant and fresh color
    - Intensified contrast and details
    - Vivid skin tone
    - Sharp edge
    - Enhanced depth of field perception
    - Accurate and independent color control
  - sRGB compliance allows end-user to experience the same colors as viewed on CRTs and other displays
  - Support xvYCC color processing
  - Programmable 10-bit RGB gamma CLUT
  - 3-D video noise reduction
  - MPEG artifact removal including de-blocking function
  - Frame rate conversion
- On-Screen OSD Controller
  - 16/256 color palette
  - 1024 1/2/4/8-bit/pixel fonts
  - Supports texture function
  - Supports 4K attribute/code
  - Horizontal and vertical stretch of OSD menus
  - Pattern generator for production test
  - Supports OSD MUX and alpha blending capability
  - Supports blinking and scrolling for closed caption applications
- Hardware JPEG
  - Supports sequential mode, single scan
  - Supports both color picture and grayscale picture
  - Operates in scan unit; hardware decoder will handle the bit stream after scan header
  - Supports programmable region of interest (ROI)
  - Supports format: 422/411/420/444/422T
  - Decoded picture will be stored in DRAM with UYVY format
  - Supports scaling down ratio: 1/2, 1/4, 1/8, applied to height and width simultaneously
- LVDS Panel Interface
  - Supports 8/10-bit dual link LVDS up to UXGA(1600x1200) / WSXGA+(1680x1050)
  - Supports 2 data output formats: Thine & TI data mappings
  - Compatible with TIA/EIA
  - Dithering with 6/8 bits options
  - Reduced swing for LVDS for low EMI
  - Supports flexible spread spectrum frequency with 360Hz~11.8MHz and up to 25% modulation
- Integrated Micro Controller
  - Embedded 8032 micro controller
  - Configurable PWM's and GPIO's
  - Low-speed ADC inputs for system control
  - SPI bus for external flash
  - Supports external MCU option controlled through 4-wire double-data-rate direct MCU bus
- External Connection/Component
  - USB 2.0 port with internal switch to host controller
  - 16-bit data bus for external frame buffer (DDR DRAM)
  - All system clocks synthesized from a single external clock
  - Integrated power management control with independent power plant to support deep sleep, and wake-up from various input

GENERAL DESCRIPTION

The MST6M16JS is a high performance and fully integrated IC for multi-function LCD monitor/TV with resolutions up to WUXGA (1920x1200). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard TV video and audio decoder, a video de-interlacer, a scaling engine, the MStarACE-3 color engine, an on-screen display controller and a built-in output panel interface. By use of external frame buffer, PIP/POP is provided for multimedia applications. Furthermore, 3-D video decoding and processing are fulfilled for high-quality TV applications. To further reduce system costs, the MST6M16JS also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		TBD	TBD	LSB
Integral Nonlinearity		TBD		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	165			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		165	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		15		ps/°C
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		1.5		V
Output High		2.0		V

Parameter	Min	Typ	Max	Unit
AUDIO				
ADC Input		2.0		V p-p
DAC Output		2.0		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p
FSSW Input[1]	0		1.8	V
SAR ADC Input	0		3.3	V
FB ADC Input[2]	0		1.25	V

Specifications subject to change without notice.
Notes:
1. **Input full scale is typically 1.8V, but input range is 0 ~ 3.3V.**
2. **Input full scale is 1.25V, but input range is 0 ~ 3.3V.**

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}			3.6	V
2.5V Supply Voltages	V_{VDD_25}			2.75	V
1.26V Supply Voltages	V_{VDD_126}			1.32	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$			5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}			V_{VDD_33}	V
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Junction Temperature	T_J			150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
MST6M16JS-LF	0°C to +70°C	LQFP	**216**
MST6M16JS-LF-S1	0°C to +70°C	LQFP	**216**
MST6M16JS-LF-S2	0°C to +70°C	LQFP	**216**
MST6M16JS-LF-S3	0°C to +70°C	LQFP	**216**
MST6M16JS-LF-S4	0°C to +70°C	LQFP	**216**
MST6M16JS-LF-S5	0°C to +70°C	LQFP	**216**

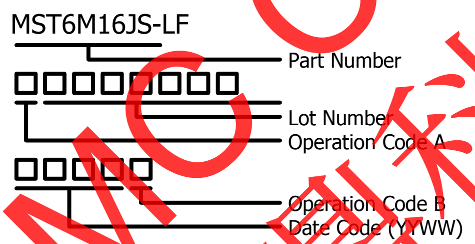
Note on product suffix:
1. "LF": Lead-free version.
2. "S1" ~ "S5": Advanced surround features.

Code	Description
S1	SRS TruSurround XT™
S2	Dolby® ProLogic® II + Dolby® Virtual Speaker
S3	Dolby® ProLogic® II + Virtual Dolby® Surround
S4	BBE®
S5	BBE® ViVA™

The SRS TruSurround XT™ technology rights incorporated in the MST6M16JS are owned by SRS Labs, a U.S. Corporation and licensed to MStar. Purchaser of MST6M16JS must sign a license for use of the chip and display of the SRS Labs trademarks. Any products incorporating the MST6M16JS must be sent to SRS Labs for review. SRS TruSurround XT is protected under US and foreign patents issued and/or pending. SRS TruSurround XT, SRS and (O) symbol are trademarks of SRS Labs, Inc. in the United States and selected foreign countries. Neither the purchase of the MST6M16JS, nor the corresponding sale of audio enhancement equipment conveys the right to sell commercialized recordings made with any SRS technology. SRS Labs requires all set makers to comply with all rules and regulations as outlined in the SRS Trademark Usage Manual separately provided.

Supply of this Implementation of Dolby Technology does not convey a license nor imply a right under any patent, or any other Industrial or Intellectual Property Right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. Companies planning to use this Implementation in products must obtain a license from Dolby Laboratories Licensing Corporation before designing such products.

MARKING INFORMATION



DISCLAIMER

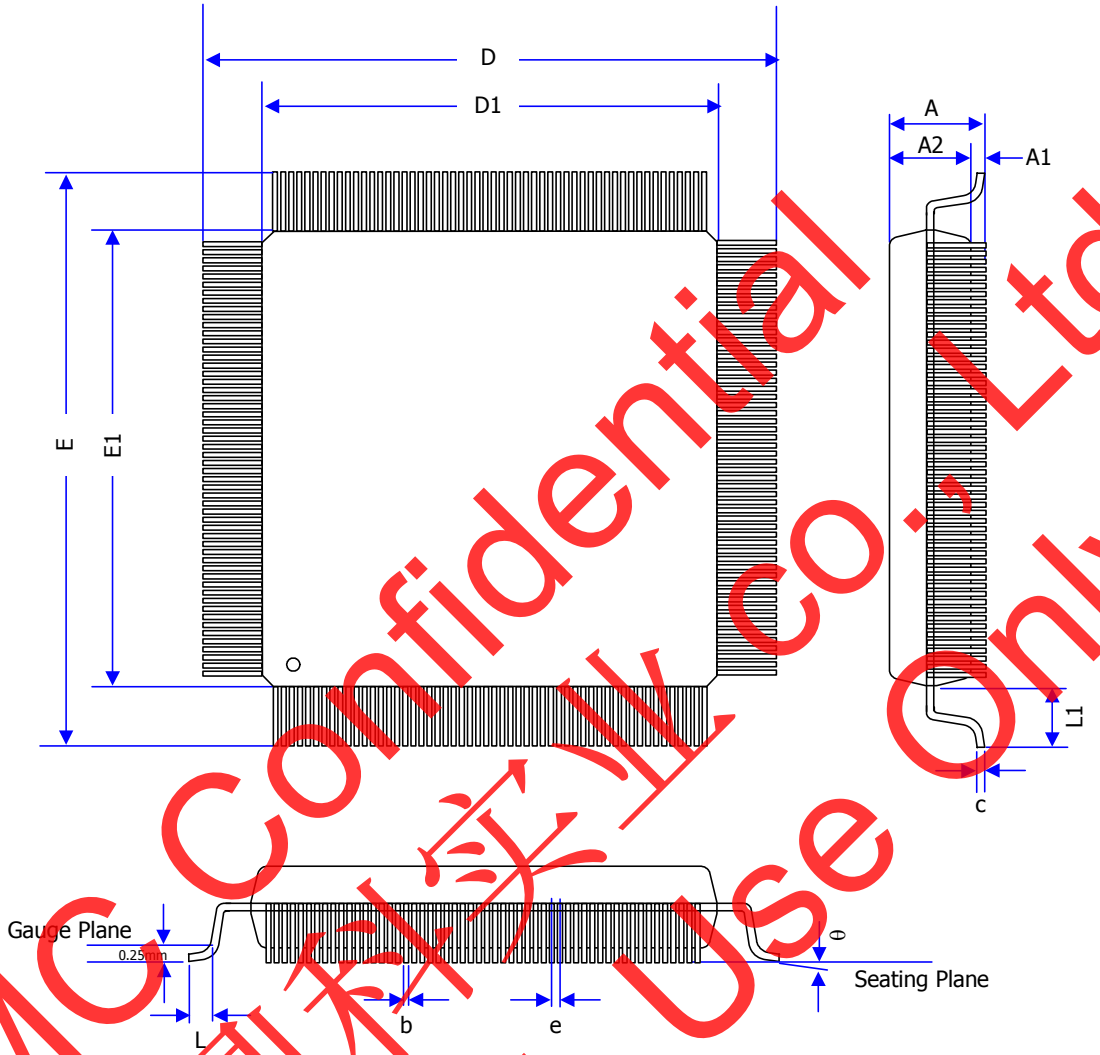
MSTAR SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. NO RESPONSIBILITY IS ASSUMED BY MSTAR SEMICONDUCTOR ARISING OUT OF THE APPLICATION OR USER OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST6M16JS comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST6M16JS_ds_v01	• Initial release	Dec 2008

MECHANICAL DIMENSIONS



Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.60	-	-	0.063
A1	0.05	-	0.15	0.002	-	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	26.00			1.024		
D1	24.00			0.945		
E	26.00			1.024		
E1	24.00			0.945		

Symbol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
b	-	0.18	-	-	0.007	-
c	-	0.14	-	-	0.006	-
e	0.40 BSC			0.016 BSC		

REGISTER DESCRIPTION

ISP Register (Bank = 08)

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (0800h)	**REG0800**	**7:0**	**Default : 0x55**	**Access : R/W**
	ISP_PASSWORD[7:0]	7:0	ISP Password 0xAAAA. If password is correct, enable ISP. If password is incorrect, disable ISP.	
00h (0801h)	**REG0801**	**7:0**	**Default : 0x55**	**Access : R/W**
	ISP_PASSWORD[15:8]	7:0	See description of '0800h'.	
01h (0802h)	**REG0802**	**7:0**	**Default : 0x00**	**Access : WO**
	SPI_COMMAND[7:0]	7:0	SPI command. Writing data to this port will cause ISP to start operation.	
02h (0804h)	**REG0804**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDRESS1[7:0]	7:0	SPI address 1, A[7:0].	
02h (0805h)	**REG0805**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDERSS2[7:0]	7:0	SPI address 2, A[15:8].	
03h (0806h)	**REG0806**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADDRESS3[7:0]	7:0	SPI address 3, A[23:16].	
04h (0808h)	**REG0808**	**7:0**	**Default : 0x00**	**Access : WO**
	WDATA[7:0]	7:0	SPI write data register.	
05h (080Ah)	**REG080A**	**7:0**	**Default : 0x00**	**Access : RO**
	RDATA[7:0]	7:0	SPI read data register.	
06h (080Ch)	**REG080C**	**7:0**	**Default : 0x04**	**Access : R/W**
	SPI_CLK_DIV16	7	SPI_CLOCK = MCU_CLOCK/16.	
	SPI_CLK_DIV8	6	SPI_CLOCK = MCU_CLOCK/8.	
	-	5:3	Reserved.	
	SPI_CLK_DIV4	2	SPI_CLOCK = MCU_CLOCK/4.	
	-	1	Reserved.	
	SPI_CLK_DIV2	0	SPI_CLOCK = MCU_CLOCK/2.	
06h (080Dh)	**REG080D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPI_CLK_DIV128	2	SPI_CLOCK = MCU_CLOCK/128.	
	SPI_CLK_DIV64	1	SPI_CLOCK = MCU_CLOCK/64.	
	SPI_CLK_DIV32	0	SPI_CLOCK = MCU_CLOCK/32.	

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
07h (080Eh)	**REG080E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DEVICE_SELECT[2:0]	2:0	Select Device. 000: PMC.MXIC. 001: NextFlash. 010: ST. 011: SST. 100: ATMEL.	
08h (0810h)	**REG0810**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SPI_CE_CLR	0	SPI chip enable clear. Software can force SPI chip disable at burst SPI read/write. This bit is a write-then-clear register. 1: Clear. 0: Not clear.	
09h (0812h)	**REG0812**	**7:0**	**Default : 0x01**	**Access : R/W**
	TCES_TIME[7:0]	7:0	SPI chip enable setup/hold time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clocks. 0x000f: Delay 16 SPI clocks. 0xffff: Delay 64k SPI clocks. Default: Delay 2 SPI clocks.	
09h (0813h)	**REG0813**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCES_TIME[15:8]	7:0	See description of '0812h'.	
0Ah (0814h)	**REG0814**	**7:0**	**Default : 0xF3**	**Access : R/W**
	TBP_TIME[7:0]	7:0	Byte-Program time for Device SST. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clocks. 0x000f: Delay 16 SPI clocks. 0xffff: Delay 64k SPI clocks. Default: Delay 500 SPI clocks. Assume SPI clock is 40ns, delay 500*40 = 20 us.	
0Ah (0815h)	**REG0815**	**7:0**	**Default : 0x01**	**Access : R/W**
	TBP_TIME[15:8]	7:0	See description of '0814h'.	
0Bh (0816h)	**REG0816**	**7:0**	**Default : 0x04**	**Access : R/W**
	TCEH_TIME[7:0]	7:0	SPI chip enable pulse high time. 0x0000: Delay 1 SPI clock.	

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0x0001: Delay 2 SPI clocks. 0x000f: Delay 16 SPI clocks. 0xffff: Delay 64k SPI clocks. Default: Delay 5 SPI clocks.	
0Bh (0817h)	**REG0817**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCEH_TIME[15:8]	7:0	See description of '0816h'.	
0Ch (0818h)	**REG0818**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SPI_RD_REQ	0	SPI Read Data Request, for CPU to read SPI data via RIU. If CPU reads SPI data via XIU, request is not needed.	
0Dh (081Ah)	**REG081A**	**7:0**	**Default : 0x14**	**Access : R/W**
	ISP_RP_ADR1[7:0]	7:0	Programmable ISP read port address[15:0].	
0Dh (081Bh)	**REG081B**	**7:0**	**Default : 0xC2**	**Access : R/W**
	ISP_RP_ADR1[15:8]	7:0	See description of '081Ah'.	
0Eh (081Ch)	**REG081C**	**7:0**	**Default : 0x81**	**Access : R/W**
	ISP_RP_ADR2[7:0]	7:0	Programmable ISP read port address[31:0].	
0Eh (081Dh)	**REG081D**	**7:0**	**Default : 0x1F**	**Access : R/W**
	ISP_RP_ADR2[15:8]	7:0	See description of '081Ch'.	
0Fh (081Eh)	**REG081E**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	ENDIAN_SEL_SPI	0	0: Big endian. 1: Little endian.	
10h (0820h)	**REG0820**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ISP_ACTIVE	0	ISP active flag.	
11h (0822h)	**REG0822**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CPU_ACTIVE	1	CPU active flag.	
	-	0	Reserved.	
13h (0826h)	**REG0826**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	ISP_FSM[5:0]	5:0	ISP FSM.	
14h (0828h)	**REG0828**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPI_MASTER_FSM[2:0]	2:0	SPI master FSM.	
15h (082Ah)	**REG082A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_RD_DATA_RDY	0	SPI Read Data Ready flag. 1: Read data ready. 0: Read data not ready.	
16h (082Ch)	**REG082C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_WR_DATA_RDY	0	SPI Write Data Ready flag. 1: Write data ready. 0: Write data not ready.	
17h (082Eh)	**REG082E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	SPI_WR_CM_RDY	0	SPI Write Command Ready flag. 1: Write command ready. 0: Write command not ready.	
18h (0830h)	**REG0830**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CPU_RST_FM_ISP	0	ISP generated reset to CPU. When ISP programming is done, software can issue a reset to CPU.	
19h (0832h)	**REG0832**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ISP_OLD_EN	0	Read flag for ISP_OLD_EN.	
20h (0840h)	**REG0840**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FORCE_ISP_IDLE	0	Force ISP Idle.	
21h (0842h)	**REG0842**	**7:0**	**Default : 0x00**	**Access : R/W**
	AAI_NUM[7:0]	7:0	For SST SPI Flash use. In AAI mode, set how much data will be written. 0x0000: For 1-byte programming. 0x0001: For 2-byte programming. 0xFFFF: For 64-kbyte programming.	
21h (0843h)	**REG0843**	**7:0**	**Default : 0x00**	**Access : R/W**
	AAI_NUM[15:8]	7:0	See description of '0842h'.	

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
22h (0844h)	**REG0844**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAGE_PRO_REG	7	FORCE SPI COMMAND: Force PAGE PROGRAMMING.	
	FAST_READ_REG	6	FORCE SPI COMMAND: Force FAST READ.	
	READ_REG	5	FORCE SPI COMMAND: Force READ.	
	WRCR_REG	4	FORCE SPI COMMAND: Force WRCR.	
	RDCR_REG	3	FORCE SPI COMMAND: Force RDCR.	
	WRSR_REG	2	FORCE SPI COMMAND: Force WRSR.	
	RDSR_REG	1	FORCE SPI COMMAND: Force RDSR.	
	AAI_REG	0	FORCE SPI COMMAND: Force AAI mode.	
22h (0845h)	**REG0845**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:2	Reserved.	
	MAN_ID_REG	1	FORCE SPI COMMAND: Force READ MANUFACTURER ID.	
	B_ERASE_REG	0	FORCE SPI COMMAND: Force BLOCK ERASE.	
25h (084Ah)	**REG084A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MODE[7:0]	7:0	User defined SPI waveform. 0x7777: User defined. Others: Not user defined. Before entering TEST_MODE, make sure ISP/DMA is disabled.	
25h (084Bh)	**REG084B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MODE[15:8]	7:0	See description of '084Ah'.	
26h (084Ch)	**REG084C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_CEB	0	User generated SPI chip enable waveform.	
27h	**REG084E**	**7:0**	**Default : 0x00**	**Access : R/W**

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(084Eh)	-	7:1	Reserved.	
	TEST_SPI_SCK	0	User generated SPI clock waveform.	
28h (0850h)	**REG0850**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	TEST_SPI_SI	0	User generated SPI data waveform.	
29h (0852h)	**REG0852**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	TEST_SPI_SO	0	SPI data output for RIU read. Delay 1us for every setting (test mode). Example 1: W (0x21, 0x0) --> delay 1us --> W (0x23, 0x1) --> delay 1us --> W (0x22, 0x1) --> delay 1us --> W (0x22, 0x0) --> delay 1us ..... --> W (0x21, 0x1). Example 2: W (0x21, 0x0) --> delay 1us --> W (0x22, 0x1) --> delay 1us --> W (0x22, 0x0) --> delay 1us --> R (0x24) --> delay 1us ..... -> W (0x21, 01).	
2Ah (0854h)	**REG0854**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRIGGER_MODE[7:0]	7:0	0x3333: Trigger mode. Others: Not Trigger mode. Before entering Trigger mode, make sure ISP/DMA is disabled.	
2Ah (0855h)	**REG0855**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRIGGER_MODE[15:8]	7:0	See description of '0854h'.	
30h (0860h)	**REG0860**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	DMA_START	0	DMA Start, DMA between MIU and SPI Device.	
31h (0862h)	**REG0862**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_CNT[7:0]	7:0	DMA transfer size (byte).	
31h (0863h)	**REG0863**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_CNT[15:8]	7:0	See description of '0862h'.	
32h (0864h)	**REG0864**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MIU_START_ADR1[7:0]	7:0	DMA source address, unit = word address, MIU Address[15:0].	
32h (0865h)	**REG0865**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MIU_START_ADR1[15:8]	7:0	See description of '0864h'.	
33h	**REG0866**	**7:0**	**Default : 0x00**	**Access : R/W**

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(0866h)	DMA_MIU_START_ADR2[7:0]	7:0	DMA source address, unit = word address, MIU Address[31:16].	
33h (0867h)	**REG0867**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MIU_START_ADR2[15:8]	7:0	See description of '0866h'.	
34h (0868h)	**REG0868**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	DMA_DONE	1	DMA done flag.	
	DMA_BUSY	0	DMA busy flag.	
35h (086Ah)	**REG086A**	**7:0**	**Default : 0x00**	**Access : RO**
	DMA_CNT_STATUS[7:0]	7:0	DMA counter status.	
35h (086Bh)	**REG086B**	**7:0**	**Default : 0x00**	**Access : RO**
	DMA_CNT_STATUS[15:8]	7:0	See description of '086Ah'.	
36h (086Ch)	**REG086C**	**7:0**	**Default : 0x01**	**Access : R/W**
	CHIP_SELECT8	7	Chip select for SPI Device 6. 1: Enable. 0: Disable.	
	CHIP_SELECT7	6	Chip select for SPI Device 5. 1: Enable. 0: Disable.	
	CHIP_SELECT6	5	Chip select for SPI Device 4. 1: Enable. 0: Disable.	
	CHIP_SELECT5	4	Chip select for SPI Device 3. 1: Enable. 0: Disable.	
	CHIP_SELECT4	3	Chip select for SPI Device 2. 1: Enable. 0: Disable.	
	CHIP_SELECT3	2	Chip select for SPI Device 1. 1: Enable. 0: Disable.	
	CHIP_SELECT2	1	Chip select for SPI Flash 2. 1: Enable. 0: Disable.	
	CHIP_SELECT1	0	Chip select for SPI Flash 1. 1: Enable.	

ISP Register (Bank = 08)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable.	
37h (086Eh)	**REG086E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CPHA	1	Configure the data sampling point. When 0, data is sampled when "SCLK" goes to active state (see CPOL). When 1, data is sampled when "SCLK" goes to idle state (see CPOL).	
	CPOL	0	Clock Polarity. Configure the idle state of "SCLK" when SPI is enabled (when disabled, "SCLK" is at high level). When 1, the "SCLK" output is set (SCLK = 1), otherwise it is cleared (SCLK = 0).	

MCU Register (Bank = 10)

MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1000h)	**REG1000**	**7:0**	**Default : 0x01**	**Access : R/W**
	SRAM_START_ADDR_1[7:0]	7:0	SRAM Start Address[23:16].	
00h (1001h)	**REG1001**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAM_START_ADDR_1[15:8]	7:0	See description of '1000h'.	
01h (1002h)	**REG1002**	**7:0**	**Default : 0x01**	**Access : R/W**
	SRAM_END_ADDR_1[7:0]	7:0	SRAM End Address[23:16].	
01h (1003h)	**REG1003**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAM_END_ADDR_1[15:8]	7:0	See description of '1002h'.	
02h (1004h)	**REG1004**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAM_START_ADDR_0[7:0]	7:0	SRAM End Address[15:0].	
02h (1005h)	**REG1005**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAM_START_ADDR_0[15:8]	7:0	See description of '1004h'.	
03h (1006h)	**REG1006**	**7:0**	**Default : 0x00**	**Access : R/W**
	SRAM_END_ADDR_0[7:0]	7:0	SRAM End Address[15:0].	
03h (1007h)	**REG1007**	**7:0**	**Default : 0x80**	**Access : R/W**
	SRAM_END_ADDR_0[15:8]	7:0	See description of '1006h'.	
04h (1008h)	**REG1008**	**7:0**	**Default : 0x01**	**Access : R/W**
	DRAM_START_ADDR_1[7:0]	7:0	DRAM Start Address[23:16].	
04h (1009h)	**REG1009**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_START_ADDR_1[15:8]	7:0	See description of '1008h'.	
05h (100Ah)	**REG100A**	**7:0**	**Default : 0x0F**	**Access : R/W**
	DRAM_END_ADDR_1[7:0]	7:0	DRAM End Address[23:16].	
05h (100Bh)	**REG100B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_END_ADDR_1[15:8]	7:0	See description of '100Ah'.	
06h (100Ch)	**REG100C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DRAM_START_ADDR_0[7:0]	7:0	DRAM Start Address[15:0].	
06h (100Dh)	**REG100D**	**7:0**	**Default : 0x80**	**Access : R/W**
	DRAM_START_ADDR_0[15:8]	7:0	See description of '100Ch'.	
07h (100Eh)	**REG100E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DRAM_END_ADDR_0[7:0]	7:0	DRAM End Address[15:0].	
07h (100Fh)	**REG100F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DRAM_END_ADDR_0[15:8]	7:0	See description of '100Eh'.	

MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
08h (1010h)	**REG1010**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_1[7:0]	7:0	SPI Start Address[23:16].	
08h (1011h)	**REG1011**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_1[15:8]	7:0	See description of '1010h'.	
09h (1012h)	**REG1012**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_END_ADDR_1[7:0]	7:0	SPI End Address[23:16].	
09h (1013h)	**REG1013**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_END_ADDR_1[15:8]	7:0	See description of '1012h'.	
0Ah (1014h)	**REG1014**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_0[7:0]	7:0	SPI Start Address[15:0].	
0Ah (1015h)	**REG1015**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPI_START_ADDR_0[15:8]	7:0	See description of '1014h'.	
0Bh (1016h)	**REG1016**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SPI_END_ADDR_0[7:0]	7:0	SPI End Address[15:0].	
0Bh (1017h)	**REG1017**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SPI_END_ADDR_0[15:8]	7:0	See description of '1016h'.	
0Ch (1018h)	**REG1018**	**7:0**	**Default : 0x02**	**Access : R/W**
	MCU_BANK_USE_XFR	7	Use XFR to switch bank.	
	TEST_SEL[2:0]	6:4	Test bus selection.	
	ICACHE_RSTZ	3	Icache enable.	
	DRAM_EN	2	DRAM enable.	
	SPI_EN	1	SPI enable.	
	SRAM_EN	0	SRAM enable.	
0Ch (1019h)	**REG1019**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU_BANK_XFR[7:0]	7:0	XFR bank (64KB).	
0Dh (101Ah)	**REG101A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TWA[7:0]	7:0	TWA for RIU bridge.	
0Dh (101Bh)	**REG101B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAW[7:0]	7:0	TAW for RIU bridge.	
20h (1040h)	**REG1040**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_OV[7:0]	7:0	P0 override by P0_REG. 0: Disable. 1: Enable.	

MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (1041h)	**REG1041**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_REG[7:0]	7:0	Data to override P0.	
21h (1042h)	**REG1042**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OV[7:0]	7:0	P1 override by P1_REG. 0: Disable. 1: Enable.	
21h (1043h)	**REG1043**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_REG[7:0]	7:0	Data to override P1.	
22h (1044h)	**REG1044**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OV[7:0]	7:0	P2 override by P2_REG. 0: Disable. 1: Enable.	
22h (1045h)	**REG1045**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_REG[7:0]	7:0	Data to override P2.	
23h (1046h)	**REG1046**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OV[7:0]	7:0	P3 override by P3_REG. 0: Disable. 1: Enable.	
23h (1047h)	**REG1047**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_REG[7:0]	7:0	Data to override P3.	
24h (1048h)	**REG1048**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_CTRL[7:0]	7:0	MCU Port 0 output enable control.	
25h (104Ah)	**REG104A**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_OE[7:0]	7:0	MCU Port 0 output enable.	
26h (104Ch)	**REG104C**	**7:0**	**Default : 0x00**	**Access : R/W**
	P0_IN[7:0]	7:0	MCU Port 0 output enable from output data.	
27h (104Eh)	**REG104E**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_CTRL[7:0]	7:0	MCU Port 1 output enable control.	
28h (1050h)	**REG1050**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_OE[7:0]	7:0	MCU Port 1 output enable.	
29h (1052h)	**REG1052**	**7:0**	**Default : 0x00**	**Access : R/W**
	P1_IN[7:0]	7:0	MCU Port 1 output enable from output data.	
2Ah (1054h)	**REG1054**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_CTRL[7:0]	7:0	MCU Port 2 output enable control.	

MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Bh (1056h)	**REG1056**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_OE[7:0]	7:0	MCU Port 2 output enable.	
2Ch (1058h)	**REG1058**	**7:0**	**Default : 0x00**	**Access : R/W**
	P2_IN[7:0]	7:0	MCU Port 2 output enable from output data.	
2Dh (105Ah)	**REG105A**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_CTRL[7:0]	7:0	MCU Port 3 output enable control.	
2Eh (105Ch)	**REG105C**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_OE[7:0]	7:0	MCU Port 3 output enable.	
2Fh (105Eh)	**REG105E**	**7:0**	**Default : 0x00**	**Access : R/W**
	P3_IN[7:0]	7:0	MCU Port 3 output enable from output data.	
40h (1080h)	**REG1080**	**7:0**	**Default : 0x55**	**Access : R/W**
	RESET_CPU0[7:0]	7:0	Reset CPU 0.	
40h (1081h)	**REG1081**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RESET_CPU0[15:8]	7:0	See description of '1080h'.	
41h (1082h)	**REG1082**	**7:0**	**Default : 0x55**	**Access : R/W**
	RESET_CPU1[7:0]	7:0	Reset CPU 1.	
41h (1083h)	**REG1083**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RESET_CPU1[15:8]	7:0	See description of '1082h'.	
42h (1084h)	**REG1084**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU0[7:0]	7:0	S/W reset CPU 0 (8051).	
42h (1085h)	**REG1085**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU0[15:8]	7:0	See description of '1084h'.	
43h (1086h)	**REG1086**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU1[7:0]	7:0	S/W reset CPU 1 (32-bit MCU).	
43h (1087h)	**REG1087**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_RESET_CPU1[15:8]	7:0	See description of '1086h'.	
58h (10B0h)	**REG10B0**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR0[7:0]	7:0	HK MCU program counter.	
58h (10B1h)	**REG10B1**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR0[15:8]	7:0	See description of '10B0h'.	
59h (10B2h)	**REG10B2**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR0[23:16]	7:0	See description of '10B0h'.	
59h	**REG10B3**	**7:0**	**Default : 0x00**	**Access : RO**

MCU Register (Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10B3h)	IB_DATAI0[7:0]	7:0	HK MCU inst return data.	
5Ah (10B4h)	**REG10B4**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR1[7:0]	7:0	VD MCU program counter.	
5Ah (10B5h)	**REG10B5**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR1[15:8]	7:0	See description of '10B4h'.	
5Bh (10B6h)	**REG10B6**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR1[23:16]	7:0	See description of '10B4h'.	
5Bh (10B7h)	**REG10B7**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_DATAI1[7:0]	7:0	VD MCU inst return data.	
5Ch (10B8h)	**REG10B8**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR2[7:0]	7:0	TT MCU program counter.	
5Ch (10B9h)	**REG10B9**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR2[15:8]	7:0	See description of '10B8h'.	
5Dh (10BAh)	**REG10BA**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_ADDR2[23:16]	7:0	See description of '10B8h'.	
5Dh (10BBh)	**REG10BB**	**7:0**	**Default : 0x00**	**Access : RO**
	IB_DATAI2[7:0]	7:0	TT MCU inst return data.	
70h (10E0h)	**REG10E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ERAM_LB[7:0]	7:0	ERAM map HK XDATA low boundary (unit: 1k). Recommended setting: 0x14.	
70h (10E1h)	**REG10E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ERAM_HB[7:0]	7:0	ERAM map HK XDATA high boundary (unit: 1k). Recommended setting: 0x14.	
72h (10E4h)	**REG10E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	XD2ERAM_ADRH[7:0]	7:0	ERAM base address (unit: 1k, 0x000-0x3FF).	
73h (10E6h)	**REG10E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	XD2ERAM_EN	0	Enable ERAM mapping.	

MIU1 Register (Bank = 11)

MIU1 Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (11E0h)	**REG11E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RDPTG_EN	3	Functional test: Read pattern generator enable.	
	WDCRC_STOP	2	Functional test: CRC test stop.	
	WDCRC_START	1	Functional test: CRC test start.	
	WDCRC_RST	0	Functional test: Software reset.	
71h (11E2h)	**REG11E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_MODE[7:0]	7:0	Pattern generator mode.	
71h (11E3h)	**REG11E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_MODE[15:8]	7:0	See description of '11E2h'.	
72h (11E4h)	**REG11E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA0[7:0]	7:0	Pattern generator data0.	
72h (11E5h)	**REG11E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA0[15:8]	7:0	See description of '11E4h'.	
73h (11E6h)	**REG11E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA1[7:0]	7:0	Pattern generator data1.	
73h (11E7h)	**REG11E7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA1[15:8]	7:0	See description of '11E6h'.	
74h (11E8h)	**REG11E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA2[7:0]	7:0	Pattern generator data2.	
74h (11E9h)	**REG11E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA2[15:8]	7:0	See description of '11E8h'.	
75h (11EAh)	**REG11EA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA3[7:0]	7:0	Pattern generator data3.	
75h (11EBh)	**REG11EB**	**7:0**	**Default : 0x00**	**Access : R/W**
	PTN_DATA3[15:8]	7:0	See description of '11EAh'.	
76h (11ECh)	**REG11EC**	**7:0**	**Default : 0x00**	**Access : RO**
	ADDR_CRC[7:0]	7:0	CRC result.	
76h (11EDh)	**REG11ED**	**7:0**	**Default : 0x00**	**Access : RO**
	ADDR_CRC[15:8]	7:0	See description of '11ECh'.	
77h (11EEh)	**REG11EE**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA0_CRC[7:0]	7:0	Word0 CRC.	

MIU1 Register (Bank = 11)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
77h (11EFh)	**REG11EF**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA0_CRC[15:8]	7:0	See description of '11EEh'.	
78h (11F0h)	**REG11F0**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA1_CRC[7:0]	7:0	Word1 CRC.	
78h (11F1h)	**REG11F1**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA1_CRC[15:8]	7:0	See description of '11F0h'.	
79h (11F2h)	**REG11F2**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA2_CRC[7:0]	7:0	Word2 CRC.	
79h (11F3h)	**REG11F3**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA2_CRC[15:8]	7:0	See description of '11F2h'.	
7Ah (11F4h)	**REG11F4**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA3_CRC[7:0]	7:0	Word3 CRC.	
7Ah (11F5h)	**REG11F5**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA3_CRC[15:8]	7:0	See description of '11F4h'.	

MIU0 Register (Bank = 12)

MIU0 Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1200h)	**REG1200**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	INIT_MIU	0	Issue initial MIU cycle.	
00h (1201h)	**REG1201**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	INIT_DONE	7	Initialization done flag.	
	-	6:0	Reserved.	
01h (1202h)	**REG1202**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDR_DQ	7	For pad select.	
	DDR	6	DDR/SDR select.	
	DRAM_BUS[1:0]	5:4	DRAM bus width. 0: 16b. 1: 32b. 2: 64b.	
	DYNAMIC_CK	3	Dynamically turn on/off output clock.	
	DYNAMIC_CKE	2	Dynamically turn on CKE.	
	SELF_REFRESH	1	Enter self refresh cycle.	
	CKE	0	Turn on CKE.	
01h (1203h)	**REG1203**	**7:0**	**Default : 0x70**	**Access : R/W**
	CS_Z	7	Chip select, low active.	
	ADR_OENZ	6	Address output enable, low active.	
	DQ_OENZ	5	Data output enable, low active.	
	CKE_OENZ	4	CKE output enable, low active.	
	-	3	Reserved.	
	COL_SIZE[1:0]	2:1	00: 8-column. 01: 9-column. 10: 10-column.	
	4BA	0	0: 2-bank. 1: 4-bank.	
02h (1204h)	**REG1204**	**7:0**	**Default : 0x40**	**Access : R/W**
	RD_TIMING[3:0]	7:4	Read data cycle.	
	-	3	Reserved.	
	FORCE_DDR_RD_ACT	2	Force DDR_RD_ACT.	
	RD_MCK_SEL	1	Read data clock select.	

MIU0 Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Feedback. 1: Internal.	
	RD_IN_PHASE	0	Read data phase. 0: Normal. 1: Inverse.	
02h (1205h)	**REG1205**	**7:0**	**Default : 0x03**	**Access : R/W**
	SRC_MCLK_DLY[1:0]	7:6	SDRAM source clock option: delay selection.	
	SRC_MCLK_INV	5	SDRAM source clock option. 0: MCLK. 1: MCLK_N.	
	SRC_MCLK_SEL	4	SDRAM source clock option. 0: MCLK. 1: PLL.	
	-	3	Reserved.	
	CAS_LATENCY[2:0]	2:0	Cas latency. SDR: 2/3. DDR: 2/6.	
03h (1206h)	**REG1206**	**7:0**	**Default : 0x00**	**Access : R/W**
	TREFPERIOD[7:0]	7:0	Refresh cycle, unit is 16T.	
03h (1207h)	**REG1207**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PRIORITY_SW	6	Switch the priority of group 0 and group 1.	
	MCP_TYPE	5	MCP bonding type selection.	
	MCP_EN	4	MCP pad-share enable.	
	-	3	Reserved.	
	SIZE_MASK[2:0]	2:0	Mask high address > DRAM support.	
04h (1208h)	**REG1208**	**7:0**	**Default : 0xC8**	**Access : R/W**
	TRC[3:0]	7:4	DRAM TRC setting.	
	TRAS[3:0]	3:0	DRAM TRAS setting.	
04h (1209h)	**REG1209**	**7:0**	**Default : 0x33**	**Access : R/W**
	TRP[3:0]	7:4	DRAM TRP setting.	
	TRCD[3:0]	3:0	DRAM TRCD setting.	
05h (120Ah)	**REG120A**	**7:0**	**Default : 0x62**	**Access : R/W**
	TWR[3:0]	7:4	DRAM TWR timing.	

MIU0 Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TRRD[3:0]	3:0	DRAM TRRD timing.	
05h (120Bh)	**REG120B**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	TMRD[3:0]	3:0	DRAM TMRD timing.	
06h (120Ch)	**REG120C**	**7:0**	**Default : 0x63**	**Access : R/W**
	W2R_OEN_DLY[3:0]	7:4	Write to read output enable delay cycle. W2R_DLY + 3.	
	W2R_DLY[3:0]	3:0	Write to read command delay cycle.	
06h (120Dh)	**REG120D**	**7:0**	**Default : 0x86**	**Access : R/W**
	R2W_OEN_DLY[3:0]	7:4	Read to write output enable delay cycle. R2W_DLY + 2.	
	R2W_DLY[3:0]	3:0	Read to write command delay cycle.	
07h (120Eh)	**REG120E**	**7:0**	**Default : 0x0E**	**Access : R/W**
	BA_REORDER[2:0]	7:5	Reorder bank address.	
	TRFC[4:0]	4:0	DRAM TRFC timing.	
0Ah (1214h)	**REG1214**	**7:0**	**Default : 0x00**	**Access : R/W**
	MRD_EXT[7:0]	7:0	Extend Mode Register setting value.	
0Ah (1215h)	**REG1215**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESET_DLL	7	Reset DLL.	
	-	6	Reserved.	
	MRD_EXT[13:8]	5:0	See description of '1214h'.	
0Eh (121Ch)	**REG121C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MCP_IN_PHASE	6	MCP read data DFF clock phase selection.	
	MCP_RD_TIMING[1:0]	5:4	MCP read data timing selection.	
	MCP_DIN_BYPASS	3	MCP data pad DFF bypass enable.	
	MCP_D_SWAP	2	MCP data swap for different DRAM type.	
	MCP_MCSZ_OUT	1	MCP CSZ out.	
	MCP_PAD_EN	0	MCP pad enable.	
0Fh (121Eh)	**REG121E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DFT_ADRMD	1	For DFT coverage.	
	SW_RST_MIU	0	MIU software reset.	

MIU0 Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
10h (1220h)	**REG1220**	**7:0**	**Default : 0x09**	**Access : R/W**
	DDFSET[3:0]	7:4	DDR_FREQ (DDR clock frequency). = (MPLL_FREQ*128*LOOP_DIV1*LOOP_DIV2)/ (DDFSET*IN_DIV1*IN_DIV2). DDR Frequency Set. DDFSET[9:0] must be located between 290 and 832 (Dec).	
	DDRIP[1:0]	3:2	DDR clock generator charge pump current. 00: 0.25uA. 01: 0.50uA. 10: 1.5uA (default). 11: 3.0uA.	
	DDRRP[1:0]	1:0		
10h (1221h)	**REG1221**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	DDFSET[9:4]	5:0	See description of '1220h'.	
11h (1222h)	**REG1222**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSPAN[7:0]	7:0	DDR clock spread spectrum period. DDR_SPREAD (DDR spread period) = (4* LOOP_DIV1*LOOP_DIV2*DDFSPAN)/ (DDR_FREQ*IN_DIV1*IN_DIV2).	
11h (1223h)	**REG1223**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ENFRUNZ	4	VCO Free Run Disable.	
	DDFT[1:0]	3:2	DDR clock generator test mode. 00: Normal operation (default). 01: Synthesizer truncate to integer divide. 10: Synthesizer bypass (equivalent to divide = 1). 11: Reserved.	
	DDFSPAN[9:8]	1:0	See description of '1222h'.	
12h (1224h)	**REG1224**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDFSTEP[7:0]	7:0	DDR Clock Spread Spectrum Step. DDR_SWB (DDR spread bandwidth) = DDR_FREQ* (2*DDFSPAN*DDFSTEP) / (DDFSET*1024).	
12h	**REG1225**	**7:0**	**Default : 0x40**	**Access : R/W**

MIU0 Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(1225h)	DDRPLL_LOOP_DIV_FIRST[1:0]	7:6	Loop divider1 ratio control. 00: Divide by 1. 01: Divide by 2 (default). 10: Divide by 4. 11: Divide by 8.	
	DDRPLL_INPUT_DIV_FIRST[1:0]	5:4	Input divider1 ratio control. 00: Divide by 1 (default). 01: Divide by 2. 10: Divide by 4. 11: Divide by 8.	
	DDRPLL_RESET	3	DDR PLL Reset.	
	DDRPLL_PORST	2	DDR PLL Power On Reset.	
	DDRPLL_PD	1	DDR PLL Power Down.	
	DDR_SSC_EN	0	DDR PLL Spread Spectrum Control Enable.	
13h (1226h)	**REG1226**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRPLL_INPUT_DIV_SECOND[7:0]	7:0	Input divider2 ratio (1/N), default: 0. 0: N=1. Other: N=IN_DIV[7:0].	
13h (1227h)	**REG1227**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRPLL_LOOP_DIV_SECOND[7:0]	7:0	Loop divider2 ratio (1/N), default: 0. 0: N=1. Other: N=IN_DIV[7:0].	
14h (1228h)	**REG1228**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[7:0]	7:0	DDR clock generator analog test modes and reserved bits.	
14h (1229h)	**REG1229**	**7:0**	**Default : 0x00**	**Access : R/W**
	DDRAT[15:8]	7:0	See description of '1228h'.	
18h (1230h)	**REG1230**	**7:0**	**Default : 0x00**	**Access : R/W**
	DQSPH1[3:0]	7:4	DDR DQS1 input phase control. 0.5T/12 steps.	
	DQSPH0[3:0]	3:0	DDR DQS0 input phase control. 0.5T/12 steps.	
19h (1232h)	**REG1232**	**7:0**	**Default : 0x00**	**Access : R/W**
	DQSPH1_2ND[3:0]	7:4	DDR DQS5 input phase control. 0.5T/12 steps.	
	DQSPH0_2ND[3:0]	3:0	DDR DQS4 input phase control.	

MIU0 Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
			0.5T/12 steps.	
1Ah (1235h)	**REG1235**	**7:0**	**Default : 0x00**	**Access : R/W**
	DQS_OEN_MASK[7:0]	7:0	DQS output enable mask.	
1Bh (1236h)	**REG1236**	**7:0**	**Default : 0x60**	**Access : R/W**
	CLK_DRV[2:0]	7:5	DDR CLK IO driving control.	
	DDR_CLK_SWITCH[1:0]	4:3	Source clock select. 00: DDR_CLK. 01: DDR_CLK_INV. 10: DDR_CLK_DLY. 11: DDR_CLK_DLY_INV.	
	CLKPH[2:0]	2:0	DDR output clock phase control. 1T/8 steps.	
1Bh (1237h)	**REG1237**	**7:0**	**Default : 0x00**	**Access : R/W**
	MD_DRV[1:0]	7:6	DDR Data IO driving control.	
	ADR_DRV[1:0]	5:4	DDR command and address IO driving control.	
	DM_DRV[1:0]	3:2	DDR Data Mask IO driving control.	
	DQS_DRV[1:0]	1:0	DDR DQS IO driving control.	
1Ch (1238h)	**REG1238**	**7:0**	**Default : 0x00**	**Access : R/W**
	FB_CLK_SEL	7	SDR read data clock select. 0: FBCLK. 1: PLL 2nd PH.	
	CLKPH1[2:0]	6:4	PLL 2nd output clock phase control. 1T/8 steps.	
	-	3:2	Reserved.	
	FORCE_D2A_FIFO_EN	1	Force D2A_FIFO_EN value.	
	FORCE_CKE_IN	0	Force CKE value.	
1Ch (1239h)	**REG1239**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LADR_DRV[5:0]	5:0	Addr[2:0] pad driving strength.	
1Dh (123Ah)	**REG123A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DDR266[4:0]	4:0	TR[2:0], LEG[1:0].	
1Dh (123Bh)	**REG123B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

MIU0 Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DDR_LEG2[6:0]	6:0	LEG2 for each byte.	
1Fh (123Eh)	**REG123E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DS_RESTEN	2	DQS test mode enable.	
	DQS_IN_I_SEL	1	Select DQS_I as DQS DLL input, for test mode.	
	DQS_LOWPOWER	0	DQS DLL low power mode (without clock in when writing).	
1Fh (123Fh)	**REG123F**	**7:0**	**Default : 0x00**	**Access : RO**
	DDRPLL_LOCK	7	DDR PLL lock status (read only).	
	-	6:0	Reserved.	
20h (1240h)	**REG1240**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RQ0_GROUP_DEADLINE_EN	5	Group0 deadline enable.	
	RQ0_TIMEOUT_EN	4	Group0 timeout enable.	
	RQ0_GROUP_LIMIT_EN	3	Limit group0 request number enable.	
	RQ0_MEMBER_LIMIT_EN	2	Limit group0 client request number enable.	
	RQ0_SET_PRIORITY	1	Set group0 fixed priority.	
	RQ0_ROUND_ROBIN	0	Turn on group0 round robin.	
20h (1241h)	**REG1241**	**7:0**	**Default : 0x00**	**Access : R/W**
	NO_RQ_CTRL_EN	7	No request flow control enable.	
	-	6:3	Reserved.	
	RQ0_CNT2_CTRL_EN	2	Flow control counter 2 enable.	
	RQ0_CNT1_CTRL_EN	1	Flow control counter 1 enable.	
	RQ0_CNT0_CTRL_EN	0	Flow control counter 0 enable.	
21h (1242h)	**REG1242**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_MEMBER_MAX[7:0]	7:0	Limit group0 client request number, unit is 4.	
21h (1243h)	**REG1243**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_GROUP_MAX[7:0]	7:0	Limit group0 client request number, unit is 32.	
22h (1244h)	**REG1244**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_TIMEOUT[7:0]	7:0	Limit group0 timeout number.	
22h (1245h)	**REG1245**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_TIMEOUT[15:8]	7:0	See description of '1244h'.	
23h	**REG1246**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU0 Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
(1246h)	RQ0_MASK[7:0]	7:0	Limit group0 request mask.	
23h (1247h)	**REG1247**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_MASK[15:8]	7:0	See description of '1246h'.	
24h (1248h)	**REG1248**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_HPMASK[7:0]	7:0	Limit group0 high priority request mask.	
24h (1249h)	**REG1249**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_HPMASK[15:8]	7:0	See description of '1248h'.	
25h (124Ah)	**REG124A**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ01_PRIORITY[3:0]	7:4	Limit group0 client 1 fixed priority number.	
	RQ00_PRIORITY[3:0]	3:0	Limit group0 client 0 fixed priority number.	
25h (124Bh)	**REG124B**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ03_PRIORITY[3:0]	7:4	Limit group0 client 3 fixed priority number.	
	RQ02_PRIORITY[3:0]	3:0	Limit group0 client 2 fixed priority number.	
26h (124Ch)	**REG124C**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ05_PRIORITY[3:0]	7:4	Limit group0 client 5 fixed priority number.	
	RQ04_PRIORITY[3:0]	3:0	Limit group0 client 4 fixed priority number.	
26h (124Dh)	**REG124D**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ07_PRIORITY[3:0]	7:4	Limit group0 client 7 fixed priority number.	
	RQ06_PRIORITY[3:0]	3:0	Limit group0 client 6 fixed priority number.	
27h (124Eh)	**REG124E**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ09_PRIORITY[3:0]	7:4	Limit group0 client 9 fixed priority number.	
	RQ08_PRIORITY[3:0]	3:0	Limit group0 client 8 fixed priority number.	
27h (124Fh)	**REG124F**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ0B_PRIORITY[3:0]	7:4	Limit group0 client b fixed priority number.	
	RQ0A_PRIORITY[3:0]	3:0	Limit group0 client a fixed priority number.	
28h (1250h)	**REG1250**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ0D_PRIORITY[3:0]	7:4	Limit group0 client d fixed priority number.	
	RQ0C_PRIORITY[3:0]	3:0	Limit group0 client c fixed priority number.	
28h (1251h)	**REG1251**	**7:0**	**Default : 0xFE**	**Access : R/W**
	RQ0F_PRIORITY[3:0]	7:4	Limit group0 client f fixed priority number.	
	RQ0E_PRIORITY[3:0]	3:0	Limit group0 client e fixed priority number.	
29h (1253h)	**REG1253**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_GROUP_DEADLINE[7:0]	7:0	Group0 deadline, unit is 64.	

MIU0 Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
2Ah (1254h)	**REG1254**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT0_ID1[3:0]	7:4	ID1 for group0 flow control counter0.	
	RQ0_CNT0_ID0[3:0]	3:0	ID0 for group0 flow control counter0.	
2Ah (1255h)	**REG1255**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT0_PERIOD[7:0]	7:0	Group0 flow control counter0.	
2Bh (1256h)	**REG1256**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT1_ID1[3:0]	7:4	ID1 for group0 flow control counter1.	
	RQ0_CNT1_ID0[3:0]	3:0	ID0 for group0 flow control counter1.	
2Bh (1257h)	**REG1257**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT1_PERIOD[7:0]	7:0	Group0 flow control counter1.	
2Ch (1258h)	**REG1258**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT2_ID1[3:0]	7:4	ID1 for group0 flow control counter2.	
	RQ0_CNT2_ID0[3:0]	3:0	ID0 for group0 flow control counter2.	
2Ch (1259h)	**REG1259**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ0_CNT2_PERIOD[7:0]	7:0	Group0 flow control counter2.	
30h (1260h)	**REG1260**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	RQ1_GROUP_DEADLINE_EN	5	Group1 deadline enable.	
	RQ1_TIMEOUT_EN	4	Group1 timeout enable.	
	RQ1_GROUP_LIMIT_EN	3	Limit group1 request number enable.	
	RQ1_MEMBER_LIMIT_EN	2	Limit group1 client request number enable.	
	RQ1_SET_PRIORITY	1	Set group1 fixed priority.	
	RQ1_ROUND_ROBIN	0	Turn on group1 round robin.	
30h (1261h)	**REG1261**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	RQ1_CNT2_CTRL_EN	2	Flow control counter 2 enable.	
	RQ1_CNT1_CTRL_EN	1	Flow control counter 1 enable.	
	RQ1_CNT0_CTRL_EN	0	Flow control counter 0 enable.	
31h (1262h)	**REG1262**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MEMBER_MAX[7:0]	7:0	Limit group1 client request number, unit is 4.	
31h (1263h)	**REG1263**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_GROUP_MAX[7:0]	7:0	Limit group1 client request number, unit is 32.	
32h	**REG1264**	**7:0**	**Default : 0x00**	**Access : R/W**

MIU0 Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1264h)	RQ1_TIMEOUT[7:0]	7:0	Limit group1 timeout number.	
32h (1265h)	**REG1265**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_TIMEOUT[15:8]	7:0	See description of '1264h'.	
33h (1266h)	**REG1266**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MASK[7:0]	7:0	Limit group1 request mask.	
33h (1267h)	**REG1267**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_MASK[15:8]	7:0	See description of '1266h'.	
34h (1268h)	**REG1268**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_HPMASK[7:0]	7:0	Limit group1 high priority request mask.	
34h (1269h)	**REG1269**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_HPMASK[15:8]	7:0	See description of '1268h'.	
35h (126Ah)	**REG126A**	**7:0**	**Default : 0x10**	**Access : R/W**
	RQ11_PRIORITY[3:0]	7:4	Limit group1 client 1 fixed priority number.	
	RQ10_PRIORITY[3:0]	3:0	Limit group1 client 0 fixed priority number.	
35h (126Bh)	**REG126B**	**7:0**	**Default : 0x32**	**Access : R/W**
	RQ13_PRIORITY[3:0]	7:4	Limit group1 client 3 fixed priority number.	
	RQ12_PRIORITY[3:0]	3:0	Limit group1 client 2 fixed priority number.	
36h (126Ch)	**REG126C**	**7:0**	**Default : 0x54**	**Access : R/W**
	RQ15_PRIORITY[3:0]	7:4	Limit group1 client 5 fixed priority number.	
	RQ14_PRIORITY[3:0]	3:0	Limit group1 client 4 fixed priority number.	
36h (126Dh)	**REG126D**	**7:0**	**Default : 0x76**	**Access : R/W**
	RQ17_PRIORITY[3:0]	7:4	Limit group1 client 7 fixed priority number.	
	RQ16_PRIORITY[3:0]	3:0	Limit group1 client 6 fixed priority number.	
37h (126Eh)	**REG126E**	**7:0**	**Default : 0x98**	**Access : R/W**
	RQ19_PRIORITY[3:0]	7:4	Limit group1 client 9 fixed priority number.	
	RQ18_PRIORITY[3:0]	3:0	Limit group1 client 8 fixed priority number.	
37h (126Fh)	**REG126F**	**7:0**	**Default : 0xBA**	**Access : R/W**
	RQ1B_PRIORITY[3:0]	7:4	Limit group1 client b fixed priority number.	
	RQ1A_PRIORITY[3:0]	3:0	Limit group1 client a fixed priority number.	
38h (1270h)	**REG1270**	**7:0**	**Default : 0xDC**	**Access : R/W**
	RQ1D_PRIORITY[3:0]	7:4	Limit group1 client d fixed priority number.	
	RQ1C_PRIORITY[3:0]	3:0	Limit group1 client c fixed priority number.	
38h	**REG1271**	**7:0**	**Default : 0xFE**	**Access : R/W**

MIU0 Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1271h)	RQ1F_PRIORITY[3:0]	7:4	Limit group1 client f fixed priority number.	
	RQ1E_PRIORITY[3:0]	3:0	Limit group1 client e fixed priority number.	
39h (1273h)	**REG1273**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_GROUP_DEADLINE[7:0]	7:0	Group1 deadline, unit is 64.	
3Ah (1274h)	**REG1274**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT0_ID1[3:0]	7:4	ID1 for group1 flow control counter0.	
	RQ1_CNT0_ID0[3:0]	3:0	ID0 for group1 flow control counter0.	
3Ah (1275h)	**REG1275**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT0_PERIOD[7:0]	7:0	Group1 flow control counter0.	
3Bh (1276h)	**REG1276**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT1_ID1[3:0]	7:4	ID1 for group1 flow control counter1.	
	RQ1_CNT1_ID0[3:0]	3:0	ID0 for group1 flow control counter1.	
3Bh (1277h)	**REG1277**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT1_PERIOD[7:0]	7:0	Group1 flow control counter1.	
3Ch (1278h)	**REG1278**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT2_ID1[3:0]	7:4	ID1 for group1 flow control counter2.	
	RQ1_CNT2_ID0[3:0]	3:0	ID0 for group1 flow control counter2.	
3Ch (1279h)	**REG1279**	**7:0**	**Default : 0x00**	**Access : R/W**
	RQ1_CNT2_PERIOD[7:0]	7:0	Group1 flow control counter2.	
60h (12C0h)	**REG12C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PROTECT0_EN	0	Protect 0 enable.	
60h (12C1h)	**REG12C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT0_ID[5:0]	5:0	Protect 0 ID.	
61h (12C2h)	**REG12C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_START[7:0]	7:0	Protect 0 start address.	
61h (12C3h)	**REG12C3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_START[15:8]	7:0	See description of '12C2h'.	
62h (12C4h)	**REG12C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_END[7:0]	7:0	Protect 0 end address.	
62h (12C5h)	**REG12C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT0_END[15:8]	7:0	See description of '12C4h'.	

MIU0 Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
63h (12C6h)	**REG12C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PROTECT1_EN	0	Protect 1 enable.	
63h (12C7h)	**REG12C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT1_ID[5:0]	5:0	Protect 1 ID.	
64h (12C8h)	**REG12C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_START[7:0]	7:0	Protect 1 start address.	
64h (12C9h)	**REG12C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_START[15:8]	7:0	See description of '12C8h'.	
65h (12CAh)	**REG12CA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_END[7:0]	7:0	Protect 1 end address.	
65h (12CBh)	**REG12CB**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT1_END[15:8]	7:0	See description of '12CAh'.	
66h (12CCh)	**REG12CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PROTECT2_EN	0	Protect 2 enable.	
66h (12CDh)	**REG12CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PROTECT2_ID[5:0]	5:0	Protect 2 ID.	
67h (12CEh)	**REG12CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_START[7:0]	7:0	Protect 2 start address.	
67h (12CFh)	**REG12CF**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_START[15:8]	7:0	See description of '12CEh'.	
68h (12D0h)	**REG12D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_END[7:0]	7:0	Protect 2 end address.	
68h (12D1h)	**REG12D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT2_END[15:8]	7:0	See description of '12D0h'.	
69h (12D2h)	**REG12D2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PROTECT3_EN	0	Protect 3 enable.	
69h (12D3h)	**REG12D3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

MIU0 Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PROTECT3_ID[5:0]	5:0	Protect 3 ID.	
6Ah (12D4h)	**REG12D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_START[7:0]	7:0	Protect 3 start address.	
6Ah (12D5h)	**REG12D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_START[15:8]	7:0	See description of '12D4h'.	
6Bh (12D6h)	**REG12D6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_END[7:0]	7:0	Protect 3 end address.	
6Bh (12D7h)	**REG12D7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PROTECT3_END[15:8]	7:0	See description of '12D6h'.	
6Fh (12DEh)	**REG12DE**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	HIT_PROTECT_FLAG	7	Flag to show the protected area has been hit.	
	-	6:1	Reserved.	
	PROTECT_LOG_CLR	0	Clear hit-protect log.	
6Fh (12DFh)	**REG12DF**	**7:0**	**Default : 0x00**	**Access : RO**
	HIT_PROTECT_NO[1:0]	7:6	Number of the hit area.	
	HIT_PROTECT_ID[5:0]	5:0	ID of the rule-breaking client.	
70h (12E0h)	**REG12E0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FORCE_IN	6	Force read data to TEST_DATA.	
	FORCE_OUT	5	Force write data to TEST_DATA.	
	TEST_LOOP	4	Loop mode.	
	INV_DATA	3	Inverse test data.	
	TEST_MODE[1:0]	2:1	MIU self test mode. 00: Address mode. 01: From TEST_DATA. 10: Shift data.	
	TEST_EN	0	MIU self test enable.	
70h (12E1h)	**REG12E1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TEST_FINISH	7	Test finish indicator.	
	TEST_FAIL	6	Test fail indicator.	
	TEST_FLAG	5	Test fail indicator.	
	-	4	Reserved.	
	TEST_BYTE[1:0]	3:2	Read back data byte switch.	

MIU0 Register (Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	WRITE_ONLY	1	Only issue write command.	
	READ_ONLY	0	Only issue read command.	
71h (12E2h)	**REG12E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[7:0]	7:0	Test base address.	
71h (12E3h)	**REG12E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_BASE[15:8]	7:0	See description of '12E2h'.	
72h (12E4h)	**REG12E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_L[7:0]	7:0	Test length.	
72h (12E5h)	**REG12E5**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_L[15:8]	7:0	See description of '12E4h'.	
73h (12E6h)	**REG12E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_LENGTH_H[23:16]	7:0	Test length.	
73h (12E7h)	**REG12E7**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_MASK[7:0]	7:0	Test data mask.	
74h (12E8h)	**REG12E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[7:0]	7:0	Test data.	
74h (12E9h)	**REG12E9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_DATA[15:8]	7:0	See description of '12E8h'.	
75h (12EAh)	**REG12EA**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_STATUS[7:0]	7:0	Test status.	
75h (12EBh)	**REG12EB**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_STATUS[15:8]	7:0	See description of '12EAh'.	
7Fh (12FEh)	**REG12FE**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:5	Reserved.	
	SYNC_OUT_THRESHOLD[4:0]	4:0	Sync out FIFO full threshold.	

VD_MCU Register (Bank = 13)

VD_MCU Register (Bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h ~ 05h (1300h ~ 130Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
06h (130Ch)	**REG130C**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	HK2VD_INT	1	HK MCU interrupt to VDMCU.	
	VD_MCU_RESET	0	VD MCU reset.	
06h ~ 27h (130Dh ~ 134Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
28h (1350h)	**REG1350**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	VD_SPI_EN	2	Code using SPI.	
	VD_DRAM_EN	1	Code using DRAM.	
	VD_SRAM_EN	0	Code using SRAM.	
29h (1352h)	**REG1352**	**7:0**	**Default : 0x00**	**Access : R/W**
	VD_ROM_BANK[7:0]	7:0	Code ROM bank.	

RF Register (Bank = 14)

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1400h)	**REG1400**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7	Reserved.	
	TAGC_PWR	6	Tuner AGC power control. 1: Power on. 0: Power off.	
	-	5	Reserved.	
	VIF_CBC_PWRS	4	Power on the sound path of central bias circuit. 1: Power on.(VIF_CBC_PWR must =1) 0:power off.	
	VIF_CBC_PWR	3	Power on central bias circuit. 1: Power on. 0: Power off.	
	VIF_PLL_PWR	2	Power on VIF PLL. 1: Power on. 0: Power off.	
	VIF_VCOREG_PWR	1	VCO regulator power on. 1: Power on. 0: Power off.	
	VIF_VCO_PWR	0	VCO power on, 1:power on. 0: Power off.	
00h (1401h)	**REG1401**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VIF_PGPWRV	7	PGA1_V power on. 1: Power on. 0: Power off.	
	VIF_MXPWRV	6	MX_V power on. 1: Power on. 0: Power off.	
	VIF_PWR_LPFV	5	LPF_V power on. 1: Power on. 0: Power off.	
	VIF_PWR_PGA2V	4	PGA2_V power on. 1: Power on. 0: Power off.	
	VIF_PGPWRS	3	PGA1_S power on. 1: Power on. 0: Power off.	

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VIF_MXPWRS	2	MX_S power on. 1: Power on. 0: Power off.	
	VIF_PWR_LPFS	1	LPF_S power on. 1: Power on. 0: Power off.	
	VIF_PWR_PGA2S	0	PGA2_S power on. 1: Power on. 0: Power off.	
01h (1402h)	**REG1402**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	VIF_PLL_RSTZ	4	Reset the feedback divider. 0: Reset. 1: Normal opearation.	
	-	3:2	Reserved.	
	VIF_PLL_R[1:0]	1:0	Regulator input source and output voltage setting. See Table 1.	
01h (1403h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (1404h)	**REG1404**	**7:0**	**Default : 0x24**	**Access : R/W**
	TAGC_ODMODE	7	TAGC DAC output open-drain mode. 1: Open-drain voltage output. 0: 1mA current sink output.	
	-	6	Reserved.	
	VIF_PLL_MSEL	5	Bypass feedfack divider re-sync function. 1: Resync. 0: Bypass resync.	
	-	4	Reserved.	
	VIF_PLL_M[3:0]	3:0	PLL post divider (Divion ratio = 2~15).	
02h (1405h)	**REG1405**	**7:0**	**Default : 0x59**	**Access : R/W**
	VIF_PLL_RSEL	7	Bypass reference divider. 1: Bypass(divide-by-1). 0: Normal operation(divide-by-2 or 3).	
	VIF_PLL_RDIV	6	PLL reference divider. 1: Fxtal/3. 0: Fxtal/2.	

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VIF_PLL_N[5:0]	5:0	PLL feedback divider (Divion ratio = 2~63).default:divide-by-25.	
03h (1406h)	**REG1406**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:4	Reserved.	
	VIF_PLL_LPEX	3	Charge pump current power control. 1: Power off. 0: Power on.	
	-	2:0	Reserved.	
03h (1407h)	**REG1407**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	VIF_PLL_SBIAS	4	VCO self bias enable. 1: Enable. 0: Disable.	
	VIF_VCO_REF	3	VCO bandgap reference voltage selection. 1: 1.20V. 0: 1.10V.	
	VIF_VCOREG_SBIAS	2	VCO self bias enable. 1: Enable. 0: Disable.	
	-	1:0	Reserved.	
04h (1408h)	**REG1408**	**7:0**	**Default : 0x44**	**Access : R/W**
	VIF_CAL_START	7	VCO band calibration start. 1: Enable. 0: No operation. (self-clear).	
	VIF_VCO_LK	6	Kvco control bit 1. 1: Kvco~170MHz/V. 0: Kvco~120MHz/V.	
	-	5	Reserved.	
	VIF_VCO_LP	4	VCO low power mode. 1: 4m. 0: 6mA.	
	-	3	Reserved.	
	VIF_VCO_BANK_W[2:0]	2:0	Override bits for VCO bank selection. See Table 4.	
04h ~ 05h	**-**	**7:0**	**Default : -**	**Access : -**

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1409h ~ 140Ah)	-	-	Reserved.	
05h (140Bh)	**REG140B**	**7:0**	**Default : 0xAA**	**Access : R/W**
	VIF_CALIB_TUNE	7	LPF calibration enable (power on). 1: Enable. 0: Disable.	
	-	6	Reserved.	
	VIF_RN_TUNE	5	Reset for LPF tuning circuit. 1: Normal operation. 0: Reset (restart calibration after reset finished).	
	-	4:0	Reserved.	
06h ~ 07h (140Ch ~ 140Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
08h (1410h)	**REG1410**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAGC_TAFC_NRZDATA	7	TAGC/TAFC DAC NRZ input data selection. 1: NRZ input data. 0: RZ input data.	
		6:0	Reserved.	
08h ~ 09h (1411h ~ 1413h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Bh (1416h)	**REG1416**	**7:0**	**Default : 0x90**	**Access : R/W**
	-	7:5	Reserved.	
	TAGC_POLARITY	4	Tuner AGC polarity control. 1: Positive logic. 0: Negative logic.	
	-	3:0	Reserved.	
0Bh (1417h)	**REG1417**	**7:0**	**Default : 0xD0**	**Access : R/W**
	TAGC_DITHER_EN	7	Dither signal enable. 1: Enable. 0: Disable.	
	TAGC_SEL_SECORDER	6	Select 2nd order delta-sigma modulator. 1: 2nd order. 0: 1st order.	

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TAGC_DITHER_SHIFT[2:0]	5:3	Dither signal gain setting. 0~7 -> 2^0~2^-7.	
	-	2:0	Reserved.	
0Ch (1419h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Dh (141Ah)	**REG141A**	**7:0**	**Default : 0x00**	**Access : RO**
	VCOCAL_FAIL	7	VCO bank calibration flag. 1: Fail. 0: Pass.	
	VCTRL_OVER	6	1: VCTRL larger than 2V. 0: VCTRL less than 2V.	
	VCTRL_UNDER	5	1: VCTRL less than 1V. 0: VCTRL larger than 1V.	
	LOCK	4	PLL LOCK detection, 1:LOCKed. 0: UnLOCKed.	
	VIF_PLL_CPINIT	3	Charge pump output open and tied to 1.5V. 1: Charge pump output tied to 1.5V. 0: Normal operation.	
	VIF_VCO_BANK[2:0]	2:0	VCO bank selection. See Table 4.	
0Dh (141Bh)	**REG141B**	**7:0**	**Default : 0x00**	**Access : RO**
	VIF_PGA1GAINV[3:0]	7:4	DBB PGA1_V gain setting low byte. See Table 5.	
	VIF_PGA1GAINS[3:0]	3:0	DBB PGA1_S gain setting low byte. See Table 5.	
0Eh (141Ch)	**REG141C**	**7:0**	**Default : 0x00**	**Access : RO**
	VIF_GAIN_PGA2V[3:0]	7:4	DBB PGA2_V gain setting high byte. See Table 6.	
	VIF_GAIN_PGA2S[3:0]	3:0	DBB PGA2_S gain setting low byte. See Table 6.	
0Eh (141Dh)	**REG141D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	VIF_CAL_FINISH	6	VCO Calibration Finish.	
	VIF_STOPCAL_TUNE	5	LPF calibration finished flag. 1: Finished (disbale LPF tuning circuit clock). 0: Under LPF calibrating.	

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VIF_FCODE_OUT[4:0]	4:0	LPF cap bank calibration output code.	
0Fh (141Eh)	**REG141E**	**7:0**	**Default : 0x00**	**Access : RO**
	VIF_CAL_GAP[7:0]	7:0	VIF VCO Calibration gap.	
10h (1420h)	**REG1420**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	VSYNC_VD_POLARITY	1	It respects to the vsync polarity from VD; 0=low active; 1=high active.	
	VSYNC_VD_MASK	0	1=mask vsync from VD.	
10h ~ 13h (1421h ~ 1426h)	**-**	**7:0**	**Default : -**	**Access : -**
	-		Reserved.	
14h (1428h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h (1440h)	**REG1440**	**7:0**	**Default : 0x0B**	**Access : R/W**
	-	7:5	Reserved.	
	CLAMPGAIN_STATUS_FREEZE	4	1=freeze clampgain status.	
	CLAMPGAIN_SEL	3	1=clamp select porch 0=clamp select sync bottom.	
	CLAMPGAIN_EN	2	1=clampgain enable.	
	CLAMPGAIN_BYPASS	1	1=clampgain bypass.	
	CLAMPGAIN_RSTZ	0	0=clampgain reset.	
21h (1442h)	**REG1442**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLAMPGAIN_SYNCBOTT_REF[7:0]	7:0	Porch or syncbottom reference level.	
21h (1443h)	**REG1443**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLAMPGAIN_SYNCHEIGHT_REF[7:0]	7:0	Syncheight reference level.	
22h (1444h)	**REG1444**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CLAMPGAIN_KG[2:0]	6:4	Gain loop filter parameter 1~7->2^-3~2^-9.	
	-	3	Reserved.	
	CLAMPGAIN_KC[2:0]	2:0	Clamp loop filter parameter 1~7->2^-3~2^-9.	
22h (1445h)	**REG1445**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CLAMPGAIN_GAIN_OREN	1	1=gain override enable.	
	CLAMPGAIN_CLAMP_OREN	0	1=clamp override enable.	

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
23h (1446h)	**REG1446**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLAMPGAIN_CLAMP_OVERWRITE[7:0]	7:0	Clamp override value.	
23h (1447h)	**REG1447**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CLAMPGAIN_CLAMP_OVERWRITE[10:8]	2:0	See description of '1446h'.	
24h (1448h)	**REG1448**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLAMPGAIN_GAIN_OVERWRITE[7:0]	7:0	Gain override value.	
24h (1449h)	**REG1449**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CLAMPGAIN_GAIN_OVERWRITE[10:8]	2:0	See description of '1448h'.	
25h (144Ah)	**REG144A**	**7:0**	**Default : 0x80**	**Access : R/W**
	CLAMPGAIN_CLAMP_MIN[7:0]	7:0	Clamp min.	
25h (144Bh)	**REG144B**	**7:0**	**Default : 0x7F**	**Access : R/W**
	CLAMPGAIN_CLAMP_MAX[7:0]	7:0	Clamp max.	
26h (144Ch)	**REG144C**	**7:0**	**Default : 0x40**	**Access : R/W**
	CLAMPGAIN_GAIN_MIN[7:0]	7:0	Gain min.	
26h (144Dh)	**REG144D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CLAMPGAIN_GAIN_MAX[7:0]	7:0	Gain max.	
27h (144Eh)	**REG144E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CLAMPGAIN_SYNCBOTTOM_OFFSET[6:0]	6:0	Sync bottom offset.	
27h (144Fh)	**REG144F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CLAMPGAIN_GAIN_RATIO[2:0]	2:0	Update ratio.	
28h (1450h)	**REG1450**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLAMPGAIN_SYNCBOTTOM_CNT[7:0]	7:0	Sync bottom counter max.	
28h (1451h)	**REG1451**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CLAMPGAIN_SYNCBOTTOM_CNT[11:8]	3:0	See description of '1450h'.	
29h (1452h)	**REG1452**	**7:0**	**Default : 0xF8**	**Access : R/W**
	CLAMPGAIN_PORCH_CNT[7:0]	7:0	Porch counter max.	
29h (1453h)	**REG1453**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CLAMPGAIN_PORCH_CNT[8]	0	See description of '1452h'.	
2Ah (1454h)	**REG1454**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_PEAK_MEAN[7:0]	7:0	Peak mean.	
2Ah (1455h)	**REG1455**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_PEAK_MEAN[15:8]	7:0	See description of '1454h'.	
2Bh (1456h)	**REG1456**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_SYNCBOTTOM_MEAN[7:0]	7:0	Sync bottom mean.	
2Bh (1457h)	**REG1457**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_SYNCBOTTOM_MEAN[15:8]	7:0	See description of '1456h'.	
2Ch (1458h)	**REG1458**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_PORCH_MEAN[7:0]	7:0	Porch mean.	
2Ch (1459h)	**REG1459**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_PORCH_MEAN[15:8]	7:0	See description of '1458h'.	
2Dh (145Ah)	**REG145A**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_CLAMP[7:0]	7:0	Clamp.	
2Dh (145Bh)	**REG145B**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_CLAMP[15:8]	7:0	See description of '145Ah'.	
2Eh (145Ch)	**REG145C**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_GAIN[7:0]	7:0	Gain.	
2Eh (145Dh)	**REG145D**	**7:0**	**Default : 0x00**	**Access : RO**
	CLAMPGAIN_GAIN[15:8]	7:0	See description of '145Ch'.	
30h (1460h)	**REG1460**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	AUDIO_FIFO_BYPASS	1	1=audio FIFO bypass.	
	AUDIO_FIFO_RSTZ	0	Audio input front end FIFO reset.	
30h (1461h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
50h (14A0h)	**REG14A0**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	PDN_VIFADC	1	1=power down vif adc.	
	VIFADC_ENABLE_VD	0	1=enable the vif video part.	
51h (14A2h)	**REG14A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

RF Register (Bank = 14)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VIFADC_GAIN[1:0]	1:0	Gain of vif adc.	
51h (14A3h)	**REG14A3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	VIFADC_OFFSET[4:0]	4:0	Offset of vif adc.	
7Ah (14F4h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

DBB1 Register (Bank = 15)

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1500h)	**REG1500**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	ADAGC_SOFT_RSTZ	6	AAGC software reset (low active).	
	AAGC_SOFT_RSTZ	5	AAGC software reset (low active).	
	VDAGC2_SOFT_RSTZ	4	VDAGC2 software reset (low active).	
	VDAGC1_SOFT_RSTZ	3	VDAGC1 software reset (low active).	
	VAGC_SOFT_RSTZ	2	VAGC software reset (low active).	
	FILTER_SOFT_RSTZ	1	Filter software reset (low active).	
	AFC_SOFT_RSTZ	0	AFC software reset (low active).	
01h (1502h)	**REG1502**	**7:0**	**Default : 0xC0**	**Access : R/W**
	BYPASS_CR_NOTCH2	7	0: Not bypass CR notch2. 1: Bypass CR notch2.	
	BYPASS_N_A4	6	0: Not bypass NOTCH filter A4. 1: Bypass NOTCH filter A4.	
	-	5:4	Reserved.	
	MODULATION_TYPE[3:0]	3:0	Bit[0]: filter modulation type bit[1]: VAGC modulation type bit[2]: VDAGC1 modulation type bit[3]: VDAGC2 modulation type 0: negative modulation 1: positive modulation.	
02h (1504h)	**REG1504**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	AUDIO_BYPASS[1:0]	1:0	00: Normal audio path mode. 01: Bypass audio mixer input data. 10: Bypass audio mixer output data. 11: Normal audio path mode.	
03h (1506h)	**REG1506**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	LOCK_LEAKY_FF_SEL	0	1=sel lock_leaky2_ff.	
04h (1508h)	**REG1508**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_CODIC_TH[7:0]	7:0	CR_CODIC_TH. <14,15>.	
04h (1509h)	**REG1509**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CR_CODIC_TH[13:8]	5:0	See description of '1508h'.	
05h (150Ah)	**REG150A**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	BYPASS_SOS32	5	1=bypass sos32 filter.	
	BYPASS_SOS31	4	1=bypass sos31 filter.	
	BYPASS_SOS22	3	1=bypass sos22 filter.	
	BYPASS_SOS21	2	1=bypass sos21 filter.	
	BYPASS_SOS12	1	1=bypass sos12 filter.	
	BYPASS_SOS11	0	1=bypass sos11 filter.	
05h (150Bh)	**REG150B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	BYPASS_NYQUIST_ACI	5	1=bypass nyquist_slope filter or nyquist ACI rejection filter.	
	-	4:0	Reserved.	
0Ah (1514h)	**REG1514**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CR_DL_A[3:0]	3:0	(user-added) audio delay. Delay = delay_a*8. {4}.	
0Ah (1515h)	**REG1515**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CR_F_OFFSET[5:0]	5:0	(user-added) frequency offset. (6,0).	
0Bh (1516h)	**REG1516**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CR_PD_ERR_MAX[7:0]	7:0	Maximum phase error (absolute value). <14,15>. (double load).	
0Bh (1517h)	**REG1517**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	CR_PD_ERR_MAX[13:8]	5:0	See description of '1516h'.	
0Ch (1518h)	**REG1518**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_KL[7:0]	7:0	Scaling factor for hard limiter. <14,15>. (double load).	
0Ch	**REG1519**	**7:0**	**Default : 0x00**	**Access : R/W**

DBB1 Register (Bank = 15)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(1519h)	-	7:6	Reserved.
	CR_KL[13:8]	5:0	See description of '1518h'.
0Dh (151Ah)	**REG151A**	**7:0**	**Default : 0x00** **Access : R/W**
	CR_NOTCH_A1[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).
0Dh (151Bh)	**REG151B**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	CR_NOTCH_A1[11:8]	3:0	See description of '151Ah'.
0Eh (151Ch)	**REG151C**	**7:0**	**Default : 0x00** **Access : R/W**
	CR_NOTCH_A2[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).
0Eh (151Dh)	**REG151D**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	CR_NOTCH_A2[11:8]	3:0	See description of '151Ch'.
0Fh (151Eh)	**REG151E**	**7:0**	**Default : 0x00** **Access : R/W**
	CR_NOTCH_B1[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).
0Fh (151Fh)	**REG151F**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	CR_NOTCH_B1[11:8]	3:0	See description of '151Eh'.
10h (1520h)	**REG1520**	**7:0**	**Default : 0x7E** **Access : R/W**
	CR_PD_LINITER	7	Hard limiter. 0: No hard limier. 1: Hard limiter.
	CR_K_SEL	6	Loop parameter select. 0: Kp1, ki1, kf1, kp2, ki2, kf2. 1: Kp, ki, kf.
	-	5	Reserved.
	CR_LPF_SEL	4	LPF select. 0: LPF1. 1: LPF2.

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CR_INV	3	Output inversion. 0: Not invert output. 1: Invert output based on in-phase component.	
	CR_PD_X2	2	(cordic). 0: Lock 0 degree. 1: Lock 0 or 180 degree.	
	CR_PD_MODE	1	0: Imaginary party. 1: Cordic.	
	CR_ANCO_SEL	0	Audio nco select. 0: Nco_ff. 1: Nco_ff_a.	
11h (1522h)	**REG1522**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_KI_SW[3:0]	7:4	Loop filter integral coefficient. 0 -> 0. 1~11 -> 2^-12 ~ 2^-22. 12~15 -> 0.	
	CR_KP_SW[3:0]	3:0	Loop filter proportional coefficient. 0 -> 0. 1~11 -> 2^-2 ~ 2^-12. 12~15 -> 0.	
11h (1523h)	**REG1523**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CR_KF_SW[3:0]	3:0	Loop filter frequency coefficient. 0 -> 0. 1~11 -> 2^-8 ~ 2^-18. 12~15 -> 0.	
12h (1524h)	**REG1524**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_RATE[7:0]	7:0	Rate = Fc/(Fs/2) + f_offset. Fs: Sampling frequency. Fc: Carrier frequency. <21,22> (double load).	
12h (1525h)	**REG1525**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_RATE[15:8]	7:0	See description of '1524h'.	
13h (1526h)	**REG1526**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CR_RATE[20:16]	4:0	See description of '1524h'.	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (1528h)	**REG1528**	**7:0**	**Default : 0x43**	**Access : R/W**
	CR_KI1_HW[3:0]	7:4	Loop filter integral coefficient. 0 -> 0. 1~11 -> 2^-12 ~ 2^-22. 12~15 -> 0.	
	CR_KP1_HW[3:0]	3:0	Loop filter proportional coefficient. 0 -> 0. 1~11 -> 2^-2 ~ 2^-12. 12~15 -> 0.	
14h (1529h)	**REG1529**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	CR_KF1_HW[3:0]	3:0	Loop filter frequency coefficient. 0 -> 0. 1~11 -> 2^-8 ~ 2^-18. 12~15 -> 0.	
15h (152Ah)	**REG152A**	**7:0**	**Default : 0x64**	**Access : R/W**
	CR_KI2_HW[3:0]	7:4	Loop filter integral coefficient. 0 -> 0. 1~11 -> 2^-12 ~ 2^-22. 12~15 -> 0.	
	CR_KP2_HW[3:0]	3:0	Loop filter proportional coefficient. 0 -> 0. 1~11 -> 2^-2 ~ 2^-12. 12~15 -> 0.	
15h (152Bh)	**REG152B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CR_KF2_HW[3:0]	3:0	Loop filter frequency coefficient. 0 -> 0. 1~11 -> 2^-8 ~ 2^-18. 12~15 -> 0.	
16h (152Ch)	**REG152C**	**7:0**	**Default : 0x40**	**Access : R/W**
	CR_LOCK_TH[7:0]	7:0	Lock threshold. <10,10>. (double load).	
16h (152Dh)	**REG152D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CR_LOCK_TH[9:8]	1:0	See description of '152Ch'.	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
17h (152Eh)	**REG152E**	**7:0**	**Default : 0x60**	**Access : R/W**
	CR_FOE_SCAL_FACTOR[7:0]	7:0	Frequency offset estimation scaling factor. Foe_scale_factor = (Fs/2)/(F_step/4). Fs: Sampling frequency. F_step: Tuner frequency step, e.g. 62.5 KHz, 50 KHz. (12,-2). (double load)	
17h (152Fh)	**REG152F**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	CR_FOE_SCAL_FACTOR[11:8]	3:0	See description of '152Eh'.	
18h (1530h)	**REG1530**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_LOCK_NUM[7:0]	7:0	Lock number. <20,0>. (double load).	
18h (1531h)	**REG1531**	**7:0**	**Default : 0x80**	**Access : R/W**
	CR_LOCK_NUM[15:8]	7:0	See description of '1530h'.	
19h (1532h)	**REG1532**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CR_LOCK_NUM[19:16]	3:0	See description of '1530h'.	
1Ah (1534h)	**REG1534**	**7:0**	**Default : 0x40**	**Access : R/W**
	CR_UNLOCK_NUM[7:0]	7:0	Unlock number. <20,0>. (double load).	
1Ah (1535h)	**REG1535**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_UNLOCK_NUM[15:8]	7:0	See description of '1534h'.	
1Bh (1536h)	**REG1536**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CR_UNLOCK_NUM[19:16]	3:0	See description of '1534h'.	
1Ch (1538h)	**REG1538**	**7:0**	**Default : 0x00**	**Access : RO**
	CR_FOE[7:0]	7:0	Frequency offset estimation. (8,0).	
1Ch (1539h)	**REG1539**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CR_LOCK_STATUS	0	Lock status. 0: Unlock. 1: Lock.	
1Dh (153Ah)	**REG153A**	**7:0**	**Default : 0x00**	**Access : RO**
	CR_LOCK_LEAKY_FF_I[7:0]	7:0	(in-phase) lock leaky integrator flip-flop. (16,16).	
1Dh (153Bh)	**REG153B**	**7:0**	**Default : 0x00**	**Access : RO**
	CR_LOCK_LEAKY_FF_I[15:8]	7:0	See description of '153Ah'.	
1Eh (153Ch)	**REG153C**	**7:0**	**Default : 0x00**	**Access : RO**
	CR_LOCK_LEAKY_FF_Q[7:0]	7:0	(quadrature) lock leaky integrator flip-flop. (16,16).	
1Eh (153Dh)	**REG153D**	**7:0**	**Default : 0x00**	**Access : RO**
	CR_LOCK_LEAKY_FF_Q[15:8]	7:0	See description of '153Ch'.	
1Fh (153Eh)	**REG153E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_NOTCH2_A1[7:0]	7:0	Notch filter (denominator) coefficient. <12,22> (double load).	
1Fh (153Fh)	**REG153F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CR_NOTCH2_A1[11:8]	3:0	See description of '153Eh'.	
20h (1540h)	**REG1540**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_NOTCH2_A2[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).	
20h (1541h)	**REG1541**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CR_NOTCH2_A2[11:8]	3:0	See description of '1540h'.	
21h (1542h)	**REG1542**	**7:0**	**Default : 0x00**	**Access : R/W**
	CR_NOTCH2_B1[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).	
21h (1543h)	**REG1543**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CR_NOTCH2_B1[11:8]	3:0	See description of '1542h'.	
22h	**REG1544**	**7:0**	**Default : 0x00**	**Access : RO**

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1544h)	CR_LF_FF_RPT[7:0]	7:0	LF_FF report.	
22h (1545h)	**REG1545**	**7:0**	**Default : 0x00**	**Access : RO**
	CR_LF_FF_RPT[15:8]	7:0	See description of '1544h'.	
23h (1546h)	**REG1546**	**7:0**	**Default : 0x00**	**Access : RO**
	CR_LF_FF_RPT[23:16]	7:0	See description of '1544h'.	
23h (1547h)	**REG1547**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CR_LF_FF_RPT[28:24]	4:0	See description of '1544h'.	
24h ~ 27h (1548h ~ 154Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-		Reserved.	
40h (1580h)	**REG1580**	**7:0**	**Default : 0x10**	**Access : R/W**
	A_BP_OUT_X2	7	1: A_BPF output x2. 0: A_BPF output.	
	ACI_REJ_NTSC	6	1: NTSC. 0: PAL.	
	BYPASS_IMAGE_REJ1	5	0: Not bypass image rejection filter1. 1: Bypass image rejection filter1.	
	BYPASS_GDE	4	0: Not bypass gde. 1: Bypass gde.	
	BYPASS_N_A2	3	0: Not bypass NOTCH filter A2. 1: Bypass NOTCH filter A2.	
	BYPASS_N_A1	2	0: Not bypass NOTCH filter A1. 1: Bypass NOTCH filter A1.	
	BYPASS_DC	1	0: Not bypass DC_notch on video path. 1: Bypass DC_notch on video path.	
	-	0	Reserved.	
40h (1581h)	**REG1581**	**7:0**	**Default : 0x38**	**Access : R/W**
	-	7	Reserved.	
	BYPASS_IMAGE_REJ2	6	0: Not bypass image rejection filter2. 1: Bypass image rejection filter2.	
	BYPASS_N_A3	5	0: Not bypass NOTCH filter A3. 1: Bypass NOTCH filter A3.	
	VD_SIGNED_UNSIGNED	4	0: Signed. 1: Unsigned.	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AD_SIGNED_UNSIGNED	3	0: Signed. 1: Unsigned.	
	BYPASS_A_NOTCH	2	0: Not bypass A_notch. 1: Bypass A_notch.	
	BYPASS_1ST_A_BP	1	0: Not bypass 1st_A_BP. 1: Bypass 1st_A_BP.	
	BYPASS_A_DC	0	0: Not bypass A_DC_NOTCH on video path. 1: Bypass A_DC_NOTCH on video path.	
41h (1582h)	**REG1582**	**7:0**	**Default : 0x10**	**Access : R/W**
	DC_C[7:0]	7:0	Coefficient of DC_NOTCH on video path.	
41h (1583h)	**REG1583**	**7:0**	**Default : 0x10**	**Access : R/W**
	A_DC_C[7:0]	7:0	Coefficient of A_DC_NOTCH on audio path.	
42h (1584h)	**REG1584**	**7:0**	**Default : 0x1F**	**Access : R/W**
	N_A1_C0[7:0]	7:0	Coefficient of Notch_A1 on video path(double load).	
42h (1585h)	**REG1585**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	N_A1_C0[10:8]	2:0	See description of '1584h'.	
43h (1586h)	**REG1586**	**7:0**	**Default : 0x3C**	**Access : R/W**
	N_A1_C1[7:0]	7:0	Coefficient of Notch_A1 on video path(double load).	
43h (1587h)	**REG1587**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:3	Reserved.	
	N_A1_C1[10:8]	2:0	See description of '1586h'.	
44h (1588h)	**REG1588**	**7:0**	**Default : 0xAE**	**Access : R/W**
	N_A1_C2[7:0]	7:0	Coefficient of Notch_A1 on video path(double load).	
44h (1589h)	**REG1589**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:3	Reserved.	
	N_A1_C2[10:8]	2:0	See description of '1588h'.	
45h (158Ah)	**REG158A**	**7:0**	**Default : 0x99**	**Access : R/W**
	N_A2_C0[7:0]	7:0	Coefficient of Notch_A2 on video path(double load).	
45h (158Bh)	**REG158B**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	N_A2_C0[10:8]	2:0	See description of '158Ah'.	
46h (158Ch)	**REG158C**	**7:0**	**Default : 0x3C**	**Access : R/W**
	N_A2_C1[7:0]	7:0	Coefficient of Notch_A2 on video path(double load).	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
46h (158Dh)	**REG158D**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:3	Reserved.	
	N_A2_C1[10:8]	2:0	See description of '158Ch'.	
47h (158Eh)	**REG158E**	**7:0**	**Default : 0x2D**	**Access : R/W**
	N_A2_C2[7:0]	7:0	Coefficient of Notch_A2 on video path(double load).	
47h (158Fh)	**REG158F**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:3	Reserved.	
	N_A2_C2[10:8]	2:0	See description of '158Eh'.	
48h (1590h)	**REG1590**	**7:0**	**Default : 0xA7**	**Access : R/W**
	AN_C0[7:0]	7:0	Coefficient of A_NOTCH on audio path(double load).	
48h (1591h)	**REG1591**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	AN_C0[10:8]	2:0	See description of '1590h'.	
49h (1592h)	**REG1592**	**7:0**	**Default : 0x3C**	**Access : R/W**
	AN_C1[7:0]	7:0	Coefficient of A_NOTCH on audio path(double load).	
49h (1593h)	**REG1593**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:3	Reserved.	
	AN_C1[10:8]	2:0	See description of '1592h'.	
4Ah (1594h)	**REG1594**	**7:0**	**Default : 0x4F**	**Access : R/W**
	AN_C2[7:0]	7:0	Coefficient of A_NOTCH on audio path(double load).	
4Ah (1595h)	**REG1595**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	AN_C2[10:8]	2:0	See description of '1594h'.	
4Bh (1596h)	**REG1596**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS11_C0[7:0]	7:0	Coefficient of sos11(double load).	
4Bh (1597h)	**REG1597**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS11_C0[10:8]	2:0	See description of '1596h'.	
4Ch (1598h)	**REG1598**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS11_C1[7:0]	7:0	Coefficient of sos11(double load).	
4Ch (1599h)	**REG1599**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS11_C1[10:8]	2:0	See description of '1598h'.	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Dh (159Ah)	**REG159A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS11_C2[7:0]	7:0	Coefficient of sos11(double load).	
4Dh (159Bh)	**REG159B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS11_C2[10:8]	2:0	See description of '159Ah'.	
4Eh (159Ch)	**REG159C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS11_C3[7:0]	7:0	Coefficient of sos11(double load).	
4Eh (159Dh)	**REG159D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS11_C3[10:8]	2:0	See description of '159Ch'.	
4Fh (159Eh)	**REG159E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS11_C4[7:0]	7:0	Coefficient of sos11(double load).	
4Fh (159Fh)	**REG159F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS11_C4[10:8]	2:0	See description of '159Eh'.	
50h (15A0h)	**REG15A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS12_C0[7:0]	7:0	Coefficient of sos12(double load).	
50h (15A1h)	**REG15A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS12_C0[10:8]	2:0	See description of '15A0h'.	
51h (15A2h)	**REG15A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS12_C1[7:0]	7:0	Coefficient of sos12(double load).	
51h (15A3h)	**REG15A3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS12_C1[10:8]	2:0	See description of '15A2h'.	
52h (15A4h)	**REG15A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS12_C2[7:0]	7:0	Coefficient of sos12(double load).	
52h (15A5h)	**REG15A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS12_C2[10:8]	2:0	See description of '15A4h'.	
53h (15A6h)	**REG15A6**	**7:0**	**Default : 0x00**	**Access : R/W**
	N_A3_C0[7:0]	7:0	Coefficient of Notch_A3 on video path(double load).	
53h	**REG15A7**	**7:0**	**Default : 0x00**	**Access : R/W**

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15A7h)	-	7:3	Reserved.	
	N_A3_C0[10:8]	2:0	See description of '15A6h'.	
54h (15A8h)	**REG15A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	N_A3_C1[7:0]	7:0	Coefficient of Notch_A3 on video path(double load).	
54h (15A9h)	**REG15A9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	N_A3_C1[10:8]	2:0	See description of '15A8h'.	
55h (15AAh)	**REG15AA**	**7:0**	**Default : 0x00**	**Access : R/W**
	N_A3_C2[7:0]	7:0	Coefficient of Notch_A3 on video path(double load).	
55h (15ABh)	**REG15AB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	N_A3_C2[10:8]	2:0	See description of '15AAh'.	
56h (15ACh)	**REG15AC**	**7:0**	**Default : 0x83**	**Access : R/W**
	N_A4_C0[7:0]	7:0	Coefficient of Notch_A4 on video path(double load).	
56h (15ADh)	**REG15AD**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	N_A4_C0[10:8]	2:0	See description of '15ACh'.	
57h (15AEh)	**REG15AE**	**7:0**	**Default : 0x3C**	**Access : R/W**
	N_A4_C1[7:0]	7:0	Coefficient of Notch_A4 on video path(double load).	
57h (15AFh)	**REG15AF**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:3	Reserved.	
	N_A4_C1[10:8]	2:0	See description of '15AEh'.	
58h (15B0h)	**REG15B0**	**7:0**	**Default : 0x54**	**Access : R/W**
	N_A4_C2[7:0]	7:0	Coefficient of Notch_A4 on video path(double load).	
58h (15B1h)	**REG15B1**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:3	Reserved.	
	N_A4_C2[10:8]	2:0	See description of '15B0h'.	
59h (15B2h)	**REG15B2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS12_C3[7:0]	7:0	Coefficient of sos12(double load).	
59h (15B3h)	**REG15B3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS12_C3[10:8]	2:0	See description of '15B2h'.	
5Ah	**REG15B4**	**7:0**	**Default : 0x00**	**Access : R/W**

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(15B4h)	SOS12_C4[7:0]	7:0	Coefficient of sos12(double load).	
5Ah (15B5h)	**REG15B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS12_C4[10:8]	2:0	See description of '15B4h'.	
5Bh (15B6h)	**REG15B6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS21_C0[7:0]	7:0	Coefficient of sos21(double load).	
5Bh (15B7h)	**REG15B7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS21_C0[10:8]	2:0	See description of '15B6h'.	
5Ch (15B8h)	**REG15B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS21_C1[7:0]	7:0	Coefficient of sos21 (double load).	
5Ch (15B9h)	**REG15B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS21_C1[10:8]	2:0	See description of '15B8h'.	
5Dh (15BAh)	**REG15BA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS21_C2[7:0]	7:0	Coefficient of sos21 (double load).	
5Dh (15BBh)	**REG15BB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS21_C2[10:8]	2:0	See description of '15BAh'.	
5Eh (15BCh)	**REG15BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS21_C3[7:0]	7:0	Coefficient of sos21(double load).	
5Eh (15BDh)	**REG15BD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS21_C3[10:8]	2:0	See description of '15BCh'.	
5Fh (15BEh)	**REG15BE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS21_C4[7:0]	7:0	Coefficient of sos21 (double load).	
5Fh (15BFh)	**REG15BF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS21_C4[10:8]	2:0	See description of '15BEh'.	
60h (15C0h)	**REG15C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS22_C0[7:0]	7:0	Coefficient of sos22(double load).	
60h (15C1h)	**REG15C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SOS22_C0[10:8]	2:0	See description of '15C0h'.	
61h (15C2h)	**REG15C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS22_C1[7:0]	7:0	Coefficient of sos22(double load).	
61h (15C3h)	**REG15C3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS22_C1[10:8]	2:0	See description of '15C2h'.	
62h (15C4h)	**REG15C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS22_C2[7:0]	7:0	Coefficient of sos22(double load).	
62h (15C5h)	**REG15C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS22_C2[10:8]	2:0	See description of '15C4h'.	
63h (15C6h)	**REG15C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS22_C3[7:0]	7:0	Coefficient of sos22(double load).	
63h (15C7h)	**REG15C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS22_C3[10:8]	2:0	See description of '15C6h'.	
64h (15C8h)	**REG15C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS22_C4[7:0]	7:0	_b4tob0.	
64h (15C9h)	**REG15C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS22_C4[10:8]	2:0	See description of '15C8h'.	
65h (15CAh)	**REG15CA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS31_C0[7:0]	7:0	Coefficient of sos31 (double load).	
65h (15CBh)	**REG15CB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS31_C0[10:8]	2:0	See description of '15CAh'.	
66h (15CCh)	**REG15CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS31_C1[7:0]	7:0	Coefficient of sos31 (double load).	
66h (15CDh)	**REG15CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS31_C1[10:8]	2:0	See description of '15CCh'.	
67h (15CEh)	**REG15CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS31_C2[7:0]	7:0	Coefficient of sos31 (double load).	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
67h (15CFh)	**REG15CF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS31_C2[10:8]	2:0	See description of '15CEh'.	
68h (15D0h)	**REG15D0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS31_C3[7:0]	7:0	Coefficient of sos31 (double load).	
68h (15D1h)	**REG15D1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS31_C3[10:8]	2:0	See description of '15D0h'.	
69h (15D2h)	**REG15D2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS31_C4[7:0]	7:0	Coefficient of sos31 (double load).	
69h (15D3h)	**REG15D3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS31_C4[10:8]	2:0	See description of '15D2h'.	
6Ah (15D4h)	**REG15D4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS32_C0[7:0]	7:0	Coefficient of sos32 (double load).	
6Ah (15D5h)	**REG15D5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS32_C0[10:8]	2:0	See description of '15D4h'.	
6Bh (15D6h)	**REG15D6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS32_C1[7:0]	7:0	Coefficient of sos32 (double load).	
6Bh (15D7h)	**REG15D7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS32_C1[10:8]	2:0	See description of '15D6h'.	
6Ch (15D8h)	**REG15D8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS32_C2[7:0]	7:0	Coefficient of sos32 (double load).	
6Ch (15D9h)	**REG15D9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS32_C2[10:8]	2:0	See description of '15D8h'.	
6Dh (15DAh)	**REG15DA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS32_C3[7:0]	7:0	Coefficient of sos32 (double load).	
6Dh (15DBh)	**REG15DB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS32_C3[10:8]	2:0	See description of '15DAh'.	

DBB1 Register (Bank = 15)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Eh (15DCh)	**REG15DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOS32_C4[7:0]	7:0	Coefficient of sos32 (double load).	
6Eh (15DDh)	**REG15DD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SOS32_C4[10:8]	2:0	See description of '15DCh'.	
7Fh ~ 7Fh (15FEh ~ 15FFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

DBB2 Register (Bank = 16)

DBB2 Register (Bank = 16)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1600h)	**REG1600**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7	Reserved.	
	VAGC_VSYNC_ENB	6	0: PGA1/PGA2 update in any time. 1: PGA1/PGA2 update in Vsync blanking.	
	VAGC_VSYNC_ENA	5	0: PGA1/PGA2 update in any time. 1: PGA1/PGA2 update in Vsync blanking.	
	VAGC_GAIN_SLOPE	4	0: Negative gain slope. 1: Positive gain slope.	
	VAGC_MEAN_SEL[1:0]	3:2	Select mean. 00: 1 line. 01: 16 line. 1x: 256 line.	
	VAGC_MODE	1	Mode for positive modulation. 0: Porch. 1: Sync height (from VDAGC). Ready.	
	VAGC_ENABLE	0	0: VAGC disable. 1: VAGC enable. VAGC_ENABLE turn on must after setting ready.	
00h (1601h)	**REG1601**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	VAGC_VSYNC_POL	0	0: Low active. 1: High active.	
01h (1602h)	**REG1602**	**7:0**	**Default : 0x40**	**Access : R/W**
	VAGC_LINE_CNT[7:0]	7:0	Line counter max (double load).	
01h (1603h)	**REG1603**	**7:0**	**Default : 0x00**	**Access : R/W**
	VAGC_LINE_CNT[15:8]	7:0	See description of '1602h'.	
02h (1604h)	**REG1604**	**7:0**	**Default : 0xE0**	**Access : R/W**
	VAGC_PORCH_CNT[7:0]	7:0	Porch counter max (double load).	
02h (1605h)	**REG1605**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VAGC_PORCH_CNT[8]	0	See description of '1604h'.	
03h (1606h)	**REG1606**	**7:0**	**Default : 0x00**	**Access : R/W**
	VAGC_PEAK_CNT[7:0]	7:0	Peak counter max (double load).	

DBB2 Register (Bank = 16)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (1607h)	**REG1607**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:4	Reserved.	
	VAGC_PEAK_CNT[11:8]	3:0	See description of '1606h'.	
04h (1608h)	**REG1608**	**7:0**	**Default : 0x9A**	**Access : R/W**
	VAGC_REF[7:0]	7:0	Reference level (double load).	
04h (1609h)	**REG1609**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VAGC_REF[8]	0	See description of '1608h'.	
05h (160Ah)	**REG160A**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:3	Reserved.	
	VAGC_K[2:0]	2:0	Loop filter parameter. 0 -> 0. 1~7 -> 2^-2~2^-8.	
05h (160Bh)	**REG160B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VAGC_OFFSET[6:0]	6:0	VAGC porch counter offset.	
09h (1612h)	**REG1612**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VAGC_PGA1_MIN[3:0]	3:0	PGA1 min.	
09h (1613h)	**REG1613**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	VAGC_PGA1_MAX[3:0]	3:0	PGA1 max.	
0Ah (1614h)	**REG1614**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VAGC_PGA2_MIN[3:0]	3:0	PGA2 min.	
0Ah (1615h)	**REG1615**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VAGC_PGA2_MAX[3:0]	3:0	PGA2 max.	
0Bh (1616h)	**REG1616**	**7:0**	**Default : 0x00**	**Access : R/W**
	VAGC_VGA_MIN[7:0]	7:0	VGA min (double load).	
0Bh (1617h)	**REG1617**	**7:0**	**Default : 0x80**	**Access : R/W**
	VAGC_VGA_MIN[15:8]	7:0	See description of '1616h'.	
0Ch	**REG1618**	**7:0**	**Default : 0xFF**	**Access : R/W**

DBB2 Register (Bank = 16)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1618h)	VAGC_VGA_MAX[7:0]	7:0	VGA max (double load).	
0Ch (1619h)	**REG1619**	**7:0**	**Default : 0x7F**	**Access : R/W**
	VAGC_VGA_MAX[15:8]	7:0	See description of '1618h'.	
10h (1620h)	**REG1620**	**7:0**	**Default : 0x00**	**Access : RO**
	VAGC_MEAN0[7:0]	7:0	Mean: 1 line.	
11h (1622h)	**REG1622**	**7:0**	**Default : 0x00**	**Access : RO**
	VAGC_MEAN16[7:0]	7:0	Mean: 16 line.	
12h (1624h)	**REG1624**	**7:0**	**Default : 0x00**	**Access : RO**
	VAGC_MEAN256[7:0]	7:0	Mean: 256 line.	
13h (1626h)	**REG1626**	**7:0**	**Default : 0x00**	**Access : RO**
	VAGC_DIFF[7:0]	7:0	Diff.	
13h (1627h)	**REG1627**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	VAGC_DIFF[9:8]	1:0	See description of '1626h'.	
14h (1628h)	**REG1628**	**7:0**	**Default : 0x00**	**Access : RO**
	VAGC_VGA[7:0]	7:0	Tuner VGA value.	
14h (1629h)	**REG1629**	**7:0**	**Default : 0x00**	**Access : RO**
	VAGC_VGA[15:8]	7:0	See description of '1628h'.	
15h (162Ah)	**REG162A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	VAGC_PGA1A[3:0]	3:0	PGA1a.	
15h (162Bh)	**REG162B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	VAGC_PGA2A[3:0]	3:0	PGA2a.	
16h (162Ch)	**REG162C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	VAGC_PGA1B[3:0]	3:0	PGA1b.	
16h (162Dh)	**REG162D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	VAGC_PGA2B[3:0]	3:0	PGA2b.	
17h (162Eh)	**REG162E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	VAGC_PGA1C[3:0]	3:0	PGA1c.	

DBB2 Register (Bank = 16)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
17h (162Fh)	**REG162F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	VAGC_PGA2C[3:0]	3:0	PGA2c.	
18h (1631h)	**REG1631**	**7:0**	**Default : 0x00**	**Access : RO**
	VAGC_MAX_MEAN[7:0]	7:0	Max mean.	
23h (1646h)	**REG1646**	**7:0**	**Default : 0x00**	**Access : R/W**
	VAGC_VGA_THR[7:0]	7:0	VGA threshold (double load).	
23h (1647h)	**REG1647**	**7:0**	**Default : 0x80**	**Access : R/W**
	VAGC_VGA_THR[15:8]	7:0	See description of '1646h'.	
24h (1648h)	**REG1648**	**7:0**	**Default : 0x00**	**Access : R/W**
	VAGC_VGA_BASE[7:0]	7:0	Digital VGA base adjustment.	
24h (1649h)	**REG1649**	**7:0**	**Default : 0x00**	**Access : R/W**
	VAGC_VGA_OFFS[7:0]	7:0	Digital VGA offs adjustment.	
25h ~ 27h (164Ah ~ 164Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
51h (16A2h)	**REG16A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	AAGC_LINE_CNT[5:0]	5:0	AAGC line counter max.	
52h (16A4h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
52h (16A5h)	**REG16A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	AAGC_DEC[7:0]	7:0	Decimation (for mean). <8,0>.	
54h (16A8h)	**REG16A8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	AAGC_PGA1_MIN[3:0]	3:0	PGA1 min.	
54h (16A9h)	**REG16A9**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	AAGC_PGA1_MAX[3:0]	3:0	PGA1 max.	
55h (16AAh)	**REG16AA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	AAGC_PGA2_MIN[3:0]	3:0	PGA2 min.	

DBB2 Register (Bank = 16)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (16ABh)	**REG16AB**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	AAGC_PGA2_MAX[3:0]	3:0	PGA2 max.	
56h (16ACh)	**REG16AC**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7	Reserved.	
	AAGC_MEAN_MIN[6:0]	6:0	Mean min.	
56h (16ADh)	**REG16AD**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7	Reserved.	
	AAGC_MEAN_MAX[6:0]	6:0	Mean max.	
57h (16AEh)	**REG16AE**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	AAGC_MEAN[6:0]	6:0	Mean.	
58h (16B0h)	**REG16B0**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	AAGC_PEAKMEAN[6:0]	6:0	Peak mean.	
59h (16B2h)	**REG16B2**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	AAGC_PGA1[3:0]	3:0	PGA1.	
59h (16B3h)	**REG16B3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	AAGC_PGA2[3:0]	3:0	PGA2.	
5Ah (16B4h)	**REG16B4**	**7:0**	**Default : 0xFF**	**Access : R/W**
	AAGC_CNT[7:0]	7:0	AAGC counter max (double load).	
5Ah (16B5h)	**REG16B5**	**7:0**	**Default : 0x3F**	**Access : R/W**
	AAGC_CNT[15:8]	7:0	See description of '16B4h'.	
5Bh (16B6h)	**REG16B6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	AAGC_CNT[20:16]	4:0	See description of '16B4h'.	
70h ~ 71h (16E0h ~ 16E3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

DBB3 Register (Bank = 1B)

DBB3 Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1B00h)	**REG1B00**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	VDAGC1_DL_BYPASS	3	1=VDAGC1 delay line bypass.	
	-	2	Reserved.	
	VDAGC1_BYPASS	1	1=VDAGC1 bypass.	
	VDAGC1_ENABLE	0	1=VDAGC1 enable.	
00h (1B01h)	**REG1B01**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	VDAGC2_DL_BYPASS	3	1=VDAGC2 delay line bypass.	
	-	2	Reserved.	
	VDAGC2_BYPASS	1	1=VDAGC2 bypass.	
	VDAGC2_ENABLE	0	1=VDAGC2 enable.	
03h (1B06h)	**REG1B06**	**7:0**	**Default : 0x26**	**Access : R/W**
	-	7:6	Reserved.	
	VDAGC1_REF[5:0]	5:0	VDAGC1 ref.	
03h (1B07h)	**REG1B07**	**7:0**	**Default : 0x26**	**Access : R/W**
	-	7:6	Reserved.	
	VDAGC2_REF[5:0]	5:0	VDAGC2 ref.	
04h (1B08h)	**REG1B08**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:3	Reserved.	
	VDAGC1_LEVEL_SHIFT[2:0]	2:0	VDAGC1 level shift.	
04h (1B09h)	**REG1B09**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:3	Reserved.	
	VDAGC2_LEVEL_SHIFT[2:0]	2:0	VDAGC2 level shift.	
05h (1B0Ah)	**REG1B0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	VDAGC1_RATIO[2:0]	2:0	VDAGC1 lpf update ratio.	
05h (1B0Bh)	**REG1B0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	VDAGC2_RATIO[2:0]	2:0	VDAGC2 lpf update ratio.	
06h (1B0Ch)	**REG1B0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDAGC1_PEAK_CNT[7:0]	7:0	VDAGC1 peak counter max(double load).	

DBB3 Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (1B0Dh)	**REG1B0D**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:4	Reserved.	
	VDAGC1_PEAK_CNT[11:8]	3:0	See description of '1B0Ch'.	
07h (1B0Eh)	**REG1B0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDAGC2_PEAK_CNT[7:0]	7:0	VDAGC2 peak counter max(double load).	
07h (1B0Fh)	**REG1B0F**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:4	Reserved.	
	VDAGC2_PEAK_CNT[11:8]	3:0	See description of '1B0Eh'.	
08h (1B10h)	**REG1B10**	**7:0**	**Default : 0xF8**	**Access : R/W**
	VDAGC1_PORCH_CNT[7:0]	7:0	VDAGC1 porch counter max(double load).	
08h (1B11h)	**REG1B11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VDAGC1_PORCH_CNT[8]	0	See description of '1B10h'.	
09h (1B12h)	**REG1B12**	**7:0**	**Default : 0xF8**	**Access : R/W**
	VDAGC2_PORCH_CNT[7:0]	7:0	VDAGC2 porch counter max(double load).	
09h (1B13h)	**REG1B13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VDAGC2_PORCH_CNT[8]	0	See description of '1B12h'.	
0Ah (1B14h)	**REG1B14**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC1_MEAN[7:0]	7:0	VDAGC1 mean.	
0Ah (1B15h)	**REG1B15**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC1_MEAN[15:8]	7:0	See description of '1B14h'.	
0Bh (1B16h)	**REG1B16**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC1_VAR[7:0]	7:0	VDAGC1 variance.	
0Bh (1B17h)	**REG1B17**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC1_VAR[15:8]	7:0	See description of '1B16h'.	
0Ch (1B18h)	**REG1B18**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC2_MEAN[7:0]	7:0	VDAGC2 mean.	
0Ch (1B19h)	**REG1B19**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC2_MEAN[15:8]	7:0	See description of '1B18h'.	
0Dh (1B1Ah)	**REG1B1A**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC2_VAR[7:0]	7:0	VDAGC2 variance.	
0Dh	**REG1B1B**	**7:0**	**Default : 0x00**	**Access : RO**

DBB3 Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1B1Bh)	VDAGC2_VAR[15:8]	7:0	See description of '1B1Ah'.	
0Eh (1B1Ch)	**REG1B1C**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC1_GAIN[7:0]	7:0	VDAGC1 internal gain.	
0Eh (1B1Dh)	**REG1B1D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	VDAGC1_GAIN[13:8]	5:0	See description of '1B1Ch'.	
0Fh (1B1Eh)	**REG1B1E**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC2_GAIN[7:0]	7:0	VDAGC2 internal gain.	
0Fh (1B1Fh)	**REG1B1F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	VDAGC2_GAIN[13:8]	5:0	See description of '1B1Eh'.	
10h (1B20h)	**REG1B20**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC1_SYNCHEIGHT[7:0]	7:0	VDAGC1 sync height.	
10h (1B21h)	**REG1B21**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	VDAGC1_VSYNC	4	VDAGC1 Vsync coast pulse (high active).	
	-	3:1	Reserved.	
	VDAGC1_SYNCHEIGHT[8]	0	See description of '1B20h'.	
11h (1B22h)	**REG1B22**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC2_SYNCHEIGHT[7:0]	7:0	VDAGC2 sync height.	
11h (1B23h)	**REG1B23**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	VDAGC2_VSYNC	4	VDAGC2 vsync coast pulse (high active).	
	-	3:1	Reserved.	
	VDAGC2_SYNCHEIGHT[8]	0	See description of '1B22h'.	
12h (1B24h)	**REG1B24**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC1_LPF_DELAY_0[7:0]	7:0	VDAGC1 lpf delay line first element.	
12h (1B25h)	**REG1B25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	VDAGC1_LPF_DELAY_0[8]	0	See description of '1B24h'.	
13h (1B26h)	**REG1B26**	**7:0**	**Default : 0x00**	**Access : RO**
	VDAGC2_LPF_DELAY_0[7:0]	7:0	VDAGC2 lpf delay line first element.	
13h	**REG1B27**	**7:0**	**Default : 0x00**	**Access : RO**

DBB3 Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1B27h)	-	7:1	Reserved.	
	VDAGC2_LPF_DELAY_0[8]	0	See description of '1B26h'.	
14h (1B28h)	**REG1B28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VDAGC1_OFFSET[6:0]	6:0	VDAGC1 porch counter offset.	
14h (1B29h)	**REG1B29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VDAGC2_OFFSET[6:0]	6:0	VDAGC2 porch counter offset.	
40h (1B80h)	**REG1B80**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	ADAGC_PEAK_MEAN_SEL	2	1=select peak.	
	ADAGC_BYPASS	1	1=ADAGC1 bypass.	
	ADAGC_ENABLE	0	1=ADAGC1 enable.	
40h (1B81h)	**REG1B81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ADAGC_K[2:0]	2:0	1~7:2^-1~2^-7.	
41h (1B82h)	**REG1B82**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADAGC_CNT[7:0]	7:0	ADAGC counter max(double load).	
41h (1B83h)	**REG1B83**	**7:0**	**Default : 0x01**	**Access : R/W**
	ADAGC_CNT[15:8]	7:0	See description of '1B82h'.	
42h (1B84h)	**REG1B84**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ADAGC_CNT[20:16]	4:0	See description of '1B82h'.	
43h (1B86h)	**REG1B86**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADAGC_DEC[7:0]	7:0	ADAGC decimation.	
43h (1B87h)	**REG1B87**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ADAGC_LINE_CNT[5:0]	5:0	ADAGC line counter max.	
44h (1B88h)	**REG1B88**	**7:0**	**Default : 0x50**	**Access : R/W**
	ADAGC_REF[7:0]	7:0	ADAGC ref.	
45h (1B8Ah)	**REG1B8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ADAGC_GAIN_OREN	0	1=ADAGC gain overwrite enable.	

DBB3 Register (Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
46h (1B8Ch)	**REG1B8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADAGC_GAIN_OV[7:0]	7:0	ADAGC gain overwrite value(double load).	
46h (1B8Dh)	**REG1B8D**	**7:0**	**Default : 0x01**	**Access : R/W**
	ADAGC_GAIN_OV[15:8]	7:0	See description of '1B8Ch'.	
50h (1BA0h)	**REG1BA0**	**7:0**	**Default : 0x00**	**Access : RO**
	ADAGC_MEAN[7:0]	7:0	ADAGC mean.	
50h (1BA1h)	**REG1BA1**	**7:0**	**Default : 0x00**	**Access : RO**
	ADAGC_PEAK[7:0]	7:0	ADAGC peak.	
51h (1BA2h)	**REG1BA2**	**7:0**	**Default : 0x00**	**Access : RO**
	ADAGC_GAIN[7:0]	7:0	ADAGC gain.	
51h (1BA3h)	**REG1BA3**	**7:0**	**Default : 0x00**	**Access : RO**
	ADAGC_GAIN[15:8]	7:0	See description of '1BA2h'.	

OSD Register (Bank = 1C)

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1C01h)	**REG1C01**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DBL[1:0]	2:1	Double buffer load. 00: Keep old register value. 01: Load new data (auto reset to 00 when load finish). 10: Automatically load data at VSYNC blanking. 11: Reserved.	
	DBE	0	Double buffer enable. 0: Disable. 1: Enable.	
01h (1C02h)	**REG1C02**	**7:0**	**Default : 0x00**	**Access : R/W DB**
	OHSTA[7:0]	7:0	OSD window horizontal start position = OHSTA (pixel).	
01h (1C03h)	**REG1C03**	**7:0**	**Default : 0x00**	**Access : R/W DB**
	-	7:3	Reserved.	
	OHSTA[10:8]	2:0	Please see description of '1C02h'.	
02h (1C04h)	**REG1C04**	**7:0**	**Default : 0x00**	**Access : R/W DB**
	OVSTA[7:0]	7:0	OSD window vertical start position = OVSTA (line).	
02h (1C05h)	**REG1C05**	**7:0**	**Default : 0x00**	**Access : R/W DB**
	-	7:3	Reserved.	
	OVSTA[10:8]	2:0	Please see description of '1C04h'.	
03h (1C06h)	**REG1C06**	**7:0**	**Default : 0x00**	**Access : R/W DB**
	OSDW[7:0]	7:0	OSD window width = OSDW + 1 (column), maximum 128 columns.	
03h (1C07h)	**REG1C07**	**7:0**	**Default : 0x00**	**Access : R/W DB**
	-	7:6	Reserved.	
	OSDH[5:0]	5:0	OSD window vertical height = OSDH + 1 (row), maximum 64 rows.	
04h (1C08h)	**REG1C08**	**7:0**	**Default : 0x00**	**Access : R/W**
	OHSPA[7:0]	7:0	OSD window horizontal space start position = OHSPA + 1 (row).	
04h (1C09h)	**REG1C09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OVSPA[5:0]	5:0	OSD window vertical space start position	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			= OVSPA + 1 (column).	
05h (1C0Ah)	**REG1C0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPW[9:2]	7:0	OSD space width = 2 * OSPW (pixel).	
05h (1C0Bh)	**REG1C0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPH[9:2]	7:0	OSD space height = 2 * OSPH (pixel).	
06h (1C0Ch)	**REG1C0C**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OVS[1:0]	7:6	OSD vertical scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.	
	OHS[1:0]	5:4	OSD Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.	
	-	3:1	Reserved	
	MWIN	0	OSD main window display. 0: Main window off. 1: Main window on.	
06h (1C0Dh)	**REG1C0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MFWZ_EN	7	Mono font width zoom x2 enable.	
	-	6	Reserved.	
	MFHZ_EN	5	Mono font high zoom x2/x4 enable. When this bit is set, AEh[3] will be treated as code index bit9 with Mono Font 1K Mode.	
	MT_EN	4	Mono texture enable.	
	TEX_TRASP_EN	3	Texture transparency enable. 0: Disable. 1: Enable.	
	MF16P	2	OSD mono font uses first 16 colors of 256-color palette. 0: Disable. 1: Enable.	
	C16PT_EN	1	OSD 16-color palette transparency enable. 0: Disable. 1: Enable.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			When this bit is set, color index 0x0F will be treated as transparency.	
	CP_SEL	0	OSD color palette select. 0: 16-color palette. 1: 256-color palette.	
07h (1C0Eh)	**REG1C0E**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	SDALL	7	Shadow with all OSD direction, co-work with bit 4. 0: Shadow at right/down side. 1: Shadow at all sides.	
	TXEN	6	OSD texture function enable. 0: Disable. 1: Enable.	
	O_BLK	5	Whole OSD blink function enable. 0: Disable. 1: Enable.	
	SDC	4	OSD window shadow control. 0: Off. 1: On.	
	SCLR[3:0]	3:0	OSD window shadow color index. 0000: Color index 0. 0001: Color index 1. … 1111: Color index 15.	
07h (1C0Fh)	**REG1C0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDSH[3:0]	7:4	OSD shadow height.	
	OSDSW[3:0]	3:0	OSD shadow width.	
08h (1C10h ~ 1C11h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
09h (1C12h)	**REG1C12**	**7:0**	**Default : 0x00**	**Access : R/W**
	COFFS_SEL	7	OSD code buffer offset select. 0: Use OSDW[6:0] as offset. 1: Use OOFFS[6:0] as offset.	
	OOFFS[6:0]	6:0	OSD code buffer Offset value.	
09h (1C13h)	**REG1C13**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OSDBA[7:0]	7:0	OSD code base address.	
0Ah	**REG1C14**	**7:0**	**Default : 0x00**	**Access : R/W, DB**

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1C14h)	-	7:5	Reserved.	
	OSDBA[12:8]	4:0	Please see description of '1C13h'.	
0Ah (1C15h)	**REG1C15**	**7:0**	**Default : 0x00**	**Access : R/W**
	GVS[1:0]	7:6	Gradually color vertical scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.	
	GHS[1:0]	5:4	Gradually color horizontal scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.	
	GRAD	3	Enable OSD gradually color function. 0: Disable. 1: Enable.	
	GCRNG[2:0]	2:0	Gradually color applied range. 000: OSD sub window 0. 001: OSD sub window 1. 010: OSD sub window 2. 011: OSD sub window 3. 1xx: Full screen.	
0Bh (1C16h)	**GRADCLR**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCS	7	Gradually color source. 0: Use this register bit[5:0] to define color. 1: Use Bank 00 background color to define color.	
	F/B	6	Gradually applied color. 0: Background color. 1: Foreground color.	
	RCLR[1:0]	5:4	Red starting gradually color. 00: Red color is 00h. 01: Red color is 55h. 10: Red color is AAh. 11: Red color is FFh.	
	GCLR[1:0]	3:2	Green starting gradually color. 00: Green color is 00h. 01: Green color is 55h. 10: Green color is AAh.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: Green color is FFh.	
	BCLR[1:0]	1:0	Blue starting gradually color. 00: Blue color is 00h. 01: Blue color is 55h. 10: Blue color is AAh. 11: Blue color is FFh.	
0Bh (1C17h)	**REG1C17**	**7:0**	**Default : 0x00**	**Access : R/W**
	SR	7	Sign bit of red color. 0: Increase. 1: Decrease.	
	IRH	6	Inverse bit of red color. 0: Normal. 1: Invert.	
	R_GRADH[5:0]	5:0	Increase/Decrease value of red color.	
0Ch (1C18h)	**REG1C18**	**7:0**	**Default : 0x00**	**Access : R/W**
	SG	7	Sign bit of green color. 0: Increase. 1: Decrease.	
	IGH	6	Inverse bit of green color. 0: Normal. 1: Invert.	
	G_GRADH[5:0]	5:0	Increase/Decrease value of green color.	
0Ch (1C19)	**REG1C19**	**7:0**	**Default : 0x00**	**Access : R/W**
	SB	7	Sign bit of blue color. 0: Increase. 1: Decrease.	
	IBH	6	Inverse bit of blue color. 0: Normal. 1: Invert.	
	B_GRADH[5:0]	5:0	Increase/Decrease value of blue color.	
0Dh (1C1A)	**REG1C1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HGRADSR[7:0]	7:0	Horizontal gradually step of red color.	
0Dh (1C1Bh)	**REG1C1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HGRADSG[7:0]	7:0	Horizontal gradually step of green color.	
0Eh	**REG1C1C**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1C1Ch)	HGRADSB[7:0]	7:0	Horizontal gradually step of blue color.	
	For example, of RCLR=0, R_GRADH=16h, and HGRADSR=20h, then Pixel 0 ~ 19 = 0; Pixel 20 ~ 39 = 16; Pixel 40 ~ 59 = 32; … etc.			
0Eh (1C1Dh)	**REG1C1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SR	7	Sign bit of red color. 0: Increase. 1: Decrease.	
	IRV	6	Inverse bit of red color. 0: Normal. 1: Invert.	
	R_GRADV[5:0]	5:0	Increase/Decrease value of red color.	
0Fh (1C1Eh)	**REG1C1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SG	7	Sign bit of green color. 0: Increase. 1: Decrease.	
	IGV	6	Inverse bit of green color. 0: Normal. 1: Invert.	
	G_GRADV[5:0]	5:0	Increase/Decrease value of green color.	
0Fh (1C1Fh)	**REG1C1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SB	7	Sign bit of blue color. 0: Increase. 1: Decrease.	
	IBV	6	Inverse bit of blue color. 0: Normal. 1: Invert.	
	B_GRADV[5:0]	5:0	Increase/Decrease value of blue color.	
10h (1C20h)	**REG1C20**	**7:0**	**Default : 0x00**	**Access : R/W**
	VGRADSR[7:0]	7:0	Vertical gradually step of red color.	
10h (1C21h)	**REG1C21**	**7:0**	**Default : 0x00**	**Access : R/W**
	VGRADSG[7:0]	7:0	Vertical gradually step of green color.	
11h (1C22h)	**REG1C22**	**7:0**	**Default : 0x00**	**Access : R/W**
	VGRADSB[7:0]	7:0	Vertical gradually step of blue color.	
11h	**REG1C23**	**7:0**	**Default : 0x00**	**Access : R/W, DB**

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1C23h)	-	7:2	Reserved.	
	SUB0C	1	OSD sub window 0 color select. 0: From OSD sub window 0 attribute. 1: From attribute RAM.	
	SUB0E	0	Enable OSD sub window 0. 0: Disable. 1: Enable.	
12h (1C24h)	**REG1C24**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	SUB0HST[7:0]	7:0	OSD sub window 0 horizontal start position.	
12h (1C25h)	**REG1C25**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	SUB0HEND[7:0]	7:0	OSD sub window 0 horizontal end position.	
13h (1C26h)	**REG1C26**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:6	Reserved.	
	SUB0VST[5:0]	5:0	OSD sub window 0 vertical start position.	
13h (1C27h)	**SUB0VEND**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:6	Reserved.	
	SUB0VEND[5:0]	5:0	OSD sub window 0 vertical end position.	
14h (1C28h)	**REG1C28**	**7:0**	**Default : 0x00**	**Access : R/W**
	FGCLR[3:0]	7:4	OSD sub window 0 foreground color select. 0000: Color index 0. 0001: Color index 1. … 1110: Color index E. 1111: Color index F.	
	BGCLR[3:0]	3:0	OSD sub window 0 background color select. 0000: Color index 0. 0001: Color index 1. … 1110: Color index E. 1111: Color index F.	
14h (1C29h)	**REG1C29**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:2	Reserved.	
	SUB1C	1	OSD sub window 1 color select.	
	SUB1E	0	Enable OSD sub window 1.	
15h (1C2Ah)	**REG1C2A**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	SUB1HST[7:0]	7:0	Sub window 1 horizontal start position.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (1C2Bh)	**REG1C2B**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	SUB1HEND[7:0]	7:0	OSD sub window 1 horizontal end position.	
16h (1C2Ch)	**REG1C2C**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:6	Reserved.	
	SUB1VST[5:0]	5:0	OSD sub window 1 vertical start position.	
16h (1C2Dh)	**REG1C2D**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:6	Reserved.	
	SUB1VEND[5:0]	5:0	OSD sub window 1 vertical end position.	
17h (1C2Eh)	**REG1C2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FGCLR[3:0]	7:4	OSD sub window 1 foreground color select. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index F.	
	BGCLR[3:0]	3:0	OSD sub window 1 background color select. 0000: Color index 0. 0001: Color index 1. ... 1110: Color index E. 1111: Color index F.	
17h (1C2Fh)	**REG1C2F**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:2	Reserved.	
	SUB2C	1	OSD sub window 2 color select.	
	SUB2E	0	Enable OSD sub window 2.	
18h (1C30h)	**REG1C30**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	SUB2HST[7:0]	7:0	OSD sub window 2 horizontal start position.	
18h (1C31h)	**REG1C31**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	SUB2HEND[7:0]	7:0	OSD sub window 2 horizontal end position.	
19h (1C32h)	**REG1C32**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:6	Reserved.	
	SUB2VST[5:0]	5:0	OSD sub window 2 vertical start position.	
19h (1C33h)	**REG1C33**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7:6	Reserved.	
	SUB2VEND[5:0]	5:0	OSD sub window 2 vertical end position.	
1Ah	**REG1C34**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Bank = 1C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(1C34h)	FGCLR[3:0]	7:4	OSD sub window 2 foreground color select. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index F.
	BGCLR[3:0]	3:0	OSD sub window 2 background color select. 0000: Color index 0. 0001: Color index 1. ... 1110: Color index E. 1111: Color index F.
1Ah (1C35h)	**REG1C35**	**7:0**	**Default : 0x00** **Access : R/W, DB**
	-	7:2	Reserved.
	SUB3C	1	OSD sub window 3 color select.
	SUB3E	0	Enable OSD sub window 3.
1Bh (1C36h)	**REG1C36**	**7:0**	**Default : 0x00** **Access : R/W, DB**
	SUB3HST[7:0]	7:0	OSD sub window 3 horizontal start position.
1Bh (1C37h)	**REG1C37**	**7:0**	**Default : 0x00** **Access : R/W, DB**
	SUB3HEND[7:0]	7:0	OSD sub window 3 horizontal end position.
1Ch (1C38h)	**REG1C38**	**7:0**	**Default : 0x00** **Access : R/W, DB**
	-	7:6	Reserved.
	SUB3VST[5:0]	5:0	OSD sub window 3 vertical start position.
1Ch (1C39h)	**REG1C39**	**7:0**	**Default : 0x00** **Access : R/W, DB**
	-	7:6	Reserved.
	OSDSUB3VEND[5:0]	5:0	OSD sub window 3 vertical end position.
1Dh (1C3Ah)	**REG1C3A**	**7:0**	**Default : 0x00** **Access : R/W**
	FGCLR[3:0]	7:4	OSD sub window 3 foreground color select. 0000: Color index 0. 0001: Color index 1. ... 1111: Color index F.
	BGCLR[3:0]	3:0	OSD sub window 3 background color select. 0000: Color index 0. 0001: Color index 1. ... 1110: Color index E.

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1111: Color index F.	
1Dh (1C3Bh)	**REG1C3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	OHSPA2[7:0]	7:0	OSD window horizontal space start position 2 = OHSPA 2+ 1 (row).	
1Eh (1C3Ch)	**REG1C3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OVSPA2[5:0]	5:0	OSD window vertical space start position 2 = OVSPA 2+ 1 (column).	
1Eh (1C3Dh)	**REG1C3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPW2[9:2]	7:0	OSD space width 2 = 2 * OSPW2 (pixel).	
1Fh (1C3Eh)	**REG1C3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPH2[9:2]	7:0	OSD space height 2 = 2 * OSPH2 (pixel).	
1Fh (1C3Fh)	**REG1C3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	BREN	7	OSD brightness enable.	
	BRDIR	6	OSD brightness direction. 0: Increase. 1: Decrease.	
	DBRVAL[5:0]	5:0	OSD brightness value * 4.	
20h (1C40h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
20h (1C41h)	**REG1C42**	**7:0**	**Default : 0x1F**	**Access : R/W**
	BLINKSPD[7:0]	7:0	OSD blink speed, the numbers of VSYNCx2.	
21h (1C42h)	**REG1C43**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCRLSPD[7:0]	7:0	OSD Scroll function speed, the numbers of VSYNCx2.	
21h (1C43h)	**SCRLLINE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCREN	7	OSD scroll function enable.	
	VSCR_FAST	6	Scroll at every VSYNC.	
	TRUC_EN	5	Truncate code/attribute enable.	
	SCRLLINE	4:0	OSD scroll function, the numbers of scan lines per scroll.	
22h (1C44h)	**REG1C44**	**7:0**	**Default :**	**Access : R/W**
	-	7:6	Reserved.	
	TEXIR[5:0]	5:0	Initial texture row number. Hardware will automatically increase after scrolling. Software must	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			clear this register after scrolling if texture function is used.	
22h (1C45h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
23h (1C46h)	**REG1C46**	**7:0**	**Default : 0x10**	**Access : R/W**
	FONT_W	7	0: Write font with width 12. 1: Write font with width 16.	
	FONT_H16	6	0: Write font with height 18. 1: Write font with height 16.	
	FNT_W16	5	0: Font width depends on AEh[1]. 1: Force display font width 16.	
	FNT_W12	4	0: Font width depends on AEh[1]. 1: Force display font width 12.	
	FONT_H32	3	0: Write font with height 18. 1: Write font with height 32. Do not simultaneously set bit[6] and bit[3].	
	-	2:0	Reserved.	
23h (1C47h)	**REG1C47**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	DEF_CH_W[3:0]	3:0	The real display font width of font width 16.	
24h (1C48h)	**REG1C48**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	DEF_CH_H[3:0]	3:0	The display font Height of display OSD (2*(DEF_CH_H +1)).	
24h (1C49h)	**REG1C49**	**7:0**	**Default : 0x31**	**Access : R/W**
	CA_TRC_NUM	7:0	Truncate number of 4k code/attribute, only active when 43h[5] is set.	
25h (1C4Ah)	**REG1C4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEF_TEX_CLR[3:0]	3:0	When bank 0 REG 76h[7]=1, attribute bit[14:12] is used to define OSD blending level. Then texture color 4 high bits of 256 palette is defined here.	
25h (1C4Bh)	**REG1C4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	ITATLIC_RS_OFST[1:0]	7:6	OSD Italic right shift offset. 00: 1 pixel. 01: 2 pixels.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: 3 pixels. 11: 4 pixels.	
	ITALIC_1ST_LINE[1:0]	5:4	OSD Italic start scan line. 00: 0 line. 01: 1 lines. 10: 2 lines. 11: 3 lines.	
	ITALIC_LS_STEP[1:0]	3:2	OSD Italic left shift step. 00: 0.001 (pixel, binary). 01: 0.010 (pixel, binary). 10: 0.011 (pixel, binary). 11: 0.100 (pixel, binary).	
	ITATLIC_EN	1	OSD Italic function enable.	
	ITALIC_FORCE	0	All mono character force to Italic.	
26h (1C4Ch)	**REG1C4C**	**7:0**	**Default : 0x81**	**Access : R/W**
	UN_LL	7	Under line at last line.	
	UN_LL2	6	Under line at last 2 lines.	
	OSD_MUX_IP_DATA	5	OSD MUX with IP data path. 0: Main window. 1: Sub window.	
	OSD_IVS_SEL	4	OSD input VSYNC signal select. 0: Sample range V signal related. 1: VSYNC signal related.	
	-	3:2	Reserved.	
	OSD_EXT	1	OSD 8bit -> 10 bit extend method. 0: extend 0. 1: extend MSB.	
	-	0	Reserved.	
26h ~ 27h (1C4Dh ~ 1C4Eh)	-	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
27h (1C4Fh)	**REG1C4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ABM[2:0]	2:0	Alpha blending mode. 000: No alpha blending. 001: Background alpha blending. 101: Foreground alpha blending.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			011: Color key alpha blending. 100: Not color key alpha blending. 101: Entire OSD alpha blending. 11x: Reserved	
28h (1C50h)	**REG1C50**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY1[7:0]	7:0	OSD color key 1 for 256-color palette.	
28h (1C51h)	**REG1C51**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY2[7:0]	7:0	OSD color key 2 for 256-color palette.	
29h (1C52h)	**REG1C52**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY3[7:0]	7:0	OSD color key 3 for 256-color palette.	
29h (1C53h)	**REG1C53**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY4[7:0]	7:0	OSD color key 4 for 256-color palette.	
2Ah (1C54h)	**REG1C54**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY5[7:0]	7:0	OSD color key 5 for 256-color palette.	
2Ah (1C55h)	**REG1C55**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY6[7:0]	7:0	OSD color key 6 for 256-color palette.	
2Bh (1C56h)	**REG1C56**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY7[7:0]	7:0	OSD color key 7 for 256-color palette.	
2Bh (1C57h)	**REG1C57**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY8[7:0]	7:0	OSD color key 8 for 256-color palette.	
2Ch (1C58h)	**REG1C58**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY9[7:0]	7:0	OSD color key 9 for 256-color palette.	
2Ch (1C59h)	**REG1C59**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY10[7:0]	7:0	OSD color key 10 for 256-color palette.	
2Dh (1C5Ah)	**REG1C5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY11[7:0]	7:0	OSD color key 11 for 256-color palette.	
2Dh (1C5Bh)	**REG1C5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY12[7:0]	7:0	OSD color key 12 for 256-color palette.	
2Eh (1C5Ch)	**REG1C5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY13[7:0]	7:0	OSD color key 13 for 256-color palette.	
2Eh (1C5Dh)	**REG1C5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY14[7:0]	7:0	OSD color key 14 for 256-color palette.	
2Fh (1C5Eh)	**REG1C5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY15[7:0]	7:0	OSD color key 15 for 256-color palette.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Fh (1C5Fh)	**REG1C5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCKEY16[7:0]	7:0	OSD color key 16 for 256-color palette.	
30h (1C60h)	**REG1C60**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBC_DTATA[7:0]	7:0	OSD clear function data.	
30h (1C61h)	**REG1C61**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBC_DTATA[15:8]	7:0	Please see description of '1C60h'.	
31h (1C62h)	**REG1C62**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OBC_ADR[7:0]	7:0	OSD clear function start address.	
31h (1C63h)	**REG1C63**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OBC_ATR1_EN	7	OSD clear attribute1 enable.	
	OBC_ATR0_EN	6	OSD clear attribute0 enable.	
	OBC_CODE_EN	5	OSD clear code enable.	
	OBC_ADR[12:8]	4:0	Please see description of '1C62h'.	
32h (1C64h)	**REG1C64**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	-	7	Reserved.	
	OBC_WIDTH	7:0	OSD clear function width.	
32h (1C65h)	**REG1C65**	**7:0**	**Default : 0x00**	**Access : R/W, DB**
	OBC_OFFSET[7:0]	7:0	OSD clear function offset.	
33h (1C66h)	**OSPHW_LSB**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSPH2[1:0]	7:6	See description for OSPH2.	
	OSPW2[1:0]	5:4	See description for OSPW2.	
	OSPH[1:0]	3:2	See description for OSPH.	
	OSPW[1:0]	1:0	See description for OSPW.	
33h (1C67h)	**REG1C67**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBCT	7	OSD clear function trigger. Setting this bit to "1" will trigger H/W to clear OSD block during VSYNC display period. H/W will set this bit back to "0" when OSD block is cleared.	
	OBC_HIGH	6:0	OSD clear function high.	
34h ~ 38h (1C68h ~ 1C70h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
38h (1C71h)	**REG1C71**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TG_BIT	4	Test pattern resolution. 0: 8 bits. 1: 10 bits.	
	-	3	Reserved.	
	NOISE_MD	2:0		
39h (1C73h)	**REG1C73**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
3Ah (1C74h)	**REG1C74**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:0	Reserved.	
3Ah (1C75h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
3Bh (1C76h)	**REG1C76**	**7:0**	**Default : 0x00**	**Access : R/W**
	BLEND_MD	7	OSD blend mode.	
	BLEND_POL	6	OSD blend polarity.	
	BLEND[5:0]	5:0	OSD blend value.	
3Bh (1C77h)	**REG1C77**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	-	7:2	Reserved.	
	VERT_FLIP_EN	1	OSD vertical flip enable. 0: Disable. 1: Enable. Before setting this bit to "1", firmware needs to set 13h/14h VERT_FLIP code base address.	
	FONT_SHRINK_EN	0	OSD font shrink enable. 0: Disable. 1: Enable.	
3Ch (1C78h)	**REG1C78**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SHRINK_BG_EN	7	Font shrink back ground enable.	
	ATR1_SRC_SEL	6	ATR1 source select. 0: New ATR request. 1: Original ATR request.	
	OBC_LOAD_INV	5	OBC load invert. 1: Means select start trigger invert.	
	OBC_LOAD_SEL[1:0]	4:3	OBC load select. 00: Select start trigger from VS_PLS. 01: Select start trigger from VDE_END_PLS. 10: Select start trigger from IVS.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: Select start trigger from CPURW_BLOCK_AREA.	
	WP_FIFO_FULL	2	Write FIFO full (for different type writes, firmware needs to check this bit). 0: Not full. 1: Full.	
	WP_FIFO_EMPTY	1	Write FIFO empty (for different type writes, firmware needs to check this bit). 0: Not empty. 1: Empty.	
	-	0	Reserved.	
3Ch (1C79h)	**REG1C79**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:3	Reserved.	
	RP_BW_FAIL	2	OSD read path bandwidth fail.	
	RP_BW_FAIL_CLR	1	Clear OSD read path bandwidth fail signal.	
	OBC_FORCE_START	0	OBC force start. 1: OBC start trigger from S/W OBCT enable.	
40h (1C80h)	**REG1C80**	**7:0**	**Default : 0x00**	**Access : R/W**
	WP_CODE_BASADR[7:0]	7:0	OSD write path code base-address.	
40h (1C81h)	**REG1C81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WP_CODE_BASADR[11:8]	3:0	Please see description of '1C80h'.	
41h (1C82h)	**REG1C82**	**7:0**	**Default : 0x00**	**Access : R/W**
	WP_ATTRI0_BASADR[7:0]	7:0	OSD write path attribute0 base-address.	
41h (1C83h)	**REG1C83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WP_ATTRI0_BASADR[11:8]	3:0	Please see description of '1C82h'.	
42h (1C84h)	**REG1C84**	**7:0**	**Default : 0x00**	**Access : R/W**
	WP_ATTRI1_BASADR[7:0]	7:0	OSD write path attribute1 base-address.	
42h (1C85h)	**REG1C85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WP_ATTRI1_BASADR[11:8]	3:0	Please see description of '1C84h'.	
43h (1C86h)	**REG1C86**	**7:0**	**Default : 0x00**	**Access : R/W**
	WP_TEX_GRP_BASADR[7:0]	7:0	OSD write path texture group base-address.	
43h	**REG1C87**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1C87h)	-	7:4	Reserved.	
	WP_TEX_GRP_BASADR[11:8]	3:0	Please see description of '1C86h'.	
44h (1C88h)	**REG1C88**	**7:0**	**Default : 0x00**	**Access : R/W**
	WP_FONT1BP_BASADR[7:0]	7:0	OSD write path 1bp font base-address.	
44h (1C89h)	**REG1C89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WP_FONT1BP_BASADR[11:8]	3:0	Please see description of '1C88h'.	
45h (1C8Ah)	**REG1C8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	WP_FONT2BP_BASADR[7:0]	7:0	OSD write path 2bp font base-address.	
45h (1C8Bh)	**REG1C8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WP_FONT2BP_BASADR[11:8]	3:0	Please see description of '1C8Ah'.	
46h (1C8Ch)	**REG1C8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	WP_FONT4BP_BASADR[7:0]	7:0	OSD write path 4bp font base-address.	
46h (1C8Dh)	**REG1C8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WP_FONT4BP_BASADR[11:8]	3:0	Please see description of '1C8Ch'.	
47h (1C8Eh)	**REG1C8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	WP_FONT8BP_BASADR[7:0]	7:0	OSD write path 8bp font base-address.	
47h (1C8Fh)	**REG1C8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WP_FONT8BP_BASADR[11:8]	3:0	Please see description of '1C8Eh'.	
48h (1C90h)	**REG1C90**	**7:0**	**Default : 0x00**	**Access : R/W**
	RP_CODE_BASADR[7:0]	7:0	OSD read path code base-address.	
48h (1C91h)	**REG1C91**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:4	Reserved.	
	RP_CODE_BASADR[11:8]	3:0	Please see description of '1C90h'.	
49h (1C92h)	**REG1C92**	**7:0**	**Default : 0x00**	**Access : R/W**
	RP_ATTRI0_BASADR[7:0]	7:0	OSD read path attribute0 base-address.	
49h (1C93h)	**REG1C93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RP_ATTRI0_BASADR[11:8]	3:0	Please see description of '1C92h'.	
4Ah	**REG1C94**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1C94h)	RP_ATTRI1_BASADR[7:0]	7:0	OSD read path attribute1 base-address.	
4Ah (1C95h)	**REG1C95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RP_ATTRI1_BASADR[11:8]	3:0	Please see description of '1C94h'.	
4Bh (1C96h)	**REG1C96**	**7:0**	**Default : 0x00**	**Access : R/W**
	RP_TEX_GRP_BASADR[7:0]	7:0	OSD read path texture group base-address.	
4Bh (1C97h)	**REG1C97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RP_TEX_GRP_BASADR[11:8]	3:0	Please see description of '1C96h'.	
4Ch (1C98h)	**REG1C98**	**7:0**	**Default : 0x00**	**Access : R/W**
	RP_FONT1BP_BASADR[7:0]	7:0	OSD read path 1bp font base-address.	
4Ch (1C99h)	**REG1C99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RP_FONT1BP_BASADR[11:8]	3:0	Please see description of '1C98h'.	
4Dh (1C9Ah)	**REG1C9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RP_FONT2BP_BASADR[7:0]	7:0	OSD read path 2bp font base-address.	
4Dh (1C9Bh)	**REG1C9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RP_FONT2BP_BASADR[11:8]	3:0	Please see description of '1C9Ah'.	
4Eh (1C9Ch)	**REG1C9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RP_FONT4BP_BASADR[7:0]	7:0	OSD read path 4bp font base-address.	
4Eh (1C9Dh)	**REG1C9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RP_FONT4BP_BASADR[11:8]	3:0	Please see description of '1C9Ch'.	
4Fh (1C9Eh)	**REG1C9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	RP_FONT8BP_BASADR[7:0]	7:0	OSD read path 8bp font base-address.	
4Fh (1C9Fh)	**REG1C9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RP_FONT8BP_BASADR[11:8]	3:0	Please see description of '1C9Eh'.	
60h (1CC0h)	**REG1CC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP0[7:0]	7:0	OSD texture group 0.	
60h (1CC1h)	**REG1CC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP0[15:8]	7:0	Please see description of '1CC0h'.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
61h (1CC2h)	**REG1CC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP1[7:0]	7:0	OSD texture group 1.	
61h (1CC3h)	**REG1CC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP1[15:8]	7:0	Please see description of '1CC2h'.	
62h (1CC4h)	**REG1CC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP2[7:0]	7:0	OSD texture group 2.	
62h (1CC5h)	**REG1CC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP2[15:8]	7:0	Please see description of '1CC4h'.	
63h (1CC6h)	**REG1CC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP3[7:0]	7:0	OSD texture group 3.	
63h (1CC7h)	**REG1CC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP3[15:8]	7:0	Please see description of '1CC6h'.	
64h (1CC8h)	**REG1CC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP4[7:0]	7:0	OSD texture group 4.	
64h (1CC9h)	**REG1CC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP4[15:8]	7:0	Please see description of '1CC8h'.	
65h (1CCAh)	**REG1CCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP5[7:0]	7:0	OSD texture group 5.	
65h (1CCBh)	**REG1CCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP5[15:8]	7:0	Please see description of '1CCAh'.	
66h (1CCCh)	**REG1CCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP6[7:0]	7:0	OSD texture group 6.	
66h (1CCDh)	**REG1CCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP6[15:8]	7:0	Please see description of '1CCCh'.	
67h (1CCEh)	**REG1CCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP7[7:0]	7:0	OSD texture group 7.	
67h (1CCFh)	**REG1CCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP7[15:8]	7:0	Please see description of '1CCEh'.	
68h (1CD0h)	**REG1CD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP8[7:0]	7:0	OSD texture group 8.	
68h (1CD1h)	**REG1CD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP8[15:8]	7:0	Please see description of '1CD0h'.	
69h	**REG1CD2**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1CD2h)	TOTAL_TEX_GRP9[7:0]	7:0	OSD texture group 9.	
69h (1CD3h)	**REG1CD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP9[15:8]	7:0	Please see description of '1CD2h'.	
6Ah (1CD4h)	**REG1CD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP10[7:0]	7:0	OSD texture group 10.	
6Ah (1CD5h)	**REG1CD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP10[15:8]	7:0	Please see description of '1CD4h'.	
6Bh (1CD6h)	**REG1CD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP11[7:0]	7:0	OSD texture group 11.	
6Bh (1CD7h)	**REG1CD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP11[15:8]	7:0	Please see description of '1CD6h'.	
6Ch (1CD8h)	**REG1CD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP12[7:0]	7:0	OSD texture group 12.	
6Ch (1CD9h)	**REG1CD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP12[15:8]	7:0	Please see description of '1CD8h'.	
6Dh (1CDAh)	**REG1CDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP13[7:0]	7:0	OSD texture group 13.	
6Dh (1CDBh)	**REG1CDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP13[15:8]	7:0	Please see description of '1CDAh'.	
6Eh (1CDCh)	**REG1CDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP14[7:0]	7:0	OSD texture group 14.	
6Eh (1CDDh)	**REG1CDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP14[15:8]	7:0	Please see description of '1CDCh'.	
6Fh (1CDEh)	**REG1CDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP15[7:0]	7:0	OSD texture group 15.	
6Fh (1CDFh)	**REG1CDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOTAL_TEX_GRP15[15:8]	7:0	Please see description of '1CDEh'.	
70h (1CE0h)	**REG1CE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEX32	7	Texture 32 enable.	
	TEX_EN	6	OSD read path texture and font share the same request.	
	FRAME_START_SEL	5	Select frame start signal source. 0: By HW. 1: By SW.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FRAME_START	4	Generate frame start signal by SW.	
	DRAM_BUS	3	Dram bus width. 0: Means dram bus width is 16 bits. 1: No-use.	
	DRAM_4BA	2	Dram bank bits. 0: Means DRAM has 1 bits banks. 1: Means 2 bits banks.	
	DRAM_9COL	1	DRAM column bits. 0: Means dram has 8 bits columns. 1: Means 9 bits columns.	
	DRAM_10COL	0	DRAM column bits. 1: 10-bit columns.	
70h (1CE1h)	**REG1CE1**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	FWRESETZ_RP	5	OSD read path SW reset.	
	FWRESETZ_WP	4	OSD write path SW reset.	
	OSD_SEL[1:0]	3:2	OSD select. 00: OSD port0 select OSD2, OSD port1 select OSD1. 01: OSD port0 select OSD1, OSD port1 select OSD1. 10: OSD port0 select OSD2, OSD port1 select OSD2. 11: OSD port0 select OSD1, OSD port1 select OSD2.	
	OSD_RP_PRI	1	1 means OSD2MI_RRDY has higher priority.	
	-	0	Reserved.	
71h (1CE2h)	**REG1CE2**	**7:0**	**Default : -**	**Access : RO**
	BIST_FAIL_TEX_SRAM_32X64_1	7	Texture SRAM32x64_1 BIST fail status.	
	BIST_FAIL_TEX_SRAM_32X64_0	6	Texture SRAM32x64_0 BIST fail status.	
	BIST_FAIL_ATRI0_SRAM_24X128_1	5	Attribute0 SRAM24x128_1 BIST fail status.	
	BIST_FAIL_ATRI0_SRAM_24X128_0	4	Attribute0 SRAM24x128_0 BIST fail status.	
	BIST_FAIL_FONT_SRAM_96X128_1	3	Font SRAM96x128_1 BIST fail status.	
	BIST_FAIL_FONT_SRAM_96X128_0	2	Font SRAM96x128_0 BIST fail status.	
	BIST_FAIL_CODE_SRAM_24X64_1	1	Code SRAM24x64_1 BIST fail status.	
	BIST_FAIL_CODE_SRAM_24X64_0	0	Code SRAM24x64_0 BIST fail status.	
71h (1CE3h)	**REG1CE3**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.	
	BIST_FAIL_CPRAM	4	CPRAM BIST fail status.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BIST_FAIL_FP_SRAM_96X8_1	3	FP SRAM96x8_1 BIST fail status.	
	BIST_FAIL_FP_SRAM_96X8_0	2	FP SRAM96x8_0 BIST fail status.	
	BIST_FAIL_SC_SRAM_96X16_1	1	SC SRAM96x16_1 BIST fail status.	
	BIST_FAIL_SC_SRAM_96X16_0	0	SC SRAM96x16_0 BIST fail status.	
72h (1CE4h)	**REG1CE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD1_HWCSR_EN	7	1: Hardware cursor to show on OSD1.	
	OSD2_HWCSR_EN	6	1: Hardware cursor to show on OSD2.	
	BW_IMPROVE	5	1: OSD read path has more bandwidth tolerance.	
	OSD2MI_WPTY	4	1: OSD2MI_WRDY has higher priority.	
	HWCSR_LASTLINE	3	Set as "0" if HWCSR_Y_POS = 0; else, set as "1".	
	SHRINK MODE_AREA_A	1:0	00: Shrink_LEFT_MODE for area A. 01: Shrink_RIGHT_MODE for area A. 10: Reserved. 11: Shrink_MID mode for area A.	
	-	0	Reserved.	
72h (1CE5h)	**REG1CE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OOFFS[7]	3	Please see description of '1C12h'.	
	GOP_PAL_SEL	2	0: Use OSD1 palette SRAM. 1: Use GOP palette SRAM.	
	OSD_8BP_PAL_SEL	1	OSD 8bp palette select. 0: Use OSD1 palette. 1: Use OSD2 palette.	
	-	0	Reserved.	
73h (1CE6h)	**REG1CE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_MIR_EN	7	OSD mirror enable. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	-	5	Reserved.	
	PAL_DMA_EN	4	Palette DMA mode enable. 0: Disable. 1: Enable.	
	CA8K_MODE_EN	3	Code/attribute 8k mode enable. 0: Disable.	

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Enable.	
	SHRINK_MIX_EN	2	Shrink mix mode enable. 0: Disable. 1: Enable.	
	SHRINK MODE_AREA_B	1:0	00: Shrink_LEFT_MODE for area B. 01: Shrink_RIGHT_MODE for area B. 10: Reserved. 11: Shrink_MID mode for area B.	
73h (1CE7h)	**REG1CE7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	-	6:4	Reserved.	
	OSD_OUT_PORT_SEL[3]	3	0: OSD2 output port select OSD1. 1: OSD2 output port select OSD2.	
	OSD_OUT_PORT_SEL[2]	2	0: OSD1 output port select OSD1. 1: OSD1 output port select OSD2.	
	-	1	Reserved.	
	-	0	Reserved.	
78h (1CF0h)	**REG1CF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	HWCSR_V_DUP	7:6	Vertical size up. 00: x1. 01: x2. 10: x3. 11: x4.	
	HWCSR_H_DUP	5:4	Horizontal size up. 00: x1. 01: x2. 10: x3. 11: x4.	
	HC_PRI	3	1: HC2MI_RRDY to has higher priority.	
	HWCSR_BIT	2	Hardware cursor. 0: 2bp. 1: 4bp.	
	HWCSR_SIZE	1	Hardware cursor size. 0: 32x32. 1: 64x64.	
	HWCSR_EN	0	Hardware cursor enable.	
78h	**REG1CF1**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD Register (Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1CF1h)	-	7:6	Reserved.	
	HWCSR_COLOR_OFST[5:0]	5:0	HWCSR_COLOR_OFFSET, for 2bp case, the 8bp HWCSR is HWCSR_COLOR_OFFSET[5:0], HWCSR_BIT[1:0], for 4bp case, the 8bp HWCSR is HWCSR_COLOR_OFFSET[5:2], HWCSR_BIT[3:0].	
79h (1CF2h)	**REG1CF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	HWCSR_HST[7:0]	7:0	Hardware cursor horizontal start position.	
79h (1CF3h)	**REG1CF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HWCSR_HST[11:8]	3:0	Please see description of '1CF2h'.	
7Ah (1CF4h)	**REG1CF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HWCSR_VST[7:0]	7:0	Hardware cursor vertical start position.	
7Ah (1CF5h)	**REG1CF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HWCSR_VST[11:8]	3:0	Please see description of '1CF4h'.	
7Bh (1CF6h)	**REG1CF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	HWCSR_BASADR[7:0]	7:0	The base-address for reading out the hardware cursor.	
7Bh (1CF7h)	**REG1CF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	HWCSR_BASADR[15:8]	7:0	Please see description of '1CF6h'.	

CHIPTOP Register (Bank = 1E)

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (1E00h)	**REG1E00**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHIP_CONFIG_OVERWRITE[7:0]	7:0	Chip configuration overwrite. [0]: SEL_SBUS_OVEN. [1]: SEL_SBUS_OV. [2]: SEL_DBUS_OVEN. [3]: SEL_DBUS_OV. Others: Reserved.	
00h (1E01h)	**REG1E01**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHIP_CONFIG_OVERWRITE[15:8]	7:0	See description of '1E00h'.	
01h (1E02h)	**REG1E02**	**7:0**	**Default : 0x00**	**Access : R/W**
	UTMI_MODE	7	Enable power down crystal (REV_C ECO) for test machine.	
	-	6:1	Reserved.	
	FORCE_MODPAD	0	Force all MOD pads controlled by PAD_TOP, mainly for test mode.	
01h (1E03h)	**REG1E03**	**7:0**	**Default : 0x00**	**Access : R/W**
	SBSETL	7	Series bus pads set low.	
	SBSETH	6	Series bus pads set high.	
	SETL	5	Digital pads set low.	
	SETH	4	Digital pads set high.	
	-	3	Reserved.	
	UART_RX_ENABLE	2	1: Enable UART0 RX. 0: Disable UART0 RX.	
	-	1:0	Reserved.	
02h (1E04h)	**REG1E04**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_OUT_MODE[1:0]	7:6	PAD_SAR[3:0] control. [0]: 0: Controlled by PAD_TOP. 1: Controlled by SAR_TOP. [1]: Reserved.	
	OSC_MODE[1:0]	5:4	Delay chain mode. 0: Low IR drop. 1: Whole chip. 2: High IR drop. 3: Audio DSP.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CARD_MS[1:0]	3:0	Reserved.	
02h (1E05h)	**REG1E05**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:6	Reserved.	
	GP_DDCR_CK_IN	5	C read back when PAD_DDCROM_CLK is used as GPIO.	
	GP_DDCR_DA_IN	4	C read back when PAD_DDCROM_DAT is used as GPIO.	
	GP_DDCR_CK_OEN	3	OEN control when PAD_DDCROM_CLK is used as GPIO.	
	GP_DDCR_CK_OUT	2	I control when PAD_DDCROM_CLK is used as GPIO.	
	GP_DDCR_DA_OEN	1	OEN control when PAD_DDCROM_DAT is used as GPIO.	
	GP_DDCR_DA_OUT	0	I control when PAD_DDCROM_DAT is used as GPIO.	
03h (1E06h)	**REG1E06**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOTPLUG	7	REV_D ECO (enable dbus pad switch to TEST_OUT).	
	TCOM	6	0: Disable. 1: Specify PAD_GPIOB as TCON function.	
	SPI_PAD[5:0]	5:0	SPI pads control registers. PAD_SPI_CK/ C0: SPI_PAD[0]. PAD_SPI_CK/ C1: SPI_PAD[1]. PAD_SPI_CZ / C0: SPI_PAD[2]. PAD_SPI_CZ / C1: SPI_PAD[3]. PAD_SPI_DI / C0: SPI_PAD[4]. PAD_SPI_DI / C1: SPI_PAD[5].	
03h (1E07h)	**REG1E07**	**7:0**	**Default : 0xF0**	**Access : R/W**
	PWM_OEN[3:0]	7:4	Output Enable Bar of PWM pads. Should be set to input when initialized to capture CHIP_CONFIG while reset.	
	-	3:2	Reserved.	
	DDCROM_GPIO	1	0: Disable. 1: Specify PAD_DDCROM_XX as GPIO function.	
	DDCROM_EN	0	0: Disable. 1: Specify PAD_DDCROM_XX as DDCROM function.	
04h (1E09h)	**REG1E09**	**7:0**	**Default : 0x00**	**Access : R/W**
	IIC_MST[3:0]	7:4	Specify 2 pads as IIC master function. 0: Disable. Others: See GPIO table.	
	GPIO_8051[1:0]	3:2	Specify 4 pads as GPIO_8051 function. 0: Disable. 1: PAD_SAR[3:0].	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2: PAD_PWM[1:0] + PAD_DDCROM*. 3: PAD_GPIOM[3:0].	
	GPIO_AU[1:0]	1:0	Specify 4 pads as GPIO_AUDIO function. 0: Disable. 1: PAD_GPIOD[3:0]. 2: PAD_ICLK + PAD_DI[2:0]. 3: PAD_DI[7:4].	
05h (1E0Ah)	**REG1E0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	BT656_OUT[2:0]	6:4	Specify 8 pads as BT656 out function. 0: Disable. Others: See GPIO table.	
	BT656_10BIT	3	Specify 2 pads as BT656[9:8] function (for testing purpose). 0: Disable. 1: PAD_LHSYNC for BT656[8]. PAD_LVSYNC for BT656[9].	
	BT656_IN[2:0]	2:0	Specify 8 pads as BT656[7:0] function. 0: Disable. Others: See GPIO table.	
05h (1E0Bh)	**REG1E0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	UART1[2:0]	6:4	Specify 2 pads as UART1 function. 0: Disable. Others: See GPIO table.	
	UART0[3:0]	3:0	Specify 2 pads as UART0 function. 0: Disable. Others: See GPIO table.	
06h (1E0Ch)	**REG1E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	I2S_OUT1[3:0]	7:4	Specify 4 pads as I2S out1 function. 0: Disable. Others: See GPIO table.	
	I2S_IN[3:0]	3:0	Specify 3 pads as I2S in function. 0: Disable. Others: See GPIO table.	
06h (1E0Dh)	**REG1E0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	4	Reserved.	
	I2S_MUTE[3:0]	3:0	Specify 1 pad as I2S mute function. 0: Disable. Others: See GPIO table.	
07h (1E0Eh)	**REG1E0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_A	7	0: Disable. 1: Specify PAD_ICLK + PAD_DI[7:0] as GPIOA.	
	-	6:4	Reserved.	
	HDMI_CEC[3:0]	3:0	Specify 1 pad as HDMI_CEC function. 0: Disable. Others: See GPIO table.	
07h (1E0Fh)	**REG1E0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_T[1:0]	7:6	0: Disable. 1: Specify PAD_GPIOT[3:0] as GPIOT.	
	GPIO_R	5	0: Disable. 1: Specify PAD_GPIOR[10:0] as GPIOR.	
	GPIO_M	4	Dbus pads set low (REV_C ECO).	
	GPIO_L	3	0: Disable. 1: Specify PAD_GPIOL[4:0] as GPIOL.	
	GPIO_H	2	Dbus pads set high (REV_C ECO).	
	GPIO_D	1	0: Disable. 1: Specify PAD_GPIOD[18:0] as GPIOD.	
	GPIO_B	0	0: Disable. 1: Specify PAD_GPIOB[13:0] as GPIOB.	
08h (1E10h)	**REG1E10**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOA_OUT[7:0]	7:0	I control when specifying PAD_ICLK + PAD_DI[7:0] as GPIOA.	
08h (1E11h)	**REG1E11**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOL_OUT[4:0]	7:3	I control when specifying PAD_GPIOL[4:0] as GPIOL.	
	GPIOA_OUT[10:8]	2:0	See description of '1E10h'.	
09h (1E12h)	**REG1E12**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOA_OEN[7:0]	7:0	OEN control when specifying PAD_ICLK + PAD_DI[7:0] as GPIOA.	
09h (1E13h)	**REG1E13**	**7:0**	**Default : 0xF8**	**Access : R/W**
	GPIOL_OEN[4:0]	7:3	OEN control when specifying PAD_GPIOL[4:0] as GPIOL.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPIOA_OEN[10:8]	2:0	See description of '1E12h'.	
0Ah (1E14h)	**REG1E14**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOB_OUT[7:0]	7:0	I control when specifying PAD_GPIOB[15:0] as GPIOB.	
0Ah (1E15h)	**REG1E15**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOB_OUT[15:8]	7:0	See description of '1E14h'.	
0Bh (1E16h)	**REG1E16**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIOB_OEN[7:0]	7:0	OEN control when specifying PAD_GPIOB[15:0] as GPIOB.	
0Bh (1E17h)	**REG1E17**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIOB_OEN[15:8]	7:0	See description of '1E16h'.	
0Ch (1E18h)	**REG1E18**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOD_OUT[7:0]	7:0	I control when specifying PAD_GPIOD[18:0] as GPIOD.	
0Ch (1E19h)	**REG1E19**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOD_OUT[15:8]	7:0	See description of '1E18h'.	
0Dh (1E1Ah)	**REG1E1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOM_OUT[3:0]	7:4	I control when specifying PAD_GPIOM[3:0] as GPIOM.	
	-	3	Reserved.	
	GPIOD_OUT[18:16]	2:0	See description of '1E18h'.	
0Dh (1E1Bh)	**REG1E1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPIOT_OUT[3:0]	3:0	I control when specifying PAD_GPIOT[3:0] as GPIOT.	
0Eh (1E1Ch)	**REG1E1C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIOD_OEN[7:0]	7:0	OEN control when specifying PAD_GPIOD[18:0] as GPIOD.	
0Eh (1E1Dh)	**REG1E1D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIOD_OEN[15:8]	7:0	See description of '1E1Ch'.	
0Fh (1E1Eh)	**REG1E1E**	**7:0**	**Default : 0xF7**	**Access : R/W**
	GPIOM_OEN[3:0]	7:4	OEN control when specifying PAD_GPIOM[3:0] as GPIOM.	
	-	3	Reserved.	
	GPIOD_OEN[18:16]	2:0	See description of '1E1Ch'.	
0Fh (1E1Fh)	**REG1E1F**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	GPIOT_OEN[3:0]	3:0	OEN control when specifying PAD_GPIOT[3:0] as GPIOT.	
10h	**REG1E20**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
(1E20h)	-	7:3	Reserved.
	MCU_QUICK_RST	2	0: Normal. 1: MCU quick reset.
	MCU_RESET	1	1: MCU reset by s/w.
	POFF_RST_EN	0	1: Power off reset enable.
11h (1E22h)	**REG1E22**	**7:0**	**Default : 0x00** **Access : R/W**
	STC0_CW_SEL	7	Select STC0 control word from: 0: Register controlled by House Keeping MCU. 1: Reserved.
	-	6	Reserved.
	STC0SYN_RST	5	STC0 synthesizer software reset, active high.
	USBSYN_RST	4	USB synthesizer software reset, active high.
	DE_ONLY_F2	3	DE only mode for SC_TOP main window.
	DE_ONLY_F1	2	DE only mode for SC_TOP PIP window.
	CLK_VD_SEL	1	Select VD clock from ADC1 or ADC2. 0: Select VD_ADC_CLK. 1: Select ADC_CLK.
	SW_MCU_CLK	0	MCU clock setting. 0: DFT_LIVE. 1: Select the output according to CKG_MCU.
11h (1E23h)	**REG1E23**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7	Reserved.
	UPDATE_DC0_SYNC_CW	6	Update the control words of DC0 synthesizer, that is, synchronize to STC0.
	-	5:4	Reserved.
	UPDATE_DC0_FREERUN_CW	3	Update the control words of DC0 free-running synthesizer.
	-	2	Reserved.
	UPDATE_STC0_CW	1	Update the control word of STC0 synthesizer.
	-	0	Reserved.
12h (1E24h)	**REG1E24**	**7:0**	**Default : 0x01** **Access : R/W**
	CKG_RIU[3:0]	7:4	[0]: Select CLK_VD_P from 8*fsc or VIF_43M. 0: CLK_VD_P from 8*fsc. 1: CLK_VD_P from VIF_43M. [1]: CLK_VIF selection for CLK_DAC. 0: Select 43m.

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Select 86m. 0: From SBM_SDA_OUT (open drain). 1: From SBM_SDA_OEZ. [3]: DI clock selection (CCIR656 in). 0: From CLK_IDCLK_F2 (main window). 1: From CLK_IDCLK_F1 (sub window).	
	-	3:2	Reserved.	
	CKG_USB30[1:0]	1:0	CLK_UHC clock setting. [0]: Disable clock. [1]: Invert clock.	
12h (1E25h)	**REG1E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_MIU[3:0]	7:4	CLK_MIU clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 200MHz (MEMPLL out). 01: 170MHz. 10: 216MHz (REV_D ECO). 11: 100MHz (MEMPLL divided by 2).	
	CKG_DDR[3:0]	3:0	CLK_MIU2 clock setting. [0]: Disable clock. [1]: Invert clock. Selection of test clock out for OSD line buffer. [2]: 0: Select CLK_FT0LB. 1: Select CLK_FT1LB. [3]: 0: Select CLK_CA0LB. 1: Select CLK_CA1LB.	
13h (1E26h)	**REG1E26**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_AEON[1:0]	7:6	CLK_OSDLB_P clock setting. 00: From ODCLK. 01: From IDCLK1 with gating. 10: From IDCLK2 with gating. 11: Reserved.	
	CKG_TCK[1:0]	5:4	CLK_TCK clock setting. [0]: Disable clock. [1]: Invert clock.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CKG_TS0[3:0]	3:0	CLK_MINI clock setting. [0]: Disable clock. [1]: Invert clock. [2]: Select clock source. 1: From CLK_DFT. 0: From CLK_MINI_BUF. CLK_MIU2 clock setting. [3]: Force from CLK_DFT.	
13h (1E27h)	**REG1E27**	**7:0**	**Default : 0x01**	**Access : R/W**
	CKG_STC0[3:0]	7:4	CLK_MCP clock setting. [3]: 1: From CLK_DFT. 0: From CLK_MCP_P. CLK_USB clock setting. [2]: Select clock source. 1: From CLK_DFT. 0: From CLK_USB_BUF. [1]: Invert clock. [0]: Disable clock.	
	CKG_TSP[3:0]	3:0	CLK_FT0LB, CLK_FT1LB, CLK_CA0LB, CLK_CA1LB clock setting. [3]: 1: From CLK_DFT. 0: From CLK_XXX_P. CLK_MLOAD clock setting. [2]: Select clock source. 1: From CLK_DFT. 0: From CLK_MLOAD_P. [1]: Invert clock. [0]: Disable clock.	
14h (1E28h)	**REG1E28**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_MAD_STC[3:0]	7:4	CLK_CA0LB clock setting. [0]: Disable clock. [1]: Invert clock. CLK_CA1LB clock setting. [2]: Disable clock. [3]: Invert clock.	
	-	3:0	Reserved.	
14h	**REG1E29**	**7:0**	**Default : 0x18**	**Access : R/W**

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1E29h)	CKG_MVD[3:0]	7:4	CLK_MCU_MAIL0/CLK_MCU_MAIL1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. For CLK_MCU_MAIL0: 00: From CLK_HKMCU_P. 01: From CLK_VDMCU_P. For CLK_MCU_MAIL1: 00: From CLK_VDMCU_P. 01: From CLK_HKMCU_P. 10: Reserved. 11: From CLK_DFT.	
	CKG_MVD_BOOT[3:0]	3:0	Reserved.	
15h (1E2Ah)	**REG1E2A**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_DC0[3:0]	7:4	CLK_FT0LB clock setting. [0]: Disable clock. [1]: Invert clock. CLK_FT1LB clock setting. [2]: Disable clock. [3]: Invert clock.	
	CKG_M4V[3:0]	3:0	CLK_MCP clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 200MHz (MEMPLL out). 01: 170MHz. 10: 123MHz. 11: 100MHz (MEMPLL divided by 2).	
15h (1E2Bh)	**REG1E2B**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_GE[3:0]	7:4	CLK_OSD2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: IDCLK. 01: ODCLK1 with gating. 10: ODCLK2 with gating. 11: CLK_DFT.	
	-	3:0	Reserved.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (1E2Ch)	**REG1E2C**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_GOPG1[3:0]	7:4	CLK_CA0LB2 clock setting. [0]: Disable clock. [1]: Invert clock. CLK_CA1LB2 clock setting. [2]: Disable clock. [3]: Invert clock.	
	CKG_GOPG0[3:0]	3:0	CLK_FT0LB2 clock setting. [0]: Disable clock. [1]: Invert clock. CLK_FT1LB2 clock setting. [2]: Disable clock. [3]: Invert clock.	
16h (1E2Dh)	**REG1E2D**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_VD[3:0]	7:4	CLK_VD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] 00: CLK_VD_P. 01: CLK_VIF_43M. 10: Test clock in. 11: CLK_DFT.	
	CKG_GOPD[3:0]	3:0	CLK_MIU clock setting. [3]: 1 => from CLK_DFT. 0 => from CLK_MIU_P. CLK_FT0LB2, CLK_FT1LB2, CLK_CA0LB2, CLK_CA1LB2 clock source setting. [2]: 1=> from CLK_DFT. 0 =>from CLK_XXX_P. CLK_OSDLB2_P clock source. [1:0] 00: From odclk. 01: From idclk1 with gating. 10: From idclk2 with gating. 11: Reserved.	
17h (1E2Eh)	**REG1E2E**	**7:0**	**Default : 0x21**	**Access : R/W**
	CKG_VD200[2:0]	7:5	CLK_VD200 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source.	

CHIPTOP Register (Bank = 1E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			00: 216MHz. 01: 216MHz. 10: 216MHz. 11: Select XTAL.
	CKG_VDMCU[4:0]	4:0	Reserved.
17h (1E2Fh)	**REG1E2F**	**7:0**	**Default : 0x12** **Access : R/W**
	-	7	Reserved.
	CKG_DHC[5:0]	6:1	CLK_DHC clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: 12MHz. 0001: 54MHz. 0010: 62MHz. 0011: 72MHz. 0100: 86MHz. 0101: 108MHz. 0110: 0. 0111: 0. 1xxx: XTAL.
	CKG_VD200[3]	0	See description of '1E2Eh'.
18h (1E30h)	**REG1E30**	**7:0**	**Default : 0x10** **Access : R/W**
	CKG_FICLK_F2[3:0]	7:4	CLK_FICKL_F2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select CLK_IDCLK2. 01: Select CLK_FCLK. 10: 0. 11: Select XTAL.
	CKG_FICLK_F1[3:0]	3:0	CLK_FICKL_F1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 2b'00: Select CLK_IDCLK1. 01: Select CLK_FCLK. 10: 0. 11: Select XTAL.

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
18h (1E31h)	**REG1E31**	**7:0**	**Default : 0x10**	**Access : R/W**
	CKG_PCM[3:0]	7:4	CLK_PCM clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: 27MHz. 01: 27MHz. 10: XTAL. 11: XTAL.	
	-	3:0	Reserved.	
19h (1E33h)	**REG1E33**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_VIF0[3:0]	7:4	CLK_VIF_43M clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select 43MHz. 01: Select 43MHz. 10: Select 43MHz. 11: Select XTAL.	
	CKG_VIF1[3:0]	3:0	CLK_VIF_86M clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select 86MHz. 01: Select 86MHz. 10: Select 86MHz. 11: Select XTAL.	
1Ah (1E34h)	**REG1E34**	**7:0**	**Default : 0x01**	**Access : R/W**
	CKG_SDR[3:0]	7:4	Reserved.	
	CKG_DAC[3:0]	3:0	CLK_DAC clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: Select ODCLK. 01: Select CLK_VIF_43M. 10: Select CLK_VD. 11: Select XTAL.	
1Ah	**REG1E35**	**7:0**	**Default : 0x01**	**Access : R/W**

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1E35h)	-	7:6	Reserved.	
	CKG_FCLK[5:0]	5:0	CLK_FCLK clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select FIX_CLK from MPLL. 0001: Select CLK_MIU. 0010: Select CLK_ODCLK. 0011: Select 216MHz. 0100: Select CLK_IDCLK2. 0101: Select 200MHz. 0110: 0. 0111: Select XTAL. 1xxx: Select XTAL.	
1Bh (1E36h)	**REG1E36**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_FMCLK[5:0]	5:0	CLK_FMCLK clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select CLK_MIU. 0001: Select FIX_CLK from MPLL. 0010: Select CLK_ODCLK. 0011: 0. 0100: Select CLK_IDCLK2. 0101: 0. 0110: 0. 0111: 0. 1xxx: Select DFT_LIVE.	
1Bh (1E37h)	**REG1E37**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_ODCLK[5:0]	5:0	CLK_ODCLK clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select CLK_ADC. 0001: Select CLK_DVI. 0010: Select CLK_VD. 0011: 1.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0100: 1. 0101: Select external DI clock. 0110: Select CLK_VD_ADC. 0111: Select CLK_LPLL_BUF. 1xxxx: Select XTAL.	
1Ch (1E38h)	**REG1E38**	**7:0**	**Default : 0x0D**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_JPD[5:0]	5:0	CLK_JPD clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: Select clock source. 000: Select CLK_MPLL_DIV. 001: Select 160MHz. 010: Select 144MHz. 011: Select 123MHz. 100: Select 108MHz. 101: MEMPLL_CLK_BUF. 110: MEMPLL_CLK_BUF_DIV2. 111: Select 86MHz. [5]: Reserved.	
1Ch (1E39h)	**REG1E39**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7	Reserved.	
	CKG_FCIE[6:0]	6:0	CLK_FCIE clock setting. [0]: Disable clock. [1]: Invert clock. [6:2]: Select clock source. 00000: CLK86_DIV256. 00001: CLK86_DIV64. 00010: CLK86_DIV16. 00011: CLK54_DIV4. 00100: CLK72_DIV4. 00101: CLK86_DIV4. 00110: CLK54_DIV2. 00111: CLK72_DIV2. 01000: CLK86_DIV2. 01001: 54MHz. 01010: 72MHz. 01011: 0. 01100: 0.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			01101: 0. 01110: 0. 01111: 0. 1xxxx: Select XTAL.	
1Fh (1E3Eh)	**REG1E3E**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_IDCLK1[5:0]	5:0	CLK_IDCLK_F1 clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select CLK_ADC. 0001: Select CLK_DVI. 0010: Select CLK_VD. 0011: Select CLK_ODCLK. 0100: 1. 0101: Select external DI clock. 0110: Select CLK_VD_ADC. 0111: 0. 1xxx: Select XTAL.	
1Fh (1E3Fh)	**REG1E3F**	**7:0**	**Default : 0x21**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_IDCLK2[5:0]	5:0	CLK_IDCLK_F2 clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: Select clock source. 0000: Select CLK_ADC. 0001: Select CLK_DVI. 0010: Select CLK_VD. 0011: Select CLK_ODCLK. 0100: 1. 0101: Select external DI clock. 0110: Select CLK_VD_ADC. 0111: 0. 1xxx: Select XTAL.	
20h (1E40h)	**REG1E40**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_NUM[7:0]	7:0	Numerator of the synthesizer of DC0.	
20h (1E41h)	**REG1E41**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_NUM[15:8]	7:0	See description of '1E40h'.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (1E42h)	**REG1E42**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_DEN[7:0]	7:0	Denominator of the synthesizer of DC0.	
21h (1E43h)	**REG1E43**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_DEN[15:8]	7:0	See description of '1E42h'.	
22h (1E44h)	**REG1E44**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_STRLD[3:0]	3:0	CLK_OSD clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: Select clock source. 00: IDCLK. 01: ODCLK1 with gating. 10: ODCLK2 with gating. 11: CLK_DFT.	
22h (1E45h)	**REG1E45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CKG_MCU[4:0]	4:0	CLK_MCU clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: 000: 170MHz. 001: 160MHz. 010: 144MHz. 011: 123MHz. 100: 108MHz. 101: MEM_CLOCK. 110: MEM_CLOCK divided by 2. 111: XTAL divided by 128.	
24h (1E48h)	**REG1E48**	**7:0**	**Default : 0x00**	**Access : R/W**
	USBSYN_CW[7:0]	7:0	Control word of the synthesizer for USB PHY.	
24h (1E49h)	**REG1E49**	**7:0**	**Default : 0x00**	**Access : R/W**
	USBSYN_CW[15:8]	7:0	See description of '1E48h'.	
25h (1E4Ah)	**REG1E4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	USBSYN_CW[23:16]	7:0	See description of '1E48h'.	
25h (1E4Bh)	**REG1E4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	USBSYN_CW[31:24]	7:0	See description of '1E48h'.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
26h (1E4Ch)	**REG1E4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC0SYN_CW[7:0]	7:0	Control word of the synthesizer of STC0 clocks.	
26h (1E4Dh)	**REG1E4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC0SYN_CW[15:8]	7:0	See description of '1E4Ch'.	
27h (1E4Eh)	**REG1E4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC0SYN_CW[23:16]	7:0	See description of '1E4Ch'.	
27h (1E4Fh)	**REG1E4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	STC0SYN_CW[31:24]	7:0	See description of '1E4Ch'.	
2Ah (1E54h)	**REG1E54**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_FREERUN_CW[7:0]	7:0	Control word of the synthesizer of MPEG VOP0 clocks.	
2Ah (1E55h)	**REG1E55**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_FREERUN_CW[15:8]	7:0	See description of '1E54h'.	
2Bh (1E56h)	**REG1E56**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_FREERUN_CW[23:16]	7:0	See description of '1E54h'.	
2Bh (1E57h)	**REG1E57**	**7:0**	**Default : 0x00**	**Access : R/W**
	DC0_FREERUN_CW[31:24]	7:0	See description of '1E54h'.	
2Ch (1E58h)	**REG1E58**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:6	Reserved.	
	CKG_DHC_SYNTH[3:0]	5:2	CLK_DHC_SYNTH clock setting. [0]: Gate. [1]: Inverse. [3:2] = 00: MPLL_VCO_DIV2. [3:2] = 01: MPLL_VCO_DIV2P5. [3:2] = 10: MPLL_VCO_DIV3. [3:2] = 11: MPLL_VCO_DIV4.	
	CKG_DHC_DDR[1:0]	1:0	CLK_DHC_DDR clock setting. [0]: Gate. [1]: Inverse.	
2Ch (1E59h)	**REG1E59**	**7:0**	**Default : 0x21**	**Access : R/W**
	CKG_DHC_LIVE[1:0]	7:6	CLK_DHC_LIVE clock setting. [0]: Gate. [1]: Inverse.	
	CKG_DHC_MCU[5:0]	5:0	CLK_DHC_MCU clock setting. [0]: Gate. [1]: Inverse.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[5:2] = 1XXX: xtali. [5:2] = 0000: 43. [5:2] = 0001: 54. [5:2] = 0010: 62. [5:2] = 0011: 72. [5:2] = 0100: 86. [5:2] = 0101: 108. [5:2] = Others: Reserved.	
32h (1E64h)	**REG1E64**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_FT0LB2[3:0]	7:4		
	CKG_OSD2[3:0]	3:0		
32h (1E65h)	**REG1E65**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7	Reserved.	
	CKG_OSD2_SEL[2:0]	6:4		
	CKG_CA0LB2[3:0]	3:0		
36h (1E6Ch)	**REG1E6C**	**7:0**	**Default : 0x00**	**Access : RO**
	TSO_GPIO_IN[7:0]	7:0	Read back when dbus pads are used as GPIO. [3:0]: PAD_AD[3:0]_C. [4]: PAD_WRZ_C. [5]: PAD_RDZ_C. [6]: PAD_ALE_C. [10:7]: Reserved.	
36h (1E6Dh)	**REG1E6D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	TSO_GPIO_IN[10:8]	2:0	See description of '1E6Ch'.	
37h (1E6Eh)	**REG1E6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSO_GPIO_OUT[7:0]	7:0	[6:0]: OEN control when dbus pads are used as GPIO. [3:0]: PAD_AD[3:0]_OEN. [4]: PAD_WRZ_OEN. [5]: PAD_RDZ_OEN. [6]: PAD_ALE_OEN. [7]: Reserved. [8]: Reserved. [9]: Reserved. [10]: Reserved.	
37h (1E6Fh)	**REG1E6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TSO_GPIO_OUT[10:8]	2:0	See description of '1E6Eh'.	
38h (1E70h)	**REG1E70**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSO_GPIO_OEN[7:0]	7:0	PAD_GPIOD[1:0] control. [0]: PAD_GPIOD0 drive. [1]: PAD_GPIOD0 pull down. [2]: PAD_GPIOD0 pull high. [3]: PAD_GPIOD0 pull high PCI. [4]: PAD_GPIOD1 drive. [5]: PAD_GPIOD1 pull down. [6]: PAD_GPIOD1 pull high. [7]: PAD_GPIOD1 pull high PCI.	
38h (1E71h)	**REG1E71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TSO_GPIO_OEN[10:8]	2:0	See description of '1E70h'.	
39h (1E72h)	**REG1E72**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	TS1_GPIO_IN[3:0]	3:0	[0]: PAD_INT_C read back when PAD_INT is used as GPIO. [3:1]: Reserved.	
3Ah (1E74h)	**REG1E74**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TS1_GPIO_OUT[3:0]	3:0	[0]: OEN control when PAD_INT is used as GPIO. [1]: I control when PAD_INT is used as GPIO. [3:2]: Reserved.	
3Bh (1E76h)	**REG1E76**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TS1_GPIO_OEN[3:0]	3:0	PAD_GPIOD2 control. [0]: PAD_GPIOD2 drive. [1]: PAD_GPIOD2 pull down. [2]: PAD_GPIOD2 pull high. [3]: PAD_GPIOD2 pull high PCI.	
3Dh (1E7Ah)	**REG1E7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DI_GPIO_OUT[7:0]	7:0	[6:0]: I control when the following pads are used as GPIO. [3:0]: PAD_AD[3:0]_I. [4]: PAD_WRZ_I. [5]: PAD_RDZ_I. [6]: PAD_ALE_I.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[7]: Reserved. [8]: Reserved.	
3Dh (1E7Bh)	**REG1E7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DI_GPIO_OUT[8]	0	See description of '1E7Ah'.	
3Eh (1E7Ch)	**REG1E7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DI_GPIO_OEN[7:0]	7:0	PAD_GPIOD[4:3] control. [0]: PAD_GPIOD3 drive. [1]: PAD_GPIOD3 pull down. [2]: PAD_GPIOD3 pull high. [3]: PAD_GPIOD3 pull high PCI. [4]: PAD_GPIOD4 drive. [5]: PAD_GPIOD4 pull down. [6]: PAD_GPIOD4 pull high. [7]: PAD_GPIOD4 pull high PCI. [8]: Reserved.	
3Eh (1E7Dh)	**REG1E7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DI_GPIO_OEN[8]	0	See description of '1E7Ch'.	
3Fh (1E7Eh)	**REG1E7E**	**7:0**	**Default : 0x00**	**Access : RO**
	I2S_GPIO_IN[7:0]	7:0	[3:0]: PAD_SAR[3:0]_C read back when PAD_SAR[3:0] is used as GPIO. [7:4]: Reserved.	
3Fh (1E7Fh)	**REG1E7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	I2S_GPIO_IN[8]	0	See description of '1E7Eh'.	
40h (1E80h)	**REG1E80**	**7:0**	**Default : 0x00**	**Access : R/W**
	I2S_GPIO_OUT[7:0]	7:0	[3:0]: OEN control when PAD_SAR[3:0] is used as GPIO. [7:4]: I control when PAD_SAR[3:0] is used as GPIO. [8]: PAD_INT is used as GPIO (GPIOECO_1).	
40h (1E81h)	**REG1E81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	I2S_GPIO_OUT[8]	0	See description of '1E80h'.	
41h (1E82h)	**REG1E82**	**7:0**	**Default : 0x00**	**Access : R/W**
	I2S_GPIO_OEN[7:0]	7:0	PAD_GPIOD[6:5] control. [0]: PAD_GPIOD5 drive.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[1]: PAD_GPIOD5 pull down. [2]: PAD_GPIOD5 pull high. [3]: PAD_GPIOD5 pull high PCI. [4]: PAD_GPIOD6 drive. [5]: PAD_GPIOD6 pull down. [6]: PAD_GPIOD6 pull high. [7]: PAD_GPIOD6 pull high PCI. [8]: Reserved.	
41h (1E83h)	**REG1E83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	I2S_GPIO_OEN[8]	0	See description of '1E82h'.	
42h (1E84h)	**REG1E84**	**7:0**	**Default : 0x00**	**Access : RO**
	PCI_GPIO_IN[7:0]	7:0	[3:0] PAD_PWM[3:0]_C read back when PAD_PWM is used as GPIO. [8]: PAD_LCK_ODD_C read back when PAD_LCK_ODD is used as GPIO. [9]: PAD_LHSYNC_C read back when PAD_LHSYNC is used as GPIO. [10]: PAD_LVSYNC_C read back when PAD_LVSYNC is used as GPIO. [11] PAD_LDE_C read back when it is used as GPIO. Others: Reserved.	
42h (1E85h)	**REG1E85**	**7:0**	**Default : 0x00**	**Access : RO**
	PCI_GPIO_IN[15:8]	7:0	See description of '1E84h'.	
43h (1E86h)	**REG1E86**	**7:0**	**Default : 0x00**	**Access : RO**
	PCI_GPIO_IN[23:16]	7:0	See description of '1E84h'.	
43h (1E87h)	**REG1E87**	**7:0**	**Default : 0x00**	**Access : RO**
	PCI_GPIO_IN[31:24]	7:0	See description of '1E84h'.	
44h (1E88h)	**REG1E88**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	PCI_GPIO_IN[33:32]	1:0	See description of '1E84h'.	
45h (1E8Ah)	**REG1E8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCI_GPIO_OUT[7:0]	7:0	[3:0]: OEN control when PAD_PWM[3:0] is used as GPIO. [7:4]: I control when PAD_PWM[3:0] is used as GPIO. [10:8]: OEN control when {PAD_LVSYNC, PAD_LHSYNC, PAD_LCK_ODD} is used as GPIO. [11] PAD_LDE OEN control when used as GPIO.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[14:12]: I control when {PAD_LVSYNC, PAD_LHSYNC, PAD_LCK_ODD} is used as GPIO. [15] PAD_LDE I control when used as GPIO. Others: Reserved.	
45h (1E8Bh)	**REG1E8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCI_GPIO_OUT[15:8]	7:0	See description of '1E8Ah'.	
46h (1E8Ch)	**REG1E8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCI_GPIO_OUT[23:16]	7:0	See description of '1E8Ah'.	
46h (1E8Dh)	**REG1E8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCI_GPIO_OUT[31:24]	7:0	See description of '1E8Ah'.	
47h (1E8Eh)	**REG1E8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PCI_GPIO_OUT[33:32]	1:0	See description of '1E8Ah'.	
48h (1E90h)	**REG1E90**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCI_GPIO_OEN[7:0]	7:0	PAD_GPIOD7 control. [0]: PAD_GPIOD7 drive. [1]: PAD_GPIOD7 pull down. [2]: PAD_GPIOD7 pull high. [3]: PAD_GPIOD7 pull high PCI. PAD_AD0 control. [4]: PAD_AD0 drive. [5]: PAD_AD0 pull down. [6]: PAD_AD0 pull high. [7]: PAD_AD0 pull high PCI. PAD_AD1 control. [8]: PAD_AD1 drive. [9]: PAD_AD1 pull down. [10]: PAD_AD1 pull high. [11]: PAD_AD1 pull high PCI. PAD_AD2 control. [12]: PAD_AD2 drive. [13]: PAD_AD2 pull down. [14]: PAD_AD2 pull high. [15]: PAD_AD2 pull high PCI. [33:16]: Reserved.	
48h (1E91h)	**REG1E91**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCI_GPIO_OEN[15:8]	7:0	See description of '1E90h'.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
49h (1E92h)	**REG1E92**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCI_GPIO_OEN[23:16]	7:0	See description of '1E90h'.	
49h (1E93h)	**REG1E93**	**7:0**	**Default : 0xFC**	**Access : R/W**
	PCI_GPIO_OEN[31:24]	7:0	See description of '1E90h'.	
4Ah (1E94h)	**REG1E94**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	PCI_GPIO_OEN[33:32]	1:0	See description of '1E90h'.	
4Bh (1E96h)	**REG1E96**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	TCON_GPIO_OUT[3:0]	7:4	Reserved.	
	TCON_GPIO_IN[3:0]	3:0	[0]: Read back status of INT_PWRISNOGOOD. Others: Reserved.	
4Bh (1E97h)	**REG1E97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	TCON_GPIO_OEN[3:0]	3:0	Reserved.	
50h (1EA0h)	**REG1EA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	I2S_OUT2[3:0]	7:4	Specify 4 pads as I2S out2 function. 0: Disable. Others: See GPIO table.	
	SPDIF[3:0]	3:0	Specify 2 pads as SPDIF function. 0: Disable. Others: See GPIO table.	
50h (1EA1h)	**REG1EA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	USB2_DRVVBUS[3:0]	7:4	Specify 1 pad as USB 2.0 DRVVBUS function. 0: Disable. Others: See GPIO table.	
	USB1_DRVVBUS[3:0]	3:0	Specify 1 pad as USB 1.1 DRVVBUS function. 0: Disable. Others: See GPIO table.	
53h (1EA6h)	**REG1EA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DHC_RESET	2	DHC reset signal, active high.	
	-	1:0	Reserved.	
54h (1EA8h)	**REG1EA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DI_CLK_INV	5	DI_CLK invert.	
	SEL_DI_DDR	4	DIN DDR select. 0: Select SDR signals. 1: Select DDR signals.	
	DI_CLK_SEL[3:0]	3:0	DI_CLK delay level selection.	
54h (1EA9h)	**REG1EA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DO_CLK_INV	5	DOUT_CLK invert.	
	DOUT_SRC_SEL	4	DOUT DDR select. 0: Select SDR signals. 1: Select DDR signals.	
	DO_CLK_SEL[3:0]	3:0	DOUT_CLK delay level selection.	
56h (1EACh)	**REG1EAC**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIOA_IN[7:0]	7:0	Read back of GPIOA_C.	
56h (1EADh)	**REG1EAD**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIOL_IN[4:0]	7:3	Read back of GPIOL_C.	
	GPIOA_IN[10:8]	2:0	See description of '1EACh'.	
57h (1EAEh)	**REG1EAE**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIOB_IN[7:0]	7:0	Read back of GPIOB_C.	
57h (1EAFh)	**REG1EAF**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIOB_IN[15:8]	7:0	See description of '1EAEh'.	
58h (1EB0h)	**REG1EB0**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIOD_IN[7:0]	7:0	Read back of GPIOD_C.	
58h (1EB1h)	**REG1EB1**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIOD_IN[15:8]	7:0	See description of '1EB0h'.	
59h (1EB2h)	**REG1EB2**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIOM_IN[3:0]	7:4	Read back of GPIOM_C.	
	-	3	Reserved.	
	GPIOD_IN[18:16]	2:0	See description of '1EB0h'.	
59h (1EB3h)	**REG1EB3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	GPIOT_IN[3:0]	3:0	Read back of GPIOT_C.	
5Ah (1EB4h)	**REG1EB4**	**7:0**	**Default : 0x00**	**Access : RO**
	GPIOR_IN[7:0]	7:0	Read back of GPIOR_C.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Ah (1EB5h)	**REG1EB5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	GPIOR_IN[10:8]	2:0	See description of '1EB4h'.	
62h (1EC4h)	**REG1EC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDD2LOW_CTRL[7:0]	7:0	VDD2LOW_CTRL. [5:0]: Power off period selection. 0: Power off with 2.2us. 1: Power off with 4.4us. 2: Power off with 9.0us. 3: Power off with 17.9us. 4: Power off with 39.8us. 5: Power off with 71.6us. [6]: Enable power too low reset. [7]: Clear interrupt of "PWRISNOGOOD".	
63h (1EC6h)	**REG1EC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_OV_KEY[7:0]	7:0	Set bonding overwrite key.	
63h (1EC7h)	**REG1EC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_OV_KEY[15:8]	7:0	See description of '1EC6h'.	
65h (1ECAh)	**REG1ECA**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	CHIP_CONFIG_STAT[3:0]	3:0	CHIP_CONFIG status.	
66h (1ECCh)	**REG1ECC**	**7:0**	**Default : 0x00**	**Access : RO**
	DEVICE_ID[7:0]	7:0	Device ID.	
66h (1ECDh)	**REG1ECD**	**7:0**	**Default : 0x00**	**Access : RO**
	DEVICE_ID[15:8]	7:0	See description of '1ECCh'.	
67h (1ECEh)	**REG1ECE**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_VERSION[7:0]	7:0	Chip version	
67h (1ECFh)	**REG1ECF**	**7:0**	**Default : 0x00**	**Access : RO**
	CHIP_REVISION[7:0]	7:0	Chip revision.	
68h (1ED0h)	**REG1ED0**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_OV_EN[7:0]	7:0	Bonding overwrite enable.	
68h (1ED1h)	**REG1ED1**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_OV_EN[15:8]	7:0	See description of '1ED0h'.	
69h	**REG1ED2**	**7:0**	**Default : 0x00**	**Access : R/W**

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1ED2h)	-	7:1	Reserved.	
	BOND_OV_EN[16]	0	See description of '1ED0h'.	
6Ah (1ED4h)	**REG1ED4**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_OV[7:0]	7:0	Bonding overwrite value.	
6Ah (1ED5h)	**REG1ED5**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOND_OV[15:8]	7:0	See description of '1ED4h'.	
6Bh (1ED6h)	**REG1ED6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BOND_OV[16]	0	See description of '1ED4h'.	
6Ch (1ED8h)	**REG1ED8**	**7:0**	**Default : 0x00**	**Access : RO**
	STAT_BOND[7:0]	7:0	Bonding status read back.	
6Ch (1ED9h)	**REG1ED9**	**7:0**	**Default : 0x00**	**Access : RO**
	STAT_BOND[15:8]	7:0	See description of '1ED8h'.	
6Dh (1EDAh)	**REG1EDA**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	STAT_BOND[16]	0	See description of '1ED8h'.	
70h (1EE0h)	**REG1EE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIOR_OUT[7:0]	7:0	I control when specifying PAD_GPIOR as GPIOR.	
70h (1EE1h)	**REG1EE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GPIOR_OUT[10:8]	2:0	See description of '1EE0h'.	
71h (1EE2h)	**REG1EE2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPIOR_OEN[7:0]	7:0	OEN control when specifying PAD_GPIOR as GPIOR.	
71h (1EE3h)	**REG1EE3**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	GPIOR_OEN[10:8]	2:0	See description of '1EE2h'.	
72h (1EE4h)	**REG1EE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_A[7:0]	7:0	Spare Registers A. <GPIOECO_4>. [0]: GPIO_XA_00S (PAD_AD0). [1]: GPIO_XA_01S (PAD_AD1). [2]: GPIO_XA_02S (PAD_AD2). [3]: GPIO_XA_03S (PAD_AD3). [4]: GPIO_XA_04S (PAD_WRZ).	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[5]: GPIO_XA_05S (PAD_RDZ). [6]: GPIO_XA_06S (PAD_ALE). [7]: Reserved. <GPIOECO_2>. [8]: GPIO_XB_00S (PAD_SAR0). [9]: GPIO_XB_01S (PAD_SAR1). [10]: GPIO_XB_02S (PAD_SAR2). [11]: GPIO_XB_03S (PAD_SAR3). <GPIOECO_3>. [12]: GPIO_XC_00S (PAD_PWM0). [13]: GPIO_XC_01S (PAD_PWM1). [14]: GPIO_XC_02S (PAD_PWM2). [15]: GPIO_XC_03S (PAD_PWM3).	
72h (1EE5h)	**REG1EE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_A[15:8]	7:0	See description of '1EE4h'.	
73h (1EE6h)	**REG1EE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPARE_B[7:0]	7:0	Spare Registers B. <GPIOECO_5>. [0]: GPIO_XD_00S (PAD_LVSYNC). [1]: GPIO_XD_01S (PAD_LHSYNC). [2]: GPIO_XD_02S (PAD_LCK_ODD). [3]: GPIO_XD_03S (PAD_LDE).	
73h (1EE7h)	**REG1EE7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:0	Reserved.	
74h (1EE8h)	**REG1EE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:0	Reserved.	
74h (1EE9h)	**REG1EE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:0	Reserved.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
76h (1EECh)	**REG1EEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	UART_INNER_LOOPBACK[4:0]	7:3		
76h (1EEDh)	**REG1EED**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	UART_PAD_INVERSE[1:0]	3:2		
	UART_OUTER_LOOPBACK[1:0]	1:0		
78h (1EF0h)	**REG1EF0**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Reserved.	
78h (1EF1h)	**REG1EF1**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Reserved.	
79h (1EF2h)	**REG1EF2**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Reserved.	
79h (1EF3h)	**REG1EF3**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:0	Reserved.	
7Ah (1EF4h)	**REG1EF4**	**7:0**	**Default : 0x00**	**Access : RO**
		7:0	Reserved.	
7Ah (1EF5h)	**REG1EF5**	**7:0**	**Default : 0x00**	**Access : RO**
		7:0	Reserved.	
7Bh (1EF6h)	**REG1EF6**	**7:0**	**Default : 0x00**	**Access : RO**
		7:0	Reserved.	
7Bh (1EF7h)	**REG1EF7**	**7:0**	**Default : 0x00**	**Access : RO**
		7:0	Reserved.	
7Ch (1EF8h)	**REG1EF8**	**7:0**	**Default : 0x00**	**Access : RO**
		7:0	Reserved.	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Ch (1EF9h)	**REG1EF9**	**7:0**	**Default : 0x00**	**Access : RO**
		7:0	Reserved.	
7Dh (1EFAh)	**REG1EFA**	**7:0**	**Default : 0x00**	**Access : RO**
		7:0	Reserved.	
7Dh (1EFBh)	**REG1EFB**	**7:0**	**Default : 0x00**	**Access : RO**
		7:0	Reserved.	

OSD3 Register (Bank = 1F)

OSD3 Register (Bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ch (1F78h)	**REG1F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW0GDSR	7	Sub Window 0 Gradient color Sign bit of Red color. 0: Decrease. 1: Increase.	
	SW0GDSTPR	6:4	Sub Window 0 Gradient color Step of Red color.	
	SW0GDINCR	3:0	Sub Window 0 Gradient color Increase/Decrease value of Red color.	
3Ch (1F79h)	**REG1F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW0GDSG	7	Sub Window 0 Gradient color Sign bit of Green color. 0: Decrease. 1: Increase.	
	SW0GDSTPG	6:4	Sub Window 0 Gradient color Step of Green color.	
	SW0GDINCG	3:0	Sub Window 0 Gradient color Increase/Decrease value of Green color.	
3Dh (1F7Ah)	**REG1F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW0GDSB	7	Sub Window 0 Gradient color Sign bit of Blue color. 0: Decrease. 1: Increase.	
	SW0GDSTPB	6:4	Sub Window 0 Gradient color Step of Blue color.	
	SW0GDINCB	3:0	Sub Window 0 Gradient color Increase/Decrease value of Blue color.	
3Dh (1F7Bh)	**REG1F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW0DAR	7:4	Sub Window 0 Gradient color Delta value of Red color.	

OSD3 Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
	SW0DAG	3:0	Sub Window 0 Gradient color Delta value of Green color.
3Eh (1F7Ch)	**REG1F7C**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	SW0DAB	3:0	Sub Window 0 Gradient color Delta value of Blue color.
3Eh (1F7Dh)	**REG1F7D**	**7:0**	**Default : 0x00** **Access : R/W**
	SW0GDDE[7:0]	7:0	Sub Window 0 Gradient color DE range value[7:0].
3Fh (1F7Eh)	**REG1F7E**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:3	Reserved.
	SW0GDDE[10:8]	2:0	See description for SW0GDDE[7:0].
3Fh (1F7Fh)	**REG1F7F**	**7:0**	**Default : 0x00** **Access : R/W**
	SW0GDSDE[7:0]	7:0	Sub Window 0 Gradient color Sub DE range value[7:0].
40h (1F80h)	**REG1F80**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:2	Reserved.
	SW0GDSDE[9:8]	1:0	See description for SW0GDSDE[7:0].
40h (1F81h)	**REG1F81**	**7:0**	**Default : 0x00** **Access : R/W**
	GDEN	7	Gradient color enable. Double Buffer. 0: Disable. 1: Enable.
	-	6	Reserved.
	-	5	Reserved.
	SW0GDOFEN	4	Sub Window 0 Gradient color Overflow enable. 0: Disable. 1: Enable.
	SW0GDDESM	3:2	Sub Window 0 Gradient color DE Select Mode. 00: Sub DE is equal to full DE 01: Sub DE at left side of DE 10: Sub DE at both side of DE 11: Sub DE at right side of DE
	SW0GDVSEL	1	Sub Window 0 Gradient color Vertical Direction Select. 0: Vertical Direction Disable. 1: Vertical Direction Enable.
	SW0GDHSEL	0	Sub Window 0 Gradient color Horizontal Direction Select. 0: Horizontal Direction Disable.

OSD3 Register (Bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Horizontal Direction Enable.	
41h (1F82h)	**REG1F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW0GDINIR[7:0]	7:0	Sub Window 0 Gradient color Initial value of Red color.	
41h (1F83h)	**REG1F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW0GDINIG[7:0]	7:0	Sub Window 0 Gradient color Initial value of Green color.	
42h (1F84h)	**REG1F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW0GDINIB[7:0]	7:0	Sub Window 0 Gradient color Initial value of Blue color.	
42h (1F85h)	**REG1F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1GDSR	7	Sub Window 1 Gradient color Sign bit of Red color. 0: Decrease. 1: Increase.	
	SW1GDSTPR	6:4	Sub Window 1 Gradient color Step of Red color.	
	SW1GDINCR	3:0	Sub Window 1 Gradient color Increase/Decrease value of Red color.	
43h (1F86h)	**REG1F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1GDSG	7	Sub Window 1 Gradient color Sign bit of Green color. 0: Decrease. 1: Increase.	
	SW1GDSTPG	6:4	Sub Window 1 Gradient color Step of Green color.	
	SW1GDINCG	3:0	Sub Window 1 Gradient color Increase/Decrease value of Green color.	
43h (1F87h)	**REG1F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1GDSB	7	Sub Window 1 Gradient color Sign bit of Blue color. 0: Decrease. 1: Increase.	
	SW1GDSTPB	6:4	Sub Window 1 Gradient color Step of Blue color.	
	SW1GDINCB	3:0	Sub Window 1 Gradient color Increase/Decrease value of Blue color.	
44h (1F88h)	**REG1F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1DAR	7:4	Sub Window 1 Gradient color Delta value of Red color.	
	SW1DAG	3:0	Sub Window 1 Gradient color Delta value of Green color.	
44h (1F89h)	**REG1F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW1DAB	3:0	Sub Window 1 Gradient color Delta value of Blue color.	

OSD3 Register (Bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
45h (1F8Ah)	**REG1F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1GDDE[7:0]	7:0	Sub Window 1 Gradient color DE range value[7:0].	
45h (1F8Bh)	**REG1F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SW1GDDE[10:8]	2:0	See description for SW1GDDE[7:0].	
46h (1F8Ch)	**REG1F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1GDSDE[7:0]	7:0	Sub Window 1 Gradient color Sub DE range value[7:0].	
46h (1F8Dh)	**REG1F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SW1GDSDE[9:8]	1:0	See description for SW1GDSDE[7:0].	
47h (1F8Eh)	**REG1F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SW1GDOFEN	4	Sub Window 1 Gradient color Overflow enable. 0: Disable. 1: Enable.	
	SW1GDDESM	3:2	Sub Window 1 Gradient color DE Select Mode. 00: Sub DE is equal to full DE 01: Sub DE at left side of DE 10: Sub DE at both side of DE 11: Sub DE at right side of DE	
	SW1GDVSEL	1	Sub Window 1 Gradient color Vertical Direction Select. 0: Vertical Direction Disable. 1: Vertical Direction Enable.	
	SW1GDHSEL	0	Sub Window 1 Gradient color Horizontal Direction Select. 0: Horizontal Direction Disable. 1: Horizontal Direction Enable.	
47h (1F8Fh)	**REG1F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1GDINIR[7:0]	7:0	Sub Window 1 Gradient color Initial value of Red color.	
48h (1F90h)	**REG1F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1GDINIG[7:0]	7:0	Sub Window 1 Gradient color Initial value of Green color.	
48h (1F91h)	**REG1F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW1GDINIB[7:0]	7:0	Sub Window 1 Gradient color Initial value of Blue color.	
49h	**REG1F92**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD3 Register (Bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1F92h)	SW2GDSR	7	Sub Window 2 Gradient color Sign bit of Red color. 0: Decrease. 1: Increase.	
	SW2GDSTPR	6:4	Sub Window 2 Gradient color Step of Red color.	
	SW2GDINCR	3:0	Sub Window 2 Gradient color Increase/Decrease value of Red color.	
49h (1F93h)	**REG1F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW2GDSG	7	Sub Window 2 Gradient color Sign bit of Green color. 0: Decrease. 1: Increase.	
	SW2GDSTPG	6:4	Sub Window 2 Gradient color Step of Green color.	
	SW2GDINCG	3:0	Sub Window 2 Gradient color Increase/Decrease value of Green color.	
4Ah (1F94h)	**REG1F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW2GDSB	7	Sub Window 2 Gradient color Sign bit of Blue color. 0: Decrease. 1: Increase.	
	SW2GDSTPB	6:4	Sub Window 2 Gradient color Step of Blue color.	
	SW2GDINCB	3:0	Sub Window 2 Gradient color Increase/Decrease value of Blue color.	
4Ah (1F95h)	**REG1F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW2DAR	7:4	Sub Window 2 Gradient color Delta value of Red color.	
	SW2DAG	3:0	Sub Window 2 Gradient color Delta value of Green color.	
4Bh (1F96h)	**REG1F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW2DAB	3:0	Sub Window 2 Gradient color Delta value of Blue color.	
4Bh (1F97h)	**REG1F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW2GDDE[7:0]	7:0	Sub Window 2 Gradient color DE range value[7:0].	
4Ch (1F98h)	**REG1F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SW2GDDE[10:8]	2:0	See description for SW2GDDE[7:0].	
4Ch (1F99h)	**REG1F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW2GDSDE[7:0]	7:0	Sub Window 2 Gradient color Sub DE range value[7:0].	
4Dh	**REG1F9A**	**7:0**	**Default : 0x00**	**Access : R/W**

OSD3 Register (Bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1F9Ah)	-	7:2	Reserved.	
	SW2GDSDE[9:8]	1:0	See description for SW2GDSDE[7:0].	
4Dh (1F9Bh)	**REG1F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SW2GDOFEN	4	Sub Window 2 Gradient color Overflow enable. 0: Disable. 1: Enable.	
	SW2GDDESM	3:2	Sub Window 2 Gradient color DE Select Mode. 00: Sub DE is equal to full DE 01: Sub DE at left side of DE 10: Sub DE at both side of DE 11: Sub DE at right side of DE	
	SW2GDVSEL	1	Sub Window 2 Gradient color Vertical Direction Select. 0: Vertical Direction Disable. 1: Vertical Direction Enable.	
	SW2GDHSEL	0	Sub Window 2 Gradient color Horizontal Direction Select. 0: Horizontal Direction Disable. 1: Horizontal Direction Enable.	
4Eh (1F9Ch)	**REG1F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW2GDINIR[7:0]	7:0	Sub Window 2 Gradient color Initial value of Red color.	
4Eh (1F9Dh)	**REG1F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW2GDINIG[7:0]	7:0	Sub Window 2 Gradient color Initial value of Green color.	
4Fh (1F9Eh)	**REG1F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW2GDINIB[7:0]	7:0	Sub Window 2 Gradient color Initial value of Blue color.	
4Fh (1F9Fh)	**REG1F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW3GDSR	7	Sub Window 3 Gradient color Sign bit of Red color. 0: Decrease. 1: Increase.	
	SW3GDSTPR	6:4	Sub Window 3 Gradient color Step of Red color.	
	SW3GDINCR	3:0	Sub Window 3 Gradient color Increase/Decrease value of Red color.	
50h (1FA0h)	**REG1FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW3GDSG	7	Sub Window 3 Gradient color Sign bit of Green color. 0: Decrease.	

OSD3 Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
			1: Increase.
	SW3GDSTPG	6:4	Sub Window 3 Gradient color Step of Green color.
	SW3GDINCG	3:0	Sub Window 3 Gradient color Increase/Decrease value of Green color.
50h (1FA1h)	**REG1FA1**	**7:0**	**Default : 0x00** **Access : R/W**
	SW3GDSB	7	Sub Window 3 Gradient color Sign bit of Blue color. 0: Decrease. 1: Increase.
	SW3GDSTPB	6:4	Sub Window 3 Gradient color Step of Blue color.
	SW3GDINCB	3:0	Sub Window 3 Gradient color Increase/Decrease value of Blue color.
51h (1FA2h)	**REG1FA2**	**7:0**	**Default : 0x00** **Access : R/W**
	SW3DAR	7:4	Sub Window 3 Gradient color Delta value of Red color.
	SW3DAG	3:0	Sub Window 3 Gradient color Delta value of Green color.
51h (1FA3h)	**REG1FA3**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	SW3DAB	3:0	Sub Window 3 Gradient color Delta value of Blue color.
52h (1FA4h)	**REG1FA4**	**7:0**	**Default : 0x00** **Access : R/W**
	SW3GDDE[7:0]	7:0	Sub Window 3 Gradient color DE range value[7:0].
52h (1FA5h)	**REG1FA5**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:3	Reserved.
	SW3GDDE[10:8]	2:0	See description for SW3GDDE[7:0].
53h (1FA6h)	**REG1FA6**	**7:0**	**Default : 0x00** **Access : R/W**
	SW3GDSDE[7:0]	7:0	Sub Window 3 Gradient color Sub DE range value[7:0].
53h (1FA7h)	**REG1FA7**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:2	Reserved.
	SW3GDSDE[9:8]	1:0	See description for SW3GDSDE[7:0].
54h (1FA8h)	**REG1FA8**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:5	Reserved.
	SW3GDOFEN	4	Sub Window 3 Gradient color Overflow enable. 0: Disable. 1: Enable.
	SW3GDDESM	3:2	Sub Window 3 Gradient color DE Select Mode. 00: Sub DE is equal to full DE

OSD3 Register (Bank = 1F)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			01: Sub DE at left side of DE 10: Sub DE at both side of DE 11: Sub DE at right side of DE
	SW3GDVSEL	1	Sub Window 3 Gradient color Vertical Direction Select. 0: Vertical Direction Disable. 1: Vertical Direction Enable.
	SW3GDHSEL	0	Sub Window 3 Gradient color Horizontal Direction Select. 0: Horizontal Direction Disable. 1: Horizontal Direction Enable.
54h (1FA9h)	**REG1FA9**	**7:0**	**Default : 0x00** **Access : R/W**
	SW3GDINIR[7:0]	7:0	Sub Window 3 Gradient color Initial value of Red color.
55h (1FAAh)	**REG1FAA**	**7:0**	**Default : 0x00** **Access : R/W**
	SW3GDINIG[7:0]	7:0	Sub Window 3 Gradient color Initial value of Green color.
55h (1FABh)	**REG1FAB**	**7:0**	**Default : 0x00** **Access : R/W**
	SW3GDINIB[7:0]	7:0	Sub Window 3 Gradient color Initial value of Blue color.

PM_CEC Register (Bank = 21)

PM_CEC Register (Bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2100h)	**REG2100**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CEC_TX_LEN[3:0]	3:0	Number of bytes of data that initiator wants to send. Write this register to trigger a new TX request. 0: Only header block is sent.	
00h (2101h)	**REG2101**	**7:0**	**Default : 0x03**	**Access : R/W**
	CEC_SAMPLE_SEL[2:0]	7:5	Sample times select for CEC line high/low detection. 000: 1X. 001: 2X. 010: 4X. .. 110: 12X. 111: 14X.	
	TX_LOW_BIT_SEL[1:0]	4:3	The period select for follower to generate a low bit period when the current received bit is too short to be a valid bit. 00: 1X nominal data bit period. 01: 1.4X nominal data bit period. 10: 1.5X nominal data bit period. 11: 1.6X nominal data bit period.	
	RETRY_CNT[2:0]	2:0	The retry times for re-transmitting a message (max).	
01h (2102h)	**REG2102**	**7:0**	**Default : 0x00**	**Access : R/W**
	CEC_CTRL_EN	7	Enable CEC controller. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	CEC_CLK_GATE	5	CEC main clock input is gated or not. 0: Not gate. 1: Gate.	
	CANCEL_TX_REQ	4	Cancel current TX request. 0: Normal. 1: Cancel.	
	TX_FALLING_SHIFT_SEL[1:0]	3:2	TX falling edge is shifted backward. 00: 0us. 01: 50us. 10: 100us. 11: 200us.	

PM_CEC Register (Bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TX_RISING_SHIFT_SEL[1:0]	1:0	TX rising edge is shifted backward. 00: 0us. 01: 50us. 10: 100us. 11: 200us.	
01h (2103h)	**REG2103**	**7:0**	**Default : 0x53**	**Access : R/W**
	CEC_FREE_CNT2[3:0]	7:4	The necessary free bit period when new initiator wants to send a frame.	
	CEC_FREE_CNT1[3:0]	3:0	The necessary free bit period when pervious attempt to send frame is unsuccessful.	
02h (2104h)	**REG2104**	**7:0**	**Default : 0x07**	**Access : R/W**
	CEC_LOGICAL_ADDR[3:0]	7:4	Device logical address.	
	CEC_FREE_CNT3[3:0]	3:0	The necessary free bit period when present initiator wants to send another frame immediately after the previous one.	
02h (2105h)	**REG2105**	**7:0**	**Default : 0x8C**	**Access : R/W**
	CNT_10US_VALUE[7:0]	7:0	Number of counts to achieve 10us (integer part). 0: 256 clock cycles. 1: 1 clock cycle. 2: 2 clock cycles. ... 255: 255 clock cycles. (Unit: clock cycle).	
03h (2106h)	**REG2106**	**7:0**	**Default : 0x03**	**Access : R/W**
	RX_BOUND_SHIFT[3:0]	7:4	RX upper/lower bound is shifted forward/backward N*10us.	
	F_CNT_10US_VALUE[3:0]	3:0	Number of counts to achieve 10us (fractional part). This part is useless when CNT_10US_VALUE = 1 (clock cycle). (Unit: 0.0625 clock cycle).	
03h (2107h)	**REG2107**	**7:0**	**Default : 0x08**	**Access : R/W**
	IGNORE_UNEXP_OP_LEN	7	Ignore unexpected length for opcode 0~3.	
	NSUP_CMD_ACT[1:0]	6:5	Action for non-supported command. 00: Ignore and ACK. 01: NACK. 1x: Feature abort.	
	CEC_CTRL_SEL	4	Select which CEC controller is active. 0: Normal CEC controller. 1: Power down hardware CEC controller.	
	LOST_ABT_SEL	3	Cancel TX request or retry if TX loses arbitration to a second	

PM_CEC Register (Bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			initiator. 0: Retry. 1: Cancel.	
	CEC_OVERRIDE_FUN	2	Force CEC line low. 0: Disable. 1: Enable.	
	-	1	Reserved.	
	DIS_EH	0	Disable CEC error handling. 0: Normal. 1: Disable.	
04h (2108h)	**REG2108**	**7:0**	**Default : 0x00**	**Access : RO**
	HW_CEC_STS	7	Hardware CEC controller status. 0: Busy. 1: Idle.	
	CEC_TX_REQ_STS	6	Indicate the TX request status (RO). 0: End. 1: Ongoing.	
	CEC_LINE	5	CEC line status.	
	CEC_RX_LEN[4:0]	4:0	The length of received message (RO). 0: Only header block is received.	
04h (2109h)	**REG2109**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	CHKSM_CMP_ERR_STS	0	Event status bit for checksum error.	
07h (210Eh)	**REG210E**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAKEUP_INT_MASK	7	Mask wakeup event interrupt.	
	OP3_OPERAND1_EN	6	Wakeup enable for the second operand specific to opcode 3.	
	OP2_OPERAND1_EN	5	Wakeup enable for the second operand specific to opcode 2.	
	OP_EN[4:0]	4:0	Wakeup enable for opcode 0~4.	
07h (210Fh)	**REG210F**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXP_OP4_LEN[3:0]	7:4	Expected RX length for opcode 4. Header and opcode are not included.	
	OPERAND_EN[3:0]	3:0	Wakeup enable for the operand specific to opcode 0~3.	
08h (2110h)	**REG2110**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE0[7:0]	7:0	Revive opcode 0 to wake up.	
08h	**REG2111**	**7:0**	**Default : 0x00**	**Access : R/W**

PM_CEC Register (Bank = 21)

Index (Absolute)	Mnemonic	Bit	Description	
(2111h)	OPCODE1[7:0]	7:0	Revive opcode 1 to wake up.	
09h (2112h)	**REG2112**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE2[7:0]	7:0	Revive opcode 2 to wake up.	
09h (2113h)	**REG2113**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE3[7:0]	7:0	Revive opcode 3 to wake up.	
0Ah (2114h)	**REG2114**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPCODE4[7:0]	7:0	Revive opcode 4 to wake up.	
0Ah (2115h)	**REG2115**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP0_OPERAND[7:0]	7:0	Revive the operand specific to opcode 0 to wake up.	
0Bh (2116h)	**REG2116**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1_OPERAND[7:0]	7:0	Revive the operand specific to opcode 1 to wake up.	
0Bh (2117h)	**REG2117**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP2_OPERAND0[7:0]	7:0	Revive the operand specific to opcode 2 to wake up.	
0Ch (2118h)	**REG2118**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP2_OPERAND1[7:0]	7:0	Revive the operand specific to opcode 2 to wake up.	
0Ch (2119h)	**REG2119**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP3_OPERAND0[7:0]	7:0	Revive the operand specific to opcode 3 to wake up.	
0Dh (211Ah)	**REG211A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP3_OPERAND1[7:0]	7:0	Revive the operand specific to opcode 3 to wake up.	
0Dh (211Bh)	**REG211B**	**7:0**	**Default : 0x04**	**Access : R/W**
	OP_ACC_TYPE[4:0]	7:3	Access type for opcode 0~4. 0: Direct. 1: Broadcast.	
	CEC_VERSION[2:0]	2:0	CEC version. 000: Version 1.1. 001: Version 1.2. 010: Version 1.2a. 011: Version 1.3. 1xx: Version 1.3a.	
0Eh (211Ch)	**REG211C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHYSICAL_ADDR[7:0]	7:0	Device physical address.	
0Eh (211Dh)	**REG211D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PHYSICAL_ADDR[15:8]	7:0	See description of '211Ch'.	
0Fh	**REG211E**	**7:0**	**Default : 0x00**	**Access : R/W**

PM_CEC Register (Bank = 21)

Index (Absolute)	Mnemonic	Bit	Description	
(211Eh)	VENDOR_ID[7:0]	7:0	Device vendor ID.	
0Fh (211Fh)	**REG211F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VENDOR_ID[15:8]	7:0	See description of '211Eh'.	
10h (2120h)	**REG2120**	**7:0**	**Default : 0x00**	**Access : R/W**
	VENDOR_ID[23:16]	7:0	See description of '211Eh'.	
10h (2121h)	**REG2121**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ABORT_REASON[2:0]	2:0	Feature abort reason. 000: "Unrecognized opcode". 001: "Not in correct mode to respond". 010: "Cannot provide source". 011: "Invalid operand". 100: "Refused".	
11h (2122h)	**REG2122**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	WAKEUP_INT	6	Wakeup interrupt event.	
	RX_BIT_TOO_LONG	5	RX bit too long.	
	RX_BIT_TOO_SHORT	4	RX bit too short.	
	HW_RX_EVENT_STS3	3	Receive GIVE_DEVICE_VENDOR_ID message in power down mode.	
	HW_RX_EVENT_STS2	2	Receive GET_CEC_VERSION message in power down mode.	
	HW_RX_EVENT_STS1	1	Receive GIVE_PHYSICAL_ADDRESS message in power down mode.	
	HW_RX_EVENT_STS0	0	Receive GIVE_DEVICE_POWER_STATUS message in power down mode.	
11h (2123h)	**REG2123**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	CEC_EVENT_INT[4:0]	4:0	CEC event status. [0]: New message received successfully. [1]: Message sent successfully. [2]: Retry failed. [3]: Lost arbitration to the second initiator. [4]: Follower transmits NACK.	
12h (2124h)	**REG2124**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

PM_CEC Register (Bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CEC_EVENT_INT_FORCE[4:0]	4:0	Force CEC event interrupt.	
12h (2125h)	**REG2125**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CEC_EVENT_INT_CLEAR[4:0]	4:0	Clear CEC event interrupt.	
13h (2126h)	**REG2126**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CEC_EVENT_INT_MASK[4:0]	4:0	Mask CEC event interrupt.	
14h (2128h)	**REG2128**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CHKSUM_ERR_MASK	3	Checksum error wakeup interrupt mask.	
	CLR_CHKSUM_ERR	2	Clear checksum error.	
	-	1:0	Reserved.	
14h (2129h)	**REG2129**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEV_TYPE[7:0]	7:0	CEC device type for GET_PHYSICAL_ADDRESS message.	
18h (2130h)	**REG2130**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA0[7:0]	7:0	Data block 0 for TX.	
18h (2131h)	**REG2131**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA1[7:0]	7:0	Data block 1 for TX.	
19h (2132h)	**REG2132**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA2[7:0]	7:0	Data block 2 for TX.	
19h (2133h)	**REG2133**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA3[7:0]	7:0	Data block 3 for TX.	
1Ah (2134h)	**REG2134**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA4[7:0]	7:0	Data block 4 for TX.	
1Ah (2135h)	**REG2135**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA5[7:0]	7:0	Data block 5 for TX.	
1Bh (2136h)	**REG2136**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA6[7:0]	7:0	Data block 6 for TX.	
1Bh (2137h)	**REG2137**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA7[7:0]	7:0	Data block 7 for TX.	

PM_CEC Register (Bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ch (2138h)	**REG2138**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA8[7:0]	7:0	Data block 8 for TX.	
1Ch (2139h)	**REG2139**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA9[7:0]	7:0	Data block 9 for TX.	
1Dh (213Ah)	**REG213A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA10[7:0]	7:0	Data block 10 for TX.	
1Dh (213Bh)	**REG213B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA11[7:0]	7:0	Data block 11 for TX.	
1Eh (213Ch)	**REG213C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA12[7:0]	7:0	Data block 12 for TX.	
1Eh (213Dh)	**REG213D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA13[7:0]	7:0	Data block 13 for TX.	
1Fh (213Eh)	**REG213E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA14[7:0]	7:0	Data block 14 for TX.	
1Fh (213Fh)	**REG213F**	**7:0**	**Default : 0x00**	**Access : R/W**
	TX_DATA15[7:0]	7:0	Data block 15 for TX.	
20h (2140h)	**REG2140**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA0[7:0]	7:0	Data block 0 for RX.	
20h (2141h)	**REG2141**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA1[7:0]	7:0	Data block 1 for RX.	
21h (2142h)	**REG2142**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA2[7:0]	7:0	Data block 2 for RX.	
21h (2143h)	**REG2143**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA3[7:0]	7:0	Data block 3 for RX.	
22h (2144h)	**REG2144**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA4[7:0]	7:0	Data block 4 for RX.	
22h (2145h)	**REG2145**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA5[7:0]	7:0	Data block 5 for RX.	
23h (2146h)	**REG2146**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA6[7:0]	7:0	Data block 6 for RX.	
23h (2147h)	**REG2147**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA7[7:0]	7:0	Data block 7 for RX.	
24h	**REG2148**	**7:0**	**Default : 0x00**	**Access : RO**

PM_CEC Register (Bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2148h)	RX_DATA8[7:0]	7:0	Data block 8 for RX.	
24h (2149h)	**REG2149**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA9[7:0]	7:0	Data block 9 for RX.	
25h (214Ah)	**REG214A**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA10[7:0]	7:0	Data block 10 for RX.	
25h (214Bh)	**REG214B**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA11[7:0]	7:0	Data block 11 for RX.	
26h (214Ch)	**REG214C**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA12[7:0]	7:0	Data block 12 for RX.	
26h (214Dh)	**REG214D**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA13[7:0]	7:0	Data block 13 for RX.	
27h (214Eh)	**REG214E**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA14[7:0]	7:0	Data block 14 for RX.	
27h (214Fh)	**REG214F**	**7:0**	**Default : 0x00**	**Access : RO**
	RX_DATA15[7:0]	7:0	Data block 15 for RX.	

UHC0 Register (Bank = 24)

UHC0 Register (Bank = 24)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2400h)	**HCCAP**	**7:0**	**Default : 0x10**	**Access : RO**
	CAPLENGTH	7:0	Capability Register Length. This register is used as an offset to be added to register base to determine the beginning of the Operational Register Space.	
00h (2401h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
01h (2402h)	**HCCAP**	**7:0**	**Default : 0x00**	**Access : RO**
	HCIVERSION[7:0]	7:0	Host Controller Interface Version Number. This register is a two-byte register containing a BCD encoding of the EHCI revision number supported by the Host Controller.	
01h (2403h)	**HCCAP**	**7:0**	**Default : 0x01**	**Access : RO**
	HCIVERSION[15:8]	7:0	See description of '2402h'.	
02h (2404h)	**HCSPARAMS**	**7:0**	**Default : 0x01**	**Access : RO**
	-	7:4	Reserved.	
	N_PORTS	3:0	Number of Ports. This field specifies the number of physical downstream ports implemented on the Host Controller.	
02h ~ 03h (2405h ~ 2407h)	**-**	**7:0**	**Default : -**	**Access : -**
		7:0	Reserved.	
04h (2408h)	**HCCPARAMS**	**7:0**	**Default : 0x06**	**Access : RO**
	-	7:3	Reserved.	
	ASYN_SCH_PARK_CAP	2	Asynchronous Schedule Park Capability. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via the Frame List Size field of USBCMD register. This requirement ensures the frame list is always physically contiguous.	
	PROG_FR_LIST_FLAG	1	Programmable Frame List Flag. When this bit is set to '1', system software can specify and use a smaller frame list and configure the Host Controller via Frame List Size Field of USBCMD register. This requirement ensures the frame list is	

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
			always physically contiguous.
	-	0	Reserved.
04h ~ 07h (2409h ~ 240Fh)	**-**	**7:0**	**Default : -** **Access : -**
	-	7:0	Reserved.
08h (2410h)	**USBCMD**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7	Reserved.
	INT_OAAD	6	Interrupt on Asynchronous Advance Doorbell. This bit is used as a doorbell by software to ring the Host Controller to issue an interrupt at the next advance of Asynchronous Schedule.
	ASCH_EN	5	Asynchronous Schedule Enable. This bit controls whether the Host Controller should skip the processing of Asynchronous Schedule. 0: Do not process Asynchronous Schedule. 1: Use the ASYNCLISTADDR register to access the Asynchronous Schedule.
	PSCH_EN	4	Periodic Schedule Enable. This bit controls whether the Host Controller should skip the processing of Periodic Schedule. 0: Do not process Periodic Schedule. 1: Use the PERIODICKISTBASE register to access the Periodic Schedule.
	FRL_SIZE	3:2	Frame List Size. This field specifies the size of the frame list. 00: 1024 elements (4096 bytes; default value). 01: 512 elements (2048 bytes). 10: 256 elements (1024 bytes). 11: Reserved.
	HC_RESET	1	Host Controller Reset. This control bit is used by software to reset the Host Controller.
	RS	0	Run/Stop. When this bit is set to '1', the Host Controller proceeds with the execution of schedule. 0: Stop. 1: Run.
08h	**USBCMD**	**7:0**	**Default : 0x0b** **Access : R/W**

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
(2411h)	-	7:4	Reserved.
	ASYN_PK_EN	3	Asynchronous Schedule Park Mode Enable. Software uses this register to enable or disable the Park mode. When this register is set to 1, the Park mode is enabled.
	-	2	Reserved.
	ASYN_PK_CNT	1:0	Asynchronous Schedule Park Mode Count. This field contains a count for the number of successive transactions that the Host Controller is allowed to execute from a high-speed queue head on Asynchronous Schedule.
09h (2412h)	**USBCMD**	**7:0**	**Default : 0x08** **Access : R/W**
	INT_THRC	7:0	Interrupt Threshold Control. This field is used by system software to select the maximum rate at which the Host Controller will issue interrupts. The only valid values are described below: Value Maximum Interrupt Interval for High Speed 00h Reserved. 01h 1 micro-frame. 02h 2 micro-frames. 04h 4 micro-frames. 08h 8 micro-frames (default, equals to 1ms). 10h 16 micro-frames (2 ms). 20h 32 micro-frames (4 ms). 40h 64 micro-frames (8 ms). Note: For Full Speed, these registers are reserved.
09h (2413h)	**-**	**7:0**	**Default : -** **Access : -**
	-	7:0	Reserved.
0Ah (2414h)	**USBSTS**	**7:0**	**Default : 0x00** **Access : R/WC**
	-	7:6	Reserved.
	INT_OAA	5	Interrupt on Async Advance. This status bit indicates the assertion of interrupt on Async Advance Doorbell.
	H_SYSERR	4	Host System Error. The Host Controller sets this bit to 1 when a serious error occurred during a host system access involving the Host Controller module.
	FRL_ROL	3	Frame List Rollover.

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
			The Host Controller sets this bit to 1 when the Frame List Index rolls over from its maximum value to zero.
	PO_CHG_DET	2	Port Change Detect. The Host Controller sets this bit to '1' when any port has a change bit transition from '0' to '1'. In addition, this bit is loaded with the OR of all of the PORTSC change bits.
	USBERR_INT	1	USB Error Interrupt. The Host Controller sets this bit to '1' when the completion of a USB transaction results in an error condition.
	USB_INT	0	USB Interrupt. The Host Controller sets this bit to '1' upon the completion of a USB transaction.
0Ah (2415h)	**USBSTS**	**7:0**	**Default : 0x10** **Access : RO**
	ASCH_STS	7	Asynchronous Schedule Status. This bit reports the actual status of Asynchronous Schedule.
	PSCH_STS	6	Periodic Schedule Status. This bit reports the actual status of Periodic Schedule.
	RECLAMATION	5	Reclamation. This is a read-only status bit, and is used to detect an empty or Asynchronous Schedule.
	HCHALTED	4	Host Controller Halted. This bit is a zero whenever the Run/Stop bit is set to '1'. The Host Controller sets this bit to '1' after it has stopped the executing as a result of the Run/Stop bit being set to '0'.
	-	3:0	Reserved.
0Bh (2416h ~ 2417h)	**-**	**7:0**	**Default : -** **Access : -**
	-	7:0	Reserved.
0Ch (2418h)	**USBINTR**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:6	Reserved.
	INT_OAA_EN	5	Interrupt on Async Advance Enable. When this bit is set to '1', and the Interrupt on Async Advance bit in the USBSTS register is set to '1' also, the

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			Host Controller will issue an interrupt at the next interrupt threshold.	
	H_SYSERR_EN	4	Host System Error Enable. When this bit is set to '1', and the Host System Error Status bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	FRL_ROL_EN	3	Frame List Rollover Enable. When this bit is set to '1', and the Frame List Rollover bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	PO_CHG_INT_EN	2	Port Change Interrupt Enable. When this bit is set to '1', and the Port Change Detect bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt.	
	USBERR_INT_EN	1	USB Error Interrupt Enable. When this bit is set to '1', and the USBERRINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
	USB_INT_EN	0	USB Interrupt Enable. When this bit is set to '1', and the USBINT bit in the USBSTS register is set to '1' also, the Host Controller will issue an interrupt at the next interrupt threshold.	
0Ch ~ 0Dh (2419h ~ 241Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
0Eh (241Ch)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRINDEX[7:0]	7:0	Frame Index. This register is used by the Host Controller to index the frame into the Periodic Frame List. It updates every 125 microseconds. This register cannot be written unless the Host Controller is in the Halted state.	
0Eh (241Dh)	**FRINDEX**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRINDEX[13:8]	5:0	See description of '1Ch'.	
0Fh ~ 12h (241Eh ~ 2424h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
12h (2425h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[15:12]	7:4	Periodic Frame List Base Address. This register contains the beginning address of the Periodic Frame List in the system memory. These bits correspond to memory address signals [31:12].	
	-	3:0	Reserved	
13h (2426h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[23:16]	7:0	See description of '25h'.	
13h (2427h)	**PERIODICLISTBASE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PERI_BASADR[31:24]	7:0	See description of '25h'.	
14h (2428h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[7:5]	7:5	Current Asynchronous List Address. This register contains the address of the next asynchronous queue head to be executed. These bits correspond to memory address signals [31:5].	
	-	4:0	Reserved.	
14h (2429h)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[15:8]	7:0	See description of '28h'.	
15h (242Ah)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[23:16]	7:0	See description of '28h'.	
15h (242Bh)	**ASYNCLISTADDR**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASYNC_LADR[31:24]	7:0	See description of '28h'.	
16h ~ 17h (242Ch ~ 242Fh)		**7:0**	**Default : -**	**Access :-**
	Reserved	7:0	Reserved.	
18h (2430h)	**PORTSC**	**7:0**	**Default : 0x00**	**Access : R/W, R/WC, RO**
	PO_SUSP	7	Port Suspend (R/W). 1: Port is in suspend state. 0: Port is not in suspend state. The Port Enable bit and Suspend bit of this register define the port state as follows: Bits [Port Enable, Suspend] — Port State 0X — Disable 10 — Enable 11 — Suspend	

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
			During the suspend state, downstream propagation of data is blocked on this port, except for port reset. While in the suspend state, the port is sensitive to resume detection. Writing a zero to this bit is ignored by the Host Controller. The Host Controller will unconditionally set this bit to a zero when: • The software sets Force Port Resume bit to a zero (from a one) • The software sets Port Reset bit to a one (from a zero) Note: Before setting this bit, RUN/STOP bit should be set to 0.
	F_PO_RESM	6	Force Port Resume (R/W). 1: Resume detected/driven on port. 0: Not resume detected/driven on port. Software sets this bit to a one to resume signaling. The Host Controller sets this bit to a one if a J-to-K transition is detected while the port is in the suspend state. When this bit transits to a one for the detection of a J-to-K transition, the Port Change Detect bit in USBSTS register is also set to a one.
	-	5:4	Reserved.
	PO_EN_CHG	3	Port Enable/Disable Change (R/WC). 1: Port enable/disable status has changed. 0: No change.
	PO_EN	2	Port Enable/Disable (R/W). 1: Enable. 0: Disable. Ports can only be enabled by the Host Controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field.
	CONN_CHG	1	Connect Status Change (R/WC). 1: Change current connect status. 0: No change. This bit indicates a change has occurred in the port's current connect status.
	CONN_STS	0	Current Connect Status (RO). 1: Device is present on the port. 0: No device is present.

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
			This value reflects the current state of the port, and may not correspond directly to cause the Connect Status Change bit to be set. When TST_FORCEEN is set to '1', this signal is the output of U_HDISCON.
18h (2431h)	**PORTSC**	**7:0**	**Default : 0x00** **Access : R/W, RO**
	-	7:4	Reserved.
	LINE_STS	3:2	Line Status (RO). These bits reflect the current logical levels of the D+ and D- signal lines.
	-	1	Reserved.
	PO_RESET	0	Port Reset. 1: Port is in reset. 0: Port is not in reset. When the software writes a one to this bit, the bus reset sequence as defined in the USB spec. is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence. Note: Before setting this bit, RUN/STOP bit should be set to 0.
19h 2432h	**-**	**7:0**	**Default : 0x00** **Access : R/W**
	-	**7:1**	Reserved.
	FORCE_TST_ENABLE	**0**	Force UHC to enter test mode to issue test packet. The bit must be set before clearing VBUS_OFF. Otherwise it cannot enter test mode successfully.
19h (2433h ~ 2433h)	**-**	**7:0**	**Default : -** **Access : -**
	-	7:0	Reserved.
1Ah (2434h)	**HCMISC**	**7:0**	**Default : 0x40** **Access : R/W**
	-	7	Reserved.
	U_SUSP_N	6	Transceiver Suspend Mode. Active LOW places the transceiver in suspend mode that draws minimal power from power supplies. This is part of the power management.
	EOF2_TIME	5:4	EOF 2 Timing Points, controlling EOF 2 timing point before next SOF. High-Speed EOF2 Time:

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
			00: 2 clocks (30 MHz) = 66ns. 01: 4 clocks (30 MHz) = 133ns. 10: 8 clocks (30 MHz) = 266ns. 11: 16 clocks (30 MHz) = 533ns. Full-Speed EOF2 Time: 00: 20 clocks (30 MHz) = 666ns. 01: 40 clocks (30 MHz) = 1.333us. 10: 80 clocks (30 MHz) = 2.66us. 11: 160 clocks (30 MHz) = 5.3us. Low-Speed EOF2 Time: 00: 40 clocks (30 MHz) = 1.33us. 01: 80 clocks (30 MHz) = 2.66us. 10: 160 clocks (30 MHz) = 5.33us. 11: 320 clocks (30 MHz) = 10.66us.
	EOF1_TIME	3:2	EOF 1 Timing Points, controlling EOF 1 timing point before next SOF. This value should be adjusted according to the maximum packet size. High Speed EOF1 Time: 00: 540 clocks (30 MHz) = 18us. 01: 360 clocks (30 MHz) = 12us. 10: 180 clocks (30 MHz) = 6us. 11: 720 clocks (30 MHz) = 24us. Full-Speed EOF1 Time: 00: 1600 clocks (30 MHz) = 53.3us. 01: 1400 clocks (30 MHz) = 46.6us. 10: 1200 clocks (30 MHz) = 40us. 11: 21000 clocks (30 MHz) = 700us. Low-Speed EOF1 Time: 00: 3750 clocks (30 MHz) = 125us. 01: 3500 clocks (30 MHz) = 116us. 10: 3250 clocks (30 MHz) = 108us. 11: 4000 clocks (30 MHz) = 133us.
	ASYN_SCH_SLPT	1:0	Asynchronous Schedule Sleep Timer, controlling the Asynchronous Schedule sleep timer. 00: 5us. 01: 10us. 10: 15us. 11: 20us.
1Ah ~ 1Fh	**-**	**7:0**	**Default : -** **Access : -**

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
(2435h ~ 243Fh)	-	7:0	Reserved.	
20h (2440h)	**BMCS**	**7:0**	**Default : 0x10**	**Access : R/W**
	FORCE_NO_CHIRP	7	Force Full/Low speed mode.	
	-	6:5	Reserved (must be set to '0' at all times).	
	VBUS_OFF	4	VBUS Off. This bit controls the voltage on VBUS ON/OFF (default is OFF) or in other words, the signal U_DRVBUS. 0: VBUS On. 1: VBUS Off.	
	INT_POLARITY	3	Control the polarity of system interrupt signal SYS_INT_N. 0: Active LOW (default). 1: Active HIGH.	
	HALF_SPEED	2	Half Speed Enable. 1: FIFO controller asserts ACK to DMA once every two clock cycles. 0: FIFO controller asserts ACK to DMA continuously. This bit is set to '1' while implementing FPGA.	
	HDISCON_FLT_SEL	1	Select a timer to filter out noise of HDISCON from UTMI+. 0: Approximated to 135 us. 1: Approximated to 270 us.	
	VBUS_FLT_SEL	0	Select a timer to filter out noise of VBUS_VLD from UTMI+. This signal is valid when signal U_VBUSVLD is connected. 0: Approximated to 135 us. 1: Approximated to 472 us.	
20h (2441h)	**BMCS**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	HOST_SPD_TYP	2:1	Host Speed Type, indicating speed type of the attached device. 10: HS. 00: FS. 01: LS. 11: Reserved.	
	VBUS_VLD	0	VBUS Valid. When the voltage on VBUS is above the valid VBUS	

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			threshold, this signal is valid when U_VBUSVLD is connected.	
21h (2442h ~ 2443h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
22h (2444h)	**BUSMONINTSTS**	**7:0**	**Default : 0x00**	**Access : R/WC**
	-	7:5	Reserved.	
	DMA_ERROR	4	DMA Error Interrupt. DMA operation cannot be finished normally, and an error signal is received. When CPU initiates DMA to fill up or read out device's FIFO, and DMA controller gets error response from system bus, this bit will be set. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DMA_CMPLT	3	DMA Completion Interrupt. DMA operation is finished normally. When CPU initiates DMA to fill up or read out device's FIFO, this bit will be set after mission completion. This bit can only be cleared by firmware. It is not affected by USB bus reset.	
	DPLGRMV	2	Device Plug Remove. This register is set to '1' once the device plug is removed. Writing '1' clears this register and writing '0' takes no effect.	
	OVC	1	Over Current Detection. This register is set to '1' when the VBUS does not reach VBUS_VLD within the expected time. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
	VBUS_ERR	0	VBUS Error. This register is set to '1' when the Bus Monitor state machine moves to "VBUS_ERROR" state. Writing '1' clears this register and writing '0' takes no effect. This signal is valid when signal U_VBUSVLD is connected.	
22h ~ 23h (2445h ~ 2447h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
24h	**BUSMONINTEN**	**7:0**	**Default : 0x00**	**Access : R/W**

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
(2448h)	-	7:5	Reserved.
	DMA_ERROR_EN	4	DMA_ERROR interrupt enable.
	DMA_CMPLT_EN	3	DMA_CMPLT interrupt enable.
	BPLGRMV_EN	2	BPLGRMV interrupt enable.
	OVC_EN	1	OVC interrupt enable.
	A_VBUS_ERR_EN	0	A_VBUS_ERR interrupt enable.
24h ~ 27h (2449h ~ 244Fh)	**-**	**7:0**	**Default : -** **Access : -**
	-	7:0	Reserved.
28h (2450h)	**TST**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:5	Reserved.
	TST_LOOPBK	4	FIFO Loop Back Mode. A '1' turns on the loop-back mode. When this bit is set to '1', the Host Controller will enter the loop-back mode. During the loop-back mode, the Host Controller will use manual setting of DMA control to trigger DMA master.
	TST_MOD	3	Test Mode. A '1' turns on the test mode. When this bit is set to '1', the Host Controller will enter the test mode. This test mode can save simulation time. In normal mode, the Host Controller uses a counter for 10 ms detection of USB reset. The count is a large number. In test mode, the Host Controller will use a smaller number counter for USB reset detection to save the test cycle on test machine.
	TST_PKT	2	Test Mode for Packet. Upon writing a '1' to this bit, the Host Controller repetitively sends the packet defined in UTMI spec. to transceiver. Run/Stop bit should also be enabled to enable the function.
	TST_KSTA	1	Upon writing a '1', the D+/D- is set to the high-speed K state.
	TST_JSTA	0	Upon writing a '1', the D+/D- is set to the high-speed J state.
28h ~ 37h	**-**	**7:0**	**Default : -** **Access : -**

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
(2451h ~ 246Fh)	-	7:0	Reserved.	
38h (2470h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DMA_IO	3	DMA IO to IO. Force DMA Controller not to toggle address. This bit is set when the DMA target is not a system memory but an IO device. If this register is set to '1', the 'DMA_LEN' must be an integer multiple of DWORD (4 byes), and the 'DMA_MADDR' must align to the boundary of DWORD (4 bytes).	
	-	2	Reserved.	
	DMA_TYPE	1	DMA Type, the transfer type of data moving. 0: FIFO to Memory. 1: Memory to FIFO.	
	DMA_START	0	DMA Start, informing DMA Controller to initiate DMA transfer. This bit is set to start the transfer and cleared when the DMA operation is completed. Note that this bit cannot be cleared by software; it can only be cleared by hardware in the case of either DMA completion or DMA error. Note that if DMA_LEN and DMA_START are set at the same time, the DMA_LEN will take effect immediately.	
38h (2471h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[7:0]	7:0	DMA Length. The total bytes the DMA Controller will move. The unit is byte. The maximum length could be 1024B-1.	
39h (2472h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_LEN[15:8]	7:0	See description of '71h'.	
39h (2473h)	**DMACTLPARA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DMA_LEN[16]	0	See description of '71h'.	
3Ah (2474h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[7:0]	7:0	DMA Memory Address. The starting address of memory to request DMA transfer.	

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
3Ah (2475h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[15:8]	7:0	See description of '74h'.	
3Bh (2476h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[23:16]	7:0	See description of '74h'.	
3Bh (2477h)	**DMACTLPARA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_MADDR[31:24]	7:0	See description of '74h'.	
3Ch~3Fh (2478h~247Fh)	-	-	**Default: -**	**Access: -**
	-	-	Reserved.	
40h (2480h)	**PROJ_SPEC_REG0**	7:0	**Default: 0x00**	**Access: R/W, WO**
	DBUS_SELECT	7:5	Select debug bus banks.	
	UTMI_SELECT	4	Select external UTMI.	
	OLD_XI2PV	3	Enable old version XIU access.	
	CLK_STOP	2	Trigger the clock stop mechanism.	
	EN_RD_RD_SCRAMBLE	1	Enable memory inverted read.	
	EN_RD_WR_SCRAMBLE	0	Enable memory inverted write.	
40h (2481h)	**PROJ_SPEC_REG1**	**7:0**	**Default: 0x00**	**Access: R/W**
	SPLIT_SHORT_PKT_CLR_ACT	7	If the transfer is a periodic split transaction, the active status will be cleared when a short packet is received.	
	NON_ALIGN_EN	6	Enable MIU address non-alignment mode. It also means enabling new PV2MI bridge.	
	INVALID_MIU_ACS_INTEN	5	Enable interrupt when MIU invalid write occurs.	
	MIU_WR_PROTECT_EN	4	Enable MIU write protect.	
	DAT_RD_PRI_EN	3	The enable option (MIU priority access) of the "data read".	
	DAT_WR_PRI_EN	2	The enable option (MIU priority access) of the "data write".	
	QT_RD_PRI_EN	1	The enable option (MIU priority access) of the "q-table read".	
	QT_WR_PRI_EN	0	The enable option (MIU priority access) of the "q-table write".	
41h (2482h)	**PROJ_SPEC_REG2**	**7:0**	**Default: 0x00**	**Access: R/W**
	QT_RD_PRI_SEL	7:6	The selection (delay time of MIU priority assert) of the "q-table read".	

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
	QT_WR_PRI_SEL	5:4	The selection (delay time of MIU priority assert) of the "q-table write".	
	DAT_RD_PRI_SEL	3:2	The selection (delay time of MIU priority assert) of the "data read".	
	DAT_RD_PRI_SEL	1:0	The selection (delay time of MIU priority assert) of the "data write".	
41h (2483h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	7:0	Reserved.	
42h (2484h)	**FDBUS_REG0**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[7:0]	7:0	Internal bus for debugging.	
42h (2485h)	**FDBUS_REG1**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[15:8]	7:0	Internal bus for debugging.	
43h (2486h)	**FDBUS_REG2**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[23:16]	7:0	Internal bus for debugging.	
43h (2487h)	**FDBUS_REG3**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[31:24]	7:0	Internal bus for debugging.	
44h (2488h)	**FDBUS_REG4**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[39:32]	7:0	Internal bus for debugging.	
44h (2489h)	**FDBUS_REG5**	**7:0**	**Default: 0x00**	**Access: RO**
	fusbh200_dbus[47:40]	7:0	Internal bus for debugging.	
45h (248Ah)	**STATUS_REG**	**7:0**	**Default: 0x00**	**Access: R/W1C**
	-	7:1	Reserved.	
	INVALID_MIU_ACS	0	Interrupt status of invalid MIU write.	
45h (248B)	**-**	**7:0**	**Default: -**	**Access: -**
		7:0	Reserved.	
46h (248Ch)	**MIU_WRITE_RANGE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[7:0]	7:0	MIU write protect lower boundary address[7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
46h (248Dh)	**MIU_WRITE_RANGE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[15:8]	7:0	MIU write protect lower boundary address[15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower	

UHC0 Register (Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
			boundary address.	
47h (248Eh)	**MIU_WRITE_RANGE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOWER_BOUND[23:16]	7:0	MIU write protect lower boundary address[23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
47h (248Fh)	**MIU_WRITE_RANGE3**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[7:0]	7:0	MIU write protect upper boundary address[7:0]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
48h (2490h)	**MIU_WRITE_RANGE4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[15:8]	7:0	MIU write protect upper boundary address[15:8]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
48h (2491h)	**MIU_WRITE_RANGE5**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND[23:16]	7:0	MIU write protect upper boundary address[23:16]: MIU write will be an invalid access if the write address is above the upper boundary address or below the lower boundary address.	
49h~7Fh (2492h ~ 24FFh)	-	-	**Default: -**	**Access: R/W**
	-	-	Reserved.	

ATOP Register (Bank = 25)

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2500h)	**REG2500**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	VD_AMUX	6	0/1=select ADC RGB/CYU for VD.	
	VD_RGB_EN	5	1=enable ADC RGB/CYU for SCART RGB fast blanking function.	
	VD_YC_EN	4	1=enable S-Video input function.	
	VD_EN	3	1=enable VD function.	
	DVI_EN	2	1=enable DVI function.	
	ADC_ENB	1	1=enable ADC_B RGB function.	
	ADC_ENA	0	1=enable ADC_A RGB function.	
01h (2502h)	**REG2502**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	AMUXB[1:0]	3:2	Select ADC_B RGB channel, VDA FB mode RGB channel. 00: Select input channel 0 for ADCB. 01: Select input channel 1 for ADCB. 10: Select input channel 2 for ADCB.	
	AMUXA[1:0]	1:0	Select ADC_A RGB channel, VDB FB mode RGB channel. 00: Select input channel 0 for ADCA. 01: Select input channel 1 for ADCA. 10: Select input channel 2 for ADCA.	
02h (2504h)	**REG2504**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VD_CMUX[3:0]	7:4	Select VD SC channel. 0000=CVBS0. 0001=CVBS1. 0010=CVBS2. 0011=CVBS3. 0100=CVBS4(Y0). 0101=CVBS6(Y1). 0110=CVBS5(C0). 0111=CVBS7(C1). 1000=SOG0. 1001=SOG1. 1010=SOG2. Other=none.	

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description
	VD_YMUX[3:0]	3:0	Select VD CVBS/Y channel. 0000=CVBS0. 0001=CVBS1. 0010=CVBS2. 0011=CVBS3. 0100=CVBS4(Y0). 0101=CVBS6(Y1). 0110=CVBS5(C0). 0111=CVBS7(C1). 1000=SOG0. 1001=SOG1. 1010=SOG2. Other=none.
04h (2508h)	**REG2508**	**7:0**	**Default : 0xFF** **Access : R/W**
	PDN_ADCREF	7	1=power down ADC voltage reference.
	PDN_VREF	6	1=power down voltage reference.
	PDN_ADCR	5	1=power down ADC_R.
	PDN_ADCG	4	1=power down ADC_G.
	PDN_ADCB	3	1=power down ADC_B.
	PDN_PHD	2	1=power down phase digitizer.
	PDN_PLL	1	1=power down ADC PLL.
	PDN_DPLBG	0	1=power down DPL bandgap.
04h (2509h)	**REG2509**	**7:0**	**Default : 0xFF** **Access : R/W**
	PDN_ICLP_Y	7	1=power down I-clamp on Y channel.
	PDN_ICLP_C	6	1=power down I-clamp on C channel.
	PDN_ADCU	5	1=power down ADC_U.
	PDN_ADCY	4	1=power down ADC_Y.
	PDN_ADCC	3	1=power down ADC_C.
	PDN_PHD2	2	1=power down VD PLL phase digitalizer.
	PDN_PLL2	1	1=power down VD PLL.
	PDN_DPLBG2	0	1=power down VD PLL band-gap.
05h (250Ah)	**REG250A**	**7:0**	**Default : 0xFF** **Access : R/W**
	PDN_HSYNC[2:0]	7:5	1=power down HSYNC[2:0] comparator.
	GMC_BYPASS	4	1=enable GMC bypass mode.
	PDN_GMC_TUNE	3	1=power down GMC tune.

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PDN_GMC_BIAS	2	1=power down GMC bias circuit.	
	PDN_GMC_Y	1	1=power down GMC on Y channel.	
	PDN_GMC_C	0	1=power down GMC on C channel.	
06h (250Ch)	**REG250C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PD_CLK[7:0]	7:0	Clock power down control. [0]: PD_CLKXTAL. [1]: PD_CLK200. [2]: PD_CLKPLLA. [3]: PD_CLKADCA. [4]: PD_CLKPLLB. [5]: PD_CLKADCB. [6]: PD_CLKD_VD. [7]: PD_CLKGMC. [8]: PD_CLK_DVI. [9]: PD_CLK_HDCP. [10]: PD_AUTO_HDCP. [11]: PD_CLK_HDMI. [12]: PD_AUTO_HDMI. [13]: PD_ICLK. [14]: PD_CLK200_FB. [15]: PD_DVIDETCLK.	
06h (250Dh)	**REG250D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PD_CLK[15:8]	7:0	See description of '250Ch'.	
07h (250Eh)	**REG250E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOFTRST[7:0]	7:0	1=soft reset for adcdvipll blocks. [15:8]: reserved. [7]: Soft-reset atop control. [6]: Soft-reset hdmi. [5]: Soft-reset hdcp. [4]: Soft-reset dvi. [3]: Soft-reset pll_dig_b. [2]: Soft-reset adc_vd. [1]: Soft-reset pll_dig_a. [0]: Soft-reset adc_dig_a.	
07h (250Fh)	**REG250F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SOFTRST[15:8]	7:0	See description of '250Eh'.	
08h	**REG2510**	**7:0**	**Default : 0x76**	**Access : R/W**

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2510h)	MPLL_PDIV	7	Select mpll post divider. 0=div3. 1=div2.5.	
	MPLL_PORST	6	1=mpll power-on reset.	
	MPLL_RESET	5	1=mpll reset.	
	MPLL_PD	4	1=mpll power down.	
	MPLL_VCO_OFFSET	3	Mpll vco offset.	
	MPLL_ICTRL[2:0]	2:0	Mpll current control.	
08h (2511h)	**REG2511**	**7:0**	**Default : 0x0D**	**Access : RO, R/W**
	-	7:6	Reserved.	
	MPLL_HV_FLAG	5	Mpll vco high supply voltage flag.	
	MPLL_LOCK	4	Mpll lock status.	
	MPLL_PD_VIFCLK	3	1=power down mpll output divider clock for VIF ADC.	
	MPLL_MCU_SEL[2:0]	2:0	Select mpll post divider for mcu clock, 000:MPLL_CLK/2. 001: /2.5. 010: /3. 011: /3.5. 100: /4. 101: /8.	
09h (2512h)	**REG2512**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	MPLL_OUTPUT_DIV1[1:0]	5:4	Select mpll output first divider, 00=div1, 01=div2, 10=div4, 11=div8.	
	MPLL_LOOP_DIV1[1:0]	3:2	Select mpll loop first divider, 00=div1, 01=div2, 10=div4, 11=div8.	
	MPLL_INPUT_DIV1[1:0]	1:0	Select mpll input first divider, 00=div1, 01=div2, 10=div4, 11=div8.	
09h (2513h)	**REG2513**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPLL_INPUT_DIV2[7:0]	7:0	Select mpll input second divider, 0,1=div1, N=divN.	
0Ah (2514h)	**REG2514**	**7:0**	**Default : 0x24**	**Access : R/W**
	MPLL_LOOP_DIV2[7:0]	7:0	Select mpll loop second divider, 0,1=div1, N=divN.	
0Ah (2515h)	**REG2515**	**7:0**	**Default : 0x00**	**Access : R/W**
	MPLL_OUTPUT_DIV2[7:0]	7:0	Select mpll output second divider, 0,1=div1, N=divN.	
0Bh (2516h)	**REG2516**	**7:0**	**Default : 0x3F**	**Access : R/W**
	MPLL_EN_SIFCK_DIV2	7	1=select output mpll sif clock div2.	

ATOP Register (Bank = 25)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	MPLL_EN_SIFCK	6	1=enable output mpll sif adc clock.
	MPLL_OUTDIV_PD[5:0]	5:0	1=power down mpll output divider clocks, [0]=PD USB CLK, [1]=PD DIV7, [2]=PD DIV5, [3]=PD DIV3, [4]=PD DIV2, [5]=PD DIV3.5.
0Bh (2517h)	**REG2517**	**7:0**	**Default : 0x00** **Access : R/W**
	MPLL_TEST[7:0]	7:0	Mpll test registers. [4]: Enable mpll lock detector.
0Ch (2518h)	**REG2518**	**7:0**	**Default : 0x01** **Access : R/W**
	ADC_PLL_EXTCK	7	1=select external clock mode for ADC PLL.
	ADC_PLL_SELBG	6	Select band-gap source for ADC PLL, 0=ADC bandgap, 1=GMC bandgap.
	ADC_PLL_PDIV[2:0]	5:3	ADC PLL clock post divider. b000: Div1. b001: Div2. b011: Div4. b111: Div8. others: Reserved.
	ADC_PLL_MULT[2:0]	2:0	ADC PLL clock multiplier = N+1.
11h (2523h)	**REG2523**	**7:0**	**Default : 0x00** **Access : RO**
	-	7:5	Reserved.
	ADC_PLL_STATUS[4:0]	4:0	Adc pll detector status. [4]: DPL_HV_FLAG. [3]: DPL_LOCK. [2]: DPL_FLAG. [1]: DPL_DUTYH. [0]: DPL_DUTYL.
12h (2524h)	**REG2524**	**7:0**	**Default : 0x01** **Access : R/W**
	VD_PLL_EXTCK	7	1=select external clock mode for VD(ADCB) PLL.
	VD_PLL_SELBG	6	Select band-gap source for VD(ADCB) PLL, 0=GMC bandgap, 1=ADC bandgap.
	VD_PLL_PDIV[2:0]	5:3	VD(ADCB) PLL clock post divider. b000: Div1. b001: Div2. b011: Div4. b111: Div8. others: Reserved.
	VD_PLL_MULT[2:0]	2:0	VD(ADCB) PLL clock multiplier = N+1.

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
17h (252Fh)	**REG252F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	VD_PLL_STATUS[4:0]	4:0	VD(ADCB) pll detector status. [4]: DPL_HV_FLAG. [3]: DPL_LOCK. [2]: DPL_FLAG. [1]: DPL_DUTYH. [0]: DPL_DUTYL.	
19h (2532h)	**REG2532**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	ADC_ENC_OV	6	1=override ADC offset cancel mode by register.	
	ADC_ENC[5:0]	5:0	Enable ADC offset cancel mode for VD. [5]=U. [4]=Y. [3]=C. [2]=B. [1]=G. [0]=R.	
19h (2533h)	**REG2533**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	ADC_GSHIFT_OV	6	1=override ADC gain shift by register.	
	ADC_GSHIFT[5:0]	5:0	Override enable ADC gain shift. [5]=U. [4]=Y. [3]=C. [2]=B. [1]=G. [0]=R.	
1Ah (2534h)	**REG2534**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	ADC_VCTRL_RGB[2:0]	5:3	ADC voltage control for ADC_RGB.	
	ADC_IBIAS_RGB[2:0]	2:0	Select ADC main bias current for ADC_RGB.	
1Bh	**REG2536**	**7:0**	**Default : 0x55**	**Access : R/W**

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2536h)	ADC_ICTRL_RGB[7:0]	7:0	ADC RGB bias current control. [13:12]: ADC reference buffer bias current control. [11:10]: ADC input buffer current control. [9:8]: ADC PGA bias current control. [7:6]: ADC 1st stage bias current control. [5:4]: ADC 2nd stage bias current control. [3:2]: ADC 3rd stage bias current control. [1:0]: ADC 4th stage bias current control.	
1Bh (2537h)	**REG2537**	**7:0**	**Default : 0x15**	**Access : R/W**
	-	7:6	Reserved.	
	ADC_ICTRL_RGB[13:8]	5:0	See description of '2536h'.	
1Ch (2538h)	**REG2538**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:6	Reserved.	
	SOG_DISA	5	1=disable active SOG comparator.	
	SOG_THA[4:0]	4:0	Select SOG comparator threshold, step=10mv.	
1Ch (2539h)	**REG2539**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADCBWA[3:0]	7:4	Select ADC input filter bandwidth. 0000: 260MHz. 0001: 190MHz. 0010: 150MHz. 0011: 120MHz. 0100: 60MHz. 0101: 30MHz. 0110: 25MHz. 0111: 23MHz. 1000: 21MHz. 1001: 20MHz. 1010: 18MHz. 1011: 17MHz. 1100: 16MHz. 1101: 15MHz. 1110: 14MHz. 1111: 6MHz.	
	SOG_OPTFIRA	3	0/1=disable/enable SOG input low bandwidth filter.	
	SOG_BWA[2:0]	2:0	Select SOG input filter bandwidth.	
1Dh (253Ah)	**REG253A**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADC_VCTRL_YC[2:0]	5:3	ADC voltage control for ADC_YC.	
	ADC_IBIAS_YC[2:0]	2:0	Select ADC main bias current for ADC_YC.	
1Eh (253Ch)	**REG253C**	**7:0**	**Default : 0x55**	**Access : R/W**
	ADC_ICTRL_YC[7:0]	7:0	ADC YC bias current control. [13:12]: ADC reference buffer bias current control. [11:10]: ADC input buffer current control. [9:8]: ADC PGA bias current control. [7:6]: ADC 1st stage bias current control. [5:4]: ADC 2nd stage bias current control. [3:2]: ADC 3rd stage bias current control. [1:0]: ADC 4th stage bias current control.	
1Eh (253Dh)	**REG253D**	**7:0**	**Default : 0x15**	**Access : R/W**
	-	7:6	Reserved.	
	ADC_ICTRL_YC[13:8]	5:0	See description of '253Ch'.	
1Fh (253Eh)	**REG253E**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:6	Reserved.	
	SOG_DISB	5	1=disable active SOG comparator.	
	SOG_THB[4:0]	4:0	Select SOG comparator threshold, step=10mv.	
1Fh (253Fh)	**REG253F**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADCBWB[3:0]	7:4	Select ADC input filter bandwidth.	
	SOG_OPTFIRB	3	0/1=disable/enable SOG input low bandwidth filter.	
	SOG_BWB[2:0]	2:0	Select SOG input filter bandwidth.	
20h (2540h)	**REG2540**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HSYNC_LVL[2:0]	2:0	Select HSYNC trigger level.	
20h ~ 22h (2541h ~ 2545h)	**-**	**7:0**	**Default : -**	**Access : -**
		-	Reserved.	
23h (2546h)	**REG2546**	**7:0**	**Default : 0x38**	**Access : R/W**
	-	7	Reserved.	
	CKEXT_SEL	6	0/1=select VSYNC0/VSYNC1 as pll external clock input.	
	XTAL_EN	5	1=enable XTAL pad (obsolete, Hwreset need to pass glitch removal circuit & clocked by XTAL).	
	XTAL_SEL[1:0]	4:3	Select XTAL driving strength.	
	VDD2LO_EN	2	1=enable vdd too low reset.	

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	TST_POR[1:0]	1:0	Power on reset test registers.	
23h (2547h)	**REG2547**	**7:0**	**Default : 0x30**	**Access : R/W**
	XTAL_FREQ[7:0]	7:0	Set XTAL frequency for timing detection normalization (default=12MHz, format=6.2 MHz).	
24h (2548h)	**REG2548**	**7:0**	**Default : 0x00**	**Access : R/W**
	REFDAC0[7:0]	7:0	ADC reference DAC0 output level override value.	
24h (2549h)	**REG2549**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:5	Reserved.	
	REFDAC0_OV	4	1=override ADC refernce DAC0 output.	
	REFDAC0[11:8]	3:0	See description of '2548h'.	
25h (254Ah)	**REG254A**	**7:0**	**Default : 0x00**	**Access : R/W**
	REFDAC1[7:0]	7:0	ADC reference DAC1 output level override value.	
25h (254Bh)	**REG254B**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:5	Reserved.	
	REFDAC1_OV	4	1=override ADC refernce DAC1 output.	
	REFDAC1[11:8]	3:0	See description of '254Ah'.	
26h (254Ch)	**REG254C**	**7:0**	**Default : 0x58**	**Access : R/W**
	-	7	Reserved.	
	REF_SEL_VD	6	Select ADC reference DAC for VD function (perfer DAC1 assigned to VD).	
	REF_SEL[5:0]	5:0	Select ADC reference DAC for ADC {U.Y.C.B.G.R}. 0=DAC0. 1=DAC1.	
26h (254Dh)	**REG254D**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:2	Reserved.	
	RDAC_ICTRL[1:0]	1:0	Select reference DAC bias current.	
28h (2550h)	**REG2550**	**7:0**	**Default : 0x80**	**Access : R/W**
	VD_CGAIN[7:0]	7:0	VD ADC C channel gain control (override).	
28h (2551h)	**REG2551**	**7:0**	**Default : 0x70**	**Access : R/W**
	VD_COFFSET[7:0]	7:0	VD ADC C channel offset control.	
29h (2552h)	**REG2552**	**7:0**	**Default : 0x80**	**Access : R/W**
	VD_YGAIN[7:0]	7:0	VD ADC Y channel gain control (override).	
29h (2553h)	**REG2553**	**7:0**	**Default : 0x70**	**Access : R/W**
	VD_YOFFSET[7:0]	7:0	VD ADC Y channel offset control.	

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
2Ah (2554h)	**REG2554**	**7:0**	**Default : 0x00**	**Access : RO, R/W, WO**
	VD_YGAIN_OV	7	1=override VD ADC_Y gain control.	
	VD_CGAIN_OV	6	1=override VD ADC_C gain control.	
	-	5	Reserved.	
	CLROVF_YC	4	Write an 1 to clear ADC_YC overflow flags.	
	OVF_YC[3:0]	3:0	ADC overflow flags, {OVFY, UNFY, OVFC, UNFC}.	
2Ch (2558h)	**REG2558**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VMID_SELA	6	Select vmid mode. 0=controlled by ADCB gain, 1=constant voltage.	
	BSEL_CVA[1:0]	5:4	Select vclamp voltage for ADC B input. 00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
	GSEL_CVA[1:0]	3:2	Select vclamp voltage for ADC G input. 00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
	RSEL_CVA[1:0]	1:0	Select vclamp voltage for ADC R input. 00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
2Ch (2559h)	**REG2559**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VMID_SELB	6	Select vmid mode. 0=controlled by ADCU gain, 1=constant voltage.	
	BSEL_CVB[1:0]	5:4	Select vclamp voltage for ADCB B input. 00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
	GSEL_CVB[1:0]	3:2	Select vclamp voltage for ADCB G input. 00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
	RSEL_CVB[1:0]	1:0	Select vclamp voltage for ADCB R input. 00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
2Dh (255Ah)	**REG255A**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	ADC_INMSEL	4	0/1=select ADC INM pins, differential/shared mode.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SVCLP[3:0]	3:0	Select GMC VCLAMP voltage level. 0000=1.15V. 0001=1.2V. 0010=0.85V. 0011=0.90V. 0100=0.95V. 0101=1.00V. 0110=1.05V. 0111=1.10V. 1000=0.3V. 1001=0.4V. 1010=0.5V. 1011=0.6V. 1100=0.7V. 1101=0.8V. 111x=0.6V.	
2Dh (255Bh)	**REG255B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FB_RGBCLP	6	0/1=select RGB clamp pulse from VD/ADC for FB mode.	
	CLAMP_YC_OV[1:0]	5:4	Override clamp control for YC, 0x=pulse. 10=disable. 11=force clamp.	
	CLAMP_RGB2_OV[1:0]	3:2	Override clamp control for RGB2, 0x=pulse. 10=disable. 11=force clamp.	
	CLAMP_RGB_OV[1:0]	1:0	Override clamp control for RGB, 0x=pulse. 10=disable. 11=force clamp.	
2Eh (255Ch)	**REG255C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICLP_M1[1:0]	7:6	Select I-clamp current range for Y channel.	
	ICLP_M0[1:0]	5:4	Select I-clamp current range for C channel.	
	SEL_ICLAMP[3:0]	3:0	Select I-clamp bias current.	
30h (2560h)	**REG2560**	**7:0**	**Default : 0x01**	**Access : R/W**
	GMC_UPD_SEL	7	Select GMC update during 0=VSYNC. 1=HSYNC.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GMC_STS_SEL	6	Select GMC status. 0=GMC control code. 1=GMC tuning code.	
	GMC_HOLD	5	1=hold current GMC control.	
	GMC_UPDA	4	1=always update GMC control.	
	GMC_HYS_TH[3:0]	3:0	Select GMC update hysteresis threshold.	
30h (2561h)	**REG2561**	**7:0**	**Default : 0x08**	**Access : R/W**
	GMC_ACC_TH[7:0]	7:0	Select accumulator threshold for GMC control update.	
31h (2562h)	**REG2562**	**7:0**	**Default : 0x00**	**Access : RO**
	GMC_STATUS[7:0]	7:0	GMC tuning status. [8]: Comparator output. [7:0]: GMC control/tuning code.	
31h (2563h)	**REG2563**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	GMC_STATUS[8]	0	See description of '2562h'.	
32h (2564h)	**REG2564**	**7:0**	**Default : 0x00**	**Access : R/W**
	GMC_TUNE_OV[7:0]	7:0	Override GMC tuning code by register. [8]: 1=override enable. [7:0]: override value.	
32h (2565h)	**REG2565**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GMC_TUNE_OV[8]	0	See description of '2564h'.	
33h (2566h)	**REG2566**	**7:0**	**Default : 0x00**	**Access : R/W**
	GMC_CTRL_OV[7:0]	7:0	Override GMC control code by register. [8]: 1=override enable. [7:0]: override value.	
33h (2567h)	**REG2567**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GMC_CTRL_OV[8]	0	See description of '2566h'.	
34h (2568h)	**REG2568**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:6	Reserved.	
	GMC_CKDIV[5:0]	5:0	Select divider down ratio for GMC clock, clock div=2N+2.	
34h (2569h)	**REG2569**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AGC_GMC_1ST	6	1=use GMC gain 2X first when tuning AGC.	
	GMC_YGAIN_OV[2:0]	5:3	1=override GMC gain on Y channel. 0xx: Auto. 100=1X. 101=2X. 11x=4X.	
	GMC_CGAIN_OV[2:0]	2:0	1=override GMC gain on C channel. 0xx: Auto. 100=1X. 101=2X. 11x=4X.	
35h (256Ah)	**REG256A**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTVCMM[7:0]	7:0	GMC common mode voltage test mode.	
35h (256Bh)	**REG256B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTVCMO[7:0]	7:0	GMC reserved registers.	
36h (256Ch)	**REG256C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTGMC_C[7:0]	7:0	GMC test registers for C channel.	
36h (256Dh)	**REG256D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTGMC_Y[7:0]	7:0	GMC test registers for Y channel.	
37h (256Eh)	**REG256E**	**7:0**	**Default : 0x00**	**Access : R/W**
	TST_GMC_TUNE[7:0]	7:0	GMC tune test register.	
37h (256Fh)	**REG256F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TST_GMC_TUNE[8]	0	See description of '256Eh'.	
38h (2570h)	**REG2570**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7	Reserved.	
	CVBSO_MUXEN[2:0]	6:4	CVBS buffer input channel enable. [6]: 1=CP channel enable. [5]: 1=YN channel enable. [4]: 1=YP channel enable.	
	PDN_CVBSO_CPOS	3	1=CP channel clamp power down.	
	PDN_CVBSO_YPOS	2	1=YP channel clamp power down.	
	PDN_CVBSO_LSH	1	1=power down CVBS output buffer level shift.	
	PDN_CVBSO	0	1=power down CVBS output buffer.	
39h	**REG2572**	**7:0**	**Default : 0x00**	**Access : R/W**

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2572h)	CVBSO_YNMUX[3:0]	7:4	Select YN channel input. 0000=VCOM0. 0001=VCOM1. 0010=VCOM1. 0011=VCOM1. 0100=VCOM2. 0101=VCOM2. 0110=VCOM2. 0111=VCOM2. 1000=VCOM2. 1001=VCOM2. 1010=VCOM2. 1011=CVBS_DACM.	
	CVBSO_YPMUX[3:0]	3:0	Select YP channel input. 0000=CVBS0. 0001=CVBS1. 0010=CVBS2. 0011=CVBS3. 0100=CVBS4(Y0). 0101=CVBS5(C0). 0110=CVBS6(Y1). 0111=CVBS7(C1). 1000=SOG0. 1001=SOG1. 1010=SOG2. 1011=CVBS DAC.	
39h (2573h)	**REG2573**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CVBSO_CPMUX[3:0]	3:0	Select CP channel input. 0000=CVBS0. 0001=CVBS1. 0010=CVBS2. 0011=CVBS3. 0100=CVBS4(Y0). 0101=CVBS5(C0). 0110=CVBS6(Y1). 0111=CVBS7(C1). 1000=SOG0. 1001=SOG1. 1010=SOG2. 1011=CVBS DAC.	
3Ah (2574h)	**REG2574**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CVBSO_ISINK[2:0]	5:3	Select CVBSO clamp sink current.	
	CVBSO_HISOURCE	2	1=enable CVBSO clamp high sourcing current.	
	CVBSO_CBW[1:0]	1:0	C channel clamp bandwidth.	
3Bh ~ 3Bh (2576h ~ 2577h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Ch (2578h)	**REG2578**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7	Reserved.	
	CVBSO2_MUXEN[2:0]	6:4	CVBS buffer input channel enable. [6]: 1=CP channel enable. [5]: 1=YN channel enable. [4]: 1=YP channel enable.	
	PDN_CVBSO2_CPOS	3	1=CP channel clamp power down.	
	PDN_CVBSO2_YPOS	2	1=YP channel clamp power down.	
	PDN_CVBSO2_LSH	1	1=power down CVBS output buffer level shift.	
	PDN_CVBSO2	0	1=power down CVBS output buffer.	
3Dh	**REG257A**	**7:0**	**Default : 0x00**	**Access : R/W**

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(257Ah)	CVBSO2_YNMUX[3:0]	7:4	Select YN channel input. 0000=VCOM0. 0001=VCOM1. 0010=VCOM1. 0011=VCOM1. 0100=VCOM2. 0101=VCOM2. 0110=VCOM2. 0111=VCOM2. 1000=VCOM2. 1001=VCOM2. 1010=VCOM2. 1011=CVBS_DACM.	
	CVBSO2_YPMUX[3:0]	3:0	Select YP channel input. 0000=CVBS0. 0001=CVBS1. 0010=CVBS2. 0011=CVBS3. 0100=CVBS4(Y0). 0101=CVBS5(C0). 0110=CVBS6(Y1). 0111=CVBS7(C1). 1000=SOG0. 1001=SOG1. 1010=SOG2. 1011=CVBS DAC.	
3Dh (257Bh)	**REG257B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CVBSO2_CPMUX[3:0]	3:0	Select CP channel input. 0000=CVBS0. 0001=CVBS1. 0010=CVBS2. 0011=CVBS3. 0100=CVBS4(Y0). 0101=CVBS5(C0). 0110=CVBS6(Y1). 0111=CVBS7(C1). 1000=SOG0. 1001=SOG1. 1010=SOG2. 1011=CVBS DAC.	
3Eh (257Ch)	**REG257C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CVBSO2_ISINK[2:0]	5:3	Select CVBSO clamp sink current.	
	CVBSO2_HISOURCE	2	1=enable CVBSO clamp high sourcing current.	
	CVBSO2_CBW[1:0]	1:0	C channel clamp bandwidth.	
40h (2580h)	**REG2580**	**7:0**	**Default : 0x40**	**Access : R/W**
	FBLANK_CKINV	7	1=invert fast blanking ADC sampling clock.	
	PDN_FBLANK	6	1=power down fast blanking ADC.	
	FBLANK_SEL[1:0]	5:4	Select fast blanking input 00=none. 01=FB input 0. 10=FB input 1. 11=FB input 2.	
	FBLANK_GX[3:0]	3:0	Select fast blanking ADC gain.	
42h (2584h)	**REG2584**	**7:0**	**Default : 0x00**	**Access : R/W**
	FB_MODE[1:0]	7:6	Select fast blanking mixing mode. 00=off. 01=blending by reg. 10=bi-level. 11=blending by FB.	
	FB_CSC_EN	5	1=enable RGB input color space conversion before fast flanking.	
	FB_SRST	4	1=software reset fast blanking down sample block.	
	CSDOWN_168	3	1=enable down sampling RGB input from 16 fsc to 8 fsc.	
	CSDOWN_84	2	1=enable down sampling RGB input from 8 fsc to 4 fsc.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FB_DTHR[1:0]	1:0	1=enable dither for down sampling. [1]: Dither for 16-to-8 down sample. [0]: Dither for 8-to-4 down sample.	
43h (2586h)	**REG2586**	**7:0**	**Default : 0x00**	**Access : R/W**
	FB_FINE_DLY[1:0]	7:6	Select FB input fine delay.	
	FB_PG_DLY[5:0]	5:0	Select FB input pipe delay. Use as FB value for register mode.	
43h (2587h)	**REG2587**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_FINE_DLY[1:0]	7:6	Select RGB input fine delay.	
	RGB_PG_DLY[5:0]	5:0	Select RGB input pipe delay.	
44h (2588h)	**REG2588**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FB_DOFFS[5:0]	5:0	Fast blanking input digital offset adjust (0.6).	
44h (2589h)	**REG2589**	**7:0**	**Default : 0x44**	**Access : R/W**
	FB_DGAIN[7:0]	7:0	Fast blanking input digital gain adjust (2.6).	
45h (258Ah)	**REG258A**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	FB_BILTH[5:0]	5:0	Select fast blanking active threshold for bi-level mode.	
45h (258Bh)	**REG258B**	**7:0**	**Default : 0x00**	**Access : RO, WO**
		7:6	Reserved.	
	FB_ACT_CLR	5	Write an 1 to clear FB_ACT flag.	
	FB_ACT_FLAG	4	Fast blanking input active status (sticky flag).	
	FBLANK_DOUT[3:0]	3:0	Fast blank input value status.	
46h (258Ch)	**REG258C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CVBS_DAC_EN	7	1=enable CVBS DAC.	
	CVBS_DAC_SEL	6	Select CVBS DAC input sources. 0: From video encoder. 1: From VIF decoder.	
	CVBS_DAC_CLK_INV	5	CVBS DAC clock invert enable. 0: Disable clock invert. 1: Enable clock invert.	
	RESERVED_46H	4	Reserved.	
	-	3:0	Reserved.	
46h	**REG258D**	**7:0**	**Default : 0x00**	**Access : R/W**

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
(258Dh)	CVBS_DAC_GAIN[3:0]	7:4	CVBS DAC gain control.	
	CVBS_DAC_OFFSET[3:0]	3:0	CVBS DAC offset control.	
47h (258Eh)	**REG258E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	ADCBW_CU_OREN	1	ADC CU input filter bandwidth overwrite enable. 0: ADC CU input filter bandwidth controlled by REG_ADCBWA. 1: ADC CU input filter bandwidth controlled by REG_ADCBW_RB_OV.	
	ADCBW_RB_OREN	0	ADC RB input filter bandwidth overwrite enable. 0: ADC RB input filter bandwidth controlled by REG_ADCBWA. 1: ADC RB input filter bandwidth controlled by REG_ADCBW_RB_OV.	
47h (258Fh)	**REG258F**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADCBW_CU_OV[3:0]	7:4	ADC CU input filter bandwidth overwrite.	
	ADCBW_RB_OV[3:0]	3:0	ADC RB input filter bandwidth overwrite.	
48h (2590h)	**REG2590**	**7:0**	**Default : 0x03**	**Access : R/W**
		7:2	Reserved.	
	PDN_MODULE	1	1: Power down 2nd reference module.	
	PDN_VCLP	0	1: Power down vclp reference voltage.	
4Ch (2598h)	**REG2598**	**7:0**	**Default : 0x00**	**Access : RO, R/W, WO**
	SAR2_DONE	7	1=SAR one-shot mode done status.	
	SAR2_TRIG	6	Write an 1 to restart SAR conversion.	
	SAR2_EN	5	0/1=power-down/enable SAR ADC.	
	SAR2_FREERUN	4	Select SAR ADC operation mode. 0=one-shot. 1=freerun mode.	
	SAR2_CH_EN[3:0]	3:0	Channel enable bit for SAR[3:0] inputs.	
4Ch (2599h)	**REG2599**	**7:0**	**Default : 0x04**	**Access : R/W**
	SAR2_PERIOD[7:0]	7:0	SAR ADC input sampling pulse duration.	
4Dh (259Ah)	**REG259A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	SAR2_DATA0[5:0]	5:0	SAR ADC channel 0 data.	
4Dh	**REG259B**	**7:0**	**Default : 0x00**	**Access : RO**

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(259Bh)	-	7:6	Reserved.	
	SAR2_DATA1[5:0]	5:0	SAR ADC channel 1 data.	
4Eh (259Ch)	**REG259C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	SAR2_DATA2[5:0]	5:0	SAR ADC channel 2 data.	
4Eh (259Dh)	**REG259D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	SAR2_DATA3[5:0]	5:0	SAR ADC channel 3 data.	
4Fh (259Eh)	**REG259E**	**7:0**	**Default : 0x01**	**Access : R/W**
	SAR2_TEST[7:0]	7:0	SAR ADC test registers. [9:8]: select SAR ADC Bandwidth; 00=1MHz; 01=500KHz; 10=100KHz; 11=50KHz. [7:6]: select SAR ADC current; 00=100%; 01=120%; 10=150%; 11=300%. [5]: 1=connect SAR ADC Input to Vref. [4:3]: SAR clock main divider; 00=4; 01=16; 10=64; 11=256. [2:0]: SAR clock sub divider; 000=2; 001=3; 010=4; 011=5; 100=6; 101=7; 110=8; 111=10.	
4Fh (259Fh)	**REG259F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SAR2_TEST[9:8]	1:0	See description of '259Eh'.	
50h (25A0h)	**REG25A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ID_THL[5:0]	5:0	Select SCART function select switch (FSSW) low threshold.	
50h (25A1h)	**REG25A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ID_THH[5:0]	5:0	Select SCART function select switch (FSSW) high threshold.	
51h (25A2h)	**REG25A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	ID1_EN	7	1=enable ID1 change detect.	
	ID1_SEL[2:0]	6:4	0~3: reserved. 4~7: select SAR2[0:3] as ID1 source.	
	ID0_EN	3	1=enable ID0 change detect.	
	ID0_SEL[2:0]	2:0	0~3: reserved. 4~7: select SAR2[0:3] as ID0 source.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
51h (25A3h)	**REG25A3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCART_ID1[1:0]	3:2	SCART ID1 level status.	
	SCART_ID0[1:0]	1:0	SCART ID0 level status.	
54h (25A8h)	**REG25A8**	**7:0**	**Default : 0xC8**	**Access : R/W**
	ATTEN_CLPENR	7	1=force a clamp duration when attenuator on.	
	ATTEN_CLPENF	6	1=force a clamp duration when attenuator off.	
	ATTEN_CLPDUR[5:0]	5:0	Select clamp duration when switch from/to attenuator, N*1024 CLKFSC.	
54h (25A9h)	**REG25A9**	**7:0**	**Default : 0x40**	**Access : R/W**
	ATTEN_SWDLY[1:0]	7:6	Select enable attenuator to switch mux delay, N*64 CLKFSC.	
	ATTEN_OV[5:0]	5:0	Override CVBS input attenuator. [5]: Override attenuator Y enable. [4]: Enable attenuator Y input mux. [3]: Enable attenuator Y. [2]: Override attenuator C enable. [1]: Enable attenuator C input mux. [0]: Enable attenuator C.	
55h (25AAh)	**REG25AA**	**7:0**	**Default : 0x08**	**Access : RO, R/W**
		7	Reserved.	
	AGC_COARSE[2:0]	6:4	VD coarse gain status.	
	ATTEN_SYCLP[3:0]	3:0	Select clamp level when attenuator enable.	
56h (25ACh)	**REG25AC**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATTEN_TSTC[7:0]	7:0	VD_C input attenuator test registers.	
56h (25ADh)	**REG25AD**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATTEN_TSTY[7:0]	7:0	VD_Y input attenuator test registers.	
5Ah (25B4h)	**REG25B4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RAMP_EN	6	1=enable ramp counter.	
	RAMP_VREF1	5	1=enable ramp counter to VREF_DAC1.	
	RAMP_VREF0	4	1=enable ramp counter to VREF_DAC0.	
	RAMP_DIV[3:0]	3:0	Select ramp speed divider. 2^N - 1.	

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
5Bh (25B6h)	**REG25B6**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATOP_RESERVED[7:0]	7:0	Atop reserved registers.	
5Bh (25B7h)	**REG25B7**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATOP_RESERVED[15:8]	7:0	See description of '25B6h'.	
5Ch (25B8h)	**REG25B8**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATOP_RESERVED[23:16]	7:0	See description of '25B6h'.	
5Ch (25B9h)	**REG25B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATOP_RESERVED[31:24]	7:0	See description of '25B6h'.	
5Dh (25BAh)	**REG25BA**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIF_TST[7:0]	7:0	VIF test register.	
60h (25C0h)	**REG25C0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PDN_DVIPLL	7	1=power down DVI PLL.	
	PDN_DVIPLLBG	6	1=power down DVI PLL band-gap.	
	PDN_DVIPLLREG	5	1=power down DVI PLL regulator.	
	PDN_DMIBEX	4	1=power down DVI output bias current.	
	PDN_DVICK	3	1=power down DVI clock receiver.	
	PDN_DM[2:0]	2:0	1=power down DVI de-multiplexer.	
60h (25C1h)	**REG25C1**	**7:0**	**Default : 0x7F**	**Access : R/W**
	-	7	Reserved.	
	PDN_DVIRCK[1:0]	6:5	1=power down DVI clock channels pull-up resistors.	
	PDN_DVIPD[1:0]	4:3	1=power down DVI data channels pull-up resisitors.	
	PDN_DPLMXR[2:0]	2:0	1=power down DPL mixer [2:0].	
61h (25C2h)	**REG25C2**	**7:0**	**Default : 0x35**	**Access : R/W**
	-	7	Reserved.	
	BBEN	6	1=BBEN mode.	
	DM_MODE_OV[1:0]	5:4	Override DM operation mode. 0x=auto. 10=high speed option mode. 11=normal mode.	
	SWCKB	3	1=enable CLKB input switch.	
	SWCKA	2	1=enable CLKA input switch.	
	SWB	1	1=enable DATA_B input switch.	
	SWA	0	1=enable DATA_A input switch.	

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
61h (25C3h)	**REG25C3**	**7:0**	**Default : 0x10**	**Access : R/W**
	HR_SEL[2:0]	7:5	Select DVI pull-up resistor.	
	DVI_RCTRL[4:0]	4:0	DVI termination resistor control.	
67h (25CEh)	**REG25CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DVI_DPL_TST[50:48]	2:0	See description of '25C8h'.	
68h (25D0h)	**REG25D0**	**7:0**	**Default : 0xC0**	**Access : RO, R/W**
	HOTPLUG_OEN[1:0]	7:6	0=hotplug GPIO[1:0] output enable.	
	HOTPLUG[1:0]	5:4	Write HOTPLUG GPIO[1:0] output value. Read HOTPLUG GPIO[1:0] input value.	
	DVI_DPL_STATUS[3:0]	3:0	DVI DPL detector status. [3]: DVIPLL_LOCK. [2]: DVIPLL_FLAG. [1]: DVIPLL_DUTYH. [0]: DVIPLL_DUTYL.	
70h (25E0h)	**REG25E0**	**7:0**	**Default : 0x00**	**Access : RO**
	ADCDVI_IRQ_STATUS[7:0]	7:0	ADCDVI IRQ status. {0, SCART_ID1_CHG, SCART_ID0_CHG, HDMI_MODE_CHG, DVI_CK_CHG}.	
70h (25E1h)	**REG25E1**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADCDVI_IRQ_MASK[7:0]	7:0	ADCDVI IRQ mask control.	
71h (25E2h)	**REG25E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADCDVI_IRQ_FORCE[7:0]	7:0	ADCDVI IRQ force control.	
71h (25E3h)	**REG25E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADCDVI_IRQ_CLR[7:0]	7:0	ADCDVI IRQ clear control.	
72h (25E4h)	**REG25E4**	**7:0**	**Default : 0x08**	**Access : R/W**
	GAIN_AGC0[7:0]	7:0	Select ADC gain control for VD AGC_COARSE=0.	
72h (25E5h)	**REG25E5**	**7:0**	**Default : 0x10**	**Access : R/W**
	GAIN_AGC1[7:0]	7:0	Select ADC gain control for VD AGC_COARSE=1.	
73h (25E6h)	**REG25E6**	**7:0**	**Default : 0x10**	**Access : R/W**
	GAIN_AGC2[7:0]	7:0	Select ADC gain control for VD AGC_COARSE=2.	
73h (25E7h)	**REG25E7**	**7:0**	**Default : 0xE0**	**Access : R/W**
	GAIN_AGC3[7:0]	7:0	Select ADC gain control for VD AGC_COARSE=3.	
74h	**REG25E8**	**7:0**	**Default : 0xC1**	**Access : R/W**

ATOP Register (Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(25E8h)	GMC_AGC[3:0]	7:4	Select GMC gain control for VD AGC_COARSE.	
	GSHIFT_AGC[3:0]	3:0	Select ADC gain shift control for VD AGC_COARSE.	
74h ~ 78h	**-**	**7:0**	**Default : -**	**Access : -**
(25E9h ~ 25F1h)	-	-	Reserved.	

ADC Register (Bank = 26)

ADC Register (Bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2600h)	**REG2600**	**7:0**	**Default : 0x95**	**Access : R/W**
	PLLDIV[7:0]	7:0	ADC PLL divider ratio (htotal-3), (write sequence LSB -> MSB).	
00h (2601h)	**REG2601**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	PLLDIV[12:8]	4:0	See description of '2600h'.	
01h (2602h)	**REG2602**	**7:0**	**Default : 0x82**	**Access : R/W**
	BWCOEF[7:0]	7:0	ADC PLL bandwidth coefficient.	
01h (2603h)	**REG2603**	**7:0**	**Default : 0x09**	**Access : R/W**
	FREQCOEF[7:0]	7:0	ADC PLL frequency coefficient.	
02h (2604h)	**REG2604**	**7:0**	**Default : 0x05**	**Access : R/W**
	DAMPCOEF[7:0]	7:0	ADC PLL damping coefficient.	
03h (2606h)	**REG2606**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PHASE_CC[5:0]	5:0	Select ADC sampling clock phase.	
03h (2607h)	**REG2607**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:6	Reserved.	
	PHASE_DELTA[5:0]	5:0	Select ADC phase delta between clkcc & clkADC.	
04h (2608h)	**REG2608**	**7:0**	**Default : 0x05**	**Access : R/W**
	PLL_STATUS_SEL[2:0]	7:5	Select pll digital status.	
	PHD_CAL_DIS	4	Disable phase digitalizer calibartion.	
	SETTLE_CNT[3:0]	3:0	Select phase digitalizer settling time.	
04h (2609h)	**REG2609**	**7:0**	**Default : 0xC6**	**Access : R/W**
	WDOG_TOL[1:0]	7:6	Select PLL watch dog reset tolerance.	
	IQCLR_TH[2:0]	5:3	Pll lock to unlock threshold.	
	IQSET_TH[2:0]	2:0	Pll unlock to lock threshold.	
05h (260Ah)	**REG260A**	**7:0**	**Default : 0x00**	**Access : RO**
	PLL_STATUS[7:0]	7:0	Pll digital status. 000: {LOCK, IQ, SLOW, FAST, FREERUN, 3'b000}.	
07h	**REG260E**	**7:0**	**Default : 0x8A**	**Access : R/W**

ADC Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description
(260Eh)	HSYNC_POL	7	Input HSYNC polarity. 0: Low active. 1: High active.
	SOG_EN	6	Select pll locking source. 0: HSYNC. 1: SOG.
	HSYNC_EDGE	5	Select pll locking edge. 0: HSYNC leading edge. 1: HSYNC trailing edge.
	CLAMP_EDGE	4	Select clamp reference edge. 0: HSYNC trailing edge. 1: HSYNC leading edge.
	CCDIS	3	1=disable clamp during coast region.
	WDOG_DIS	2	1=disable ADC PLL watch dog.
	COAST_POL	1	Select coast polarity. 0: Low active. 1: High active.
	DB_LOAD	0	1=enable ADC register double buffer.
07h (260Fh)	**REG260F**	**7:0**	**Default : 0x00** **Access : R/W**
	HSOUT_PW[7:0]	7:0	Select extended HSOUT pulse width.
08h (2610h)	**REG2610**	**7:0**	**Default : 0x80** **Access : R/W**
	GAIN_R[7:0]	7:0	ADC R channel gain control.
08h (2611h)	**REG2611**	**7:0**	**Default : 0x80** **Access : R/W**
	OFFSET_R[7:0]	7:0	ADC R channel offset control.
09h (2612h)	**REG2612**	**7:0**	**Default : 0x80** **Access : R/W**
	GAIN_G[7:0]	7:0	ADC G channel gain control.
09h (2613h)	**REG2613**	**7:0**	**Default : 0x80** **Access : R/W**
	OFFSET_G[7:0]	7:0	ADC G channel offset control.
0Ah (2614h)	**REG2614**	**7:0**	**Default : 0x80** **Access : R/W**
	GAIN_B[7:0]	7:0	ADC B channel gain control.
0Ah (2615h)	**REG2615**	**7:0**	**Default : 0x80** **Access : R/W**
	OFFSET_B[7:0]	7:0	ADC B channel offset control.
0Bh (2616h)	**REG2616**	**7:0**	**Default : 0x05** **Access : R/W**
	CLAMP_DLY[7:0]	7:0	Select clamp pulse start position relative to input HSYNC edge.

ADC Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
0Bh (2617h)	**REG2617**	**7:0**	**Default : 0x05**	**Access : R/W**
	CLAMP_DUR[7:0]	7:0	Select clamp pulse duration.	
0Ch (2618h)	**REG2618**	**7:0**	**Default : 0x24**	**Access : R/W**
	HSOUT_GEN	7	1=enable HSOUT pulse extension.	
	CLAMP_VEN	6	1=enable clamp once per vsync mode.	
	RGB_SWAP[5:0]	5:0	Select rgb data to scalar, [1:0]=SEL R, [3:2]=SEL G, [5:4]=SEL B, 00=R, 01=G, 10=B, 11=blank.	
0Ch (2619h)	**REG2619**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLAMP_VDLY[7:0]	7:0	Clamp pulse line delay from vsync.	
0Dh (261Ah)	**REG261A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MASK_DUR[7:0]	7:0	Select blank ADC data duration after HSYNC.	
0Dh (261Bh)	**REG261B**	**7:0**	**Default : 0x7A**	**Access : R/W**
	-	7	Reserved.	
	MASK_EN[3:0]	6:3	Enable blank ADC for CAL.	
	MASK_COAST	2	1=blank ADC data during COAST.	
	MASK_CDIS	1	1=disable H blank ADC data during COAST.	
	MASK_EDGE	0	0/1=select blank ADC data from HSYNC leading/trailing edge.	
0Eh (261Ch)	**REG261C**	**7:0**	**Default : 0x40**	**Access : R/W**
	TIMEOUT_H[7:0]	7:0	HSYNC activity timeout period (100us).	
0Fh (261Dh)	**REG261D**	**7:0**	**Default : 0x64**	**Access : R/W**
	TIMEOUT_V[7:0]	7:0	VSYNC activity timeout period (ms).	
0Fh (261Eh)	**REG261E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	SOG_TOG	2	1=active channel sog toggle status.	
	VSYNC_TOG	1	1=active channel vsync toggle status.	
	HSYNC_TOG	0	1=active channel hsync toggle status.	
10h (2620h)	**REG2620**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	CALG_TRIG	7	Write an 1 to start gain CAL procedure.	
	CALO_TRIG	6	Write an 1 to start offset CAL procedure.	
	CALG_EN	5	1=enable gain auto CAL procedure.	
	CALO_EN	4	1=enable offset auto CAL procedure.	

ADC Register (Bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CALO_MODE[1:0]	3:2	Select offset CAL procedure, 0x(normal), 10(live only), 11(normal=>live).	
	CALO_INPUT[1:0]	1:0	Select offset CAL reference, 0=CAL to internal vref, 1=CAL to input. [0]: Select for normal procedure. [1]: Select for live procedure.	
10h (2621h)	**REG2621**	**7:0**	**Default : 0x04**	**Access : R/W**
	CALO_BLK	7	Select offset CAL target DOUT code. 0: 0. 1: 16.	
	CAL_STOP	6	1=stop CAL procedure.	
	CAL_MANCH[1:0]	5:4	Select manual CAL channel. b00: R. b01: G. b10: B.	
	CAL_DB_HS	3	0/1=select VSYNC/HSYNC to update CAL display.	
	CALG_DISP	2	1=enable gain CAL for display.	
	CALG_DB_LD	1	1=force load gain CAL result to display.	
	CALG_DB_HOLD	0	1=hold current gain CAL result for display.	
11h (2622h)	**REG2622**	**7:0**	**Default : 0x92**	**Access : R/W**
	CALO_DISP	7	1=enable offset CAL for display.	
	CALO_DB_LD	6	1=force load CAL result to display.	
	CALO_DB_HOLD	5	1=hold current CAL result for display.	
	CALD_DISP	4	1=enable digital offset CAL for display.	
	CALD_DB_TH[3:0]	3:0	Select threshold level to update CAL result.	
11h (2623h)	**REG2623**	**7:0**	**Default : 0x40**	**Access : R/W**
	CALO_HOLDY	7	1=hold current ADC_Y offset CAL result.	
	CAL_LOCK	6	1=wait pll lock to start CAL for ADC mode.	
	CAL_LIVET	5	1=enable fast tracking in CAL live mode.	
	CAL_LMT	4	1=enable limit CAL result range for CAL live mode.	
	CAL_LMTV[3:0]	3:0	Select limited range for CAL result update.	
12h (2624h)	**REG2624**	**7:0**	**Default : 0x60**	**Access : R/W**
	CAL_VS	7	1=CAL synchronize to VSYNC.	
	CAL_BW	6	1=enable max ADC bandwidth during CAL.	

ADC Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
	CAL_COREV[3:0]	5:2	Select error coring threshold for CAL fine mode.	
	CAL_ERRCOEF[1:0]	1:0	Select CAL error coefficient; 00=1; 01=1/2; 10=1/4; 11=1/8.	
12h (2625h)	**REG2625**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CALD_EN	6	1=enable digital offset calibration function.	
	CALD_DIT_CAL	5	1=enable digital dither for CAL.	
	CALD_DIT_DISP	4	1=enable digital dither for display.	
	DGAIN_SEL[1:0]	3:2	Select digital gain of ADC data. b00: 1.0. b01: 1.004. b10: 1.008. b11: 1.016.	
	CALD_MAX[1:0]	1:0	Select digital offset max range; 00=1; 01=2; 10=3; 11=4(8-bit LSB).	
13h (2626h)	**REG2626**	**7:0**	**Default : 0x0A**	**Access : R/W**
	RESERVED_13H[1:0]	7:6	Reserved.	
	CAL_SWOV[1:0]	5:4	Override CAL switch control, 00=none, 01=CALO, 10=CALG_VL, 11=CALG_VH.	
	CAL_A2D_STEP[3:0]	3:0	Define equivalent code of 1 ADC offset step (in 12-bit resolution).	
13h (2627h)	**REG2627**	**7:0**	**Default : 0x68**	**Access : R/W**
	NORM_GAIN[7:0]	7:0	Select ADC normal gain of 0.7Vpp for CALG.	
14h (2628h)	**REG2628**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAL_EDGE0	7	0/1=select CAL start from HSYNC leading/trailing edge for CAL to reference.	
	CAL_DLY0[6:0]	6:0	CAL pulse start delay (N+1).	
15h (262Ah)	**REG262A**	**7:0**	**Default : 0x10**	**Access : R/W**
	CAL_SMPDLY0[7:0]	7:0	CAL sample data delay (N+1).	
15h (262Bh)	**REG262B**	**7:0**	**Default : 0x10**	**Access : R/W**
	CAL_SMPDUR0[7:0]	7:0	CAL sample data duration (N+1).	
16h (262Ch)	**REG262C**	**7:0**	**Default : 0x90**	**Access : R/W**
	CAL_EDGE1	7	0/1=select CAL start from HSYNC leading/trailing edge for CAL live mode.	
	CAL_DLY1[6:0]	6:0	CAL pulse start delay (N+1).	

ADC Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
17h (262Eh)	**REG262E**	**7:0**	**Default : 0x08**	**Access : R/W**
	CAL_SMPDLY1[7:0]	7:0	CAL sample data delay (N+1).	
17h (262Fh)	**REG262F**	**7:0**	**Default : 0x08**	**Access : R/W**
	CAL_SMPDUR1[7:0]	7:0	CAL sample data duration (N+1).	
18h (2630h)	**REG2630**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAL_SKIPLINE[7:0]	7:0	Skip lines for CAL pulse, [3:0]=normal mode, [7:4]=live mode.	
19h (2632h)	**REG2632**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAL_WD[7:0]	7:0	Write data to CAL registers.	
19h (2633h)	**REG2633**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	RESERVED_19H[2:0]	7:5	Reserved.	
	CAL_WP	4	Write an 1 to write data to CAL registers.	
	CAL_WSEL[3:0]	3:0	Select CAL registers to write.	
1Ah (2634h)	**REG2634**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_1AH[3:0]	7:4	Reserved.	
	CAL_STATUS_SEL[3:0]	3:0	Select CAL status report.	
1Bh (2636h)	**REG2636**	**7:0**	**Default : 0x00**	**Access : RO**
	CAL_STATUS[7:0]	7:0	Internal CAL status.	
1Bh (2637h)	**REG2637**	**7:0**	**Default : 0x00**	**Access : RO**
	CAL_STATUS[15:8]	7:0	See description of '2636h'.	
1Ch (2638h)	**REG2638**	**7:0**	**Default : 0x00**	**Access : RO**
	ADC_CLPERR[7:0]	7:0	ADC clamp error status (format=S3), [3:0]=R, [7:4]=G, [11:8]=B.	
1Ch (2639h)	**REG2639**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	ADC_CLPERR[11:8]	3:0	See description of '2638h'.	
1Dh (263Ah)	**REG263A**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7	Reserved.	
	CLROVF_RGB	6	Write an 1 to clear ADC_RGB overflow flags.	
	OVF_RGB[5:0]	5:0	ADC overflow flags, {OVFB, UNFB, OVFG, UNFG, OVFR, UNFR}.	
1Eh (263Ch)	**REG263C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DITV_R[1:0]	7:6	ADC_R dither dc level.	

ADC Register (Bank = 26)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	DIT_CAL[2:0]	5:3	Select ADC dither mode for CAL. b000: Off. b001: 1-bit noise. b010: 2-bit noise. b011: 3-bit noise. b100: Seq2 1-bit toggle noise. b101: Seq2 2-bit toggle noise. b110: Seq4 2-bit toggle noise. b110: Seq4 3-bit toggle noise.
	DIT_DISP[2:0]	2:0	Select ADC dither mode for display.
1Eh (263Dh)	**REG263D**	**7:0**	**Default : 0x49** **Access : R/W**
	-	7	Reserved.
	DITV_B[2:0]	6:4	ADC_B dither dc level.
	DITV_G[2:0]	3:1	ADC_G dither dc level.
	DITV_R[2]	0	See description of '263Ch'.

HDMI Register (Bank = 27)

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (2702h)	**REG2702**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_PKT	7	Vendor Specific Packet or User Specified Packet received. NOTE: All bits in HDMIST1 register represent, when reading back 1, one or more than one packets have been received by the HDMI receiver engine between the previous read and the current read. No packet has been received since last read if a bit is read back as 0.	
	ACR_PKT	6	Audio Clock Regeneration Packet received.	
	ASAMPLE_PKT	5	Audio Sample Packet received.	
	GCP_PKT	4	General Control Packet received.	
	AVI_PKT	3	AVI InfoFrame Packet received.	
	SPD_PKT	2	SPD InfoFrame Packet received.	
	AUI_PKT	1	Audio InfoFrame Packet received.	
	MPEG_PKT	0	MPEG InfoFrame Packet received.	
01h (2703h)	**REG2703**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GM_PKT	5	Gamut Metadata Packet received. NOTE: Bits [13:0] in register represent, when reading back 1, one or more than one packets have been received by the HDMI receiver engine between the previous read and the current read. No packet has been received since last read if a bit is read back as 0.	
	DSD_PKT	4	DSD Packet received.	
	ACP_PKT	3	ACP Packet received.	
	ISRC1_PKT	2	ISRC1 Packet received.	
	ISRC2_PKT	1	ISRC2 Packet received.	
	NULL_PKT	0	Null Packet received.	
02h (2704h)	**REG2704**	**7:0**	**Default : 0x00**	**Access : R/W**
	VCLK_BIG_CHG	7	HDMI video clock frequency big change.	
	CTSN_OV_RANGE	6	Received CTS N over range.	
	PIX_DE_CNT_DIFF	5	Number of DE pixels changed. 0: No event.	

HDMI Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description
			1: Changed.
	-	4	Reserved.
	AFIFO34_FULL	3	Audio FIFO 3/4 Full. Write 1 to clear.
	AFIFO34_EMPTY	2	Audio FIFO 3/4 Empty. Write 1 to clear.
	AFIFO12_FULL	1	Audio FIFO 1/2 Full. Write 1 to clear.
	AFIFO12_EMPTY	0	Audio FIFO 1/2 Empty. Write 1 to clear.
02h (2705h)	**REG2705**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	-	7:5	Reserved.
	VCLK_STABLE	4	HDMI video clock stable or not. 0: Not stable. 1: Stable.
	-	3:0	Reserved.
04h (2708h)	**REG2708**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:6	Reserved.
	AS_PBIT_ERR	5	Audio sample parity bit error detected. Write 1 to clear.
	ASAMPLE_ERR	4	Audio sample packet receive error occurred; sample repeated.
	UNSUPPKT	3	Unsupported Packet received. Write 1 to clear.
	CHECKSUM_ERR	2	Checksum error occurred; packet discarded. Write 1 to clear.
	BCHPRTY_ERR	1	BCH parity error occurred; packet discarded. Write 1 to clear.
	BCHERR_CORRECTED	0	Single bit BCH parity error occurred and corrected. Write 1 to clear.
05h (270Ah)	**REG270A**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7	Reserved.
	RESET_CTS_FIFO	6	Reset CTS FIFO. 0: Enable. 1: Disable.

HDMI Register (Bank = 27)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	AFIFO_TH[1:0]	5:4	Audio FIFO start operation threshold. 00: Immediately. 01: After 1/4 fullness. 10: After 1/2 fullness. 11: After 3/4 fullness.
	-	3:2	Reserved.
	EN_USPPKT	1	Enable user specified packet based on header type defined at PKTTYPE register. 0: Disable. 1: Enable.
	-	0	Reserved.
06h (270Dh)	**REG270D**	**7:0**	**Default : 0xE0** **Access : R/W**
	VIDEO_BLANK_SEL	7	Output black level in video blanking for YCbCr format. 0: Output Y=0, Cb=0, and Cr=0. 1: Output black level.
	GCP_OUT_SEL	6	Output current deep color information or new received GCP packet to GCONTROL register. 0: New received GCP packet. 1: Deep color information.
	ASFLAT_CHK	5	Audio sample flat bit check. 0: Disable. 1: Enable.
	AFIFO_RST	4	Reset Audio FIFO / (Clear FIFO Contents); all channels. 0: Normal. 1: Reset audio FIFO.
	EN_AVMUTE	3	Enable video mute. 0: Disable. 1: Enable when AVMUTE signal is received.
	VMUTEBLANK	2	Blanking when AV mute is active. 0: Disable. 1: Enable.
	HDMI_AUTO_EN	1	Enable HDMI/DVI mode detection. 0: HDMI/DVI mode is set by F/W. 1: HDMI/DVI mode is detected by hardware automatically.
	EN_AVMUTEDET	0	Enable Auto Video Mute processing based on AVMUTE. 0: No action. 1: Enter video mute and free run automatically when AVMUTE is set.

HDMI Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
			Free run is cleared back to normal mode by F/W.	
07h (270Eh)	**REG270E**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	MANUAL_AP_SEL	7	Manual adjust phase select. 0: Adjust phase by default phase. 1: Write MANUAL_ADJUST_PHASE bit to shift one phase.	
	MANUAL_ADJUST_PHASE	6	Write 1 to this bit to adjust pixel packing phase. Valid only if MANUAL_COLOR_DEPTH`0 and MANUAL_AP_SEL=1.	
	DIS_NO_GCP_QUIT	5	Disable deep color mode auto exit if the sink does not receive a GCP with non-zero CD for more than 4 consecutive video fields. 0: Enable. 1: Disable.	
	MANUAL_COLOR_DEPTH[1:0]	4:3	Manual color depth. 00: Disable. 01: 30 bits per pixel. 10: 36 bits per pixel. 11: Reserved.	
	EN_DF_ADJUST	2	Adjust phase by default phase in deep color mode. 0: Disable. 1: Enable.	
	AUTO_RST_DC_FIFO	1	Auto reset deep color FIFO if overflow or underflow occurs. 0: Disable. 1: Enable.	
	EN_DEEP_COLOR	0	Enable deep color mode. 0: Disable. 1: Enable.	
07h (270Fh)	**REG270F**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	UPDATE_LMT_CTSN	7	Update limited CTS/N values of CTSN filter from CTS_LMT/N_LMT registers. 0: Disable. 1: Enable.	
	EN_CTSN_FILTER	6	Enable CTS N filter. 0: Disable. 1: Enable.	
	GMP_OUT_EN	5	GM packet is mapped to ISRC_HB1 and ISRC0~ISRC10. Write ISRC_HB1 to load GM packet to register.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Original ISRC packet. 1: GM packet.	
	GMP_OUT_SEL	4	GMP register output select. 0: Output new received GM packet to GMP register. 1: Output current affected GM packet to GMP register.	
	-	3:2	Reserved.	
	CD_ZERO_UPDATE	1	0: Update Deep Color information only if received CD value is not zero. 1: Update Deep Color information when any GCP packet is received.	
	WP_AUTO_ADJUST	0	Wrong phase auto adjustment in deep color mode. 0: Normal. 1: Auto adjust phase.	
08h (2710h)	**REG2710**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CTSN_OUT2REG_SEL	0	Select the type of CTS and N value to be outputted to register. 0: Bypass CTSN filter. 1: From CTSN filter.	
08h (2711h)	**REG2711**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HDMI_DCLK_INV	3	Invert HDMI audio PLL DCLK clock. 0: Normal. 1: Invert.	
	HDMI_DCLK_EN	2	Enable HDMI audio PLL DCLK clock. 0: Disable. 1: Enable.	
	HDMI_FBCLK_INV	1	Invert HDMI audio PLL FBCLK clock. 0: Normal. 1: Invert.	
	HDMI_FBCLK_EN	0	Enable HDMI audio PLL FBCLK clock. 0: Disable. 1: Enable.	
09h (2713h)	**REG2713**	**7:0**	**Default : 0x00**	**Access : R/W**
	N_LMT_1[3:0]	7:4	Limited N value [19:16].	
	CTS_LMT_1[3:0]	3:0	Limited CTS value [19:16].	

HDMI Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
0Ah (2714h)	**REG2714**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTS_LMT_0[7:0]	7:0	Limited CTS value [15:0].	
0Ah (2715h)	**REG2715**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTS_LMT_0[15:8]	7:0	See description of '2714h'.	
0Bh (2716h)	**REG2716**	**7:0**	**Default : 0x00**	**Access : R/W**
	N_LMT_0[7:0]	7:0	Limited N value [15:0].	
0Bh (2717h)	**REG2717**	**7:0**	**Default : 0x00**	**Access : R/W**
	N_LMT_0[15:8]	7:0	See description of '2716h'.	
0Ch (2718h)	**REG2718**	**7:0**	**Default : 0x0A**	**Access : R/W**
	VLD_CTS_RANGE[7:0]	7:0	Program these bits to define valid CTS range. CTS_LMT - VLD_CTS_RANGE < Valid CTS < CTS_LMT + VLD_CTS_RANGE.	
0Ch (2719h)	**REG2719**	**7:0**	**Default : 0x0A**	**Access : R/W**
	VLD_N_RANGE[7:0]	7:0	Program these bits to define valid N range. N_LMT - VLD_N_RANGE < Valid N < N_LMT + VLD_N_RANGE.	
0Dh (271Ah)	**REG271A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMPVAL50[7:0]	7:0	50M count value.	
0Dh (271Bh)	**REG271B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMPVAL50[15:8]	7:0	See description of '271Ah'.	
0Eh (271Ch)	**REG271C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMPVAL100[7:0]	7:0	100M count value.	
0Eh (271Dh)	**REG271D**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMPVAL100[15:8]	7:0	See description of '271Ch'.	
0Fh (271Eh)	**REG271E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMPVAL200[7:0]	7:0	200M count value.	
0Fh (271Fh)	**REG271F**	**7:0**	**Default : 0x00**	**Access : R/W**
	CMPVAL200[15:8]	7:0	See description of '271Eh'.	
10h (2720h)	**REG2720**	**7:0**	**Default : 0x00**	**Access : R/W**
	PKT_TYPE[7:0]	7:0	Used for vendor specific packet capture.	
11h (2722h)	**REG2722**	**7:0**	**Default : 0x00**	**Access : RO**
	CNT_VAL[7:0]	7:0	Count value of TMDS clock.	
11h (2723h)	**REG2723**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	

HDMI Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
	FIN[1:0]	6:5	TMDS clock frequency range detection. 00: Less than 50 MHz. 01: Between 50 and 100 MHz. 10: Between 100 and 200 MHz. 11: Greater than 200 MHz.	
	CNT_VAL[12:8]	4:0	See description of '2722h'.	
12h (2724h)	**REG2724**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTS_0[7:0]	7:0	CTS[15:0] value received from Audio clock regeneration packet. Write this register to update CTS and N values.	
12h (2725h)	**REG2725**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTS_0[15:8]	7:0	See description of '2724h'.	
13h (2726h)	**REG2726**	**7:0**	**Default : 0x00**	**Access : RO**
	N_0[7:0]	7:0	N[15:0] value received from audio clock regeneration packet.	
13h (2727h)	**REG2727**	**7:0**	**Default : 0x00**	**Access : RO**
	N_0[15:8]	7:0	See description of '2726h'.	
14h (2728h)	**REG2728**	**7:0**	**Default : 0x00**	**Access : RO**
	N_1[7:4]	7:4	N[15:0] value received from audio clock regeneration packet.	
	CTS_1[3:0]	3:0	CTS[19:16] value received from audio clock regeneration packet.	
15h (272Ah)	**REG272A**	**7:0**	**Default : 0x00**	**Access : RO**
	GCONTROL[7:0]	7:0	[0]: AVMUTE received from general control packet. 0: Clear AVMUTE. 1: Set AVMUTE. [1]: Default phase in GCP subpacket byte 2. [4:2]: RX last packing phase for each video period (RO). 000: Phase 0 (10P0, 12P0, 16P0). 001: Phase 1 (10P1, 12P1, 16P1). 010: Phase 2 (10P2, 12P2). 011: Phase 3 (10P3). 100: Phase 4 (10P4). 101~111: Reserved. [7:5]: Previous last packing phase. [11:8]: Color depth in GCP subpacket byte 1. [15:12]: Pixel packing phase in GCP subpacket byte 1.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (272Bh)	**REG272B**	**7:0**	**Default : 0x00**	**Access : RO**
	GCONTROL[15:8]	7:0	See description of '272Ah'.	
16h (272Ch)	**REG272C**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_HDR1[7:0]	7:0	Content protection type field from Audio Content Protection (ACP) packet. 0x00: Generic Audio. 0x01: IEC 60958-identified Audio. 0x02: DVD Audio. 0x03: Reserved for Super Audio CD (SACD). 0x04~0xFF: Reserved.	
17h (272Eh)	**REG272E**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB0[7:0]	7:0	ACP packet payload byte 0.	
17h (272Fh)	**REG272F**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB1[7:0]	7:0	ACP packet payload byte 1.	
18h (2730h)	**REG2730**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB2[7:0]	7:0	ACP packet payload byte 2.	
18h (2731h)	**REG2731**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB3[7:0]	7:0	ACP packet payload byte 3.	
19h (2732h)	**REG2732**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB4[7:0]	7:0	ACP packet payload byte 4.	
19h (2733h)	**REG2733**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB5[7:0]	7:0	ACP packet payload byte 5.	
1Ah (2734h)	**REG2734**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB6[7:0]	7:0	ACP packet payload byte 6.	
1Ah (2735h)	**REG2735**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB7[7:0]	7:0	ACP packet payload byte 7.	
1Bh (2736h)	**REG2736**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB8[7:0]	7:0	ACP packet payload byte 8.	
1Bh (2737h)	**REG2737**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB9[7:0]	7:0	ACP packet payload byte 9.	
1Ch (2738h)	**REG2738**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB10[7:0]	7:0	ACP packet payload byte 10.	
1Ch (2739h)	**REG2739**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB11[7:0]	7:0	ACP packet payload byte 11.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (273Ah)	**REG273A**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB12[7:0]	7:0	ACP packet payload byte 12.	
1Dh (273Bh)	**REG273B**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB13[7:0]	7:0	ACP packet payload byte 13.	
1Eh (273Ch)	**REG273C**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB14[7:0]	7:0	ACP packet payload byte 14.	
1Eh (273Dh)	**REG273D**	**7:0**	**Default : 0x00**	**Access : RO**
	ACP_PB15[7:0]	7:0	ACP packet payload byte 15.	
1Fh (273Eh)	**REG273E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISRC1_HDR1[7:0]	7:0	ISRC1 packet header byte 1. Write this register to update GM packet.	
1Fh (273Fh)	**REG273F**	**7:0**	**Default : 0x00**	**Access : RO**
	GBD_HDR2[7:0]	7:0	GM packet header byte 2.	
20h (2740h)	**REG2740**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB0[7:0]	7:0	ISRC packet payload byte 0.	
20h (2741h)	**REG2741**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB1[7:0]	7:0	ISRC packet payload byte 1.	
21h (2742h)	**REG2742**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB2[7:0]	7:0	ISRC packet payload byte 2.	
21h (2743h)	**REG2743**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB3[7:0]	7:0	ISRC packet payload byte 3.	
22h (2744h)	**REG2744**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB4[7:0]	7:0	ISRC packet payload byte 4.	
22h (2745h)	**REG2745**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB5[7:0]	7:0	ISRC packet payload byte 5.	
23h (2746h)	**REG2746**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB6[7:0]	7:0	ISRC packet payload byte 6.	
23h (2747h)	**REG2747**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB7[7:0]	7:0	ISRC packet payload byte 7.	
24h (2748h)	**REG2748**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB8[7:0]	7:0	ISRC packet payload byte 8.	
24h (2749h)	**REG2749**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB9[7:0]	7:0	ISRC packet payload byte 9.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
25h (274Ah)	**REG274A**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB10[7:0]	7:0	ISRC packet payload byte 10.	
25h (274Bh)	**REG274B**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB11[7:0]	7:0	ISRC packet payload byte 11.	
26h (274Ch)	**REG274C**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB12[7:0]	7:0	ISRC packet payload byte 12.	
26h (274Dh)	**REG274D**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB13[7:0]	7:0	ISRC packet payload byte 13.	
27h (274Eh)	**REG274E**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB14[7:0]	7:0	ISRC packet payload byte 14.	
27h (274Fh)	**REG274F**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB15[7:0]	7:0	ISRC packet payload byte 15.	
28h (2750h)	**REG2750**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB16[7:0]	7:0	ISRC packet payload byte 16.	
28h (2751h)	**REG2751**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB17[7:0]	7:0	ISRC packet payload byte 17.	
29h (2752h)	**REG2752**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB18[7:0]	7:0	ISRC packet payload byte 18.	
29h (2753h)	**REG2753**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB19[7:0]	7:0	ISRC packet payload byte 19.	
2Ah (2754h)	**REG2754**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB20[7:0]	7:0	ISRC packet payload byte 20.	
2Ah (2755h)	**REG2755**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB21[7:0]	7:0	ISRC packet payload byte 21.	
2Bh (2756h)	**REG2756**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB22[7:0]	7:0	ISRC packet payload byte 22.	
2Bh (2757h)	**REG2757**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB23[7:0]	7:0	ISRC packet payload byte 23.	
2Ch (2758h)	**REG2758**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB24[7:0]	7:0	ISRC packet payload byte 24.	
2Ch (2759h)	**REG2759**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB25[7:0]	7:0	ISRC packet payload byte 25.	
2Dh	**REG275A**	**7:0**	**Default : 0x00**	**Access : RO**

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(275Ah)	ISRC_PB26[7:0]	7:0	ISRC packet payload byte 26.	
2Dh (275Bh)	**REG275B**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB27[7:0]	7:0	ISRC packet payload byte 27.	
2Eh (275Ch)	**REG275C**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB28[7:0]	7:0	ISRC packet payload byte 28.	
2Eh (275Dh)	**REG275D**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB29[7:0]	7:0	ISRC packet payload byte 29.	
2Fh (275Eh)	**REG275E**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB30[7:0]	7:0	ISRC packet payload byte 30.	
2Fh (275Fh)	**REG275F**	**7:0**	**Default : 0x00**	**Access : RO**
	ISRC_PB31[7:0]	7:0	ISRC packet payload byte 31.	
30h (2760h)	**REG2760**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_HDR0[7:0]	7:0	Vender Specific Packet header byte 0.	
30h (2761h)	**REG2761**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_HDR1[7:0]	7:0	Vender Specific Packet header byte 1.	
31h (2762h)	**REG2762**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_HDR2[7:0]	7:0	Vender Specific Packet header byte 2.	
32h (2764h)	**REG2764**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF1[7:0]	7:0	Vendor Specific Packet payload byte 1.	
32h (2765h)	**REG2765**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF2[7:0]	7:0	Vendor Specific Packet payload byte 2.	
33h (2766h)	**REG2766**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF3[7:0]	7:0	Vendor Specific Packet payload byte 3.	
33h (2767h)	**REG2767**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF4[7:0]	7:0	Vendor Specific Packet payload byte 4.	
34h (2768h)	**REG2768**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF5[7:0]	7:0	Vendor Specific Packet payload byte 5.	
34h (2769h)	**REG2769**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF6[7:0]	7:0	Vendor Specific Packet payload byte 6.	
35h (276Ah)	**REG276A**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF7[7:0]	7:0	Vendor Specific Packet payload byte 7.	
35h (276Bh)	**REG276B**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF8[7:0]	7:0	Vendor Specific Packet payload byte 8.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
36h (276Ch)	**REG276C**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF9[7:0]	7:0	Vendor Specific Packet payload byte 9.	
36h (276Dh)	**REG276D**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF10[7:0]	7:0	Vendor Specific Packet payload byte 10.	
37h (276Eh)	**REG276E**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF11[7:0]	7:0	Vendor Specific Packet payload byte 11.	
37h (276Fh)	**REG276F**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF12[7:0]	7:0	Vendor Specific Packet payload byte 12.	
38h (2770h)	**REG2770**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF13[7:0]	7:0	Vendor Specific Packet payload byte 13.	
38h (2771h)	**REG2771**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF14[7:0]	7:0	Vendor Specific Packet payload byte 14.	
39h (2772h)	**REG2772**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF15[7:0]	7:0	Vendor Specific Packet payload byte 15.	
39h (2773h)	**REG2773**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF16[7:0]	7:0	Vendor Specific Packet payload byte 16.	
3Ah (2774h)	**REG2774**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF17[7:0]	7:0	Vendor Specific Packet payload byte 17.	
3Ah (2775h)	**REG2775**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF18[7:0]	7:0	Vendor Specific Packet payload byte 18.	
3Bh (2776h)	**REG2776**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF19[7:0]	7:0	Vendor Specific Packet payload byte 19.	
3Bh (2777h)	**REG2777**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF20[7:0]	7:0	Vendor Specific Packet payload byte 20.	
3Ch (2778h)	**REG2778**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF21[7:0]	7:0	Vendor Specific Packet payload byte 21.	
3Ch (2779h)	**REG2779**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF22[7:0]	7:0	Vendor Specific Packet payload byte 22.	
3Dh (277Ah)	**REG277A**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF23[7:0]	7:0	Vendor Specific Packet payload byte 23.	
3Dh (277Bh)	**REG277B**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF24[7:0]	7:0	Vendor Specific Packet payload byte 24.	
3Eh	**REG277C**	**7:0**	**Default : 0x00**	**Access : RO**

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(277Ch)	VS_IF25[7:0]	7:0	Vendor Specific Packet payload byte 25.	
3Eh (277Dh)	**REG277D**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF26[7:0]	7:0	Vendor Specific Packet payload byte 26.	
3Fh (277Eh)	**REG277E**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF27[7:0]	7:0	Vendor Specific Packet payload byte 27.	
3Fh (277Fh)	**REG277F**	**7:0**	**Default : 0x00**	**Access : RO**
	VS_IF28[7:0]	7:0	Vendor Specific Packet payload byte 28.	
40h (2780h)	**REG2780**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF1[7:0]	7:0	AVI InfoFrame byte 1. [1:0]: Scan info. [3:2]: Ban info. [4]: Active format info present. [6:5]: RGB or YCbCr. [7]: Version.	
40h (2781h)	**REG2781**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF2[7:0]	7:0	AVI InfoFrame byte 2. [3:0]: Active format aspect ratio. [5:4]: Picture aspect ratio. [7:6]: Colorimetry.	
41h (2782h)	**REG2782**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF3[7:0]	7:0	AVI InfoFrame byte 3. [1:0]: Non-conforming Picture Scaling. 00: No known non-uniform scaling. 01: Picture has been scaled horizontally. 10: Picture has been scaled vertically. 11: Picture has been scaled horizontally and vertically. [3:2]: Quantization range. [5:4]: Extended colorimetry. [7]: IT content.	
41h (2783h)	**REG2783**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF4[7:0]	7:0	AVI InfoFrame byte 4. Video Identification Code. Refer to EIA/CEA 861B specification.	
42h (2784h)	**REG2784**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF5[7:0]	7:0	AVI InfoFrame byte 5. [3:0]: Pixel repetition; pixel sent (PR+1) times.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h (2785h)	**REG2785**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF6[7:0]	7:0	AVI InfoFrame byte 6. Line number of end of Top bar [7:0].	
43h (2786h)	**REG2786**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF7[7:0]	7:0	AVI InfoFrame byte 7. Line number of end of Top bar [15:8].	
43h (2787h)	**REG2787**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF8[7:0]	7:0	AVI InfoFrame byte 8. Line number of start of Bottom bar [7:0].	
44h (2788h)	**REG2788**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF9[7:0]	7:0	AVI InfoFrame byte 9. Line number of start of Bottom bar [15:8].	
44h (2789h)	**REG2789**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF10[7:0]	7:0	AVI InfoFrame byte 10. Pixel number of end of Left bar [7:0].	
45h (278Ah)	**REG278A**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF11[7:0]	7:0	AVI InfoFrame byte 11. Pixel number of end of Left bar [15:8].	
45h (278Bh)	**REG278B**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF12[7:0]	7:0	AVI InfoFrame byte 12. Pixel number of end of Right bar [7:0].	
46h (278Ch)	**REG278C**	**7:0**	**Default : 0x00**	**Access : RO**
	AVI_IF13[7:0]	7:0	AVI InfoFrame byte 13. Pixel number of end of Left bar [15:8].	
47h (278Eh)	**REG278E**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF1[7:0]	7:0	SPD InfoFrame byte 1.	
47h (278Fh)	**REG278F**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF2[7:0]	7:0	SPD InfoFrame byte 2.	
48h (2790h)	**REG2790**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF3[7:0]	7:0	SPD InfoFrame byte 3.	
48h (2791h)	**REG2791**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF4[7:0]	7:0	SPD InfoFrame byte 4.	
49h (2792h)	**REG2792**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF5[7:0]	7:0	SPD InfoFrame byte 5.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
49h (2793h)	**REG2793**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF6[7:0]	7:0	SPD InfoFrame byte 6.	
4Ah (2794h)	**REG2794**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF7[7:0]	7:0	SPD InfoFrame byte 7.	
4Ah (2795h)	**REG2795**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF8[7:0]	7:0	SPD InfoFrame byte 8.	
4Bh (2796h)	**REG2796**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF9[7:0]	7:0	SPD InfoFrame byte 9.	
4Bh (2797h)	**REG2797**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF10[7:0]	7:0	SPD InfoFrame byte 10.	
4Ch (2798h)	**REG2798**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF11[7:0]	7:0	SPD InfoFrame byte 11.	
4Ch (2799h)	**REG2799**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF12[7:0]	7:0	SPD InfoFrame byte 12.	
4Dh (279Ah)	**REG279A**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF13[7:0]	7:0	SPD InfoFrame byte 13.	
4Dh (279Bh)	**REG279B**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF14[7:0]	7:0	SPD InfoFrame byte 14.	
4Eh (279Ch)	**REG279C**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF15[7:0]	7:0	SPD InfoFrame byte 15.	
4Eh (279Dh)	**REG279D**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF16[7:0]	7:0	SPD InfoFrame byte 16.	
4Fh (279Eh)	**REG279E**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF17[7:0]	7:0	SPD InfoFrame byte 17.	
4Fh (279Fh)	**REG279F**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF18[7:0]	7:0	SPD InfoFrame byte 18.	
50h (27A0h)	**REG27A0**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF19[7:0]	7:0	SPD InfoFrame byte 19.	
50h (27A1h)	**REG27A1**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF20[7:0]	7:0	SPD InfoFrame byte 20.	
51h (27A2h)	**REG27A2**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF21[7:0]	7:0	SPD InfoFrame byte 21.	
51h	**REG27A3**	**7:0**	**Default : 0x00**	**Access : RO**

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(27A3h)	SPD_IF22[7:0]	7:0	SPD InfoFrame byte 22.	
52h (27A4h)	**REG27A4**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF23[7:0]	7:0	SPD InfoFrame byte 23.	
52h (27A5h)	**REG27A5**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF24[7:0]	7:0	SPD InfoFrame byte 24.	
53h (27A6h)	**REG27A6**	**7:0**	**Default : 0x00**	**Access : RO**
	SPD_IF25[7:0]	7:0	SPD InfoFrame byte 25.	
54h (27A8h)	**REG27A8**	**7:0**	**Default : 0x00**	**Access : RO**
	AU_IF1[7:0]	7:0	Audio InfoFrame byte 1.	
54h (27A9h)	**REG27A9**	**7:0**	**Default : 0x00**	**Access : RO**
	AU_IF2[7:0]	7:0	Audio InfoFrame byte 2.	
55h (27AAh)	**REG27AA**	**7:0**	**Default : 0x00**	**Access : RO**
	AU_IF3[7:0]	7:0	Audio InfoFrame byte 3.	
55h (27ABh)	**REG27AB**	**7:0**	**Default : 0x00**	**Access : RO**
	AU_IF4[7:0]	7:0	Audio InfoFrame byte 4.	
56h (27ACh)	**REG27AC**	**7:0**	**Default : 0x00**	**Access : RO**
	AU_IF5[7:0]	7:0	Audio InfoFrame byte 5.	
57h (27AEh)	**REG27AE**	**7:0**	**Default : 0x00**	**Access : RO**
	MPEG_IF1[7:0]	7:0	MPEG InfoFrame byte 1.	
57h (27AFh)	**REG27AF**	**7:0**	**Default : 0x00**	**Access : RO**
	MPEG_IF2[7:0]	7:0	MPEG InfoFrame byte 2.	
58h (27B0h)	**REG27B0**	**7:0**	**Default : 0x00**	**Access : RO**
	MPEG_IF3[7:0]	7:0	MPEG InfoFrame byte 3.	
58h (27B1h)	**REG27B1**	**7:0**	**Default : 0x00**	**Access : RO**
	MPEG_IF4[7:0]	7:0	MPEG InfoFrame byte 4.	
59h (27B2h)	**REG27B2**	**7:0**	**Default : 0x00**	**Access : RO**
	MPEG_IF5[7:0]	7:0	MPEG InfoFrame byte 5.	
5Ah (27B4h)	**REG27B4**	**7:0**	**Default : 0x00**	**Access : RO**
	HDMI_CS[7:0]	7:0	HDMI audio channel status.	
5Ah (27B5h)	**REG27B5**	**7:0**	**Default : 0x00**	**Access : RO**
	HDMI_CS[15:8]	7:0	See description of '27B4h'.	
5Bh (27B6h)	**REG27B6**	**7:0**	**Default : 0x00**	**Access : RO**
	HDMI_CS[23:16]	7:0	See description of '27B4h'.	

HDMI Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
5Bh (27B7h)	**REG27B7**	**7:0**	**Default : 0x00**	**Access : RO**
	HDMI_CS[31:24]	7:0	See description of '27B4h'.	
5Ch (27B8h)	**REG27B8**	**7:0**	**Default : 0x00**	**Access : RO**
	HDMI_CS[39:32]	7:0	See description of '27B4h'.	
5Ch (27B9h)	**REG27B9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MANUAL_HPLL_DIV	7	Enable PLL divider to be controlled by registers. 0: Disable. 1: Enable.	
	HPLL_PORST	6	HDMI PLL reset. 0: Normal. 4: Reset (all analog front-end & dividers).	
	HPLL_RESET_TP	5	HDMI PLL post clock divider reset (KP). 0: Normal. 3: Reset.	
	HPLL_RESET_TF	4	HDMI PLL feedback clock divider reset (FBDIV & KM). 0: Normal. 2: Reset.	
	HPLL_RESET_TI	3	HDMI PLL input clock divider reset (DDIV & KN). 0: Normal. 1: Reset.	
	HPLL_VCO_OFFSET	2	Enable VCO free running. 0: Enable. 1: Disable.	
	HPLL_RESET	1	HDMI PLL reset. 0: No reset. 1: Reset.	
	HPLL_PDN	0	HDMI PLL power down. 0: No action. 1: Power down.	
5Dh (27BAh)	**REG27BA**	**7:0**	**Default : 0x10**	**Access : R/W**
	HPLL_KN[1:0]	7:6	HDMI PLL KN divider ratio for new mode. 00: / 1. 01: / 2. 10: / 4. 11: / 4.	
	HPLL_RCTRL[2:0]	5:3	HDMI PLL loop filter resistor control. 000: 23.1K ohm.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			001: 26.4K ohm. 010: 29.7K ohm. ... 111: 42.9K ohm.	
	HPLL_ICTRL[2:0]	2:0	HDMI PLL charge pump current control. 000: 0.65uA. 001: 1.29uA. 010: 1.935uA. 011: 2.58uA. 100: 3.225uA. 101: 3.87uA. 110: 5.16uA. 111: 10.32uA.	
5Dh (27BBh)	**REG27BB**	**7:0**	**Default : 0x00**	**Access : R/W**
	HPLL_KP[3:0]	7:4	HDMI PLL post divider ratio (KP) for new mode. 0000: / 1. 0001: / 2. 0010: / 4. ... 1001: / 512. 1010: / 1024. 1011: / 1024. ... 1111: / 1024.	
	HPLL_KM[3:0]	3:0	HDMI PLL KM divider ratio for new mode. 0000: / 1. 0001: / 2. 0010: / 4. ... 0111: / 128. 1000: / 256. 1001: / 256. ... 1111: / 256.	
5Eh (27BCh)	**REG27BC**	**7:0**	**Default : 0x00**	**Access : R/W**
	HPLL_DDIV[3:0]	7:4	HDMI PLL feedback overwrite divider value from noise-shape quantizer for new mode. 0000: N.A. (/ 16). 0001: N.A. (/ 17).	

HDMI Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description
			0010: / 2. 0011: / 3. ... 1111: / 15.
	HPLL_FBDIV[3:0]	3:0	HDMI PLL input overwrite divider value from noise-shape quantizer for new mode. 0000: N.A. (/ 16). 0001: N.A. (/ 17). 0010: / 2. 0011: / 3. ... 1111: / 15.
5Fh (27BEh)	**REG27BE**	**7:0**	**Default : 0x00** **Access : RO**
	-	7:6	Reserved.
	FRAME_RP_VAL[2:0]	5:3	Frame repetition value.
	HPLL_LOCK_RAW	2	HDMI PLL lock raw flag.
	HPLL_HIGH_FLAG	1	HDMI PLL output flag for VCO supply voltage too high.
	HPLL_LOCK	0	HDMI PLL lock flag.
5Fh (27BFh)	**REG27BF**	**7:0**	**Default : 0x00** **Access : R/W**
	PKT_RST[7:0]	7:0	[0]: Reset AVMUTE register at GCONTROL:AVMUTE. 0: No reset. 1: Reset AVMUTE to 0 (clear AVMUTE). [1]: Reset Y (color format) register at AVI_IF1:Y[1:0]. 0: No reset. 1: Reset Y to 00 (RGB format). [2]: Reset Pixel Repetition register at AVI_IF4:PR[3:0]. 0: No reset. 1: Reset PR to 0 (no repetition). [3]: Reset frame repetition to 0. 0: Output frame repetition information to video engine based on frame format. 1: Reset frame repetition to 0. [4]: Reset CD, PP, and default phase value of GCP packet. 0: No reset. 1: Reset. [5]: Reset deep color FIFO. 0: No reset. 1: Reset.

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[6]: Reserved. [7]: Reset HDMI status registers. Asserting this bit resets HDMIST1~HDMIST2, HDMI_ERR1, AVI_IF0~AVI_IF6, AUDIO_IF0~AUDIO_IF2, SPD_IF0~SPD_IF12, MPEG_IF0~MPEG_IF2, VS_HDR0~VS_HDR1, VS_IF0~VS_IF13, ACP_HB1, ACP_DATA0~ACP_DATA7, ISRC_HB1, and ISRC_DATA0~ISRC_DATA15 registers. 0: No reset. 1: Reset.	
60h (27C0h)	**REG27C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_MASK[7:0]	7:0	Mask packet reception update interrupt (generate an interrupt when a new packet is received and it is different from the previous received packet). 0: Unmask. 1: Mask. [0]: General Control packet. [1]: AVI InfoFrame packet. [2]: Audio InfoFrame packet. [3]: MPEG InfoFrame packet. [4]: ACP packet. [5]: ISRC packet. [6]: BCH error. [7]: Gamut Metadata packet. [12]: CTS N over range. [13]: HDMI video clock frequency big change.	
60h (27C1h)	**REG27C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INT_MASK[13:8]	5:0	See description of '27C0h'.	
61h (27C2h)	**REG27C2**	**7:0**	**Default : 0x00**	**Access : RO**
	INT_STATUS[7:0]	7:0	Interrupt status. [0]: General Control packet. [1]: AVI InfoFrame packet. [2]: Audio InfoFrame packet. [3]: MPEG InfoFrame packet. [4]: ACP packet. [5]: ISRC packet. [6]: BCH error. [7]: Gamut Metadata packet.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[12]: CTS N over range. [13]: HDMI video clock frequency big change.	
61h (27C3h)	**REG27C3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INT_STATUS[13:8]	5:0	See description of '27C2h'.	
62h (27C4h)	**REG27C4**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_FORCE[7:0]	7:0	Force interrupt. [0]: General Control packet. [1]: AVI InfoFrame packet. [2]: Audio InfoFrame packet. [3]: MPEG InfoFrame packet. [4]: ACP packet. [5]: ISRC packet. [6]: BCH error. [7]: Gamut Metadata packet. [12]: CTS N over range. [13]: HDMI video clock frequency big change.	
62h (27C5h)	**REG27C5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INT_FORCE[13:8]	5:0	See description of '27C4h'.	
63h (27C6h)	**REG27C6**	**7:0**	**Default : 0x00**	**Access : R/W**
	INT_CLR[7:0]	7:0	Clear interrupt. [0]: General Control packet. [1]: AVI InfoFrame packet. [2]: Audio InfoFrame packet. [3]: MPEG InfoFrame packet. [4]: ACP packet. [5]: ISRC packet. [6]: BCH error. [7]: Gamut Metadata packet. [12]: CTS N over range. [13]: HDMI video clock frequency big change.	
63h (27C7h)	**REG27C7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INT_CLR[13:8]	5:0	See description of '27C6h'.	
64h (27C8h)	**REG27C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRAME_RP_MODE[3:0]	7:4	[2:0]: Frame repetition value for manual mode.	

HDMI Register (Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Allowed values: 1, 2, and 4. [3]: Frame repetition mode. 0: Auto mode. 1: Manual mode.	
	AUDIO_MODE[3:0]	3:0	[0]: Manual non-PCM mode. [1]: Auto detect non-PCM mode. [2]: Manual DSD mode. [3]: Auto detect DSD mode.	
64h (27C9h)	**REG27C9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HDMI_AU_FIFO_MUTE_EN[4:0]	4:0	Enable the following events to trigger audio controller to output mute audio (DC value). [0]: HDMI CTS/N over limited range (CTSN_OV_RANGE bit). [1]: HDMI video clock frequency big change (VCLK_BIG_CHG bit). [2]: AVMute. [3]: Audio sample parity error (AS_PBIT_ERR bit). [4]: Audio sample BCH error (ASAMPLE_ERR bit).	
65h (27CAh)	**REG27CA**	**7:0**	**Default : 0x00**	**Access : RO**
	PIX_DE_CNT[7:0]	7:0	Pixel DE count.	
65h (27CBh)	**REG27CB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	PIX_DE_CNT[12:8]	4:0	See description of '27CAh'.	

IRQ Register (Bank = 2B)

IRQ Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2B00h)	**REG2B00**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[7:0]	7:0	Mask for FIQ, bit[31:0]. 1: Mask. 0: Not mask.	
00h (2B01h)	**REG2B01**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[15:8]	7:0	See description of '2B00h'.	
01h (2B02h)	**REG2B02**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[23:16]	7:0	See description of '2B00h'.	
01h (2B03h)	**REG2B03**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FIQ_MASK[31:24]	7:0	See description of '2B00h'.	
02h (2B04h)	**REG2B04**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[7:0]	7:0	Force for FIQ, bit[31:0]. 1: Force. 0: Not force.	
02h (2B05h)	**REG2B05**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[15:8]	7:0	See description of '2B04h'.	
03h (2B06h)	**REG2B06**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[23:16]	7:0	See description of '2B04h'.	
03h (2B07h)	**REG2B07**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_FORCE[31:24]	7:0	See description of '2B04h'.	
04h (2B08h)	**REG2B08**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR[7:0]	7:0	Clear for FIQ, bit[31:0]. 1: Clear. 0: Not clear.	
04h (2B09h)	**REG2B09**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR[15:8]	7:0	See description of '2B08h'.	
05h (2B0Ah)	**REG2B0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR[23:16]	7:0	See description of '2B08h'.	
05h (2B0Bh)	**REG2B0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_CLR[31:24]	7:0	See description of '2B08h'.	
06h (2B0Ch)	**REG2B0C**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[7:0]	7:0	FIQ raw status, bit[31:0]. Interrupt source status for FIQ.	

IRQ Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
06h (2B0Dh)	**REG2B0D**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[15:8]	7:0	See description of '2B0Ch'.	
07h (2B0Eh)	**REG2B0E**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[23:16]	7:0	See description of '2B0Ch'.	
07h (2B0Fh)	**REG2B0F**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_RAW_STATUS[31:24]	7:0	See description of '2B0Ch'.	
08h (2B10h)	**REG2B10**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[7:0]	7:0	FIQ final status, bit[31:0]. Final interrupt status for FIQ.	
08h (2B11h)	**REG2B11**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[15:8]	7:0	See description of '2B10h'.	
09h (2B12h)	**REG2B12**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[23:16]	7:0	See description of '2B10h'.	
09h (2B13h)	**REG2B13**	**7:0**	**Default : 0x00**	**Access : RO**
	FIQ_FINAL_STATUS[31:24]	7:0	See description of '2B10h'.	
0Ah (2B14h)	**REG2B14**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[7:0]	7:0	High or low trigger select, bit[31:0]. Inverse source polarity for FIQ.	
0Ah (2B15h)	**REG2B15**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '2B14h'.	
0Bh (2B16h)	**REG2B16**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '2B14h'.	
0Bh (2B17h)	**REG2B17**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FIQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '2B14h'.	
0Ch (2B18h)	**REG2B18**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[7:0]	7:0	Mask for IRQ, bit[31:0]. 1: Mask. 0: Not mask.	
0Ch (2B19h)	**REG2B19**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[15:8]	7:0	See description of '2B18h'.	
0Dh (2B1Ah)	**REG2B1A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[23:16]	7:0	See description of '2B18h'.	
0Dh (2B1Bh)	**REG2B1B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_IRQ_MASK[31:24]	7:0	See description of '2B18h'.	

IRQ Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description	
0Eh (2B1Ch)	**REG2B1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[7:0]	7:0	Force for IRQ, bit[31:0]. 1: Force. 0: Not force.	
0Eh (2B1Dh)	**REG2B1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[15:8]	7:0	See description of '2B1Ch'.	
0Fh (2B1Eh)	**REG2B1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[23:16]	7:0	See description of '2B1Ch'.	
0Fh (2B1Fh)	**REG2B1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_FORCE[31:24]	7:0	See description of '2B1Ch'.	
10h (2B20h)	**REG2B20**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[7:0]	7:0	High or low trigger select, bit[31:0]. Inverse source polarity for IRQ.	
10h (2B21h)	**REG2B21**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '2B20h'.	
11h (2B22h)	**REG2B22**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '2B20h'.	
11h (2B23h)	**REG2B23**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_IRQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '2B20h'.	
12h (2B24h)	**REG2B24**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[7:0]	7:0	IRQ raw status, bit[31:0]. Interrupt source status for IRQ.	
12h (2B25h)	**REG2B25**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[15:8]	7:0	See description of '2B24h'.	
13h (2B26h)	**REG2B26**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[23:16]	7:0	See description of '2B24h'.	
13h (2B27h)	**REG2B27**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS[31:24]	7:0	See description of '2B24h'.	
14h (2B28h)	**REG2B28**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[7:0]	7:0	IRQ final status, bit[31:0]. Final interrupt status for IRQ.	
14h (2B29h)	**REG2B29**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[15:8]	7:0	See description of '2B28h'.	
15h	**REG2B2A**	**7:0**	**Default : 0x00**	**Access : RO**

IRQ Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2B2Ah)	IRQ_FINAL_STATUS[23:16]	7:0	See description of '2B28h'.	
15h (2B2Bh)	**REG2B2B**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS[31:24]	7:0	See description of '2B28h'.	
7Eh (2BFCh)	**REG2BFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CPU0_2_CPU1_IRQ	0	CPU0 to CPU1 interrupt.	
7Fh (2BFEh)	**REG2BFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CPU1_2_CPU0_IRQ	0	CPU1 to CPU0 interrupt.	

ICACHE Register (Bank = 2B)

ICACHE Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (2B80h)	**REG2B80**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDRAM_CODE_MAP[7:0]	7:0	SDRAM code map address, unit is 64-Kbyte.	
40h (2B81h)	**REG2B81**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDRAM_CODE_MAP[15:8]	7:0	See description of '2B80h'.	
41h (2B82h)	**REG2B82**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ADR_L[7:0]	7:0	CPU address[15:0].	
41h (2B83h)	**REG2B83**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ADR_L[15:8]	7:0	See description of '2B82h'.	
42h (2B84h)	**REG2B84**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ADR_H[7:0]	7:0	CPU address[23:0].	
42h (2B85h)	**REG2B85**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ADR_H[15:8]	7:0	See description of '2B84h'.	
43h (2B86h)	**REG2B86**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ROM_DATA0[7:0]	7:0	Icache return data[15:0] to CPU.	
43h (2B87h)	**REG2B87**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ROM_DATA0[15:8]	7:0	See description of '2B86h'.	
44h (2B88h)	**REG2B88**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ROM_DATA1[7:0]	7:0	Icache return data[31:16] to CPU.	
44h (2B89h)	**REG2B89**	**7:0**	**Default : 0x00**	**Access : RO**
	CPU_ROM_DATA1[15:8]	7:0	See description of '2B88h'.	
45h (2B8Ah)	**REG2B8A**	**7:0**	**Default : 0x00**	**Access : RO**
	CACHE_MISS_COUNT[7:0]	7:0	Cache Miss counter.	
45h (2B8Bh)	**REG2B8B**	**7:0**	**Default : 0x00**	**Access : RO**
	CACHE_MISS_COUNT[15:8]	7:0	See description of '2B8Ah'.	
46h (2B8Ch)	**REG2B8C**	**7:0**	**Default : 0x00**	**Access : RO**
	CACHE_HIT_COUNT[7:0]	7:0	Cache Hit counter.	
46h (2B8Dh)	**REG2B8D**	**7:0**	**Default : 0x00**	**Access : RO**
	CACHE_HIT_COUNT[15:8]	7:0	See description of '2B8Ch'.	
47h (2B8Eh)	**REG2B8E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	CPU_WAIT	1	CPU wait flag. 1: Wait.	

ICACHE Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Hit.	
	CACHE_MISS_FLAG	0	Cache Miss flag. 1: Miss. 0: Hit.	
48h (2B90h)	**REG2B90**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	CACHE_FSM[3:0]	3:0	Cache FSM.	
4Ah (2B94h)	**REG2B94**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMP[7:0]	7:0	Temp register.	
4Ah (2B95h)	**REG2B95**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMP[15:8]	7:0	See description of '2B94h'.	
50h (2BA0h)	**REG2BA0**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	CACHE_BY_PASS	0	Cache bypass mode.	

XDMIU Register (Bank = 2B)

XDMIU Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (2BC0h)	**REG2BC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SOFTWARE_RST	0	Set 1 to reset HK_MCU XDATA to MIU.	
61h ~ 61h (2BC2h ~ 2BC3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
62h (2BC4h)	**REG2BC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	XB_SDR_MAP_EN	2	Set 1 to enable mapping of HK_MCU XDATA to MIU.	
	XD2MIU_WPRI	1	XDATA to MIU write priority.	
	XD2MIU_RPRI	0	XDATA to MIU read priority.	
63h (2BC6h)	**REG2BC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR[7:0]	7:0	Low bound address of MCU XDATA mapping to MIU. The unit is 1k bytes. The XDATA address is hit if (XB_ADDR[15:8] > XDATA_ADDR[15:10] >= XB_ADDR[7:0]).	
63h (2BC7h)	**REG2BC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR[15:8]	7:0	See description of '2BC6h'.	
64h (2BC8h)	**REG2BC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP[7:0]	7:0	Low byte address to access XDATA from MIU. The granularity is 64k bytes. The actual address[23:0] to MIU would be {SDR_XD_MAP[10:8], SDR_XD_MAP[7:0], XDATA_ADDR[15:3]}, where XDATA_ADDR[15:0] are MCU XDATA addresses of 64k bytes.	
64h (2BC9h)	**REG2BC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP[15:8]	7:0	See description of '2BC8h'.	
65h (2BCAh)	**REG2BCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR_1[7:0]	7:0	Low bound address of MCU XDATA mapping to MIU. The unit is 1k bytes. The XDATA address is hit if (XB_ADDR_1[15:8] > XDATA_ADDR[15:10] >= XB_ADDR_1[7:0]).	
65h (2BCBh)	**REG2BCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	XB_ADDR_1[15:8]	7:0	See description of '2BCAh'.	

XDMIU Register (Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
66h (2BCCh)	**REG2BCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_0[7:0]	7:0	Low byte address to access XDATA from MIU. The granularity is 1k bytes. The actual address[23:0] to MIU would be {SDR_XD_MAP_1_1[0], SDR_XD_MAP_1_0[15:8], SDR_XD_MAP_1_0[7:0], XDATA_ADDR[9:3]}, where XDATA_ADDR[15:0] are MCU XDATA addresses of 64k bytes.	
66h (2BCDh)	**REG2BCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_0[15:8]	7:0	See description of '2BCCh'.	
67h (2BCEh)	**REG2BCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_1[7:0]	7:0	Low byte address to access XDATA from MIU. The granularity is 1k bytes. The actual address[23:0] to MIU would be {SDR_XD_MAP_1_1[0], SDR_XD_MAP_1_0[15:8], SDR_XD_MAP_1_0[7:0], XDATA_ADDR[9:3]}, where XDATA_ADDR[15:0] are MCU XDATA addresses of 64k bytes.	
67h (2BCFh)	**REG2BCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	SDR_XD_MAP_1_1[15:8]	7:0	See description of '2BCEh'.	

AUDIO0 Register (Bank = 2C)

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2C00h)	**REG2C00**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CLKGEN_RESET	1	Audio engine clkgen reset. 0: Normal. 1: Reset.	
	SOFTWARE_RESET	0	Audio engine software reset. 0: Normal. 1: Reset. Note: This command cannot reset register value.	
01h (2C02h)	**REG2C02**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_CARD_READER_FIX_SYNTH	7	Enable card reader audio sample frequency fixed synthesizer module. 0: Disable. 1: Enable (256Fs).	
	EN_DVB_FIX_SYNTH	6	Enable DVB audio sample frequency fixed synthesizer module. 0: Disable. 1: Enable (256Fs).	
	EN_DVB_SYNC_SYNTH	5	Enable DVB audio sample frequency synthesizer module, synchronous to 27MHz clock. 0: Disable. 1: Enable (256Fs).	
	I2S_IN_FMT	4	Configure input I2S interface format. 0: I2S justified (standard format). 1: Left-justified.	
	EN_I2S_SYNTH	3	Enable I2S audio sample frequency synthesizer module. 0: Disable. 1: Enable (256Fs).	
	EN_SIF_SYNTH	2	Enable SIF audio sample frequency synthesizer module. 0: Disable. 1: Enable (256Fs).	
	EN_SPDIF_CDR	1	Enable S/PDIF input clock data recovery module. 0: Disable. 1: Enable (256Fs).	
	EN_ADC_SYNTH	0	Enable ADC audio sample frequency synthesizer module. 0: Disable.	

AUDIO0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable (256Fs).	
01h (2C03h)	**REG2C03**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPDIF_IN_BLOCK_NO_CHECK	7	Don't care the block interval of SPDIF IN. 0: Normal. 1: Enable (don't care).	
	AUTO_CLEAR_PC_PD	6	Auto clear PC & PD. 0: Enable. 1: Disable.	
	-	5	Reserved.	
	EN_768_FS_SYNTH	4	Enable 768 fs audio sample frequency synthesizer module. 0: Disable. 1: Enable (256Fs).	
	-	3	Reserved.	
	DVB_PLL_LOCK_CURRENT_FREQ	2	Force lock current DVB SYNC synthesizer frequency. 0: Disable. 1: Enable.	
	DVB_FREQ_GAIN	1	Audio DVB SYNC synthesizer Cs gain selection. 0: Normal. 1: Enhanced (smaller Cs).	
	DVB_PHASE_GAIN	0	Audio DVB SYNC synthesizer Cp gain selection. 0: Normal. 1: Enhanced (smaller Cp).	
02h (2C04h)	**REG2C04**	**7:0**	**Default : 0x00**	**Access : RO**
	DVB_SYNC_FREQ[7:0]	7:0	Audio DVB SYNC synthesizer frequency value.	
02h (2C05h)	**REG2C05**	**7:0**	**Default : 0x00**	**Access : RO**
	DVB_SYNC_NO_SIGNAL	7	Audio DVB SYNC synthesizer input signal detect. 0: Signal detected. 1: No signal input.	
	DVB_SYNC_FREQ[14:8]	6:0	See description of '2C04h'.	
03h (2C06h)	**REG2C06**	**7:0**	**Default : 0x00**	**Access : RO**
	I2S_FREQ[7:0]	7:0	Audio I2S clock data recovery frequency value.	
03h (2C07h)	**REG2C07**	**7:0**	**Default : 0x00**	**Access : RO**
	I2S_NO_SIGNAL	7	Audio I2S clock data recovery input signal detect. 0: Signal detected. 1: No signal input.	
	I2S_FREQ[14:8]	6:0	See description of '2C06h'.	

AUDIO0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
04h (2C08h)	**REG2C08**	**7:0**	**Default : 0x00**	**Access : RO**
	SIF_FREQ[7:0]	7:0	Audio SIF clock data recovery frequency value.	
04h (2C09h)	**REG2C09**	**7:0**	**Default : 0x00**	**Access : RO**
	SIF_NO_SIGNAL	7	Audio SIF clock data recovery input signal detect. 0: Signal detected. 1: No input signal.	
	SIF_FREQ[14:8]	6:0	See description of '2C08h'.	
06h (2C0Ch)	**REG2C0C**	**7:0**	**Default : 0x00**	**Access : RO**
	HDMI_MODE[1:0]	7:6	Status of audio stream from HDMI input interface. 00: PCM audio. 01: Non-PCM (Compressed) audio. 10: One Bit Audio. 11: N/A.	
	HDMI_AUDIO_MUTE	5	Status of HDMI audio decoder (pre-setting error event). 0: Normal. 1: Mute.	
	HDMI_AVMUTE	4	Decoded AVMUTE bit from HDMI received General Control packet. 0: Clear AVMUTE. 1: Set AVMUTE.	
	-	3:0	Reserved.	
10h (2C20h)	**REG2C20**	**7:0**	**Default : 0x32**	**Access : R/W**
	AUPLL_RST	7	HDMI audio PLL reset. 0: No action. 1: Reset.	
	AUPLL_ICTRL[2:0]	6:4	Audio HDMI CODEC PLL charge pump current control.	
	AUPLL_PDN	3	DMI audio PLL power down. 0: No action. 1: Power down.	
	AUPLL_RCTRL[2:0]	2:0	Audio HDMI CODEC PLL loop filter resistor control. R: 15 +5* RCTRL (kohm).	
11h (2C22h)	**REG2C22**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUPLL_TEST_IN[7:0]	7:0	HDMI AUPLL test input.	
11h (2C23h)	**REG2C23**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUPLL_TEST_IN[15:8]	7:0	See description of '2C22h'.	
12h	**REG2C24**	**7:0**	**Default : 0x00**	**Access : R/W**

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2C24h)	AUPLL_VCO_OFFSET	7	Enable VCO free running. 0: Enable. 1: Disable.	
	AUPLL_INTDIVIDE	6	Enable intercept audio driver in HDMI PLL synthesizer. 0: Normal. 1: Enable.	
	EN_CLKPIX2X	5	Enable video clock 2x output clock. 0: Disable. 1: Enable.	
	AUPLL_LCKDCT	4	Enable TMDS PLL lock detection. 0: Disable. 1: Enable.	
	AUPLL_PORST	3	HDMI audio PLL reset. 0: Normal. 1: Reset (all analog front-end & dividers).	
	AUPLL_RESETP	2	HDMI audio PLL post clock divider reset (KP). 0: Normal. 1: Reset.	
	AUPLL_RESETF	1	HDMI audio PLL feedback clock divider reset (FBDIV & KM). 0: Normal. 1: Reset.	
	-	0	Reserved.	
13h (2C26h)	**REG2C26**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUPLL_KP[3:0]	7:4	HDMI PLL post divider ratio (KP) for new mode. 0000: /1. 0001: /2. 0010: /4. ... 1001: /512. 1010: /1024. 1011: /1024. ... 1111: /1024.	
	AUPLL_KM[3:0]	3:0	HDMI PLL KM divider ratio for new mode. 0000: /1. 0001: /2. 0010: /4. ...	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0111: /128. 1000: /256. 1001: /256. ... 1111: /256.	
13h (2C27h)	**REG2C27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	AUPLL_KN[1:0]	1:0	HDMI PLL KN divider ratio for new mode. 00: /1. 01: /2. 10: /4. 11: /4.	
14h (2C28h)	**REG2C28**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUPLL_DDIV[3:0]	7:4	HDMI PLL input overwrite divider value from noise-shape quantizer for new mode. 0000: N.A. (/16). 0001: N.A. (/17). 0010: /2. 0011: /3. ... 1111: /15.	
	AUPLL_FBDIV[3:0]	3:0	HDMI PLL feedback overwrite divider value from noise-shape quantizer for new mode. 0000: N.A. (/16). 0001: N.A. (/17). 0010: /2. 0011: /3. ... 1111: /15.	
15h (2C2Ah)	**REG2C2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_CTS_N_SYNTH	7	Audio HDMI CTS-N synthesizer control. 0: Idle. 1: Enable (never disable CTS-N synthesizer after it is enabled).	
	-	6	Reserved.	
	SYNTH_PLL_LOCK_SEL	5	Audio HDMI CTS-N synthesizer lock function select. 0: Manual. 1: Auto.	

AUDIO0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
	SYNTH_256FS_EXPANDER	4	S/PDIF 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width).
	SYNTH_PLL_LOCK_FREQ	3	Audio HDMI CTS-N synthesizer lock current frequency. 0: Normal. 1: Lock.
	SYNTH_FREQ_GAIN	2	Audio HDMI CTS-N synthesizer Cs gain selection. 0: Normal. 1: Enhanced (smaller Cs).
	SYNTH_PH_GAIN	1	Audio HDMI CTS-N synthesizer Cp gain selection. 0: Normal. 1: Enhanced (smaller Cp).
	SYNTH_SEL_CTS_REF	0	Audio HDMI CTS-N synthesizer CTS REF selection. 0: Select CTS FIFO out valid. 1: Select CTS[19:0].
15h (2C2Bh)	**REG2C2B**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	NO_INPUT_CTRL_EN	3	Enable no input HDMI clock to mute audio.
	SYNTH_NO_INPUT_LOCK_EN	2	Enable CTS N synthesizer to lock no input control signal output. 0: Unlock. 1: Lock.
	SYNTH_NO_INPUT_SEL	1	CTS N synthesizer selection of lock or unlock no input signal to control output 256fs. 0: Select unlock no input signal. 1: Select lock no input signal.
	CLR_SYNTH_LOCK	0	Clear synthesizer's lock state. 0: Normal. 1: Clear.
16h (2C2Ch)	**REG2C2C**	**7:0**	**Default : 0x00** **Access : RO**
	CTS_N_SYNTH_FREQ[7:0]	7:0	Audio HDMI CTS-N synthesizer frequency value.
16h (2C2Dh)	**REG2C2D**	**7:0**	**Default : 0x00** **Access : RO**
	DVI_NO_INPUT	7	Audio HDMI CTS-N synthesizer input signal detect. 0: Signal detected. 1: No input signal.
	CTS_N_SYNTH_FREQ[14:8]	6:0	See description of '2C2Ch'.

AUDIO0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
17h (2C2Eh)	**REG2C2E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	AUPLL_HIGH_FLAG	1	HDMI AUPLL VCO too high flag.	
	AUPLL_LOCK	0	HDMI AUPLL lock indication.	
18h (2C30h)	**REG2C30**	**7:0**	**Default : 0x0A**	**Access : R/W**
	VCLK_CHK_RANGE[7:0]	7:0	HDMI video clock check range. The video clock is judged as stable if the jitter of video clock count number is smaller than this range.	
18h (2C31h)	**REG2C31**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:5	Reserved.	
	REF_CNT_NUM_SEL	4	Period for checking video clock. 0: 128 XTAL clock. 1: 256 XTAL clock.	
	VCLK_STABLE_TIMES[3:0]	3:0	Stable video clock check times.	
19h (2C32h)	**REG2C32**	**7:0**	**Default : 0x00**	**Access : RO**
	VIDEO_CLK_CNT[7:0]	7:0	HDMI video clock count.	
19h (2C33h)	**REG2C33**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	VCLK_STABLE	5	HDMI video clock stable indication.	
	VIDEO_CLK_CNT[12:8]	4:0	See description of '2C32h'.	
1Ah (2C34h)	**REG2C34**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_AUDIO_MUTE_EN[3:0]	7:4	Enable the following events to mute HDMI audio. [0]: CTS-N big change. [1]: Video clock frequency big change. [2]: HDMI AVMUTE. [3]: Reserved.	
	SYNTH_PLL_LOCK_EN[3:0]	3:0	Enable the following events to freeze audio HDMI CTS-N synthesizer. [0]: CTS-N big change. [1]: Video clock frequency big change. [3:2]: Reserved.	
20h (2C40h)	**REG2C40**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HDMI_PC[7:0]	7:0	HDMI input non-PCM preamble Pc.	
20h (2C41h)	**REG2C41**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HDMI_PC[15:8]	7:0	See description of '2C40h'.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (2C42h)	**REG2C42**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HDMI_PD[7:0]	7:0	HDMI input non-PCM preamble Pd.	
21h (2C43h)	**REG2C43**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HDMI_PD[15:8]	7:0	See description of '2C42h'.	
22h (2C44h)	**REG2C44**	**7:0**	**Default : 0x10**	**Access : R/W**
	HDMI_MATRIX0[7:0]	7:0	[15] Reserved. [14:12] HDMI Audio channel 4 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. d110: Mapped from channel 7. 111: Mapped from channel 8. [11] Reserved. [10:8] HDMI Audio channel 3 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8. [7] Reserved. [6:4] HDMI Audio channel 2 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8. [3] Reserved. [2:0] HDMI Audio channel 1 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8.	
22h (2C45h)	**REG2C45**	**7:0**	**Default : 0x32**	**Access : R/W**
	HDMI_MATRIX0[15:8]	7:0	See description of '2C44h'.	
23h (2C46h)	**REG2C46**	**7:0**	**Default : 0x54**	**Access : R/W**
	HDMI_MATRIX1[7:0]	7:0	[15] Reserved. [14:12] HDMI Audio channel 8 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8. [11] Reserved. [10:8] HDMI Audio channel 7 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8. [7] Reserved. [6:4] HDMI Audio channel 6 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[3] Reserved. [2:0] HDMI Audio channel 5 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8.	
23h (2C47h)	**REG2C47**	**7:0**	**Default : 0x76**	**Access : R/W**
	HDMI_MATRIX1[15:8]	7:0	See description of '2C46h'.	
24h (2C48h)	**REG2C48**	**7:0**	**Default : 0x00**	**Access : R/W**
	DOWN_SAMPLE[7:0]	7:0	[15:14] Input SRC path down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved. [13:8] Reserved. [7:6] Input DVB down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved. [5:4] Input I2S down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved. [3:2] Input SPDIF down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved. [1:0] Input HDMI down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (2C50h)	**REG2C50**	**7:0**	**Default : 0x0F**	**Access : R/W**
	DAC_CMP0[7:0]	7:0	Coefficient 0 of DAC's compensation filter.	
28h (2C51h)	**REG2C51**	**7:0**	**Default : 0x00**	**Access : R/W**
	DAC_CMP0[15:8]	7:0	See description of '2C50h'.	
29h (2C52h)	**REG2C52**	**7:0**	**Default : 0xA4**	**Access : R/W**
	DAC_CMP1[7:0]	7:0	Coefficient 1 of DAC's compensation filter.	
29h (2C53h)	**REG2C53**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DAC_CMP1[15:8]	7:0	See description of '2C52h'.	
2Ah (2C54h)	**REG2C54**	**7:0**	**Default : 0x40**	**Access : R/W**
	DAC_CMP2[7:0]	7:0	Coefficient 2 of DAC's compensation filter.	
2Ah (2C55h)	**REG2C55**	**7:0**	**Default : 0x7F**	**Access : R/W**
	DAC_CMP2[15:8]	7:0	See description of '2C54h'.	
2Bh (2C56h)	**REG2C56**	**7:0**	**Default : 0x22**	**Access : R/W**
	ADC_CMP0[7:0]	7:0	Coefficient 0 of ADC's compensation filter.	
2Bh (2C57h)	**REG2C57**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADC_CMP0[15:8]	7:0	See description of '2C56h'.	
2Ch (2C58h)	**REG2C58**	**7:0**	**Default : 0xF9**	**Access : R/W**
	ADC_CMP1[7:0]	7:0	Coefficient 1 of ADC's compensation filter.	
2Ch (2C59h)	**REG2C59**	**7:0**	**Default : 0xFE**	**Access : R/W**
	ADC_CMP1[15:8]	7:0	See description of '2C58h'.	
2Dh (2C5Ah)	**REG2C5A**	**7:0**	**Default : 0x61**	**Access : R/W**
	ADC_CMP2[7:0]	7:0	Coefficient 2 of ADC's compensation filter.	
2Dh (2C5Bh)	**REG2C5B**	**7:0**	**Default : 0x44**	**Access : R/W**
	ADC_CMP2[15:8]	7:0	See description of '2C5Ah'.	
2Eh (2C5Ch)	**REG2C5C**	**7:0**	**Default : 0x34**	**Access : R/W**
	ADC_GAIN[7:0]	7:0	Pre-scale of ADC's decimation filter (format: unsigned 2.14).	
2Eh (2C5Dh)	**REG2C5D**	**7:0**	**Default : 0x73**	**Access : R/W**
	ADC_GAIN[15:8]	7:0	See description of '2C5Ch'.	
30h (2C60h)	**REG2C60**	**7:0**	**Default : 0x00**	**Access : R/W**
	DECODER1_CFG[7:0]	7:0	[7:3] Reserved. [2:0] DSP decoder input function selection. 000: TSP Data (DVB synthesizer). 001: TSP Data (Card Reader synthesizer). 010: S/PDIF non-PCM (SPDIF synthesizer).	

AUDIO0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description	
			011: SIF (SIF synthesizer). 100: HDMI non-PCM (CTS-N synthesizer). Others: Reserved.	
31h (2C62h)	**REG2C62**	**7:0**	**Default : 0x00**	**Access : R/W**
	DECODER2_CFG[7:0]	7:0	[3] Bypass mode for AUDIO_SPDIF_NONPCM_DECODER. [2:0] DSP decoder input function selection. 000: HDMI non-PCM (CTS-N synthesizer). 001: SIF (Card Reader synthesizer). 010: S/PDIF non-PCM (SPDIF synthesizer). 011: SIF (SIF synthesizer). 100: TSP2 Data (Card Reader synthesizer). 101: TSP2 Data (DVB synthesizer). Others: Reserved.	
32h (2C64h)	**REG2C64**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_CFG[7:0]	7:0	[7] Audio output channel 1 enable setting. 0: Idle (power saving). 1: Enable. [6] Audio output channel 1 source clock selection. 0: Normal. 1: Synchronous to codec PLL (while codec PLL reference clock is the same as this channel). [5] Audio output channel 1 sampling rate converter setting. 0: Normal. 1: SRC mode. [4] Audio output channel 1 over sampling rate setting. 0: 128 fs. 1: 256 fs. [3] Audio output channel 1 sigma delta modulator enable setting. 0: Idle (power saving). 1: Enable. [2:0] Audio output channel 1 source selection. 000: From DSP decoder1 output. 001: From DSP decoder2 output. 010: From audio ADC. 011: From input S/PDIF interface. 100: From input I2S interface. 101: From HDMI (sample stream 1 & 2). 110: Reserved.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			111: From decimation output.	
33h (2C66h)	**REG2C66**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH2_CFG[7:0]	7:0	[7] Audio output channel 2 enable setting. 0: Idle (power saving). 1: Enable. [6] Audio output channel 2 source clock selection. 0: Normal. 1: Synchronous to codec PLL (while codec PLL reference clock is the same as this channel). [5] Audio output channel 2 sampling rate converter setting. 0: Normal. 1: SRC mode. [4] Audio output channel 2 over sampling rate setting. 0: 128 fs. 1: 256 fs. [3] Audio output channel 2 sigma delta modulator enable setting. 0: Idle (power saving). 1: Enable. [2:0] Audio output channel 2 source selection. 000: From DSP decoder1 output. 001: From DSP decoder2 output. 010: From audio ADC. 011: From input S/PDIF interface. 100: From input I2S interface. 101: From HDMI (sample stream 3 & 4). 110: Reserved. 111: From decimation output.	
34h (2C68h)	**REG2C68**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH3_CFG[7:0]	7:0	[7] Audio output channel 3 enable setting. 0: Idle (power saving). 1: Enable. [6] Audio output channel 3 source clock selection. 0: Normal. 1: Synchronous to codec PLL (while codec PLL reference clock is the same as this channel). [5] Audio output channel 3 sampling rate converter setting. 0: Normal. 1: SRC mode.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			[4] Audio output channel 3 over sampling rate setting. 0: 128 fs. 1: 256 fs. [3] Audio output channel 3 sigma delta modulator enable setting. 0: Idle (power saving). 1: Enable. [2:0] Audio output channel 3 source selection. 000: From DSP decoder1 output. 001: From DSP decoder2 output. 010: From audio ADC. 011: From input S/PDIF interface. 100: From input I2S interface. 101: From HDMI (sample stream 5 & 6). 110: Reserved. 111: From decimation output.
35h (2C6Ah)	**REG2C6A**	**7:0**	**Default : 0x00** **Access : R/W**
	CH4_CFG[7:0]	7:0	[7] Audio output channel 4 enable setting. 0: Idle (power saving). 1: Enable. [6] Audio output channel 4 source clock selection. 0: Normal. 1: Synchronous to codec PLL (while codec PLL reference clock is the same as this channel). [5] Audio output channel 4 sampling rate converter setting. 0: Normal. 1: SRC mode. [4] Audio output channel 4 over sampling rate setting. 0: 128 fs. 1: 256 fs. [3] Audio output channel 4 sigma delta modulator enable setting. 0: Idle (power saving). 1: Enable. [2:0] Audio output channel 4 source selection. 000: From DSP decoder1 output. 001: From DSP decoder2 output. 010: From audio ADC. 011: From input S/PDIF interface. 100: From input I2S interface.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			101: From HDMI (sample stream 7 & 8). 110: Reserved. 111: Reserved.	
36h (2C6Ch)	**REG2C6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INPUT_REGEN_CFG[7:0]	7:0	[13] TIMING_GEN genshot selection. 0: Bypass genshot (recommended). 1: Use genshot. [12:9] Reserved. [8] Fixed SPDIF, I2S & M-Link Extra PCM SRC mode. 0: Disable. 1: Enable (recommended). [7] HDMI clock auto re-generator function enable. 0: Disable. 1: Enable. [6] SIF clock auto re-generator function enable. 0: Disable. 1: Enable. [5] I2S clock auto re-generator function enable. 0: Disable. 1: Enable. [4] S/PDIF clock auto re-generator function enable. 0: Disable. 1: Enable. [3] DVB clock auto re-generator function enable. 0: Disable. 1: Enable. [2] SRC mode for SPDIF. 0: Normal. 1: Enable. [1] SRC mode for 1st I2S encoder. 0: Normal. 1: Enable. [0] Reserved.	
36h (2C6Dh)	**REG2C6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	INPUT_REGEN_CFG[15:8]	7:0	See description of '2C6Ch'.	
40h (2C80h)	**REG2C80**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPDIF_OUT_CS0[7:0]	7:0	S/PDIF Output Channel Status [0:7] (refer to CR04.4).	
41h	**REG2C82**	**7:0**	**Default : 0x00**	**Access : R/W**

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2C82h)	SPDIF_OUT_CS1[7:0]	7:0	S/PDIF Output Channel Status [8:15] (refer to CR04.4).	
42h (2C84h)	**REG2C84**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPDIF_OUT_CS2[7:0]	7:0	S/PDIF Output Channel Status [16:23] (refer to CR04.4).	
43h (2C86h)	**REG2C86**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPDIF_OUT_CS3[7:0]	7:0	S/PDIF Output Channel Status [24:31] (refer to CR04.4).	
44h (2C88h)	**REG2C88**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPDIF_OUT_CS4[7:0]	7:0	S/PDIF Output Channel Status [32:39] (refer to CR04.4).	
45h (2C8Ah)	**REG2C8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SPDIF_OUT_CFG[7:0]	7:0	[15] Insert Validity Bit. 0: Disable. 1: Enable. [14] SPDIF source selection. 0: Data after Sound Effect. 1: Data before Sound Effect. [13:11] Reserved. [10] Counter reset value selection. 0: Counter value set 0. 1: Counter value set 64 (recommended). [9] Automatically synchronize input and output timing of the S/PDIF encoders. Set to 0 in SRC mode. 0: Disable. 1: Enable (recommended). [8] Automatically synchronize input and output timing of the S/PDIF encoders. Set to 0 in SRC mode. 0: Disable. 1: Enable. [7] Audio output channel S/PDIF enable setting. 0: Idle (power saving). 1: Enable. [6] Reset S/PDIF output modules. This bit shall be toggled after data or clock is changed for S/PDIF output modules. 0: Normal. 1: Reset (synchronous input Fs and output Fs). [5] Audio output channel S/PDIF sampling rate converter setting.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			0: Normal. 1: SRC mode. [4] Enable channel status insertion for output S/PDIF module. 0: Disable (refer from S/PDIF / HDMI input channel status). 1: Enable (refer from SPDIF_OUT_CS0..4). [3] Audio output channel 1/2/3/4 test source selection. 0: Normal (16 bits). 1: From DSP output 24-bit interface (only without SRC) (only for SEL_SPDIF_CH[1:0]). [2:0] Audio output channel S/PDIF source selection (16/24 bits). 000: From audio output channel 1. 001: From audio output channel 2. 010: From audio output channel 3. 011: From audio output channel 4. 100: HDMI bypass. 101: DVB non-PCM output. 110: N.A. 111: N.A.
45h (2C8Bh)	**REG2C8B**	**7:0**	**Default : 0x00** **Access : R/W**
	SPDIF_OUT_CFG[15:8]	7:0	See description of 2C8Ah.
46h (2C8Ch)	**REG2C8C**	**7:0**	**Default : 0x00** **Access : R/W**
	I2S_OUT1_CFG[7:0]	7:0	[15] Audio output channel I2S enable setting. 0: Idle (power saving). 1: Enable. [14] Reset I2S output modules. This bit shall be toggled after data or clock is changed for I2S output modules. 0: Normal. 1: Reset (synchronous input Fs and output Fs). [13] Automatically synchronize input and output timing of the I2S encoders. Set to 0 in SRC mode. 0: Disable. 1: Enable (recommended). [12] Counter reset value selection. 0: Counter value set 0. 1: Counter value set 16 (recommended). [11] Audio output channel 1/2/3/4 test source selection.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Normal (16-bit). 1: From DSP output 24-bit interface (only without SRC) (only for SEL_I2S_CH[1:0]). [10] Audio output channel I2S source selection (24-bit). 0: Normal (following SEL_I2S_CH[1:0]). 1: From HDMI audio link. [9:8] Audio output channel I2S source selection (16/24 bits). 00: From audio output channel 1. 01: From audio output channel 2. 10: From audio output channel 3. 11: From audio output channel 4. [7] Automatically synchronize input and output timing of the I2S encoders. Set to 0 in SRC mode. 0: Disable. 1: Enable. [6:4] Clock frequency select for AUMCKO output pin (I2S MCLK). 000: Synthesizer 64 Fs. 001: Synthesizer 128 Fs. 010: Synthesizer 256 Fs. 011: Test clock (only for VLSI designer). 100: PLL 64 Fs. 101: PLL 128 Fs. 110: PLL 256 Fs. 111: PLL 384 Fs. [3] Output I2S interface format. 0: I2S-justified (standard format). 1: Left-justified. [2:0] Output I2S interface encoder word width (bit rate). 000: Synthesizer 16 clock cycles per sample word (16-bit). 001: Reserved. 010: Synthesizer 32 clock cycles per sample word (32-bit). 011: Reserved. 100: PLL 16 clock cycles per sample word (16-bit). 101: PLL 24 clock cycles per sample word (24-bit). 110: PLL 32 clock cycles per sample word (32-bit). 111: Reserved.	
46h (2C8Dh)	**REG2C8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	I2S_OUT1_CFG[15:8]	7:0	See description of '2C8Ch'.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
47h (2C8Eh)	**REG2C8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	I2S_OUT2_CFG[7:0]	7:0	[15:0] Reserved.	
47h (2C8Fh)	**REG2C8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	I2S_OUT2_CFG[15:8]	7:0	See description of '2C8Eh'.	
48h (2C90h)	**REG2C90**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PAD_CFG[7:0]	7:0	[15:12] Reserved. [11:10] SPDIF pad output source selection. 00: SPDIF output. 01: I2S SD1 output. 10: I2S SD2 output. 11: I2S SD3 output. [9:8] I2S MCLK pad output source selection. 00: I2S MCLK output. 01: I2S SD1 output. 10: I2S SD2 output. 11: I2S SD3 output. [7:6] I2S output mux control. 2: DSD output interface. Others: I2S output interfaces. [5:2] Reserved. [1] Output enable for the first I2S interface pins. 0: Enable. 1: Tri-state. [0] Output enable for SPDIFO output pin (S/PDIF Output). 0: Enable. 1: Tri-state.	
48h (2C91h)	**REG2C91**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAD_CFG[15:8]	7:0	See description of '2C90h'.	
49h (2C92h)	**REG2C92**	**7:0**	**Default : 0x00**	**Access : R/W**
	MUTE_CFG[7:0]	7:0	[7:6] Output selection for the MUTE output pin. 00: MUTE. 01: SD_1. 10: SD_2. 11: SD_3. [5:4] Select source for output AUMUTE pin (Audio Mute). 00: From audio DSP channel 1 mute control. 01: From audio DSP channel 2 mute control. 10: From audio DSP channel 3 mute control.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			11: From audio DSP channel 4 mute control. [3] Reserved. [2] Mute function setting on AUMUTE pin (Audio Mute). 0: Disable. 1: Output is active. [1] Configure AUMUTE output polarity (Audio Mute). 0: Active-low for mute. 1: Active-high for mute. [0] Output enable for AUMUTE output pin (Audio Mute). 0: Enable. 1: Tri-state.
4Ah (2C94h)	**REG2C94**	**7:0**	**Default : 0x00** **Access : R/W**
	MUTE_CTRL1[7:0]	7:0	[7] Enable Audio DSP channel 1 mute from SIF mute. 0: Disable. 1: Enable. [6] Enable Audio DSP channel 1 mute when DSD audio stream is received from HDMI receiver. 0: Disable. 1: Enable. [5] Enable Audio DSP channel 1 mute from HDMI (flat sample, decode error, PLL unlock, etc). 0: Disable. 1: Enable. [4] Enable Audio DSP channel 1 mute when AVMUTE signal is received from HDMI receiver. 0: Disable. 1: Enable. [3] Enable Audio DSP channel 1 mute when non-PCM audio stream is received from HDMI receiver. 0: Disable. 1: Enable. [2] Enable Audio DSP channel 1 mute when SPDIF input decoding error occurs. 0: Disable. 1: Enable. [1] Enable Audio DSP channel 1 mute when non-PCM audio stream is received from SPDIF input. 0: Disable. 1: Enable. [0] Enable Audio DSP channel 1 force Mute control.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Mute. 1: Normal.	
4Bh (2C96h)	**REG2C96**	**7:0**	**Default : 0x00**	**Access : R/W**
	MUTE_CTRL2[7:0]	7:0	[7] Enable Audio DSP channel 2 mute from SIF mute. 0: Disable. 1: Enable. [6] Enable Audio DSP channel 2 mute when DSD audio stream is received from HDMI receiver. 0: Disable. 1: Enable. [5] Enable Audio DSP channel 2 from HDMI (flat sample, decode error, PLL unlock, etc). 0: Disable. 1: Enable. [4] Enable Audio DSP channel 2 mute when AVMUTE signal is received from HDMI receiver. 0: Disable. 1: Enable. [3] Enable Audio DSP channel 2 mute when non-PCM audio stream is received from HDMI receiver. 0: Disable. 1: Enable. [2] Enable Audio DSP channel 2 mute when SPDIF input decoding error occurs. 0: Disable. 1: Enable. [1] Enable Audio DSP channel 2 mute when non-PCM audio stream is received from SPDIF input. 0: Disable. 1: Enable. [0] Enable Audio DSP channel 2 force Mute. 0: Mute. 1: Normal.	
4Ch (2C98h)	**REG2C98**	**7:0**	**Default : 0x00**	**Access : R/W**
	MUTE_CTRL3[7:0]	7:0	[7] Enable Audio DSP channel 3 mute from SIF mute. 0: Disable. 1: Enable. [6] Enable Audio DSP channel 3 mute when DSD audio stream is received from HDMI receiver.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable. [5] Enable Audio DSP channel 3 from HDMI (flat sample, decode error, PLL unlock, etc). 0: Disable. 1: Enable. [4] Enable Audio DSP channel 3 mute when AVMUTE signal is received from HDMI receiver. 0: Disable. 1: Enable. [3] Enable Audio DSP channel 3 mute when non-PCM audio stream is received from HDMI receiver. 0: Disable. 1: Enable. [2] Enable Audio DSP channel 3 mute when SPDIF input decoding error occurs. 0: Disable. 1: Enable. [1] Enable Audio DSP channel 3 mute when non-PCM audio stream is received from SPDIF input. 0: Disable. 1: Enable. [0] Enable Audio DSP channel 3 force Mute. 0: Mute. 1: Normal.	
4Dh (2C9Ah)	**REG2C9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MUTE_CTRL4[7:0]	7:0	[7] Enable Audio DSP channel 4 mute from SIF mute. 0: Disable. 1: Enable. [6] Enable Audio DSP channel 4 mute when DSD audio stream is received from HDMI receiver. 0: Disable. 1: Enable. [5] Enable Audio DSP channel 4 from HDMI (flat sample, decode error, PLL unlock, etc). 0: Disable. 1: Enable. [4] Enable Audio DSP channel 4 mute when AVMUTE signal is received from HDMI receiver. 0: Disable.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			1: Enable. [3] Enable Audio DSP channel 4 mute when non-PCM audio stream is received from HDMI receiver. 0: Disable. 1: Enable. [2] Enable Audio DSP channel 4 mute when SPDIF input decoding error occurs. 0: Disable. 1: Enable. [1] Enable Audio DSP channel 4 mute when non-PCM audio stream is received from SPDIF input. 0: Disable. 1: Enable. [0] Enable Audio DSP channel 4 force Mute. 0: Mute. 1: Normal.
50h (2CA0h)	**REG2CA0**	**7:0**	**Default : 0xA9** **Access : R/W**
	CODEC_SYNTH[7:0]	7:0	CODEC synthesizer N.f = 6.10. 256fs = 214 / N.f.
50h (2CA1h)	**REG2CA1**	**7:0**	**Default : 0x45** **Access : R/W**
	CODEC_SYNTH[15:8]	7:0	See description of '2CA0h'.
51h (2CA2h)	**REG2CA2**	**7:0**	**Default : 0x00** **Access : R/W**
	PLL_REF_CFG[7:0]	7:0	[6:4] SRC 256FS clock selection. 000: From DSP decoder1 input. 001: From DSP decoder2 input. 010: From Audio ADC. 011: From input S/PDIF interface. 100: From input I2S interface. 101: From HDMI. 110: From HDMI. 111: From MPLL/15 or AU_PLL. [3] Audio codec PLL reference clock control. 0: Stop. 1: Enable. [2:0] Audio codec PLL reference clock selection. 000: From DSP decoder1 input. 001: From DSP decoder2 input. 010: From Audio ADC. 011: From input S/PDIF interface.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			100: From input I2S interface. 101: From HDMI. 110: From HDMI. 111: From HDMI.	
52h (2CA4h)	**REG2CA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG0[7:0]	7:0	[15] Audio CLK_150MHZ_ZR_MAC selection. 0: SIF PLL 8X /3 (recommended). 1: SIF PLL 8X /2.5. [14:13] Audio CLK_256FS_ADC_IN selection. 00: Codec synthesizer 128 FS. 01: Codec synthesizer 256 FS. 10: Codec PLL 128 FS. 11: Codec PLL 256 FS. [12] Audio CLK_SPDIF_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [11] Audio CLK_I2S_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [10] Audio CLK_SIF_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [9] Audio CLK_CODEC_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [8] Audio CLK_HDMI_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [7:6] Audio SIF FM demodulator clock source selection. 00: MPLL / 4. 01: MPLL / 2 (recommended). 10: VIF-ADC Clock. 11: SIF-ADC Clock. [5]: Reserved. [4] Audio codec PLL post divider stage 2 selection. 0: Selected by SEL_C768NFS_DIV (recommended). 1: Divide by 5. [3] Audio SIF channel enable setting. 0: Idle (power saving). 1: Enable.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			[2] Audio HDMI ACR engine selection. 0: Normal mode. 1: Test mode (CTS_N digital synthesizer). [1:0] Audio codec PLL post divider stage 2 selection. 00: Divide by 1 when SEL_C768NFS_DIV5 is set to 0. 01: Divide by 2 when SEL_C768NFS_DIV5 is set to 0. 10: Divide by 3 when SEL_C768NFS_DIV5 is set to 0. 11: Divide by 4 when SEL_C768NFS_DIV5 is set to 0. xx: Divide by 5 when SEL_C768NFS_DIV5 is set to 1.
52h (2CA5h)	**REG2CA5**	**7:0**	**Default : 0x00** **Access : R/W**
	CLK_CFG0[15:8]	7:0	See description of '2CA4h'.
53h (2CA6h)	**REG2CA6**	**7:0**	**Default : 0x00** **Access : R/W**
	CLK_CFG1[7:0]	7:0	[15] Audio CLK_MCLK_I2S_ENCODER invert setting. 0: Normal. 1: Invert. [14] Audio CLK_SPDIF_ENCODER invert setting. 0: Normal. 1: Invert. [13] Audio CLK_SPDIF_DECODER invert setting. 0: Normal. 1: Invert. [12] Audio CLK_SPDIF_SYNTH invert setting. 0: Normal. 1: Invert. [11] Audio CLK_I2S_SYNTH invert setting. 0: Normal. 1: Invert. [10] Audio CLK_SIF_SYNTH invert setting. 0: Normal. 1: Invert. [9] Audio CLK_CODEC_SYNTH invert setting. 0: Normal. 1: Invert. [8] Audio CLK_HDMI_SYNTH invert setting. 0: Normal. 1: Invert. [7] Audio CLK_SIF_ADC_R2B invert setting. 0: Normal. 1: Invert.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[6] Audio CLK_SIF_ADC_R2B_FIFO invert setting. 0: Normal. 1: Invert. [5] Audio CLK_SIF_ADC_CIC invert setting. 0: Normal. 1: Invert. [4] Audio CLK_DSP_230 invert setting. 0: Normal. 1: Invert. [3] Audio CLK_HDMI_DECODER invert setting. 0: Normal. 1: Invert. [2] Audio CLK_64FS_HDMI_DSD invert setting. 0: Normal. 1: Invert. [1] Audio CLK_BCLK_I2S_DECODER invert setting. 0: Normal. 1: Invert. [0] Audio CLK_BCLK_I2S_ENCODER invert setting. 0: Normal. 1: Invert.	
53h (2CA7h)	**REG2CA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG1[15:8]	7:0	See description of '2CA6h'.	
54h (2CA8h)	**REG2CA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG2[7:0]	7:0	[15] Audio CLK_256FS_CH4_OUT invert setting. 0: Normal. 1: Invert. [14] Audio CLK_256FS_CH3_OUT invert setting. 0: Normal. 1: Invert. [13] Audio CLK_256FS_CH2_OUT invert setting. 0: Normal. 1: Invert. [12] Audio CLK_256FS_CH1_OUT invert setting. 0: Normal. 1: Invert. [11] Audio CLK_214M_I2S_SRC invert setting. 0: Normal. 1: Invert.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[10] Audio CLK_214M_SPDIF_SRC invert setting. 0: Normal. 1: Invert. [9] Audio CLK_256FS_ADC_IN invert setting. 0: Normal. 1: Invert. [8] Audio CLK_CODEC_PLL_REF invert setting. 0: Normal. 1: Invert. [7] Audio CLK_256FS_CH4_IN invert setting. 0: Normal. 1: Invert. [6] Audio CLK_256FS_CH3_IN invert setting. 0: Normal. 1: Invert. [5] Audio CLK_256FS_CH2_IN invert setting. 0: Normal. 1: Invert. [4] Audio CLK_256FS_CH1_IN invert setting. 0: Normal. 1: Invert. [3] Audio CLK_214M_CH4_SRC invert setting. 0: Normal. 1: Invert. [2] Audio CLK_214M_CH3_SRC invert setting. 0: Normal. 1: Invert. [1] Audio CLK_214M_CH2_SRC invert setting. 0: Normal. 1: Invert. [0] Audio CLK_214M_CH1_SRC invert setting. 0: Normal. 1: Invert.	
54h (2CA9h)	**REG2CA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG2[15:8]	7:0	See description of '2CA8h'.	
55h (2CAAh)	**REG2CAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG3[7:0]	7:0	[15] Audio CLK_DSP_230 enable setting. 0: Idle (power saving). 1: Enable.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			[14] Audio CLK_HDMI_DECODER enable setting. 0: Idle (power saving). 1: Enable. [13] Audio CLK_64FS_HDMI_DSD enable setting. 0: Idle (power saving). 1: Enable. [12] Audio CLK_BCLK_I2S_DECODER enable setting. 0: Idle (power saving). 1: Enable. [11] Audio CLK_150MHZ_ZR_MAC enable setting. 0: Idle (power saving). 1: Enable. [10] Audio CLK_256FS_ADC_IN enable setting. 0: Idle (power saving). 1: Enable. [9] Reserved. [8] Audio test clock enable setting. 0: Idle (power saving). 1: Enable. [7] Audio CLK_ICE_DSP_230 enable setting. 0: Idle (power saving). 1: Enable. [6] Reserved. [5] Audio CLK_SPDIF_DECODER enable setting. 0: Idle (power saving). 1: Enable. [4] Audio CLK_SPDIF_SYNTH enable setting. 0: Idle (power saving). 1: Enable. [3] Audio CLK_I2S_SYNTH enable setting. 0: Idle (power saving). 1: Enable. [2] Audio CLK_SIF_SYNTH enable setting. 0: Idle (power saving). 1: Enable. [1] Audio CLK_CODEC_SYNTH enable setting. 0: Idle (power saving). 1: Enable. [0] Audio CLK_HDMI_SYNTH enable setting. 0: Idle (power saving).

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Enable.	
55h (2CABh)	**REG2CAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG3[15:8]	7:0	See description of '2CAAh'.	
56h (2CACh)	**REG2CAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG4[7:0]	7:0	[15] Audio CH4 SRC clock system source selection. 0: Analog codec PLL. 1: PLL reference. [14] Audio 768fs clock system source selection. 0: Analog codec PLL. 1: Digital 768fs synthesizer. [13] Audio DAC CH1~3 SRC clock 256fs selection. 0: From 768fs clock system. 1: From MPLL/15. [12] Audio CLK_768FS_PLL_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [11] Audio CLK_DVB_FIX_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [10] Audio CLK_DVB_SYNC_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [9] Audio CLK_27MHZ_DVB_REF source selection. 0: 27 MHz. 1: 13.5 MHz. [8] Audio DVB clock source selection. 0: Sync mode (following system clock). 1: Fixed mode (DSP N.f mode). [7] Reserved. [6] Audio CLK_CARD_READER_SYNTH selection. 0: 214 MHz. 1: 107 MHz. [5] Audio CLK_ CLK_CARD_READER_SYNTH invert setting. 0: Normal. 1: Invert. [4] Audio CLK_CARD_READER_SYNTH enable setting. 0: Idle (power saving). 1: Enable. [3] Audio DAC output SRC clock source selection.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Select codec PLL output clock 256 fs. 1: Select codec PLL reference clock 256 fs. [2:0] Reserved.	
56h (2CADh)	**REG2CAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG4[15:8]	7:0	See description of '2CACh'.	
57h (2CAEh)	**REG2CAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG5[7:0]	7:0	[15] Enable external clock. 0: Disable. 1: Enable. [14] Audio CLK_14318KHZ_FREE enable setting. 0: Idle (power saving). 1: Enable. [13] Audio CLK_214MHZ_MLINK_DECODER enable setting. 0: Idle (power saving). 1: Enable. [12] Audio CLK_ALL_768FS_SYNTH enable setting. 0: Idle (power saving). 1: Enable. [11] Audio CLK_214MHZ_DVB_FIX_SYNTH enable setting. 0: Idle (power saving). 1: Enable. [10] K11B CLK_ALL_DVB_SYNC_SYNTH enable setting (214 MHz / 256 fs feedback / 270 MHz). 0: Idle (power saving). 1: Enable. [9] Audio CLK_256FS_DVB_TIMING_GEN enable setting (Audio CLK_ DSP_DECODER1_TIMING_GEN enable setting). 0: Idle (power saving). 1: Enable. [8] Audio CLK_256FS_SIF_TIMING_GEN enable setting (Audio CLK_ DSP_DECODER2_TIMING_GEN enable setting). 0: Idle (power saving). 1: Enable. [7] Audio INV_CLK_185MHZ_CORDIC invert setting. 0: Normal. 1: Invert. [6] Audio CLK_768FS_PLL_SYNTH invert setting. 0: Normal. 1: Invert.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[5] Audio CLK_128FS_SPDIF_NON_PCM_TRUE invert setting. 0: Normal. 1: Invert. [4] Audio CLK_256FS_DVB_SYNC_SYNTH_TRUE invert setting. 0: Normal. 1: Invert. [3] Audio CLK_214MHZ_DVB_FIX_SYNTH invert setting. 0: Normal. 1: Invert. [2] Audio CLK_214MHZ_DVB_SYNC_SYNTH invert setting. 0: Normal. 1: Invert. [1] Audio CLK_256FS_DVB_TIMING_GEN invert setting (INV_DSP_DECODER1_TIMING_GEN). 0: Normal. 1: Invert. [0] Audio CLK_256FS_SIF_TIMING_GEN invert setting (INV_DSP_DECODER2_TIMING_GEN). 0: Normal. 1: Invert.	
57h (2CAEh)	**REG2CAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG5[15:8]	7:0	See description of '2CAEh'.	
58h (2CB0h)	**REG2CB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG6[7:0]	7:0	[15:14] Reserved. [13] Audio CLK_185MHZ_CORDIC source selection. 0: DSP CLK (recommended). 1: DSP CLK*2/2.5. [12] Reserved. [11:10] Audio SRC_FIX_XTAL_CH4 source selection. 00: Codec PLL (SEL_SRC_SOURCE_SYNTH_CH4 = 0) or Codec PLL ref (SEL_SRC_SOURCE_SYNTH_CH4 = 1). 01: MPLL /15. 10: SYNTH_DVB_FIX_256_FS. 11: SYNTH_CARD_READER_256_FS. [9:8] Audio SIF DSP 216 clock source selection. 00: SIF PLL 8X / 2. 01: SIF PLL 8X / 2.5. 10: SIF PLL 8X / 3.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			11: SIF PLL 8X / 4. [7:6] Audio test clock post divider selection. 00: /1. 01: /2. 10: /4. 11: /8. [5:0] Audio test clock selection. 00h: CLK_50MHZ_SIF_ADC_R2B_Z. 01h: CLK_50MHZ_SIF_ADC_R2B_FIFO_OUT_Z. 02h: CLK_100MHZ_SIF_ADC_CIC_Z. 03h: CLK_150MHZ_DSP_230_Z. 04h: CLK_ICE_DSP_230_Z. 05h: CLK_25MHZ_I_CLAMP_Z. 06h: CLK_150MHZ_ZR_MAC_GATE_Z. 07h: CLK_BCLK_I2S_DECODER_Z. 08h: CLK_BCLK_I2S_ENCODER_Z. 09h: CLK_150MHZ_ZR_MAC_FREE_Z. 0Ah: CLK_128FS_SPDIF_ENCODER_Z. 0Bh: CLK_128FS_SPDIF_DECODER_Z. 0Ch: CLK_214MHZ_SPDIF_SYNTH_Z. 0Dh: CLK_214MHZ_I2S_SYNTH_Z. 0Eh: CLK_214MHZ_SIF_SYNTH_Z. 0Fh: CLK_214MHZ_CODEC_SYNTH_Z. 10h: CLK_256FS_CHANNEL_1_IN_Z. 11h: CLK_256FS_CHANNEL_2_IN_Z. 12h: CLK_256FS_CHANNEL_3_IN_Z. 13h: CLK_256FS_CHANNEL_4_IN_Z. 14h: CLK_214MHZ_CHANNEL_1_SRC_Z. 15h: CLK_214MHZ_CHANNEL_2_SRC_Z. 16h: CLK_214MHZ_CHANNEL_3_SRC_Z. 17h: CLK_214MHZ_CHANNEL_4_SRC_Z. 18h: CLK_256FS_CHANNEL_1_OUT_Z. 19h: CLK_256FS_CHANNEL_2_OUT_Z. 1Ah: CLK_256FS_CHANNEL_3_OUT_Z. 1Bh: CLK_256FS_CHANNEL_4_OUT_Z. 1Ch: CLK_256FS_ADC_IN_Z. 1Dh: CLK_256FS_REF_CODEC_PLL_Z. 1Eh: CLK_128FS_HDMI_Z. 1Fh: CLK_100MHZ_BIU_WR9_GATE_Z. 20h: CLK_100MHZ_FREE_Z.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			21h: CLK_214MHZ_CHANNEL_I2S_SRC_Z. 22h: CLK_214MHZ_CHANNEL_SPDIF_SRC_Z. 23h: CLK_214MHZ_HDMI_SYNTH_Z. 24h: CLK_64FS_HDMI_DSD_Z. 25h: CLK_128FS_HDMI_TRUE_Z. 26h: CLK_128FS_SPDIF_DECODER_TRUE_Z. 27h: CLK_256FS_PCM_DELAY_Z. 28h: CLK_FM_DEMODULATOR_Z. 29h: CLK_BCLK_I2S_OUT2_ENCODER_Z. 2Ah: CLK_MCLK_I2S_OUT2_ENCODER_Z. 2Bh: CLK_214MHZ_CHANNEL_I2S_OUT2_SRC_Z. 2Ch: CLK_214MHZ_DVB_FIX_SYNTH_Z. 2Dh: CLK_214MHZ_DVB_SYNC_SYNTH_Z. 2Eh: CLK_256FS_DVB_SYNC_SYNTH_TRUE_Z. 2Fh: CLK_256FS_DVB_TIMING_GEN_Z. 30h: CLK_256FS_SIF_TIMING_GEN_Z. 31h: CLK_256FS_CHANNEL_2_OUT_DAC_X1_Z. 32h: CLK_128FS_SPDIF_NON_PCM_TRUE_Z. 33h: CLK_270MHZ_DVB_REF_Z. 34h: CLK_14318KHZ_FREE_Z. 35h: CLK_214MHZ_768FS_PLL_SYNTH_Z. 36h: CLK_768FS_SYNTH_FEED_BACK_256_FS_DIV6_Z. 37h: CLK_768FS_PLL_REF_128_Z. 38h: CLK_128FS_CTS_N_SYNTH_FEED_BACK_Z. 39h: CLK_214MHZ_CARD_READER_FIX_SYNTH_Z. 3Ah: N.A. 3Bh: N.A. 3Ch: N.A. 3Dh: N.A. 3Eh: N.A. 3Fh: N.A.	
58h (2CB1h)	**REG2CB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLK_CFG6[15:8]	7:0	See description of '2CB0h'.	
59h (2CB2h)	**REG2CB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTH_EXPANDER[7:0]	7:0	[7] Lock current frequency of I2S synthesizer. 0: Normal. 1: Lock current frequency. [6] CARD_READER 256 fs synthesizer clock pulse expander. 0: Normal (1T width).	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Expander (2T width). [5] DVB_FIX 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width). [4] DVB_SYNC 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width). [3] Bandwidth of I2S synthesizer. 0: Low bandwidth. 1: High bandwidth. [2] S/PDIF 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width). [1] CODEC 256 fs synthesizer clock pulse expander. 0: Normal (1T width). 1: Expander (2T width). [0] Bandwidth of SIF 32k synthesizer. 0: Low bandwidth. 1: High bandwidth.	
5Ah (2CB4h)	**REG2CB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTH_768_CONFIG_0[7:0]	7:0	Synthesizer 768 fs PDF frequency setting. X=M=N.	
5Ah (2CB5h)	**REG2CB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTH_768_CONFIG_0[15:8]	7:0	See description of '2CB4h'.	
5Bh (2CB6h)	**REG2CB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SYNTH_768_CONFIG_1[7:0]	7:0	[7:3] Reserved. [2] Lock current frequency of SYNTH_768 synthesizer. 0: Normal. 1: Lock current frequency. [1] Audio SYNTH_768 synthesizer Cs gain selection. 0: Normal. 1: Enhanced (smaller Cs). [0] Audio SYNTH_768 synthesizer Cp gain selection. 0: Normal. 1: Enhanced (smaller Cp).	
5Ch (2CB8h)	**REG2CB8**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_SYNTH_768_FRE	7:0	[15] Audio SYNTH_768 input signal detect.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	Q[7:0]		0: Signal detected. 1: No signal input. [14:0] Audio SYNTH_768 frequency value.	
5Ch (2CB9h)	**REG2CB9**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_SYNTH_768_FREQ[15:8]	7:0	See description of '2CB8h'.	
5Fh (2CBEh)	**REG2CBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	TMXCTRL[7:0]	7:0	Internal debug port selection (only for VLSI designer). Refer to TEST MUX detailed description.	
60h (2CC0h)	**REG2CC0**	**7:0**	**Default : 0x0C**	**Access : R/W**
	ASIF_CONFIG0[7:0]	7:0	[15:14] Audio SIF ADC bias generator reference current selection. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA. [13] Audio SIF ADC band-gap chopping control (ADC clock /8). 0: Disable. 1: Enable. [12] Audio SIF ADC GMC filter control. 0: Enable. 1: Power-down. [11] Audio SIF ADC GMC filter bias control. 0: Enable. 1: Power-down. [10] AAF_X2. [9] Audio SIF ADC mode control. 0: Test mode. 1: Audio SIF mode (mid clamp). [8:4] Reserved. [3] Audio SIF ADC control. 0: Normal. 1: Power-down. [2] Audio SIF I-clamp control. 0: Normal. 1: Power-down. [1] Audio SIF ADC 8-bit voltage dither mode (test mode). 0: Disable.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			1: Enable. Note: LSB 3-bit dither summation (1 1/2 1/4). [0] Gain calibration reference voltage source select. 0: 0.1V. 1: 0.6V (only for VLSI designer).
60h (2CC1h)	**REG2CC1**	**7:0**	**Default : 0x1A** **Access : R/W**
	ASIF_CONFIG0[15:8]	7:0	See description of '2CC0h'.
61h (2CC2h)	**REG2CC2**	**7:0**	**Default : 0x43** **Access : R/W**
	ASIF_CONFIG1[7:0]	7:0	[15:12] AAF_TSTVCMO[3:0]. [11:8] Audio SIF ADC GMC filter gain control. 000: 1. 001: 2. 010: 4. 011: 8. 100: 16. 101: 4. 110: 6. 111: 12. Others: Reserved. [7:4] Audio SIF ADC voltage clamp Vref selection. 0000: 1.15 V. 0001: 1.20 V. 0010: 0.85 V. 0011: 0.90 V. 0100: 0.95 V. 0101: 1.00 V. 0110: 1.05 V. 0111: 1.10 V. 1000: 0.30 V. 1001: 0.40 V. 1010: 0.50 V. 1011: 0.60 V. 1100: 0.70 V. 1101: 0.80 V. 1110: N.A. 1111: N.A. [3:2] Audio SIF ADC I-Clamp bias current control (I: 2.5uA). 00: 1* I. 01: 2* I.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: 3* I. 11: 4* I. [1] Audio SIF ADC Vref generator DAC bias current control. 0: Normal. 1: Power-down. [0] Audio SIF ADC Vref generator DAC resister stream control. 0: Normal. 1: Power-down.	
61h (2CC3h)	**REG2CC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIF_CONFIG1[15:8]	7:0	See description of '2CC2h'.	
62h (2CC4h)	**REG2CC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIF_CONFIG2[7:0]	7:0	[15] Audio SIF ADC GMC filter gain control driver. 0: DSP core control GMC filter gain (coarse gain). 1: MCU overwrite GMC filter gain. [14:13] Reserved. [12] Audio SIF ADC fine gain control driver. 0: Select DSP control ADC fine gain value. 1: Select MUC to overwrite ADC fine gain value. [11] Audio SIF ADC gain shift control. 0: 12/13 to 28/13. 1: 6/13 to 22/13. [10] Select ADC clock source. [9:8] Reserved. [7] Audio SIF ADC GMC filter auto tuning control. 0: GMC filter auto tuning from AAF_CTL[7:0]. 1: GMC filter auto tuning from Audio SIF DSP230. [6] Reserved. [5:4] SIF ADC resolution selection. 00: 10 bits. 01: 8 bits. 10: 6 bits. 11: 6 bits. [3] Audio SIF ADC GMC Vref buffer control. 0: Normal. 1: Disable GMC Vref buffer. [2:0] Audio SIF ADC GMC filter common mode Vref setting. 000: 1.15625 V. 001: 1.18750 V. 010: 1.21875 V.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			011: 1.25000 V. 100: 1.25000 V. 101: 1.09375 V. 110: 1.06250 V. 111: 1.03125 V.	
62h (2CC5h)	**REG2CC5**	**7:0**	**Default : 0x10**	**Access : R/W**
	ASIF_CONFIG2[15:8]	7:0	See description of '2CC4h'.	
63h (2CC6h)	**REG2CC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIF_CONFIG3[7:0]	7:0	[15:8] Audio SIF ADC gain control value. 00: 12/13 (min). 01: 12/13 + (16/13 * 1/256). 02: 12/13 + (16/13 * 2/256). &. FF: 12/13 + (16/13 * 255/256) (max). [7:0] GMC filter fine tune value to define PGA cut-off frequency. Bit 7:. Bit 6: 19.20260 x 2 f-F (addition). Bit 5: 20.25815 x 2 f-F (addition). Bit 4: 42.59300 x 1 f-F (addition). Bit 3: 22.6600 x 1 f-F (addition). Bit 2: 12.41510 x 1 f-F (addition). Bit 1: 7.24688 x 1 f-F (addition). Bit 0: 4.28975 x 1 f-F (addition).	
63h (2CC7h)	**REG2CC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIF_CONFIG3[15:8]	7:0	See description of '2CC6h'.	
64h (2CC8h)	**REG2CC8**	**7:0**	**Default : 0x10**	**Access : R/W**
	ASIF_CONFIG4[7:0]	7:0	[15] Audio SIF ADC GMC filter DC test mode control. 0: Normal. 1: Enable DC Test Mode. [14] Audio SIF ADC GMC filter bias test mode control. 0: Normal. 1: Enable self bias setting for test mode. [13] Audio SIF ADC GMC filter 3rd order test mode control. 0: Normal Mode (3rd). 1: Enable Half-bypass Mode (3rdè1st). [12] Audio SIF ADC GMC filter output stage source following test mode control.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			0: Normal. 1: Disable Output Source Follower (test mode). [11] Audio SIF ADC GMC filter comparator test mode control. 0: Normal. 1: Disable comparator (test mode). [10] Audio SIF ADC GMC filter Gm-cell internal control. 0: Normal. 1: Disable (test mode). [9:8] Audio SIF ADC GMC filter Gm I-bias control. 00: 50 uA. 01: 62.5 uA. 10: 37.5 uA. 11: 50 uA. [7:0] Audio SIF ADC offset control value. 00: 5/13 * 0.5 V (min). 01: (5/13 + (16/13 * 1/256)) * 0.5 V. 02: (5/13 + (16/13 * 2/256)) * 0.5 V. .. FF: (5/13 + (16/13 * 255/256)) * 0.5 V (max).
64h (2CC9h)	**REG2CC9**	**7:0**	**Default : 0x00** **Access : R/W**
	ASIF_CONFIG4[15:8]	7:0	See description of 2CC8h.
65h (2CCAh)	**REG2CCA**	**7:0**	**Default : 0x55** **Access : R/W**
	ASIF_ICTRL[7:0]	7:0	[15:14] Reserved. [13:10] SIF ADC bias control. [9:8] Audio SIF ADC VRP/G/M OP amp bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA. [7:6] Audio SIF ADC PGA front-end buffer bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA. [5:4] Audio SIF ADC PGA bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA.

AUDIO0 Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			11: 80 uA. [3:2] Audio SIF ADC Stage-1 OP amp & comparator bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA. [1:0] Audio SIF ADC Stage-2 OP amp & comparator bias current control. 00: 20 uA (normal). 01: 40 uA. 10: 60 uA. 11: 80 uA.
65h (2CCBh)	**REG2CCB**	**7:0**	**Default : 0x15** **Access : R/W**
	-	7:6	Reserved.
	ASIF_ICTRL[13:8]	5:0	See description of '2CCAh'.
66h (2CCCh)	**REG2CCC**	**7:0**	**Default : 0x00** **Access : R/W**
	ASIF_AMUX[7:0]	7:0	[15:13] Reserved. [12] Select SIF Clock x2. 0: MPLL /2. 1: MPLL /4. [11] To VIF_ENABLE_AU. [10] To VIF_CKSEL. [9] For VIF/SIF clock & data switch. 0: SIF mode. 1: VIF mode. [8] SIF I/Q selection by down-converter enable option. 0: I/Q select by down-converter enable only once. 1: I/Q select by DATA_LATEN in SIF FIFO out dynamically. [7] SIF ADC FIFO enable control source selection. 0: FIFO enable controlled by MCU. 1: FIFO enable controlled by DSP. [6] ASIF_FIFO_MODE. 0: Select 2-stage FIFO. 1: Select 4-stage FIFO. [5] ASIF_FIFO_ENABLE. 0: Disable FIFO operation. 1: Set to start FIFO operation for synchronization. [4] Audio SIF input selection.

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			0: SIF[0] is the input of ADC. 1: SIF[1] is the input of ADC. [3:2] Audio SIF ADC V-clamp selection of IN-M. 00: V-clamp to VP0 (while CR64[6]=1). 01: V-clamp to middle pull resister. 10: V-clamp to weak pull resister. 11: V-clamp to VP1 (while CR64[6]=1). [1:0] Audio SIF ADC V-clamp selection of IN-P. In each case, I-clamp can be enabled. However, I-clamp can only function normally when there is no V-clamp. 00: No V-clamp. 01: V-clamp to middle pull resister. 10: V-clamp to weak pull resister. 11: No V-clamp.
66h (2CCDh)	**REG2CCD**	**7:0**	**Default : 0x0C** **Access : R/W**
	ASIF_AMUX[15:8]	7:0	See description of '2CCCh'.
67h (2CCEh)	**REG2CCE**	**7:0**	**Default : 0x00** **Access : R/W**
	ASIF_TST[7:0]	7:0	[15:14] Reserved. [13] I-clamp path to SIF input. 0: Normal (I-clamp to input, write CR54[2] for choice). 1: Disable I-clamp. [12] Audio SIF GMC filter bypass enable. 0: Normal (use GMC). 1: Bypass (no GMC, direct to ADC). [11] Disable input selection. 0: Normal (choose one input to GMC or ADC, write CR54[2] for choice). 1: No input goes to GMC or ADC. [10] ASIF_TST[10:9]. 00: Normal. 01: Select PGA output to ATEST_1 & ATEST_2. 10: Increase ADC clock no-overlap interval. 11: Increase ADC clock no-overlap interval. [8:7] ASIF_TST[8:7]. 00: Normal. 01: Select VRP (ADC Vref top) output to ATEST_1. 10: Select VRG (ADC Vref common) output to ATEST_1. 11: Select VRM (ADC Vref bottom) output to ATEST_1.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[6:5] Audio SIF ADC internal I-ref source selection. 00: From bandgap (normal). 01: Select bandgap I output to ATEST_1. 10: From ATEST_1 pad. 11: Select bandgap I output to ATEST_1 & from ATEST_1 pad. [4:3] Audio SIF ADC internal V-ref source selection. 00: From bandgap (normal). 01: Select bandgap V output to ATEST_2. 10: From ATEST_2 pad. 11: Select bandgap V output to ATEST_2 & from ATEST_2 pad. [2:0] Audio SIF ADC I-bias adjustment. 000: 62.5 uA. 001: 75.0 uA. 010: 87.5 uA. 011: 100 uA. 100: 12.5 uA. 101: 25.0 uA. 110: 37.5 uA. 111: 50.0 uA.	
67h (2CCFh)	**REG2CCF**	**7:0**	**Default : 0x30**	**Access : R/W**
	ASIF_TST[15:8]	7:0	See description of '2CCEh'.	
68h (2CD0h)	**REG2CD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIF_ADCREF[7:0]	7:0	[15:13] ADC_VCTRL ADC common mode bias control. [12] Reserved. [11:0] Audio SIF ADC Vref range control (center voltage = 1.5V). [11:8] ASIF_ADCREF. 000h: 0.25V. 001h: 0.25 + 1/4096. 002h: 0.25 + 2/4096. .. FFFh: 0.25 + 4095/4096.	
68h (2CD1h)	**REG2CD1**	**7:0**	**Default : 0x6C**	**Access : R/W**
	ASIF_ADCREF[15:8]	7:0	See description of '2CD0h'.	
6Ch (2CD8h)	**REG2CD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIFPLL_EXT[7:0]	7:0	[15:4] Reserved.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[3] SIF CH1 and CH2 use the same enable signal. 0: Use respective enable signals. 1: Both use CH1 enable signal. [2:0] Reserved.	
6Ch (2CD9h)	**REG2CD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIFPLL_EXT[15:8]	7:0	See description of '2CD8h'.	
6Eh (2CDCh)	**REG2CDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIF_TST_EXT[7:0]	7:0	[15:4] Reserved.	
6Eh (2CDDh)	**REG2CDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	ASIF_TST_EXT[15:8]	7:0	See description of '2CDCh'.	
6Fh (2CDEh)	**REG2CDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIF_CONFIG0[7:0]	7:0	[15:4] Reserved.	
6Fh (2CDFh)	**REG2CDF**	**7:0**	**Default : 0x4C**	**Access : R/W**
	VIF_CONFIG0[15:8]	7:0	See description of '2CDEh'.	
70h (2CE0h)	**REG2CE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG0[7:0]	7:0	[15:14] Line-Out (AA) OPamp Bias Current. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA. [13:12] ADC Input Mixer (anti aliasing filter) OPamp Bias Current. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA. [11:10] ADC Integrator OPamp Bias Current. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA. [9:8] Audio DAC OPamp Bias Current. 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA. [7:6] Audio Reference Voltage Generator OPamp Bias Control. 00: 20uA.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			01: 15uA. 10: 30uA. 11: 25uA. [5:4] Reserved Current Control (for future use). 00: 20uA. 01: 15uA. 10: 30uA. 11: 25uA. [3:2] Audio ADC Output Duty Cycle Test. 00: Select AVSS. 01: Select AVSS. 10: Select Left Channel ADC Output. 11: Select Right Channel ADC Output. [1] Reserved. [0] Reset FF #16 in DAC. 0: Normal function. 1: Reset.	
70h (2CE1h)	**REG2CE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG0[15:8]	7:0	See description of '2CE0h'.	
71h (2CE2h)	**REG2CE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG1[7:0]	7:0	[15] Audio ADC Left Channel Dithering. 0: Disable. 1: Enable. [14] Audio ADC Integrator of Left Channel Reset. 0: Normal. 1: Reset active. [13] Audio ADC Left Dithering Amount Reduce. 0: Normal. 1: Reduced (50%). [12] Audio ADC Right Channel Dithering. 0: Disable. 1: Enable. [11] Audio ADC Integrator of Right Channel Reset. 0: Normal. 1: Reset active. [10] Audio ADC Right Dithering Amount Reduce. 0: Normal. 1: Reduced (50%). [9:6] Reserved.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			[5] Power Down Reference Current Generator. 0: Power on. 1: Power down (OR gated with DSP). [4] Power Down Reference Voltage Generator. 0: Power on. 1: Power down (OR gated with DSP). [3] Power Down All Bias Current Sources. 0: Power on. 1: Power down (OR gated with DSP). [2] Enable self-bias current. 0: Disable. 1: Enable. [1] Reserved. [0] AUSDM Vref Soft-Discharge Enable. 0: Disable soft-discharge. 1: Enable soft-discharge.
71h (2CE3h)	**REG2CE3**	**7:0**	**Default : 0x00** **Access : R/W**
	CODEC_CFG1[15:8]	7:0	See description of '2CE2h'.
72h (2CE4h)	**REG2CE4**	**7:0**	**Default : 0x00** **Access : R/W**
	CODEC_CFG2[7:0]	7:0	[15] Power Down Right Channel ADC. 0: Normal. 1: Power down. [14] Power Down Left Channel ADC. 0: Normal. 1: Power down. [13] Power Down Audio ADC Input Clock. 0: Normal. 1: Power down. [12] Select Audio ADC Input Clock Source. 0: From clock generator. 1: From external pad (video VSYNC_0). [11:9] SDMADC Clock Delay (unit: inverter buffer 70ps). 000: Delay 0 time unit. 001: Delay 4 time units. 010: Delay 8 time units. 011: Delay 12 time units. 100: Delay 16 time units. 101: Delay 20 time units. 110: Delay 24 time units.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			111: Delay 28 time units. [8] Reserved. [7:6] Audio SDMADC Left Channel Internal Feedback Coefficient. 00: 0.300 pF. 01: 0.225 pF. 10: 0.270 pF. 11: 0.345 pF. [5:4] Audio SDMADC Right Channel Internal Feedback Coefficient. 00: 0.300 pF. 01: 0.225 pF. 10: 0.270 pF. 11: 0.345 pF. [3:0] Reserved.	
72h (2CE5h)	**REG2CE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG2[15:8]	7:0	See description of '2CE4h'.	
73h (2CE6h)	**REG2CE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG3[7:0]	7:0	[15] DE_POP Line-Out[0] Amplifier Control (feedback R = 0). 0: Normal. 1: Mute. [14:11] Audio Line-Out[0] (AA_0) Input Source Selection. 0000: Line-in [0]. 0001: Line-in [1]. 0010: Line-in [2]. 0011: Line-in [3]. 0100: AVSS. 0101: AVSS. 0110: DACL1 & DACR1 out. 0111: DACL0 & DACR0 out. 1000: DACL2 & DACR2 out. 1001: AVSS. 1010: Line-in [4]. 1011: Line-in [5]. 1100: AVSS. Others: N.A. [10:9] Audio Line-Out[0] (AA_0) Gain Control. 00: 0 dB. 01: -3 dB.	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: -6 dB. 11: +3 dB. [8] Audio ADC Input Mixer (Anti Alias Filter) OPamp Control. 0: Normal Anti Alias Filter OPamp. 1: Mute Anti Alias Filter OPamp (feedback R = 0). [7] Power Down Audio ADC Input Mixer (Anti Alias Filter) OPamp. 0: Normal. 1: Power Down. [6:3] Audio ADC Input Mixer Source Selection. 0000: Line-in[0]. 0001: Line-in[1]. 0010: Line-in[2]. 0011: Line-in[3]. 0100: AVSS. 0101: AVSS. 0110: DAL1 & DAR1. 0111: DAL0 & DAR0. 1000: DAL2 & DAR2. 1001: AVSS. 1010: Line-in[4]. 1011: Line-in[5]. 1100: Line-Out[0] left & right (AA0). 1101: Line-Out[1] left & right (AA1). Others: N.A. [2:0] Audio ADC Input Mixer (Anti Alias Filter) Gain Control. 000: 0 dB. 001: -3 dB. 010: -6 dB. 011: +3 dB. 100: +6 dB. 101: +9 dB. 110: +12 dB.	
73h (2CE7h)	**REG2CE7**	**7:0**	**Default : 0x28**	**Access : R/W**
	CODEC_CFG3[15:8]	7:0	See description of '2CE6h'.	
74h (2CE8h)	**REG2CE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG4[7:0]	7:0	[15] DE_POP Line-Out[1] (AA_1) Amplifier Control (feedback R = 0). 0: Normal.	

AUDIO0 Register (Bank = 2C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			1: Mute. [14:11] Audio Line-Out[1] (AA_1) Input Source Selection. 0000: Line-in [0]. 0001: Line-in [1]. 0010: Line-in [2]. 0011: Line-in [3]. 0100: AVSS. 0101: AVSS. 0110: DACL1 & DACR1 out. 0111: DACL0 & DACR0 out. 1000: DACL2 & DACR2 out. 1001: AVSS. 1010: Line-in[4]. 1011: Line-in[5]. 1100: Line-Out[0] left & right (AA0). 1101: Line-Out[1] left & right (AA1). Others: N.A. [10:9] Audio Line-Out[1] (AA_1) Gain Control. 00: 0 dB. 01: -3 dB. 10: -6 dB. 11: +3 dB. [8] Reserved. [7] Audio Line-Out[0] (AA_0) Right Channel Amplifier Driving Strength. 0: Normal. 1: Reduce to 1%. [6] Audio Line-Out[0] (AA_0) Left Channel Amplifier Driving Strength. 0: Normal. 1: Reduce to 1%. [5] Audio Line-Out[0] (AA_0) Right Channel Amplifier Low Power Mode. 0: Normal. 1: Low Power Mode (50% Bias Current). [4] Audio Line-Out[0] (AA_0) Left Channel Amplifier Low Power Mode. 0: Normal. 1: Low Power Mode (50% Bias Current). [3] Reserved.

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[2] Disable DAC[2] Re-latch Clock. 0: Normal. 1: Clock disabled. [1] Disable DAC[0] Re-latch Clock. 0: Normal. 1: Clock disabled. [0] Disable DAC[1] Re-latch Clock. 0: Normal. 1: Clock disabled.	
74h (2CE9h)	**REG2CE9**	**7:0**	**Default : 0x28**	**Access : R/W**
	CODEC_CFG4[15:8]	7:0	See description of '2CE8h'.	
75h (2CEAh)	**REG2CEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG5[7:0]	7:0	[15] Audio DAC Right Channel[1] Low Power Mode. 0: Normal. 1: Low power mode (50%). [14] Audio DAC Right Channel[1] Amplifier Driving Strength. 0: Normal. 1: Reduce to 1%. [13] Audio DAC Left Channel[1] Low Power Mode. 0: Normal. 1: Low power mode (50%). [12] Audio DAC Left Channel[1] Amplifier Driving Strength. 0: Normal. 1: Reduce to 1%. [11] Reserved. [10] Reset DAC[2] Re-latch Flip-flip. 0: Normal. 1: Reset (OR gated with DSP). [9] Reset DAC[0] Re-latch Flip-flip. 0: Normal. 1: Reset (OR gated with DSP). [8] Reset DAC[1] Re-latch Flip-flip. 0: Normal. 1: Reset (OR gated with DSP). [7] Audio Line-Out[1] (AA_1) Right Channel Amplifier Driving Strength. 0: Normal. 1: Reduce to 1%. [6] Audio Line-Out[1] (AA_1) Left Channel Amplifier Driving	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Strength. 0: Normal. 1: Reduce to 1%. [5] Audio Line-Out[1] (AA_1) Right Channel Amplifier Low Power Mode. 0: Normal. 1: Low Power Mode (50% Bias Current). [4] Audio Line-Out[1] (AA_1) Left Channel Amplifier Low Power Mode. 0: Normal. 1: Low Power Mode (50% Bias Current). [3] Mute Audio Line-Out[1] (AA_1) (Input Floating). 0: Normal. 1: Mute. [2] Mute Audio Line-Out[0] (Input Floating). 0: Normal. 1: Mute. [1] Power Down Audio Line-Out[1] (AA_1). 0: Power on. 1: Power down (OR gated with DSP). [0] Power down Audio Line-Out[0] (AA_0). 0: Power on. 1: Power down (OR gated with DSP).	
75h (2CEBh)	**REG2CEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG5[15:8]	7:0	See description of '2CEAh'.	
76h (2CECh)	**REG2CEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG6[7:0]	7:0	[15] Audio DAC Right Channel[0] Low Power Mode. 0: Normal. 1: Low power mode (50%). [14] Audio DAC Right Channel[0] Amplifier Driving Strength. 0: Normal. 1: Reduce to 1%. [13] Power Down Audio DAC Right Channel[1] L Driving OPamp. 0: Power on. 1: Power down (OR gated with DSP). [12] Power Down Audio DAC Right Channel[1] L Vref OPamp. 0: Power on. 1: Power down (OR gated with DSP).	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[11] Audio DAC Left Channel[0] Low Power Mode. 0: Normal. 1: Low power mode (50%). [10] Audio DAC Left Channel[0] Amplifier Driving Strength. 0: Normal. 1: Reduce to 1%. [9] Power Down Audio DAC Channel[0] Driving OPamp. 0: Power on. 1: Power down (OR gated with DSP). [8] Power Down Audio DAC Channel[0] Vref OPamp. 0: Power on. 1: Power down (OR gated with DSP). [7:6] Reserved. [5] Power Down Audio DAC Channel[1] R Driving OPamp. 0: Power on. 1: Power down (OR gated with DSP). [4] Power Down Audio DAC Channel[1] R Vref OPamp. 0: Power on. 1: Power down (OR gated with DSP). [3] Audio DAC Data Latching Mode Select. 0: Negative edge select. 1: Positive edge select. [2] Power Down Audio DAC Reference Current Generator. 0: Power on. 1: Power down (OR gated with DSP). [1] Audio DAC Reference Current Test Mode. 0: Normal. 1: Bypass test current to pad (SOG_[1:0] = Test [1:0]). [0] Reserved.	
76h (2CEDh)	**REG2CED**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG6[15:8]	7:0	See description of '2CECh'.	
77h (2CEEh)	**REG2CEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG7[7:0]	7:0	[15:10] Reserved. [9] DAC Discharge Control. 0: Disable. 1: Enable (OR gated with DSP). [8] VREF Discharge Control. 0: Disable. 1: Enable (OR gated with DSP).	

AUDIO0 Register (Bank = 2C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[7:0] Reserved.	
77h (2CEFh)	**REG2CEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	CODEC_CFG7[15:8]	7:0	See description of '2CEEh'.	
7Bh (2CF6h)	**REG2CF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CTRL1[7:0]	7:0	[15:0] Reserved.	
7Bh (2CF7h)	**REG2CF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CTRL1[15:8]	7:0	See description of '2CF6h'.	
7Ch (2CF8h)	**REG2CF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CTRL2[7:0]	7:0	[15:0] Reserved.	
7Ch (2CF9h)	**REG2CF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CTRL2[15:8]	7:0	See description of '2CF8h'.	
7Dh (2CFAh)	**REG2CFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CTRL3[7:0]	7:0	[15:0] Reserved.	
7Dh (2CFBh)	**REG2CFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CTRL3[15:8]	7:0	See description of '2CFAh'.	
7Eh (2CFCh)	**REG2CFC**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_BUS_OUT_L[7:0]	7:0	Test bus output LSB.	
7Eh (2CFDh)	**REG2CFD**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_BUS_OUT_L[15:8]	7:0	See description of '2CFCh'.	
7Fh (2CFEh)	**REG2CFE**	**7:0**	**Default : 0x00**	**Access : RO**
	TEST_BUS_OUT_H[7:0]	7:0	Test bus output MSB.	

AUDIO1 Register (Bank = 2D)

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2D00h)	**REG2D00**	**7:0**	**Default : 0x03**	**Access : RO, R/W**
	-	7	Reserved.	
	DSP16K_BANK_SEL	6	DSP16K Bank Select. 0: IDMA access memory 0~16K. 1: IDMA access memory > 16K.	
	INT_TRIGGER	5	MIPS-triggered DSP PIO[8] interrupt. 0: De-assert DSP PIO[8] interrupt. 1: Assert DSP PIO[8] interrupt.	
	IDMA_WR_CMD_STA	4	IDMA write command status. 0: IDMA write command finish. 1: IDMA write ongoing (busy).	
	IDMA_RD_CMD_STA	3	IDMA Read Command / Status. Command: 0: N.A. 1: Set IDMA read command, auto-clear when finished. Status: 0: Read command finished. 1: Read command busy.	
	IDMA_WR2ND	2	IDMA needs to write 2nd Data Set. 0: IDMA write data finished. 1: IDMA needs to write 2nd data set. Note: Write 0 to clear.	
	IDMA_BOOT_MODE	1	DSP IDMA Boot Mode Enable. 0: Disable. 1: Enable.	
	DSP_SOFT_RST	0	DSP Audio Software Reset. 0: Reset. 1: Normal.	
01h (2D02h)	**REG2D02**	**7:0**	**Default : 0x00**	**Access : WO**
	DSP_BRG_DATA[7:0]	7:0	Host Download DSP Data Port. 24-bit mode: 1: Write high 2 bytes {DATA[23:8]}. 2: Write low byte {8'b0, DATA[7:0]}. 3: Loop to step 1.	
01h (2D03h)	**REG2D03**	**7:0**	**Default : 0x00**	**Access : WO**
	DSP_BRG_DATA[15:8]	7:0	See description of '2D02h'.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
02h (2D04h)	**REG2D04**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDMA_WRBASE_ADDR[7:0]	7:0	Channel 1 IDMA address base IAD.	
02h (2D05h)	**REG2D05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CH1_MEM_SEL	6	Channel 1 IDMA address base PM/CM/DM control. 0: Select PM/CM. 1: Select DM.	
	IDMA_WRBASE_ADDR[13:8]	5:0	See description of '2D04h'.	
03h (2D06h)	**REG2D06**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1IDMA_ATR_SIZE[7:0]	7:0	IDMAtrSize.	
03h (2D07h)	**REG2D07**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	CH1IDMA_CIRCULAR_BUF	6	Disable IDMA CH2 circular buffer. 0: Enable circular buffer. 1: Disable circular buffer.	
	CH1IDMA_ATR_SIZE[13:8]	5:0	See description of '2D06h'.	
04h (2D08h)	**REG2D08**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDMA_RDBASE_ADDR[7:0]	7:0	Channel 2 IDMA address base IAD.	
04h (2D09h)	**REG2D09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CH2_MEM_SEL	6	Channel 2 IDMA address base PM/CM/DM control. 0: Select PM/CM. 1: Select DM.	
	IDMA_RDBASE_ADDR[13:8]	5:0	See description of '2D08h'.	
05h (2D0Ah)	**REG2D0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH2IDMA_ATR_SIZEH[7:0]	7:0	IDMAtrSize.	
05h (2D0Bh)	**REG2D0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CH2IDMA_ATR_SIZEH_DIS	6	Disable IDMA CH2 circular buffer. 0: Enable circular buffer. 1: Disable circular buffer.	
	CH2IDMA_ATR_SIZEH[13:8]	5:0	See description of '2D0Ah'.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
06h (2D0Ch)	**REG2D0C**	**7:0**	**Default : 0x00**	**Access : RO**
	IDMA_RDDATA_H[7:0]	7:0	IDMA CH2 MIPS Read DSP Data Port [23:8], for transferring data from DSP to MIPS.	
06h (2D0Dh)	**REG2D0D**	**7:0**	**Default : 0x00**	**Access : RO**
	IDMA_RDDATA_H[15:8]	7:0	See description of '2D0Ch'.	
07h (2D0Eh)	**REG2D0E**	**7:0**	**Default : 0x00**	**Access : RO**
	IDMA_RDDATA_L[7:0]	7:0	IDMA CH2 MIPS Read DSP Data Port [7:0], for transferring data from DSP to MIPS.	
08h (2D10h)	**REG2D10**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSP_ICACHE_BASE[7:0]	7:0	[15:8] FD230 I-Cache MIU base address [23:16]. [7:0] ICU base address = {DSP_ICH_BASE[15:0], 8'b0} + ICU_MIU_ADDR[15:0].	
08h (2D11h)	**REG2D11**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSP_ICACHE_BASE[15:8]	7:0	See description of '2D10h'.	
09h (2D12h)	**REG2D12**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU2DSP_MAILBOX_CFG[3:0]	7:4	MCU to DSP mailbox configuration. 0000: M2D_MAILBOX_0 (0x7000). 0001: M2D_MAILBOX_1 (0x7001). 0010: M2D_MAILBOX_2 (0x7002). 0011: M2D_MAILBOX_3 (0x7003). 0100: M2D_MAILBOX_4 (0x7004). 0101: M2D_MAILBOX_5 (0x7005). 0110: M2D_MAILBOX_6 (0x7006). 0111: M2D_MAILBOX_7 (0x7007). 1000: M2D_MAILBOX_8 (0x7008). 1001: M2D_MAILBOX_9 (0x7009).	
	DSP2MCU_MAILBOX_CFG[3:0]	3:0	DSP to MCU mailbox configuration. 0000: D2M_MAILBOX_0. 0001: D2M_MAILBOX_1. 0010: D2M_MAILBOX_2. 0011: D2M_MAILBOX_3. 0100: D2M_MAILBOX_4. 0101: D2M_MAILBOX_5. 0110: D2M_MAILBOX_6. 0111: D2M_MAILBOX_7.	
0Ah (2D14h)	**REG2D14**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU2DSP_MAILBOX[7:0]	7:0	MCU to DSP Mailbox.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
			Indirect Mailbox Write to DSP Port.	
0Ah (2D15h)	**REG2D15**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU2DSP_MAILBOX[15:8]	7:0	See description of '2D14h'.	
0Bh (2D16h)	**REG2D16**	**7:0**	**Default : 0x00**	**Access : RO**
	DSP2MCU_MAILBOX[7:0]	7:0	DSP to MCU Mailbox. Indirect Mailbox Read from DSP Port.	
0Bh (2D17h)	**REG2D17**	**7:0**	**Default : 0x00**	**Access : RO**
	DSP2MCU_MAILBOX[15:8]	7:0	See description of '2D16h'.	
0Ch (2D18h)	**REG2D18**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RIU2DSP_INFO	0	UP interrupt DSP signal, software controlled H/L.	
10h (2D20h)	**REG2D20**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_SEL_SET	7	Audio SIF Standard Set Command. 0: Manual. 1: Auto.	
	STD_SEL[6:0]	6:0	SIF audio standard Selection. For PAL DSP code: [7:4]: Mode Selection. 0x10: FM mono hideviation mode.	
11h (2D22h)	**REG2D22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	STD_PRE45[1:0]	2:1	Preference in automatic standard Selection of 4.5MHz carrier. 00: Standard M (Korea). 01: Standard M (BTSC). 10: Standard M (Japan). 11: Not a sound carrier.	
	STD_PRE65	0	Preference in automatic standard Selection of 6.5MHz carrier. 0: Standard L (SECAM). 1: Standard D/K.	
12h (2D24h)	**REG2D24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIF_SOUND_MOD1[7:0]	7:0	SIF BTSC/A2 demodulator automatic/manual sound mode output select. 0xxxxxxx: Manual sound select. 0000-0000: BTSC Mono. 00000001: BTSC Stereo. 00000010: BTSC SAP.	

AUDIO1 Register (Bank = 2D)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			00000100: A2 Mono. 00000101: A2 Stereo. 00000110: A2 Dual B. 00000111: A2 Dual A+B. 1xxxxxxx: Auto sound select. 10000000: BTSC Mono <-> Mute. 10000001: BTSC Stereo <-> Mono <-> Mute. 10000010: BTSC SAP <-> Mono <-> Mute. 10000100: A2 Mono <-> Mute. 10000101: A2 Stereo <-> Mono <-> Mute. 10000110: A2 Dual B <-> Mono <-> Mute. 10000111: A2 Dual B <-> Stereo->Mono <-> Mute.
13h (2D26h)	**REG2D26**	**7:0**	**Default : 0x00** **Access : R/W**
	SIF_SOUND_MOD2[7:0]	7:0	SIF NICAM demodulator sound mode output select. 00000000: NICAM Auto Mode. NICAM Sound (Auto) FM/AM Mono Mute. 0x01: FM/AM Mono (OSD). 0x02: Stereo L/R FM/AM Mono (OSD). 0x03: Stereo L/L FM/AM Mono (OSD). 0x04: Stereo R/R FM/AM Mono (OSD). 0x05: Dual A/B FM/AM Mono. 0x06: Dual A/A FM/AM Mono. 0x07: Dual B/B FM/AM Mono. 0x08: NICAM Mono FM/AM Mono. 0x80: Force NICAM Sound.
14h (2D28h)	**REG2D28**	**7:0**	**Default : 0x00** **Access : R/W**
	AVC_CLIP[7:0]	7:0	Fine Tune AVC Clip Level.
15h (2D2Ah)	**REG2D2A**	**7:0**	**Default : 0x00** **Access : R/W**
	DBG_CMD[7:0]	7:0	SIF common command set: 0x00: No action. 0x01: Common command - get firmware version. 0x02: Common command - set memory data. 0x03: Common command - set DM memory address. 0x04: Common command - set PM memory address. 0x05: Common command - read DM memory address. BTSC command: 0x10: BTSC_CMD_UPDATE_PILOT_ON_THR. Pilot Off to On Threshold Update Command. 0x11: BTSC_CMD_UPDATE_PILOT_OFF_THR.

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Pilot On to Off Threshold Update Command. 0x12: BTSC_CMD_UPDATE_CARRIER_ON_THR. Carrier Off to On Threshold Update Command. 0x13: BTSC_CMD_UPDATE_CARRIER_OFF_THR. Carrier On to Off Threshold Update Command. 0x14: BTSC_CMD_UPDATE_SAP_ON_THR. SAP Off to On Threshold Update Command. 0x15: BTSC_CMD_UPDATE_SAP_OFF_THR. SAP On to Off Threshold Update Command. A2 Command: 0x20: A2_CMD_UPDATE_CARRIER_ON_THR. Carrier Off to On Threshold Update Command. 0x21: A2_CMD_UPDATE_CARRIER_OFF_THR. Carrier On to Off Threshold Update Command. 0x22: A2_CMD_UPDATE_MONO_ON_THR. Mono Off to On Threshold Update Command. 0x23: A2_CMD_UPDATE_MONO_OFF_THR. Mono On to Off Threshold Update Command. 0x24: A2_CMD_UPDATE_STEREO_DUAL_THR. Stereo / Dual Threshold Update Command. 0x30: A2_CMD_GET_CARRIER_1_AMP. Carrier 1 Amplitude Output Command. 0x31: A2_CMD_GET_CARRIER_1_VAR. 0x32: A2_CMD_GET_CARRIER_2_AMP. Carrier 2 Amplitude Output Command. 0x33: A2_CMD_GET_CARRIER_2_VAR. 0x34: A2_CMD_GET_MONO_AMP. Mono Amplitude Output Command. 0x35: A2_CMD_GET_STEREO_AMP. Stereo Amplitude Output Command. 0x36: A2_CMD_GET_DUAL_AMP. Dual Amplitude Output Command.	
16h (2D2Ch)	**REG2D2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_DATA_H[7:0]	7:0	Data-high, from 8051 to DSP, which needs to match cmd (0x85).	
17h (2D2Eh)	**REG2D2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBG_DATA_L[7:0]	7:0	Data-low, from 8051 to DSP, which needs to match cmd (0x85).	
18h	**REG2D30**	**7:0**	**Default : 0x00**	**Access : R/W**

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2D30h)	DEBUG_REG_0[7:0]	7:0	8 bytes for software utilization.	
19h (2D32h)	**REG2D32**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEBUG_REG_1[7:0]	7:0	8 bytes for software utilization.	
1Ah (2D34h)	**REG2D34**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEBUG_REG_2[7:0]	7:0	8 bytes for software utilization.	
1Bh (2D36h)	**REG2D36**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEBUG_REG_3[7:0]	7:0	8 bytes for software utilization.	
1Ch (2D38h)	**REG2D38**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEBUG_REG_4[7:0]	7:0	8 bytes for software utilization.	
1Dh (2D3Ah)	**REG2D3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEBUG_REG_5[7:0]	7:0	8 bytes for software utilization.	
1Eh (2D3Ch)	**REG2D3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEBUG_REG_6[7:0]	7:0	8 bytes for software utilization.	
1Fh (2D3Eh)	**REG2D3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEBUG_REG_7[7:0]	7:0	8 bytes for software utilization.	
20h (2D40h)	**REG2D40**	**7:0**	**Default : 0x00**	**Access : RO**
	STD_RESULT_FINISH	7	Audio SIF Standard Detection Flag. 0: Standard detection finished. 1: Standard detection not finished.	
	STD_RESULT[6:0]	6:0	SIF Standard Detect Result. 00h: Standard not found. 01h: AU_SYS_M_BTSC. 02h: AU_SYS_M_KOREA. 03h: AU_SYS_M_JAPAN. 04h: AU_SYS_BG_A2. 05h: AU_SYS_DK1_A2. 06h: AU_SYS_DK2_A2. 07h: AU_SYS_DK3_A2. 08h: AU_SYS_BG_NICAM. 09h: AU_SYS_DK_NICAM. 0ah: AU_SYS_I_NICAM. 0bh: AU_SYS_L_NICAM. 0ch: AU_SYS_FM_RADIO.	
22h (2D44h)	**REG2D44**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_MOD[7:0]	7:0	Sound Mode Status. [0]: BTSC Mono existing.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[1]: BTSC Stereo existing. [2]: BTSC Sap existing. [3]: A2 Carrier 1 existing. [4]: A2 Carrier 2 existing. [5]: A2 Stereo existing. [6]: A2 Dual existing. [7]: A2 Mono existing.	
25h (2D4Ah)	**REG2D4A**	**7:0**	**Default : 0x00**	**Access : RO**
	DBG_OUTPUT_L[7:0]	7:0	Debugging Data Port. Directly output data from DSP230 I/O Write Command.	
26h (2D4Ch)	**REG2D4C**	**7:0**	**Default : 0x00**	**Access : RO**
	DBG_OUTPUT_H[7:0]	7:0	Debugging Data Port. Directly output data from DSP230 I/O Write Command.	
27h (2D4Eh)	**REG2D4E**	**7:0**	**Default : 0x00**	**Access : RO**
	INC_COUNTER[7:0]	7:0	DSP Sample Counter. SIF PCM output sample counter.	
28h (2D50h)	**REG2D50**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIL_BOX_0[7:0]	7:0	DSP to MCU Mailbox Data.	
29h (2D52h)	**REG2D52**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIL_BOX_1[7:0]	7:0	DSP to MCU Mailbox Data.	
2Ah (2D54h)	**REG2D54**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIL_BOX_2[7:0]	7:0	DSP to MCU Mailbox Data.	
2Bh (2D56h)	**REG2D56**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIL_BOX_3[7:0]	7:0	DSP to MCU Mailbox Data.	
2Ch (2D58h)	**REG2D58**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIL_BOX_4[7:0]	7:0	DSP to MCU Mailbox Data.	
2Dh (2D5Ah)	**REG2D5A**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIL_BOX_5[7:0]	7:0	DSP to MCU Mailbox Data.	
2Eh (2D5Ch)	**REG2D5C**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIL_BOX_6[7:0]	7:0	DSP to MCU Mailbox Data.	
2Fh (2D5Eh)	**REG2D5E**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIL_BOX_7[7:0]	7:0	DSP to MCU Mailbox Data.	
30h (2D60h)	**REG2D60**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	DWA_RST	7	Reset DWA.	

AUDIO1 Register (Bank = 2D)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			0: Normal. 1: DWA outputs all ZERO to analog.
	INIT_DATA_SRAM	6	Initial Data SRAM (8051 software control). 0: Normal. 1: Initial time (> 512 * MAC_CLK).
	MAC_OVL	5	MAC is overloaded. 0: Normal. 1: Overloaded.
	MOD_ENABLE	4	Modulator input Test Mode setting. 1: Normal. 0: Input 16h8000 to Modulator.
	DAC_TEST	3	DAC Test Mode. 0: Normal. 1: Test Mode for mass production.
	-	2	Reserved.
	DAC_EN_BIU	1	CH1~4 clock enable. 0: Disable. 1: Enable.
	DSD_IRQ_MASK	0	DSD IRQ Mask.
31h (2D62h)	**REG2D62**	**7:0**	**Default : 0x00** **Access : R/W**
	DAC_CH4_MAC_IRQ_MASK	7	CH4 IRQ Mask. 0: IRQ valid. 1: Mask.
	DAC_CH3_MAC_IRQ_MASK	6	CH3 IRQ Mask. 0: IRQ valid. 1: Mask.
	DAC_CH2_MAC_IRQ_MASK	5	CH2 IRQ Mask. 0: IRQ valid. 1: Mask.
	DAC_CH1_MAC_IRQ_MASK	4	CH1 IRQ Mask. 0: IRQ valid. 1: Mask.
	DAC_CH4_FD230_BYPASS	3	CH4 FD230 Bypass Mode (Hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	DAC_CH3_FD230_BYPASS	2	CH3 FD230 Bypass Mode (Hardware). 0: Normal.

AUDIO1 Register (Bank = 2D)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			1: Mask FD230 IRQ & hardware bypass.
	DAC_CH2_FD230_BYPASS	1	CH2 FD230 Bypass Mode (Hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	DAC_CH1_FD230_BYPASS	0	CH1 FD230 Bypass Mode (Hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
32h (2D64h)	**REG2D64**	**7:0**	**Default : 0x00** **Access : R/W**
	ADC1_MAC_IRQ_MASK	7	ADC1 IRQ Mask. 0: IRQ valid. 1: Mask.
	ADC1_FD230_BYPASS	6	ADC1 FD230 Bypass Mode. 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	-	5:3	Reserved.
	SRC_OSZOH_TEST	2	SRC interpolation function control. 0: Normal (linear interpolation). 1: Sample and hold (disable interpolation).
	SRC_FS_TEST	1	SRC interpolation ratio Selection. 0: Normal SRC Interpolation Mode (8fs to 256fs). 1: SRC Interpolation Test Mode (fs to 256fs).
	ZRMAC_CLKON_ALWAYS	0	0: MAC clock auto power down mode. 1: Disable MAC clock auto power down mode.
33h (2D66h)	**REG2D66**	**7:0**	**Default : 0x00** **Access : R/W**
	DWA_SHIFT_DIS	7	Disable DWA's shift function. 0: Normal. 1: Disable.
	DITHER_SEL[1:0]	6:5	Dither energy Selection. DITHER_EXTRA_SEL=0: 00: 1 delta. 01: 2 delta. 10: 1/2 delta. 11: 1/4 delta. DITHER_EXTRA_SEL=1: 00: 1/8 delta. 01: 1/16 delta. 10: 1/32 delta.

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: 1/64 delta.	
	SDM_MODE	4	SDM Mode (2nd order). 0: 1st order. 1: 2nd order.	
	-	3	Reserved.	
	DITHER_EXTRA_SEL	2	See "DITHER_SEL".	
	DWAOUT_FIX_MID	1	Fix DWA's output. 0: Disable. 1: Enable.	
	-	0	Reserved.	
34h (2D68h)	**REG2D68**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CLEAR_FIFO_STATUS	7	Clear FIFO Status bits. 0: Normal. 1: Clear FIFO Status.	
	FIFO_STATUS_6	6	ADC Right FIFO Status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_5	5	ADC Left FIFO Status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_4	4	DAC CH3 Left FIFO Status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_3	3	DAC CH2 Right FIFO Status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_2	2	DAC CH2 Left FIFO Status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_1	1	DAC CH1 Right FIFO Status. 0: Balance. 1: Overflow or under-run.	
	FIFO_STATUS_0	0	DAC CH1 Left FIFO Status. 0: Balance. 1: Overflow or under-run.	
35h	**REG2D6A**	**7:0**	**Default : 0x00**	**Access : R/W**

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2D6Ah)	-	7	Reserved.	
	SEL_ADCOUT	6	Select ADC source for SPDIF/IIS output. 0: Select channel 1. 1: Select channel 2.	
	-	5:1	Reserved.	
	DAC2_SEL	0	Analog DAC2 select DWA source. 0: Select source from DWA 2 (channel 2). 1: Select DWA from DWA 1 (channel 1). Note: Channel 2 Left = Sub-woofer / Right = Channel 1 Right.	
36h (2D6Ch)	**REG2D6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FS_SRC_EN	2	New FS SRC Mode. 0: Disable. 1: Enable.	
	CMP_SEL	1	Selection for the compensation filter's coefficient. 0: Default value. 1: Customer setting.	
	-	0	Reserved.	
37h (2D6Eh)	**REG2D6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRI_SEL2[3:0]	7:4	CODEC Filter Priority Selection 2.	
	PRI_SEL1[3:0]	3:0	CODEC Filter Priority Selection 1.	
38h (2D70h)	**REG2D70**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRI_SEL4[3:0]	7:4	CODEC Filter Priority Selection 4.	
	PRI_SEL3[3:0]	3:0	CODEC Filter Priority Selection 3.	
39h (2D72h)	**REG2D72**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRI_SEL6[3:0]	7:4	CODEC Filter Priority Selection 6.	
	PRI_SEL5[3:0]	3:0	CODEC Filter Priority Selection 5.	
3Bh (2D76h)	**REG2D76**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEBUG_CTRL1	3	Swap DAC4 L & R.	
	DEBUG_CTRL2	2	Swap DAC3 L & R.	
	DEBUG_CTRL3	1	Swap DAC2 L & R.	
	DEBUG_CTRL4	0	Swap DAC1 L & R.	
3Fh	**REG2D7E**	**7:0**	**Default : 0x00**	**Access : R/W**

AUDIO1 Register (Bank = 2D)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2D7Eh)	DAC0_INV_LR[7:0]	7:0	[7] DAC FIFO auto reset enable for channel 1, 2, 3 & 4. 0: Disable. 1: Enable. [6] DAC FIFO reset bundle with channel enable. 0: Disable. 1: Enable. [5:4] Reserved. [3:0] RIU control DAC FIFO manual reset. DAC FIFO channel 1 Reset: (RIU_DACFIFO_RESET[0] == 1) or (DSP DM_IO418F[0] == 1). DAC FIFO channel 2 Reset: (RIU_DACFIFO_RESET[1] == 1) or (DSP DM_IO418F[1] == 1). DAC FIFO channel 3 Reset: (RIU_DACFIFO_RESET[2] == 1) or (DSP DM_IO418F[2] == 1). DAC FIFO channel 4 Reset: (RIU_DACFIFO_RESET[3] == 1) or (DSP DM_IO418F[3] == 1).
40h (2D80h)	**REG2D80**	**7:0**	**Default : 0x00** **Access : R/W**
	CH1_PRESCALE[7:0]	7:0	Pre-scale value for channel 1 gain control. 00h: Off (mute). ... 19h: 0 dB (recommended). ... 7Fh: +14 dB (-0.13725 dB per step).
41h (2D82h)	**REG2D82**	**7:0**	**Default : 0x00** **Access : R/W**
	STEREO_SOURCE	7	Audio source setting (combined with CRB1.2). 0: Mono. 1: Stereo.
	SNDEFFECT_ON	6	Sound effect function for channel 1 global control. 0: Disable (software bypass). 1: Enable.
	-	5	Reserved.
	AVC	4	Auto Volume Control function setting. 0: Disable. 1: Enable.

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TONE	3	TONE (Bass/Treble) effect control. 0: Disable. 1: Enable.	
	SPATIAL	2	SPATIAL Surround function control. 0: Disable. 1: Enable. Note: 1) Dependent on bit 7 while enabled. 2) Bit 7 = 0, do mono to stereo. 3) Bit 7 = 1, do surrounding effect.	
	VOLUME_BALANCE	1	Volume and Balance function control. 0: Disable. 1: Enable.	
	SUBWOOFER	0	Enable SUBWOOFER function. 0: Disable.	
42h (2D84h)	**REG2D84**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_GRAPHICEQ	7	Enable CH1 Graphic EQ. 0: Disable. 1: Enable (priority higher than tone effect).	
	CH1_LOUDNESS	6	Enable CH1 Loudness. 0: Disable. 1: Enable.	
	GEQ_BAND_SEL	5	Graphic EQ Band Select. 0: 5-Band EQ. 1: 7-Band EQ.	
	-	4	Reserved.	
	CH1_LOUDNES_MODE[1:0]	3:2	Loudness mode (valid while 0x2D84[5] = 1). 00: Mode 0 (low slope). 01: Mode 1. 10: Mode 2. 11: Mode 3 (high slope).	
	CH1_AVC_MODE[1:0]	1:0	Response Time Selection for Auto Volume Control function. 00: Mode 0 (-20dB/-6dB). 01: Mode 1 (-20dB/-6dB). 10: Mode 2 (-20dB/-6dB). 11: Mode 3 (-20dB/-6dB).	
43h	**REG2D86**	**7:0**	**Default : 0x00**	**Access : R/W**

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2D86h)	-	7:5	Reserved.	
	CH1_BASS[4:0]	4:0	Bass Effect Selection. 0-0000: +00db. 0-0001: +01db. 0-0010: +02db. 0-0011: +03db. 0-0100: +04db. 0-0101: +05db. 0-0110: +06db. 0-0111: +07db. 0-1000: +08db. 0-1001: +09db. 0-1010: +10db. 0-1011: +11db. 0-1100: +12db. 0-1101: +13db. 0-1110: +14db. 0-1111: +15db. 1-0000: -16db. 1-0001: -15db. 1-0010: -14db. 1-0011: -13db. 1-0100: -12db. 1-0101: -11db. 1-0110: -10db. 1-0111: -09db. 1-1000: -08db. 1-1001: -07db. 1-1010: -06db. 1-1011: -05db. 1-1100: -04db. 1-1101: -03db. 1-1110: -02db. 1-1111: -01db.	
44h (2D88h)	**REG2D88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CH1_TREBLE[4:0]	4:0	Treble Effect Selection. 0-0000: +00db. 0-0001: +01db.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0-0010: +02db. 0-0011: +03db. 0-0100: +04db. 0-0101: +05db. 0-0110: +06db. 0-0111: +07db. 0-1000: +08db. 0-1001: +09db. 0-1010: +10db. 0-1011: +11db. 0-1100: +12db. 0-1101: +13db. 0-1110: +14db. 0-1111: +15db. 1-0000: -16db. 1-0001: -15db. 1-0010: -14db. 1-0011: -13db. 1-0100: -12db. 1-0101: -11db. 1-0110: -10db. 1-0111: -09db. 1-1000: -08db. 1-1001: -07db. 1-1010: -06db. 1-1011: -05db. 1-1100: -04db. 1-1101: -03db. 1-1110: -02db. 1-1111: -01db.	
45h (2D8Ah)	**REG_2D8A**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:6	Reserved.	
	CH1_MONO2STEREO_MODE[1:0]	5:4	Mode Selection for Mono to Stereo. 00: Virtual 40 degree source. 01: Virtual 20 degree source. 10: Virtual -20 degree source. 11: Virtual -40 degree source.	
	-	3:2	Reserved.	
	CH1_SURROUND_MODE[1:	1:0	Mode Selection for Surround.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	0]		00: Mountain Mode. 01: Champaign Mode. 10: City Mode. 11: Theater Mode.	
46h (2D8Ch)	**REG2D8C**	**7:0**	**Default : 0x81**	**Access : R/W**
	CH1_SOFTMUTE	7	Software Mute Channel 1. 0: Normal. 1: Mute.	
	CH1_VOLUME[6:0]	6:0	Volume control. Gain setting = 12db _ N*1.0 dB (+12db ~ -114db). N = 0 ~ 11 (+12 ~ +1db). N = 12 (0db). N = 13 ~ 126 (-1 ~ -114db). N = 127, mute.	
47h (2D8Eh)	**REG2D8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CH1_BALANCEL[3:0]	3:0	Left channel attenuation level. 0000: 0 db. 0001: -1 db. 0010: -2 db. 0011: -3 db. 0100: -4 db. 0101: -5 db. 0110: -6 db. 0111: -7 db. 1000: -8 db. 1001: -9 db. 1010: -10 db. 1011: -11 db. 1100: -12 db. 1101: -13 db. 1110: -14 db. 1111: Mute.	
48h (2D90h)	**REG2D90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CH1_BALANCER[3:0]	3:0	Right channel attenuation level. 0000: 0 db. 0001: -1 db.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0010: -2 db. 0011: -3 db. 0100: -4 db. 0101: -5 db. 0110: -6 db. 0111: -7 db. 1000: -8 db. 1001: -9 db. 1010: -10 db. 1011: -11 db. 1100: -12 db. 1101: -13 db. 1110: -14 db. 1111: Mute.	
49h (2D92h)	**REG2D92**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CH1_SUBWOFER[3:0]	3:0	Cut-frequency Selection for Sub-woofer. 0000: 50 Hz. 0001: 100 Hz. 0010: 150 Hz. 0011: 200 Hz. 0100: 250 Hz. 0101: 300 Hz. 0110: 350 Hz. 0111: 400 Hz. 1000: 450 Hz. 1001: 500 Hz. 1010: 550 Hz. 1011: 600 Hz. 1100: 650 Hz. 1101: 700 Hz. 1110: 750 Hz. 1111: 800 Hz.	
4Ah (2D94h)	**REG2D94**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND1 [4:0]	4:0	Center frequency is 120Hz. 00000: -12 db. 00001: -11 db. 00010: -10 db.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			00011: - 9 db. 00100: - 8 db. 00101: - 7 db. 00110: - 6 db. 00111: - 5 db. 01000: - 4 db. 01001: - 3 db. 01010: - 2 db. 01011: - 1 db. 01100: 0 db. 01101: 1 db. 01110: 2 db. 01111: 3 db. 10000: 4 db. 10001: 5 db. 10010: 6 db. 10011: 7 db. 10100: 8 db. 10101: 9 db. 10110: 10 db. 10111: 11 db. 11000: 12 db.	
4Bh (2D96h)	**REG2D96**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND2 [4:0]	4:0	Center frequency is 500Hz. Gain setting is the same as 0xBA.	
4Ch (2D98h)	**REG2D98**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND3 [4:0]	4:0	Center frequency is 1.5KHz. Gain setting is the same as 0xBA.	
4Dh (2D9Ah)	**REG2D9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND4 [4:0]	4:0	Center frequency is 5KHz. Gain setting is the same as 0xBA.	
4Eh (2D9Ch)	**REG2D9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND5	4:0	Center frequency is 10KHz.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	[4:0]		Gain setting is the same as 0xBA.	
50h (2DA0h)	**REG2DA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH2_SOFTMUTE	7	Software Mute Channel 2. 0: Normal. 1: Mute.	
	-	6	Reserved.	
	CH3_SOFTMUTE	5	Software Mute Channel 3. 0: Normal. 1: Mute.	
	-	4	Reserved.	
	CH4_SOFTMUTE	3	Software Mute Channel 4. 0: Normal. 1: Mute.	
	-	2:0	Reserved.	
51h (2DA2h)	**REG2DA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH2_PRESCALE[7:0]	7:0	Pre-scale value for channel 2 gain control. 00h: Off (mute). ... 19h: 0 dB (recommended). ... 7Fh: +14 dB (-0.13725 dB per step).	
52h (2DA4h)	**REG2DA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH3_PRESCALE[7:0]	7:0	Pre-scale value for channel 3 gain control. 00h: Off (mute). ... 19h: 0 dB (recommended). ... 7Fh: +14 dB (-0.13725 dB per step).	
53h (2DA6h)	**REG2DA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH4_PRESCALE[7:0]	7:0	Pre-scale value for channel 4 gain control. 00h: Off (mute). ... 19h: 0 dB (recommended). ... 7Fh: +14 dB (-0.13725 dB per step).	
54h (2DA8h)	**REG2DA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
	CH1_VOLUME_FRAC[2:0]	6:4	Fraction volume control of CH1. Gain setting = 0.125db * N (0~0.875db). N = 000, 0db. N = 001, 0.125db. N = 010, 0.250db. N = 011, 0.375db. N = 100, 0.500db. N = 101, 0.625db. N = 110, 0.750db. N = 111, 0.875db.	
	-	3:0	Reserved.	
56h (2DACh)	**REG2DAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	CH1_DAC_POWER_DOWN	7	DAC power down enable. 0: Normal mode. 1: Power down mode.	
	CH1_SWITCH_SOURCE	6	Channel switch. 0: Channel not switched. 1: Channel switched.	
	CH2_DAC_POWER_DOWN	5	DAC power down enable. 0: Normal mode. 1: Power down mode.	
	CH2_SWITCH_SOURCE	4	Channel switch. 0: Channel not switched. 1: Channel switched.	
	CH3_DAC_POWER_DOWN	3	DAC power down enable. 0: Normal mode. 1: Power down mode.	
	CH3_SWITCH_SOURCE	2	Channel switch. 0: Channel not switched. 1: Channel switched.	
	CH4_DAC_POWER_DOWN	1	DAC power down enable. 0: Normal mode. 1: Power down mode.	
	CH4_SWITCH_SOURCE	0	Channel switch. 0: Channel not switched. 1: Channel switched.	
57h	**REG2DAE**	**7:0**	**Default : 0x00**	**Access : R/W**

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2DAEh)	FM_RESERVED_REG[7:0]	7:0	For firmware application.	
60h (2DC0h)	**REG2DC0**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	DSP_DAC_CURRENT[4:0]	4:0	Audio DAC Current Selection (L/R/LFE). 0-0000: Minimum current. ... 1-1111: Maximum current.	
61h (2DC2h)	**REG2DC2**	**7:0**	**Default : 0x00**	**Access : RO**
	DSP_FD230_CODE_VER[7:0]	7:0	DSP FD230 code version.	
64h (2DC8h)	**REG2DC8**	**7:0**	**Default : 0x00**	**Access : RO**
	EN_AUDIO_L_VMID	7	Enable control of L-channel Vmid buffer. 0: Power-down L-channel Vmid buffer. 1: Power-up L-channel Vmid buffer.	
	EN_AUDIO_S_VMID	6	Enable control of S-channel Vmid buffer. 0: Power-down of S-channel Vmid buffer. 1: Power-up of S-channel Vmid buffer.	
	EN_AUDIO_R_BUFFER	5	Enable control of R-channel Output buffer. 0: Power-down R-channel Output buffer. 1: Power-up R-channel Output buffer.	
	EN_AUDIO_L_BUFFER	4	Enable control of L-channel Output buffer. 0: Power-down L-channel Output buffer. 1: Power-up L-channel Output buffer.	
	EN_AUDIO_S_BUFFER	3	Enable control of LFE-channel Output buffer. 0: Power-down LFE-channel Output buffer. 1: Power-up LFE-channel Output buffer.	
	EN_AUDIO_VREF	2	Enable control of Vref generator. 0: Power-down Vref generator. 1: Power-up Vref generator.	
	EN_AUDIO_VREF_BIAS	1	Enable control of bias current generator. 0: Power-down bias current generator. 1: Power-up bias current generator.	
	EN_AUDIO_BANDGAP	0	Enable control of audio bandgap. 0: Power-down audio bandgap. 1: Power-up audio bandgap.	
65h	**REG2DCA**	**7:0**	**Default : 0x00**	**Access : RO**

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2DCAh)	-	7:5	Reserved.	
	EN_AUDIO_I_REF	4	Enable control of audio current mirror. 0: Power-down audio current mirror. 1: Power-up audio current mirror.	
	-	3:2	Reserved.	
	EN_AUDIO_DAC_BIAS	1	Enable control of audio DAC bias circuit. 0: Power-down audio DAC bias circuit. 1: Power-up audio DAC bias circuit.	
	EN_AUDIO_R_VMID	0	Enable control of R-channel Vmid buffer. 0: Power-down R-channel Vmid buffer. 1: Power-up R-channel Vmid buffer.	
67h (2DCEh)	**REG2DCE**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CH1_DWA_RST	7	Reset DWA. 0: Normal. 1: DWA outputs all ZERO to analog.	
	CH1_DAC_CLK_ENABLE	6	DAC clock gate. 0: Normal. 1: Enable DAC clock.	
	CH1_FORCE_2ND_ORDER	5	Modulator Order. 0: 1st Order. 1: 2nd Order.	
	CH1_DAC_MODULATOR_ENABLE	4	DAC modulation enable. 0: Enable. 1: Disable.	
	CH2_DWA_RST	3	Reset DWA. 0: Normal. 1: DWA outputs all ZERO to analog.	
	CH2_DAC_CLK_ENABLE	2	DAC clock gate. 0: Normal. 1: Enable DAC clock.	
	CH2_FORCE_2ND_ORDER	1	Modulator Order. 0: 1st Order. 1: 2nd Order.	
	CH2_DAC_MODULATOR_ENABLE	0	DAC modulation enable. 0: Enable. 1: Disable.	
68h	**REG2DD0**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
(2DD0h)	CH3_DWA_RST	7	Reset DWA. 0: Normal. 1: DWA outputs all ZERO to analog.
	CH3_DAC_CLK_ENABLE	6	DAC clock gate. 0: Normal. 1: Enable DAC clock.
	CH3_FORCE_2ND_ORDER	5	Modulator Order. 0: 1st Order. 1: 2nd Order.
	CH3_DAC_MODULATOR_ENABLE	4	DAC modulation enable. 0: Enable. 1: Disable.
	CH4_DWA_RST	3	Reset DWA. 0: Normal. 1: DWA outputs all ZERO to analog.
	CH4_DAC_CLK_ENABLE	2	DAC clock gate. 0: Normal. 1: Enable DAC clock.
	CH4_FORCE_2ND_ORDER	1	Modulator Order. 0: 1st Order. 1: 2nd Order.
	CH4_DAC_MODULATOR_ENABLE	0	DAC modulation enable. 0: Enable. 1: Disable.
70h (2DE0h)	**REG2DE0**	**7:0**	**Default : 0x00** **Access : R/W**
	AUD_RST_MAD	7	Reset MPEG Audio Decoder Module. 0: Normal. 1: Software reset MAD module.
	AUD_DIS_DMA	6	Disable MIU DMA request. 0: Normal. 1: Disable (stop accessing DRAM).
	AUD_CLR_FIFO_STA	5	Clear ES/PCMI/PCMO FIFO Status (combined with DSP). 0: Normal. 1: Clear.
	AUD_SEL	4	0: MPEG. 1: AC3.
	-	3:1	Reserved.

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUD_MADBASE_SEL	0	MCU sets this bit to identify whether MCU or DSP is to configure MAD_OFFSET_BASE. 0: MCU. 1: DSP.	
70h (2DE1h)	**REG2DE1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CTRL_15	7	ES1_MLINK_MODE, M-link allows for modification of ES1_CNT.	
	CTRL_14	6	ES2_MLINK_MODE, M-link allows for modification of ES2_CNT.	
	CTRL_13	5	MCU1_ES1_MODE, MCU1 allows for modification of ES1_CNT.	
	CTRL_12	4	MCU2_ES2_MODE, MCU2 allows for modification of ES1_CNT.	
	AUD_ES1R_STA	3	ES1R channel status. 0: Idle. 1: Ongoing.	
	AUD_MASK_ES1R	2	CPU mask DSP doing ES1R. 0: Normal. 1: Mask ES1R.	
	AUD_RST_PAS	1	MIPS reset Audio PAS. 0: Normal. 1: Software reset Audio PAS.	
	AUD_SEL_INTR	0	Select interrupt PIO[7] interrupt source. 0: Stream type change. 1: SAR detect.	
71h (2DE2h)	**REG2DE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	STR_TYPE	0	DVB audio stream type, to DSP.	
72h (2DE4h)	**REG2DE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAD_OFFSET_BASE[7:0]	7:0	MAD memory (including ES, SIF and PCM) buffer base[31:16].	
72h (2DE5h)	**REG2DE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAD_OFFSET_BASE[15:8]	7:0	See description of '2DE4h'.	
73h (2DE6h)	**REG2DE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MBASE[7:0]	7:0	Indirect configuration memory buffer base[23:16]. Must set MEM_CFG first.	
74h	**REG2DE8**	**7:0**	**Default : 0xFF**	**Access : R/W**

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2DE8h)	MSIZE_H[7:0]	7:0	Indirect configuration memory buffer end [15:8]. Must set MEM_CFG first. Memory buffer end [7:0] = 0xff. Actual buffer size = MSIZE + 1.	
75h (2DEAh)	**REG2DEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MEM_CFG[2:0]	2:0	Indirect configured 0x03 and 0x04 memory space. 000: SIF-ch1 memory configuration. 001 =SIF-ch2 memory configuration. 010: ES-ch1 memory configuration. 011: ES-ch2 memory configuration. 100: PCM-ch1 memory configuration. 101: PCM-ch2 memory configuration. 11x: DSP data memory configuration.	
76h (2DECh)	**REG2DEC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	P_AUD_OUT_MODE[1:0]	7:6	DVB audio PCM output mode. 00: Stereo. 01: Left Channel. 10: Right Channel. 11: Mute.	
	P_AUD_TYPE	5	1: Free run. 0: AV sync.	
	P_AUD_MODE_CMD[4:0]	4:0	System command. 0-0000: Stop (mute). 0-0001: Play. 0-0010: Play file (MHEG5/MP3). Others: Reserved.	
77h (2DEFh)	**REG2DEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DSPDMA_CMD_STA	5	Command/Status. 0: Idle/Finish. 1: Assert to start DMA, auto-clear when work is finished.	
	DSPDMA_CLR_CNT	4	Clear memory counter. Clear read/write pointer. Update DMA address to base address.	
	DSPDMA_SET_PRIORITY	3	MIU Priority. 0: Low priority.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: High priority.	
	DSPDMA_WIDTH_SEL	2	Data width. 0: 16 bits. 1: 24 bits.	
	DSPDMA_BURST_LENGTH[1:0]	1:0	Burst length. 00: Reserved. 01: 2 * 64 bits. 10: 3 * 64 bits. 11: 6 * 64 bits. In 24-bit mode, it must align to 3 burst length.	
78h (2DF0h)	**REG2DF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSPDMA_MIU_ADDR[7:0]	7:0	MIU start address for DMA transfer. Auto-increasing when DMA is working. Auto-wrap to base address when counting to end address.	
78h (2DF1h)	**REG2DF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSPDMA_MIU_ADDR[15:8]	7:0	See description of '2DF0h'.	
79h (2DF2h)	**REG2DF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSPDMA_DSP_ADDR[7:0]	7:0	IDMA address IAD.	
79h (2DF3h)	**REG2DF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSPDMA_DSP_RW	7	DSP IDMA read/write DRAM. 0: Read. 1: Write.	
	DSPDMA_DSP_MEM_SEL	6	DSP IDMA start address for DMA transfer. Auto-increasing when DMA is working. 0: Select PM / CM. 1: Select DM.	
	DSPDMA_DSP_ADDR[13:8]	5:0	See description of '2DF2h'.	
7Ah (2DF4h)	**REG2DF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DSPDMA_DMA_SIZE[7:0]	7:0	DMA transfer size in unit of 128 bits. It must align to burst length.	
7Ah (2DF5h)	**REG2DF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DSPDMA_DMA_SIZE[11:8]	3:0	See description of '2DF4h'.	
7Bh (2DF6h)	**REG2DF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description	
	DSPDMA_CFG[1:0]	1:0	0x58F7 ~ 0x58FA configuration. 00: DMA1. 01: DMA2. 10: DMA3. 11: DMA4.	
7Ch (2DF8h)	**REG2DF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	ES1_CNT[7:0]	7:0	Allow CPU to control ES1 MIU counter. Steps are as follows: 1: Mask DSP ES1 read (AUD_CTRL[10]). 2: Double read and check ES1R status (AUD_CTRL[11]). 3: Read ES1_CNT. 4: Modify it and write back. 5: Unmask ES1 read.	
7Ch (2DF9h)	**REG2DF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	ES1_CNT[15:8]	7:0	See description of '2DF8h'.	
7Dh (2DFAh)	**REG2DFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	AD_CFG[2:0]	4:2	Indirect access select. 0: AD_BUF_BASE[23:8]. 1: AD_BUF_BASE[7:0]. 2: AD_BUF_SIZE[15:0]. 3: AD_SUB_ES2_CNT[7:0]. 4: AD_ADD_AD_CNT[7:0].	
	ES2_CNT_MASK	1	MIPS read ES2_CNT, must be masked first to avoid meta-stable issue.	
	AD_MODE	0	Audio Description Mode Enable.	
7Eh (2DFCh)	**REG2DFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	INDIR_WR_DATA[7:0]	7:0	Indirect Write Data when writing OP, or. Indirect Read Data when reading OP.	
7Eh (2DFDh)	**REG2DFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	INDIR_WR_DATA[15:8]	7:0	See description of '2DFCh'.	
7Fh (2DFEh)	**REG2DFE**	**7:0**	**Default : 0x00**	**Access : RO**
	ES2_CNT[7:0]	7:0	ES2_CNT for AD mode.	
7Fh (2DFFh)	**REG2DFF**	**7:0**	**Default : 0x00**	**Access : RO**
	ES2_CNT[15:8]	7:0	See description of '2DFEh'.	

Scaler 1 Register (Bank = 2F)

GOP_INT Register (Bank = 2F, Sub-Bank = 00)

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	SC_RIU_BANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]:. SWRST1[4]: IP, include F1 and F2.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			SWRST1[3]: OP include OP1, VIP and VOP. SWRST1[2]: IP_F2. SWRST1[1]: IP_F1. SWRST1[0]: All engines.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PDMD[1:0]	1:0	PowerDown mode:. 01: IDCLK. Others: IDCLK and ODCLK.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 VS INT Edge. 1: Tailing. 0: Leading.	
	IPVSINT_EDGE	0	IP VS INT Edge. 1: Tailing. 0: Leading.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CHG_HMD	0	CHG_HMD: H Change Mode for INT. 0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_SYNC_TO_GOP_SEL[1:0]	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.	
	GOP2IP_EN	5	GOP blending to IP enable.	
	-	4:0	Reserved.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GOP2IP_DATA_SEL[1:0]	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	COP_EN	7	Enable cop for VOP2.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_7_0[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
11h	**REG2F23**	**7:0**	**Default : 0x00**	**Access : RO**

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F23h)	IRQ_FINAL_STATUS_31_24[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[0]: IPHCs1_DET_INT_F2.	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
17h (2F2Fh)	**REG2F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_7_0[7:0]	7:0	The raw status of interrupt source. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_15_8[7:0]	7:0	The raw status of interrupt source. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_23_16[7:0]	7:0	The raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
19h (2F33h)	**REG2F33**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_31_24[7:0]	7:0	The raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (2F41h)	**REG2F41**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	See description of '2F40h'.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (2F45h)	**REG2F45**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '2F44h'.	
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '2F46h'.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (2F49h)	**REG2F49**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	See description of '2F48h'.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0xE1**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.	
33h (2F67h)	**REG2F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	WDT_EN	0	H/V sync lose watch dog timer count enable.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
00h	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2F00h)	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.
02h **(2F04h)**	**REG2F04**	**7:0**	**Default : 0x83** **Access : R/W**
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.
	CSC_EN	3	Input CSC function. 0: Disable (RGB -> RGB, default). 1: Enable (RGB -> YCbCr).

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: HDTV. 111: HDMI.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. 0: Disable (Auto selected by h/W, used when input is video, default). 1: Enable (use 02h[14:12] as divider).	
	-	6	Reserved.	
	VD_PORT_SEL	5	External VD Port. 0: Port 0. 1: Port 1.	
	VD_ITU	4	VD ITU656 out, and Digital In for scaler.	
	VDEXT_SYNMD	3	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. 00: External 8/10 bits video port. 01: Internal video decoder mode A. 10: External 16/20 bits video port. 11: Internal video decoder mode B.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	VS_DLYMD	5	Input VSYNC Delay select. 0: Delay 1/4 input HSYNC. 1: No delay.
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.
	EXTEND_EARLY_LN	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.
	VWRAP	1	Input image Vertical wrap. 0: Disable. 1: Enable.
	HWRAP	0	Input image Horizontal wrap. 0: Disable. 1: Enable.
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x80** **Access : R/W**
	FRCV	7	Source Sync Enable. 1: Display will adaptive follow the Source. If Display Select this source. 0: Display Free Run. If Display Select this source.
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change,. The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.
	FREE_FOLLOW	5	No memory bank control (used when FRCV= 1).
	FRC_FREEMD	4	Force output odd/even toggle when. 2DDi for interlace input..
	DATA10BIT	3	Set 10 bit input mode.
	DATA8_ROUND	2	Use rounding for 8 bits input mode.
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.
	RESERVED	0	

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	See description of '2F08h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	See description of '2F0Ah'.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_VDC[10:8]	2:0	See description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_HDC[10:8]	2:0	See description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. 0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. 0: Mask. 1: No mask.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). 0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. 1: Use Hsync only. When ISEL = 011:(DVI). 0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). 0: Normal. 1: Output Black at blanking.
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.
	VDO_ML_SWAP	0	MSB/LSB Swap. 0: Normal. 1: MSB/LSB swap.
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00** **Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.
	-	6	Reserved.
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. 0: Use Separate Hs for Coast Period. 1: Use PLL Hsout for Coast Period.
	-	4	Reserved.
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00** **Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]= 1.
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. 0: Leading edge. 1: Tailing edge.
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]= 0 is better).
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. 0: Auto Switch VST(04), VDC (06). 1: Disable Auto Switch VST(04), VDC(06).

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. 0000: 8 Line Ahead from SPRange_Vst. 0001: 1 Line Ahead from SPRange_Vst. 0010: 2 Line Ahead from SPRange_Vst. 0011: 3 Line Ahead from SPRange_Vst. .. 1111: 15 Line Ahead from SPRange_Vst.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Bh (2F17h)	**REG2F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_MIR	7	H Mirror Enable.	
	-	6:0	Reserved.	
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. 0: HW Auto Decide. 1: SW Program.	
0Dh (2F1Ah)	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5 tap support. 1: Down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5 tap. 1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Eh	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F1Ch)	ATG_HIR	7	Max value flag for R channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. 0: Disable. 1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. 0: Result not ready. 1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. 0: Disable. 1: Enable.	
0Eh (2F1Dh)	**REG2F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_10BIT	7	Auto gain 10bits mode.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AV_DET	6	AV Detect for Cb Cr. 0: CbCr Range is define by 03[2]. YCbCr_En. 1: Cb Cr Min is define in 89 ATP_GTH,. Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (2F1Eh)	**REG2F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. 0: Disable. 1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). 0: Coast is inactive. 1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	PIP_SW_DOUBLE	3	Double Sample for. 1. VD. 2. Ext VD 656 Format. 3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. 000: Minimum R value. 001: Minimum G value. 010: Minimum G value. 011: Maximum R value. 100: Maximum G value. 101: Maximum B value. 11x: Reserved.
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: Right result.
	JIT_SWCLR_SB	6	Jitter Software clear. 0: Not clear. 1: Clear.
	-	5	Reserved.
	JITTER_HISMD	4	Jitter function Mode. 0: Update every frame. 1: Keep the history value.
	JITTER	3	JITTER function Result. 0: No JITTER. 1: JITTER present.
	ATS_HISMD	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.
	ATS_READY	1	Auto position result Ready. 0: Result ready. 1: Result not ready.

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATS_EN	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	THOLD[3:0]	7:4	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. & 1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Positoin Force Pixel Mode. 0: DE or Pixel decide by the Source. 1: Force Pixel Mode.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Auto Gain Value. (selected by register 0Fh[2:0]).	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '2F22h'.	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	ATS_VSTDBUF[10:8]	2:0	See description of '2F24h'.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	ATS_HSTDBUF[11:8]	3:0	See description of '2F26h'.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h	**REG2F29**	**7:0**	**Default : 0x00**	**Access : RO**

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F29h)	-	7:3	Reserved.	
	ATS_VEDDBUF[10:8]	2:0	See description of '2F28h'.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	ATS_HEDDBUF[11:8]	3:0	See description of '2F2Ah'.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on 10h[7] (default = 7fh).	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	REG_JLST[11:8]	3:0	See description of '2F2Ch'.	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	L12_LIMIT_EN	5	Background Noise reduction Enable. 0: Disable. 1: Enable.	
	HIPX_LIMIT_EN	4	High level Noise reduction Enable. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. 111: Noise level = 16.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24].	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.
	ATP_READY	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.
	ATP_EN	0	Auto Phase function Enable. 0: Disable. 1: Enable.
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00** **Access : R/W**
	ATP[7:0]	7:0	Auto Phase Value.
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x00** **Access : R/W**
	ATP[15:8]	7:0	See description of '2F34h'.
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00** **Access : R/W**
	ATP[23:16]	7:0	See description of '2F34h'.
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00** **Access : R/W**
	ATP[31:24]	7:0	See description of '2F34h'.
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	LB_TUNE_READY	7	Input VSYNC Blanking Status. 0: In display. 1: In blanking.
	DELAYLN_NUM[2:0]	6:4	Delay Line After Sample V Start for Input Trigger Point.
	-	3:2	Reserved.
	UNDERRUN	1	Under run status for FIFO.
	OVERRUN	0	Over run status for FIFO.
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0x05** **Access : R/W**
	-	7	Reserved.
	DE_LOCKH_MD	6	DE Lock H Postion Mode.
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. 5: Default value.

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. 0: Disable. 1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. 1: Default value.	
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_OFFMUX[1:0]	7:6	Off Line SOG source select. 00: Select analog 1 SOG. 01: Select analog 2 SOG. 10: Select analog 3 SOG.	
	IPHCS0_ACT	5	Analog 1 HSYNC Pin Active.	
	IPHCS1_ACT	4	Analog 2 HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. 0: Not active. 1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. 0: Not active. 1: Active.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description
	CS_DET	5	Composite Sync Detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.
	SOG_DET	4	Sync-On-Green Detected status. 0: Input is not SOG. 1: Input is detected as SOG.
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.
	FIELD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0x00** **Access : R/W**
	VTT[7:0]	7:0	Input Vertical Total, count by HSYNC.
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00** **Access : R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.
	-	6	Reserved.
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.
	-	4:3	Reserved.
	VTT[10:8]	2:0	See description of '2F3Eh'.
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x00** **Access : R/W**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.
20h (2F41h)	**REG2F41**	**7:0**	**Default : 0x00** **Access : R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. 0: 1 line. 1: 8 lines.

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	TEST_CSHTT	6	Report Sync Seperator Htt by E5, E4. 0: Htt Report by Mode Detector. 1: Htt Report by Sync Seperator.
	HTT_FOR_READ[13:8]	5:0	See description of '2F40h'.
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00** **Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. 0: Old method. 1: New method.
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD = 1. 0: Active low. 1: Active high.
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_VsPol).
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD = 1. 0: Active low. 1: Active high.
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_HsPol).
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_IntLac).
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00** **Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. 00: Sample V End. 01: Sample V Start. 10: Sample V Start Ahead by Current Bank 09[3:0]. 11: Sample V Start Ahead by Current Bank 09[3:0] x 2.

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. 0: Mode Change Provide in data clock Domain. 1: Mode Change Provide in data clock and Fix Clock Domain (recommended).
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. 0: Form Input DE. 1: From Re-generated DE.
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. 0: Normal. 1: Invert.
	EXT_FIELDMD	2	Video External Field. 0: Use result of internal circuit detection. 1: Use external field.
	FIELD_DETMD	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.
	FIELD_INV	0	Interlace Field Invert. 0: Normal. 1: Invert.
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00** **Access : RO**
	HSPW[7:0]	7:0	Pulse Width Report. If Current Bank HSPW_sel (1F[13]) = 0, Report HSYNC. If Current Bank HSPW_sel (1F[13]) = 1, Report VSYNC.
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x1E** **Access : R/W**
	DVICK_WIDTH[7:0]	7:0	DVI clock detection threshold, see Cah for usage (default 0x1E). Cah[6] = 0: DVI clock is OK, Freq(DVI) > Freq(xtal) * 23h/128. Cah[6] = 1: DVI clock is missing, Freq(DVI) < Freq(xtal) * 23h/128. Where Ebh default to 0x1E(30).
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. 0: RAW VSYNC (H / V Relationship is Keep for Interlace Detect). 1: HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) =. 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. 0: PC Source. 1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) =. 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). 0: Disable. 1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. 0: Internal Seperated VSYNC.(Default). 1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h	**REG2F49**	**7:0**	**Default : 0x00**	**Access : R/W**

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2F49h)	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. &. 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x00** **Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. &. 254: Coast end at 255 HSYNC leading edge. 255: Coast end at 256 HSYNC leading edge.
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00** **Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. 0: Disable. 1: Enable.
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog:. 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI:. 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog:. 0: Filter off. 1: Filter on. When input source is DVI:. 0: Normal. 1: More tolerance for unstable DE.
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. 0: Normal. 1: Invert.	
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AFT	7	ATP Filter for Text (4 frames). 0: Disable. 1: Enable.	
	IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.	
	VSGR	5	VSYNC glitch removal with line less than 2 (DE Only). 0: Disable. 1: Enable.	
	VSP	4	VSYNC Protect with V total (DE Only). 0: Disable. 1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable. 1: Enable.	
	-	1:0	Reserved.	
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. 00: Off. 01: Only for line total number is even. 10: All case. 11: Off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (2F53h)	**REG2F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. 0: Define Automatically. 1: Define by Current Bank 2a-2b.	
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATRANGE_VST[10:8]	2:0	See description of '2F54h'.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATRANGE_HST[10:8]	2:0	See description of '2F56h'.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATRANGE_VDC[10:8]	2:0	See description of '2F58h'.	
2Dh (2F5Ah)	**REG2F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (2F5Bh)	**REG2F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATRANGE_HDC[10:8]	2:0	See description of '2F5Ah'.	
2Eh (2F5Ch)	**REG2F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GOP_CLK_FREE	1	GOP clock gating enable. 0: Can gate the GOP clock. 1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. 0: Don't gate the idclk. 1: Can gate the idclk.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '2F60h'.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync lock_number_offset enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '2F62h'.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK[7:0]	7:0	VLOCK.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. 0x: Reference 21[15:14]. 10: Sample V end delay 3 line. 11: Sample V end delay 4 line.	
	-	5:3	Reserved.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	

IP2_M Register (Bank = 2F, Sub-Bank = 02)

IP2_M Register (Bank = 2F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HWSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	

IP2_M Register (Bank = 2F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (2F03h)	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bits to 8-bits.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '2F04h'.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '2F04h'.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '2F08h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '2F08h'.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode. 0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	

IP2_M Register (Bank = 2F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[15:8]	7:0	See description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '2F10h'.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '2F10h'.	
09h (2F13h)	**REG2F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB 1: Bilinear	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	-	4:0	Reserved.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP	6	Cb/Cr swap for 444 to 422.	
	-	5	Reserved.	
	YDELAY_EN	4	Y delay enable.	
	YCDELAY_STEP[3:0]	3:0	Y/C delay pipe step.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0xF2**	**Access : R/W**
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x1F**	**Access : R/W**
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x5E**	**Access : R/W**
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0xF4**	**Access : R/W**
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	

IP2_M Register (Bank = 2F, Sub-Bank = 02)

Index (Absolute)	Mnemonic	Bit	Description	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x0C**	**Access : R/W**
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x5A**	**Access : R/W**
	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x37**	**Access : R/W**
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0xF5**	**Access : R/W**
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y0. Format: S7 of 2's complement (-15 <= Y0 <= 15).	
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 127).	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:4	Reserved.	
	PRE_ALIGN_WIDTH[3:0]	3:0	Insert pixel number for mirror mode.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x44**	**Access : R/W**
	-	7	Reserved.	
	CTI_STEP[2:0]	6:4	CTI filter step.	
	-	3	Reserved.	
	CTI_LPF_COEF[2:0]	2:0	CTI low-pass filter coefficient.	
2Ch	**REG2F59**	**7:0**	**Default : 0x3F**	**Access : R/W**

IP2_M Register (Bank = 2F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F59h)	-	7:6	Reserved.	
	CTI_BAND_COEF[5:0]	5:0	CTI band-pass filter coefficient.	
2Dh (2F5Ah)	**REG2F5A**	**7:0**	**Default : 0x88**	**Access : R/W**
	CTI_MEDIAN_EN	7	CTI median filter enable.	
	-	6:4	Reserved.	
	CTI_CORING_THRD[3:0]	3:0	CTI coring threshold.	
2Dh (2F5Bh)	**REG2F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN	7	CTI enable.	
	-	6:4	Reserved.	
	CTI_AUTO_NO_MED	3	CTI auto-turn-off median mode.	
	-	2:0	Reserved.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x81**	**Access : R/W**
	IP2_STATUS_CLR	7	IP2 status clear.	
	-	6:1	Reserved.	
	DLAST_ALIGN_EN	0	Data last signal align with IPM fetch number.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IP2_FLOW_CTRL_EN	4	IP2 flow control enable.	
	FLOW_CTRL_VALUE[3:0]	3:0	IP2 flow control count.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VIN_CTRL_EN	4	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	3	IP2 VSD input line count number setting enable.	
	VSD_IN_NUM_USR[10:8]	2:0	See description of '2F6Ch'.	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (2F6Fh)	**REG2F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VOUT_CTRL_EN	4	IP2 VSD output line count control enable.	
	-	3	Reserved.	
	VSD_OUT_NUMBER[10:8]	2:0	See description of '2F6Eh'.	

IP2_M Register (Bank = 2F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Dh (2F7Ah)	**REG2F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_LBUF_CNT[7:0]	7:0	IP2 line buffer max pixels count.	
3Dh (2F7Bh)	**REG2F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	BW_NOT_ENOUGH	0	IP2 line buffer full.	
3Eh (2F7Ch)	**REG2F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (2F7Dh)	**REG2F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	READ_HSD_OUT_CNT[11:8]	3:0	See description of '2F7Ch'.	
3Fh (2F7Eh)	**REG2F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (2F7Fh)	**REG2F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	READ_VSD_OUT_CNT[10:8]	2:0	See description of '2F7Eh'.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.	
	CSC_EN	3	Input CSC function.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable (RGB -> RGB, default). 1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: HDTV. 111: HDMI.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. 0: Disable (Auto selected by h/W, used when input is video, default). 1: Enable (use 02h[14:12] as divider).	
	-	6	Reserved.	
	VD_PORT_SEL	5	External VD Port. 0: Port 0. 1: Port 1.	
	VD_ITU	4	VD ITU656 out, and Digital In for scaler.	
	VDEXT_SYNMD	3	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Fromat.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. 00: External 8/10 bits video port. 01: Internal video decoder mode A. 10: External 16/20 bits video port. 11: Internal video decoder mode B.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	VS_DLYMD	5	Input VSYNC Delay select. 0: Delay 1/4 input HSYNC. 1: No delay.
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.
	EXTEND_EARLY_LN	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.
	VWRAP	1	Input image Vertical wrap. 0: Disable. 1: Enable.
	HWRAP	0	Input image Horizontal wrap. 0: Disable. 1: Enable.
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x80** **Access : R/W**
	FRCV	7	Source Sync Enable. 1: Display will adaptive follow the Source. If Display Select this source. 0: Display Free Run. If Display Select this source.
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change,. The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.
	FREE_FOLLOW	5	No memory bank control (used when FRCV= 1).
	FRC_FREEMD	4	Force output odd/even toggle when. 2DDi for interlace input..
	DATA10BIT	3	Set 10 bit input mode.
	DATA8_ROUND	2	Use rounding for 8 bits input mode.
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.
	RESERVED	0	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	See description of '2F08h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	See description of '2F0Ah'.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_VDC[10:8]	2:0	See description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_HDC[10:8]	2:0	See description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. 0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. 0: Mask. 1: No mask.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). 0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. 1: Use Hsync only. When ISEL = 011:(DVI). 0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). 0: Normal. 1: Output Black at blanking.
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.
	VDO_ML_SWAP	0	MSB/LSB Swap. 0: Normal. 1: MSB/LSB swap.
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00** **Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.
	-	6	Reserved.
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. 0: Use Separate Hs for Coast Period. 1: Use PLL Hsout for Coast Period.
	-	4	Reserved.
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00** **Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]= 1.
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. 0: Leading edge. 1: Tailing edge.
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]= 0 is better).
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. 0: Auto Switch VST(04), VDC (06). 1: Disable Auto Switch VST(04), VDC(06).
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Switch. 0000: 8 Line Ahead from SPRange_Vst. 0001: 1 Line Ahead from SPRange_Vst. 0010: 2 Line Ahead from SPRange_Vst. 0011: 3 Line Ahead from SPRange_Vst. .. 1111: 15 Line Ahead from SPRange_Vst.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Bh (2F17h)	**REG2F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_MIR	7	H Mirror Enable.	
	-	6:0	Reserved.	
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. 0: HW Auto Decide. 1: SW Program.	
0Dh (2F1Ah)	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5 tap support. 1: Down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5 tap. 1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). 0: Normal.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. 0: Disable. 1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. 0: Result not ready. 1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. 0: Disable. 1: Enable.	
0Eh (2F1Dh)	**REG2F1D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_10BIT	7	Auto gain 10bits mode.	
	AV_DET	6	AV Detect for Cb Cr. 0: CbCr Range is define by 03[2]. YCbCr_En. 1: Cb Cr Min is define in 89 ATP_GTH,.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			Cb Cr Max is define in 8A ATP_TH.
	-	5:3	Reserved.
	ATG_UPR	2	Min value flag for R channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.
	ATG_UPG	1	Min value flag for G channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.
	ATG_UPB	0	Min value flag for B channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.
0Fh (2F1Eh)	**REG2F1E**	**7:0**	**Default : 0x00** **Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. 0: Disable. 1: Enable.
	OP2_COAST	6	. Coast Status (Read only). 0: Coast is inactive. 1: Coast is active (free run).
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.
	PIP_SW_DOUBLE	3	Double Sample for. 1. VD. 2. Ext VD 656 Format.

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. 000: Minimum R value. 001: Minimum G value. 010: Minimum G value. 011: Maximum R value. 100: Maximum G value. 101: Maximum B value. 11x: Reserved.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: Right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. 0: Not clear. 1: Clear.	
		5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. 0: Update every frame. 1: Keep the history value.	
	JITTER	3	JITTER function Result. 0: No JITTER. 1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. 0: Result ready. 1: Result not ready.	
	ATS_EN	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h	**REG2F21**	**7:0**	**Default : 0x00**	**Access : R/W**

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F21h)	THOLD[3:0]	7:4	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. &. 1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Positoin Force Pixel Mode. 0: DE or Pixel decide by the Source. 1: Force Pixel Mode.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Auto Gain Value. (selected by register 0Fh[2:0]).	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '2F22h'.	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	ATS_VSTDBUF[10:8]	2:0	See description of '2F24h'.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	ATS_HSTDBUF[11:8]	3:0	See description of '2F26h'.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	ATS_VEDDBUF[10:8]	2:0	See description of '2F28h'.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h	**REG2F2B**	**7:0**	**Default : 0x00**	**Access : RO**

IP1_S Register (Bank = 2F, Sub-Bank = 03)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2F2Bh)	-	7:4	Reserved.
	ATS_HEDDBUF[11:8]	3:0	See description of '2F2Ah'.
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0x00** **Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on 10h[7] (default = 7fh).
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x00** **Access : RO**
	-	7:4	Reserved.
	REG_JLST[11:8]	3:0	See description of '2F2Ch'.
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:6	Reserved.
	L12_LIMIT_EN	5	Background Noise reduction Enable. 0: Disable. 1: Enable.
	HIPX_LIMIT_EN	4	High level Noise reduction Enable. 0: Disable. 1: Enable.
	-	3	Reserved.
	PIX_TH[2:0]	2:0	Auto Noise Level 111: Noise level = 16.
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x01** **Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x10** **Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24].
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	-	7	Reserved.
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).
	ATP_TXT	5	Auto Phase Text detect (Read Only).
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit.

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			110: Mask 6 bit. 111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. 0: Disable. 1: Enable.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP[7:0]	7:0	Auto Phase Value.	
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP[15:8]	7:0	See description of '2F34h'.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP[23:16]	7:0	See description of '2F34h'.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP[31:24]	7:0	See description of '2F34h'.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LB_TUNE_READY	7	Input VSYNC Blanking Status. 0: In display. 1: In blanking.	
	DELAYLN_NUM[2:0]	6:4	Delay Line After Sample V Start for Input Trigger Point.	
	-	3:2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7	Reserved.	
	DE_LOCKH_MD	6	DE Lock H Postion Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. 5: Default value.	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Sepertator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. 0: Disable. 1: Enable (update Htt after 4 sequential lines over	

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description
			tolerance).
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. 1: Default value.
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	SOG_OFFMUX[1:0]	7:6	Off Line SOG source select. 00: Select analog 1 SOG. 01: Select analog 2 SOG. 10: Select analog 3 SOG.
	IPHCS0_ACT	5	Analog 1 HSYNC Pin Active.
	IPHCS1_ACT	4	Analog 2 HSYNC Pin Active.
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0x00** **Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. 0: Not active. 1: Active.
	IPHS_ACT	6	Input On Line Source HSYNC Active. 0: Not active. 1: Active.
	CS_DET	5	Composite Sync Detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.
	SOG_DET	4	Sync-On-Green Detected status. 0: Input is not SOG. 1: Input is detected as SOG.

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.
	FIELD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0x00** **Access : R/W**
	VTT[7:0]	7:0	Input Vertical Total, count by HSYNC.
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00** **Access : R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulase Width for Measurement.
	-	6	Reserved.
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.
	-	4:3	Reserved.
	VTT[10:8]	2:0	See description of '2F3Eh'.
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x00** **Access : R/W**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.
20h (2F41h)	**REG2F41**	**7:0**	**Default : 0x00** **Access : R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. 0: 1 line. 1: 8 lines.
	TEST_CSHTT	6	Report Sync Seperator Htt by E5, E4. 0: Htt Report by Mode Detector. 1: Htt Report by Sync Seperator.
	HTT_FOR_READ[13:8]	5:0	See description of '2F40h'.
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00** **Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. 0: Old method.

IP1_S Register (Bank = 2F, Sub-Bank = 03)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			1: New method.
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD = 1. 0: Active low. 1: Active high.
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_VsPol).
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD = 1. 0: Active low. 1: Active high.
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_HsPol).
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_IntLac).
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00** **Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. 00: Sample V End. 01: Sample V Start. 10: Sample V Start Ahead by Current Bank 09[3:0]. 11: Sample V Start Ahead by Current Bank 09[3:0] x 2.
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. 0: Mode Change Provide in data clock Domain. 1: Mode Change Provide in data clock and Fix Clock Domain (recommended).
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. 0: Form Input DE. 1: From Re-generated DE.

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. 0: Normal. 1: Invert.	
	EXT_FIELDMD	2	Video External Field. 0: Use result of internal circuit detection. 1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. 0: Normal. 1: Invert.	
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	Pulse Width Report. If Current Bank HSPW_sel (1F[13]) = 0, Report HSYNC. If Current Bank HSPW_sel (1F[13]) = 1, Report VSYNC.	
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x1E**	**Access : R/W**
	DVICK_WIDTH[7:0]	7:0	DVI clock detection threshold, see Cah for usage (default 0x1E). Cah[6] = 0: DVI clock is OK, Freq(DVI) > Freq(xtal) * 23h/128. Cah[6] = 1: DVI clock is missing, Freq(DVI) < Freq(xtal) * 23h/128. Where Ebh default to 0x1E(30).	
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Seperator VSYNC for Mode Detect. 0: RAW VSYNC (H / V Relationship is Keep for Interlace Detect). 1: HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			(VIDEO_D1L_H + Video_D1L_L) =. 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. 0: PC Source. 1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) =. 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). 0: Disable. 1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. 0: Internal Seperated VSYNC.(Default). 1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (2F49h)	**REG2F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. &. 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.	
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. &. 254: Coast end at 255 HSYNC leading edge.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			255: Coast end at 256 HSYNC leading edge.	
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. 0: Disable. 1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog:. 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI:. 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog:. 0: Filter off. 1: Filter on. When input source is DVI:. 0: Normal. 1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommand).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. 0: Normal. 1: Invert.	
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AFT	7	ATP Filter for Text (4 frames). 0: Disable. 1: Enable.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.
	VSGR	5	VSYNC glitch removal with line less than 2 (DE Only). 0: Disable. 1: Enable.
	VSP	4	VSYNC Protect with v total (DE Only). 0: Disable. 1: Enable.
	-	3	Reserved.
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable. 1: Enable.
	-	1:0	Reserved.
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode 00: Off. 01: Only for line total number is even. 10: All case. 11: Off.
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.
29h (2F53h)	**REG2F53**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.
	-	3:1	Reserved.
	ATRANGE_EN	0	Auto Range Enable. 0: Define Automatically. 1: Define by Current Bank 2a-2b.
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00** **Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.

IP1_S Register (Bank = 2F, Sub-Bank = 03)

Index (Absolute)	Mnemonic	Bit	Description	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATRANGE_VST[10:8]	2:0	See description of '2F54h'.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATRANGE_HST[10:8]	2:0	See description of '2F56h'.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATRANGE_VDC[10:8]	2:0	See description of '2F58h'.	
2Dh (2F5Ah)	**REG2F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (2F5Bh)	**REG2F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATRANGE_HDC[10:8]	2:0	See description of '2F5Ah'.	
2Eh (2F5Ch)	**REG2F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. 0: Can gate the GOP clock. 1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. 0: Don't gate the idclk. 1: Can gate the idclk.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	

IP1_S Register (Bank = 2F, Sub-Bank = 03)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INSERT_NUM[10:8]	2:0	See description of '2F60h'.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync lock_number_offset enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '2F62h'.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK[7:0]	7:0	VLOCK.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. 0x: Reference 21[15:14]. 10: Sample V end delay 3 line. 11: Sample V end delay 4 line.	
	-	5:3	Reserved.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	

IP2_S Register (Bank = 2F, Sub-Bank = 04)

IP2_S Register (Bank = 2F, Sub-Bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
01h	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**

IP2_S Register (Bank = 2F, Sub-Bank = 04)

Index (Absolute)	Mnemonic	Bit	Description	
(2F03h)	-	7:4	Reserved.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bits to 8-bits.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '2F04h'.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '2F04h'.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '2F08h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '2F08h'.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode. 0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[15:8]	7:0	See description of '2F0Eh'.	

IP2_S Register (Bank = 2F, Sub-Bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '2F10h'.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '2F10h'.	
09h (2F13h)	**REG2F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	-	4:0	Reserved.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP	6	Cb/Cr swap for 444 to 422.	
	-	5	Reserved.	
	YDELAY_EN	4	Y delay enable.	
	YCDELAY_STEP[3:0]	3:0	Y/C delay pipe step.	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:4	Reserved.	
	PRE_ALIGN_WIDTH[3:0]	3:0	Insert pixel number for mirror mode.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x44**	**Access : R/W**
	-	7	Reserved.	
	CTI_STEP[2:0]	6:4	CTI filter step.	
	-	3	Reserved.	
	CTI_LPF_COEF[2:0]	2:0	CTI low-pass filter coefficient.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_BAND_COEF[5:0]	5:0	CTI band-pass filter coefficient.	
2Dh	**REG2F5A**	**7:0**	**Default : 0x88**	**Access : R/W**

IP2_S Register (Bank = 2F, Sub-Bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F5Ah)	CTI_MEDIAN_EN	7	CTI median filter enable.	
	-	6:4	Reserved.	
	CTI_CORING_THRD[3:0]	3:0	CTI coring threshold.	
2Dh (2F5Bh)	**REG2F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN	7	CTI enable.	
	-	6:4	Reserved.	
	CTI_AUTO_NO_MED	3	CTI auto-turn off median mode.	
	-	2:0	Reserved.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x81**	**Access : R/W**
	IP2_STATUS_CLR	7	IP2 status clear.	
	-	6:1	Reserved.	
	DLAST_ALIGN_EN	0	Data last signal align with IPM fetch number.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IP2_FLOW_CTRL_EN	4	IP2 flow control enable.	
	FLOW_CTRL_VALUE[3:0]	3:0	IP2 flow control count.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VIN_CTRL_EN	4	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	3	IP2 VSD input line count number setting enable.	
	VSD_IN_NUM_USR[10:8]	2:0	See description of '2F6Ch'.	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (2F6Fh)	**REG2F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VOUT_CTRL_EN	4	IP2 VSD output line count control enable.	
	-	3	Reserved.	
	VSD_OUT_NUMBER[10:8]	2:0	See description of '2F6Eh'.	
3Dh (2F7Ah)	**REG2F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_LBUF_CNT[7:0]	7:0	IP2 line buffer max pixels count.	
3Dh	**REG2F7B**	**7:0**	**Default : 0x00**	**Access : RO**

IP2_S Register (Bank = 2F, Sub-Bank = 04)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F7Bh)	-	7:1	Reserved.	
	BW_NOT_ENOUGH	0	IP2 line buffer full.	
3Eh (2F7Ch)	**REG2F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (2F7Dh)	**REG2F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	READ_HSD_OUT_CNT[11:8]	3:0	See description of '2F7Ch'.	
3Fh (2F7Eh)	**REG2F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (2F7Fh)	**REG2F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	READ_VSD_OUT_CNT[10:8]	2:0	See description of '2F7Eh'.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_FQ_SEL[1:0]	1:0	CSC coefficient select.	

PNR_REG Register (Bank = 2F, Sub-Bank = 05)

PNR_REG Register (Bank = 2F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F1	7	Sub Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F1	6	Sub Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F1	5	Sub Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F1	4	Sub Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F1	3	Sub Window Post Noise Reduction for Y.	
	PNR_ENC_F1	2	Sub Window Post Noise Reduction for C.	
	RATIOYC_FB1[1:0]	1:0	Sub Window Motion Ratio.	
01h (2F03h)	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

PNR_REG Register (Bank = 2F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SEL_NEXT_FIELD_INV_F1	0	Sub Window select next field inverter for noc_sel.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:5	Reserved.	
	DITH_MODE_F1[1:0]	4:3	Sub Window PNR dither mode, 00: No process, 01: Truncate, 10: Rounding, 11: Dither.	
	PNR_BYPASS_F1	2	Sub Window PNR function bypass enable.	
	NR_EN_F1	1	Sub Window Post NR enable.	
	PCCS_EN_F1	0	Sub Window Post CCS enable.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F1[2:0]	7:5	Sub Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F1[2:0]	4:2	Sub Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F1	1	Sub Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F1	0	Sub Window user-defined Y motion threshold enable.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F1	6	Sub Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F1	5	Sub Window enable select max motion for c.	
	YMOT_MAX_SEL_F1	4	Sub Window enable select max motion for y.	
	CMOT_DIV_MODE_F1[1:0]	3:2	Sub Window C motion divide mode.	
	YMOT_DIV_MODE_F1[1:0]	1:0	Sub Window Y motion divide mode.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_FB2[1:0]	1:0	Main Window Motion Ratio.	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for noc_sel.	
12h	**REG2F24**	**7:0**	**Default : 0x18**	**Access : R/W**

PNR_REG Register (Bank = 2F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F24h)	-	7:5	Reserved.	
	DITH_MODE_F2[1:0]	4:3	Main Window PNR dither mode, 00: No process, 01: Truncate, 10: Rounding, 11: Dither.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for c.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window c motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window y motion divide mode.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLEY_15_0[7:0]	7:0	PNR Table Y.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLEY_15_0[15:8]	7:0	See description of '2F60h'.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x12**	**Access : R/W**
	PNR_TABLEY_31_16[7:0]	7:0	PNR Table Y.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY_31_16[15:8]	7:0	See description of '2F62h'.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY_47_32[7:0]	7:0	PNR Table Y.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY_47_32[15:8]	7:0	See description of '2F64h'.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY_63_48[7:0]	7:0	PNR Table Y.	
33h	**REG2F67**	**7:0**	**Default : 0x00**	**Access : R/W**

PNR_REG Register (Bank = 2F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F67h)	PNR_TABLEY_63_48[15:8]	7:0	See description of '2F66h'.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLEC_15_0[7:0]	7:0	PNR Table C.	
40h (2F81h)	**REG2F81**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLEC_15_0[15:8]	7:0	See description of '2F80h'.	
41h (2F82h)	**REG2F82**	**7:0**	**Default : 0x12**	**Access : R/W**
	PNR_TABLEC_31_16[7:0]	7:0	PNR Table C.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC_31_16[15:8]	7:0	See description of '2F82h'.	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC_47_32[7:0]	7:0	PNR Table C.	
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC_47_32[15:8]	7:0	See description of '2F84h'.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC_63_48[7:0]	7:0	PNR Table C.	
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC_63_48[15:8]	7:0	See description of '2F86h'.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLECCS_15_0[7:0]	7:0	PNR CCS Table, smooth_en, smooth_step, mv_gain.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x08**	**Access : R/W**
	PNR_TABLECCS_15_0[15:8]	7:0	See description of '2FA0h'.	
51h (2FA2h)	**REG2FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLECCS_31_16[7:0]	7:0	PNR CCS Table, mv_offset, ev_gain_cc, ev_weight_cc.	
51h (2FA3h)	**REG2FA3**	**7:0**	**Default : 0x86**	**Access : R/W**
	PNR_TABLECCS_31_16[15:8]	7:0	See description of '2FA2h'.	
52h (2FA4h)	**REG2FA4**	**7:0**	**Default : 0x0A**	**Access : R/W**
	PNR_TABLECCS_47_32[7:0]	7:0	PNR CCS Table, pre_weight_c, pre_weight_y.	
52h (2FA5h)	**REG2FA5**	**7:0**	**Default : 0x0A**	**Access : R/W**
	PNR_TABLECCS_47_32[15:8]	7:0	See description of '2FA4h'.	
53h (2FA6h)	**REG2FA6**	**7:0**	**Default : 0x03**	**Access : R/W**
	PNR_TABLECCS_63_48[7:0]	7:0	PNR CCS Table, post_weight_c, post_weight_y.	
53h (2FA7h)	**REG2FA7**	**7:0**	**Default : 0x04**	**Access : R/W**
	PNR_TABLECCS_63_48[15:8]	7:0	See description of '2FA6h'.	

PNR_REG Register (Bank = 2F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
54h (2FA8h)	**REG2FA8**	**7:0**	**Default : 0x08**	**Access : R/W**
	PNR_TABLECCS_79_64[7:0]	7:0	PNR CCS Table, y_ev_weight_y, y_ev_offset_y.	
54h (2FA9h)	**REG2FA9**	**7:0**	**Default : 0x20**	**Access : R/W**
	PNR_TABLECCS_79_64[15:8]	7:0	See description of '2FA8h'.	
55h (2FAAh)	**REG2FAA**	**7:0**	**Default : 0x08**	**Access : R/W**
	PNR_TABLECCS_95_80[7:0]	7:0	PNR CCS Table, y_ev_weight_c, y_ev_offset_c.	
55h (2FABh)	**REG2FAB**	**7:0**	**Default : 0x20**	**Access : R/W**
	PNR_TABLECCS_95_80[15:8]	7:0	See description of '2FAAh'.	
56h (2FACh)	**REG2FAC**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	PNR_TABLECCS_99_96[3:0]	3:0	PNR CCS Table, ev_weight_rc.	
57h (2FAEh)	**REG2FAE**	**7:0**	**Default : 0x0C**	**Access : R/W**
	PCCS_CORING_Y[7:0]	7:0	PCCS coring Y.	
57h (2FAFh)	**REG2FAF**	**7:0**	**Default : 0x0C**	**Access : R/W**
	PCCS_CORING_C[7:0]	7:0	PCCS coring C.	
60h (2FC0h)	**REG2FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE_15_0[7:0]	7:0	PCCS Table.	
60h (2FC1h)	**REG2FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE_15_0[15:8]	7:0	See description of '2FC0h'.	
61h (2FC2h)	**REG2FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE_31_16[7:0]	7:0	PCCS Table.	
61h (2FC3h)	**REG2FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE_31_16[15:8]	7:0	See description of '2FC2h'.	
62h (2FC4h)	**REG2FC4**	**7:0**	**Default : 0x31**	**Access : R/W**
	PCCS_TABLE_47_32[7:0]	7:0	PCCS Table.	
62h (2FC5h)	**REG2FC5**	**7:0**	**Default : 0x75**	**Access : R/W**
	PCCS_TABLE_47_32[15:8]	7:0	See description of '2FC4h'.	
63h (2FC6h)	**REG2FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE_63_48[7:0]	7:0	PCCS Table.	
63h (2FC7h)	**REG2FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	PCCS_TABLE_63_48[15:8]	7:0	See description of '2FC6h'.	

DNR_REG Register (Bank = 2F, Sub-Bank = 06)

DNR_REG Register (Bank = 2F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	F1_MR_SOURCE_NRY	4	F1 Motion Source Cur Select. 0: Cur non-NR. 1: Cur after NR.	
	-	3	Reserved.	
	F1_DNR_TABLE_USER_EN	2	F1 DNR USE USER TABLE.	
	F1_DNR_CORE_EN	1	F1 DNR CORE FUNCTION EN.	
	F1_DNR_EN	0	F1 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
01h	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**

DNR_REG Register (Bank = 2F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F03h)	F1_LUT_SOURCE_C[1:0]	7:6	F1 DNR Table C source select. x1: From Y-diff. 10: From MED. 00: From C-diff.	
	F1_LUT_SOURCE_Y[1:0]	5:4	F1 DNR Table Y source select. x1: From C-diff. 10: From MED. 00: From Y-diff.	
	F1_DNR_TABLEC_LSB_EN	3	F1 DNR Table C LSB Mapping EN.	
	F1_DNR_TABLEY_LSB_EN	2	F1 DNR Table Y LSB Mapping EN.	
	F1_NR_TABLE_SEL_C	1	F1 DNR Table C Mapping Select. 0: Non-linear. 1: Linear.	
	F1_NR_TABLE_SEL_Y	0	F1 DNR Table Y Mapping Select. 0: Non-linear. 1: Linear.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_DITHER_CTRL[7:0]	7:0	F1_DNR_DITHER_CTRL. [2]: Previous lsb cat 2 bit for Y. [3]: Previous lsb cat 2 bit for C. [4]: Previous lsb cat current lsb for Y. [5]: Previous lsb cat current lsb for C. [10]: Previous lsb cat 2 dither bit for Y. [11]: Previous lsb cat 2 dither bit for C.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_DITHER_CTRL[15:8]	7:0	See description of '2F08h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	F1_NR_ROUND_BIT_C	5	Set C_ROUND describe as above.	
	F1_NR_ROUND_BIT_Y	4	Set Y_ROUND describe as above.	
	F1_ROUND_MODE_C[1:0]	3:2	F1 DNR C blend rounding select. 00: Add {C_ROUND,0}. 01: Add {dither.0}. 10: Add frame-base dither. 11: Add {dither[1:0]}.	

DNR_REG Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
	F1_ROUND_MODE_Y[1:0]	1:0	F1 DNR Y blend rounding select. 00: Add {Y_ROUND,0}. 01: Add {dither.0}. 10: Add frame-base dither. 11: Add {dither[1:0]}.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F1_MAX_MOT_ENABLE_C	3	F1_MAX_MOT_ENABLE_C.	
	F1_MAX_MOT_ENABLE_Y	2	F1_MAX_MOT_ENABLE_Y.	
	F1_DNR_FILTER_EN_C	1	F1_DNR_FILTER_EN_C.	
	F1_DNR_FILTER_EN_Y	0	F1_DNR_FILTER_EN_Y.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_FILTER_DIV0_C[2:0]	7:5	F1_DNR_FILTER_DIV0_C.	
	F1_DNR_FILTER_DIV0_Y[2:0]	4:2	F1_DNR_FILTER_DIV0_Y.	
	F1_DNR_FILTER_SIGN_C	1	F1_DNR_FILTER_SIGN_C.	
	F1_DNR_FILTER_SIGN_Y	0	F1_DNR_FILTER_SIGN_Y.	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_FILTER_MODE_C[1:0]	7:6	F1_DNR_FILTER_MODE_C.	
	F1_DNR_FILTER_MODE_Y[1:0]	5:4	F1_DNR_FILTER_MODE_Y.	
	F1_DNR_FILTER_DIV1_C[1:0]	3:2	F1_DNR_FILTER_DIV1_C.	
	F1_DNR_FILTER_DIV1_Y[1:0]	1:0	F1_DNR_FILTER_DIV1_Y.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	F2_MR_SOURCE_NRY	4	F2 Motion Source Cur Select. 0: Cur after NR. 1: Cur non-NR.	
		3:2	Reserved.	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION EN.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_LUT_SOURCE_C[1:0]	7:6	F2 DNR Table C source select. x1: From Y-diff. 10: From MED. 00: From C-diff.	

DNR_REG Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description
	F2_LUT_SOURCE_Y[1:0]	5:4	F2 DNR Table Y source select. x1: From C-diff. 10: From MED. 00: From Y-diff.
	F2_DNR_TABLEC_LSB_EN	3	F2 DNR Table C LSB Mapping EN.
	F2_DNR_TABLEY_LSB_EN	2	F2 DNR Table Y LSB Mapping EN.
	F2_NR_TABLE_SEL_C	1	F2 DNR Table C Mapping Select. 0: Non-linear. 1: Linear.
	F2_NR_TABLE_SEL_Y	0	F2 DNR Table Y Mapping Select. 0: Non-linear. 1: Linear.
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:3	Reserved.
	F2_SNR_METHOD_SEL	2	Reserved.
	F2_SNR_MD_MODE_EN	1	F2 SNR Motion Mode EN.
	F2_SNR_EN	0	F2 SNR FUNCTION EN.
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:6	Reserved.
	F2_NR_ROUND_BIT_C	5	Set C_ROUND described as above.
	F2_NR_ROUND_BIT_Y	4	Set Y_ROUND described as above.
	F2_ROUND_MODE_C[1:0]	3:2	F2 DNR C blend rounding select. 00: Add {C_ROUND,0}. 01: Add {dither.0}. 10: Add frame-base dither. 11: Add {dither[1:0]}.
	F2_ROUND_MODE_Y[1:0]	1:0	F2 DNR Y blend rounding select. 00: Add {Y_ROUND,0}. 01: Add {dither.0}. 10: Add frame-base dither. 11: Add {dither[1:0]}.
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	F2_MAX_MOT_ENABLE_C	3	F2_MAX_MOT_ENABLE_C.
	F2_MAX_MOT_ENABLE_Y	2	F2_MAX_MOT_ENABLE_Y.
	F2_DNR_FILTER_EN_C	1	F2_DNR_FILTER_EN_C.

DNR_REG Register (Bank = 2F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F2_DNR_FILTER_EN_Y	0	F2_DNR_FILTER_EN_Y.	
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_DIV0_C[2:0]	7:5	F2_DNR_FILTER_DIV0_C.	
	F2_DNR_FILTER_DIV0_Y[2:0]	4:2	F2_DNR_FILTER_DIV0_Y.	
	F2_DNR_FILTER_SIGN_C	1	F2_DNR_FILTER_SIGN_C.	
	F2_DNR_FILTER_SIGN_Y	0	F2_DNR_FILTER_SIGN_Y.	
27h (2F4Fh)	**REG2F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_MODE_C[1:0]	7:6	F2_DNR_FILTER_MODE_C.	
	F2_DNR_FILTER_MODE_Y[1:0]	5:4	F2_DNR_FILTER_MODE_Y.	
	F2_DNR_FILTER_DIV1_C[1:0]	3:2	F2_DNR_FILTER_DIV1_C.	
	F2_DNR_FILTER_DIV1_Y[1:0]	1:0	F2_DNR_FILTER_DIV1_Y.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x08**	**Access : R/W**
	F2_SHARP_LEVEL[7:0]	7:0	F2 SNR sharpness level.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	F2_POW_NUM[3:0]	3:0	F2 SNR power number.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_SNR_MDIFF_WT[2:0]	2:0	F2 MED motion different shift.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0xBD**	**Access : R/W**
	F1_DNR_TABLEY_0[7:0]	7:0	F1 DNR TABLEY_0.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x79**	**Access : R/W**
	F1_DNR_TABLEY_0[15:8]	7:0	See description of '2F60h'.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x56**	**Access : R/W**
	F1_DNR_TABLEY_1[7:0]	7:0	F1 DNR TABLEY_1.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x34**	**Access : R/W**
	F1_DNR_TABLEY_1[15:8]	7:0	See description of '2F62h'.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x12**	**Access : R/W**
	F1_DNR_TABLEY_2[7:0]	7:0	F1 DNR TABLEY_2.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_2[15:8]	7:0	See description of '2F64h'.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_3[7:0]	7:0	F1 DNR TABLEY_3.	

DNR_REG Register (Bank = 2F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
33h (2F67h)	**REG2F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEY_3[15:8]	7:0	See description of '2F66h'.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0xBD**	**Access : R/W**
	F1_DNR_TABLEC_0[7:0]	7:0	F1 DNR TABLEC_0.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x79**	**Access : R/W**
	F1_DNR_TABLEC_0[15:8]	7:0	See description of '2F68h'.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x56**	**Access : R/W**
	F1_DNR_TABLEC_1[7:0]	7:0	F1 DNR TABLEC_1.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0x34**	**Access : R/W**
	F1_DNR_TABLEC_1[15:8]	7:0	See description of '2F6Ah'.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x12**	**Access : R/W**
	F1_DNR_TABLEC_2[7:0]	7:0	F1 DNR TABLEC_2.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_2[15:8]	7:0	See description of '2F6Ch'.	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_3[7:0]	7:0	F1 DNR TABLEC_3.	
37h (2F6Fh)	**REG2F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F1_DNR_TABLEC_3[15:8]	7:0	See description of '2F6Eh'.	
38h (2F70h)	**REG2F70**	**7:0**	**Default : 0x70**	**Access : R/W**
	F1_DNR_TABLEY_LSB[7:0]	7:0	F1 DNR TABLEY_LSB.	
38h (2F71h)	**REG2F71**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	F1_DNR_TABLEY_LSB[11:8]	3:0	See description of '2F70h'.	
39h (2F72h)	**REG2F72**	**7:0**	**Default : 0x70**	**Access : R/W**
	F1_DNR_TABLEC_LSB[7:0]	7:0	F1 DNR TABLEC_LSB.	
39h (2F73h)	**REG2F73**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	F1_DNR_TABLEC_LSB[11:8]	3:0	See description of '2F72h'.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (2F81h)	**REG2F81**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '2F80h'.	
41h	**REG2F82**	**7:0**	**Default : 0x56**	**Access : R/W**

DNR_REG Register (Bank = 2F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F82h)	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '2F82h'.	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '2F84h'.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '2F86h'.	
44h (2F88h)	**REG2F88**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (2F89h)	**REG2F89**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '2F88h'.	
45h (2F8Ah)	**REG2F8A**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h (2F8Bh)	**REG2F8B**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEC_1[15:8]	7:0	See description of '2F8Ah'.	
46h (2F8Ch)	**REG2F8C**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (2F8Dh)	**REG2F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '2F8Ch'.	
47h (2F8Eh)	**REG2F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (2F8Fh)	**REG2F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '2F8Eh'.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x70**	**Access : R/W**
	DNR_TABLEY_LSB[7:0]	7:0	DNR TABLEY_LSB.	
48h (2F91h)	**REG2F91**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	DNR_TABLEY_LSB[11:8]	3:0	See description of '2F90h'.	
49h	**REG2F92**	**7:0**	**Default : 0x70**	**Access : R/W**

DNR_REG Register (Bank = 2F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F92h)	DNR_TABLEC_LSB[7:0]	7:0	DNR TABLEC_LSB.	
49h (2F93h)	**REG2F93**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:4	Reserved.	
	DNR_TABLEC_LSB[11:8]	3:0	See description of '2F92h'.	
78h (2FF0h)	**REG2FF0**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HCNT_F1[7:0]	7:0	F1 hcnt for debug.	
78h (2FF1h)	**REG2FF1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	STATUS_HCNT_F1[10:8]	2:0	See description of '2FF0h'.	
79h (2FF2h)	**REG2FF2**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_VCNT_F1[7:0]	7:0	F1 vcnt for debug.	
79h (2FF3h)	**REG2FF3**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	STATUS_CLR_F1	7	F1 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F1[10:8]	2:0	See description of '2FF2h'.	
7Ah (2FF4h)	**REG2FF4**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HCNT_F2[7:0]	7:0	F2 hcnt for debug.	
7Ah (2FF5h)	**REG2FF5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	STATUS_HCNT_F2[10:8]	2:0	See description of '2FF4h'.	
7Bh (2FF6h)	**REG2FF6**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_VCNT_F2[7:0]	7:0	F2 vcnt for debug.	
7Bh (2FF7h)	**REG2FF7**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	STATUS_CLR_F2	7	F2 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F2[10:8]	2:0	See description of '2FF6h'.	

SNR Register (Bank = 2F, Sub-Bank = 0C)

SNR Register (Bank = 2F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SNR_STD_MOTION_RATIO_EN_F1	6	De-blocking and SNR active threshold motion ratio enable F1.	
	SNR_MOTION_RATIO_EN_F1	5	De-blocking and SNR motion ratio enable F1.	
	SNR_EN_F1	4	SNR enable F1.	
	-	3	Reserved.	
	SNR_STD_MOTION_RATIO_EN_F2	2	De-blocking and SNR active threshold motion ratio enable F2.	
	SNR_MOTION_RATIO_EN_F2	1	De-blocking and SNR motion ratio enable F2.	
	SNR_EN_F2	0	SNR enable F2.	

SNR Register (Bank = 2F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SNR_STD_LOW_THRD[7:0]	7:0	SNR active threshold.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x48**	**Access : R/W**
	SNR_ALPHA_STEP[2:0]	7:5	SNR alpha step.	
	-	4	Reserved.	
	SNR_STRENGTH_GAIN_F2[3:0]	3:0	SNR strength F2.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	SNR_STRENGTH_GAIN_F1[3:0]	3:0	SNR strength F1.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0xCF**	**Access : R/W**
	SNR_TABLE_01[7:0]	7:0	SNR LUT_01.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x69**	**Access : R/W**
	SNR_TABLE_23[7:0]	7:0	SNR LUT_23.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x24**	**Access : R/W**
	SNR_TABLE_45[7:0]	7:0	SNR LUT_45.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0x01**	**Access : R/W**
	SNR_TABLE_67[7:0]	7:0	SNR LUT_67.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_89[7:0]	7:0	SNR LUT_89.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_AB[7:0]	7:0	SNR LUT_AB.	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_CD[7:0]	7:0	SNR LUT_CD.	
37h (2F6Fh)	**REG2F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_EF[7:0]	7:0	SNR LUT_EF.	
58h (2FB0h)	**REG2FB0**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_01[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_01.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_23[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_23.	
59h (2FB2h)	**REG2FB2**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_45[7:0]	7:0	De-blocking and SNR active threshold motion ratio	

SNR Register (Bank = 2F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			LUT_45.	
59h (2FB3h)	**REG2FB3**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_67[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_67.	
5Ah (2FB4h)	**REG2FB4**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_89[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_89.	
5Ah (2FB5h)	**REG2FB5**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_AB[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_AB.	
5Bh (2FB6h)	**REG2FB6**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_CD[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_CD.	
5Bh (2FB7h)	**REG2FB7**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_STD_LOW_MOTION_TABLE_EF[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_EF.	
5Ch (2FB8h)	**REG2FB8**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_MOTION_TABLE_01[7:0]	7:0	De-blocking and SNR motion ratio LUT_01.	
5Ch (2FB9h)	**REG2FB9**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_MOTION_TABLE_23[7:0]	7:0	De-blocking and SNR motion ratio LUT_23.	
5Dh (2FBAh)	**REG2FBA**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_MOTION_TABLE_45[7:0]	7:0	De-blocking and SNRmotion ratio LUT_45.	
5Dh (2FBBh)	**REG2FBB**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_MOTION_TABLE_67[7:0]	7:0	De-blocking and SNR motion ratio LUT_67.	
5Eh (2FBCh)	**REG2FBC**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_MOTION_TABLE_89[7:0]	7:0	De-blocking and SNR motion ratio LUT_89.	
5Eh (2FBDh)	**REG2FBD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_MOTION_TABLE_AB[7:0]	7:0	De-blocking and SNR motion ratio LUT_AB.	
5Fh (2FBEh)	**REG2FBE**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_MOTION_TABLE_CD[7:0]	7:0	De-blocking and SNR motion ratio LUT_CD.	
5Fh (2FBFh)	**REG2FBF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_MOTION_TABLE_EF[7:0]	7:0	De-blocking and SNR motion ratio LUT_EF.	
70h ~ 70h (2FE0h ~	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SNR Register (Bank = 2F, Sub-Bank = 0C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
2FE1h)			

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:1	Reserved.	
	MW_BD_REG_EN	0	Main Window Border Register Enable. 0: Sub window Border register enable. 1: Main window Border register Enable.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO_BO[3:0]	7:4	Main window border outside height of Left side.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.	
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.	
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.	
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.	
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.	
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.	
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.	
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.	
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.	
	-	3:2	Reserved.	
	181FWINSEL[1:0]	1:0	18h~1Fh Display Window Select. 00: 1st window. 01: 2nd window.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: 3rd window. 11: 4th window.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST[7:0]	7:0	Sub window Horizontal Start.	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	See description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	See description of '2F10h'.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST[7:0]	7:0	Sub window Vertical Star.	
09h (2F13h)	**REG2F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	See description of '2F12h'.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND[7:0]	7:0	Sub window Vertical End.	
0Ah (2F15h)	**REG2F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND[11:8]	3:0	See description of '2F14h'.	
0Bh (2F16h)	**REG2F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.	
0Bh (2F17h)	**REG2F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	See description of '2F16h'.	
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.	
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	See description of '2F18h'.	
0Dh	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
(2F1Ah)	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.	
0Dh (2F1Bh)	**REG2F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	See description of '2F1Ah'.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.	
0Eh (2F1Dh)	**REG2F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	See description of '2F1Ch'.	
0Fh (2F1Eh)	**REG2F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.	
0Fh (2F1Fh)	**REG2F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	See description of '2F1Eh'.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	See description of '2F20h'.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_3RD[11:8]	3:0	See description of '2F22h'.	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	See description of '2F24h'.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	S_HDEST_4TH[11:8]	3:0	See description of '2F26h'.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_4TH[11:8]	3:0	See description of '2F28h'.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	See description of '2F2Ah'.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_4TH[11:8]	3:0	See description of '2F2Ch'.	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWBCOL[7:0]	7:0	Sub Window Border Color.	
17h (2F2Fh)	**REG2F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HBC_GAIN[3:0]	7:4	HBC gain for sub window.	
	S_HBC_EN	3	HBC function enable for sub window.	
	S_HBC_ROUNDING	2	HBC rounding enable for sub window.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	See description of '2F36h'.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (2F39h)	**REG2F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[15:8]	7:0	See description of '2F38h'.	
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '2F3Ah'.	
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '2F3Ch'.	
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '2F3Eh'.	
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
20h (2F41h)	**REG2F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CM21[12:8]	4:0	See description of '2F40h'.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '2F42h'.	
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
22h (2F45h)	**REG2F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '2F44h'.	
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '2F46h'.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
24h (2F49h)	**REG2F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '2F48h'.	
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
25h (2F4Bh)	**REG2F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '2F4Ah'.	
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	-	3	Reserved.
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.
26h (2F4Dh)	**REG2F4D**	**7:0**	**Default : 0x00** **Access : R/W**
	SMEN	7	SVM Main window Enable.
	SMTE	6	SVM Main window Tap Enable.
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.
	SSWEN	3	SVM Sub window Enable.
	SSWETE	2	SVM Sub window Tap Enable.
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x00** **Access : R/W**
	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.
	SVMBYS[1:0]	5:4	SVM Bypass Y Select. 0x: SMV data. 10: Original Y data. 11: Y with tap filter.
	SCORING[3:0]	3:0	SVM Coring.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
27h (2F4Fh)	**REG2F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SVMLMT[7:0]	7:0	SVM Limit.	
28h (2F50h)	**REG2F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM Main window Step.	
	SMGAIN[3:0]	3:0	SVM Main window Gain.	
28h (2F51h)	**REG2F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM Sub window Step.	
	SWGAIN[3:0]	3:0	SVM Sub window Gain.	
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM Pipe Adjust.	
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.	
29h (2F53h)	**REG2F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SVM_SEP_DLY	7	SVM Separate Delay Enable.	
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.	
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	C1080I	7	1080i mode. 0: Follow DE. 1: Follow HSYNC.	
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.	
	IPFI	5	To Pad Field Invert enable.	
	I1440	4	Interlace 1440 mode. This bit works at frame SBPCM= 0. 0: Disable, horizontal valid pixel = 720; SVM support. 1: Enable, horizontal valid pixel = 1440; does not	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			support SVM.	
	IRDEN	3	Random 10 bit DAC Enable.	
	IHSRE	2	HSYNC Shift control. 0: Shift left. 1: Shift right.	
	IOFI	1	Interlace Output Field Invert.	
	IOEN	0	Interlace Output Enable.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.	
	-	3:0	Reserved.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_FINV	7	IP Field Inverse.	
	IP_ITLC	6	IP Interlace.	
	SIM	5	Single Interlace Mode. 0: Disable. 1: Enable.	
	LPM	4	LVDS 10 bit Mode. 0: Disable. 1: Enable.	
	BES[1:0]	3:2	Border Extend for SVM.	
	OES[1:0]	1:0	OSD Extend for SVM.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSOFFS[7:0]	7:0	HSYNC Shift Offset.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.	
	RESERVED[1:0]	6:5	RESERVED.	
	-	4	Reserved.	
	HSOFFS[11:8]	3:0	See description of '2F58h'.	
	-	-	Reserved.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_BRI_OFFSET[7:0]	7:0	Offset for R data.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_EN	7	Brightness enable (after gamma).	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	CON_EN	6	Contrast enable (after gamma).	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	See description of '2F60h'.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	G_BRI_OFFSET[10:8]	2:0	See description of '2F62h'.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	See description of '2F64h'.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	
33h (2F67h)	**REG2F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	See description of '2F66h'.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	See description of '2F68h'.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	See description of '2F6Ah'.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_R[7:0]	7:0	Brightness offset (bri_function) for main window R.	
36h	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F6Dh)	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	See description of '2F6Ch'.	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_G[7:0]	7:0	Brightness offset (bri_function) for main window G.	
37h (2F6Fh)	**REG2F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_G[10:8]	2:0	See description of '2F6Eh'.	
38h (2F70h)	**REG2F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_B[7:0]	7:0	Brightness offset (bri_function) for main window B.	
38h (2F71h)	**REG2F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	See description of '2F70h'.	
39h (2F72h)	**REG2F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_R[7:0]	7:0	Brightness offset (bri_function) for sub window R.	
39h (2F73h)	**REG2F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	See description of '2F72h'.	
3Ah (2F74h)	**REG2F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_G[7:0]	7:0	Brightness offset (bri_function) for sub window G.	
3Ah (2F75h)	**REG2F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	See description of '2F74h'.	
3Bh (2F76h)	**REG2F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_B[7:0]	7:0	Brightness offset (bri_function) for sub window B.	
3Bh (2F77h)	**REG2F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	See description of '2F76h'.	
3Ch (2F78h)	**REG2F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE0[7:0]	7:0	Check value for auto mload base0 R channel.	
3Ch	**REG2F79**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F79h)	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE0[11:8]	3:0	See description of '2F78h'.	
3Dh (2F7Ah)	**REG2F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE1[7:0]	7:0	Check value for auto mload base1 R channel.	
3Dh (2F7Bh)	**REG2F7B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE1[11:8]	3:0	See description of '2F7Ah'.	
3Eh (2F7Ch)	**REG2F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE0[7:0]	7:0	Check value for auto mload base0 G channel.	
3Eh (2F7Dh)	**REG2F7D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE0[11:8]	3:0	See description of '2F7Ch'.	
3Fh (2F7Eh)	**REG2F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE1[7:0]	7:0	Check value for auto mload base1 G channel.	
3Fh (2F7Fh)	**REG2F7F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_1	7	Base1 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE1[11:8]	3:0	See description of '2F7Eh'.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE0[7:0]	7:0	Check value for auto mload base0 B channel.	
40h (2F81h)	**REG2F81**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE0[11:8]	3:0	See description of '2F80h'.	
41h (2F82h)	**REG2F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE1[7:0]	7:0	Check value for auto mload base1 B channel.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE1[11:8]	3:0	See description of '2F82h'.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
46h (2F8Ch)	**REG2F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAP_STAGE[3:0]	7:4	Capture stage selection. 0: VOP2_dp input data. 1: BRI output. 2: HBC output. 3: CON_BRI output. 4: FWC output. 5: Gamma output. 6: Noise dither output.	
	-	3:0	Reserved.	
46h (2F8Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
47h (2F8Eh)	**REG2F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.	
47h (2F8Fh)	**REG2F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '2F8Eh'.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.	
48h (2F91h)	**REG2F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '2F90h'.	
49h (2F92h)	**REG2F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.	
49h (2F93h)	**REG2F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '2F92h'.	
4Ah (2F94h)	**REG2F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.	
4Ah (2F95h)	**REG2F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_CON_GAIN[11:8]	3:0	See description of '2F94h'.	
4Bh (2F96h)	**REG2F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Bh (2F97h)	**REG2F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_CON_GAIN[11:8]	3:0	See description of '2F96h'.	
4Ch (2F98h)	**REG2F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.	
4Ch (2F99h)	**REG2F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_CON_GAIN[11:8]	3:0	See description of '2F98h'.	
4Dh (2F9Ah)	**REG2F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.	
4Dh (2F9Bh)	**REG2F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '2F9Ah'.	
4Eh (2F9Ch)	**REG2F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.	
4Eh (2F9Dh)	**REG2F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '2F9Ch'.	
4Fh (2F9Eh)	**REG2F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.	
4Fh (2F9Fh)	**REG2F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '2F9Eh'.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '2FA0h'.	
51h (2FA2h)	**REG2FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.	
51h (2FA3h)	**REG2FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '2FA2h'.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (2FA4h)	**REG2FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.	
52h (2FA5h)	**REG2FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '2FA4h'.	
53h (2FA6h)	**REG2FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.	
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma CON_BRI.	
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.	
53h (2FA7h)	**REG2FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.	
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.	
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.	
54h (2FA8h)	**REG2FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.	
54h (2FA9h)	**REG2FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FREEZ_VCNT_VALUE[10:8]	2:0	See description of '2FA8h'.	
55h (2FAAh)	**REG2FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when NEW_LOCK_POINT is set high.	
55h (2FABh)	**REG2FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LOCK_VCNT_VALUE[10:8]	2:0	See description of '2FAAh'.	
56h	**REG2FAC**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FACh)	-	7:6	Reserved.	
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.	
	OTUPUT_FIELD_INV	4	Invert field for output reference signal.	
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.	
	IVS_SEL	2	Select insert_end point as input reference for frame PLL.	
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.	
	INPUT_FREEZ	0	V-counter freeze enable.	
56h (2FADh)	**REG2FAD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VCNT_FREEZ_REGION	7	In V-counter freeze status.	
	-	6:2	Reserved.	
	IVS_CNT[9:8]	1:0	Frame number for input reference generate.	
57h (2FAEh)	**REG2FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for CCIR656 format.	
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for CCIR656 format.	
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.	
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.	
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.	
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.	
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.	
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.	
57h (2FAFh)	**REG2FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
		7	Reserved.	
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.	
	NOISE_DITH_EN	5	Noise dither enable.	
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.	
	CAP_EN	3	Capture image to IP enable.	
	-	2:0	Reserved.	
58h (2FB0h)	**REG2FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. MAIN_R_MIN_SIGN = 1:.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			MAIN_R_MIN = -MAIN_R_MIN_LIMIT. MAIN_R_MIN_SIGN = 0:. MAIN_R_MIN = MAIN_R_MIN_LIMIT.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '2FB0h'.	
59h (2FB2h)	**REG2FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
59h (2FB3h)	**REG2FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '2FB2h'.	
5Ah (2FB4h)	**REG2FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. MAIN_G_MIN_SIGN = 1:. MAIN_G_MIN = -MAIN_G_MIN_LIMIT. MAIN_G_MIN_SIGN = 0:. MAIN_G_MIN = MAIN_G_MIN_LIMIT.	
5Ah (2FB5h)	**REG2FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '2FB4h'.	
5Bh (2FB6h)	**REG2FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Bh (2FB7h)	**REG2FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '2FB6h'.	
5Ch (2FB8h)	**REG2FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. MAIN_B_MIN_SIGN = 1:. MAIN_R_MIN = -MAIN_B_MIN_LIMIT. MAIN_B_MIN_SIGN = 0:. MAIN_R_MIN = MAIN_B_MIN_LIMIT.	
5Ch (2FB9h)	**REG2FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '2FB8h'.	
5Dh	**REG2FBA**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FBAh)	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Dh (2FBBh)	**REG2FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '2FBAh'.	
5Eh (2FBCh)	**REG2FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value. S.12 format sign bit is bit-12. SUB_R_MIN_SIGN = 1: MAIN_R_MIN = SUB_R_MIN_LIMIT. SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.	
5Eh (2FBDh)	**REG2FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '2FBCh'.	
5Fh (2FBEh)	**REG2FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
5Fh (2FBFh)	**REG2FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '2FBEh'.	
60h (2FC0h)	**REG2FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. SUB_G_MIN_SIGN = 1:. MAIN_G_MIN = -SUB_G_MIN_LIMIT. SUB_G_MIN_SIGN = 0:. MAIN_G_MIN = SUB_G_MIN_LIMIT.	
60h (2FC1h)	**REG2FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '2FC0h'.	
61h (2FC2h)	**REG2FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
61h (2FC3h)	**REG2FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '2FC2h'.	
62h	**REG2FC4**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FC4h)	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. SUB_B_MIN_SIGN = 1:. MAIN_R_MIN = -SUB_B_MIN_LIMIT. SUB_B_MIN_SIGN = 0:. MAIN_R_MIN = SUB_B_MIN_LIMIT.	
62h (2FC5h)	**REG2FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '2FC4h'.	
63h (2FC6h)	**REG2FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
63h (2FC7h)	**REG2FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '2FC6h'.	
6Ch (2FD8h)	**REG2FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[7:0]	7:0	New add function for RGB_compression.	
6Ch (2FD9h)	**REG2FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[15:8]	7:0	See description of '2FD8h'.	
70h (2FE0h)	**REG2FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FWC_SUB_EN	4	FWC_SUB_EN	
	-	3:2	Reserved.	
	FWC_DITHER_EN	1	FWC_DITHER_EN	
	FWC_MAIN_EN	0	FWC_MAIN_EN	
70h (2FE1h)	**REG2FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:4	Reserved.	
	FWC_STRENGTH[3:0]	3:0	FWC_STRENGTH	
71h (2FE2h)	**REG2FE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FWC_SLOPE[5:0]	5:0	FWC_SLOPE	
71h (2FE3h)	**REG2FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	FWC_CTH[7:0]	7:0	FWC_CTH	
72h (2FE4h)	**REG2FE4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[7:0]	7:0	FWC_DELTA_R	
72h	**REG2FE5**	**7:0**	**Default : 0x80**	**Access : R/W**

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FE5h)	FWC_DELTA_R[15:8]	7:0	See description of '2FE4h'.	
73h (2FE6h)	**REG2FE6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[23:16]	7:0	See description of '2FE4h'.	
73h (2FE7h)	**REG2FE7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[31:24]	7:0	See description of '2FE4h'.	
74h (2FE8h)	**REG2FE8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[39:32]	7:0	See description of '2FE4h'.	
74h (2FE9h)	**REG2FE9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[47:40]	7:0	See description of '2FE4h'.	
75h (2FEAh)	**REG2FEA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[55:48]	7:0	See description of '2FE4h'.	
75h (2FEBh)	**REG2FEB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[63:56]	7:0	See description of '2FE4h'.	
76h (2FECh)	**REG2FEC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[71:64]	7:0	See description of '2FE4h'.	
76h (2FEDh)	**REG2FED**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[79:72]	7:0	See description of '2FE4h'.	
77h (2FEEh)	**REG2FEE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[87:80]	7:0	See description of '2FE4h'.	
77h (2FEFh)	**REG2FEF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[95:88]	7:0	See description of '2FE4h'.	
7Ah (2FF4h)	**REG2FF4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[7:0]	7:0	FWC_DELTA_B	
7Ah (2FF5h)	**REG2FF5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[15:8]	7:0	See description of '2FF4h'.	
7Bh (2FF6h)	**REG2FF6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[23:16]	7:0	See description of '2FF4h'.	
7Bh (2FF7h)	**REG2FF7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[31:24]	7:0	See description of '2FF4h'.	
7Ch (2FF8h)	**REG2FF8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[39:32]	7:0	See description of '2FF4h'.	
7Ch (2FF9h)	**REG2FF9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[47:40]	7:0	See description of '2FF4h'.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Dh (2FFAh)	**REG2FFA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[55:48]	7:0	See description of '2FF4h'.	
7Dh (2FFBh)	**REG2FFB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[63:56]	7:0	See description of '2FF4h'.	
7Eh (2FFCh)	**REG2FFC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[71:64]	7:0	See description of '2FF4h'.	
7Eh (2FFDh)	**REG2FFD**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[79:72]	7:0	See description of '2FF4h'.	
7Fh (2FFEh)	**REG2FFE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[87:80]	7:0	See description of '2FF4h'.	
7Fh (2FFFh)	**REG2FFF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[95:88]	7:0	See description of '2FF4h'.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND0[7:0]	7:0	20h: Recommended value (power on default value is 0).	
01h (2F03h)	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:1	Reserved.	
	DB_MASK	0	Double buffer register mask signal. The double buffer register is updated when DB_MASK and DB_LOAD.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSST[7:0]	7:0	Output VSYNC start (only useful when AOVS= 1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h - 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No Signal VSYNC. Registers 22h and 23h are used to define minimum H total.	
	VSST[10:8]	2:0	See description of '2F04h'.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOVS= 1). 304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.	
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	VSEND[10:8]	2:0	See description of '2F06h'.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHST[7:0]	7:0	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEHST[11:8]	3:0	See description of '2F08h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHEND[7:0]	7:0	Output DE Horizontal END. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEHEND[11:8]	3:0	See description of '2F0Ah'.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVST[7:0]	7:0	Output DE Vertical Start. 00: Default value.	
06h	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F0Dh)	VSTSEL	7	Vertical Start Select. 0: DEVST[10:0] is Output DE vertical start. 1: DEVST[10:0] is Scaling Image Window vertical start.	
	-	6:4	Reserved.	
	DEVST[11:8]	3:0	See description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVEND[7:0]	7:0	Output DE Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEVEND[11:8]	3:0	See description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start. 48h: Recommended value (power on default is 0).	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIHST[11:8]	3:0	See description of '2F10h'.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.	
09h (2F13h)	**REG2F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIHEND[11:8]	3:0	See description of '2F12h'.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVST[7:0]	7:0	Scaling Image window Vertical Start.	
0Ah (2F15h)	**REG2F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVST[11:8]	3:0	See description of '2F14h'.	
0Bh	**REG2F16**	**7:0**	**Default : 0x00**	**Access : R/W**

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
(2F16h)	SIVEND[7:0]	7:0	Scaling Image window Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.
0Bh (2F17h)	**REG2F17**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	SIVEND[11:8]	3:0	See description of '2F16h'.
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0x00** **Access : R/W**
	HDTOT[7:0]	7:0	Output Horizontal Total. 53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	HDTOT[11:8]	3:0	See description of '2F18h'.
0Dh (2F1Ah)	**REG2F1A**	**7:0**	**Default : 0x00** **Access : R/W**
	VDTOT[7:0]	7:0	Output Vertical Total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output.
0Dh (2F1Bh)	**REG2F1B**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:4	Reserved.
	VDTOT[11:8]	3:0	See description of '2F1Ah'.
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00** **Access : R/W**
	HSEND[7:0]	7:0	20h: Recommended value (power on default value is 0).
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x4C** **Access : R/W**
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 - 0x23).
	OUTM	6	Output Mode. 0: Mode 0. 1: Mode 1.
	HRSM	5	HSYNC Remove Mode. 0: Normal. 1: Remove HSYNC when GPOA (Bank 2 register0x62 - 0x6A) is low.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	VSGP	4	VSYNC use GPO9. 0: Disable. 1: Enable (using Bank 2 register 0x59 - 0x61 to define OVSYNC).
	EHTT	3	Even H Total. 0: Enable, Output H Total is always even pixels. 1: Disable, Output H Total is always odd pixels.
	MOD2	2	Mode 2. 0: Disable. 1: Enable.
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00** **Access : R/W**
	FPLLMD0	7	Frame PLL Mode 0.
	SL_TUNE_EN	6	Short line tune enable.
	AUTO_H_TOTAL_UPDATE_EN	5	Enable update AUTO_H_TOTAL value to H_TOTAL.
	-	4:2	Reserved.
	SSC_SHIFT	1	0: Enable. 1: Disable.
	CLKDIV2_POINT_SELECT	0	0: Original. 1: New.
11h (2F23h)	**-**	**7:0**	**Default : -** **Access : -**
	-	-	Reserved.
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x20** **Access : R/W**
	LCK_TH[7:0]	7:0	Frame PLL Lock Threshold.
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x08** **Access : R/W**
	LCK_TH[15:8]	7:0	See description of '2F24h'.
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x10** **Access : R/W**
	FTNF[7:0]	7:0	Frame Tune Number of Frame.
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x10** **Access : R/W**
	FTNS[3:0]	7:4	Tune Frame Number of Short-line tune.

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3	Reserved.	
	PIP_REG_EN	2	PIP Register Enable.	
	FPLL_REP_EN	1	Frame PLL Report Enable.	
	NOISY_GEN	0	Noise Generator.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT1[7:0]	7:0	Frame PLL Limit.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT0[7:0]	7:0	Frame PLL Limit.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT[7:0]	7:0	Frame PLL Limit.	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_LMT_OFST0[7:0]	7:0	Frame PLL Limit Offset low byte.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_LMT_OFST1[7:0]	7:0	Frame PLL Limit Offset high byte.	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0xF0**	**Access : R/W**
	M_HBC_GAIN[3:0]	7:4	Main window High brightness gain.	
	M_HBC_EN	3	Main window High brightness enable.	
	M_HBC_ROUNDING	2	Main window High brightness enable.	
	-	1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADEAD_EN	7	Ahead mode enable.	
	SWBLBK	6	Sub window Blue screen color. 0: Black color. 1: Blue color.	
	SWBLUE	5	Sub window Blue screen control. 0: Off. 1: On.	
	S_FMCLR_EN	4	Sub window frame color enable.	
	-	3	Reserved.	
	MBD_EN	2	Main window Border Enable.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MBLK	1	Main window Black screen control. 0: Off. 1: On.	
	NOSC_EN	0	No Signal Color Enable.	
19h (2F33h)	**REG2F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_R[7:0]	7:0	Frame Color - Red.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_G[7:0]	7:0	Frame Color - Green.	
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_B[7:0]	7:0	Frame Color - Blue.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x02**	**Access : R/W**
	DITHG[1:0]	7:6	Dither coefficient for G channel.	
	DITHB[1:0]	5:4	Dither coefficient for B channel.	
	SROT	3	Spatial coefficient Rotate. 0: Disable. 1: Enable.	
	TROT	2	Temporal coefficient Rotate. 0: Disable. 1: Enable.	
	OBN	1	Output Bits Number (used for 8/10-bit gamma). 0: 8-bit output. 1: 6-bit output (power on default value).	
	DITH	0	DITHer function. 0: Off. 1: On.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x2D**	**Access : R/W**
	TL[1:0]	7:6	Top - Left dither coefficient.	
	TR[1:0]	5:4	Top - Right dither coefficient.	
	BL[1:0]	3:2	Bottom - Left dither coefficient.	
	BR[1:0]	1:0	Bottom - Right dither coefficient.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_E_4_FRAME	7	Reset noise generator by frames enable.	
	NDMD	6	Noise Dithering Method.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.	
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.	
	DT3	3	Dither Type 2 control. 0: Disable dither type 2. 1: Enable dither type 2.	
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.	
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.	
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.	
1Ch (2F39h)	**REG2F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SHORT_1LINE_DISABLE	6	1: Disable. 0: Enable.	
	-	5	Reserved.	
	EGWT	4	Encode Gamma Write.	
	HTOTAL	3	H Total End 11.	
	HDE_END	2	HDE End 11.	
	HFDE_END	1	HFDE END 11.	
	OUTFRR_EN0	0	Output Free-run Enable.	
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0x03**	**Access : R/W**
	IVS_DIFF_THR[7:0]	7:0	Input vs Different Thresholds.	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x07**	**Access : R/W**
	TUNE_FIELD_IP	7	Select insert point of one field for VOP_DISP inset signal.	
	IVS_STB_THR[6:0]	6:0	Input vs Stable Thresholds.	
1Eh	**REG2F3C**	**7:0**	**Default : 0x00**	**Access : R/W**

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F3Ch)	LMT_ADD_NMB[7:0]	7:0	Limit adjust Number in ACC_FPLL mode.	
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_MD1	7	FPLL Mode 1.	
	FPLL_DIS	6	FPLL Stop.	
	ACC1_SEL[1:0]	5:4	Select modify numbers. 00: 3/4 diff numbers. 01: 1/2 diff numbers. Others: 1/4 diff numbers.	
	-	3	Reserved.	
	ADD_LINE_SEL	2	Select Add Line into frame or pixel into line.	
	CH_CH_MD1	1	ACC FPLL Mode 1.	
	CH_CH_MD0	0	ACC FPLL Mode 0.	
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IVS_PRD_NUM[7:0]	7:0	Count Number per Input v.s.	
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IVS_PRD_NUM[11:8]	3:0	See description of '2F3Eh'.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCPS	7	LVDS Channel Polarity Swap (P/N swap). 0: Disable. 1: Enable.	
	LCS	6	LVDS Channel Swap. 0: Disable. 1: Enable. When enabled in dual LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap, LVB0M/LVB3M swap, LVB0P/LVB3P swap, LVB1M/LVBCKM swap, LVB1P/LVBCKP swap. When enabled in single LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap.	
	MLXT0	5	MSB/LSB Exchange Type for 6/8/10-bit.	
	LTIM	4	LVDS TI Mode. 0: Normal. 1: TI Mode.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OMLX	3	Odd channel MSB/LSB Exchange. 0: Normal. 1: Exchange.	
	EMLX	2	Even channel MSB/LSB Exchange. 0: Normal. 1: Exchange.	
	ORBX	1	Odd channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.	
	ERBX	0	Even channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.	
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLXT1	7	MSB/LSB Exchange Type for 6/8/10-bit.	
	DOT	6	Differential Output Type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/Increased-swing RSDS.	
	WHTS	5	White Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	BLSK	4	Black Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	REVERSE	3	REVERSE luminosity. 0: Off. 1: On.	
	STO	2	Stagger Output (only used when DPO= 1). 0: Disable. 1: Enable.	
	DPX	1	A/B Port Swap (only used when DPO= 1). 0: Disable. 1: Enable.	
	DUAL_PIXEL_OUTPUT	0	Dual Pixel Output. 0: Single pixel. 1: Dual pixel.	
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AB_SWAP	5	LVDS AB Port Swap.	
	CKSEL[4:0]	4:0	Enable clock of internal control. 00h: TTL output. 11H: Single LVDS output. 13h: Dual LVDS output.	
22h (2F45h)	**REG2F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBLALL_SET	7	Frame buffer less all set.	
	PUT_REG_PTT1	6	Register overwrite 0 bit 1.	
	PDP10BIT	5	PDP 10 bits mode, support single 10 bit LVDS PDP.	
	TTL_LVDS	4	TTL LVDS mode, let single TTL and LVDS use same board.	
	BRGS	3	B port pixel R/G Swap. 0: Disable. 1: Enable.	
	ARGS	2	A port pixel R/G Swap. 0: Disable. 1: Enable.	
	BGBS	1	B port pixel G/B Swap. 0: Disable. 1: Enable.	
	AGBS	0	A port pixel G/B Swap. 0: Disable. 1: Enable.	
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCHBLEND	7	OSD Character Blending mode.	
	-	6	Reserved.	
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).	
	-	4	Reserved.	
	GATP	3	Gamma Automatically On/Off based on Auto Phase value. 0: Disable. 1: Enable.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0%% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	MNS_COL[7:0]	7:0	Main Window No Signal Color.	
24h (2F49h)	**REG2F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	MBCOL[7:0]	7:0	Main Window Border Color.	
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	SLOW_RAW_LIM[3:0]	6:3	Raw_threshold in FPLL_tune_slow.	
	SLOW_CNT_LIM[2:0]	2:0	Count threshold.	
25h (2F4Bh)	**REG2F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLOCK_DL_LN[2:0]	5:3	Delay line number in Flock mode.	
	FLOCK_AH_LN[2:0]	2:0	Ahead line in Flock mode.	
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
26h (2F4Dh)	**REG2F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '2F4Ch'.	
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
27h (2F4Fh)	**REG2F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '2F4Eh'.	
28h (2F50h)	**REG2F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
28h	**REG2F51**	**7:0**	**Default : 0x00**	**Access : R/W**

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F51h)	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '2F50h'.	
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
29h (2F53h)	**REG2F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '2F52h'.	
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '2F54h'.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '2F56h'.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '2F58h'.	
2Dh (2F5Ah)	**REG2F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
2Dh (2F5Bh)	**REG2F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '2F5Ah'.	
2Eh (2F5Ch)	**REG2F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
2Eh (2F5Dh)	**REG2F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '2F5Ch'.	
2Fh	**REG2F5E**	**7:0**	**Default : 0x00**	**Access : R/W**

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F5Eh)	-	7	Reserved.	
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: -128~127.	
	GRAN	1	Green Range. 0: 0~255.1: -128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: -128~127.	
2Fh (2F5Fh)	**REG2F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSFD	7	Sub window Shift Field. 0: Shift even field. 0: Shift odd field.	
	SSLN[1:0]	6:5	Sub window Shift Line Numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.	
	ILIM	4	Insert Line when Interlace Mode. 0: Do not insert. 1: Insert.	
	MSFD	3	Main window Shift Field. 0: Shift even field. 1: Shift odd field.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	MSLN[2:0]	2:0	Main window Shift Line Numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 lines between odd and even field. 010: Shift 2 lines between odd and even field. 011: Shift 3 lines between odd and even field. 1xx: Shift 4 lines between odd and even field.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[7:0]	7:0	Insert Fraction Vertical Position.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[15:8]	7:0	See description of '2F60h'.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[7:0]	7:0	Insert Fraction Width. PD Down value.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[15:8]	7:0	See description of '2F62h'.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : RO**
	OVSSTAT[7:0]	7:0	Output Vertical Total Status. Lock status. Equal to 1 when phase error less than 29h/2Ah.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	OVERDESTAT	6	Output Vertical DE Status.	
	-	5:3	Reserved.	
	OVSSTAT[10:8]	2:0	See description of '2F64h'.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	OHTSTAT0[7:0]	7:0	OHSTAT initial value.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x00**	**Access : RO**
	OHTSTAT1[7:0]	7:0	Output H Total Status.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRACST0[7:0]	7:0	Fraction initial value.	
38h (2F70h)	**REG2F70**	**7:0**	**Default : 0x00**	**Access : RO**
	FRACST1[7:0]	7:0	Fraction Status.	
39h (2F72h)	**REG2F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FRACST2[2:0]	2:0	Fraction Status.	
3Ah (2F74h)	**REG2F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FRACST3[2:0]	2:0	Fraction Status.	
3Bh (2F76h)	**REG2F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	HTTMGN[7:0]	7:0	H Total Margin.	
3Bh (2F77h)	**REG2F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSCMGN[7:0]	7:0	SSC Margin.	
3Ch (2F78h)	**REG2F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSTVALUE0[7:0]	7:0	Read Start initial value.	
3Dh (2F7Ah)	**REG2F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	RSTVALUE1[7:0]	7:0	Read Start Value.	
3Eh (2F7Ch)	**REG2F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RSTVALUE2[4:0]	4:0	Read Start initial value.	
3Fh (2F7Eh)	**REG2F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	RSTVALUE3[4:0]	4:0	Read Start Value.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRONT_BACK	5	Set front back mode.	
	-	4:0	Reserved.	
41h (2F82h)	**REG2F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	INP8	7	This bit with INE_DRV3 to enable G replace R and B for gamma mapping.	
	ONE_DRV3	6	Gamma use G replace R and B for gamma mapping.	
	GABYP	5	By pass gamma function.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	4:3	Reserved.	
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTDATA[7:0]	7:0	Reserved.	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	LFCOEF1[2:0]	7:5	Loop filter coefficient 1.	
	LFCOEF2[4:0]	4:0	Loop filter coefficient 2.	
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	TUNE_SLOW[7:0]	7:0	Tune number for OVDE lock value fine tune.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	TFRACN[7:0]	7:0	Target Fraction Number / Frame PLL limit RK[7:0].	
45h (2F8Ah)	**REG2F8A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	PDP_MASK_EN	6	Reserved.	
	-	5	Reserved.	
	FX_PROT	4	Frame Change Protect.	
	-	3:0	Reserved.	
45h (2F8Bh)	**REG2F8B**	**7:0**	**Default : 0x40**	**Access : R/W**
	TSTMD_REG_EN	7	Test Mode Register Enable. 0: Disable. 1: Enable.	
	EOCK	6	Use External Clock (pin) as Output Dot Clock. 0: Disable (use internal dot clock). 1: Enable (use external dot clock).	
	-	5:3	Reserved.	
	BPM	2	Bypass clock Mode (IDCLK as ODCLK). 0: Disable. 1: Enable.	
	PTEN	1	PLL Test register protect bit. 0: Disable. 1: Enable.	
	LRTM	0	LVDS/RSDS Test Mode enable. 0: Disable. 1: Enable.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
46h (2F8Ch)	**REG2F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLKDLYSEL[3:0]	7:4	OCKDLY[3:0]: OCLK Delay adjustment (TCON feature only). 0: 16 step to adjust. 1: Typical 0.8ns delay/step.	
	OCLK	3	Output CLK control. 0: Normal. 1: Invert.	
	ODE	2	Output DE control. 0: Active high. 1: Active low.	
	OVS	1	Output VSYNC control. 0: Active high. 1: Active low.	
	OHS	0	Output HSYNC control. 0: Active high. 1: Active low.	
46h (2F8Dh)	**REG2F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OEDB	5	Output Even Data Bus pin control. 0: Normal. 1: Tri-state.	
	OODB	4	Output Odd Data Bus pin control. 0: Normal. 1: Tri-state.	
	OVS0	3	OVSYNC pin control. 0: Normal. 1: Tri-state.	
	OHS0	2	OHSYNC pin control. 0: Normal. 1: Tri-state.	
	ODE0	1	ODE pin control. 0: Normal. 1: Tri-state.	
	OCLK0	0	OCLK pin control. 0: Normal. 1: Tri-state.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
47h (2F8Eh)	**REG2F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEDRV[1:0]	7:6	Output DE Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
	CLKDRV[1:0]	5:4	Output Clock Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
	ODDDRV[1:0]	3:2	Output data Odd channel Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
	EVENDRV[1:0]	1:0	Output data Even channel Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SKEW[1:0]	5:4	Output data SKEW.	
	ECLKDLY[3:0]	3:0	ECLK Delay adjustment (TCON feature only). 0: 16 steps to adjust. 1: Typical 0.8ns delay/step.	
48h (2F91h)	**REG2F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CLK_MODE	7	0: Disable. 1: Enable.	
	PLL_DIV2	6	0: Normal. 1: Test clock output divided by 2.	
	DDR_TEST	5	1: Select DDR 29est bus.	
	TEST_MD_D	4	1: Enable 24-bit test bus output.	
	-	3:0	Reserved.	
49h (2F92h)	**REG2F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	BIST_STS[7:0]	7:0	Reserved.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
49h (2F93h)	**REG2F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHIPID[7:0]	7:0	Chip ID.	
4Ah (2F94h)	**REG2F94**	**7:0**	**Default : 0x00**	**Access : RO**
	BOND_STS[7:0]	7:0	Reserved.	
4Bh (2F96h)	**REG2F96**	**7:0**	**Default : 0x44**	**Access : R/W**
	LP_SET0[7:0]	7:0	Output PLL Set.	
4Bh (2F97h)	**REG2F97**	**7:0**	**Default : 0x55**	**Access : R/W**
	LP_SET0[15:8]	7:0	See description of '2F96h'.	
4Ch (2F98h)	**REG2F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	LP_SET1[7:0]	7:0	Output PLL Set.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBN10	7	10-bit Bus enable.	
	DITHER_MINUS	6	1: Enable.	
	GPODDC	5	GPO, GPO[3] use for DDC DAT/CLK.	
	M_GRG	4	Main window Gamma Rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	
56h (2FACh)	**REG2FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIM_HS	7	Limit Htotal by PWM counter enable.	
	NEW_FIELD_SEL	6	Select field created method. 0: Created by Vsync and Hsync. 1: Created by VFDE.	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end. 1: Vsync end.	
	-	4:0	Reserved.	
57h (2FAEh)	**REG2FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	REM[7:0]	7:0	Htotal REMainder value.	
57h (2FAFh)	**REG2FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	REM[11:8]	3:0	See description of '2FAEh'.	
58h	**REG2FB0**	**7:0**	**Default : 0x00**	**Access : R/W**

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FB0h)	PWM5DIV[7:0]	7:0	PWM5 CLK div factor.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PWM5DIV[8]	0	See description of '2FB0h'.	
59h (2FB2h)	**REG2FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DUTY[7:0]	7:0	PWM5 period.	
5Ah (2FB4h)	**REG2FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRACE_PHASE_HTOTAL[7:0]	7:0	New Htotal for fast phase offset reduce, only active when TRACE_PHASE_EN is set to 1.	
5Ah (2FB5h)	**REG2FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NEW_HBC_CLAMP	6	Clamp function for HBC gain.	
	NEW_HBC_GAIN	5	HBC gain mode. 0: 0.4. 1: 0.04.	
	TRACE_PHASE_EN	4	Enable modify Htotal for fast phase offset reduce.	
	TRACE_PHASE_HTOTAL[11:8]	3:0	See description of '2FB4h'.	
64h (2FC8h)	**REG2FC8**	**7:0**	**Default : 0x07**	**Access : R/W**
	BIUCLK_DIV[7:0]	7:0	Calculate VDE ratio BIUCLK divider.	
64h (2FC9h)	**REG2FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RPT_VRATIO_EN	0	Report VDE Vtotal ratio enable.	
65h (2FCAh)	**REG2FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_0_REG[7:0]	7:0		
65h (2FCBh)	**REG2FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_1_REG[7:0]	7:0		
66h (2FCCh)	**REG2FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_2_REG[7:0]	7:0		
66h (2FCDh)	**REG2FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_3_REG[7:0]	7:0		
67h (2FCEh)	**REG2FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_4_REG[7:0]	7:0		
67h	**REG2FCF**	**7:0**	**Default : 0x00**	**Access : R/W**

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FCFh)	PIP_OP2_5_REG[7:0]	7:0		
68h (2FD0h)	**REG2FD0**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[7:0]	7:0	Input VDE PRD value.	
68h (2FD1h)	**REG2FD1**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[15:8]	7:0	See description of '2FD0h'.	
69h (2FD2h)	**REG2FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[7:0]	7:0	Input Vtt PRD value.	
69h (2FD3h)	**REG2FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[15:8]	7:0	See description of '2FD2h'.	
6Ah (2FD4h)	**REG2FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HIFRC_SROT	7	Enable HIFRC spatial rotation.	
	RAN[1:0]	6:5	Enable HIFRC RANdom noise latch for rotation.	
	F2_EN	4	Enable noise repeats 2 frames.	
	NEW_DITH_M	3	New dither method select.	
	-	2	Reserved.	
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.	
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.	
6Ah (2FD5h)	**REG2FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.	
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.	
	H_RAN_EN	3	H direction using random noise enable for HIFRC.	
	NEW_ACBD	2	Swap HIFRC probability sequence.	
	OLD_HIFRC	1	Select old HIFRC dither method.	
	RAN_DIR_EN	0	Enable noise as rotate direction.	
6Ch (2FD8h)	**REG2FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table r/w address.	
6Dh (2FDAh)	**REG2FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_W_FLAG2	7	LUT table blue write command.	
	LUT_W_FLAG1	6	LUT table green write command.	
	LUT_W_FLAG0	5	LUT table red write command.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	4:0	Reserved.	
6Dh (2FDBh)	**REG2FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_R_FLAG2	7	LUT table blue read command.	
	LUT_R_FLAG1	6	LUT table green read command.	
	LUT_R_FLAG0	5	LUT table red read command.	
	-	4:0	Reserved.	
6Eh (2FDCh)	**REG2FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_R[7:0]	7:0	Data write to R LUT SRAM.	
6Eh (2FDDh)	**REG2FDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_R[11:8]	3:0	See description of '2FDCh'.	
6Fh (2FDEh)	**REG2FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_G[7:0]	7:0	Data write to G LUT SRAM.	
6Fh (2FDFh)	**REG2FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_G[11:8]	3:0	See description of '2FDEh'.	
70h (2FE0h)	**REG2FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_B[7:0]	7:0	Data write to B LUT SRAM.	
70h (2FE1h)	**REG2FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_B[11:8]	3:0	See description of '2FE0h'.	
71h (2FE2h)	**REG2FE2**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_R[7:0]	7:0	Data read from R LUT SRAM.	
71h (2FE3h)	**REG2FE3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_R[11:8]	3:0	See description of '2FE2h'.	
72h (2FE4h)	**REG2FE4**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_G[7:0]	7:0	Data read from G LUT SRAM.	
72h (2FE5h)	**REG2FE5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_G[11:8]	3:0	See description of '2FE4h'.	
73h (2FE6h)	**REG2FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_B[7:0]	7:0	Data read from B LUT SRAM.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
73h (2FE7h)	**REG2FE7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_B[11:8]	3:0	See description of '2FE6h'.	
74h (2FE8h)	**REG2FE8**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:4	Reserved.	
	CLR_MLOAD_TOO_SLOW	3	Clear auto mload gamma too slow flag.	
	MLOAD_TOO_SLOW	2	Auto mload gamma too slow flag.	
	AUTO_MLOAD_SWITCH	1	Enable auto mload gamma switch gamma table by frame.	
	AUTO_MLOAD_GAMMA	0	Enable auto mload gamma function.	
75h (2FEAh)	**REG2FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.	
75h (2FEBh)	**REG2FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[15:8]	7:0	See description of '2FEAh'.	
76h (2FECh)	**REG2FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[23:16]	7:0	See description of '2FEAh'.	
77h (2FEEh)	**REG2FEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.	
77h (2FEFh)	**REG2FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[15:8]	7:0	See description of '2FEEh'.	
78h (2FF0h)	**REG2FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[23:16]	7:0	See description of '2FEEh'.	
79h (2FF2h)	**REG2FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.	
7Ah (2FF4h)	**REG2FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.	
7Ah (2FF5h)	**REG2FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE0[11:8]	3:0	See description of '2FF4h'.	
7Bh (2FF6h)	**REG2FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.	
7Bh (2FF7h)	**REG2FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE1[11:8]	3:0	See description of '2FF6h'.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Ch (2FF8h)	**REG2FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.	
7Ch (2FF9h)	**REG2FF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE0[11:8]	3:0	See description of '2FF8h'.	
7Dh (2FFAh)	**REG2FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.	
7Dh (2FFBh)	**REG2FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE1[11:8]	3:0	See description of '2FFAh'.	
7Eh (2FFCh)	**REG2FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.	
7Eh (2FFDh)	**REG2FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE0[11:8]	3:0	See description of '2FFCh'.	
7Fh (2FFEh)	**REG2FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.	
7Fh (2FFFh)	**REG2FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE1[11:8]	3:0	See description of '2FFEh'.	

SCMI Register (Bank = 2F, Sub-Bank = 12)

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data config from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data config from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data config from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data config from mode 5 change to mode 4.	
01h (2F03h)	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	
	STILL_MODE_F2	3	F2 image freeze enable.	
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.	
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAPTURE_START_F2	7	F2 image capture start.	
	IPM_READ_OFF_F2	6	F2 force IP read request disable.	
	MADI_FORCE_OFF_F2	5	F2 force madi off.	
	MADI_FORCE_ON_F2	4	F2 force madi on.	
	FBL_25D	3	F2 frame buffer less de-interlace mode.	
	YC_SEPARATE_F2	2	F2 YC separate in FB.	
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.	
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.	
	DUMMY03_6_6	6	DUMMY03_6_6	
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.	
	IPM_LINEAR_EN_F2	4	F2 IP linear address enable.	
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.	
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.	
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.	
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.	
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.	
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.	
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.	
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.	
	DOT_LN_PON_SEL_F2	1	F2 OP MADi dot line data select.	
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.	
	-	6:4	Reserved.	
	DUMMY04_2_3[1:0]	3:2	Dummy register.	
	BOB_YMR_10_EN_F2	1	F2 10-bits Bob mode with Y motion.	
	BOB_YMR_8_EN_F2	0	F2 8-bits Bob mode with Y motion.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_WBE_MASK_F2	7	F2 mask write byte enable (for test).	
	DUMMY04_14_14	6	Dummy register.	
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.	
	IP_2FRAME_BYPASS_F2	4	F2 IP bypass two frames data to OPM.	
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.	
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.	
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.	
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY05_4_15[3:0]	7:4	DUMMY05_4_15	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY05_4_15[11:4]	7:0	See description of '2F0Ah'.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY06_0_15[7:0]	7:0	Dummy register.	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY06_0_15[15:8]	7:0	See description of '2F0Ch'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x88**	**Access : R/W**
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.	
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.	
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.	
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.	
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.	
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	RW_BANK_MAP_F2[1:0]	7:6	F2 read/write bank mapping mode.	
	4FRAME_MODE_F2	5	F2 4 frames buffer for progressive mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '2F10h'.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '2F10h'.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR1_F2[7:0]	7:0	F2 IP frame buffer base address 1.	
0Ah (2F15h)	**REG2F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR1_F2[15:8]	7:0	See description of '2F14h'.	
0Bh (2F16h)	**REG2F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR1_F2[23:16]	7:0	See description of '2F14h'.	
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR2_F2[7:0]	7:0	F2 IP frame buffer base address 2.	
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR2_F2[15:8]	7:0	See description of '2F18h'.	
0Dh (2F1Ah)	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR2_F2[23:16]	7:0	See description of '2F18h'.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (2F1Dh)	**REG2F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IPM_OFFSET_F2[11:8]	3:0	See description of '2F1Ch'.	
0Fh (2F1Eh)	**REG2F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (2F1Fh)	**REG2F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_FETCH_NUM_F2[11:8]	3:0	See description of '2F1Eh'.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '2F20h'.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '2F20h'.	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '2F24h'.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '2F24h'.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR2_F2[7:0]	7:0	F2 OP frame buffer base address 2.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR2_F2[15:8]	7:0	See description of '2F28h'.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR2_F2[23:16]	7:0	See description of '2F28h'.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_OFFSET_F2[11:8]	3:0	See description of '2F2Ch'.	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.	
17h (2F2Fh)	**REG2F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '2F2Eh'.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_VCNT_LIMIT_EN_F2	4	F2 IP line count limit enable.	
	IPM_VCNT_LIMIT_NUM_F2[11:8]	3:0	See description of '2F30h'.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.	
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '2F34h'.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '2F34h'.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IPM_W_LIMIT_EN_F2	1	F2 IP write limit enable.	
	IPM_W_LIMIT_MIN_F2	0	F2 IP write limit flag 0: Maximum 1: Minimum.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.	
1Ch (2F39h)	**REG2F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SW_HMIR_OFFSET_EN_F2	4	F2 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F2[11:8]	3:0	See description of '2F38h'.	
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1D_0_15[7:0]	7:0	Dummy register.	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1D_0_15[15:8]	7:0	See description of '2F3Ah'.	
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1E_0_15[7:0]	7:0	Dummy register.	
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1E_0_15[15:8]	7:0	See description of '2F3Ch'.	
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1F_0_15[7:0]	7:0	DUMMY1F_0_15	
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1F_0_15[15:8]	7:0	See description of '2F3Eh'.	
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.	
20h	**REG2F41**	**7:0**	**Default : 0x10**	**Access : R/W**

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F41h)	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.	
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.	
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.	
22h (2F45h)	**REG2F45**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.	
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.	
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.	
24h (2F49h)	**REG2F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.	
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.	
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x28**	**Access : R/W**
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.	
25h (2F4Bh)	**REG2F4B**	**7:0**	**Default : 0x28**	**Access : R/W**
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.	
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.	
26h (2F4Dh)	**REG2F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_13_15[2:0]	7:5	DUMMY26_13_15	
	-	4:0	Reserved.	
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_0_15[7:0]	7:0	Dummy register.	
27h (2F4Fh)	**REG2F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_0_15[15:8]	7:0	See description of '2F4Eh'.	
28h (2F50h)	**REG2F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY28_0_15[7:0]	7:0	DUMMY28_0_15	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (2F51h)	**REG2F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY28_0_15[15:8]	7:0	See description of '2F50h'.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY34_7_7	7	DUMMY34_7_7	
	OPM_MIU_RRDY_BYPASS	6	F2 OPM bypass MIU enable, for test.	
	IPM_MIU_RRDY_BYPASS	5	F2 IPM bypass MIU enable, for test.	
	IPM_CHK_SUM_EN	4	F2 check sum test enable.	
	IPM_CHK_SUM_VCNT[3:0]	3:0	F2 check sum v count.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[7:0]	7:0	F2 status read out for debug.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[15:8]	7:0	See description of '2F6Ah'.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[7:0]	7:0	F2 status read out for debug.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[15:8]	7:0	See description of '2F6Ch'.	
38h (2F70h)	**REG2F70**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[7:0]	7:0	F2 status read out for debug.	
38h (2F71h)	**REG2F71**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[15:8]	7:0	See description of '2F70h'.	
39h (2F72h)	**REG2F72**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[7:0]	7:0	F2 status read out for debug.	
39h (2F73h)	**REG2F73**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[15:8]	7:0	See description of '2F72h'.	
3Ah (2F74h)	**REG2F74**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[7:0]	7:0	F2 status read out for debug.	
3Ah (2F75h)	**REG2F75**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[15:8]	7:0	See description of '2F74h'.	
3Bh (2F76h)	**REG2F76**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[7:0]	7:0	F2 status read out for debug.	
3Bh (2F77h)	**REG2F77**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[15:8]	7:0	See description of '2F76h'.	
3Ch	**REG2F78**	**7:0**	**Default : 0x00**	**Access : RO**

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F78h)	STATUS_READ_3C_F2[7:0]	7:0	F2 status read out for debug.	
3Ch (2F79h)	**REG2F79**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[15:8]	7:0	See description of '2F78h'.	
3Dh (2F7Ah)	**REG2F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[7:0]	7:0	F2 status read out for debug.	
3Dh (2F7Bh)	**REG2F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[15:8]	7:0	See description of '2F7Ah'.	
3Eh (2F7Ch)	**REG2F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[7:0]	7:0	F2 status read out for debug.	
3Eh (2F7Dh)	**REG2F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[15:8]	7:0	See description of '2F7Ch'.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x01**	**Access : R/W**
	DUMMY40_1_15[6:0]	7:1	Dummy register.	
	VSYN_LATCH_EN	0	Register latch with output V sync enable.	
40h (2F81h)	**REG2F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY40_1_15[14:7]	7:0	See description of '2F80h'.	
41h (2F82h)	**REG2F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY41_7_6[1:0]	7:6	Dummy register.	
	RGB_YUV444_10BIT_F1	5	F1 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F1	4	F1 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F1	3	F1 memory data config from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F1	2	F1 memory data config from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F1	1	F1 memory data config from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F1	0	F1 memory data config from mode 5 change to mode 4.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : R/W**
		7	Reserved.	
	MOTION_TH1_F1[2:0]	6:4	F1 Motion Threshold for normal case.	
	STILL_MODE_F1	3	F1 image freeze enable.	
	DE_INTL_MD_F1[2:0]	2:0	F1 IP memory data format.	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MEM_CONFIG_F1[3:0]	7:4	F1 OP memory data format.	
	IPM_MEM_CONFIG_F1[3:0]	3:0	F1 IP memory data format.	
42h	**REG2F85**	**7:0**	**Default : 0x00**	**Access : R/W**

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F85h)	CAPTURE_START_F1	7	F1 image capture start.	
	IPM_READ_OFF_F1	6	F1 force IP read request disable.	
	MADI_FORCE_OFF_F1	5	F1 force madi off.	
	MADI_FORCE_ON_F1	4	F1 force madi on.	
	-	3	Reserved.	
	YC_SEPARATE_F1	2	F1 YC separate in FB.	
	OPM_CONFIG_DEFINE_F1	1	F1 OP enable define memory data format.	
	IPM_CONFIG_DEFINE_F1	0	F1 IP enable define memory data format.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_REQ_RST_F1	7	F1 reset IP to MIU request signal.	
	DUMMY43_6_6	6	Dummy register.	
	OPM_LINEAR_EN_F1	5	F1 OP linear address enable.	
	IPM_LINEAR_EN_F1	4	F1 IP linear address enable.	
	OPM_4READ_EN_F1	3	F1 OP read 4 fields enable.	
	OPM_3READ_EN_F1	2	F1 OP read 3 fields enable.	
	OPM_2READ_EN_F1	1	F1 OP read 2 fields enable.	
	OPM_1READ_EN_F1	0	F1 OP read 1 field enable.	
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:6	Reserved.	
	IPM_V_MIRROR_F1	5	F1 IP Vertical mirror enable.	
	IPM_H_MIRROR_F1	4	F1 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F1	3	F1 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F1	2	F1 OP film dot line data select.	
	DOT_LN_PON_SEL_F1	1	F1 OP MADi dot line data select.	
	YC_SWAP_EN_F1	0	F1 OP Y/C data swap enable.	
44h (2F88h)	**REG2F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	3FRAME_MODE_F1	7	F1 3 frames buffer for progressive mode.	
	-	6:4	Reserved.	
	DUMMY44_2_3[1:0]	3:2	Dummy register.	
	BOB_YMR_10_EN_F1	1	F1 10-bits Bob mode with Y motion.	
	BOB_YMR_8_EN_F1	0	F1 8-bits Bob mode with Y motion.	
44h (2F89h)	**REG2F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_WBE_MASK_F1	7	F1 mask write byte enable (for test).	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DUMMY44_14_14	6	DUMMY44_14_14	
	IPM_444_READ_EN_F1	5	F1 IP 444 format read from memory enable.	
	-	4:2	Reserved.	
	IPM_Y_ONLY_W_F1	1	F1 IP write Y only.	
	IPM_Y_ONLY_R_F1	0	F1 IP read Y only.	
45h (2F8Ah)	**REG2F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY45_4_15[3:0]	7:4	Dummy registers.	
	FRC_WITH_LCNT_F1	3	F1 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F1[2:0]	2:0	F1 IP write line count status select.	
45h (2F8Bh)	**REG2F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY45_4_15[11:4]	7:0	See description of '2F8Ah'.	
46h (2F8Ch)	**REG2F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY46_0_15[7:0]	7:0	Dummy register.	
46h (2F8Dh)	**REG2F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY46_0_15[15:8]	7:0	See description of '2F8Ch'.	
47h (2F8Eh)	**REG2F8E**	**7:0**	**Default : 0x88**	**Access : R/W**
	W_VP_CNT_CLR_F1	7	F1 IP write mask field count clear.	
	W_MASK_MODE_F1[2:0]	6:4	F1 IP write mask number by field.	
	IPM_STATUS_CLR_F1	3	F1 IP status clear enable.	
	IPM_RREQ_FORCE_F1	2	F1 IP read request force enable.	
	IPM_RREQ_OFF_F1	1	F1 IP read request disable.	
	IPM_WREQ_OFF_F1	0	F1 IP write request disable.	
47h (2F8Fh)	**REG2F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	RW_BANK_MAP_F1[1:0]	7:6	F1 read/write bank mapping mode.	
	4FRAME_MODE_F1	5	F1 4 frames buffer for progressive mode.	
	BK_FIELD_INV_F1	4	F1 read/write bank inverse.	
	OPM_RBANK_FORCE_F1	3	F1 OP force read bank enable.	
	OPM_RBANK_SEL_F1[2:0]	2:0	F1 OP force read bank select.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F1[7:0]	7:0	F1 IP frame buffer base address 0.	
48h (2F91h)	**REG2F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F1[15:8]	7:0	See description of '2F90h'.	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
49h (2F92h)	**REG2F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F1[23:16]	7:0	See description of '2F90h'.	
4Ah (2F94h)	**REG2F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR1_F1[7:0]	7:0	F1 IP frame buffer base address 1.	
4Ah (2F95h)	**REG2F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR1_F1[15:8]	7:0	See description of '2F94h'.	
4Bh (2F96h)	**REG2F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR1_F1[23:16]	7:0	See description of '2F94h'.	
4Ch (2F98h)	**REG2F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR2_F1[7:0]	7:0	F1 IP frame buffer base address 2.	
4Ch (2F99h)	**REG2F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR2_F1[15:8]	7:0	See description of '2F98h'.	
4Dh (2F9Ah)	**REG2F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR2_F1[23:16]	7:0	See description of '2F98h'.	
4Eh (2F9Ch)	**REG2F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_OFFSET_F1[7:0]	7:0	F1 IP frame buffer line offset (pixel unit).	
4Eh (2F9Dh)	**REG2F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IPM_OFFSET_F1[11:8]	3:0	See description of '2F9Ch'.	
4Fh (2F9Eh)	**REG2F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_FETCH_NUM_F1[7:0]	7:0	F1 IP fetch pixel number of one line.	
4Fh (2F9Fh)	**REG2F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IPM_FETCH_NUM_F1[11:8]	3:0	See description of '2F9Eh'.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[7:0]	7:0	F1 OP frame buffer base address 0.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[15:8]	7:0	See description of '2FA0h'.	
51h (2FA2h)	**REG2FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[23:16]	7:0	See description of '2FA0h'.	
52h (2FA4h)	**REG2FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[7:0]	7:0	F1 OP frame buffer base address 1.	
52h	**REG2FA5**	**7:0**	**Default : 0x00**	**Access : R/W**

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FA5h)	OPM_BASE_ADDR1_F1[15:8]	7:0	See description of '2FA4h'.	
53h (2FA6h)	**REG2FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[23:16]	7:0	See description of '2FA4h'.	
54h (2FA8h)	**REG2FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR2_F1[7:0]	7:0	F1 OP frame buffer base address 2.	
54h (2FA9h)	**REG2FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR2_F1[15:8]	7:0	See description of '2FA8h'.	
55h (2FAAh)	**REG2FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR2_F1[23:16]	7:0	See description of '2FA8h'.	
56h (2FACh)	**REG2FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F1[7:0]	7:0	F1 OP frame buffer line offset (pixel unit).	
56h (2FADh)	**REG2FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_OFFSET_F1[11:8]	3:0	See description of '2FACh'.	
57h (2FAEh)	**REG2FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F1[7:0]	7:0	F1 OP fetch pixel number of one line.	
57h (2FAFh)	**REG2FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F1[11:8]	3:0	See description of '2FAEh'.	
58h (2FB0h)	**REG2FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_NUM_F1[7:0]	7:0	F1 IP line count limit number for frame buffer write.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_VCNT_LIMIT_EN_F1	4	F1 IP line count limit enable.	
	IPM_VCNT_LIMIT_NUM_F1[11:8]	3:0	See description of '2FB0h'.	
5Ah (2FB4h)	**REG2FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F1[7:0]	7:0	F1 IP write limit address.	
5Ah (2FB5h)	**REG2FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F1[15:8]	7:0	See description of '2FB4h'.	
5Bh (2FB6h)	**REG2FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F1[23:16]	7:0	See description of '2FB4h'.	
5Bh (2FB7h)	**REG2FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_W_LIMIT_EN_F1	1	F1 IP write limit enable.	
	IPM_W_LIMIT_MIN_F1	0	F1 IP write limit flag 0: Maximum 1: Minimum.	
5Ch (2FB8h)	**REG2FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_F1[7:0]	7:0	F1 IP H mirror line offset.	
5Ch (2FB9h)	**REG2FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SW_HMIR_OFFSET_EN_F1	4	F1 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F1[11:8]	3:0	See description of '2FB8h'.	
5Dh (2FBAh)	**REG2FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY5D_0_15[7:0]	7:0	Dummy register.	
5Dh (2FBBh)	**REG2FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY5D_0_15[15:8]	7:0	See description of '2FBAh'.	
5Eh (2FBCh)	**REG2FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY5E_0_15[7:0]	7:0	Dummy register.	
5Eh (2FBDh)	**REG2FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY5E_0_15[15:8]	7:0	See description of '2FBCh'.	
5Fh (2FBEh)	**REG2FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY5F_0_15[7:0]	7:0	Dummy register.	
5Fh (2FBFh)	**REG2FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY5F_0_15[15:8]	7:0	See description of '2FBEh'.	
60h (2FC0h)	**REG2FC0**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_THRD_F1[7:0]	7:0	F1 IP FIFO threshold for read request.	
60h (2FC1h)	**REG2FC1**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_HPRI_F1[7:0]	7:0	F1 IP high priority threshold for read request.	
61h (2FC2h)	**REG2FC2**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_THRD_F1[7:0]	7:0	F1 IP FIFO threshold for write request.	
61h (2FC3h)	**REG2FC3**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_HPRI_F1[7:0]	7:0	F1 IP high priority threshold for write request.	
62h (2FC4h)	**REG2FC4**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_MAX_F1[7:0]	7:0	F1 IP read request max number.	
62h (2FC5h)	**REG2FC5**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_MAX_F1[7:0]	7:0	F1 IP write request max number.	
65h	**REG2FCA**	**7:0**	**Default : 0x20**	**Access : R/W**

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FCAh)	IPM_RFIFO_DEPTH_F1[7:0]	7:0	F1 IP line buffer length for memory data read.	
65h (2FCBh)	**REG2FCB**	**7:0**	**Default : 0x20**	**Access : R/W**
	IPM_WFIFO_DEPTH_F1[7:0]	7:0	F1 IP line buffer length for memory data write.	
66h (2FCDh)	**REG2FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY66_13_15[2:0]	7:5	Dummy register.	
	-	4:0	Reserved.	
67h (2FCEh)	**REG2FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY67_0_15[7:0]	7:0	Dummy register.	
67h (2FCFh)	**REG2FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY67_0_15[15:8]	7:0	See description of '2FCEh'.	
68h (2FD0h)	**REG2FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY68_0_15[7:0]	7:0	Dummy register.	
68h (2FD1h)	**REG2FD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY68_0_15[15:8]	7:0	See description of '2FD0h'.	
74h (2FE8h)	**REG2FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY74_7_7	7	Dummy register.	
	-	6:0	Reserved.	
78h ~ 7Eh (2FF0h ~ 2FFDh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

ACE Register (Bank = 2F, Sub-Bank = 18)

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
10h ~ 28h (2F20h ~ 2F51h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:3	Reserved.	
	SUB_ICC_EN	2	Sub window ICC enable.	
	-	1:0	Reserved.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_R[3:0]	7:4	Sub window ICC saturation adjustment of R.	

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_G[3:0]	7:4	Sub window ICC saturation adjustment of G.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_B[3:0]	7:4	Sub window ICC saturation adjustment of B.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_C[3:0]	7:4	Sub window ICC saturation adjustment of C.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_M[3:0]	7:4	Sub window ICC saturation adjustment of M.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h (2F67h)	**REG2F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_Y[3:0]	7:4	Sub window ICC saturation adjustment of Y.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_F[3:0]	7:4	Sub window ICC saturation adjustment of F.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SIGN_SA_USER[7:0]	7:0	Sub window ICC decrease saturation.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold.	
3Ch (2F78h)	**REG2F78**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WPL_WHITE_PEAK_LIMIT_THRD[7:0]	7:0	White peak limit threshold.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IBC_EN	7	Main window IBC enable.	

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_IBC_EN	6	Sub window IBC enable.	
	-	5:0	Reserved.	
41h (2F82h)	**REG2F82**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.	
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.	
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.	
44h (2F88h)	**REG2F88**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.	
45h (2F8Ah)	**REG2F8A**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YR_ADJ[5:0]	5:0	Sub window IBC Y adjustment of R.	
45h (2F8Bh)	**REG2F8B**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YG_ADJ[5:0]	5:0	Sub window IBC Y adjustment of G.	
46h (2F8Ch)	**REG2F8C**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YB_ADJ[5:0]	5:0	Sub window IBC Y adjustment of B.	
46h	**REG2F8D**	**7:0**	**Default : 0x20**	**Access : R/W**

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F8Dh)	-	7:6	Reserved.	
	SUB_YC_ADJ[5:0]	5:0	Sub window IBC Y adjustment of C.	
47h (2F8Eh)	**REG2F8E**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YM_ADJ[5:0]	5:0	Sub window IBC Y adjustment of M.	
47h (2F8Fh)	**REG2F8F**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YY_ADJ[5:0]	5:0	Sub window IBC Y adjustment of Y.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YF_ADJ[5:0]	5:0	Sub window IBC Y adjustment of F.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_WHITE_PEAK_LIMIT_EN	3	Main window white peak limit enable.	
	-	2:0	Reserved.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_WHITE_PEAK_LIMIT_EN	3	Sub window white peak limit enable.	
	-	2:0	Reserved.	
59h ~ 5Fh (2FB2h ~ 2FBFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (2FC0h)	**REG2FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_EN	7	Main window IHC enable.	
	SUB_IHC_EN	6	Sub window IHC enable.	
	-	5:0	Reserved.	
61h (2FC2h)	**REG2FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.	
61h (2FC3h)	**REG2FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.	
62h	**REG2FC4**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FC4h)	-	7	Reserved.	
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.	
62h (2FC5h)	**REG2FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.	
63h (2FC6h)	**REG2FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.	
63h (2FC7h)	**REG2FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.	
64h (2FC8h)	**REG2FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.	
65h (2FCAh)	**REG2FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_R[6:0]	6:0	Sub window IHC hue adjustment of R.	
65h (2FCBh)	**REG2FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_G[6:0]	6:0	Sub window IHC hue adjustment of G.	
66h (2FCCh)	**REG2FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_B[6:0]	6:0	Sub window IHC hue adjustment of B.	
66h (2FCDh)	**REG2FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_C[6:0]	6:0	Sub window IHC hue adjustment of C.	
67h (2FCEh)	**REG2FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_M[6:0]	6:0	Sub window IHC hue adjustment of M.	
67h (2FCFh)	**REG2FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_Y[6:0]	6:0	Sub window IHC hue adjustment of Y.	
68h	**REG2FD0**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FD0h)	-	7	Reserved.	
	SUB_HUE_USER_F[6:0]	6:0	Sub window IHC hue adjustment of F.	
6Eh (2FDCh)	**REG2FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R2Y_EN	4	Sub window RGB to YCbCr enable.	
	-	3:2	Reserved.	
	R2Y_DITHER_EN	1	RGB to YCbCr dither enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr enable.	
6Fh (2FDEh)	**REG2FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_R2Y_EQ_SEL[1:0]	5:4	Sub window RGB to YCbCr equation selection.	
	-	3:2	Reserved.	
	MAIN_R2Y_EQ_SEL[1:0]	1:0	Main window RGB to YCbCr equation selection.	
70h ~ 74h (2FE0h ~ 2FE9h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	VPS_SRAM_ACT	7	2D peaking line-buffer sram active.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2:1	Reserved.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_PEAKING_EN	7	Main window band8 peaking enable.	
	MAIN_BAND7_PEAKING_EN	6	Main window band7 peaking enable.	
	MAIN_BAND6_PEAKING_EN	5	Main window band6 peaking enable.	
	MAIN_BAND5_PEAKING_EN	4	Main window band5 peaking enable.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.	
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.	
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.	
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_COEF_STEP[1:0]	7:6	Main window band8 coefficient step.	
	MAIN_BAND7_COEF_STEP[1:0]	5:4	Main window band7 coefficient step.	
	MAIN_BAND6_COEF_STEP[1:0]	3:2	Main window band6 coefficient step.	
	MAIN_BAND5_COEF_STEP[1:0]	1:0	Main window band5 coefficient step.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_V_LPF_COEF_2[2:0]	6:4	Main window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	
	MAIN_V_LPF_COEF_1[2:0]	2:0	Main window vertical up-down pixel Y LPF coefficient.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_OSD_SHARPNESS_CTRL[5:0]	5:0	Main window user sharpness adjust.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_LPF_COEF[2:0]	6:4	Sub window horizontal Y LPF coefficient.	
	MAIN_SUB_EXCHANGE_EN	3	Main/Sub window swap enable.	
	-	2:1	Reserved.	
	SUB_POST_PEAKING_EN	0	Sub window 2D peaking enable.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND8_PEAKING_EN	7	Sub window band8 peaking enable.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BAND7_PEAKING_EN	6	Sub window band7 peaking enable.	
	SUB_BAND6_PEAKING_EN	5	Sub window band6 peaking enable.	
	SUB_BAND5_PEAKING_EN	4	Sub window band5 peaking enable.	
	SUB_BAND4_PEAKING_EN	3	Sub window band4 peaking enable.	
	SUB_BAND3_PEAKING_EN	2	Sub window band3 peaking enable.	
	SUB_BAND2_PEAKING_EN	1	Sub window band2 peaking enable.	
	SUB_BAND1_PEAKING_EN	0	Sub window band1 peaking enable.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND4_COEF_STEP[1:0]	7:6	Sub window band4 coefficient step.	
	SUB_BAND3_COEF_STEP[1:0]	5:4	Sub window band3 coefficient step.	
	SUB_BAND2_COEF_STEP[1:0]	3:2	Sub window band2 coefficient step.	
	SUB_BAND1_COEF_STEP[1:0]	1:0	Sub window band1 coefficient step.	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND8_COEF_STEP[1:0]	7:6	Sub window band8 coefficient step.	
	SUB_BAND7_COEF_STEP[1:0]	5:4	Sub window band7 coefficient step.	
	SUB_BAND6_COEF_STEP[1:0]	3:2	Sub window band6 coefficient step.	
	SUB_BAND5_COEF_STEP[1:0]	1:0	Sub window band5 coefficient step.	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_V_LPF_COEF_2[2:0]	6:4	Sub window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	
	SUB_V_LPF_COEF_1[2:0]	2:0	Sub window vertical up-down pixel Y LPF coefficient.	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CORING_THRD_2[3:0]	7:4	Sub window coring threshold 2.	
	SUB_CORING_THRD_1[3:0]	3:0	Sub window coring threshold 1.	
17h (2F2Fh)	**REG2F2F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_OSD_SHARPNESS_CTRL[5:0]	5:0	Sub window user sharpness adjust.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.	
19h (2F33h)	**REG2F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND5_COEF[5:0]	5:0	Main window band5 coefficient.	
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND6_COEF[5:0]	5:0	Main window band6 coefficient.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND7_COEF[5:0]	5:0	Main window band7 coefficient.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND8_COEF[5:0]	5:0	Main window band8 coefficient.	
28h (2F50h)	**REG2F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND1_COEF[5:0]	5:0	Sub window band1 coefficient.	
28h (2F51h)	**REG2F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND2_COEF[5:0]	5:0	Sub window band2 coefficient.	
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND3_COEF[5:0]	5:0	Sub window band3 coefficient.	
29h (2F53h)	**REG2F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND4_COEF[5:0]	5:0	Sub window band4 coefficient.	
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BAND5_COEF[5:0]	5:0	Sub window band5 coefficient.	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND6_COEF[5:0]	5:0	Sub window band6 coefficient.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND7_COEF[5:0]	5:0	Sub window band7 coefficient.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND8_COEF[5:0]	5:0	Sub window band8 coefficient.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CORING_THRD_STEP[1:0]	5:4	Main window coring step.	
	-	3:2	Reserved.	
	SUB_CORING_THRD_STEP[1:0]	1:0	Sub window coring step.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND2_CORING_THRD[3:0]	7:4	Main window band2 coring threshold.	
	MAIN_BAND1_CORING_THRD[3:0]	3:0	Main window band1 coring threshold.	
33h (2F67h)	**REG2F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND4_CORING_THRD[3:0]	7:4	Main window band4 coring threshold.	
	MAIN_BAND3_CORING_THRD[3:0]	3:0	Main window band3 coring threshold.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND6_CORING_THRD[3:0]	7:4	Main window band6 coring threshold.	
	MAIN_BAND5_CORING_THRD[3:0]	3:0	Main window band5 coring threshold.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_CORING_THRD[3:0]	7:4	Main window band8 coring threshold.	
	MAIN_BAND7_CORING_THRD[3:0]	3:0	Main window band7 coring threshold.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND2_CORING_THRD[3:0]	7:4	Sub window band2 coring threshold.	
	SUB_BAND1_CORING_THRD[3:0]	3:0	Sub window band1 coring threshold.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND4_CORING_THRD[3:0]	7:4	Sub window band4 coring threshold.	
	SUB_BAND3_CORING_THRD[3:0]	3:0	Sub window band3 coring threshold.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND6_CORING_THRD[3:0]	7:4	Sub window band6 coring threshold.	
	SUB_BAND5_CORING_THRD[3:0]	3:0	Sub window band5 coring threshold.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND8_CORING_THRD[3:0]	7:4	Sub window band8 coring threshold.	
	SUB_BAND7_CORING_THRD[3:0]	3:0	Sub window band7 coring threshold.	
60h (2FC0h)	**REG2FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_GAUSS_LUT_STEP[1:0]	5:4	Main window Gaussian SNR LUT step.	
	-	3:1	Reserved.	
	MAIN_GAUSS_NR_EN	0	Main window Gaussian SNR enable.	
60h (2FC1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
61h (2FC2h)	**REG2FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_GAUSS_LUT_STEP[1:0]	5:4	Sub window Gaussian SNR LUT step.	
	-	3:0	Reserved.	
64h (2FC8h)	**REG2FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_0[7:0]	7:0	Gaussian SNR Table 0.	
64h (2FC9h)	**REG2FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_1[7:0]	7:0	Gaussian SNR Table 1.	
65h (2FCAh)	**REG2FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_2[7:0]	7:0	Gaussian SNR Table 2.	
65h (2FCBh)	**REG2FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_3[7:0]	7:0	Gaussian SNR Table 3.	
66h (2FCCh)	**REG2FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_4[7:0]	7:0	Gaussian SNR Table 4.	
66h (2FCDh)	**REG2FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_5[7:0]	7:0	Gaussian SNR Table 5.	
67h (2FCEh)	**REG2FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_6[7:0]	7:0	Gaussian SNR Table 6.	
67h (2FCFh)	**REG2FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_7[7:0]	7:0	Gaussian SNR Table 7.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Bh ~ 7Fh (2FF6h ~ 2FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

DLC Register (Bank = 2F, Sub-Bank = 1A)

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h ~ 0Ah (2F02h ~ 2F15h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Bh (2F16h)	**REG2F16**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximum pixel.	
0Bh (2F17h)	**REG2F17**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MAX_PIXEL[7:0]	7:0	Sub window maximum pixel.	
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MIN_PIXEL[7:0]	7:0	Sub window minimum pixel.	

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.	
0Eh (2F1Dh)	**REG2F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_BRI_ADJUST_LSB[1:0]	1:0	Sub window Y adjust low bit.	
0Fh (2F1Eh)	**REG2F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust.	
0Fh (2F1Fh)	**REG2F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BRI_ADJUST[7:0]	7:0	Sub window Y adjust.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x40**	**Access : R/W**
	MAIN_Y_GAIN[7:0]	7:0	Main window Y gain.	
14h	**REG2F29**	**7:0**	**Default : 0x40**	**Access : R/W**

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F29h)	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x40**	**Access : R/W**
	SUB_Y_GAIN[7:0]	7:0	Sub window Y gain.	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0x40**	**Access : R/W**
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x20**	**Access : R/W**
	HISTOGRAM_RANGE1[7:0]	7:0	Variable 8 section of histogram range 1.	
1Ch (2F39h)	**REG2F39**	**7:0**	**Default : 0x40**	**Access : R/W**
	HISTOGRAM_RANGE2[7:0]	7:0	Variable 8 section of histogram range 2.	
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0x60**	**Access : R/W**
	HISTOGRAM_RANGE3[7:0]	7:0	Variable 8 section of histogram range 3.	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x80**	**Access : R/W**
	HISTOGRAM_RANGE4[7:0]	7:0	Variable 8 section of histogram range 4.	
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0xA0**	**Access : R/W**
	HISTOGRAM_RANGE5[7:0]	7:0	Variable 8 section of histogram range 5.	
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0xC0**	**Access : R/W**
	HISTOGRAM_RANGE6[7:0]	7:0	Variable 8 section of histogram range 6.	
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0xE0**	**Access : R/W**
	HISTOGRAM_RANGE7[7:0]	7:0	Variable 8 section of histogram range 7.	
20h ~ 27h (2F40h ~ 2F4Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
28h (2F50h)	**REG2F50**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_1F_00[7:0]	7:0	Histogram report section1.	
28h (2F51h)	**REG2F51**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_1F_00[15:8]	7:0	See description of '2F50h'.	
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_3F_20[7:0]	7:0	Histogram report section2.	
29h (2F53h)	**REG2F53**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_3F_20[15:8]	7:0	See description of '2F52h'.	
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_5F_40[7:0]	7:0	Histogram report section3.	
2Ah	**REG2F55**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F55h)	TOTAL_5F_40[15:8]	7:0	See description of '2F54h'.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_7F_60[7:0]	7:0	Histogram report section4.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_7F_60[15:8]	7:0	See description of '2F56h'.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_9F_80[7:0]	7:0	Histogram report section5.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_9F_80[15:8]	7:0	See description of '2F58h'.	
2Dh (2F5Ah)	**REG2F5A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_BF_A0[7:0]	7:0	Histogram report section6.	
2Dh (2F5Bh)	**REG2F5B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_BF_A0[15:8]	7:0	See description of '2F5Ah'.	
2Eh (2F5Ch)	**REG2F5C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_DF_C0[7:0]	7:0	Histogram report section7.	
2Eh (2F5Dh)	**REG2F5D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_DF_C0[15:8]	7:0	See description of '2F5Ch'.	
2Fh (2F5Eh)	**REG2F5E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_FF_E0[7:0]	7:0	Histogram report section8.	
2Fh (2F5Fh)	**REG2F5F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_FF_E0[15:8]	7:0	See description of '2F5Eh'.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x18**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x28**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x38**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x48**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x58**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x68**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (2F67h)	**REG2F67**	**7:0**	**Default : 0x78**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x98**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0xA8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0xB0**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0xC8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0xE8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (2F6Fh)	**REG2F6F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
38h (2F70h)	**REG2F70**	**7:0**	**Default : 0x08**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_0[7:0]	7:0	Sub window curve table 0.	
38h (2F71h)	**REG2F71**	**7:0**	**Default : 0x18**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_1[7:0]	7:0	Sub window curve table 1.	
39h (2F72h)	**REG2F72**	**7:0**	**Default : 0x28**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_2[7:0]	7:0	Sub window curve table 2.	
39h (2F73h)	**REG2F73**	**7:0**	**Default : 0x38**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_3[7:0]	7:0	Sub window curve table 3.	
3Ah (2F74h)	**REG2F74**	**7:0**	**Default : 0x48**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_4[7:0]	7:0	Sub window curve table 4.	
3Ah (2F75h)	**REG2F75**	**7:0**	**Default : 0x58**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_5[7:0]	7:0	Sub window curve table 5.	
3Bh	**REG2F76**	**7:0**	**Default : 0x68**	**Access : R/W**

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
(2F76h)	SUB_CURVE_FIT_TABLE_6[7:0]	7:0	Sub window curve table 6.	
3Bh	**REG2F77**	**7:0**	**Default : 0x78**	**Access : R/W**
(2F77h)	SUB_CURVE_FIT_TABLE_7[7:0]	7:0	Sub window curve table 7.	
3Ch	**REG2F78**	**7:0**	**Default : 0x88**	**Access : R/W**
(2F78h)	SUB_CURVE_FIT_TABLE_8[7:0]	7:0	Sub window curve table 8.	
3Ch	**REG2F79**	**7:0**	**Default : 0x98**	**Access : R/W**
(2F79h)	SUB_CURVE_FIT_TABLE_9[7:0]	7:0	Sub window curve table 9.	
3Dh	**REG2F7A**	**7:0**	**Default : 0xA8**	**Access : R/W**
(2F7Ah)	SUB_CURVE_FIT_TABLE_10[7:0]	7:0	Sub window curve table 10.	
3Dh	**REG2F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
(2F7Bh)	SUB_CURVE_FIT_TABLE_11[7:0]	7:0	Sub window curve table 11.	
3Eh	**REG2F7C**	**7:0**	**Default : 0xC8**	**Access : R/W**
(2F7Ch)	SUB_CURVE_FIT_TABLE_12[7:0]	7:0	Sub window curve table 12.	
3Eh	**REG2F7D**	**7:0**	**Default : 0xD8**	**Access : R/W**
(2F7Dh)	SUB_CURVE_FIT_TABLE_13[7:0]	7:0	Sub window curve table 13.	
3Fh	**REG2F7E**	**7:0**	**Default : 0xE8**	**Access : R/W**
(2F7Eh)	SUB_CURVE_FIT_TABLE_14[7:0]	7:0	Sub window curve table 14.	
3Fh	**REG2F7F**	**7:0**	**Default : 0xF8**	**Access : R/W**
(2F7Fh)	SUB_CURVE_FIT_TABLE_15[7:0]	7:0	Sub window curve table 15.	
40h	**REG2F80**	**7:0**	**Default : 0x00**	**Access : RO**
(2F80h)	TOTAL_32_0[7:0]	7:0	Histogram report section 32_0.	
40h	**REG2F81**	**7:0**	**Default : 0x00**	**Access : RO**
(2F81h)	TOTAL_32_0[15:8]	7:0	See description of '2F80h'.	
41h	**REG2F82**	**7:0**	**Default : 0x00**	**Access : RO**
(2F82h)	TOTAL_32_1[7:0]	7:0	Histogram report section 32_1.	
41h	**REG2F83**	**7:0**	**Default : 0x00**	**Access : RO**
(2F83h)	TOTAL_32_1[15:8]	7:0	See description of '2F82h'.	
42h	**REG2F84**	**7:0**	**Default : 0x00**	**Access : RO**
(2F84h)	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.	
42h	**REG2F85**	**7:0**	**Default : 0x00**	**Access : RO**
(2F85h)	TOTAL_32_2[15:8]	7:0	See description of '2F84h'.	
43h	**REG2F86**	**7:0**	**Default : 0x00**	**Access : RO**
(2F86h)	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.	

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[15:8]	7:0	See description of '2F86h'.	
44h (2F88h)	**REG2F88**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.	
44h (2F89h)	**REG2F89**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[15:8]	7:0	See description of '2F88h'.	
45h (2F8Ah)	**REG2F8A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.	
45h (2F8Bh)	**REG2F8B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[15:8]	7:0	See description of '2F8Ah'.	
46h (2F8Ch)	**REG2F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.	
46h (2F8Dh)	**REG2F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[15:8]	7:0	See description of '2F8Ch'.	
47h (2F8Eh)	**REG2F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.	
47h (2F8Fh)	**REG2F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[15:8]	7:0	See description of '2F8Eh'.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.	
48h (2F91h)	**REG2F91**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[15:8]	7:0	See description of '2F90h'.	
49h (2F92h)	**REG2F92**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.	
49h (2F93h)	**REG2F93**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[15:8]	7:0	See description of '2F92h'.	
4Ah (2F94h)	**REG2F94**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.	
4Ah (2F95h)	**REG2F95**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_10[15:8]	7:0	See description of '2F94h'.	
4Bh (2F96h)	**REG2F96**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.	
4Bh	**REG2F97**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F97h)	TOTAL_32_11[15:8]	7:0	See description of '2F96h'.	
4Ch (2F98h)	**REG2F98**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.	
4Ch (2F99h)	**REG2F99**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[15:8]	7:0	See description of '2F98h'.	
4Dh (2F9Ah)	**REG2F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.	
4Dh (2F9Bh)	**REG2F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[15:8]	7:0	See description of '2F9Ah'.	
4Eh (2F9Ch)	**REG2F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.	
4Eh (2F9Dh)	**REG2F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[15:8]	7:0	See description of '2F9Ch'.	
4Fh (2F9Eh)	**REG2F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.	
4Fh (2F9Fh)	**REG2F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[15:8]	7:0	See description of '2F9Eh'.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[15:8]	7:0	See description of '2FA0h'.	
51h (2FA2h)	**REG2FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.	
51h (2FA3h)	**REG2FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[15:8]	7:0	See description of '2FA2h'.	
52h (2FA4h)	**REG2FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.	
52h (2FA5h)	**REG2FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[15:8]	7:0	See description of '2FA4h'.	
53h (2FA6h)	**REG2FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.	
53h (2FA7h)	**REG2FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[15:8]	7:0	See description of '2FA6h'.	

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
54h (2FA8h)	**REG2FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.	
54h (2FA9h)	**REG2FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[15:8]	7:0	See description of '2FA8h'.	
55h (2FAAh)	**REG2FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.	
55h (2FABh)	**REG2FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[15:8]	7:0	See description of '2FAAh'.	
56h (2FACh)	**REG2FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.	
56h (2FADh)	**REG2FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[15:8]	7:0	See description of '2FACh'.	
57h (2FAEh)	**REG2FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.	
57h (2FAFh)	**REG2FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[15:8]	7:0	See description of '2FAEh'.	
58h (2FB0h)	**REG2FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[15:8]	7:0	See description of '2FB0h'.	
59h (2FB2h)	**REG2FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.	
59h (2FB3h)	**REG2FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[15:8]	7:0	See description of '2FB2h'.	
5Ah (2FB4h)	**REG2FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.	
5Ah (2FB5h)	**REG2FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[15:8]	7:0	See description of '2FB4h'.	
5Bh (2FB6h)	**REG2FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[7:0]	7:0	Histogram report section 32_27.	
5Bh (2FB7h)	**REG2FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[15:8]	7:0	See description of '2FB6h'.	
5Ch	**REG2FB8**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FB8h)	TOTAL_32_28[7:0]	7:0	Histogram report section 32_28.	
5Ch (2FB9h)	**REG2FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[15:8]	7:0	See description of '2FB8h'.	
5Dh (2FBAh)	**REG2FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[7:0]	7:0	Histogram report section 32_29.	
5Dh (2FBBh)	**REG2FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[15:8]	7:0	See description of '2FBAh'.	
5Eh (2FBCh)	**REG2FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[7:0]	7:0	Histogram report section 32_30.	
5Eh (2FBDh)	**REG2FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[15:8]	7:0	See description of '2FBCh'.	
5Fh (2FBEh)	**REG2FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[7:0]	7:0	Histogram report section 32_31.	
5Fh (2FBFh)	**REG2FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[15:8]	7:0	See description of '2FBEh'.	
60h ~ 60h (2FC0h ~ 2FC1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
61h (2FC2h)	**REG2FC2**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MAX_PIXEL_SAT[7:0]	7:0	Main window minimum pixel saturation.	
61h (2FC3h)	**REG2FC3**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MIN_PIXEL_SAT[7:0]	7:0	Main window maximum pixel saturation.	
62h (2FC4h)	**REG2FC4**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MAX_PIXEL_SAT[7:0]	7:0	Sub window minimum pixel saturation.	
62h (2FC5h)	**REG2FC5**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MIN_PIXEL_SAT[7:0]	7:0	Sub window maximum pixel saturation.	
63h ~ 7Dh (2FC6h ~ 2FFBh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x01**	**Access : R/W**
	PIP_DISABLE	7	Disable PIP Function.	
	-	6:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	SW_SUB_EN	1	Enable sub window shown on the screen.	
	MAIN_EN	0	Enable main window shown on the screen.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	
	FBL_MASK_OVERLAP	5	Do not write overlapped portion of FBL channel to line buffer.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	FBL_SEL	4	Select FBL source. b0: Source F2 is FBL. b1: Source F1 is FBL.	
	VBLANK_SUB	3	Fill the sub windows line buffer in vertical blanking.	
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.	
	F2_IS_SUB	1	Set main window display on the foreground.	
	MAIN_IS_TOP	0	Set second channel display in sub-window.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x70**	**Access : R/W**
	-	7	Reserved.	
	EXTRA_POS[2:0]	6:4	Enable extra request at specified region. [0] Enable at bottom B session. [1] Enable at bottom A session. [2] Enable at top session.	
	EXTRA_TH_LN[3:0]	3:0	Enable extra request for overlapping when the jumping line less than this threshold.	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x07**	**Access : R/W**
	EXTRA_EN	7	Enable extra request engine.	
	VBLANK_OVL	6	Doing the extra request in vertical blanking.	
	EXTRA_Y_HALF	5	Reduce the extra_y to half.	
	-	4:3	Reserved.	
	BO_LENGTH[2:0]	2:0	Select the length of extra request. h0: 16 pixel. h1: 32 pixel. h2: 64 pixel. h3: 128 pixel. h4: (overlap length) / 8. h5: (overlap length) / 4. h6: (overlap length) / 2. h7: (overlap length).	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F2[7:0]	7:0	The starting address of f2 stored at line buffer.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F2[11:8]	3:0	See description of '2F24h'.	
13h	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F26h)	SCLB_BASE_F1[7:0]	7:0	The starting address of f1 stored at line buffer.	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F1[11:8]	3:0	See description of '2F26h'.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BA_RIGHT[7:0]	7:0	Extend the pixel of bottom A session at the right side.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BB_LEFT[7:0]	7:0	Extend the pixel of bottom B session at the left side.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F2[11:8]	3:0	See description of '2F2Ah'.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F1[7:0]	7:0	Set the maximum request lines for first channel.	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F1[11:8]	3:0	See description of '2F2Ch'.	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXT_SUB_BORDER[3:0]	7:4	Extend the specified line in sub window to insert additional border.	
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional border.	
17h (2F2Fh)	**REG2F2F**	**7:0**	**Default : 0x02**	**Access : R/W**
	EXTRA_ADV_LINE[3:0]	7:4	Advance the specified lines of extra end line (2's complement).	
	EXTRA_FETCH_LINE[3:0]	3:0	How many line will be fetched by extra request. Minimum is 1.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ATP_EN	0	Manual tune parameter.	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x38**	**Access : R/W**
	-	7	Reserved.	
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Vsync of SC_TOP. 1: Delay one line of vfde.	
	SEL_DISP[1:0]	5:4	Select the trig point to start op1 engine. h0: Down_eq7. h1: Down_eq8. h2: Down_eq9. h3: Delay lines set by disp_trig_dly.	
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. h0: Falling edge of vsync. h1: Nearly raising edge of vsync. h2: Delay line set by atp_trig_dly. h3: Manual trig by set atp_en.	
	SEL_SYNC[1:0]	1:0	Select the trig point for sync to initial engine. h0: Falling edge of vsync. h1: Raising edge of vsync. h2: Reserved. h3: Reserved.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x03**	**Access : R/W**
	ATP_TRIG_DLY[7:0]	7:0	Generate train_trig_p from delayed line of vsync.	
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ATP_TRIG_DLY[11:8]	3:0	See description of '2F34h'.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x05**	**Access : R/W**
	DISP_TRIG_DLY[7:0]	7:0	Generate disp_trig_p from delayed line of vsync.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '2F36h'.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (2F39h)	**REG2F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (2F3Ah)	**REG2F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F1[7:0]	7:0	Offset line buffer position of F1 in right direction.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIN_OVERLAP_TH[7:0]	7:0	Threshold of overlapped length. Extra_eq will be disabled when overlapped length less then this threshold.	
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIN_OVERLAP_CNT[7:0]	7:0	Stop count between two extra request.	
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0xC2**	**Access : R/W**
	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. h0: 2 pixel. h1: 4 pixel. h2: 8 pixel. h3: 16 pixel.	
	DISP_START_MODE	5	Select the display line buffer start mode. 0: Start at advance 1 display line. 1: Start at falling edge of vsync_init.	
	DISP_LB_MODE	4	Select the trig mode. 0: Line base. 1: Fill line buffer.	
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. h0: Before 8 pixel. h1: Before 16 pixel. h2: Before 32 pixel. h3: Before 64 pixel.	
	DISP_RUN_MODE[1:0]	1:0	Select the under_run value of display level. h0: Update by hsync (not optimum performance). h1: Update when session done(may error). h2: Update when line done(disp_trig_mode = 0). h3: Reserved.	
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_UNDER_MODE	3	Select the under_run value of display level. 0: 16'h0000. 1: 16'hffff.	
	DISP_PAT_EN	2	Enable internal pattern of op1_disp.	
	DISP_LB_WEZ	1	Disable wen of display line buffer.	
	DISP_TRIG_MODE	0	Select the trig mode. 0: Trigged by self_counter.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Trigged by op2.	
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.	
20h (2F41h)	**REG2F41**	**7:0**	**Default : 0x07**	**Access : R/W**
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '2F40h'.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FLAG_BB_ADR_INI	2	Status of cnt_bb_adr_ini, write 1 to switch back to hardware. h0: Calculated by hardware. h1: Written by software.	
	FLAG_BO_END_LN	1	Status of line_base_bot, write 1 to switch back to hardware. h0: Calculated by hardware. h1: Written by software.	
	-	0	Reserved.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BO_END_LN[7:0]	7:0	Software mode to set the line_base_bot for extra request.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_BO_END_LN[11:8]	3:0	See description of '2F62h'.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BB_ADR_INI[7:0]	7:0	Software mode to set the cnt_bb_adr_ini.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_BB_ADR_INI[11:8]	3:0	See description of '2F64h'.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	DISPLAY_UNDERRUN	0	Indicate that the display line buffer is underrun in previous frame.	
41h (2F82h)	**REG2F82**	**7:0**	**Default : 0x00**	**Access : RO**
	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line cnt of first display position.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '2F82h'.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line cnt of minimum display level occure.	
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	MIN_DISP_LINE[11:8]	3:0	See description of '2F84h'.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.	
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[15:8]	7:0	See description of '2F86h'.	
44h (2F88h)	**REG2F88**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.	
44h (2F89h)	**REG2F89**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[15:8]	7:0	See description of '2F88h'.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_ADR_INI[7:0]	7:0	Read SCLB_TF_ADR_INI.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_ADR_INI[11:8]	3:0	See description of '2FA0h'.	
51h (2FA2h)	**REG2FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.	
51h (2FA3h)	**REG2FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '2FA2h'.	
52h (2FA4h)	**REG2FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_ADR_INI[7:0]	7:0	Read SCLB_BB_ADR_INI.	
52h (2FA5h)	**REG2FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_ADR_INI[11:8]	3:0	See description of '2FA4h'.	
53h (2FA6h)	**REG2FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BO_ADR_INI[7:0]	7:0	Read SCLB_BO_ADR_INI.	
53h (2FA7h)	**REG2FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCLB_BO_ADR_INI[11:8]	3:0	See description of '2FA6h'.	
54h (2FA8h)	**REG2FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_LEN[7:0]	7:0	Read SCLB_TF_LEN.	
54h (2FA9h)	**REG2FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_LEN[11:8]	3:0	See description of '2FA8h'.	
55h (2FAAh)	**REG2FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.	
55h (2FABh)	**REG2FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BF_LEN[11:8]	3:0	See description of '2FAAh'.	
56h (2FACh)	**REG2FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_LEN[7:0]	7:0	Read SCLB_BA_LEN.	
56h (2FADh)	**REG2FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_LEN[11:8]	3:0	See description of '2FACh'.	
57h (2FAEh)	**REG2FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_LEN[7:0]	7:0	Read SCLB_BB_LEN.	
57h (2FAFh)	**REG2FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_LEN[11:8]	3:0	See description of '2FAEh'.	
58h (2FB0h)	**REG2FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1A[7:0]	7:0	Read FETCH_NUM_F1A.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1A[11:8]	3:0	See description of '2FB0h'.	
59h (2FB2h)	**REG2FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1B[7:0]	7:0	Read FETCH_NUM_F1B.	
59h (2FB3h)	**REG2FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1B[11:8]	3:0	See description of '2FB2h'.	
5Ah (2FB4h)	**REG2FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2A[7:0]	7:0	Read FETCH_NUM_F2A.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
5Ah (2FB5h)	**REG2FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2A[11:8]	3:0	See description of '2FB4h'.	
5Bh (2FB6h)	**REG2FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2B[7:0]	7:0	Read FETCH_NUM_F2B.	
5Bh (2FB7h)	**REG2FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2B[11:8]	3:0	See description of '2FB6h'.	
5Ch (2FB8h)	**REG2FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_OFFSET_B[7:0]	7:0	Read FETCH_OFFSET_B.	
5Ch (2FB9h)	**REG2FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_OFFSET_B[11:8]	3:0	See description of '2FB8h'.	
5Dh (2FBAh)	**REG2FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_LENGTH_RD[7:0]	7:0	Read bo_length.	
5Dh (2FBBh)	**REG2FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_LENGTH_RD[11:8]	3:0	See description of '2FBAh'.	
5Eh (2FBCh)	**REG2FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_START_LN[7:0]	7:0	Read BO_START_LN.	
5Eh (2FBDh)	**REG2FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_START_LN[11:8]	3:0	See description of '2FBCh'.	
5Fh (2FBEh)	**REG2FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_END_LN[7:0]	7:0	Read BO_END_LN.	
5Fh (2FBFh)	**REG2FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_END_LN[11:8]	3:0	See description of '2FBEh'.	
60h (2FC0h)	**REG2FC0**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_ADR_INI[7:0]	7:0	Read DISP_TF_ADR_INI.	
60h (2FC1h)	**REG2FC1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_ADR_INI[11:8]	3:0	See description of '2FC0h'.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
61h (2FC2h)	**REG2FC2**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (2FC3h)	**REG2FC3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '2FC2h'.	
62h (2FC4h)	**REG2FC4**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_ADR_INI[7:0]	7:0	Read DISP_BB_ADR_INI.	
62h (2FC5h)	**REG2FC5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_ADR_INI[11:8]	3:0	See description of '2FC4h'.	
63h (2FC6h)	**REG2FC6**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_LEN[7:0]	7:0	Read DISP_TF_LEN.	
63h (2FC7h)	**REG2FC7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_LEN[11:8]	3:0	See description of '2FC6h'.	
64h (2FC8h)	**REG2FC8**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h (2FC9h)	**REG2FC9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '2FC8h'.	
65h (2FCAh)	**REG2FCA**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_LEN[7:0]	7:0	Read DISP_BA_LEN.	
65h (2FCBh)	**REG2FCB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_LEN[11:8]	3:0	See description of '2FCAh'.	
66h (2FCCh)	**REG2FCC**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_LEN[7:0]	7:0	Read DISP_BB_LEN.	
66h (2FCDh)	**REG2FCD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_LEN[11:8]	3:0	See description of '2FCCh'.	
67h (2FCEh)	**REG2FCE**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPR_BB_ADR_INI[7:0]	7:0	Read HSPR_BB_ADR_INI.	
67h	**REG2FCF**	**7:0**	**Default : 0x00**	**Access : RO**

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2FCFh)	-	7:4	Reserved.
	HSPR_BB_ADR_INI[11:8]	3:0	See description of '2FCEh'.

ELA Register (Bank = 2F, Sub-Bank = 21)

ELA Register (Bank = 2F, Sub-Bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. 1: Enable. 0: Disable.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F1	0	F1 window EODi enable. 1: Enable. 0: Disable.	
7Fh ~ 7Fh	**-**	**7:0**	**Default : -**	**Access : -**

ELA Register (Bank = 2F, Sub-Bank = 21)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(2FFEh ~ 2FFFh)	-	-	Reserved.

TDDI Register (Bank = 2F, Sub-Bank = 22)

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x04**	**Access : R/W**
	RATIO_DIV_YCSEP_F2	7	Main window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F2[2:0]	2:0	Main window ratio divide mode when Y/C separate.	
01h (2F03h)	**REG2F03**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F2[2:0]	5:3	Main window ratio divide mode.	
	RATIO_MD_F2[2:0]	2:0	Main window ratio filter mode.	
02h	**REG2F04**	**7:0**	**Default : 0x80**	**Access : R/W**

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F04h)	RATIO_C_INDEP_F2	7	Main window C ratio independent mode. 0: Disable C ratio filter. 1: Enable C ratio filter.	
	RSV_02_2_F2[2:0]	6:4	Reserved.	
	RATIO_C_MIN_F2[3:0]	3:0	Main window C minimum ratio in independent mode.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x02**	**Access : R/W**
	RSV_02_0_F2[2:0]	7:5	Reserved.	
	-	4	Reserved.	
	RSV_02_1_F2[1:0]	3:2	Reserved.	
	RATIO_C_YMAX_SEL_F2	1	Main window C ratio takes Y ratio mode. 0: Select Y ratio before SST. 1: Select Y ratio after SST.	
	RATIO_C_YMAX_DIS_F2	0	Main window C ratio takes Y ratio mode disable. 0: Enable. 1: Disable.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_MOT_FILTER_EN_F2	7	Main Window LPF enable of DNR motion calculation.	
	-	6	Reserved.	
	PRE_MOT_OFFSET_F2[5:0]	5:0	Main Window pre-memory motion offset for motion calculation.	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_MOT_GAIN_F2[3:0]	3:0	Main Window pre-memory motion gain for motion calculation.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F2[5:0]	5:0	Main Window post-memory motion offset for motion calculation.	
09h (2F13h)	**REG2F13**	**7:0**	**Default : 0x88**	**Access : R/W**
	POST_MOT_CGAIN_F2[3:0]	7:4	Main Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F2[3:0]	3:0	Main Window post-memory motion gain for C motion calculation.	
0Ah	**REG2F14**	**7:0**	**Default : 0x86**	**Access : R/W**

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F14h)	POST_MOT_YMAX_EN_F2	7	Main Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F2[2:0]	2:0	Main Window history weighting.	
0Ah (2F15h)	**REG2F15**	**7:0**	**Default : 0x04**	**Access : R/W**
	HIS_FILTER_MODE_F2	7	Main Window history filter mode.	
	-	6:4	Reserved.	
	HIS_RATIO_OFFSET_F2[3:0]	3:0	Main Window history ratio offset.	
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0x07**	**Access : R/W**
	RSV_STAT_0_F2[1:0]	7:6	Reserved.	
	STAT_INC_MODE_F2	5	Main window ratio statistics: Ratio incremental mode.	
	STAT_SEL_C_F2	4	Main window ratio statistics: Ratio selection.	
	STAT_CORE_F2[3:0]	3:0	Main window ratio statistics: Coring threshold.	
0Dh (2F1Ah)	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[7:0]	7:0	Main window ratio statistics: Motion status.	
0Dh (2F1Bh)	**REG2F1B**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[15:8]	7:0	See description of '2F1Ah'.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[23:16]	7:0	See description of '2F1Ah'.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ADAPT_MED_EN_F2	7	Main window adaptive DFK enable.	
	WEGT_MED_EN_F2	6	Main window weighted DFK enable.	
	RSV_MED_0_F2	5	Reserved.	
	MED_MANUAL_EN_F2	4	Main window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F2[3:0]	3:0	Main window DFK manual weighting.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F2[4:0]	4:0	Main window weighted DFK low-frequency begin.	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F2[3:0]	3:0	Main window weighted DFK low-frequency slope adjustment.	
12h	**REG2F24**	**7:0**	**Default : 0x14**	**Access : R/W**

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F24h)	-	7:5	Reserved.	
	MED_HF_BEGIN_F2[4:0]	4:0	Main window weighted DFK high-frequency begin.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F2[3:0]	3:0	Main window weighted DFK high-frequency slope adjustment.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F2[5:0]	5:0	Main window adaptive DFK motion threshold.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x13**	**Access : R/W**
	SST_EN_F2	7	Main window SST enable.	
	FILM_SST_EN_F2	6	Main window enable SST in film mode.	
	RSV_SST_0_F2	5	Reserved.	
	SST_MOTION_LPF_EN_F2	4	Main window SST low-pass on motion enable.	
	SST_MOTION_TH_F2[3:0]	3:0	Main window SST motion threshold.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x27**	**Access : R/W**
	RSV_SST_1_F2[1:0]	7:6	Reserved.	
	SST_ERODE_MODE_F2[1:0]	5:4	Main window SST motion area erosion mode.	
	RSV_SST_2_F2	3	Reserved.	
	SST_DILATE_MODE_F2[2:0]	2:0	Main window SST motion area dilation mode.	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0xDF**	**Access : R/W**
	SST_POSTLPF_EN_F2	7	Main window SST post-LPF enable.	
	SST_POSTLPF_MAX_F2	6	Main window SST post-LPF maximum function enable.	
	SST_DYNAMIC_CORE_TH_F2[5:0]	5:0	Main window SST dynamic motion coring threshold.	
19h (2F33h)	**REG2F33**	**7:0**	**Default : 0x85**	**Access : R/W**
	SST_DYNAMIC_SGAIN_F2[3:0]	7:4	Main window SST dynamic motion spatial difference gain.	
	SST_DYNAMIC_TGAIN_F2[3:0]	3:0	Main window SST dynamic motion temporal difference gain.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSV_SST_3_F2[1:0]	7:6	Reserved.	
	SST_STATIC_CORE_TH_F2[5:0]	5:0	Main window SST static motion coring threshold.	
1Ah	**REG2F35**	**7:0**	**Default : 0x22**	**Access : R/W**

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F35h)	SST_STATIC_SGAIN_F2[3:0]	7:4	Main window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F2[3:0]	3:0	Main window SST static motion temporal difference gain.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSV_SST_4_F2[7:0]	7:0	Reserved.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x04**	**Access : R/W**
	RATIO_DIV_YCSEP_F1	7	Sub window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F1[2:0]	2:0	Sub window ratio divide mode when Y/C separate.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F1[2:0]	5:3	Sub window ratio divide mode.	
	RATIO_MD_F1[2:0]	2:0	Sub window ratio filter mode.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0x80**	**Access : R/W**
	RATIO_C_INDEP_F1	7	Sub window C ratio independent mode. 0: Disable C ratio filter. 1: Enable C ratio filter.	
	RSV_02_2_F1[2:0]	6:4	Reserved.	
	RATIO_C_MIN_F1[3:0]	3:0	Sub window C minimum ratio in independent mode.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x02**	**Access : R/W**
	RSV_02_0_F1[2:0]	7:5	Reserved.	
	-	4	Reserved.	
	RSV_02_1_F1[1:0]	3:2	Reserved.	
	RATIO_C_YMAX_SEL_F1	1	Sub window C ratio takes Y ratio mode. 0: Select Y ratio before SST. 1: Select Y ratio after SST.	
	RATIO_C_YMAX_DIS_F1	0	Sub window C ratio takes Y ratio mode disable. 0: Enable. 1: Disable.	
38h (2F70h)	**REG2F70**	**7:0**	**Default : 0x03**	**Access : R/W**
	PRE_MOT_FILTER_EN_F1	7	Sub Window LPF enable of DNR motion calculation.	
	-	6	Reserved.	
	PRE_MOT_OFFSET_F1[5:0]	5:0	Sub Window pre-memory motion offset for motion calculation.	
38h	**REG2F71**	**7:0**	**Default : 0x08**	**Access : R/W**

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F71h)	-	7:4	Reserved.	
	PRE_MOT_GAIN_F1[3:0]	3:0	Sub Window pre-memory motion gain for motion calculation.	
39h (2F72h)	**REG2F72**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F1[5:0]	5:0	Sub Window post-memory motion offset for motion calculation.	
39h (2F73h)	**REG2F73**	**7:0**	**Default : 0x88**	**Access : R/W**
	POST_MOT_CGAIN_F1[3:0]	7:4	Sub Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F1[3:0]	3:0	Sub Window post-memory motion gain for C motion calculation.	
3Ah (2F74h)	**REG2F74**	**7:0**	**Default : 0x86**	**Access : R/W**
	POST_MOT_YMAX_EN_F1	7	Sub Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F1[2:0]	2:0	Sub Window history weighting.	
3Ah (2F75h)	**REG2F75**	**7:0**	**Default : 0x04**	**Access : R/W**
	HIS_FILTER_MODE_F1	7	Sub Window history filter mode.	
	-	6:4	Reserved.	
	HIS_RATIO_OFFSET_F1[3:0]	3:0	Sub Window history ratio offset.	
3Ch (2F78h)	**REG2F78**	**7:0**	**Default : 0x07**	**Access : R/W**
	RSV_STAT_0_F1[1:0]	7:6	Reserved.	
	STAT_INC_MODE_F1	5	Sub window ratio statistics: Ratio incremental mode.	
	STAT_SEL_C_F1	4	Sub window ratio statistics: Ratio selection.	
	STAT_CORE_F1[3:0]	3:0	Sub window ratio statistics: Coring threshold.	
3Dh (2F7Ah)	**REG2F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F1[7:0]	7:0	Sub window ratio statistics: Motion status.	
3Dh (2F7Bh)	**REG2F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F1[15:8]	7:0	See description of '2F7Ah'.	
3Eh (2F7Ch)	**REG2F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F1[23:16]	7:0	See description of '2F7Ah'.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ADAPT_MED_EN_F1	7	Sub window adaptive DFK enable.	

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	WEGT_MED_EN_F1	6	Sub window weighted DFK enable.	
	RSV_MED_0_F1	5	Reserved.	
	MED_MANUAL_EN_F1	4	Sub window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F1[3:0]	3:0	Sub window DFK manual weighting.	
41h (2F82h)	**REG2F82**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F1[4:0]	4:0	Sub window weighted DFK low-frequency begin.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F1[3:0]	3:0	Sub window weighted DFK low-frequency slope adjustment.	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	MED_HF_BEGIN_F1[4:0]	4:0	Sub window weighted DFK high-frequency begin.	
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F1[3:0]	3:0	Sub window weighted DFK high-frequency slope adjustment.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F1[5:0]	5:0	Sub window adaptive DFK motion threshold.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x13**	**Access : R/W**
	SST_EN_F1	7	Sub window SST enable.	
	FILM_SST_EN_F1	6	Sub window enable SST in film mode.	
	RSV_SST_0_F1	5	Reserved.	
	SST_MOTION_LPF_EN_F1	4	Sub window SST low-pass on motion enable.	
	SST_MOTION_TH_F1[3:0]	3:0	Sub window SST motion threshold.	
48h (2F91h)	**REG2F91**	**7:0**	**Default : 0x27**	**Access : R/W**
	RSV_SST_1_F1[1:0]	7:6	Reserved.	
	SST_ERODE_MODE_F1[1:0]	5:4	Sub window SST motion area erosion mode.	
	RSV_SST_2_F1	3	Reserved.	
	SST_DILATE_MODE_F1[2:0]	2:0	Sub window SST motion area dilation mode.	
49h	**REG2F92**	**7:0**	**Default : 0xDF**	**Access : R/W**

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F92h)	SST_POSTLPF_EN_F1	7	Sub window SST post-LPF enable.	
	SST_POSTLPF_MAX_F1	6	Sub window SST post-LPF maximum function enable.	
	SST_DYNAMIC_CORE_TH_F1[5:0]	5:0	Sub window SST dynamic motion coring threshold.	
49h (2F93h)	**REG2F93**	**7:0**	**Default : 0x85**	**Access : R/W**
	SST_DYNAMIC_SGAIN_F1[3:0]	7:4	Sub window SST dynamic motion spatial difference gain.	
	SST_DYNAMIC_TGAIN_F1[3:0]	3:0	Sub window SST dynamic motion temporal difference gain.	
4Ah (2F94h)	**REG2F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSV_SST_3_F1[1:0]	7:6	Reserved.	
	SST_STATIC_CORE_TH_F1[5:0]	5:0	Sub window SST static motion coring threshold.	
4Ah (2F95h)	**REG2F95**	**7:0**	**Default : 0x22**	**Access : R/W**
	SST_STATIC_SGAIN_F1[3:0]	7:4	Sub window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F1[3:0]	3:0	Sub window SST static motion temporal difference gain.	
4Bh (2F96h)	**REG2F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSV_SST_4_F1[7:0]	7:0	Reserved.	
7Ch ~ 7Fh (2FF8h ~ 2FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-		Reserved.	

HVSP Register (Bank = 2F, Sub-Bank = 23)

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (2F03h)	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '2F02h'.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '2F02h'.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '2F06h'.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '2F06h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '2F0Ah'.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '2F0Ah'.	
07h (2F0Eh)	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '2F0Eh'.	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.	
09h (2F13h)	**REG2F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '2F12h'.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '2F12h'.	
0Ah (2F15h)	**REG2F15**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.	
0Bh (2F16h)	**REG2F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.	

HVSP Register (Bank = 2F, Sub-Bank = 23)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.
0Bh (2F17h)	**REG2F17**	**7:0**	**Default : 0x00** **Access : R/W**
	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0xC0** **Access : R/W**
	FORMAT_422_F2	7	Main window data format is 422.
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.
	CR_LOAD_INI_F2	5	Main Cr_load initial value.
	-	4:2	Reserved.

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.	
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.	
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.	
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.	
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.	
0Dh (2F1Ah)	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.	
0Dh (2F1Bh)	**REG2F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F2[7:0]	7:0	Main window horizontal Y coring threshold.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.	
0Eh (2F1Dh)	**REG2F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.	
0Fh (2F1Eh)	**REG2F1E**	**7:0**	**Default : 0x38**	**Access : R/W**
	HSP_DE_RING_G_ON_F2	7	Main window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F2[2:0]	6:4	Main window horizontal de-ringing threshold1.	
	HSP_DE_RING_TH0_F2[3:0]	3:0	Main window horizontal de-ringing threshold0.	
0Fh (2F1Fh)	**REG2F1F**	**7:0**	**Default : 0x58**	**Access : R/W**
	HSP_DE_RING_RB_ON_F2	7	Main window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F2[2:0]	6:4	Main window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F2[3:0]	3:0	Main window horizontal de-ringing threshold2.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET_F2[7:0]	7:0	Main window horizontal de-ringing offset.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET2_F2[7:0]	7:0	Main window horizontal de-ringing offset2.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x38**	**Access : R/W**
	VSP_DE_RING_G_ON_F2	7	Main window vertical Y de-ringing enable.	
	VSP_DE_RING_TH1_F2[2:0]	6:4	Main window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F2[3:0]	3:0	Main window vertical de-ringing threshold0.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (2F23h)	**REG2F23**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSP_DE_RING_RB_ON_F2	7	Main window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F2[2:0]	6:4	Main window vertical de-ringing threshold3.	
	VSP_DE_RING_TH2_F2[3:0]	3:0	Main window vertical de-ringing threshold2.	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET_F2[7:0]	7:0	Main window vertical de-ringing offset.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET2_F2[7:0]	7:0	Main window vertical de-ringing offset2.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.	
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F2	1	Main window field polarity switch.	
	2_INIFAC_MD_F2	0	Main window two initial factors mode.	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width0 LSB.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width0.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width1.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width2.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.	
17h (2F2Eh)	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width0.	
17h (2F2Fh)	**REG2F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width1.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width2.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.	
19h (2F33h)	**REG2F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[7:0]	7:0	Sub window horizontal initial factor.	
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[15:8]	7:0	See description of '2F42h'.	
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:4	Reserved.	
	INI_FACTOR_HO_F1[19:16]	3:0	See description of '2F42h'.	
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[7:0]	7:0	Sub window vertical initial factor 1.	
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[15:8]	7:0	See description of '2F46h'.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[23:16]	7:0	See description of '2F46h'.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[7:0]	7:0	Sub window vertical initial factor 2.	
25h (2F4Bh)	**REG2F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[15:8]	7:0	See description of '2F4Ah'.	
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[23:16]	7:0	See description of '2F4Ah'.	
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[7:0]	7:0	Sub window horizontal scaling factor.	
27h (2F4Fh)	**REG2F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[15:8]	7:0	See description of '2F4Eh'.	
28h (2F50h)	**REG2F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[23:16]	7:0	See description of '2F4Eh'.	
28h (2F51h)	**REG2F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F1	0	Sub window horizontal scaling enable.	
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[7:0]	7:0	Sub window vertical scaling factor.	
29h (2F53h)	**REG2F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[15:8]	7:0	See description of '2F52h'.	
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[23:16]	7:0	See description of '2F52h'.	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F1	7	Sub window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F1	0	Sub window vertical scaling enable.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F1	7	Sub window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F1	6	Sub window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F1	5	Sub window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F1	4	Sub window horizontal C scaling filter SRAM usage enable.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MODE_C_HO_F1[2:0]	3:1	Sub window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F1	0	Sub window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F1	7	Sub window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F1	6	Sub window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F1	5	Sub window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F1	4	Sub window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F1[2:0]	3:1	Sub window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F1	0	Sub window vertical Y scaling filter selection. (valid value:0-8).	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F1	7	Sub window data format is 422.	
	422_INTP_F1	6	Sub window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F1	5	Sub Cr_load initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F1	1	Sub window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F1	0	Sub window dithering enable for horizontal scaling process.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VSP_CORING_EN_Y_F1	3	Sub window vertical Y coring enable.	
	VSP_CORING_EN_C_F1	2	Sub window vertical C coring enable.	
	HSP_CORING_EN_Y_F1	1	Sub window horizontal Y coring enable.	
	HSP_CORING_EN_C_F1	0	Sub window horizontal C coring enable.	
2Dh (2F5Ah)	**REG2F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F1[7:0]	7:0	Sub window horizontal C coring threshold.	
2Dh (2F5Bh)	**REG2F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F1[7:0]	7:0	Sub window horizontal Y coring threshold.	
2Eh (2F5Ch)	**REG2F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F1[7:0]	7:0	Sub window vertical C coring threshold.	
2Eh (2F5Dh)	**REG2F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F1[7:0]	7:0	Sub window vertical Y coring threshold.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F1	7	Sub window vertical nonlinear scaling enable.	
	H_NL_EN_F1	6	Sub window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F1	3	Sub window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F1	2	Sub window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F1	1	Sub window field polarity switch.	
	2_INIFAC_MD_F1	0	Sub window two initial factors mode.	
33h (2F67h)	**REG2F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	V_NL_W2_LSB_F1	6	Sub window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F1	5	Sub window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F1	4	Sub window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F1	2	Sub window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F1	1	Sub window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F1	0	Sub window horizontal nonlinear scaling width0 LSB.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width0.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width1.	
35h (2F6Ah)	**REG2F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F1[7:0]	7:0	Sub window horizontal nonlinear scaling width2.	
35h (2F6Bh)	**REG2F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F1	7	Sub window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F1[6:0]	6:0	Sub window horizontal nonlinear scaling initial value.	
36h (2F6Ch)	**REG2F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F1[7:0]	7:0	Sub window horizontal nonlinear scaling delta 0.	
36h (2F6Dh)	**REG2F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F1[7:0]	7:0	Sub window horizontal nonlinear scaling delta 1.	
37h (2F6Eh)	**REG2F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F1[7:0]	7:0	Sub window vertical nonlinear scaling width0.	
37h (2F6Fh)	**REG2F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F1[7:0]	7:0	Sub window vertical nonlinear scaling width1.	
38h (2F70h)	**REG2F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F1[7:0]	7:0	Sub window vertical nonlinear scaling width2.	
38h (2F71h)	**REG2F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F1	7	Sub window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F1[6:0]	6:0	Sub window vertical nonlinear scaling initial value.	
39h (2F72h)	**REG2F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F1[7:0]	7:0	Sub window vertical nonlinear scaling delta 0.	
39h (2F73h)	**REG2F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F1[7:0]	7:0	Sub window vertical nonlinear scaling delta 1.	
41h (2F82h)	**REG2F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RAM_RW_EN	0	SRAM read/write enable.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RAM_W_PULSE	0	SRAM write data pulse.	
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_ADDR[7:0]	7:0	SRAM read/write address. 0: Address 0~127.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Address 128~255.	
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	YRAM_UPPER_SEL	0	SRAM upper address selection.	
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[7:0]	7:0	SRAM write data.	
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[15:8]	7:0	See description of '2F86h'.	
44h (2F88h)	**REG2F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[23:16]	7:0	See description of '2F86h'.	
44h (2F89h)	**REG2F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[31:24]	7:0	See description of '2F86h'.	
45h (2F8Ah)	**REG2F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[39:32]	7:0	See description of '2F86h'.	
46h (2F8Ch)	**REG2F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[7:0]	7:0	SRAM read data.	
46h (2F8Dh)	**REG2F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[15:8]	7:0	See description of '2F8Ch'.	
47h (2F8Eh)	**REG2F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[23:16]	7:0	See description of '2F8Ch'.	
47h (2F8Fh)	**REG2F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[31:24]	7:0	See description of '2F8Ch'.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[39:32]	7:0	See description of '2F8Ch'.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ROM_RESULT_MUX[2:0]	2:0	ROM data out selection when ROM BIST enable.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	COEF_ROM_RDATA[7:0]	7:0	SRAM read-out data.	
51h (2FA2h)	**REG2FA2**	**7:0**	**Default : 0x41**	**Access : R/W**
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.	
	FACTOR_MANUAL	6	Vertical factor manual mode.	
	VDOWN_SEL	5	Vertical scaling down selection.	

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Bottom. 1: Top.	
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.	
	-	3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.	
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.	
52h (2FA5h)	**REG2FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish. 1: DE end.	
	-	6:0	Reserved.	
58h ~ 5Fh (2FB0h ~ 2FBFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

FRC Register (Bank = 2F, Sub-Bank = 24)

FRC Register (Bank = 2F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
3Fh (2F7Eh)	**REG2F7E**	**7:0**	**Default : 0x1B**	**Access : R/W**
	-	7:5	Reserved.	
	TAILCUT	4	TAILCUT enable.	
	NOISE_DITH_DISABLE	3	PAFRC mixed with noise dither disable. 0: Enable. 1: Disable.	
	DITH_BITS	2	Dithering bits. 0: 2-bits. 1: 4-bits.	

FRC Register (Bank = 2F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TCON_OFF_EN	1	TCON FRC_GAMMA function off signal enable. 0: Ignore TCON gamma/dither turn off signal. 1: Gamma/dither function turn off by TCON FRC_GAMMA_OFF signal.	
	FRC_ON	0	PAFRC enable.	
40h (2F80h)	**REG2F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_ROTATE_EN	7	Box A/B/C/D relation rotation enable.	
	TOP_BOX_UNIT_FLAG[1:0]	6:5	Top box A/B/C/D swap flag. 00: Per 2x2 box. 01: Per 4x4 box. 1x: Per 8x8 box.	
	TOP_BOX_FREEZE	4	Top box freeze.	
	TOP_BOX_SHRINK	3	Top box shrink to 2x2 from 4x4.	
	FR_C2_BIT	2	Top box frame rotation step bit location for codexx10. 0: Bit[0]. 1: Bit[1].	
	C2X2_ROT_B_DIR_S	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_B_DIR_S	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
40h (2F81h)	**REG2F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	G_V_SWAP	6	Green channel vertical swap, avoid polarity not consistent.	
	G_H_SWAP	5	Green channel horizontal swap, avoid polarity not consistent.	
	B_D_SWAP	4	Blue channel diagonal swap.	
	BOX_FR_SW	3	FRAME_CNT bit [1:0] swap for box rotate.	
	BOX4X4_FR_SW	2	FRAME_CNT bit [1:0] swap for box4x4 rotate.	
	BOX8X8_ROT_UNIT	1	0: Rotate step under per A, B, C or D. 1: Rotate step between A/B/C/D.	
	BOX_FREEZE	0	Box local rotation freeze.	
41h	**REG2F82**	**7:0**	**Default : 0x00**	**Access : R/W**

FRC Register (Bank = 2F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F82h)	C2X2_ROT_G_DIR	7	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_G_DIR	6	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_G_DIR_S	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_G_DIR_S	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	A2X2_ROT_B_DIR	3	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_B_DIR	2	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_B_DIR	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_B_DIR	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
41h (2F83h)	**REG2F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	A2X2_ROT_R_DIR	7	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_R_DIR	6	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_R_DIR	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_R_DIR	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	

FRC Register (Bank = 2F, Sub-Bank = 24)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	C2X2_ROT_R_DIR_S	3	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.
	D2X2_ROT_R_DIR_S	2	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.
	A2X2_ROT_G_DIR	1	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.
	B2X2_ROT_G_DIR	0	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.
42h (2F84h)	**REG2F84**	**7:0**	**Default : 0x00** **Access : R/W**
	TOP_BOX_FR_SEQ2[7:0]	7:0	Top box frame 2nd 4 frame rotation step.
42h (2F85h)	**REG2F85**	**7:0**	**Default : 0x00** **Access : R/W**
	TOP_BOX_FR_SEQ1[7:0]	7:0	Top box frame 1st 4 frame rotation step.
43h (2F86h)	**REG2F86**	**7:0**	**Default : 0x00** **Access : R/W**
	TOP_BOX_FR_SEQ4[7:0]	7:0	Top box frame 4th 4 frame rotation step.
43h (2F87h)	**REG2F87**	**7:0**	**Default : 0x00** **Access : R/W**
	TOP_BOX_FR_SEQ3[7:0]	7:0	Top box frame 3rd 4 frame rotation step.
44h (2F88h)	**REG2F88**	**7:0**	**Default : 0x00** **Access : R/W**
	TOP_BOX_FR_C2_SEQ34[7:0]	7:0	Top box frame 3rd/4th 4 frame rotation step for codexx10.
44h (2F89h)	**REG2F89**	**7:0**	**Default : 0x00** **Access : R/W**
	TOP_BOX_FR_C2_SEQ12[7:0]	7:0	Top box frame 1st/2nd 4 frame rotation step for codexx10.
45h (2F8Ah)	**REG2F8A**	**7:0**	**Default : 0x00** **Access : R/W**
	BOX_A_ROT_DIR	7	Location A frame counter direction. 0: Counterwise. 1: Back.
	BOX_B_ROT_DIR	6	Location B frame counter direction. 0: Counterwise. 1: Back.
	BOX_C_ROT_DIR	5	Location C frame counter direction. 0: Counterwise. 1: Back.

FRC Register (Bank = 2F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BOX_D_ROT_DIR	4	Location D frame counter direction. 0: Counterwise. 1: Back.	
	-	3:0	Reserved.	
45h (2F8Bh)	**REG2F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX8X8_ROT_00[1:0]	7:6	Box8x8 entity 00 rotation step by reference.	
	BOX8X8_ROT_01[1:0]	5:4	Box8x8 entity 01 rotation step by reference.	
	BOX8X8_ROT_11[1:0]	3:2	Box8x8 entity 11 rotation step by reference.	
	BOX8X8_ROT_10[1:0]	1:0	Box8x8 entity 10 rotation step by reference.	
46h (2F8Ch)	**REG2F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_LU_00[1:0]	7:6	B 2x2 block left up entity.	
	B_RU_01[1:0]	5:4	B 2x2 block right up entity.	
	B_RD_11[1:0]	3:2	B 2x2 block right down entity.	
	B_LD_10[1:0]	1:0	B 2x2 block left down entity.	
46h (2F8Dh)	**REG2F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	A_LU_00[1:0]	7:6	A 2x2 block left up entity.	
	A_RU_01[1:0]	5:4	A 2x2 block right up entity.	
	A_RD_11[1:0]	3:2	A 2x2 block right down entity.	
	A_LD_10[1:0]	1:0	A 2x2 block left down entity.	
47h (2F8Eh)	**REG2F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	D_LU_00[1:0]	7:6	D 2x2 block left up entity.	
	D_RU_01[1:0]	5:4	D 2x2 block right up entity.	
	D_RD_11[1:0]	3:2	D 2x2 block right down entity.	
	D_LD_10[1:0]	1:0	D 2x2 block left down entity.	
47h (2F8Fh)	**REG2F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LU_00[1:0]	7:6	C 2x2 block left up entity.	
	C_RU_01[1:0]	5:4	C 2x2 block right up entity.	
	C_RD_11[1:0]	3:2	C 2x2 block right down entity.	
	C_LD_10[1:0]	1:0	C 2x2 block left down entity.	
48h (2F90h)	**REG2F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	D_LU_00_S[1:0]	7:6	D 2x2 block left up entity, 2nd.	
	D_RU_01_S[1:0]	5:4	D 2x2 block right up entity, 2nd.	
	D_RD_11_S[1:0]	3:2	D 2x2 block right down entity, 2nd.	

FRC Register (Bank = 2F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	D_LD_10_S[1:0]	1:0	D 2x2 block left down entity, 2nd.	
48h (2F91h)	**REG2F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LU_00_S[1:0]	7:6	C 2x2 block left up entity, 2nd.	
	C_RU_01_S[1:0]	5:4	C 2x2 block right up entity, 2nd.	
	C_RD_11_S[1:0]	3:2	C 2x2 block right down entity, 2nd.	
	C_LD_10_S[1:0]	1:0	C 2x2 block left down entity, 2nd.	
49h (2F92h)	**REG2F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_B_LU_00[1:0]	7:6	Location B block A LSB 2 bits plus value.	
	BOX_B_RU_01[1:0]	5:4	Location B block B LSB 2 bits plus value.	
	BOX_B_RD_11[1:0]	3:2	Location B block C LSB 2 bits plus value.	
	BOX_B_LD_10[1:0]	1:0	Location B block D LSB 2 bits plus value.	
49h (2F93h)	**REG2F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_A_LU_00[1:0]	7:6	Location A block A LSB 2 bits plus value.	
	BOX_A_RU_01[1:0]	5:4	Location A block B LSB 2 bits plus value.	
	BOX_A_RD_11[1:0]	3:2	Location A block C LSB 2 bits plus value.	
	BOX_A_LD_10[1:0]	1:0	Location A block D LSB 2 bits plus value.	
4Ah (2F94h)	**REG2F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_D_LU_00[1:0]	7:6	Location D block A LSB 2 bits plus value.	
	BOX_D_RU_01[1:0]	5:4	Location D block B LSB 2 bits plus value.	
	BOX_D_RD_11[1:0]	3:2	Location D block C LSB 2 bits plus value.	
	BOX_D_LD_10[1:0]	1:0	Location D block D LSB 2 bits plus value.	
4Ah (2F95h)	**REG2F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_C_LU_00[1:0]	7:6	Location C block A LSB 2 bits plus value.	
	BOX_C_RU_01[1:0]	5:4	Location C block B LSB 2 bits plus value.	
	BOX_C_RD_11[1:0]	3:2	Location C block C LSB 2 bits plus value.	
	BOX_C_LD_10[1:0]	1:0	Location C block D LSB 2 bits plus value.	

XV_YCC Register (Bank = 2F, Sub-Bank = 25)

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
01h (2F02h)	**REG2F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BRI_XV_YCC_EN	7	Main window brightness carry bit enable.	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	XV_YCC_MAIN_MAX_MIN_LIMIT_EN	3	Main window rgb compress max and min limited enable.	
	XV_YCC_MAIN_FIX_GAMMA_EN	2	Main window fix gamma enable.	
	XV_YCC_MAIN_DE_GA_CM_EN	1	Main window de gamma color manage enable.	
	XV_YCC_MAIN_DE_GAMMA_EN	0	Main window de gamma enable.	
01h	**REG2F03**	**7:0**	**Default : 0x00**	**Access : R/W**

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F03h)	-	7:5	Reserved.	
	XV_YCC_MAIN_DE_GAMMA_DITHER_EN	4	Main window de gamma dither bit enable.	
	XV_YCC_MAIN_FIX_GAMMA_DITHER_EN	3	Main window fix gamma dither bit enable.	
	XV_YCC_MAIN_RGB_COMPRESS_DITHER_EN	2	Main window rgb compress dither bit enable.	
	XV_YCC_MAIN_RGB_COMPRESS_EN	1	Main window rgb compress enable.	
	XV_YCC_MAIN_BYPASS_EN	0	Main window xv ycc function block bypass enable.	
02h (2F04h)	**REG2F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_SRGB11[7:0]	7:0	Matrix coefficient 11 the format is s.2.10.	
02h (2F05h)	**REG2F05**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB11[12:8]	4:0	See description of '2F04h'.	
03h (2F06h)	**REG2F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_SRGB12[7:0]	7:0	Matrix coefficient 12 the format is s.2.10.	
03h (2F07h)	**REG2F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB12[12:8]	4:0	See description of '2F06h'.	
04h (2F08h)	**REG2F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_SRGB13[7:0]	7:0	Matrix coefficient 13 the format is s.2.10.	
04h (2F09h)	**REG2F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB13[12:8]	4:0	See description of '2F08h'.	
05h (2F0Ah)	**REG2F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_SRGB21[7:0]	7:0	Matrix coefficient 21 the format is s.2.10.	
05h (2F0Bh)	**REG2F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB21[12:8]	4:0	See description of '2F0Ah'.	
06h (2F0Ch)	**REG2F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_SRGB22[7:0]	7:0	Matrix coefficient 22 the format is s.2.10.	
06h (2F0Dh)	**REG2F0D**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB22[12:8]	4:0	See description of '2F0Ch'.	
07h	**REG2F0E**	**7:0**	**Default : 0x00**	**Access : R/W**

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F0Eh)	XV_YCC_MAIN_SRGB23[7:0]	7:0	Matrix coefficient 23 the format is s.2.10.	
07h (2F0Fh)	**REG2F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB23[12:8]	4:0	See description of '2F0Eh'.	
08h (2F10h)	**REG2F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_SRGB31[7:0]	7:0	Matrix coefficient 31 the format is s.2.10.	
08h (2F11h)	**REG2F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB31[12:8]	4:0	See description of '2F10h'.	
09h (2F12h)	**REG2F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_SRGB32[7:0]	7:0	Matrix coefficient 32 the format is s.2.10.	
09h (2F13h)	**REG2F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB32[12:8]	4:0	See description of '2F12h'.	
0Ah (2F14h)	**REG2F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_SRGB33[7:0]	7:0	Matrix coefficient 33 the format is s.2.10.	
0Ah (2F15h)	**REG2F15**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_MAIN_SRGB33[12:8]	4:0	See description of '2F14h'.	
0Bh (2F16h)	**REG2F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_R_MIN_LIMIT[7:0]	7:0	R min limit value of brightness input the format is s.12.	
0Bh (2F17h)	**REG2F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_MAIN_R_MIN_LIMIT[11:8]	3:0	See description of '2F16h'.	
0Ch (2F18h)	**REG2F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_R_MAX_LIMIT[7:0]	7:0	R max limit value of brightness input the format is 12.	
0Ch (2F19h)	**REG2F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '2F18h'.	
0Dh	**REG2F1A**	**7:0**	**Default : 0x00**	**Access : R/W**

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F1Ah)	XV_YCC_MAIN_G_MIN_LIMIT[7:0]	7:0	G min limit value of brightness input the format is s.12.	
0Dh (2F1Bh)	**REG2F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_MAIN_G_MIN_LIMIT[11:8]	3:0	See description of '2F1Ah'.	
0Eh (2F1Ch)	**REG2F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_G_MAX_LIMIT[7:0]	7:0	G max limit value of brightness input the format is 12.	
0Eh (2F1Dh)	**REG2F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '2F1Ch'.	
0Fh (2F1Eh)	**REG2F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_B_MIN_LIMIT[7:0]	7:0	B min limit value of brightness input the format is s.12.	
0Fh (2F1Fh)	**REG2F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_MAIN_B_MIN_LIMIT[11:8]	3:0	See description of '2F1Eh'.	
10h (2F20h)	**REG2F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_MAIN_B_MAX_LIMIT[7:0]	7:0	B max limit value of brightness input the format is 12.	
10h (2F21h)	**REG2F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '2F20h'.	
11h (2F22h)	**REG2F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BRI_XV_YCC_EN	7	Sub window brightness carry bit enable.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	
	POST_SUB_BRI_EN	4	Sub window post brightness enable.	
	XV_YCC_SUB_MAX_MIN_LIMIT_EN	3	Sub window rgb compress max and min limited enable.	
	XV_YCC_SUB_FIX_GAMMA_EN	2	Sub window fix gamma enable.	
	-	1	Reserved.	
	XV_YCC_SUB_DE_GAMMA_EN	0	Sub window de gamma enable.	
11h	**REG2F23**	**7:0**	**Default : 0x00**	**Access : R/W**

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F23h)	-	7:5	Reserved.	
	XV_YCC_SUB_DE_GAMMA_DITHER_EN	4	Sub window de gamma dither bit enable.	
	XV_YCC_SUB_FIX_GAMMA_DITHER_EN	3	Sub window fix gamma dither bit enable.	
	XV_YCC_SUB_RGB_COMPRESS_DITHER_EN	2	Sub window rgb compress dither bit enable.	
	XV_YCC_SUB_RGB_COMPRESS_EN	1	Sub window rgb compress function enable.	
	XV_YCC_SUB_BYPASS_EN	0	Sub window xv ycc function block bypass enable.	
12h (2F24h)	**REG2F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_SRGB11[7:0]	7:0	Matrix coefficient 11 the format is s.2.10.	
12h (2F25h)	**REG2F25**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB11[12:8]	4:0	See description of '2F24h'.	
13h (2F26h)	**REG2F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_SRGB12[7:0]	7:0	Matrix coefficient 12 the format is s.2.10.	
13h (2F27h)	**REG2F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB12[12:8]	4:0	See description of '2F26h'.	
14h (2F28h)	**REG2F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_SRGB13[7:0]	7:0	Matrix coefficient 13 the format is s.2.10.	
14h (2F29h)	**REG2F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB13[12:8]	4:0	See description of '2F28h'.	
15h (2F2Ah)	**REG2F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_SRGB21[7:0]	7:0	Matrix coefficient 21 the format is s.2.10.	
15h (2F2Bh)	**REG2F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB21[12:8]	4:0	See description of '2F2Ah'.	
16h (2F2Ch)	**REG2F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_SRGB22[7:0]	7:0	Matrix coefficient 22 the format is s.2.10.	
16h (2F2Dh)	**REG2F2D**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB22[12:8]	4:0	See description of '2F2Ch'.	
17h	**REG2F2E**	**7:0**	**Default : 0x00**	**Access : R/W**

XV_YCC Register (Bank = 2F, Sub-Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
(2F2Eh)	XV_YCC_SUB_SRGB23[7:0]	7:0	Matrix coefficient 23 the format is s.2.10.	
17h (2F2Fh)	**REG2F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB23[12:8]	4:0	See description of '2F2Eh'.	
18h (2F30h)	**REG2F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_SRGB31[7:0]	7:0	Matrix coefficient 31 the format is s.2.10.	
18h (2F31h)	**REG2F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB31[12:8]	4:0	See description of '2F30h'.	
19h (2F32h)	**REG2F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_SRGB32[7:0]	7:0	Matrix coefficient 32 the format is s.2.10.	
19h (2F33h)	**REG2F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB32[12:8]	4:0	See description of '2F32h'.	
1Ah (2F34h)	**REG2F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_SRGB33[7:0]	7:0	Matrix coefficient 33 the format is s.2.10.	
1Ah (2F35h)	**REG2F35**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	XV_YCC_SUB_SRGB33[12:8]	4:0	See description of '2F34h'.	
1Bh (2F36h)	**REG2F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_R_MIN_LIMIT[7:0]	7:0	R min limit value of brightness input the format is s.12.	
1Bh (2F37h)	**REG2F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_SUB_R_MIN_LIMIT[11:8]	3:0	See description of '2F36h'.	
1Ch (2F38h)	**REG2F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_R_MAX_LIMIT[7:0]	7:0	R max limit value of brightness input the format is 12.	
1Ch (2F39h)	**REG2F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_SUB_R_MAX_LIMIT[11:8]	3:0	See description of '2F38h'.	
1Dh	**REG2F3A**	**7:0**	**Default : 0x00**	**Access : R/W**

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F3Ah)	XV_YCC_SUB_G_MIN_LIMIT[7:0]	7:0	G min limit value of brightness input the format is s.12.	
1Dh (2F3Bh)	**REG2F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_SUB_G_MIN_LIMIT[11:8]	3:0	See description of '2F3Ah'.	
1Eh (2F3Ch)	**REG2F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_G_MAX_LIMIT[7:0]	7:0	G max limit value of brightness input the format is 12.	
1Eh (2F3Dh)	**REG2F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_SUB_G_MAX_LIMIT[11:8]	3:0	See description of '2F3Ch'.	
1Fh (2F3Eh)	**REG2F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_B_MIN_LIMIT[7:0]	7:0	B min limit value of brightness input the format is s.12.	
1Fh (2F3Fh)	**REG2F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_SUB_B_MIN_LIMIT[11:8]	3:0	See description of '2F3Eh'.	
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	XV_YCC_SUB_B_MAX_LIMIT[7:0]	7:0	B max limit value of brightness input the format is 12.	
20h (2F41h)	**REG2F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XV_YCC_SUB_B_MAX_LIMIT[11:8]	3:0	See description of '2F40h'.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post r channel offset.	
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '2F42h'.	
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post g channel offset.	
22h (2F45h)	**REG2F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '2F44h'.	
23h	**REG2F46**	**7:0**	**Default : 0x00**	**Access : R/W**

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2F46h)	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post b channel offset.	
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '2F46h'.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post r channel gain.	
24h (2F49h)	**REG2F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '2F48h'.	
25h (2F4Ah)	**REG2F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post g channel gain.	
25h (2F4Bh)	**REG2F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '2F4Ah'.	
26h (2F4Ch)	**REG2F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_CON_GAIN[7:0]	7:0	Main window post b channel gain.	
26h (2F4Dh)	**REG2F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN[11:8]	3:0	See description of '2F4Ch'.	
27h (2F4Eh)	**REG2F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_BRI_OFFSET[7:0]	7:0	Sub window post r channel offset.	
27h (2F4Fh)	**REG2F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET[10:8]	2:0	See description of '2F4Eh'.	
28h (2F50h)	**REG2F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_BRI_OFFSET[7:0]	7:0	Sub window post g channel offset.	
28h (2F51h)	**REG2F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET[10:8]	2:0	See description of '2F50h'.	
29h (2F52h)	**REG2F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_BRI_OFFSET[7:0]	7:0	Sub window post b channel offset.	
29h (2F53h)	**REG2F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	POST_SUB_B_BRI_OFFSET[10:8]	2:0	See description of '2F52h'.	
2Ah (2F54h)	**REG2F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post r channel gain.	
2Ah (2F55h)	**REG2F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[11:8]	3:0	See description of '2F54h'.	
2Bh (2F56h)	**REG2F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post g channel gain.	
2Bh (2F57h)	**REG2F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '2F56h'.	
2Ch (2F58h)	**REG2F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_CON_GAIN[7:0]	7:0	Sub window post b channel gain.	
2Ch (2F59h)	**REG2F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[11:8]	3:0	See description of '2F58h'.	
2Dh (2F5Ah)	**REG2F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAIN1_TH[7:0]	7:0	Hbc gain1 threshold.	
2Dh (2F5Bh)	**REG2F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GAMMA_OD_PIPE_SEL	0	Gamma and od pipe select, 0: Gamma before od, 1: Gamma after od.	
2Eh (2F5Ch)	**REG2F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0[7:0]	7:0	Dummy register.	
2Eh (2F5Dh)	**REG2F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0[15:8]	7:0	See description of '2F5Ch'.	
2Fh (2F5Eh)	**REG2F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1[7:0]	7:0	Dummy register.	
2Fh (2F5Fh)	**REG2F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1[15:8]	7:0	See description of '2F5Eh'.	
30h (2F60h)	**REG2F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	PAT_SWITCH	4	Initial pattern switch for pixel or dot pattern.	

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_FIT_EN	3	Enable auto fit window size.	
	SW_FREEZE_IDX	2	Software freeze pattern enable.	
	AUTO_IDX_EN	1	Auto run pattern enable.	
	PG_EN	0	Pattern generate enable.	
30h (2F61h)	**REG2F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PAT_DELTA[3:0]	3:0	Pattern increase delta value.	
31h (2F62h)	**REG2F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SW_SET_IDX[4:0]	4:0	Software set pattern idx.	
31h (2F63h)	**REG2F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAT_PERIOD[7:0]	7:0	Per pattern period, unit is frame.	
32h (2F64h)	**REG2F64**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAT_R[7:0]	7:0	R fix color.	
32h (2F65h)	**REG2F65**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	PAT_R[9:8]	1:0	See description of '2F64h'.	
33h (2F66h)	**REG2F66**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAT_G[7:0]	7:0	G fix color.	
33h (2F67h)	**REG2F67**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	PAT_G[9:8]	1:0	See description of '2F66h'.	
34h (2F68h)	**REG2F68**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAT_B[7:0]	7:0	B fix color.	
34h (2F69h)	**REG2F69**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	PAT_B[9:8]	1:0	See description of '2F68h'.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN0_X0[7:0]	7:0	OSD window0 x0 position.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN0_X0[11:8]	3:0	See description of '2FA0h'.	
51h	**REG2FA2**	**7:0**	**Default : 0x00**	**Access : R/W**

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(2FA2h)	OSD_WIN0_X1[7:0]	7:0	OSD window0 x1 position.	
51h (2FA3h)	**REG2FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN0_X1[11:8]	3:0	See description of '2FA2h'.	
52h (2FA4h)	**REG2FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN0_Y0[7:0]	7:0	OSD window0 y0 position.	
52h (2FA5h)	**REG2FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN0_Y0[11:8]	3:0	See description of '2FA4h'.	
53h (2FA6h)	**REG2FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN0_Y1[7:0]	7:0	OSD window0 y1 position.	
53h (2FA7h)	**REG2FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN0_Y1[11:8]	3:0	See description of '2FA6h'.	
54h (2FA8h)	**REG2FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN1_X0[7:0]	7:0	OSD window1 x0 position.	
54h (2FA9h)	**REG2FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN1_X0[11:8]	3:0	See description of '2FA8h'.	
55h (2FAAh)	**REG2FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN1_X1[7:0]	7:0	OSD window1 x1 position.	
55h (2FABh)	**REG2FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN1_X1[11:8]	3:0	See description of '2FAAh'.	
56h (2FACh)	**REG2FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN1_Y0[7:0]	7:0	OSD window1 y0 position.	
56h (2FADh)	**REG2FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN1_Y0[11:8]	3:0	See description of '2FACh'.	
57h (2FAEh)	**REG2FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN1_Y1[7:0]	7:0	OSD window1 y1 position.	
57h (2FAFh)	**REG2FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OSD_WIN1_Y1[11:8]	3:0	See description of '2FAEh'.	
58h (2FB0h)	**REG2FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN2_X0[7:0]	7:0	OSD window2 x0 position.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN2_X0[11:8]	3:0	See description of '2FB0h'.	
59h (2FB2h)	**REG2FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN2_X1[7:0]	7:0	OSD window2 x1 position.	
59h (2FB3h)	**REG2FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN2_X1[11:8]	3:0	See description of '2FB2h'.	
5Ah (2FB4h)	**REG2FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN2_Y0[7:0]	7:0	OSD window2 y0 position.	
5Ah (2FB5h)	**REG2FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN2_Y0[11:8]	3:0	See description of '2FB4h'.	
5Bh (2FB6h)	**REG2FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN2_Y1[7:0]	7:0	OSD window2 y1 position.	
5Bh (2FB7h)	**REG2FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN2_Y1[11:8]	3:0	See description of '2FB6h'.	
5Ch (2FB8h)	**REG2FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN3_X0[7:0]	7:0	OSD window3 x0 position.	
5Ch (2FB9h)	**REG2FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN3_X0[11:8]	3:0	See description of '2FB8h'.	
5Dh (2FBAh)	**REG2FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN3_X1[7:0]	7:0	OSD window3 x1 position.	
5Dh (2FBBh)	**REG2FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN3_X1[11:8]	3:0	See description of '2FBAh'.	
5Eh (2FBCh)	**REG2FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN3_Y0[7:0]	7:0	OSD window3 y0 position.	

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Eh (2FBDh)	**REG2FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN3_Y0[11:8]	3:0	See description of '2FBCh'.	
5Fh (2FBEh)	**REG2FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN3_Y1[7:0]	7:0	OSD window3 y1 position.	
5Fh (2FBFh)	**REG2FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN3_Y1[11:8]	3:0	See description of '2FBEh'.	
60h (2FC0h)	**REG2FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN4_X0[7:0]	7:0	OSD window4 x0 position.	
60h (2FC1h)	**REG2FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN4_X0[11:8]	3:0	See description of '2FC0h'.	
61h (2FC2h)	**REG2FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN4_X1[7:0]	7:0	OSD window4 x1 position.	
61h (2FC3h)	**REG2FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN4_X1[11:8]	3:0	See description of '2FC2h'.	
62h (2FC4h)	**REG2FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN4_Y0[7:0]	7:0	OSD window4 y0 position.	
62h (2FC5h)	**REG2FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN4_Y0[11:8]	3:0	See description of '2FC4h'.	
63h (2FC6h)	**REG2FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN4_Y1[7:0]	7:0	OSD window4 y1 position.	
63h (2FC7h)	**REG2FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN4_Y1[11:8]	3:0	See description of '2FC6h'.	
64h (2FC8h)	**REG2FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	LENGTH[7:0]	7:0	LVDS vbi tx data LENGTH.	
64h (2FC9h)	**REG2FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LENGTH[9:8]	1:0	See description of '2FC8h'.	

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
65h (2FCAh)	**REG2FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAIT_CNT[7:0]	7:0	LVDS vbi tx wait cycle.	
66h (2FCCh)	**REG2FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	TYPE[7:0]	7:0	LVDS vbi tx TYPE.	
66h (2FCDh)	**REG2FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TYPE[9:8]	1:0	See description of '2FCCh'.	
67h (2FCEh)	**REG2FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	HEADER_PW[7:0]	7:0	LVDS vbi header passwd.	
67h (2FCFh)	**REG2FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HEADER_PW[9:8]	1:0	See description of '2FCEh'.	
68h (2FD0h)	**REG2FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OSD_WIN_VALID[4:0]	4:0	OSD window valid bit.	
68h (2FD1h)	**REG2FD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBI_FIRE	7	LVDS vbi fire.	
	-	6:1	Reserved.	
	LVDS_VBI_EN	0	LVDS vbi tx enable.	

SPIKE_NR Register (Bank = 2F, Sub-Bank = 26)

SPIKE_NR Register (Bank = 2F, Sub-Bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
50h (2FA0h)	**REG2FA0**	**7:0**	**Default : 0x44**	**Access : R/W**
	-	7:6	Reserved.	
	V_C_LPF_EN_F1	5	Vertical C Low Pass Filter Enable F1.	
	SPIKE_NR_EN_F1	4	Spike NR Enable F1.	
	SPIKE_NR_MR_EN	3	Spike NR motion ratio enable.	
	-	2	Reserved.	
	V_C_LPF_EN_F2	1	Vertical C Low Pass Filter Enable F2.	
	SPIKE_NR_EN_F2	0	Spike NR Enable F2.	
50h (2FA1h)	**REG2FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SPIKE_NR_COEF[3:0]	3:0	Spike NR Coefficient.	

SPIKE_NR Register (Bank = 2F, Sub-Bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
51h (2FA3h)	**REG2FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	P_THRD_1[4:0]	4:0	Spike NR P threshold 1.	
53h (2FA6h)	**REG2FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	D_31_STEP[2:0]	6:4	Spike NR D31 Step.	
	-	3	Reserved.	
	D_11_21_STEP[2:0]	2:0	Spike NR D11_21 Step.	
53h (2FA7h)	**REG2FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	YP_22_STEP[2:0]	2:0	Spike NR YP22 Step.	
55h (2FAAh)	**REG2FAA**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_0[7:0]	7:0	Spike NR motion ratio look-up-table 0.	
55h (2FABh)	**REG2FAB**	**7:0**	**Default : 0x32**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_1[7:0]	7:0	Spike NR motion ratio look-up-table 1.	
56h (2FACh)	**REG2FAC**	**7:0**	**Default : 0x54**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_2[7:0]	7:0	Spike NR motion ratio look-up-table 2.	
56h (2FADh)	**REG2FAD**	**7:0**	**Default : 0x76**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_3[7:0]	7:0	Spike NR motion ratio look-up-table 3.	
57h (2FAEh)	**REG2FAE**	**7:0**	**Default : 0x98**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_4[7:0]	7:0	Spike NR motion ratio look-up-table 4.	
57h (2FAFh)	**REG2FAF**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_5[7:0]	7:0	Spike NR motion ratio look-up-table 5.	
58h (2FB0h)	**REG2FB0**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_6[7:0]	7:0	Spike NR motion ratio look-up-table 6.	
58h (2FB1h)	**REG2FB1**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_7[7:0]	7:0	Spike NR motion ratio look-up-table 7.	

ACE2 Register (Bank = 2F, Sub-Bank = 27)

ACE2 Register (Bank = 2F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (2F00h)	**REG2F00**	**7:0**	**Default : 0x00**	**Access : R/W**
	MODULE_REGBANK[7:0]	7:0	Register Bank Select. 00: Register of OSD/Interrupt. 01: Register of IP1 Main Window. 02: Register of IP2 Main Window. 03: Register of IP1 Sub Window. 04: Register of IP2 Sub Window. 05: Register of OPM. 06: Register of DNR. 0A: Reserved. 0C: Register of SNR. 0F: Register of S_VOP. 10: Register of VOP. 12: Register of SCMI. 18: Register of ACE. 19: Register of PEAKING. 1A: Register of DLC. 20: Register of OP1_TOP. 21: Register of ELA. 22: Register of TDDI. 23: Register of HVSP. 24: Register of PAFRC. 25: Register of xVYCC. 26: Register of DMS. 27: Register of ACE2.	
20h (2F40h)	**REG2F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CTI_MEDIAN_EN	5	Sub window CTI median enable.	
	SUB_CTI_EN	4	Sub window CTI enable.	
	-	3:2	Reserved.	
	MAIN_CTI_MEDIAN_EN	1	Main window CTI median enable.	
	MAIN_CTI_EN	0	Main window CTI enable.	
21h (2F42h)	**REG2F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CTI_STEP[1:0]	5:4	Main window CTI step.	
	-	3	Reserved.	

ACE2 Register (Bank = 2F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_CTI_LPF_COEF[2:0]	2:0	Main window CTI low pass filter coefficient.	
21h (2F43h)	**REG2F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CTI_CORING_THRD[3:0]	3:0	Main window CTI coring threshold.	
22h (2F44h)	**REG2F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CTI_BAND_COEF[5:0]	5:0	Main window CTI band pass filter coefficient.	
23h (2F46h)	**REG2F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CTI_STEP[1:0]	5:4	Sub window CTI step.	
	-	3	Reserved.	
	SUB_CTI_LPF_COEF[2:0]	2:0	Sub window CTI low pass filter enable.	
23h (2F47h)	**REG2F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_CTI_CORING_THRD[3:0]	3:0	Sub window CTI coring threshold.	
24h (2F48h)	**REG2F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CTI_BAND_COEF[5:0]	5:0	Sub window CTI band pass filter coefficient.	
25h ~ 26h (2F4Ah ~ 2F4Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

RTC Register (Bank = 34)

RTC Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (3480h)	**REG3480**	**7:0**	**Default : 0x21**	**Access : R/W**
	C_INT_CLEAR	7	Clear RTC interrupt.	
	C_INT_FORCE	6	Force RTC interrupt to be 1.	
	C_INT_MASK	5	Mask RTC interrupt.	
	C_READ_EN	4	Read enable for reading value from RTC counter (write and generate one-shot signal for latching rtc_cnt).	
	C_LOAD_EN	3	Load enable for loading value into RTC counter (write and generate one-shot enable signal).	
	C_WRAP_EN	2	Wrap RTC counter when c_match_val is reached.	
	C_CNT_EN	1	Enable RTC counter.	
	C_SOFT_RSTZ	0	RTC software reset (low active).	
41h (3482h)	**REG3482**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_FREQ_CW[7:0]	7:0	Frequency control word of RTC counter. Clock frequency of RTC counter = XTAL_frequency/control_word.	
41h (3483h)	**REG3483**	**7:0**	**Default : 0x7F**	**Access : R/W**
	C_FREQ_CW[15:8]	7:0	See description of '3482h'.	
42h (3484h)	**REG3484**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FREQ_CW[23:16]	7:0	See description of '3482h'.	
42h (3485h)	**REG3485**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_FREQ_CW[31:24]	7:0	See description of '3482h'.	
43h (3486h)	**REG3486**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LOAD_VAL[7:0]	7:0	Value to load into RTC counter.	
43h (3487h)	**REG3487**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LOAD_VAL[15:8]	7:0	See description of '3486h'.	
44h (3488h)	**REG3488**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LOAD_VAL[23:16]	7:0	See description of '3486h'.	
44h (3489h)	**REG3489**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LOAD_VAL[31:24]	7:0	See description of '3486h'.	
45h (348Ah)	**REG348A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_MATCH_VAL[7:0]	7:0	Counter match value.	
45h	**REG348B**	**7:0**	**Default : 0xFF**	**Access : R/W**

RTC Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(348Bh)	C_MATCH_VAL[15:8]	7:0	See description of '348Ah'.	
46h (348Ch)	**REG348C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_MATCH_VAL[23:16]	7:0	See description of '348Ah'.	
46h (348Dh)	**REG348D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	C_MATCH_VAL[31:24]	7:0	See description of '348Ah'.	
47h (348Eh)	**REG348E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	RTC_INT	1	RTC interrupt status.	
	RTC_RAW_INT	0	Raw interrupt status.	
48h (3490h)	**REG3490**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_CNT[7:0]	7:0	RTC counter value.	
48h (3491h)	**REG3491**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_CNT[15:8]	7:0	See description of '3490h'.	
49h (3492h)	**REG3492**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_CNT[23:16]	7:0	See description of '3490h'.	
49h (3493h)	**REG3493**	**7:0**	**Default : 0x00**	**Access : RO**
	RTC_CNT[31:24]	7:0	See description of '3490h'.	

MIIC Register (Bank = 34)

MIIC Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (3420h)	**REG3420**	**7:0**	**Default : 0x00**	**Access : R/W**
	MENABLE	7	Master IIC enable.	
	SBIT	6	Start bit assert.	
	PBIT	5	Stop bit assert.	
	MACKO	4	Ack output.	
	MACKI	3	Ack input.	
	-	2	Reserved.	
	CLR_NEW_DATA	1	Clear new data flag,. 1: Clear. 0: No use.	
	-	0	Reserved.	
11h (3422h)	**REG3422**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCLK_SEL[7:0]	7:0	Master IIC 0 clock select. 1: CLK/4. 2: CLK/8. 3: CLK/16. 4: CLK/32. 5: CLK/64. 6: CLK/128. 7: CLK/256. 8: CLK/512. 9: CLK/1024. Others: CLK/2.	
12h (3424h)	**REG3424**	**7:0**	**Default : 0x00**	**Access : R/W**
	WMBUF[7:0]	7:0	Write data.	
13h (3426h)	**REG3426**	**7:0**	**Default : 0x00**	**Access : RO**
	RMBUF[7:0]	7:0	Read data.	
14h (3428h)	**REG3428**	**7:0**	**Default : 0x00**	**Access : RO, R/W, WO**
	-	7:4	Reserved.	
	MIIC_RST	3	Set 1 to reset Master IIC circuit.	
	RD_START	2	Set 1 to start byte reading.	
	INT_CLR	1	Set 1 to clear IIC 0 interrupt status.	
	INT_STATUS	0	Write/read/stop finish. Used for software polling, the bit is set if byte write, byte	

MIIC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
			read or stop is finished. The interrupt status can be cleared by writing INT_CLR bit.	
15h (342Ah)	**REG342A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIIC_RES[6:0]	7:1	Master IIC reset.	
	EN_STOP_INT	0	Enable stop interrupt.	
15h (342Bh)	**REG342B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIIC_RES[14:7]	7:0	See description of '342Ah'.	
18h (3430h)	**REG3430**	**7:0**	**Default : 0x00**	**Access : R/W**
	MSTART[7:0]	7:0	Master IIC DMA target start address.	
18h (3431h)	**REG3431**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MSTART[14:8]	6:0	See description of '3430h'.	
19h (3432h)	**REG3432**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCOUNT[7:0]	7:0	Master IIC DMA byte count. 0: 1 byte. 1: 2 bytes. n: N+1 bytes.	
19h (3433h)	**REG3433**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIIC_DMA_EN	7	Master IIC DMA enable.	
	MCOUNT[14:8]	6:0	See description of '3432h'.	
1Ah (3434h)	**REG3434**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	EELOAD_DEV1_EN	1	EEPROM load to VD enable.	
	EELOAD_DEV0_EN	0	EEPROM load to HK enable.	
1Ah (3435h)	**REG3435**	**7:0**	**Default : 0x00**	**Access : RO**
	DMA_END	7	DMA finish flag.	
	-	6:0	Reserved.	

PWM Register (Bank = 34)

PWM Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
31h (3462h)	**REG3462**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UNIT_DIV[7:0]	7:0	PWM clock unit divider.	
32h (3464h)	**REG3464**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_PERIOD[7:0]	7:0	PWM 0 period.	
32h (3465h)	**REG3465**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM0_PERIOD[9:8]	1:0	See description of '3464h'.	
33h (3466h)	**REG3466**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_DUTY[7:0]	7:0	PWM 0 duty.	
33h (3467h)	**REG3467**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM0_DUTY[9:8]	1:0	See description of '3466h'.	
34h (3468h)	**REG3468**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_DIV[7:0]	7:0	PWM 0 divider.	
34h (3469h)	**REG3469**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PWM0_ODDEVEN_SYNC	5	PWM 0 odd & even sync.	
	PWM0_IMPULSE_EN	4	PWM 0 impulse enable.	
	PWM0_DBEN	3	PWM 0 double enable.	
	PWM0_RESET_EN	2	PWM 0 Vsync reset 0.	
	PWM0_VDBEN	1	PWM 0 Vsync double enable.	
	PWM0_POLARITY	0	PWM 0 polarity.	
35h (346Ah)	**REG346A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_PERIOD[7:0]	7:0	PWM 1 period.	
35h (346Bh)	**REG346B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM1_PERIOD[9:8]	1:0	See description of '346Ah'.	
36h (346Ch)	**REG346C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_DUTY[7:0]	7:0	PWM 1 duty.	
36h (346Dh)	**REG346D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
	PWM1_DUTY[9:8]	1:0	See description of '346Ch'.	
37h (346Eh)	**REG346E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_DIV[7:0]	7:0	PWM 1 divider.	
37h (346Fh)	**REG346F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PWM1_ODDEVEN_SYNC	5	PWM 1 odd & even sync.	
	PWM1_IMPULSE_EN	4	PWM 1 impulse enable.	
	PWM1_DBEN	3	PWM 1 double enable.	
	PWM1_RESET_EN	2	PWM 1 Vsync reset 0.	
	PWM1_VDBEN	1	PWM 1 Vsync double enable.	
	PWM1_POLARITY	0	PWM 1 polarity.	
38h (3470h)	**REG3470**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_PERIOD[7:0]	7:0	PWM 2 period.	
38h (3471h)	**REG3471**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM2_PERIOD[9:8]	1:0	See description of '3470h'.	
39h (3472h)	**REG3472**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_DUTY[7:0]	7:0	PWM 2 duty.	
39h (3473h)	**REG3473**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM2_DUTY[9:8]	1:0	See description of '3472h'.	
3Ah (3474h)	**REG3474**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_DIV[7:0]	7:0	PWM 2 divider.	
3Ah (3475h)	**REG3475**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PWM2_ODDEVEN_SYNC	5	PWM 2 odd & even sync.	
	PWM2_IMPULSE_EN	4	PWM 2 impulse enable.	
	PWM2_DBEN	3	PWM 2 double enable.	
	PWM2_RESET_EN	2	PWM 2 Vsync reset 0.	
	PWM2_VDBEN	1	PWM 2 Vsync double enable.	
	PWM2_POLARITY	0	PWM 2 polarity.	
3Bh (3476h)	**REG3476**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_PERIOD[7:0]	7:0	PWM 3 period.	

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
3Bh (3477h)	**REG3477**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM3_PERIOD[9:8]	1:0	See description of '3476h'.	
3Ch (3478h)	**REG3478**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_DUTY[7:0]	7:0	PWM 3 duty.	
3Ch (3479h)	**REG3479**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM3_DUTY[9:8]	1:0	See description of '3478h'.	
3Dh (347Ah)	**REG347A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_DIV[7:0]	7:0	PWM 3 divider.	
3Dh (347Bh)	**REG347B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PWM3_ODDEVEN_SYNC	5	PWM 3 odd & even sync.	
	PWM3_IMPULSE_EN	4	PWM 3 impulse enable.	
	PWM3_DBEN	3	PWM 3 double enable.	
	PWM3_RESET_EN	2	PWM 3 Vsync reset 0.	
	PWM3_VDBEN	1	PWM 3 Vsync double enable.	
	PWM3_POLARITY	0	PWM 3 polarity.	
3Eh (347Ch)	**REG347C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_PERIOD[7:0]	7:0	PWM 4 period.	
3Eh (347Dh)	**REG347D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM4_PERIOD[9:8]	1:0	See description of '347Ch'.	
3Fh (347Eh)	**REG347E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_DUTY[7:0]	7:0	PWM 4 duty.	
3Fh (347Fh)	**REG347F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM4_DUTY[9:8]	1:0	See description of '347Eh'.	
40h (3480h)	**REG3480**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_DIV[7:0]	7:0	PWM 4 divider.	
40h (3481h)	**REG3481**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PWM4_ODDEVEN_SYNC	5	PWM 4 odd & even sync.	

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
	PWM4_IMPULSE_EN	4	PWM 4 impulse enable.	
	PWM4_DBEN	3	PWM 4 double enable.	
	PWM4_RESET_EN	2	PWM 4 Vsync reset 0.	
	PWM4_VDBEN	1	PWM 4 Vsync double enable.	
	PWM4_POLARITY	0	PWM 4 polarity.	
41h (3482h)	**REG3482**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_PERIOD[7:0]	7:0	PWM 5 period.	
41h (3483h)	**REG3483**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM5_PERIOD[9:8]	1:0	See description of '3482h'.	
42h (3484h)	**REG3484**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_DUTY[7:0]	7:0	PWM 5 duty.	
42h (3485h)	**REG3485**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PWM5_DUTY[9:8]	1:0	See description of '3484h'.	
43h (3486h)	**REG3486**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_DIV[7:0]	7:0	PWM 5 divider.	
43h (3487h)	**REG3487**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PWM5_ODDEVEN_SYNC	5	PWM 5 odd & even sync.	
	PWM5_IMPULSE_EN	4	PWM 5 impulse enable.	
	PWM5_DBEN	3	PWM 5 double enable.	
	PWM5_RESET_EN	2	PWM 5 Vsync reset 0.	
	PWM5_VDBEN	1	PWM 5 Vsync double enable.	
	PWM5_POLARITY	0	PWM 5 polarity.	
44h (3488h)	**REG3488**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX1	7	PWM 1 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT1[3:0]	3:0	PWM 1 Hsync reset counter.	
44h (3489h)	**REG3489**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX0	7	PWM 0 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT0[3:0]	3:0	PWM 0 Hsync reset counter.	

PWM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description	
45h (348Ah)	**REG348A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX3	7	PWM 3 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT3[3:0]	3:0	PWM 3 Hsync reset counter.	
45h (348Bh)	**REG348B**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX2	7	PWM 2 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT2[3:0]	3:0	PWM 2 Hsync reset counter.	
46h (348Ch)	**REG348C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX5	7	PWM 5 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT5[3:0]	3:0	PWM 5 Hsync reset counter.	
46h (348Dh)	**REG348D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX4	7	PWM 4 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT4[3:0]	3:0	PWM 4 Hsync reset counter.	
47h (348Eh)	**REG348E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IMPULSE_DUTY_SEL[2:0]	2:0	Impulse duty select.	
48h (3490h)	**REG3490**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMPULSE_DUTY0[7:0]	7:0	Impulse duty 0.	
48h (3491h)	**REG3491**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IMPULSE_DUTY0[9:8]	1:0	See description of '3490h'.	
49h (3492h)	**REG3492**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMPULSE_DUTY1[7:0]	7:0	Impulse duty 1.	
49h (3493h)	**REG3493**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IMPULSE_DUTY1[9:8]	1:0	See description of '3492h'.	
4Ah (3494h)	**REG3494**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMPULSE_DUTY2[7:0]	7:0	Impulse duty 2.	
4Ah (3495h)	**REG3495**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

PWM Register (Bank = 34)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IMPULSE_DUTY2[9:8]	1:0	See description of '3494h'.	
4Bh (3496h)	**REG3496**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMPULSE_DUTY3[7:0]	7:0	Impulse duty 3.	
4Bh (3497h)	**REG3497**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IMPULSE_DUTY3[9:8]	1:0	See description of '3496h'.	
4Ch (3498h)	**REG3498**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMPULSE_DUTY4[7:0]	7:0	Impulse duty 4.	
4Ch (3499h)	**REG3499**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IMPULSE_DUTY4[9:8]	1:0	See description of '3498h'.	
4Dh (349Ah)	**REG349A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMPULSE_DUTY5[7:0]	7:0	Impulse duty 5.	
4Dh (349Bh)	**REG349B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IMPULSE_DUTY5[9:8]	1:0	See description of '349Ah'.	
4Eh (349Ch)	**REG349C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMPULSE_DUTY6[7:0]	7:0	Impulse duty 6.	
4Eh (349Dh)	**REG349D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IMPULSE_DUTY6[9:8]	1:0	See description of '349Ch'.	
4Fh (349Eh)	**REG349E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IMPULSE_DUTY7[7:0]	7:0	Impulse duty 7.	
4Fh (349Fh)	**REG349F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IMPULSE_DUTY7[9:8]	1:0	See description of '349Eh'.	

AFEC Register (Bank = 35)

AFEC Register (Bank = 35)				
Index	**Mnemonic**	**Bit**	**Description**	
01h ~ 19h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
1Ah	**REG1A**	**7:0**	**Default : 0x40**	**Access : R/W**
	SVIDEO_EN	7	0: Chroma source from CVBS-channel input. 1: Chroma source from C-channel input.	
	ADC_C_ALWAYS_ON	6	Chroma ADC 16fsc-to-4fsc down-sampling is enabled.	
	-	5:0	Reserved.	
1Bh ~ 6Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
6Fh	**REG6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	LINE_START_VF_SEL[1:0]	7:6	Line start V half line.	
	LINE_MIDDLE_VF_SEL[1:0]	5:4	Line middle V half line.	
	DPL_DPLDB	3	DPL_DE double mode enable.	
	DPL_DBDE	2	Double DE enable.	
	DPL_HSEN	1	DPL_HS mode enable.	
	DPL_DEEN	0	DPL_DE bypass mode enable.	
70h ~ 75h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
76h	**REG76**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	656_BLANK_MD	2	656 blank mode.	
	656_EN	1	656 enable. 0: Disable. 1: Enable.	
	-	0	Reserved.	
77h	**REG77**	**7:0**	**Default : 0x02**	**Access : R/W**
	656_BLANK_MAX[7:0]	7:0	Maximum of 656 blank region.	
78h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
79h	**REG79**	**7:0**	**Default : 0x18**	**Access : R/W**
	656_HDES_O_9_2[7:0]	7:0	BT.656 SAV position. For VCR, 656_HDES = 656_HDES_O - 656_HDES_VCR_OFST * 4. Otherwise, 656_HDES = 656_HDES_O.	
7Ah	**REG7A**	**7:0**	**Default : 0x20**	**Access : R/W**
	656_HDES_O_1_0[1:0]	7:6	656 H DE start.	
	-	5:2	Reserved.	
	656_INV_F	1	656 field inverse.	
	SELMIX	0	Mixed data out select.	
7Bh	**REG7B**	**7:0**	**Default : 0xB3**	**Access : R/W**

AFEC Register (Bank = 35)

Index	Mnemonic	Bit	Description	
	656_HDEW[7:0]	7:0	BT.656 active data width (*4+4).	
7Ch ~	**-**	**7:0**	**Default : -**	**Access : -**
7Fh	-	7:0	Reserved.	
8Ch	**REG8C**	**7:0**	**Default : 0x4A**	**Access : R/W**
	TEST_Y[7:0]	7:0	Pattern generation Y.	
8Dh	**REG8D**	**7:0**	**Default : 0xAD**	**Access : R/W**
	TEST_CB[7:0]	7:0	Pattern generation Cb.	
8Eh	**REG8E**	**7:0**	**Default : 0x27**	**Access : R/W**
	TEST_CR[7:0]	7:0	Pattern generation Cr.	
8Fh	**REG8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FSC_TABLE_3_2[1:0]	3:2	Frequency synthesizer base. 0: 160MHz. 1: 15*14.31818MHz. 2: 216Mhz 3: 15*14.31818MHz; only valid for REG_FSC_TABLE[4] = 1.	
	FSC_TABLE_1_0[1:0]	1:0	Frequency synthesizer output. 0: 4*fsc. 1: 8*fsc. 2: 16*fsc. 3: 16*fsc.	
92h ~	**-**	**7:0**	**Default : -**	**Access : -**
95h	-	7:0	Reserved.	
96h	**REG96**	**7:0**	**Default : 0xA0**	**Access : R/W**
	NOISE_DC_SEL[1:0]	7:6	Noise magnitude estimation DC level selection. 0: IIR_8. 1: IIR_8. 2: CCTRAP_13. 3: CCTRAP.	
	EDGES_NOISY[5:0]	5:0	Threshold of the average number of sliced edges per line to determine noisy mode (/ 4).	
97h	**REG97**	**7:0**	**Default : 0x05**	**Access : R/W**
	SYNC_INMUX_3_2[1:0]	7:6	Slicer input pre-filter selection. Enable when SYNC_INMUX[0] = 0. 0: CCTRAP. 1: CCTRAP_13. 2: IIR_8. 3: IIR_16.	
	SYNC_INMUX_1	5	Slicer auxiliary pre-filter selection. 0: IIR_8.	

AFEC Register (Bank = 35)				
Index	**Mnemonic**	**Bit**	**Description**	
			1: IIR_16.	
	SYNC_INMUX_0	4	Slicer input pre-filter selection extend bit. 0: See SYNC_INMUX[3:2]. 1: IIR_4.	
	-	3:0	Reserved.	
98h ~ 9Ch	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
9Dh	**REG9D**	**7:0**	**Default : 0x6C**	**Access : R/W**
	DPL_NSPL_10_3[7:0]	7:0	PI-type display PLL number of samples per line (MSB). Typically 864.	
9Eh	**REG9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DPL_NSPL_2_0[2:0]	7:5	PI-type display PLL number of samples per line (LSB). Typically 864.	
	-	4:0	Reserved.	
9Fh ~ BDh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:6	Reserved.	
BEh	**REGBE**	**7:0**	**Default : 0x6C**	**Access : R/W**
	DPL_NSPL_656_10_3[7:0]	7:0	PI-type display PLL number of samples per line for BT.656 output (MSB). Typically 864.	
BFh	**REGBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DPL_NSPL_656_2_0[2:0]	7:5	PI-type display PLL number of samples per line for BT.656 output (LSB). Typically 864.	
	-	4:1	Reserved.	
	STD_656_EN	0	Enable standard 656 output.	
E3h ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

COMB Register (Bank = 36)

COMB Register (Bank = 36)				
Index	**Mnemonic**	**Bit**	**Description**	
10h	**REG10**	**7:0**	**Default : 0x17**	**Access : R/W**
	SVDOIN	7	S-video input.	
	SVDOCBP	6	Band pass filter for S-video C channel.	
	DIRADCIN	5	Direct use ADC input (bypass AFEC).	
	NEW_COMB_EN	4	New Comb enable.	
	MANUCOMB	3	0: Auto select working mode. 1: Manual select working mode.	
	WORKMD[2:0]	2:0	Working mode. 0/1: 1D. 2: 2D. 3: 3D. Other: Enhanced 3D.	
11h	**REG11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CRMAOFF	1	Chroma off.	
	BSTOFF	0	Burst off.	
12h	**REG12**	**7:0**	**Default : 0x18**	**Access : R/W**
	FREESYNC	7	H/V sync free-run.	
	FREECNTMD	6	Free run counter mode. 0: NTSC. 1: PAL.	
	SNOWTYPE[1:0]	5:4	Snow type. 0: Never. 1: Auto. 2: Force.	
	VWINPOS[3:0]	3:0	Vertical window position.	
13h	**REG13**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:6	Reserved.	
	DEMO3DMD[1:0]	5:4	2D/3D demo mode. 0x: Off. 10: 2D/3D. 11: 3D/2D.	
	-	3:2	Reserved.	
	PKTMD[1:0]	1:0	Packet mode. 00: 64 pixels per packet.	

COMB Register (Bank = 36)				
Index	**Mnemonic**	**Bit**	**Description**	
			01: 128 pixels per packet. 10: 256 pixels per packet. 11: Reserved.	
14h	**REG14**	**7:0**	**Default : 0x88**	**Access : R/W**
	HSTRATIO[2:0]	7:5	History ratio.	
	NRLEVEL[4:0]	4:0	Noise reduction strength.	
15h	**REG15**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
16h	**REG16**	**7:0**	**Default : 0x70**	**Access : R/W**
	BNDOF2D3D[7:0]	7:0	Boundary of 2D/3D demo mode.	
17h	**REG17**	**7:0**	**Default : 0xC0**	**Access : R/W**
	HORSTPOS[7:0]	7:0	3D window horizontal starting position. 0..255 -> -128..127.	
18h	**REG18**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
19h	**REG19**	**7:0**	**Default : 0x8D**	**Access : R/W**
	FREEHTOT_LOW[7:0]	7:0	Free-run HSYNC total (L).	
1Ah	**REG1A**	**7:0**	**Default : 0x03**	**Access : R/W**
		7:4	Reserved.	
	FREEHTOT_HIGH[3:0]	3:0	Free run HSYNC total (H).	
1Bh	**REG1B**	**7:0**	**Default : 0x83**	**Access : R/W**
	PHSDETEN	7	Line-lock phase detection enable.	
	PHSDETINV	6	Output inverse.	
	NEWLLEN	5	New line lock enable (for no burst).	
	SCLR_DO_DEM	4	New comb do DEM disable.	
	PAL_CMP_INV	3	New comb pal CMP up inverse bit.	
	PHSDETSFT[2:0]	2:0	Shift-right bit number.	
1Ch	**REG1C**	**7:0**	**Default : 0xEC**	**Access : R/W**
	HSFRAFEC	7	H sync from AFEC.	
	VSFRAFEC	6	V sync from AFEC.	
	BLKFRAFEC	5	Black level from AFEC (MCU).	
	-	4	Reserved.	
	LNFRMCU	3	525/625 line information from MCU.	
	FREQFRMCU	2	3.58/4.43 MHz information from MCU.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	STDSEL[1:0]	1:0	NTSC/PAL decision. 00: From MCU. 01: Force NTSC. 10: Force PAL. 11: From AFEC.	
1Dh ~ 1Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
20h	**REG20**	**7:0**	**Default : 0x67**	**Access : R/W**
	-	7	Reserved.	
	YNCHMD[2:0]	6:4	Notch mode of Y.	
	-	3	Reserved.	
	CNCHMD[2:0]	2:0	Notch mode of C.	
21h	**REG21**	**7:0**	**Default : 0x81**	**Access : R/W**
	-	7:4	Reserved.	
	CRMAFLTMD[1:0]	3:2	Chroma filter mode. 00: Off. 01: Band pass. 10: Median type A. 11: Median type B.	
	CDEMCHK[1:0]	1:0	Chroma vertical check (DEM). 00: Off. 01: PAL only. 1x: Always do.	
22h	**REG22**	**7:0**	**Default : 0x86**	**Access : R/W**
	-	7:4	Reserved.	
	NEWMOTYSEL	3	New motion Y selection.	
	NEWMOTYDIFFSEL	2	New motion Y difference selection.	
	STLMD_ECO[1:0]	1:0	Still mode selection.	
23h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
24h	**REG24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	3DMOTDET5F	1	3D motion detection uses 5 frames.	
	MOTYC_STILECO	0	Still image motion detection add MOTYC.	
25h ~ 2Dh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
2Eh	**REG2E**	**7:0**	**Default : 0x0C**	**Access : R/W**
	THDEM[7:0]	7:0	Threshold for 2D comb filter, check separated chroma complement with up/down line or not.	
2Fh	**REG2F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	NEWMOTYTH[3:0]	7:4	New motion Y threshold.	
	DEMOFFSET[3:0]	3:0	Threshold for 2D comb filter, check separated chroma complement with up/down line or not.	
30h	**REG30**	**7:0**	**Default : 0xA7**	**Access : R/W**
	MOTXEN	7	Extra reference of motion detection.	
	MOTXSEL	6	Extra motion mode.	
	MOTZEN	5	Ultra reference of motion detection.	
	LONG3D	4	Using 5 frame do Y/C separate.	
	MOTMD[1:0]	3:2	Motion different mode select.	
	DYNTHMD[1:0]	1:0	Dynamic threshold mode.	
31h	**REG31**	**7:0**	**Default : 0x20**	**Access : R/W**
	MOTYTHU[7:0]	7:0	Upper bound motion Y threshold.	
32h	**REG32**	**7:0**	**Default : 0x10**	**Access : R/W**
	MOTYTHL[7:0]	7:0	Lower bound motion Y threshold.	
33h	**REG33**	**7:0**	**Default : 0x20**	**Access : R/W**
	MOTCTHU[7:0]	7:0	Upper bound motion C threshold.	
34h	**REG34**	**7:0**	**Default : 0x10**	**Access : R/W**
	MOTCTHL[7:0]	7:0	Lower bound motion C threshold.	
35h	**REG35**	**7:0**	**Default : 0x20**	**Access : R/W**
	MOTTHX[7:0]	7:0	Extra motion threshold.	
36h	**REG36**	**7:0**	**Default : 0x30**	**Access : R/W**
	MOTTHZ[7:0]	7:0	Z-extra motion threshold.	
37h	**REG37**	**7:0**	**Default : 0x8C**	**Access : R/W**
	STLDET	7	Still image detection enable. 0: Disable. 1: Enable.	
	STLTH[6:0]	6:0	Still threshold.	
38h	**REG38**	**7:0**	**Default : 0x04**	**Access : R/W**
	MFMD[1:0]	7:6	Motion factor mode (MAX/AVG/MOTY/MOTC).	
	PAL3D_FLT_SEL	5	Use (DIFF+LPF) or (DIFF+MAX) in special domain.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	PAL3D_DIFF_SEL	4	Use (DIFF) or (DIFF+MAX) in time domain.	
	COMB_3DETPC_SEL	3	Use chroma diff for 3D entropy calculation.	
	STDTRSP[2:0]	2:0	Still image detect response time. 000: 1 field. 001: 2 field. 010~110: Reserved. 111: 128 field.	
39h	**REG39**	**7:0**	**Default : 0x02**	**Access : R/W**
	STLBK[7:0]	7:0	Motion level go back when find motion once.	
3Ah	**REG3A**	**7:0**	**Default : 0x30**	**Access : R/W**
	DYNTH[7:0]	7:0	Dynamic motion threshold.	
3Bh	**REG3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	NOISELVL[7:0]	7:0	Noise level for dynamic motion detection.	
3Ch	**REG3C**	**7:0**	**Default : 0x2F**	**Access : R/W**
	NEWMOTYEN	7	New motion Y enable.	
	NEWMOTCEN	6	New motion C enable.	
	NEWMOTCGAIN[1:0]	5:4	New motion C gain.	
	NEWMOTCTH[3:0]	3:0	New motion C threshold.	
3Dh	**REG3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMBASEADRH[7:0]	7:0	Base address of DRAM request (H).	
3Eh	**REG3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMBASEADRM[7:0]	7:0	Base address of DRAM request (M).	
3Fh	**REG3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMBASEADRL[7:0]	7:0	Base address of DRAM request (L).	
40h	**REG40**	**7:0**	**Default : 0x9C**	**Access : R/W**
		7:3	Reserved.	
	BLNKDETMD	2	Blank level detect mode. 0: Either 240 or 252. 1: 230~262 is possible.	
	VDETMD[1:0]	1:0	Vertical timing detect mode. 0x: Auto. 10: Force 525 line. 11: Force 625 line.	
41h	**REG41**	**7:0**	**Default : 0x08**	**Access : R/W**
	SENSSIGDET[7:0]	7:0	Sensitivity of signal detect.	

COMB Register (Bank = 36)				
Index	**Mnemonic**	**Bit**	**Description**	
42h	**REG42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SYNCLVLTLRN[7:0]	7:0	Sync level tolerance.	
43h	**REG43**	**7:0**	**Default : 0x60**	**Access : R/W**
	VCRCOASTLEN[7:0]	7:0	VCR coast length.	
44h	**REG44**	**7:0**	**Default : 0x80**	**Access : R/W**
	HBIDLY[7:0]	7:0	Horizontal blanking region position.	
45h ~ 47h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
48h	**REG48**	**7:0**	**Default : 0x20**	**Access : R/W**
	YCPIPE[1:0]	7:6	Y/C pipe delay.	
	DEGPIPE[1:0]	5:4	Degree pipe delay.	
	-	3:2	Reserved.	
	-	1:0	Reserved.	
49h	**REG3692**	**7:0**	**Default : 0x00**	**Access : R/W**
	FORCERATIO_SEL[7:0]	7:0	Force ratio selection.	
4Ah ~ 4Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
4Ch	**REG4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DBGMD32	5	Debug mode for 32 bit bus test.	
	DBGMD3D	4	Debug mode for 3D. 0: Normal. 1: Use motion factor as Y.	
	-	3:0	Reserved.	
4Dh	**REG4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBGPATTERN[7:0]	7:0	Debug pattern for 32-bit bus test.	
4Eh	**REG4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PIPDBGHST[1:0]	5:4	Motion factor pipeline control.	
	PIPCHKHST[3:0]	3:0	Motion history pipeline control.	
4Fh	**REG4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	3DBLUR_GAIN[4:0]	4:0	3D blur gain (1~1/16).	
50h	**REG50**	**7:0**	**Default : 0x07**	**Access : R/W**

COMB Register (Bank = 36)				
Index	**Mnemonic**	**Bit**	**Description**	
	DBG_2DCOMB_YCETP_SEL[1:0]	7:6	Selection of (ENTROPYH/EH4/EH2) / (ENTROPYV/EV2/EV1) / (ENTROPYV-H/SW_GAIN/CDET_SWGAIN) with d[5:4] = 2'd1/2'd2/2'd3.	
	DBG_2DCOMB_ENTROPY[1:0]	5:4	00: Normal. 01: Entropy H. 10: Entropy V. 11: Entropy V - Entropy H.	
	AUTOSTOPSYNC	3	Automatic stop H/V sync when no input.	
	LNFREEMD[2:0]	2:0	Line buffer free run mode. 000: Off (always synchronize). 001: 909 return. 010: 910 return. 011: 917 return. 100: 1127 return. 101: 1135 return. 110: Decided by register. 111: Automatic.	
51h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
52h	**REG52**	**7:0**	**Default : 0x8E**	**Access : R/W**
	HRETPOS[7:0]	7:0	Horizontal return position in line buffer free run mode.	
53h	**REG53**	**7:0**	**Default : 0x03**	**Access : R/W**
		7:3	Reserved.	
	HRETPOS[10:8]	2:0	Please see description of 52h.	
54h	**REG54**	**7:0**	**Default : 0x02**	**Access : R/W**
	TILTTLRN[7:0]	7:0	Line position tilt tolerance.	
55h	**REG55**	**7:0**	**Default : 0x04**	**Access : R/W**
	TTTLRN3D[7:0]	7:0	3D timing detection tolerance.	
56h	**REG56**	**7:0**	**Default : 0x40**	**Access : R/W**
	LCKSTEP[7:0]	7:0	3D lock counter go back distance when sync unstable.	
57h	**REG57**	**7:0**	**Default : 0x68**	**Access : R/W**
	LCK3DTHU[7:0]	7:0	3D timing detection threshold.	
58h	**REG58**	**7:0**	**Default : 0x40**	**Access : R/W**
	LCK3DTHL[7:0]	7:0	3D timing detection threshold.	
59h	**REG59**	**7:0**	**Default : 0x08**	**Access : R/W**

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	JITTLRN1[7:0]	7:0	Tolerance of HSYNC jitter.	
5Ah	**REG5A**	**7:0**	**Default : 0x20**	**Access : R/W**
	JITTLRN2[7:0]	7:0	Tolerance of HSYNC jitter.	
5Bh	**REG5B**	**7:0**	**Default : 0x10**	**Access : R/W**
	HSLCKTHU[7:0]	7:0	Upper bound threshold of hysteresis HSYNC lock counter.	
5Ch	**REG5C**	**7:0**	**Default : 0x08**	**Access : R/W**
	HSLCKTHL[7:0]	7:0	Lower bound threshold of hysteresis HSYNC lock counter.	
5Dh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
5Eh	**REG5E**	**7:0**	**Default : 0x14**	**Access : R/W**
	SYNCDLY[7:0]	7:0	HSYNC (from decoder to scaler) pipe delay.	
5Fh	**REG5F**	**7:0**	**Default : 0x80**	**Access : R/W**
	HSLDCNTMD[1:0]	7:6	H-sync lead counter mode.	
	CNTSTEPMD[1:0]	5:4	Counter step mode.	
	-	3:0	Reserved.	
60h	**REG60**	**7:0**	**Default : 0x00**	**Access : R/W**
	IFMD[1:0]	7:6	IF compensation mode.	
	IFCOEF[5:0]	5:0	IF compensation coefficient, 2-bit integer, 4-bit frac.	
61h ~ 63h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
64h	**REG64**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SAWCMP2D_EN	0	SAW compensation 2D enable.	
65h ~ 6Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
6Ch	**REG6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_MD	7	ACC mode selection.	
	-	6:4	Reserved.	
	CBINV	3	Cb inverse for S-video.	
	CRINV	2	Cr inverse for S-video.	
	-	1:0	Reserved.	
6Dh ~	**-**	**7:0**	**Default : -**	**Access : -**

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
6Fh	-	7:0	Reserved.	
70h	**REG70**	**7:0**	**Default : 0xF0**	**Access : R/W**
	-	7:6	Reserved.	
	CGMD[1:0]	5:4	Auto chroma gain mode. 00: Off. 01: Auto. 10: Manu. 11: MCU control.	
	BRSTFRAFEC	3	Burst height from AFEC.	
	-	2	Reserved.	
	DBG_GAIN_SEL[1:0]	1:0	Debug gain selection.	
71h	**REG71**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SAWCMPDETEN	7	SAW compensation detection enable.	
	-	6:0	Reserved.	
72h	**REG72**	**7:0**	**Default : 0x00**	**Access : R/W**
	BSTHGHT[7:0]	7:0	Burst height for auto chroma gain. 0: Auto, 112 for NTSC and 117 for PAL. Other: Use REGBSTHGHT/DETBSTHGHT as C gain.	
73h	**REG73**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTST[7:0]	7:0	Contrast adjustment coefficient.	
74h	**REG74**	**7:0**	**Default : 0x80**	**Access : R/W**
	BRHT[7:0]	7:0	Brightness adjustment coefficient.	
75h	**REG75**	**7:0**	**Default : 0x80**	**Access : R/W**
	SAT[7:0]	7:0	Saturation adjustment coefficient.	
76h ~ 77h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
78h	**REG78**	**7:0**	**Default : 0x80**	**Access : R/W**
	CRMAGAIN[7:0]	7:0	Chroma gain value for manual chroma gain.	
79h	**REG79**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CRMAGAIN[13:8]	5:0	Please see description of 79h.	
7Ah ~ 7Ch	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
7Dh	**REG7D**	**7:0**	**Default : 0x80**	**Access : R/W**
	SNOWDLY[7:0]	7:0	Latency of snow output after signal missing.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
7Eh	**REG7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ACC_CRMAGAIN_INC[2:0]	7:5	Chroma gain step of ACC.	
	ACCUPONLY	4	ACC up only.	
	ACCDLY[3:0]	3:0	ACC latency.	
7Fh	**REG7F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	ACCMAXGAIN[7:0]	7:0	ACC maximum gain.	
80h	**REG80**	**7:0**	**Default : 0xC8**	**Access : R/W**
	YGAIN[7:0]	7:0	Luma gain for U/V demodulation.	
81h	**REG81**	**7:0**	**Default : 0x96**	**Access : R/W**
	CBGAIN[7:0]	7:0	Cb gain for U/V demodulation.	
82h	**REG82**	**7:0**	**Default : 0x6A**	**Access : R/W**
	CRGAIN[7:0]	7:0	Cr gain for U/V demodulation.	
83h	**REG83**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	CTIMD[1:0]	5:4	CTI mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
	-	3:2	Reserved.	
	CBCRLPMD[1:0]	1:0	Cb/Cr low pass mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
84h	**REG84**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CTSTDITHEN	6	Dithering when contrast adjustment.	
	CTSTDITHPOS[1:0]	5:4	Dithering position (offset) of contrast.	
	-	3	Reserved.	
	SATDITHEN	2	Dithering when saturation adjustment.	
	SATDITHPOS[1:0]	1:0	Dithering position (offset) of saturation.	
85h	**REG85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	YDEMDITHEN	6	Dithering when demodulation Y gain.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
	YDEMDITHPOS[1:0]	5:4	Dithering position (offset) of Y gain.
	-	3	Reserved.
	CDEMDITHEN	2	Dithering when demodulation C gain.
	CDEMDITHPOS[1:0]	1:0	Dithering position (offset) of C gain.
86h ~ 8Ch	**-**	**7:0**	**Default : -** **Access : -**
	-	7:0	Reserved.
8Dh	**REG8D**	**7:0**	**Default : 0x00** **Access : R/W**
	COMBCTRL[7:0]	7:0	Some control signals for FPGA.
8Eh	**REG8E**	**7:0**	**Default : 0xE0** **Access : R/W**
	FPGACTRL[7:0]	7:0	Some control signals for FPGA.
8Fh	**-**	**7:0**	**Default : -** **Access : -**
	-	7:0	Reserved.
90h	**REG90**	**7:0**	**Default : 0x13** **Access : R/W**
	-	7:6	Reserved.
	YDETV_PATCH_EN	3	YDET patch V enable.
	MBS_V_HDIFF_EN	2	Jeff H MBS-C enable. 0: 1,0,2,0,1. 1: 2,0,0,0,-2.
	MIN_YDETH_EN	1	Minimum YDETH mode enable. 0: Normal. 1: Min (2tap,3tap).
	NEW_YDET_EN	0	CVBS low pass YDET enable.
91h	**REG91**	**7:0**	**Default : 0x12** **Access : R/W**
	YDIFFV1_LUMA_ENG_GAIN[1:0]	7:6	YDET V Luma gain (div 1/2/4/8).
	YDIFFV1_CRMA_ENG_GAIN[1:0]	5:4	YDET V Chroma gain (div 1/2/4/8).
	YDIFFH2_LUMA_ENG_GAIN[1:0]	3:2	YDET H Luma gain (div 1/2/4/8).
	YDIFFH2_CRMA_ENG_GAIN[1:0]	1:0	YDET H Chroma gain (div 1/2/4/8).
92h	**REG92**	**7:0**	**Default : 0x51** **Access : R/W**
	DET_FILTER_MD_H_B[1:0]	7:6	PAL H DET filter mode B. 00: LPF[1,2,-1]. 01~10: Reserved. 11: BPF[1,-1].
	-	5	Reserved.
	PAL_MBS_TAP_MD_H_B	4	PAL H multi-burst tap B. 0: 2 tap.

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
			1: 3 tap. Note: If we set [0], DET_FILTER_MD MUST set [11].
	-	3	Reserved.
	DET_FILTER_MD_H_A[1:0]	2:1	PAL H DET filter mode A. 00: LPF[1,2,-1]. 01~10: Reserved. 11: BPF[1,-1].
	PAL_MBS_TAP_MD_H_A	0	PAL H multi-burst tap A. 0: 2 tap. 1: 3 tap. Note: If we set [0], DET_FILTER_MD must set as "11".
93h	**REG93**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:3	Reserved.
	DET_FILTER_MD_V[1:0]	2:1	PAL V DET filter mode. 0: 2 tap mode: 2,0,-2/0,2,-2. 1: 3 tap mode: 1,1,-2/0,2,-2.
	PAL_MBS_TAP_MD_V	0	PAL V multi-burst tap. 0: 2 tap. 1: 3 tap.
94h	**REG94**	**7:0**	**Default : 0x00** **Access : R/W**
	MB_GAIN_H[3:0]	7:4	YDET patch H multi-burst gain (multiply 1~16).
	C_GAIN_H[1:0]	3:2	YDET patch H Chroma gain (divide 2, 4, 8, 16).
	ENG_SCALE[1:0]	1:0	YDET patch multi-burst-Chroma energy scale (multiply 4/8/16/32).
95h	**REG95**	**7:0**	**Default : 0xCC** **Access : R/W**
	CDET_V_LUMA_ENG_GAIN[1:0]	7:6	CDET V Luma gain (multiply 1/2/4/8).
	CDET_V_CRMA_ENG_GAIN[1:0]	5:4	CDET V Chroma gain (multiply 1/2/4/8).
	CDET_H_LUMA_ENG_GAIN[1:0]	3:2	CDET H Luma gain (multiply 1/2/4/8).
	CDET_H_CRMA_ENG_GAIN[1:0]	1:0	CDET H Chroma gain (multiply 1/2/4/8).
96h	**REG96**	**7:0**	**Default : 0x00** **Access : R/W**
	CDET_SWITCH_THR[7:0]	7:0	CDET switch threshold.
97h	**REG97**	**7:0**	**Default : 0x00** **Access : R/W**
	CDET_SWITCH_STEP[1:0]	7:6	CDET switch step (multiply 1/2/4/8).
	-	5:0	Reserved.
98h	**REG98**	**7:0**	**Default : 0x2A** **Access : R/W**
	PAL_2DCNCH_MD[1:0]	7:6	PAL Chroma 2D 9x5 mode.

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
			00: V12221. 01:14641. 1x: 01210.
	PAL_DIFFV2_SEL	5	CVDiff V2 select for PAL. 0: Blend (max2, DiffUD). 1: Max (max2, DiffUD).
	LPF_FACTOR[4:0]	4:0	CVBS low pass blending factor.
99h	**REG99**	**7:0**	**Default : 0x01** **Access : R/W**
	CVH2PATCH_EN	7	SC's diagonal patch enable (NTSC443 only).
	CVDIFF_H2_GAIN[2:0]	6:4	SC's diagonal patch gain (multiply 1/0.5/0.25/0.125//0.0625/0.03125/2/4).
	PAL_DIFFV1_SEL	3	PAL CVDIFF v1 select. 0: Ian v1. 1: Jeff v1.
	PAL_CVDIFF_V2_GAIN[2:0]	2:0	CVDIFF v2 gain for PAL (multiply 0/1/2/4/8/0.5/0.25/0.125).
9Ah	**REG9A**	**7:0**	**Default : 0x03** **Access : R/W**
	AMPV1_GAIN[3:0]	7:4	AMP_YDIFF_V1 gain (div 8/16/24/32/40/48/56/64/80/96/112/128/160/192/224/256).
	AMPH2_GAIN[3:0]	3:0	AMP_YDIFF_H2 gain (div 8/16/24/32/40/48/56/64/80/96/112/128/160/192/224/256).
9Bh	**REG9B**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:5	Reserved.
	CHROMA_ADPBLD_SEL	4	Chroma fix select for adaptive Chroma blending. 0: Original. 1: 12221Fix.
	YDETHBND_TH[2:0]	3:1	YDET H bound TH by Reg.
	YDETHBND_EN	0	YDET H bound enable by Reg.
9Ch	**REG9C**	**7:0**	**Default : 0x01** **Access : R/W**
	-	7	Reserved..
	V5DBG_EN	6	Entropy V5 debug mode enable (use V2).
	V5FLT_SEL	5	Entropy V5 filter select. 0: Max. 1: LP12221.
	PALETPV_SEL	4	PAL entropy V select.

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
			0: Original. 1: Entropy V5.	
	ETP_H2GAIN[1:0]	3:2	Entropy H2 gain (multiply 1/2/4/8).	
	PALV1_EN	1	Disable PAL V1 calculation in PAL (for PAL use only).	
	H2V1_EN	0	H2 v1 enable. 0: Disable. 1: Enable.	
9Dh	**REG9D**	**7:0**	**Default : 0x08**	**Access : R/W**
	EV2_PROCFLT_SEL[1:0]	7:6	Entropy V2 proc filter select. 00: Original. 01: LP121 (NTSC only). 10: M_MAXMIN. 11: LP12221 M_CVDIFFV2.	
	-	5	Reserved.	
	EH4_PROCFLT_SEL	4	Entropy H4 proc filter select. 0: Original. 1: LP12221.	
	EV1_POSTFLT_SEL	3	Entropy V1 post filter select. 0: Original. 1: LP121.	
	EV1_PROCFLT_SEL	2	Entropy V1 proc filter select. 0: Original. 1: Min/Max.	
	EH2_POSTFLT_SEL	1	Entropy H2 post filter select. 0: Max. 1: LP12221.	
	EH2_PROCFLT_SEL	0	Entropy H2 proc filter select. 0: Original. 1: Min/Max.	
9Eh	**REG9E**	**7:0**	**Default : 0xC1**	**Access : R/W**
	IAN_MAXEH4_GAIN[1:0]	7:6	T-cross patch H4 gain (1/2/4/8).	
	IAN_MAXEH2_GAIN[1:0]	5:4	T-cross patch H2 gain (1/2/4/8).	
	-	3:1	Reserved.	
	IAN_EV_EN	0	T-cross patch V enable.	
9Fh	**REG9F**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	SAWBLENDDIV[4:0]	4:0	SAW blend division.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
A0h	**REGA0**	**7:0**	**Default : 0x48**	**Access : R/W**
	ADP9X5_CSWEN	7	Adaptive 9X5 use CDET switch gain enable.	
	ADPGAIN_SCUP_EN	6	Adaptive 9x5 scale up enable.	
	REFER_3X3LRDIFF_EN	5	Adaptive 9x5 reference adaptive 3x3 difference enable (for LR Diff).	
	REFER_H4_EN	4	Adaptive 3x3 reference adaptive 9x5 difference enable (for LR Diff).	
	ADPCRMA_SEL	3	Adaptive Chroma select. 0: 14641. 1: 12221).	
	ADPLUMA_SEL	2	Adaptive Luma select. 0: 14641. 1: 12221.	
	ADP2DSEL[1:0]	1:0	Adaptive mode (9x5/9x3/3x5/3x3).	
A1h	**REGA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADPGAINLR1P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR0P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A2h	**REGA2**	**7:0**	**Default : 0x21**	**Access : R/W**
	ADPGAINLR3P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR2P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A3h	**REGA3**	**7:0**	**Default : 0x84**	**Access : R/W**
	ADPGAINLR5P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR4P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A4h	**REGA4**	**7:0**	**Default : 0xEC**	**Access : R/W**
	ADPGAINLR7P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR6P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A5h	**REGA5**	**7:0**	**Default : 0x0F**	**Access : R/W**
	ADPGAINLR9P[3:0]	7:4	Adp3x3 gain lookup LR table.	
	ADPGAINLR8P[3:0]	3:0	Adp3x3 gain lookup LR table.	
A6h	**REGA6**	**7:0**	**Default : 0x60**	**Access : R/W**
	-	7	Reserved.	
	ADPGAINLR8TOAP[2:0]	6:4	Adp3x3 gain lookup LR table (Sign Bit), 8~AP[4].	
	ADPGAINLRAP[3:0]	3:0	Adp3x3 gain lookup LR table.	
A7h	**REGA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADPGAINLR0TO7P[7:0]	7:0	Adp3x3 gain lookup LR table (Sign Bit), 0~7P[4].	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
A8h	**REGA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADPGAINUD1P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD0P[3:0]	3:0	Adp3x3 gain lookup UD table.	
A9h	**REGA9**	**7:0**	**Default : 0x21**	**Access : R/W**
	ADPGAINUD3P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD2P[3:0]	3:0	Adp3x3 gain lookup UD table.	
AAh	**REGAA**	**7:0**	**Default : 0x84**	**Access : R/W**
	ADPGAINUD5P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD4P[3:0]	3:0	Adp3x3 gain lookup UD table.	
ABh	**REGAB**	**7:0**	**Default : 0xEC**	**Access : R/W**
	ADPGAINUD7P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD6P[3:0]	3:0	Adp3x3 gain lookup UD table.	
ACh	**REGAC**	**7:0**	**Default : 0x0F**	**Access : R/W**
	ADPGAINUD9P[3:0]	7:4	Adp3x3 gain lookup UD table.	
	ADPGAINUD8P[3:0]	3:0	Adp3x3 gain lookup UD table.	
ADh	**REGAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	ADPGAINUD8TOAP[2:0]	6:4	Adp3x3 gain lookup UD table (sign bit), 8~AP[4].	
	ADPGAINUDAP[3:0]	3:0	Adp3x3 gain lookup UD table.	
AEh	**REGAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADPGAINUD0TO7P[7:0]	7:0	Adp3x3 gain lookup UD table (sign bit), 0~7P[4].	
B0h	**REGB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ADP9X5_DBGSEL[2:0]	2:0	Adaptive 9x5 debug output select.	
B1h	**REGB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN0[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B2h	**REGB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN1[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B3h	**REGB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	ADP9X5GAIN2[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).	
B4h	**REGB4**	**7:0**	**Default : 0x0C**	**Access : R/W**

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
	-	7:6	Reserved.
	ADP9X5GAIN3[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).
B5h	**REGB5**	**7:0**	**Default : 0x0F** **Access : R/W**
	-	7:6	Reserved.
	ADP9X5GAIN4[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).
B6h	**REGB6**	**7:0**	**Default : 0x10** **Access : R/W**
	-	7:6	Reserved.
	ADP9X5GAIN5[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).
B7h	**REGB7**	**7:0**	**Default : 0x11** **Access : R/W**
	-	7:6	Reserved.
	ADP9X5GAIN6[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).
B8h	**REGB8**	**7:0**	**Default : 0x14** **Access : R/W**
	-	7:6	Reserved.
	ADP9X5GAIN7[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).
B9h	**REGB9**	**7:0**	**Default : 0x20** **Access : R/W**
	-	7:6	Reserved.
	ADP9X5GAIN8[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).
BAh	**REGBA**	**7:0**	**Default : 0x20** **Access : R/W**
	-	7:6	Reserved.
	ADP9X5GAIN9[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).
BBh	**REGBB**	**7:0**	**Default : 0x20** **Access : R/W**
	-	7:6	Reserved.
	ADP9X5GAIN10[5:0]	5:0	Adp9x5 gain lookup table (0~32) <=> (-16~16).
C0h	**REGC0**	**7:0**	**Default : 0xA0** **Access : R/W**
	CRMA2D_SEL[1:0]	7:6	Chroma 2D Select (5x5/5x5/ADP/DEMBLD).
	LUMA2D_SEL[1:0]	5:4	Luma 2D Select (5x5/5x5/ADP/adaptive).
	CRMAOUT_MD[1:0]	3:2	Chroma output mode. 00: Normal. 01: 1DH. 10: 1DV. 11: 2D.
	LUMAOUT_MD[1:0]	1:0	Luma output mode. 00: Normal. 01: 1DH. 10: 1DV.

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
			11: 2D.	
C1h	**REGC1**	**7:0**	**Default : 0x33**	**Access : R/W**
	YETPV_GAIN[3:0]	7:4	Luma Entropy gain V for lookup table (multiply (1~16)/4).	
	YETPH_GAIN[3:0]	3:0	Luma Entropy gain H for lookup table (multiply (1~16)/4).	
C2h	**REGC2**	**7:0**	**Default : 0x33**	**Access : R/W**
	CETPV_GAIN[3:0]	7:4	Chroma entropy gain V for lookup table (multiply (1~16)/4).	
	CETPH_GAIN[3:0]	3:0	Chroma Entropy gain H for lookup table (multiply (1~16)/4).	
C3h	**REGC3**	**7:0**	**Default : 0x1F**	**Access : R/W**
	-	7:5	Reserved.	
	AUTO2D_EN	4	When it is unknown TV system, force 2D output enable.	
	CETP_SCDN_EN	3	Chroma entropy scaled down enable.	
	CETP_SCUP_EN	2	Chroma entropy scaled up enable.	
	YETP_SCDN_EN	1	Luma entropy scaled down enable.	
	YETP_SCUP_EN	0	Luma entropy scaled up enable.	
C4h (3688h)	**REG3688**	**7:0**	**Default : 0x00**	**Access : R/W**
	YBLD_FORCE_SW_GAIN[3:0]	7:4	Luma blending forced switch gain (0~128).	
		3:1	Reserved.	
	YBLD_FORCE_SW	0	Luma blending forced switch enable.	
C5h	**REGC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	CROSSPT_EN	7	Cross point patch enable.	
	-	6	Reserved.	
	CROSSPT_DEBUG[1:0]	5:4	Cross point patch debug mode.	
	CROSSPOINT_CSHIFT[1:0]	3:2	Cross point C shift.	
	CMBRATIO_A[1:0]	1:0	Cross point patch, Chroma multi-burst ratio A.	
C6h	**REGC6**	**7:0**	**Default : 0x20**	**Access : R/W**
	YGAINYH1P[3:0]	7:4	Luma gain lookup table YH.	
	YGAINYH0P[3:0]	3:0	Luma gain lookup table YH.	
C7h	**REGC7**	**7:0**	**Default : 0x85**	**Access : R/W**
	YGAINYH3P[3:0]	7:4	Luma gain lookup table YH.	
	YGAINYH2P[3:0]	3:0	Luma gain lookup table YH.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
C8h	**REGC8**	**7:0**	**Default : 0x88**	**Access : R/W**
	YGAINYH5P[3:0]	7:4	Luma gain lookup table YH.	
	YGAINYH4P[3:0]	3:0	Luma gain lookup table YH.	
C9h	**REGC9**	**7:0**	**Default : 0x88**	**Access : R/W**
	YGAINYH7P[3:0]	7:4	Luma gain lookup table YH.	
	YGAINYH6P[3:0]	3:0	Luma gain lookup table YH.	
CAh	**REGCA**	**7:0**	**Default : 0x20**	**Access : R/W**
	YGAINYV1P[3:0]	7:4	Luma gain lookup table YV.	
	YGAINYV0P[3:0]	3:0	Luma gain lookup table YV.	
CBh	**REGCB**	**7:0**	**Default : 0x85**	**Access : R/W**
	YGAINYV3P[3:0]	7:4	Luma gain lookup table YV.	
	YGAINYV2P[3:0]	3:0	Luma gain lookup table YV.	
CCh	**REGCC**	**7:0**	**Default : 0x88**	**Access : R/W**
	YGAINYV5P[3:0]	7:4	Luma gain lookup table YV.	
	YGAINYV4P[3:0]	3:0	Luma gain lookup table YV.	
CDh	**REGCD**	**7:0**	**Default : 0x88**	**Access : R/W**
	YGAINYV7P[3:0]	7:4	Luma gain lookup table YV.	
	YGAINYV6P[3:0]	3:0	Luma gain lookup table YV.	
CEh	**REGCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CMPSEL[3:0]	3:0	CMP selection.	
CFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
D0h	**REGD0**	**7:0**	**Default : 0xB9**	**Access : R/W**
	PEAKING_PALCMP_INV	7	Peaking PALCMP inverse.	
	IAN_ENH_CLIP[2:0]	6:4	Clipping TH (0/16/32/64/96/128/160/192).	
	IAN_ENH_CORING[1:0]	3:2	Coring TH (0/4/8/16).	
	NTSC_PEAKING_SEL	1	NTSC peaking method select. 0: Ian mode. 1: X mode.	
	IAN_ENH_PEAKING_EN	0	Ian enhanced peaking enable.	
D1h	**REGD1**	**7:0**	**Default : 0x40**	**Access : R/W**
	IAN_ENH_Y1GAIN[7:0]	7:0	Y1 gain (div(16~128) >>3).	
D2h	**REGD2**	**7:0**	**Default : 0x40**	**Access : R/W**

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
	IAN_ENH_Y2GAIN[7:0]	7:0	Y2 gain (div(16~128) >>3).	
D3h	**REGD3**	**7:0**	**Default : 0x60**	**Access : R/W**
	IAN_ENH_Y3GAIN[7:0]	7:0	Y3 gain (div(16~128) >>3).	
D4h	**REGD4**	**7:0**	**Default : 0x20**	**Access : R/W**
	IAN_MIN_CDIFFH[7:0]	7:0	Peaking minimum C difference horizontal.	
D5h	**REGD5**	**7:0**	**Default : 0x08**	**Access : R/W**
	IAN_MIN_CDIFFV[7:0]	7:0	Peaking minimum C difference vertical.	
D6h	**REGD6**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:4	Reserved.	
	IAN_CDIFFV_RANGE[1:0]	3:2	Peaking C difference vertical range (16/32/64/128).	
	IAN_CDIFFH_RANGE[1:0]	1:0	Peaking C difference horizontal range (16/32/64/128).	
DAh	**REGDA**	**7:0**	**Default : 0x01**	**Access : R/W**
	DBG_FP_MD[3:0]	7:4	Final patch debug mode. [3]: Debug enable (1). [2:1]: VDiff(0)/HDiff(1)/Gain(2). [0]: Up(0)/Down(1).	
	-	3:1	Reserved.	
	FINALPATCH_EN	0	Ian final patch enable.	
DBh	**REGDB**	**7:0**	**Default : 0x42**	**Access : R/W**
	-	7	Reserved.	
	IAN_PLHDIFF_SC[2:0]	6:4	Ian pure Luma H-diff scale select (multiply 0/0.125/0.25/0.5/1/2/4/8).	
	-	3	Reserved.	
	IAN_PLHDIFF_TH[2:0]	2:0	Ian pure Luma H-diff threshold select (32/64/128/256).	
DCh	**REGDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	IAN_DIFF_SHIFTD[1:0]	7:6	Ian pure Luma D diff shift (div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_SHIFTU[1:0]	5:4	Ian pure Luma U diff shift (div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_MSHTD[1:0]	3:2	Ian pure Luma D diff shift (div 1/2/4/8) before TH.	
	IAN_DIFF_MSHTU[1:0]	1:0	Ian pure Luma U diff shift (div 1/2/4/8) before TH.	
DDh	**REGDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	IAN_TH_VER[7:0]	7:0	Ian pure Luma TH_VER (25): U/D diff threshold for detection.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description	
DEh	**REGDE**	**7:0**	**Default : 0x05**	**Access : R/W**
	PLHDIFF_TH[7:0]	7:0	Pure Luma H difference threshold.	
E0h	**REGE0**	**7:0**	**Default : -**	**Access : RO**
	HSLOCK	7	HSYNC lock happen.	
	LOCK3D	6	Good timing happen.	
	MEMRDBWEVN	5	Memory read bandwidth not enough.	
	MEMWRBWEVN	4	Memory write bandwidth not enough.	
	NOTHSLOCK	3	HSYNC unlock happen.	
	NOTLOCK3D	2	Good timing disappear.	
	HSCHG	1	HSYNC counter change.	
	MEMBWEVN	0	DRAM bandwidth not enough.	
E1h	**REGE1**	**7:0**	**Default : -**	**Access : RO**
	STLIMG	7	Still image happen.	
	NOTSTLIMG	6	Still image disappear.	
	CCHNLACT	5	C-channel active (maybe S-video input).	
	NOTCCHNLACT	4	C-channel quiet (maybe CVBS input).	
	-	3	Reserved.	
	FLDCNTCHG	2	Field counter change.	
	-	1:0	Reserved.	
E2h	**REGE2**	**7:0**	**Default : -**	**Access : RO**
	LN525	7	525 line system.	
	LN625	6	625 line system.	
	F358	5	3.58 MHz system.	
	F443	4	4.43 MHz system.	
	NOINPUT	3	No input.	
	VDOMD[2:0]	2:0	Video mode. 0: NTSC_M. 1: NTSC_443. 2: PAL_M. 3: PAL_BDGHIN. 4: PAL_NC. 5: PAL_60. 6: Input without burst. 7: Unknown.	
E3h	**REGE3**	**7:0**	**Default : -**	**Access : RO**

COMB Register (Bank = 36)				
Index	**Mnemonic**	**Bit**	**Description**	
	IRQ_FINAL_STS[1:0]	7:6	Raw IRQ status.	
	IRQ_RAW_STS[1:0]	5:4	Final IRQ status.	
	-	3:1	Reserved.	
	INTERLACE	0	Interlace input.	
E4h	**REGE4**	**7:0**	**Default : -**	**Access : RO**
	DETBLANK[7:0]	7:0	Detected blank level.	
E5h	**REGE5**	**7:0**	**Default : -**	**Access : RO**
	CURBLANK[7:0]	7:0	Current used blank level.	
E6h	**REGE6**	**7:0**	**Default : -**	**Access : RO**
	SYNCLVL[7:0]	7:0	Detected sync level.	
E7h	**REGE7**	**7:0**	**Default : -**	**Access : RO**
	SYNCHGHT[7:0]	7:0	Detected sync height.	
E8h	**REGE8**	**7:0**	**Default : -**	**Access : RO**
	BURSTHGHT[7:0]	7:0	Detected burst height.	
E9h	**REGE9**	**7:0**	**Default : -**	**Access : RO**
	DETHORTOTAL[7:0]	7:0	Detected horizontal total.	
EAh	**REGEA**	**7:0**	**Default : -**	**Access : RO**
	DETHORTOTAL[15:8]	7:0	Please see description of '36D2h'.	
EBh	**REGEB**	**7:0**	**Default : -**	**Access : RO**
	RPTCOVFH[7:0]	7:0	Reported chroma overflow count per line.	
ECh	**REGEC**	**7:0**	**Default : -**	**Access : RO**
	RPTCOVFV[7:0]	7:0	Reported chroma overflow count per field.	
EDh ~ FFh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

VBI Register (Bank = 37)

VBI Register (Bank = 37)				
Index	**Mnemonic**	**Bit**	**Description**	
01h ~ 0Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
10h	**REG10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TTDECRST	1	Teletext decoder software reset.	
	TTEN	0	Teletext enable. 0: Disable. 1: Enable.	
11h	**REG11**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMASRC_ADR_7_0	7:0	DMA source linear address (lower 8 bits).	
12h	**REG12**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMASRC_ADR_15_8	7:0	DMA source linear address (middle 8 bits).	
13h	**REG13**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMASRC_ADR_23_16	7:0	DMA source linear address (upper 8 bits).	
14h	**REG14**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMADES_ADR_7_0	7:0	DMA destination linear address (lower 8 bits).	
15h	**REG15**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMADES_ADR_15_8	7:0	DMA destination linear address (middle 8 bits).	
16h	**REG16**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMADES_ADR_23_16	7:0	DMA destination linear address (upper 8 bits).	
17h	**REG17**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMAQW_CNT_7_0	7:0	DMA block move count (unit: 8 bytes; lower 8 bits).	
18h	**REG18**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMAQW_CNT_15_8	7:0	DMA block move count (unit: 8 bytes; upper 8 bits).	
19h	**REG19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMA_FUNC	4:0	DMA function.	
1Ah	**REG1A**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7:2	Reserved.	
	DMA_RDY	1	DMA ready status.	
	DMA_FIRE	0	DMA engine fire signal.	
1Bh	**REG1B**	**7:0**	**Default : 0x20**	**Access : R/W**
	DMAERASE_DAT	7:0	DMA erase data.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
1Ch	**REG1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TAG_INT_EN	2	Tag interrupt enable.	
	DMA_INT_EN	1	DMA interrupt enable.	
	VBI_INT_EN	0	VBI interrupt enable.	
1Eh	**REG1E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DMA_WBE_PRE	7:4	DMA previous write byte enable.	
	DMA_WBE_POST	3:0	DMA post write byte enable.	
1Fh	**REG1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DC_RAW	3	Designation code raw data mode.	
	VBI_HEADER_RAW	2	VBI header raw data mode.	
	VBI_ALL_RAW	1	VBI data raw data mode.	
	SRH_ENG_CLEAR	0	Tag search engine clear.	
20h	**REG20**	**7:0**	**Default : -**	**Access : RO**
	VBIREADY	7	VBI line end and teletext slicer ready indication.	
	-	6:5	Reserved.	
	VBI_LN_CNT	4:0	VBI line counter.	
21h	**REG21**	**7:0**	**Default : -**	**Access : RO**
	TTSLICERRDY	7	Teletext slicer ready indication.	
	VBI_FIELD_CNT_6_0	6:0	VBI field counter.	
22h	**REG22**	**7:0**	**Default : 0x00**	**Access : R/W**
	BURST_RE_MD	7	Burst read mode enable.	
	BURST_WE_MD	6	Burst write mode enable.	
	MCU_ADR_PORT	5:0	MCU memory access address port.	
23h	**REG23**	**7:0**	**Default : 0x00**	**Access : R/W**
	MCU_DATA_PORT	7:0	MCU memory access data port.	
24h	**REG24**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAGRW_POS_7_0	7:0	Tag read/write position (lower 8 bits).	
25h	**REG25**	**7:0**	**Default : 0x00**	**Access : R/W**
	TAG_PT_DELTA32	7:4	Tag length 32 delta.	
	TAGRW_POS_11_8	3:0	Tag read/write position (upper 4 bits).	
26h	**REG26**	**7:0**	**Default : -**	**Access : RO**
	PAGEBUF_ADDR_7_0	7:0	Page buffer linear address (lower 8 bits).	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
27h	**REG27**	**7:0**	**Default : -**	**Access : RO**
	PAGEBUF_ADDR_15_8	7:0	Page buffer linear address (middle 8 bits).	
28h	**REG28**	**7:0**	**Default : -**	**Access : RO**
	PAGEBUF_ADDR_23_16	7:0	Page buffer linear address (upper 8 bits).	
29h	**REG29**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAGEBUF_CNT_7_0	7:0	Pager buffer counter (lower 8 bits).	
2Ah	**REG2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PAGEBUF_CNT_11_8	3:0	Pager buffer counter (upper 4 bits).	
2Bh	**REG2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FW_SEARCH_SEL	3	MCU memory access data switch to FW search result data.	
	CYC_DISABLE	2	Disable cyclic search when touch physical size.	
	SEARCH_NOSUB	1	Search without sub-code.	
	REQ_64	0	The length of search request. 0->32; 1->64.	
2Ch	**REG2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAGAZINE	3:0	Magazine.	
2Dh	**REG2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAGE_TENS	7:4	Page number tens.	
	PAGE_UNITS	3:0	Page number units.	
2Eh	**REG2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CODE4	5:4	Sub-code S4.	
	SUB_CODE3	3:0	Sub-code S3.	
2Fh	**REG2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_CODE2	6:4	Sub-code S2.	
	SUB_CODE1	3:0	Sub-code S1.	
30h	**REG30**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TAG_BASE_15_8	7:0	Tag base address.	
31h	**REG31**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TAG_BASE_23_16	7:0	Tag base address.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
32h	**REG32**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAGE_BASE_15_8	7:0	Page base address.	
33h	**REG33**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAGE_BASE_23_16	7:0	Page base address.	
34h	**REG34**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAGE_SIZE	7:0	One page size.	
35h	**REG35**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TAG_PHY_SIZE	7:0	Tag physical size (lower 8 bits).	
36h	**REG36**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	TAG_PHY_SIZE_11_8	3:0	Tag physical size (upper 4 bits).	
37h	**REG37**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7:4	Reserved.	
	BUF_ADDR_RDY	3	Page buffer linear address ready.	
	HIT_STS	2	Search hit status.	
	TAG_RDY	1	Tag ready status.	
	TAG_FIRE	0	Tag engine fire signal.	
38h	**REG38**	**7:0**	**Default : 0x00**	**Access : R/W**
	TTBASEADDR2_7_0	7:0	Teletext base address 2 (lower 8 bits).	
39h	**REG39**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTBASEADDR2_15_8	7:0	Teletext base address 2 (middle 8 bits).	
3Ah	**REG3A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TTBASEADDR2_23_16	7:0	Teletext base address 2 (upper 8 bits).	
3Bh	**REG3B**	**7:0**	**Default : 0x12**	**Access : R/W**
	TTVBIBUFLEN_7_0	7:0	Teletext VBI buffer length (lower 8 bits).	
3Ch	**REG3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TTVBIBUFLEN_15_8	7:0	Teletext VBI buffer length (upper 8 bits).	
3Dh	**REG3D**	**7:0**	**Default : -**	**Access : RO**
	TTPKTCNT_7_0	7:0	Teletext packet counter (lower 8 bits).	
3Eh	**REG3E**	**7:0**	**Default : -**	**Access : RO**
	TTPKTCNT_15_8	7:0	Teletext packet counter (upper 8 bits).	
40h	**REG40**	**7:0**	**Default : 0x21**	**Access : R/W**
	CRIAMPTHDL_9_8	7:6	Closed caption clock run-in amplitude L (upper 2 bits).	
	CCLNSTR1_4_3	5:4	Closed caption line start 1 (upper 2 bits).	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	CRIDETENNUM_10_8	3:1	Closed caption clock run-in detection enable number (upper 3 bits).	
	SLCTHDMD	0	Closed caption slicer threshold mode.	
41h	**REG41**	**7:0**	**Default : 0x52**	**Access : R/W**
	CCLNSTR1_2_0	7:5	Closed caption line start 1 (lower 3 bits).	
	CCLNEND1	4:0	Closed caption line end 1.	
42h	**REG42**	**7:0**	**Default : 0x1C**	**Access : R/W**
	CCINTTYPE	7	Closed caption interrupt type. 0: Assert 8T after CC line in even field if CC is found. 1: According to CCREQ.	
	-	6:0	Reserved.	
43h	**REG43**	**7:0**	**Default : 0xA8**	**Access : R/W**
	CRIDETENNUM_7_0	7:0	Closed caption clock run-un detection enable number (lower 8 bits).	
44h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
45h	**REG45**	**7:0**	**Default : 0xA0**	**Access : R/W**
	CRIAMPTHDL_7_0	7:0	Closed caption clock run-in amplitude L (lower 8 bits).	
46h	**REG46**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CCFRAMTRIGNUM_4_0	5:1	Closed caption frame trigger number. This controls CCFRAMTRIG (VBI_IRQ_STS[3]). When CCFRAMCNT == CCFRAMTRIGNUM, CCFRAMTRIG would be asserted.	
	CCEN	0	Closed caption enable.	
47h ~ 4Eh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
4Fh	**REG4F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	CRIAMPTHDH_7_0	7:0	Closed caption clock run-in amplitude upper threshold (lower 8 bits).	
50h	**REG50**	**7:0**	**Default : 0x72**	**Access : R/W**
	CRIAMPTHDH_9_8	7:6	Closed caption clock run-in amplitude upper threshold (upper 2 bits).	
	CCCRIZCTYPE	5	Closed caption CRI zero crossing type. 1: positive edge ; 0: negative edge.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	CCLNSTR2	4:0	Closed caption line start 2.	
51h	**REG51**	**7:0**	**Default : 0xB2**	**Access : R/W**
	-	7:5	Reserved.	
	CCLNEND2	4:0	Closed caption line end 2.	
52h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
53h	**REG53**	**7:0**	**Default : 0x90**	**Access : R/W**
	CCSCWINLEN	7:0	Closed caption start code checking window length.	
54h	**REG54**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	CCSTRCODEMSK	5:3	Closed caption start code mask. 1: mask(ignore) ; 0: normal.	
	CCSTRCODE	2:0	Closed caption start code.	
55h	**REG55**	**7:0**	**Default : -**	**Access : RO**
	-	7:2	Reserved.	
	CCBYTEERRH	1	Closed caption byte error (upper part).	
	CCBYTEERRL	0	Closed caption byte error (lower part).	
56h	**REG56**	**7:0**	**Default : -**	**Access : RO**
	CCODDFOUND	7	Closed caption odd byte found indication.	
	CCEVENFOUND	6	Closed cation even byte found indication.	
	-	5	Reserved.	
	CCFRAMCNT	4:0	Closed caption frame counter.	
57h	**REG57**	**7:0**	**Default : -**	**Access : RO**
	CCBYTES_7_0	7:0	Closed caption bytes (lower 8 bits).	
58h	**REG58**	**7:0**	**Default : -**	**Access : RO**
	CCBYTES_15_8	7:0	Closed caption bytes (upper 8 bits).	
5Bh	**REG5B**	**7:0**	**Default : -**	**Access : RO**
	CC_PACKET_COUNTER	7:0	Closed caption packet counter.	
5Ch	**REG5C**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7	Reserved.	
	CCBUFLEN	6:0	Closed caption buffer length.	
5Dh	**REG5D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CCBASEADDR_23_16	7:0	Closed caption base address (upper 8 bits).	
5Eh	**REG5E**	**7:0**	**Default : 0xFF**	**Access : R/W**

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	CCBASEADDR_15_8	7:0	Closed caption base address (middle 8 bits).	
5Fh	**REG5F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	CCBASEADDR_7_0	7:0	Closed caption base address (lower 8 bits).	
68h ~ 69h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	-	
6Ah	**REG6A**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	TT2KPMD	4:3	Teletext two KP mode. 00, 01: Disable. 10: Using 2nd KP value when the difference of TTINTP zero crossing value is smaller than TTINPTZXTH each line. 11: Using 2nd KP value when the difference of TTINTP zero crossing value is smaller than TTINPTZXTH each field.	
	TTKPSEL2ND	2:0	Teletext DPLL phase error gain selection 2nd parameter. 000: 2^-9. 001: 2^-10. 010: 2^-11. 011: 2^-12. 100: 2^-13. 101: 2^-14. 110: 2^-15. 111: 2^-16.	
6Bh	**REG6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBI_IRQ_FORCE	7:0	VBI interrupt request force bits.	
6Ch	**REG6C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VBI_IRQ_MSK	7:0	VBI interrupt request mask bits.	
6Dh	**REG6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBI_IRQ_CLR	7:0	VBI interrupt request clear bits.	
6Eh	**REG6E**	**7:0**	**Default : -**	**Access : RO**
	VBI_IRQ_STS	7:0	VBI interrupt request status report.	
6Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	-	
70h	**REG70**	**7:0**	**Default : 0x00**	**Access : R/W**

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
	VPS_WSS_EN	7	VPS/WSS enable. 0: Disable. 1: Enable.
	VPS_EACHFLD	6	VPS each field option. 0: Only detect in odd field. 1: Detect in odd and even field.
	WSS_EACHFLD	5	WSS each field option. 0: Only detect in odd field. 1: Detect in odd and even field.
	-	4	Reserved.
	VBI_RST	3	VBI software reset.
	TTINTTYPE	2:1	Teletext interrupt type. [1]: 0: Assert 8T cycle. 1: Wait TTX_INTACK to clear the assertion. [0]: 0: Interrupt is issued when Teletext slicer is ready after Teletext available lines. 1: Interrupt is issued after Teletext available lines no matter whether there is Teletext data.
	TTEN2	0	Teletext forced enable bit. Teletext function could be enabled by two ways. The formal way is enabled from internal MCU and stable VD state is necessary. The other way is enabled by this bit directly.
71h	**REG71**	**7:0**	**Default : 0xA0** **Access : R/W**
	TT_INI_CRIWIN_STRPT	7:0	Teletext initial state clock run-in window start point (lower 7 bits).
72h	**REG72**	**7:0**	**Default : 0x3C** **Access : R/W**
		7:6	Reserved.
	TT_LN_UPD_DEF	5	Teletext line default update enable.
	TT_LN_UPD_REG335	4	Teletext line 335 update enable.
	TT_LNUPD_REG318	3	Teletext line 318 update enable.
	TT_LNUPD_REG22	2	Teletext line 22 update enable.

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	TT_CRIWIN_MD	1	Teletext clock run-in window mode. 0: Teletext clock run-in start-point and end-point are using TT_INI_CRIWIN_STRPT and TT_INI_CRIWIN_ENDPT in initial state and TT_SDY_CRIWIN_STRPT and TT_SDY_CRIWIN_ENDPT in steady state. 1: Teletext clock run-in start-point and end-point are always using TT_INI_CRIWIN_STRPT and TT_INI_CRIWIN_ENDPT.	
	TT_INI_CRIWIN_STRPT	0	Teletext initial clock run-in window start point (MSB).	
73h	**REG73**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TT_LN_UPDREG06_13	7:0	Teletext line 6 to 13 (bit 7 to 0) update enable.	
74h	**REG74**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TT_LN_UPDREG14_21	7:0	Teletext line 14 to 21 (bit 7 to 0) update enable.	
75h	**REG75**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TT_LN_UPDREG319_326	7:0	Teletext line 319 to 326 (bit 7 to 0) update enable.	
76h	**REG76**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TT_LN_UPDREG327_334	7:0	Teletext line 327 to 334 (bit 7 to 0) update enable.	
77h	**REG77**	**7:0**	**Default : 0x26**	**Access : R/W**
	TT_CRI_AMP_ACC_PT	7:0	Teletext clock run-in amplitude accumulation start point.	
78h	**REG78**	**7:0**	**Default : 0x01**	**Access : R/W**
	TT_DPLL_PT	7:0	Teletext DPLL start point.	
79h	**REG79**	**7:0**	**Default : 0x7D**	**Access : R/W**
	TT_BLK_LVL_PT	7:0	Teletext blank level accumulation start point.	
7Ah	**REG7A**	**7:0**	**Default : 0xCF**	**Access : R/W**
	TT_VBI_LNEND_4_3	7:6	Teletext VBI line end (upper 2 bits). It is used to generate a notice signal to TTDEC_TOP to indicate Teletext data is received in this field.	
	TT_DPLL_EN_LEN	5:0	Teletext DPLL enable length.	
7Bh	**REG7B**	**7:0**	**Default : 0x27**	**Access : R/W**
	TT_FRAM_CODE	7:0	Teletext framing code value.	
7Ch	**REG7C**	**7:0**	**Default : 0x06**	**Access : R/W**
	TT_VBI_LNEND_2_0	7:5	Teletext VBI line end (lower 3 bits).	
	TT_DAT_LN_STR1	4:0	Teletext data line start 1 (odd field).	
7Dh	**REG7D**	**7:0**	**Default : 0x16**	**Access : R/W**

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
	TT_FC_WIN_MD	7	Teletext framing code window mode. This is valid when TT_CRIWIN_MD = 1.
	TT_FC_ERR_BOND	6	Teletext framing code error bond value. 0: Fully match framing code. 1: Allow 1 error in framing code.
	TT_SLICER_RDY_MD	5	Teletext slicer ready mode. 0: Teletext slicer is ready when TT_FCC_NT >= TT_FCC_NT_THD at TT_CHK_PT. 1: Teletext slicer is ready when TT_FCC_NT >= TT_FCC_NT_THD.
	TT_DAT_LNEND1	4:0	Teletext data line end 1 (odd field).
7Eh	**REG7E**	**7:0**	**Default : 0x85** **Access : R/W**
	TT_INIT_PKT_EN	7	Teletext initial packet counter enable. 0: Packet counter increases when Teletext packet is detected with upper-bound (TT_VBI_BUF_LEN). 1: Packet counter increases when Teletext packet is detected without upper-bound.
	-	6:5	Reserved.
	TT_DAT_LN_STR2	4:0	Teletext data line start 2 (even field).
7Fh	**REG7F**	**7:0**	**Default : 0xF6** **Access : R/W**
	TT_BASE_ADDR_SEL	7	Teletext base address source selection.
	TT_SL_PT_MD	6:5	Teletext single line point mode. [1]: 0: Start from TT_DAT_LINE_STRL. 1: Start from the line when previous line is no Teletext. [0]: 0: Disable TT_SL_PT_MD. 1: Enable TT_SL_PT_MD.
	TT_DAT_LN_END2	4:0	Teletext data line end 2 (even field).
80h	**REG80**	**7:0**	**Default : 0x54** **Access : R/W**

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
	TT_KP_SELMAN	7:5	Teletext DPLL phase error gain parameter selection. 000: 2^-9. 001: 2^-10. 010: 2^-11. 011: 2^-12. 100: 2^-13. 101: 2^-14. 110: 2^-15. 111: 2^-16.
	TT_BLK_LVL_MD	4	Teletext blank level mode. 0: Calculate blank level from TT_BLK_LVL_PT in the line set by TT_BLK_LVL_LN. 1: Calculate blank level in every line from TTBLKLVLPT.
	TT_BLK_LVL_LN	3:0	Teletext blank level line.
81h	**REG81**	**7:0**	**Default : 0x37** **Access : R/W**
	TT_CRI_AMP_THD	7:0	Teletext clock run-in amplitude threshold.
82h	**REG82**	**7:0**	**Default : 0x8E** **Access : R/W**
	TT_PH_ACC_INC_NORM1_15_8	7:0	Teletext phase accumulated incremental normalized parameter 1, used in PAL.
83h	**REG83**	**7:0**	**Default : 0x6B** **Access : R/W**
	TT_PH_ACC_INC_NORM1_7_0	7:0	Teletext phase accumulated incremental normalized parameter 1, used in PAL.
84h	**REG84**	**7:0**	**Default : 0x36** **Access : R/W**
	TT_INI_CRI_WIN_ENDPT_7_0	7:0	Teletext initial clock run-in window end point (lower 8 bits).
85h	**REG85**	**7:0**	**Default : 0x80** **Access : R/W**
	TT_INI_CRI_WIN_ENDPT_8	7	Teletext initial clock run-in window end point (MSB).
		6:4	Reserved.
	TT_TESTBUS_SEL	3:0	VBI test bus data selection.
86h	**REG86**	**7:0**	**Default : 0x8C** **Access : R/W**
	TT_MU_CRIAMP	7:6	Teletext blending parameter for clock run-in amplitude. 00: ¼. 01: 1/8. 10: 1/16. 11: 1/32.
	TT_CRI_WIN_LEN	5:0	Teletext clock run-in window length.
87h	**REG87**	**7:0**	**Default : 0x19** **Access : R/W**

VBI Register (Bank = 37)				
Index	**Mnemonic**	**Bit**	**Description**	
	TT_SLC_THD_TRKPT	7:0	Teletext slicer threshold track point. If TT_SLC_THD_ADPON = 1, slice threshold automatic tracking would be started after TT_SLC_THD_TRKPT.	
88h	**REG88**	**7:0**	**Default : 0xD5**	**Access : R/W**
	-	7:5	Reserved.	
	TT_SDY_FCMON_CNTTHD	4:0	Teletext line monitor counter threshold in steady state. TT_CHK_PT is at TT_DAT_LN_END when TT_MON_CNT = TT_SDY_FC_MON_CNT_THD.	
89h	**REG89**	**7:0**	**Default : 0xC1**	**Access : R/W**
	TT_INI_TPKTSEL	7	Teletext packet receiving mode selection. 0: Refresh when the field changes. 1: Refresh when reaching TTVBIBUFLEN.	
	TT_PH_ACC_MD	6	Teletext phase accumulation parameter mode. 0: Depend on SCM_FSC. 1: Depend on TTPHACCTYPE.	
	TT_PH_ACC_TYPE	5	0: TT_PH_ACC_INC_NORM1 1: TT_PH_ACC_INC_NORM2.	
	TT_SRCH_FCCNT_THD	4:0	Teletext framing code counter threshold in search-FC state. If TTFCCNT were not over threshold, re-training would be ignited.	
8Ah	**REG8A**	**7:0**	**Default : 0x31**	**Access : R/W**
		7	Reserved.	
	TT_CRI_AMP_HALF_HLMT_9_8	6:5	Teletext CRI half amplitude high limit (upper 2 bits).	
	TT_SDY_FCCNT_THD	4:0	Teletext framing code counter threshold in steady state. If TTFCCNT were not over threshold, re-training would be ignited.	
8Bh	**REG8B**	**7:0**	**Default : 0x04**	**Access : R/W**
		7:5	Reserved.	
	TT_SRCH_FCMON_CNTTHD	4:0	Teletext line monitor counter threshold in search-FC state. TT_CHK_PT is at TT_DAT_LN_END when TT_MON_CNT = TT_SRCH_FC_MON_CNT_THD.	
8Ch	**REG8C**	**7:0**	**Default : 0x9A**	**Access : R/W**

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	TT_MUCRI_FOUND_PT	7:6	Teletext blending parameter for clock run-in found point. 00: ½. 01: ¼. 10: 1/8. 11: 1/16.	
	-	5:4	Reserved.	
	TT_FAST_DPLL_ACQ_ON	3	Teletext fast DPLL acquisition on.	
	TT_SYMB_INTP_BASE	2:0	Teletext symbol interpolation base.	
8Dh	**REG8D**	**7:0**	**Default : 0xE5**	**Access : R/W**
	TT_SLC_THD_ADPON	7	Teletext slicer threshold adaptation on.	
	TT_SIG_DET_SEL	6	Teletext signal detection type selection. 0: TT_SLC_THD is based on TT_BLK_LVL + TT_CRI_AMP_VAL_HALF, which are average values after accumulation. TT_CRI_FOUND is base on mode0. 1: TT_SLC_THD is based on CC_DIN1_2FSC with error adjustment. TT_CRI_FOUND is based on mode1.	
	TT_MU_SLC_THD_ERR	5:4	Teletext slicer threshold error parameter selection, useful when TT_SIG_DET_SEL = 1. 00: ¼. 01: 1/8. 10: 1/16. 11: 1/32.	
	TT_SLC_THD_LAT_SEL	3:2	Teletext slicer threshold latch selection. Select delay point of CC_DIN1_2FSC for slice threshold. 00: 0. 01: 1. 10: 2. 11: 3.	
	TT_BLK_LVL_LAT_SEL	1:0	Teletext blank level latch selection. Select delay point of CCDIN1_2FSC for blank level. 00: 12. 01: 11. 10: 10. 11: 9.	
8Eh	**REG8E**	**7:0**	**Default : 0x78**	**Access : R/W**
	TT_PH_ACC_INC_NORM2_15_8	7:0	Teletext phase accumulated incremental normalized parameter 2, used in SECAM.	
8Fh	**REG8F**	**7:0**	**Default : 0x81**	**Access : R/W**

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	TT_PH_ACC_INC_NORM2_7_0	7:0	Teletext phase accumulated incremental normalized parameter 2, used in SECAM.	
90h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
91h	**REG91**	**7:0**	**Default : 0x50**	**Access : R/W**
	TTLN_CNTRFLD_THD_9_8	7:6	Teletext line counter folded threshold (upper 2 bits).	
	TT_CRI_DET_SEL	5	0: The same as TT_SIG_DET_SEL setting. 1: Inversion of TT_SIG_DET_SEL setting.	
	VPS_DAT_LN_STR	4:0	VPS data line start definition.	
92h	**REG92**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7	Reserved.	
	VPS_CRI_WIN_ENDPT_9_8	6:5	VPS clock run-in window end point (upper 2 bits).	
	VPS_DAT_LN_END	4:0	VPS data line end definition.	
93h	**REG93**	**7:0**	**Default : 0xA3**	**Access : R/W**
	VPS_CRI_WIN_STRPT	7:0	VPS clock run-in window start point.	
94h	**REG94**	**7:0**	**Default : 0x86**	**Access : R/W**
	VPS_CRI_WIN_ENDPT_7_0	7:0	VPS clock run-in window end point (lower 7 bits).	
95h	**REG95**	**7:0**	**Default : 0x36**	**Access : R/W**
	VPS_SLC_THDPT	7:0	VPS start point for slicer threshold calculation.	
96h	**REG96**	**7:0**	**Default : 0x14**	**Access : R/W**
	VPS_DPLLPT	7:0	VPS DPLL start point.	
97h	**REG97**	**7:0**	**Default : 0x0F**	**Access : R/W**
	TT_FC_WIN_ENDPT_9_8	7:6	Teletext framing code window end point (upper 2 bits).	
	VPS_DPLL_ENLEN	5:0	VPS DPLL enable length.	
98h	**REG98**	**7:0**	**Default : 0x37**	**Access : R/W**
	VPS_CRI_AMP_THD	7:0	VPS clock run-in amplitude threshold.	
99h	**REG99**	**7:0**	**Default : 0x8C**	**Access : R/W**
	VPS_PH_ACC_INC_NORM_15_8	7:0	VPS phase accumulation incremental normalized parameter.	
9Ah	**REG9A**	**7:0**	**Default : 0x01**	**Access : R/W**
	VPS_PH_ACC_INC_NORM_7_0	7:0	VPS phase accumulation incremental normalized parameter.	
9Bh ~ 9Ch	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
9Dh	**REG9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	TT_BASE_ADDR1_7_0	7:0	Teletext base address 1 (lower 8 bits).	
9Eh	**REG9E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TT_BASE_ADDR1_15_8	7:0	Teletext base address 1 (middle 8 bits).	
9Fh	**REG9F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TT_BASE_ADDR1_23_16	7:0	Teletext base address 1 (upper 8 bits).	
A0h	**REGA0**	**7:0**	**Default : 0xAF**	**Access : R/W**
	TT_FC_WIN_ENDPT_7_0	7:0	Teletext framing code window end point (lower 8 bits).	
A1h	**REGA1**	**7:0**	**Default : 0x39**	**Access : R/W**
	TTLN_CNTRFLD_THD_7_0	7:0	Teletext line counter folded threshold (lower 8 bits).	
A2h	**REGA2**	**7:0**	**Default : 0x24**	**Access : R/W**
	TT_CRIAMPHALFLLMT	7:0	Teletext CRI half amplitude low limit.	
A3h	**REGA3**	**7:0**	**Default : 0x2C**	**Access : R/W**
	TT_CRI_AMP_HALF_HLMT_7_0	7:0	Teletext CRI half amplitude high limit (lower 8 bits).	
A5h	**REGA5**	**7:0**	**Default : -**	**Access : RO**
	VPS_SC_CNT	7:4	VPS start code counter.	
	WSS_SC_CNT	3:0	WSS start code counter.	
A6h	**REGA6**	**7:0**	**Default : -**	**Access : RO**
	VPS_BYTE3	7:0	VPS byte 3, which is the received byte set by VPS_BYTE_IDX3.	
A7h	**REGA7**	**7:0**	**Default : -**	**Access : RO**
	VPS_BYTE4	7:0	VPS byte 4, which is the received byte set by VPS_BYTE_IDX4.	
A8h	**-**	**7:0**	**Default : -**	**Access : ***
	*	7:0	Reserved.	
A9h	**REGA9**	**7:0**	**Default : -**	**Access : RO**
	TT_PKT_CNT2_7_0	7:0	Teletext packet counter (lower 8 bits).	
AAh	**REGAA**	**7:0**	**Default : -**	**Access : RO**
	TT_PKT_CNT2_15_8	7:0	Teletext packet counter (upper 8 bits).	
ABh	**REGAB**	**7:0**	**Default : -**	**Access : RO**
	-	7:4	Reserved.	
	TT_FLD_CNT	3:0	Teletext field counter.	
ACh	**REGAC**	**7:0**	**Default : -**	**Access : RO**
	VPS_BIT_BIPH_ERR_CNT1	7:4	VPS bit bi-phase error counter 1 (index 1 byte).	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	VPS_BIT_BIPH_ERRCNT2	3:0	VPS bit bi-phase error counter 2 (Index 2 byte).	
ADh	**REGAD**	**7:0**	**Default : -**	**Access : RO**
	VPS_BYTE1	7:0	VPS byte 1, which is the received byte set by VPS_BYTE_IDX1.	
AEh	**REGAE**	**7:0**	**Default : -**	**Access : RO**
	VPS_BYTE2	7:0	VPS byte 2, which is the received byte set by VPS_BYTE_IDX2.	
AFh	**REGAF**	**7:0**	**Default : -**	**Access : RO**
	WSS_SC_STS	7	WSS start code status. 1 when WSS_SC_CNT >= WSS_SC_REAL_CNT_THD, set by WSS_SDY_SC_REAL_CNT_THD or WSS_PULL_SC_REAL_CNT_THD.	
	WSS_SLICER_RDY	6	WSS slicer ready indication.	
	-	5	Reserved.	
	VPS_SLICER_RDY	4	VPS slicer ready indication. 1 when VPS_SC_CNT >= VPS_SC_CNT_THD, set by VPS_SRCH_SC_CNT_THD or VPS_SDY_SC_CNT_THD, and VPS_ state is steady.	
	-	3:2	Reserved.	
	TT_SLICER_RDY2	1	Teletext slicer ready indication. 1 when TT_FC_CNT >= TT_FC_CNT_THD at TT_CHK_PT and TT_STATE is steady.	
	-	0	Reserved.	
B0h	**REGB0**	**7:0**	**Default : -**	**Access : RO**
	TT_BLK_LVL_9_2	7:0	Teletext blank level.	
B1h	**REGB1**	**7:0**	**Default : -**	**Access : RO**
	TT_SLC_THD_9_2	7:0	Teletext slicer threshold.	
B2h	**REGB2**	**7:0**	**Default : 0x8A**	**Access : R/W**
	VPS_STR_CODE_15_8	7:0	VPS start code (upper 8 bits).	
B3h	**REGB3**	**7:0**	**Default : 0x99**	**Access : R/W**
	VPS_STRCODE_7_0	7:0	VPS start code (lower 8 bits).	
B4h	**REGB4**	**7:0**	**Default : 0x45**	**Access : R/W**

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
	VPS_KPSEL_MAN	7:5	VPS DPLL gain parameter selection. 000: 2^-9. 001: 2^-10. 010: 2^-11. 011: 2^-12. 100: 2^-13. 101: 2^-14. 110: 2^-15. 111: 2^-16.
	VPS_SRCH_SC_CNT_THD	4:0	VPS search start code counter threshold. Refer to VPS_SLICER_RDY.
B5h	**REGB5**	**7:0**	**Default : 0x65** **Access : R/W**
	VPS_SYMB_INTP_BASE	7:5	VPS symbol interpolation base.
	VPS_SDY_SC_CNT_THD	4:0	VPS steady state start code counter threshold. Refer to VPS_SLICER_RDY.
B6h	**REGB6**	**7:0**	**Default : 0xB5** **Access : R/W**
	VPS_BYTE_IDX4	7:4	VPS byte index 4.
	VPS_BYTE_IDX3	3:0	VPS byte index 3.
B7h	**REGB7**	**7:0**	**Default : 0xED** **Access : R/W**
	VPS_BYTE_IDX2	7:4	VPS byte index 2.
	VPS_BYTE_IDX1	3:0	VPS byte index 1.
B8h	**REGB8**	**7:0**	**Default : 0x4F** **Access : R/W**
	VPS_SC_WIN_ENDPT_9_8	7:6	VPS start code window end point (upper 2 bits).
	VPS_INT_TYPE	5	VPS interrupt type. 0: Issue after VPS detection line if VPS slicer is ready. 1: Always issue after VPS detection line.
	WSS_INT_TYPE	4	WSS interrupt type. 0: Issue after WSS detection line if WSS slicer is ready. 1: Always issue afterWSS detection line.
	VPS_BYTENUM	3:0	VPS byte number.
B9h	**REGB9**	**7:0**	**Default : 0x7D** **Access : R/W**
	VW_BLK_LVL_PT	7:0	VPS / WSS start point for blank level calculation.
BAh	**REGBA**	**7:0**	**Default : 0x63** **Access : R/W**
	VPS_SC_WIN_ENDPT_7_0	7:0	VPS / WSS start code window end point (lower 8 bits).
BBh	**REGBB**	**7:0**	**Default : 0x0A** **Access : R/W**
	-	7:6	Reserved.

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	WSS_DATA_CHK_OP	5	WSS data check option. 0: No checking data difference. 1: Checking data difference.	
	VPS_SDY_SC_MON_CNT_THD	4:0	VPS steady state start code monitor counter threshold.	
BCh	**REGBC**	**7:0**	**Default : 0x60**	**Access : R/W**
	WSS525_SYMB_INTP_BASE	7:0	WSS symbol interpolation base for NTSC 525-line system.	
BDh	**REGBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	WSS525_PH_ACCINC	7:0	WSS phase accumulation incremental parameter for NTSC 525-line system.	
BEh	**REGBE**	**7:0**	**Default : 0x78**	**Access : R/W**
	WSS_CRI_AMPTHD_N	7:0	WSS clock run-in amplitude threshold for NTSC 525-line system.	
BFh	**REGBF**	**7:0**	**Default : 0x58**	**Access : R/W**
	NP_MD[1:0]	7:6	NTSC/PAL mode selection for debugging.	
	WSS_BIT_ID_THRSD	5:0	WSS bit identification threshold for 525-line system. 1 bit equals 32 cycles at 4*Fsc.	
C0h	**REGC0**	**7:0**	**Default : 0x57**	**Access : R/W**
	WSS_KPSELMAN	7:5	WSS DPLL gain parameter selection. 000: 2^-9. 001: 2^-10. 010: 2^-11. 011: 2^-12. 100: 2^-13. 101: 2^-14. 110: 2^-15. 111: 2^-16.	
	WSS_DATLNSTR_P	4:0	WSS data start line for PAL 625-line system.	
C1h	**REGC1**	**7:0**	**Default : 0xA3**	**Access : R/W**
	WSS_CRI_WIN_STRPT	7:0	WSS clock run-in window start point.	
C2h	**REGC2**	**7:0**	**Default : 0x9C**	**Access : R/W**
	WSS_CRI_WIN_ENDPT_7_0	7:0	WSS clock run-in window end point (lower 8 bits).	
C3h	**REGC3**	**7:0**	**Default : 0x4B**	**Access : R/W**
	WSS_CRI_WIN_ENDPT_9_8	7:6	WSS clock run-in window end point (upper 2 bits).	
	WSS_DPLL_ENLEN[5:0]	5:0	WSS DPLL enable length.	
C4h	**REGC4**	**7:0**	**Default : 0x32**	**Access : R/W**

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	WSS_SLC_THD_EN_ENDPT	7:0	WSS slicer threshold enable end point.	
C5h	**REGC5**	**7:0**	**Default : 0x78**	**Access : R/W**
	WSS_CRI_AMP_THD_P	7:0	WSS clock run-in amplitude threshold for PAL 625-line system.	
C6h	**REGC6**	**7:0**	**Default : 0xB8**	**Access : R/W**
	WSS_SC_WIN_ENDPT_7_0	7:0	WSS start code window end point (lower 8 bits).	
C7h	**REGC7**	**7:0**	**Default : 0x1E**	**Access : R/W**
	WSS_STR_CODE_23_16	7:0	WSS start code (upper 8 elements).	
C8h	**REGC8**	**7:0**	**Default : 0x3C**	**Access : R/W**
	WSS_STR_CODE_15_8	7:0	WSS start code (middle 8 elements).	
C9h	**REGC9**	**7:0**	**Default : 0x1F**	**Access : R/W**
	WSS_STR_CODE_7_0	7:0	WSS start code (lower 8 elements).	
CAh	**REGCA**	**7:0**	**Default : 0x42**	**Access : R/W**
	WSS_PULL_SC_MON_CNT_THD	7:4	WSS pull-in state start code monitor counter threshold.	
	WSS_PULL_SC_REAL_CNT_THD	3:0	WSS pull-in state start code real counter threshold.	
CBh	**REGCB**	**7:0**	**Default : 0xC8**	**Access : R/W**
	WSS_SDY_SC_MON_CNT_THD	7:4	WSS steady state start code monitor counter threshold.	
	WSS_SDY_SC_REAL_CNT_THD	3:0	WSS steady state start code real counter threshold.	
CCh	**REGCC**	**7:0**	**Default : 0xBD**	**Access : R/W**
	WSS_DAT_LNEND_P	7:3	WSS data end line for PAL 625-line system.	
	WSS_STUS_CHK_OP	2	WSS status check option. 0: Original method. 1: Depend on WSS_SC_CHKPT.	
	WSS_SC_WIN_ENDPT_9_8	1:0	WSS start code window end point (upper 2 bits).	
CDh	**REGCD**	**7:0**	**Default : -**	**Access : RO**
	WSS_WORD_7_0	7:0	WSS word (lower 8 bits).	
CEh	**REGCE**	**7:0**	**Default : -**	**Access : RO**
	WSS_WORD_15_8	7:0	WSS word (middle 8 bits).	
CFh	**REGCF**	**7:0**	**Default : -**	**Access : RO**
	-	7:4	Reserved.	
	WSS_WORD_19_16	3:0	WSS word (upper 4 bits).	

SECAM Register (Bank = 38)

SECAM Register (Bank = 38)				
Index	**Mnemonic**	**Bit**	**Description**	
01h	**REG01**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCM_RST	7	SECAM software reset. 0: Normal operation. 1: Reset.	
	MIXC_EN	6	Chroma mixing enable. 0: Disable. 1: Enable according to settings of WFUNC_ISO and YDEV_THRSD.	
	WFUNC_ISO	5	Chroma weighting function isolation. 0: Normal. 1: Isolate asymmetric weighting.	
	SCM_RES_OP	4	SCM_RESULT report option. 0: Immediate. 1: During VBI.	
	-	3	Reserved.	
	ID_MD	2	Identification mode selection. Set to 1 only if using frame ID for SECAM detection in line 7~15 and line 320~328.	
	SCMID_OP	1	SECAM identification option. 0: Identification is on when VD state is stable. 1: Ignore VD state stable condition.	
	SCMID_EN	0	SECAM identification forced enable.	
02h	**REG02**	**7:0**	**Default : 0x98**	**Access : R/W**
	SAMPLE_ST0_7_0	7:0	Start of sample point (lower 8 bits) for 4.43 MHz.	
03h	**REG03**	**7:0**	**Default : 0xA4**	**Access : R/W**
	SAMPLE_END0_7_0	7:0	End of sample point (lower 8 bits) for 4.43 MHz.	
04h	**REG04**	**7:0**	**Default : 0x1B**	**Access : R/W**
	LINE_STA	7:0	Start of line number of odd field.	
05h	**REG05**	**7:0**	**Default : 0x54**	**Access : R/W**
	LINE_STB_7_0	7:0	Start of line number of even field.	
06h	**REG06**	**7:0**	**Default : 0x01**	**Access : R/W**
	SAMPLE_ST0_10_8	7:5	Start of sample point (upper 3 bits) for 4.43MHz.	
	SAMPLE_END0_10_8	4:2	End of sample point (upper 3 bits) for 4.43MHz.	
	LINE_STB_9_8	1:0	Start of line number of even field (upper 2 bits).	
07h	**REG07**	**7:0**	**Default : 0xF0**	**Access : R/W**

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
	LINE_LEN0	7:0	Length of observation line for 4.43MHz.	
08h	**REG08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SCM_Y2Y601_BP	7	SECAM Y (Luma) to BT601 operation bypassing option.	
	MAG_MD	6:5	00: Original value. 01: MAG_INT/2. 10: MAG_INT/8. 11: MAG/32.	
	ID_CTR_MD	4:3	SECAM identification criterion mode. 00: Depend on magnitude difference. 01: Depend on magnitude and sign difference. 10: Depend on magnitude difference and sign flipping. 11: Depend on magnitude difference, sign difference, and sign flipping.	
	ID_ACT_FIELD	2:0	Active field number of SECAM identification.	
09h	**REG09**	**7:0**	**Default : 0x60**	**Access : R/W**
	MAG_THRSD44_7_0	7:0	Magnitude threshold for Fsc 4.43MHz (lower 8 bits).	
0Ah	**REG0A**	**7:0**	**Default : 0x21**	**Access : R/W**
	MAG_THRSD44_15_8	7:0	Magnitude threshold for Fsc 4.43MHz (middle 8 bits).	
0Bh	**REG0B**	**7:0**	**Default : 0x40**	**Access : R/W**
		7	Reserved.	
	LINE_PIXNUM_10_8	6:4	Pixel number of line buffer (upper 3 bits).	
	MAG_THRSD44_19_16	3:0	Magnitude threshold for Fsc 4.43MHz (upper 4 bits).	
0Ch	**REG0C**	**7:0**	**Default : 0x48**	**Access : R/W**
	LINE_PIXNUM_7_0	7:0	Pixel number of line buffer (if the number is 1097, program 11'h448).	
0Dh	**REG0D**	**7:0**	**Default : 0x06**	**Access : R/W**
	ID_THRSD	7:0	Threshold for SECAM identification.	
0Eh	**REG0E**	**7:0**	**Default : 0x88**	**Access : R/W**
	NONSCM_THRSD	7:4	Non-SECAM decision threshold.	
	SCM_THRSD	3:0	SECAM decision threshold.	
0Fh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
10h	**REG10**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAG_THRSD42_7_0	7:0	Magnitude threshold for Fsc 4.285MHz (lower 8 bits).	
11h	**REG11**	**7:0**	**Default : 0x20**	**Access : R/W**

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
	MAG_THRSD42_15_8	7:0	Magnitude threshold for Fsc 4.285MHz (middle 8 bits).	
12h	**REG12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAG_THRSD42_19_16	3:0	Magnitude threshold for Fsc 4.285MHz (upper 4 bits).	
13h	**REG13**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAG_DEV_THRSD_7_0	7:0	Magnitude deviation threshold for SECAM color-off detection (unsigned lower 8 bits).	
14h	**REG14**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAG_DEV_THRSD_15_8	7:0	Magnitude deviation threshold for SECAM color-off detection (unsigned upper 8 bits).	
15h	**REG15**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HW_SCM_COFF_EN	7	Hardware SECAM color-off enable. 0: Disable ; 1: Enable.	
	SCM_COFF_THRSD	6:0	Hardware SECAM color-off threshold (2 lines / unit).	
16h ~ 18h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
19h	**REG19**	**7:0**	**Default : 0x03**	**Access : R/W**
	SCM_BPYN	7	Bypass Y (Luma) notch filter option. 0: Normal mode. 1: Bypass mode.	
	OBV_MD	6	Observation mode. 0: Field base. 1: Within one field.	
	-	5:4	Reserved.	
	SCMGCLK_OP	3	SECAM clock gating option. 0: Gate SECAM clock when operating at 3.58MHZ(or not stable VD state). 1: No clock gating.	
	CMBGCLK_OP	2	Comb clock gating option. 0: No clock gating. 1: Gate comb filter clock when SECAM decoder is operating.	
	CLPMD[1:0]	1:0	Chroma LPF mode. 00: Bypass. 01: 1.5 MHz. 10: 1.25 MHz. 11: 1 MHz.	

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
1Ah ~ 1Dh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
1Eh	**REG1E**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCM_YSEP_FLTMD	7:6	Y separation filter selection. 00: Normal. 01: Medium. 10: Strong. 11: Reserved.	
	-	5	Reserved.	
	SCM_CBCRLPON	4	SECAM Cb/Cr LPF switch. 0: Off. 1: On.	
	LUMAFIXMD	3	Luma Fix Mode. 0: Normal. 1: Luma is controlled by SDBK level.	
	SCM_YDLYMD	2:0	SECAM Luma(Y) delay mode. 0: advance 4 ; 1: advance 3 ; 2: advance 2 ; 3: advance 1 ; 4: normal ; 5: delay 1 ; 6: delay 2 ; 7: delay 3.	
1Fh	**REG1F**	**7:0**	**Default : 0x30**	**Access : RO, R/W**
	SCM_IRQ_FORCE	7:6	SECAM Interrupt force bits.	
	SCM_IRQ_MSK	5:4	SECAM Interrupt mask bits.	
	SCM_IRQ_CLR	3:2	SECAM Interrupt clear bits.	
	SCM_IRQ_STS	1:0	SECAM Interrupt status bits.	
20h	**REG20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SCMINTTYPE	3	SECAM interrupt type. 0: Issue when SECAM ID result changes. 1: Issue when detection related data updates.	
	-	2:0	Reserved.	
21h ~ 24h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
25h	**REG25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SCM_IFMD	6:4	SECAM IF Compensation Filter Mode.	
	-	3:0	Reserved.	
26h	**REG26**	**7:0**	**Default : 0xFC**	**Access : R/W**

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description	
	SDBKLEVEL_7_0	7:0	Static de-blanking level (lower 8 bits).	
27h	**REG27**	**7:0**	**Default : 0x04**	**Access : R/W**
	SCMBLANKSTR	7:0	Start point of blank period.	
28h	**REG28**	**7:0**	**Default : 0x6C**	**Access : R/W**
	SCMBLANKEND	7:0	End point of blank period.	
29h	**REG29**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	SIGN_FLIP_THRSD_11_8	3:0	Frequency deviation sign flipping threshold for detection (upper 4 bits).	
2Ah	**REG2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SIGN_FLIP_THRSD_7_0	7:0	Frequency deviation sign flipping threshold for detection (lower 8 bits).	
2Bh	**REG2B**	**7:0**	**Default : 0x5F**	**Access : R/W**
	VDE_SCTL_11_8	7:4	Saturation bound value control after de-emphasis filter (upper 4 bits).	
	DCAL_SCTL_11_8	3:0	Saturation bound value control before de-emphasis filter (upper 4 bits).	
2Ch	**REG2C**	**7:0**	**Default : 0x3A**	**Access : R/W**
	DCAL_SCTL_7_0	7:0	Saturation bound value control before de-emphasis filter (lower 8 bits).	
2Dh	**REG2D**	**7:0**	**Default : 0x54**	**Access : R/W**
	VDE_SCTL_7_0	7:0	Saturation bound value control after de-emphasis filter (lower 8 bits).	
2Eh	**REG2E**	**7:0**	**Default : 0x06**	**Access : R/W**
	TRIG_LINE_NUM_7_0	7:0	Trigger line number for generating interrupt (lower 8 bits).	
2Fh	**REG2F**	**7:0**	**Default : 0x80**	**Access : R/W**
	SCM_CGAINMD	7	SECAM chroma gain register mode. 0: Controlled by DSP. 1: Controlled by 2Fh[6:5].	
	SCM_CGAINREG	6:5	SECAM chroma gain. 01: x2. 10: x4. Others: x1.	
	-	4:2	Reserved.	

SECAM Register (Bank = 38)				
Index	**Mnemonic**	**Bit**	**Description**	
	TRIG_LINE_NUM_9_8	1:0	Trigger line number for generating interrupt (upper 2 bits).	
30h	**REG30**	**7:0**	**Default : -**	**Access : RO**
	SCMID_DONE	7	SECAM identification done indication.	
	SCMID_YES	6	SECAM signal found bit.	
	DR_LINE	5	Dr line indication.	
	DB_LINE	4	Db line indication.	
	INTB	3	Line type indication.	
	SCMID_STS	2:0	SECAM ID status. 000: Idle. 001/010/011: ID progress. 110: SECAM. 111: No SECAM signal discovery.	
31h ~ 35h	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	
36h	**REG36**	**7:0**	**Default : -**	**Access : RO**
	-	7:5	Reserved.	
	HW_SCM_COFF	4	Hardware SECAM color-off indication.	
	-	3:2	Reserved.	
	SCM_FSC	1:0	Fsc status from AFEC_TOP. 00: NTSC 3.58MHz. 01: PAL 4.43MHz. 10: SECAM 4.285156MHz. 11: Reserved.	
38h ~ 3Bh	**-**	**7:0**	**Default : -**	**Access : -**
	-	7:0	Reserved.	

SAR Register (Bank = 3A)

SAR Register (Bank = 3A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3A00h)	**REG3A00**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_START	7	SAR start.	
	SAR_PD	6	SAR power down. 0: Enable. 1: Power down.	
	SAR_MODE	5	Select SAR ADC operation mode. 0: One-shot. 1: Freerun.	
	SINGLE	4	1: Enable SINGLE channel mode.	
	KEYPAD_LEVEL	3	Keypad level. 0: Active high. 1: Active low.	
	SAR_SINGLE_CH[2:0]	2:0	Select channel for single channel mode.	
01h (3A02h)	**REG3A02**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKSAMP_PRD[7:0]	7:0	CKSAMP_PRD.	
05h (3A0Ah)	**REG3A0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH1_LOB[5:0]	5:0	SAR channel 1 lower bound.	
06h (3A0Ch)	**REG3A0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH2_UPB[5:0]	5:0	SAR channel 2 upper bound.	
07h (3A0Eh)	**REG3A0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH2_LOB[5:0]	5:0	SAR channel 2 lower bound.	
08h (3A10h)	**REG3A10**	**7:0**	**Default : 0x00**	**Access : R/W**
		7:6	Reserved.	
	SAR_CH3_UPB[5:0]	5:0	SAR channel 3 upper bound.	
09h (3A12h)	**REG3A12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH3_LOB[5:0]	5:0	SAR channel 3 lower bound.	
0Ah (3A14h)	**REG3A14**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH4_UPB[5:0]	5:0	SAR channel 4 upper bound.	

SAR Register (Bank = 3A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (3A16h)	**REG3A16**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH4_LOB[5:0]	5:0	SAR channel 4 lower bound.	
0Ch (3A18h)	**REG3A18**	**7:0**	**Default : 0x00**	**Access : RO**
	SAR_RDY	7	SAR ready.	
	-	6	Reserved.	
	SAR_ADC_CH1_DATA[5:0]	5:0	SAR ADC channel 1 output data.	
0Dh (3A1Ah)	**REG3A1A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	SAR_ADC_CH2_DATA[5:0]	5:0	SAR ADC channel 2 output data.	
0Eh (3A1Ch)	**REG3A1C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	SAR_ADC_CH3_DATA[5:0]	5:0	SAR ADC channel 3 output data.	
0Fh (3A1Eh)	**REG3A1E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	SAR_ADC_CH4_DATA[5:0]	5:0	SAR ADC channel 4 output data.	
10h (3A20h)	**REG3A20**	**7:0**	**Default : 0xFF**	**Access : R/W**
	OEN_SAR_GPIO[3:0]	7:4	Output enable for GPIO pad. 0: Enable. 1: Disable.	
	SAR_AISEL[3:0]	3:0	Pad GPIO/Ain switch. 1: Analog input. 0: GPIO.	
10h (3A21h)	**REG3A21**	**7:0**	**Default : 0x00**	**Access : R/W**
	SAR_FREERUN	7	Set up SAR ADC for freerun. 0: Controlled by digital (default). 1: Freerun.	
	SARADC_PD	6	SAR ADC power down. 1: Power down. 0: Enable SAR ADC.	
	SAR_CHSEL[1:0]	5:4	SAR ADC channel select. 00: Channel 0. 01: Channel 1. 10: Channel 2. 11: Channel 3.	

SAR Register (Bank = 3A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	I_SAR_GPIO[3:0]	3:0	Output data for GPIO pad.	
12h (3A24h)	**REG3A24**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	C_SAR_GPIO[5:0]	5:0	Input data for GPIO pad.	
13h (3A26h)	**REG3A26**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	-	7:4	Reserved.	
	SAR_INT_STATUS	3	Status of SAR_INT.	
	SAR_INT_FORCE	2	Force interrupt for SAR_INT.	
	SAR_INT_CLR	1	Interrupt clear for SAR_INT.	
	SAR_INT_MASK	0	Interrupt mask for SAR_INT. 0: Enable. 1: Disable.	
15h (3A2Ah)	**REG3A2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH5_UPB[5:0]	5:0	SAR channel 5 upper bound.	
16h (3A2Ch)	**REG3A2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH5_LOB[5:0]	5:0	SAR channel 5 lower bound.	
17h (3A2Eh)	**REG3A2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH6_UPB[5:0]	5:0	SAR channel 6 upper bound.	
18h (3A30h)	**REG3A30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SAR_CH6_LOB[5:0]	5:0	SAR channel 6 lower bound.	
19h (3A32h)	**REG3A32**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	SAR_ADC_CH5_DATA[5:0]	5:0	SAR ADC for channel 5 data read back.	
1Ah (3A34h)	**REG3A34**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	SAR_ADC_CH6_DATA[5:0]	5:0	SAR ADC for channel 6 data read back.	
1Bh (3A36h)	**REG3A36**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:6	Reserved.	
	I_SAR_GPIO_EXT_2CH[1:0]	5:4	SAR[5:4] Output data for GPIO pad.	

SAR Register (Bank = 3A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OEN_SAR_GPIO_EXT_2CH[1:0]	3:2	SAR[5:4] Output enable for GPIO pad. 0: Enable. 1: Disable.	
	SAR_AISEL_EXT_2CH[1:0]	1:0	SAR[5:4] Pad GPIO/Ain switch. 1: Analog input. 0: GPIO.	
20h ~ 22h (3A40h ~ 3A45h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

PIU_MISC_0 Register (Bank = 3C)

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h ~ 0Fh (3C00h ~ 3C1Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h (3C20h)	**REG3C20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	CRC_DUM_10[4:0]	7:3	Bit 0 is used as DST_SEL_VDMCU.	
	DMA_BUSY	2	DMA busy.	
	DMA_DONE	1	DMA idle.	
	-	0	Reserved.	
10h (3C21h)	**REG3C21**	**7:0**	**Default : 0x00**	**Access : RO**
	DMA_STATE[7:0]	7:0	DMA status.	
20h (3C40h)	**REG3C40**	**7:0**	**Default : 0x11**	**Access : R/W**
	CSZ_SETUP[3:0]	7:4	Number of cycles between SPI_CSZ falling and first SPI_SCK.	
	CSZ_HOLD[3:0]	3:0	Number of cycles between last SPI_SCK and SPI_CSZ rising.	
20h (3C41h)	**REG3C41**	**7:0**	**Default : 0x01**	**Access : R/W**
	FAST	7	FAST mode.	
		6:4	Reserved.	
	CSZ_HIGH[3:0]	3:0	Number of cycles when SPI_CSZ = high.	
26h (3C4Ch)	**REG3C4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED0[7:0]	7:0	[5:0]: SPI clock selection. [8]: SPI new cycle.	
26h (3C4Dh)	**REG3C4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED0[15:8]	7:0	See description of '3C4Ch'.	
27h (3C4Eh)	**REG3C4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED0[23:16]	7:0	See description of '3C4Ch'.	
27h (3C4Fh)	**REG3C4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED0[31:24]	7:0	See description of '3C4Ch'.	
2Ah (3C54h)	**REG3C54**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	SPI_NEW_CYCLE	0	Force SPI to issue a new cycle.	
30h (3C60h)	**REG3C60**	**7:0**	**Default : 0xAA**	**Access : R/W**
	WDT_KEY[7:0]	7:0	enable: WDT_KEY != 0xaa55.	

PIU_MISC_0 Register (Bank = 3C)

Index (Absolute)	Mnemonic	Bit	Description	
30h (3C61h)	**REG3C61**	**7:0**	**Default : 0x55**	**Access : R/W**
	WDT_KEY[15:8]	7:0	See description of '3C60h'.	
31h (3C62h)	**REG3C62**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_SEL[7:0]	7:0	WDT interval, 65536 * (65536 - WDT_SEL) cycles.	
31h (3C63h)	**REG3C63**	**7:0**	**Default : 0xFC**	**Access : R/W**
	WDT_SEL[15:8]	7:0	See description of '3C62h'.	
32h (3C64h)	**REG3C64**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_INT_SEL[7:0]	7:0	When WDT_CNT[31:16] > WDT_INT_SEL, watchdog interrupt occurs.	
32h (3C65h)	**REG3C65**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WDT_INT_SEL[15:8]	7:0	See description of '3C64h'.	
33h (3C66h)	**REG3C66**	**7:0**	**Default : 0x00**	**Access : RO, WO**
	-	7:3	Reserved.	
	WDT_CLR_RESET_FLAG	2	Clear watchdog reset flag.	
	WDT_CLR_MCU	1	Clear watchdog.	
	WDT_RST	0	Watchdog reset occurs.	
38h (3C70h)	**REG3C70**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS0[7:0]	7:0	Power status 0.	
38h (3C71h)	**REG3C71**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS0[15:8]	7:0	See description of '3C70h'.	
39h (3C72h)	**REG3C72**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS1[7:0]	7:0	Power status 1.	
39h (3C73h)	**REG3C73**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS1[15:8]	7:0	See description of '3C72h'.	
3Ah (3C74h)	**REG3C74**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS2[7:0]	7:0	Power status 2.	
3Ah (3C75h)	**REG3C75**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS2[15:8]	7:0	See description of '3C74h'.	
3Bh (3C76h)	**REG3C76**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS3[7:0]	7:0	Power status 3.	
3Bh (3C77h)	**REG3C77**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS3[15:8]	7:0	See description of '3C76h'.	
3Ch	**REG3C78**	**7:0**	**Default : 0x00**	**Access : R/W**

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(3C78h)	POWER_STATUS4[7:0]	7:0	Power status 4.	
3Ch (3C79h)	**REG3C79**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS4[15:8]	7:0	See description of '3C78h'.	
3Dh (3C7Ah)	**REG3C7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS5[7:0]	7:0	Power status 5.	
3Dh (3C7Bh)	**REG3C7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS5[15:8]	7:0	See description of '3C7Ah'.	
3Eh (3C7Ch)	**REG3C7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS6[7:0]	7:0	Power status 6.	
3Eh (3C7Dh)	**REG3C7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS6[15:8]	7:0	See description of '3C7Ch'.	
3Fh (3C7Eh)	**REG3C7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS7[7:0]	7:0	Power status 7.	
3Fh (3C7Fh)	**REG3C7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	POWER_STATUS7[15:8]	7:0	See description of '3C7Eh'.	
40h (3C80h)	**REG3C80**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_MAX_0[7:0]	7:0	When internal counter == TIMER_MAX, interrupt occurs.	
40h (3C81h)	**REG3C81**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_MAX_0[15:8]	7:0	See description of '3C80h'.	
41h (3C82h)	**REG3C82**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_MAX_0[23:16]	7:0	See description of '3C80h'.	
41h (3C83h)	**REG3C83**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_MAX_0[31:24]	7:0	See description of '3C80h'.	
42h (3C84h)	**REG3C84**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CNT_CAP_0[7:0]	7:0	Captured counter.	
42h (3C85h)	**REG3C85**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CNT_CAP_0[15:8]	7:0	See description of '3C84h'.	
43h (3C86h)	**REG3C86**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CNT_CAP_0[23:16]	7:0	See description of '3C84h'.	
43h (3C87h)	**REG3C87**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CNT_CAP_0[31:24]	7:0	See description of '3C84h'.	
44h (3C88h)	**REG3C88**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:2	Reserved.	

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CLR_0	1	Clear internal counter.	
	CAPTURE_0	0	Capture internal counter.	
44h (3C89h)	**REG3C89**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_CTRL_0[7:0]	7:0	0: Disable. 3: Enable.	
50h (3CA0h)	**REG3CA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_MAX_1[7:0]	7:0	When internal counter == TIMER_MAX, interrupt occurs.	
50h (3CA1h)	**REG3CA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_MAX_1[15:8]	7:0	See description of '3CA0h'.	
51h (3CA2h)	**REG3CA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_MAX_1[23:16]	7:0	See description of '3CA0h'.	
51h (3CA3h)	**REG3CA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_MAX_1[31:24]	7:0	See description of '3CA0h'.	
52h (3CA4h)	**REG3CA4**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CNT_CAP_1[7:0]	7:0	Captured counter.	
52h (3CA5h)	**REG3CA5**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CNT_CAP_1[15:8]	7:0	See description of '3CA4h'.	
53h (3CA6h)	**REG3CA6**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CNT_CAP_1[23:16]	7:0	See description of '3CA4h'.	
53h (3CA7h)	**REG3CA7**	**7:0**	**Default : 0x00**	**Access : RO**
	TIMER_CNT_CAP_1[31:24]	7:0	See description of '3CA4h'.	
54h (3CA8h)	**REG3CA8**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:2	Reserved.	
	CLR_1	1	Clear internal counter.	
	CAPTURE_1	0	Capture internal counter.	
54h (3CA9h)	**REG3CA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	TIMER_CTRL_1[7:0]	7:0	0: Disable. 3: Enable.	
60h (3CC0h)	**REG3CC0**	**7:0**	**Default : 0x92**	**Access : R/W**
	ISP_ID[7:0]	7:0	ID of ISP.	
60h (3CC1h)	**REG3CC1**	**7:0**	**Default : 0x4D**	**Access : R/W**
	ISP_PWD1[7:0]	7:0	ISP password 1.	
61h	**REG3CC2**	**7:0**	**Default : 0x53**	**Access : R/W**

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(3CC2h)	ISP_PWD2[7:0]	7:0	ISP password 2.	
61h (3CC3h)	**REG3CC3**	**7:0**	**Default : 0x54**	**Access : R/W**
	ISP_PWD3[7:0]	7:0	ISP password 3.	
62h (3CC4h)	**REG3CC4**	**7:0**	**Default : 0x41**	**Access : R/W**
	ISP_PWD4[7:0]	7:0	ISP password 4.	
62h (3CC5h)	**REG3CC5**	**7:0**	**Default : 0x52**	**Access : R/W**
	ISP_PWD5[7:0]	7:0	ISP password 5.	
63h (3CC6h)	**REG3CC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	ISP_CTRL0[7:0]	7:0	ISP password 6.	
70h (3CE0h)	**REG3CE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_SRC_ADR_0[7:0]	7:0	Source address lower word.	
70h (3CE1h)	**REG3CE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_SRC_ADR_0[15:8]	7:0	See description of '3CE0h'.	
71h (3CE2h)	**REG3CE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_SRC_ADR_1[7:0]	7:0	Source address higher word.	
71h (3CE3h)	**REG3CE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_SRC_ADR_1[15:8]	7:0	See description of '3CE2h'.	
72h (3CE4h)	**REG3CE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_DST_ADR_0[7:0]	7:0	Destination address lower word, must align to 8-byte when destination is DRAM.	
72h (3CE5h)	**REG3CE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_DST_ADR_0[15:8]	7:0	See description of '3CE4h'.	
73h (3CE6h)	**REG3CE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_DST_ADR_1[7:0]	7:0	Destination address higher word, must align to 8-byte when destination is DRAM.	
73h (3CE7h)	**REG3CE7**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_DST_ADR_1[15:8]	7:0	See description of '3CE6h'.	
74h (3CE8h)	**REG3CE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_SIZE_0[7:0]	7:0	DMA size lower word, must align to 8-byte when destination is DRAM.	
74h (3CE9h)	**REG3CE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	DMA_SIZE_0[15:8]	7:0	See description of '3CE8h'.	
75h	**REG3CEA**	**7:0**	**Default : 0x00**	**Access : R/W**

PIU_MISC_0 Register (Bank = 3C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(3CEAh)	DMA_SIZE_1[7:0]	7:0	DMA size higher word, must align to 8-byte when destination is DRAM.
75h (3CEBh)	**REG3CEB**	**7:0**	**Default : 0x00** **Access : R/W**
	DMA_SIZE_1[15:8]	7:0	See description of '3CEAh'.
76h (3CECh)	**REG3CEC**	**7:0**	**Default : 0x00** **Access : R/W, WO**
	DMA_ADDR_INC	7	Set to 1 when destination is not increasing, for VDMCU.
	DMA_RIU_MODE	6	Same as DMA_DST_SEL.
	DMA_BIG_ENDIAN	5	Swap byte order in 4-byte word.
	-	4	Reserved.
	DMA_DST_SEL	3	0: DRAM. 1: DSP when CRC_DUM_10[0] is 0, VDMCU when CRC_DUM_10[0] is 1.
	-	2:1	Reserved.
	DMA_TRIG	0	DMA trigger bit, write only.
7Dh ~ 7Fh (3CFAh ~ 3CFEh)	**-**	**7:0**	**Default : -** **Access : -**
	-	-	Reserved.

IR Register (Bank = 3D)

IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3D00h)	**REG3D00**	**7:0**	**Default : 0x1F**	**Access : R/W**
	RC_FIFO_WFIRST	7	RC FIFO read/write first. 0: Read first. 1: Write first.	
	RC_FIFO_CLEAR	6	RC FIFO clear. 0: Disable. 1: Enable.	
	RC_AUTOCONFIG	5	RC5 and RC6 setting auto configuration.	
	RC6_LS_THR_L[4:0]	4:0	RC6 leading pulse threshold * 32.	
00h (3D01h)	**REG3D01**	**7:0**	**Default : 0x00**	**Access : R/W**
	RCIN_INV	7	RC input invert. 0: Disable. 1: Enable.	
	RC_DEBUG_SEL[2:0]	6:4	RC debug output select.	
	RC_WKUP_EN	3	RC wakeup enable. 0: Disable. 1: Enable.	
	RC5EXT_EN	2	Extended RC-5 enable. 0: Disable. 1: Enable.	
	RC6_EN	1	0: RC5. 1: RC6.	
	RC_EN	0	RC receiver enable. 0: Disable. 1: Enable.	
01h (3D02h)	**REG3D02**	**7:0**	**Default : 0xA0**	**Access : R/W**
	RC_LONGPULSE_THR[7:0]	7:0	RC long pulse threshold.	
01h (3D03h)	**REG3D03**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	RC_LONGPULSE_THR[12:8]	4:0	See description of '3D02h'.	
02h (3D04h)	**REG3D04**	**7:0**	**Default : 0xC0**	**Access : R/W**
	RC_LONGPULSE_MAR[7:0]	7:0	RC6 long pulse margin, only for RC6.	
02h (3D05h)	**REG3D05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	RC6_LS_THR_H[2:0]	4:2	RC6 leading pulse threshold * 1024.	
	RC_LONGPULSE_MAR[9:8]	1:0	See description of '3D04h'.	
03h (3D06h)	**REG3D06**	**7:0**	**Default : 0x41**	**Access : R/W**
	RC_INT_THR[6:0]	7:1	RC integrator threshold * 8.	
	RC6_ECO_EN	0	RC6 ECO function enable.	
03h (3D07h)	**REG3D07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RC_CLKDIV[4:0]	4:0	RC operating clock divisor ratio.	
04h (3D08h)	**REG3D08**	**7:0**	**Default : 0x3C**	**Access : R/W**
	RC_WDOG_COUNT[7:0]	7:0	RC watch dog counter (based on 1kHz for 1MHz clock input).	
04h (3D09h)	**REG3D09**	**7:0**	**Default : 0x10**	**Access : R/W**
	RC_TIMEOUT_COUNT[7:0]	7:0	RC timeout counter (based on 0.5kHz for 1MHz clock input).	
05h (3D0Ah)	**REG3D0A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	COMP_RCKEY1[7:0]	7:0	RC power wakeup key 1.	
05h (3D0Bh)	**REG3D0B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	COMP_RCKEY2[7:0]	7:0	RC power wakeup key 2.	
06h (3D0Ch)	**REG3D0C**	**7:0**	**Default : 0x00**	**Access : RO**
	RCKEY_ADDRESS[7:0]	7:0	RC decode address. RC5: {2'b0, toggle, address[4:0]}. RC6: Address[7:0].	
06h (3D0Dh)	**REG3D0D**	**7:0**	**Default : 0x00**	**Access : RO**
	RCKEY_COMMAND[7:0]	7:0	RC decode command. RC5: {repeat, 1'b0, command[5:0]}. RC5EXT: {repeat, command[6:0]}. RC6: Command[7:0].	
07h (3D0Eh)	**REG3D0E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	RCKEY_MISC[4:0]	4:0	RC6 decode miscellaneous data. [2:0]: MODE[2:0]. [3]: Toggle. [4]: Repeat.	
08h (3D10h)	**REG3D10**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	

IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description
	RC_FIFO_WPTR[2:0]	6:4	RC FIFO write pointer.
	-	3	Reserved.
	RC_FIFO_FULL	2	RC FIFO full.
	RC_TIMEOUT_FLAG	1	RC timeout flag.
	RC_FIFO_EMPTY	0	RC FIFO empty.
08h (3D11h)	**REG3D11**	**7:0**	**Default : 0x00** **Access : RO**
	-	7:3	Reserved.
	RC_FIFO_RPTR[2:0]	2:0	RC FIFO read pointer.
09h (3D12h)	**REG3D12**	**7:0**	**Default : 0x00** **Access : WO**
	-	7:1	Reserved.
	RC_FIFO_RD_PULSE	0	RC FIFO read pulse generator.
09h (3D13h)	**REG3D13**	**7:0**	**Default : 0x00** **Access : WO**
	-	7:1	Reserved.
	RC_WKUP_CLR	0	RC wakeup clear pulse generator.
40h (3D80h)	**REG3D80**	**7:0**	**Default : 0x00** **Access : R/W**
	IR_INV	7	Invert the polarity for input IR signal.
	IR_INT_MASK	6	IR Interrupt Request Mask for MCU.
	IR_RPCODE_EN	5	IR Repeat Code Check Enable.
	IR_LG01H_CHK_EN	4	IR Logic 0/1 High Level Edge Check Enable.
	IR_DCODE_PCHK_EN	3	IR Data Code Parity Check Enable.
	IR_CCODE_CHK_EN	2	IR Customer Code Check Enable.
	IR_LDCCHK_EN	1	IR Leader Code (header + off code) Check Enable.
	IR_EN	0	IR Decode Enable for Full/Raw mode.
40h (3D81h)	**REG3D81**	**7:0**	**Default : 0xC0** **Access : R/W**
	IR_INT_CRC_MASK	7	Interrupt Mask for IR CRC check.
	RAW_RPT_INT_MASK	6	Interrupt Mask for Repeat Code in RAW mode.
	-	5:4	Reserved.
	IR_NEC_WKUP_EN	3	Enable for IR wakeup function of NEC format. 0: Disable. 1: Enable.
	IR_CODE_BIT_LSB_EN	2	Enable bit for IR code bit count method. 1: IR engine counts code bit by "bit count". 0: IR engine counts code bit by "byte count".
	IR_SEPR_EN	1	IR Separator Code Check Enable (for Mitsubishi only).

IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IR_TIMEOUT_CHK_EN	0	IR Time-Out Check Enable.	
41h (3D82h)	**REG3D82**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_HDC_UPB[7:0]	7:0	The counter Upper Bound for Header Code.	
41h (3D83h)	**REG3D83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	IR_HDC_UPB[13:8]	5:0	See description of '3D82h'.	
42h (3D84h)	**REG3D84**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_HDC_LOB[7:0]	7:0	The counter Lower Bound for Header Code.	
42h (3D85h)	**REG3D85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	IR_HDC_LOB[13:8]	5:0	See description of '3D84h'.	
43h (3D86h)	**REG3D86**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_OFC_UPB[7:0]	7:0	The counter Upper Bound for Off Code.	
43h (3D87h)	**REG3D87**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IR_OFC_UPB[12:8]	4:0	See description of '3D86h'.	
44h (3D88h)	**REG3D88**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_OFC_LOB[7:0]	7:0	The counter Lower Bound for Off Code.	
44h (3D89h)	**REG3D89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IR_OFC_LOB[12:8]	4:0	See description of '3D88h'.	
45h (3D8Ah)	**REG3D8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_OFC_RP_UPB[7:0]	7:0	The counter Upper Bound for Repeat Off Code.	
45h (3D8Bh)	**REG3D8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IR_OFC_RP_UPB[11:8]	3:0	See description of '3D8Ah'.	
46h (3D8Ch)	**REG3D8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_OFC_RP_LOB[7:0]	7:0	The counter Lower Bound for Repeat Off Code.	
46h (3D8Dh)	**REG3D8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IR_OFC_RP_LOB[11:8]	3:0	See description of '3D8Ch'.	
47h (3D8Eh)	**REG3D8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_LG01H_UPB[7:0]	7:0	The counter Upper Bound for Logic 0/1 High level width.	

IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
47h (3D8Fh)	**REG3D8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IR_LG01H_UPB[9:8]	1:0	See description of '3D8Eh'.	
48h (3D90h)	**REG3D90**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_LG01H_LOB[7:0]	7:0	The counter Lower Bound for Logic 0/1 High level width.	
48h (3D91h)	**REG3D91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IR_LG01H_LOB[9:8]	1:0	See description of '3D90h'.	
49h (3D92h)	**REG3D92**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_LG0_UPB[7:0]	7:0	The counter Upper Bound for Logic 0 width.	
49h (3D93h)	**REG3D93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IR_LG0_UPB[10:8]	2:0	See description of '3D92h'.	
4Ah (3D94h)	**REG3D94**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_LG0_LOB[7:0]	7:0	The counter Lower Bound for Logic 0 width.	
4Ah (3D95h)	**REG3D95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IR_LG0_LOB[10:8]	2:0	See description of '3D94h'.	
4Bh (3D96h)	**REG3D96**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_LG1_UPB[7:0]	7:0	The counter Upper Bound for Logic 1 width.	
4Bh (3D97h)	**REG3D97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IR_LG1_UPB[11:8]	3:0	See description of '3D96h'.	
4Ch (3D98h)	**REG3D98**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_LG1_LOB[7:0]	7:0	The counter Lower Bound for Logic 1 width.	
4Ch (3D99h)	**REG3D99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IR_LG1_LOB[11:8]	3:0	See description of '3D98h'.	
4Dh (3D9Ah)	**REG3D9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_SEPR_UPB[7:0]	7:0	The counter Upper Bound for Separator Code width.	
4Dh (3D9Bh)	**REG3D9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IR_SEPR_UPB[11:8]	3:0	See description of '3D9Ah'.	

IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
4Eh (3D9Ch)	**REG3D9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_SEPR_LOB[7:0]	7:0	The counter Lower Bound for Separator Code width.	
4Eh (3D9Dh)	**REG3D9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IR_SEPR_LOB[11:8]	3:0	See description of '3D9Ch'.	
4Fh (3D9Eh)	**REG3D9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_TIMEOUT_CYC[7:0]	7:0	The counter value for IR Timeout Cycles. Timeout check will start when: 1: IR_TIMEOUT_CHK_EN = 1. 2: Counter value > IR_TIMEOUT_CYC.	
4Fh (3D9Fh)	**REG3D9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_TIMEOUT_CYC[15:8]	7:0	See description of '3D9Eh'.	
50h (3DA0h)	**REG3DA0**	**7:0**	**Default : 0x30**	**Access : R/W**
	IR_TIMEOUT_CLR_SW	7	IR Timeout Clear by Software. 1: Enable. 0: Disable.	
	IR_TIMEOUT_CLR_SET[2:0]	6:4	IR Timeout Clear Set. 000: Clear timeout at HDC check pass. 001: Clear timeout at OFC check pass & Decode 0 state. 010: Clear timeout at Customer Code check pass. 011: Clear timeout at Key Data Code check pass. 100: S/W clear, need also to set "TIMEOUT_CLR_SW=1". It is recommended to set 011 for NEC-like format.	
	-	3	Reserved.	
	IR_TIMEOUT_CYC[18:16]	2:0	See description of '3D9Eh'.	
50h (3DA1h)	**REG3DA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_CODE_BIT_LSB[2:0]	7:5	IR Code Bit LSB setting. If IR_CODE_BIT_LSB_EN==1 (3D81h[2]) is set, then we can set these 3 bits to specify the number of code bits. For example, if IR code bits = 36, then the register may be set as follows: 1: Set IR_CODE_BIT_LSB_EN = 1 (3D811h[2]). 2: Set IR_CODE_BYTE = 4'b0100 (3DA1h[3:0]). 3: Set IR_CODE_BIT_LSB = 3'b100 (3DA1h[7:5]).	
	IR_CCODE_BYTE	4	IR Customer Code Byte setting (full mode use only). 0: 1-byte customer code. 1: 2-byte customer code (default for NEC format).	

IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
	IR_CODE_BYTE[3:0]	3:0	IR Code Byte setting (Customer Code + Data Code + …, for full mode and raw mode use). 1: 1 byte. 2: 2 bytes. ... f: 15 bytes. It is recommended to set 4'b0100 for NEC format.	
51h (3DA2h)	**REG3DA2**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	RPT_FLAG_CLR_RAW	7	Interrupt Flag Clear for "IR repeat code flag in RAW mode". 1: Clear interrupt flag. 0: Not clear interrupt flag.	
	-	6	Reserved.	
	IR_SEPR_BIT[5:0]	5:0	IR Separator Bits setting (only used for Mitsubishi format in full mode). The code data bit decoding after this bit will go into separator state when IR_SEPR_EN = 1 (3D81h[1]).	
51h (3DA3h)	**REG3DA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	IR_SHOT_SEL[1:0]	5:4	The pshot/nshot selection for internal counter (only used in S/W mode). 01: Only pshot edge detect for counter. 10: Only nshot edge detect for counter. 00/11: Both pshot and nshot edge detect for counter.	
	IR_FIFO_FULL_EN	3	IR FIFO Full Enable (used in Full/Raw mode). 0: Disable FIFO Full (data can be written over when FIFO is full). 1: Enable FIFO Full (data will be discarded when FIFO is full).	
	IR_FIFO_DEPTH[2:0]	2:0	FIFO Depth (for decoded IR code data or IR raw data, not for S/W mode counter data).	
52h (3DA4h)	**REG3DA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_CCODE[7:0]	7:0	IR Customer Code.	
52h (3DA5h)	**REG3DA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_CCODE[15:8]	7:0	See description of '3DA4h'.	
53h (3DA6h)	**REG3DA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_GLHRM_NUM[7:0]	7:0	Glitch Removal Number for crystal based counter. The glitches will be removed whenever their cycle width is	

IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description	
			below the GLHRM_NUM cycle.	
53h (3DA7h)	**REG3DA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	IR_DECOMODE[1:0]	5:4	IR Decode Mode selection. 00/11: Full decode mode (NEC and NEC-like format). 01: S/W mode (shot mode, output edge count value). 10: Raw mode (header decode only, output raw data).	
	IR_GLHRM_EN	3	Glitch Removal Enable.	
	IR_GLHRM_NUM[10:8]	2:0	See description of '3DA6h'.	
54h (3DA8h)	**REG3DA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	IR_CKDIV_NUM[7:0]	7:0	Divided Number for input crystal clock. The divided clock is for internal counter use. 8'h00: Divided by 1. 8'h01: Divided by 2. ... 8'hFF: Divided by 256. Default: 8'h0E for Xtal clock = 14.318 MHz, 8'hFF for Xtal clock = 25.00 MHz.	
54h (3DA9h)	**REG3DA9**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_KEY_DATA[7:0]	7:0	IR Key Data Output (for Full/Raw mode data). After reading IR_KEY_DATA (3DA9h), you must set IR_FIFO_RD_PULSE = 1 (3DB0h[0]) for internal FIFO read pointer to go to the next one.	
55h (3DAAh)	**REG3DAA**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_SHOT_CNT[7:0]	7:0	IR shot count value output in S/W mode, the type of shot is selected from IR_SHOT_SEL (3DA3h[5:4]).	
55h (3DABh)	**REG3DAB**	**7:0**	**Default : 0x00**	**Access : RO**
	IR_SHOT_CNT[15:8]	7:0	See description of '3DAAh'.	
56h (3DACh)	**REG3DAC**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IR_SHOT_P	4	IR shot type (pshot/nshot) in S/W mode. 0: Nshot occurs. 1: Pshot occurs.	
	-	3	Reserved.	
	IR_SHOT_CNT[18:16]	2:0	See description of '3DAAh'.	
56h	**REG3DAD**	**7:0**	**Default : 0x00**	**Access : RO**

IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description
(3DADh)	IR_RC_WKUP_FLAG	7	IR RC wakeup function flag.
	IR_NEC_WKUP_FLAG	6	IR NEC wakeup function flag.
	IR_INT_CRC_FLAG	5	IR CRC function interrupt flag.
	IR_INT_FLAG	4	IR normal function interrupt flag.
	IR_FIFO_FULL	3	IR FIFO Full Flag. 1: FIFO is full. 0: FIFO is not full yet.
	IR_TIMEOUT_FLAG	2	IR timeout flag. 1: Timeout occurs. 0: Not timeout yet.
	IR_FIFO_EMPTY	1	IR FIFO empty flag for Full/Raw mode.
	IR_RPT_FLAG	0	IR FIFO data repeat flag for Full mode.
57h (3DAEh)	**REG3DAE**	**7:0**	**Default : 0x00** **Access : R/W**
	IR_CRC_GOLDEN[7:0]	7:0	IR CRC golden value, calculated before power down. (CRC check IR register range: 0x3D40 ~ 0x3D53).
57h (3DAFh)	**REG3DAF**	**7:0**	**Default : 0x00** **Access : R/W**
	IR_CRC_GOLDEN[15:8]	7:0	See description of '3DAEh'.
58h (3DB0h)	**REG3DB0**	**7:0**	**Default : 0x00** **Access : WO**
	-	7:4	Reserved.
	IR_NEC_WKUP_FLAG_CLR	3	IR wakeup flag clear for NEC format. 1: Clear pulse generation. 0: No operation.
	IR_FLAG_CLR	2	IR interrupt flag clear. 1: Clear pulse generation. 0: No operation.
	IR_CRC_FLAG_CLR	1	IR CRC interrupt flag clear. 1: Clear pulse generation. 0: No operation.
	IR_FIFO_RD_PULSE	0	IR FIFO Read Pulse. 1: Read. 0: Not read. Note: Need to set this bit to 1 after S/W read "IR_KEY_DATA" (3DA9h) to allow FIFO read pointer to go to the next one.
59h (3DB2h)	**REG3DB2**	**7:0**	**Default : 0xFF** **Access : R/W**
	IR_NEC_COMP_KEY1[7:0]	7:0	IR compare key 1 for wakeup function of NEC format.

IR Register (Bank = 3D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
59h (3DB3h)	**REG3DB3**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IR_NEC_COMP_KEY2[7:0]	7:0	IR compare key 2 for wakeup function of NEC format.	

DDC Register (Bank = 3E)

DDC Register (Bank = 3E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (3E00h)	**REG3E00**	**7:0**	**Default : 0x00**	**Access : RO**
	D2B_WBUF_RPORT_A0[7:0]	7:0	DDC2Bi master write buffer, MCU read point of A0.	
00h (3E01h)	**REG3E01**	**7:0**	**Default : 0x00**	**Access : R/W**
	D2B_RBUF_WPORT_A0[7:0]	7:0	DDC2Bi master read buffer, MCU write point of A0.	
02h (3E04h)	**REG3E04**	**7:0**	**Default : 0x00**	**Access : RO**
	D2B_WBUF_RPORT_D0[7:0]	7:0	DDC2Bi master write buffer, MCU read point of D0.	
02h (3E05h)	**REG3E05**	**7:0**	**Default : 0x00**	**Access : R/W**
	D2B_RBUF_WPORT_D0[7:0]	7:0	DDC2Bi master read buffer, MCU write point of D0.	
03h (3E06h)	**REG3E06**	**7:0**	**Default : 0x00**	**Access : RO**
	D2B_WBUF_RPORT_D1[7:0]	7:0	DDC2Bi master write buffer, MCU read point of D1.	
03h (3E07h)	**REG3E07**	**7:0**	**Default : 0x00**	**Access : R/W**
	D2B_RBUF_WPORT_D1[7:0]	7:0	DDC2Bi master read buffer, MCU write point of D1.	
04h (3E08h)	**REG3E08**	**7:0**	**Default : 0x00**	**Access : WO**
	D2B_RBUF_WPORT_PULSE_A0	7	MCU write pulse generate for D2B RBUF_A0.	
	-	6	Reserved.	
	D2B_RBUF_WPORT_PULSE_D0	5	MCU write pulse generate for D2B RBUF_D0.	
	D2B_RBUF_WPORT_PULSE_D1	4	MCU write pulse generate for D2B RBUF_D1.	
	-	3:0	Reserved.	
04h (3E09h)	**REG3E09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	EN_NO_ACK	1	DDC2Bi will not send Ack if data buffer has not been read by CPU. 0: Disable. 1: Enable.	
	-	0	Reserved.	
05h (3E0Ah)	**REG3E0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	D2B_ID_A0[7:0]	7:0	[7] DDC2Bi Enable for A0. [6:0] DDCBi ID[7:1] for A0.	
06h (3E0Ch)	**REG3E0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	D2B_ID_D0[7:0]	7:0	[7] DDC2Bi Enable for D0. [6:0] DDCBi ID[7:1] for D0.	
06h	**REG3E0D**	**7:0**	**Default : 0x00**	**Access : R/W**

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description	
(3E0Dh)	D2B_ID_D1[7:0]	7:0	[15] DDC2Bi Enable for D1. [14:8] DDCBi ID[7:1] for D1.	
07h (3E0Eh)	**REG3E0E**	**7:0**	**Default : 0x00**	**Access : RO**
	C_LAT_SRAM_DATA_A0[7:0]	7:0	DDC Data Read Port for ADC SRAM. CPU reads ADC SRAM data.	
07h (3E0Fh)	**REG3E0F**	**7:0**	**Default : 0x00**	**Access : RO**
	C_LAT_SRAM_DATA_D0[7:0]	7:0	DDC Data Read Port for DVI SRAM. CPU reads DVI SRAM data.	
08h (3E10h)	**REG3E10**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	D2B_INT_FINAL_STATUS_A0[6:0]	6:0	[6] DDC2Bi Start interrupt flag. [5] DDC2Bi Stop interrupt flag. [4] DDC2Bi Data Read interrupt flag. Write data into rbuf to clear. [3] DDC2Bi Data Write interrupt flag. Read data from wbuf to clear. [2] The 8th bit of the ID, interrupt flag. 0: Write. 1: Read (RO, updated automatically). [1] WADR interrupt flag. 1: The data in wbuf is the 2nd byte (WADR). 0: The data in wbuf is not the 2nd byte (not WADR). [0] DDC2Bi ID interrupt flag.	
09h (3E12h)	**REG3E12**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	D2B_INT_FINAL_STATUS_D0[6:0]	6:0	[6] DDC2Bi Start interrupt flag. [5] DDC2Bi Stop interrupt flag. [4] DDC2Bi Data Read interrupt flag. Write data into rbuf to clear. [3] DDC2Bi Data Write interrupt flag. Read data from wbuf to clear. [2] The 8th bit of the ID, interrupt flag. 0: Write. 1: Read (RO, updated automatically). [1] WADR interrupt flag. 1: The data in wbuf is the 2nd byte (WADR). 0: The data in wbuf is not the 2nd byte (not WADR). [0] DDC2Bi ID interrupt flag.	

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description	
09h (3E13h)	**REG3E13**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	D2B_INT_FINAL_STATUS_D1[6:0]	6:0	[14] DDC2Bi Start interrupt flag. [13] DDC2Bi Stop interrupt flag. [12] DDC2Bi Data Read interrupt flag. Write data into rbuf to clear. [11] DDC2Bi Data Write interrupt flag. Read data from wbuf to clear. [10] The 8th bit of the ID, interrupt flag. 0: Write. 1: Read (RO, updated automatically). [9] WADR interrupt flag. 1: The data in wbuf is the 2nd byte (WADR). 0: The data in wbuf is not the 2nd byte (not WADR). [8] DDC2Bi ID interrupt flag.	
0Ah (3E14h)	**REG3E14**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7	Reserved.	
	D2B_INT_MASK_A0[6:0]	6:0	[6] DDC2Bi Start interrupt mask. [5] DDC2Bi Stop interrupt mask. [4] DDC2Bi Data Read interrupt mask. Write data into rbuf to clear. [3] DDC2Bi Data Write interrupt mask. Read data from wbuf to clear. [2] The 8th bit of the ID, interrupt mask. 0: Write. 1: Read (RO, updated automatically). [1] WADR interrupt mask. 1: The data in wbuf is the 2nd byte (WADR). 0: The data in wbuf is not the 2nd byte (not WADR). [0] DDC2Bi ID interrupt flag.	
0Bh (3E16h)	**REG3E16**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7	Reserved.	
	D2B_INT_MASK_D0[6:0]	6:0	[6] DDC2Bi Start interrupt flag. [5] DDC2Bi Stop interrupt flag. [4] DDC2Bi Data Read interrupt flag. Write data into rbuf to clear. [3] DDC2Bi Data Write interrupt flag. Read data from wbuf to clear.	

DDC Register (Bank = 3E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			[2] The 8th bit of the ID, interrupt mask. 0: Write. 1: Read (RO, updated automatically). [1] WADR interrupt mask. 1: The data in wbuf is the 2nd byte (WADR). 0: The data in wbuf is not the 2nd byte (not WADR). [0] DDC2Bi ID interrupt flag.
0Bh (3E17h)	**REG3E17**	**7:0**	**Default : 0x06** **Access : R/W**
	-	7	Reserved.
	D2B_INT_MASK_D1[6:0]	6:0	[14] DDC2Bi Start interrupt flag. [13] DDC2Bi Stop interrupt flag. [12] DDC2Bi Data Read interrupt flag. Write data into rbuf to clear. [11] DDC2Bi Data Write interrupt flag. Read data from wbuf to clear. [10] The 8th bit of the ID, interrupt mask. 0: Write. 1: Read (RO, updated automatically). [9] WADR interrupt mask. 1: The data in wbuf is the 2nd byte (WADR). 0: The data in wbuf is not the 2nd byte (not WADR). [8] DDC2Bi ID interrupt flag.
0Ch (3E18h)	**REG3E18**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7	Reserved.
	D2B_INT_FORCE_A0[6:0]	6:0	Force D2B_INT_FINAL_STATUS_A0 to 1 by setting each of the related bits to 1.
0Dh (3E1Ah)	**REG3E1A**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7	Reserved.
	D2B_INT_FORCE_D0[6:0]	6:0	Force D2B_INT_FINAL_STATUS_D0 to 1 by setting each of the related bits to 1.
0Dh (3E1Bh)	**REG3E1B**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7	Reserved.
	D2B_INT_FORCE_D1[6:0]	6:0	Force D2B_INT_FINAL_STATUS_D1 to 1 by setting each of the related bits to 1.
0Eh (3E1Ch)	**REG3E1C**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7	Reserved.
	D2B_INT_CLR_A0[6:0]	6:0	Clear D2B_INT_FINAL_STATUS_A0 to 0 by setting each of

DDC Register (Bank = 3E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			the related bits to 1.	
0Fh (3E1Eh)	**REG3E1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	D2B_INT_CLR_D0[6:0]	6:0	Clear D2B_INT_FINAL_STATUS_D0 to 0 by setting each of the related bits to 1.	
0Fh (3E1Fh)	**REG3E1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	D2B_INT_CLR_D1[6:0]	6:0	Clear D2B_INT_FINAL_STATUS_D1 to 0 by setting each of the related bits to 1.	
21h (3E42h)	**REG3E42**	**7:0**	**Default : 0x00**	**Access : WO**
	D0_CLR_DIRTY	7	Clear dirty bit for DVI_0 (clear pulse generate). 0: Not clear. 1: Clear.	
	A0_CLR_DIRTY	6	Clear dirty bit for ADC_0 (clear pulse generate). 0: Not clear. 1: Clear.	
	D1_CLR_DIRTY	5	Clear dirty bit for DVI_1 (clear pulse generate). 0: Not clear. 1: Clear.	
	-	4:0	Reserved.	
21h (3E43h)	**REG3E43**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	EN_WDATA_CLK_D0	7	DVI SRAM write data pulse gen when CPU is in write operation. 0: Not gen pulse. 1: Gen pulse.	
	CPURRQ_ST_0_D0	6	DVI SRAM read pulse gen when CPU is in read operation. 0: Not gen pulse. 1: Gen pulse.	
	EN_WDATA_CLK_A0	5	ADC SRAM write data pulse gen when CPU is in write operation. 0: Not gen pulse. 1: Gen pulse.	
	CPURRQ_ST_0_A0	4	ADC SRAM read pulse gen when CPU is in read operation. 0: Not gen pulse. 1: Gen pulse.	
	-	3:2	Reserved.	

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description
	D0_EN_READ	1	DDC SRAM Read/Write Enable for DVI SRAM. 0: Write. 1: Read.
	-	0	Reserved.
22h (3E44h)	**REG3E44**	**7:0**	**Default : 0x00** **Access : RO, R/W, WO**
	CHK_SUM_OK	7	DDC Check Sum (256 bytes) (RO). 0: Not OK. 1: OK.
	CHK1ST_SUM_OK	6	DDC Check Sum 1 (128 bytes) (RO). 0: Not OK. 1: OK.
	MASTER_FINISH	5	DDC Master Function Finish (RO). 0: Not finish. 1: Finish.
	MASTER_OK	4	Master OK (write 128 bytes with acknowledgement received) (RO). 0: Not OK. 1: OK.
	F128_DVI	3	Send first 128 bytes to DVI (second 128 bytes to ADC). 0: DVI. 1: ADC.
	SEL_256	2	Master moves from EEPROM. 0: 128 bytes. 1: 256 bytes.
	MASTER_ENABLE	1	Master Disable/Enable. 0: Disable. 1: Enable.
	MASTER_START	0	Soft Master Stop/Start Trigger. 0: Stop. 1: Start.
22h (3E45h)	**REG3E45**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	D0_DDC_EN	7	DDC Function Enable for DVI_0. 0: Disable. 1: Enable.
	FILTER_ON	6	DDC Filter. 0: Enable. 1: Disable.

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description
	D0_DDCW_PROTECT	5	DDC I2C bus Write Protect for DVI_0 port. 0: Not protect. 1: Protect.
	BYPASS_DDC	4	Bypass DDC. 0: Disable. 1: Enable.
	BYPASS_SEL_DVI	3	Bypass Select DVI. 0: ADC. 1: DVI.
	D0_DDC_BUSY	2	DDC Busy for DVI_0 (RO). 0: Not busy. 1: Busy.
	D0_LAST_RW	1	DDC last Read/Write status for DVI_0 (RO). 0: Write. 1: Read.
	D0_DIRTY_BIT	0	DDC SRAM Dirty status for DVI_0 (RO). 0: Not dirty. 1: Dirty.
23h (3E46h)	**REG3E46**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	FILTER_MSB	7	DDC Filter MSB.
	D0_LAST_ADR[6:0]	6:0	DDC Last R/W address for DVI_0.
23h (3E47h)	**REG3E47**	**7:0**	**Default : 0x00** **Access : R/W**
	D0_CPU_ADR[7:0]	7:0	DDC Address Port for CPU read/write for DVI_0.
24h (3E48h)	**REG3E48**	**7:0**	**Default : 0x00** **Access : R/W**
	D0_CPU_WDATA[7:0]	7:0	DDC Data Port for CPU write for DVI_0.
24h (3E49h)	**REG3E49**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	A0_DDC_EN	7	DDC Function Enable for ADC_0. 0: Disable. 1: Enable.
	-	6	Reserved.
	A0_DDCW_PROTECT	5	DDC I2C bus Write Protect for ADC_0 port. 0: Not protect. 1: Protect.
	SLEW_SEL[1:0]	4:3	Slew Rate Control. 00: Bypass. 01: Drive 1 cycle.

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description
			10: Drive 2 cycles. 11: Drive 3 cycles.
	A0_DDC_BUSY	2	DDC Busy for ADC_0 (RO). 0: Not busy. 1: Busy.
	A0_LAST_RW	1	DDC last Read/Write status for ADC_0 (RO). 0: Write. 1: Read.
	A0_DIRTY_BIT	0	DDC SRAM Dirty status for ADC_0 (RO). 0: Not dirty. 1: Dirty.
25h (3E4Ah)	**REG3E4A**	**7:0**	**Default : 0x80** **Access : RO, R/W**
	-	7	Reserved.
	A0_LAST_ADR[6:0]	6:0	DDC Last R/W address for ADC_0 (RO).
25h (3E4Bh)	**REG3E4B**	**7:0**	**Default : 0x00** **Access : R/W**
	A0_EN_READ	7	DDC SRAM Read/Write Enable for ADC SRAM. 0: Write. 1: Read.
	A0_CPU_ADR[6:0]	6:0	DDC address port for CPU read/write for ADC_0.
26h (3E4Ch)	**REG3E4C**	**7:0**	**Default : 0x00** **Access : R/W**
	A0_CPU_WDATA[7:0]	7:0	DDC Data Port for CPU write for ADC_0.
26h (3E4Dh)	**REG3E4D**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	D1_DDC_EN	7	DDC Function Enable for DVI_1. 0: Disable. 1: Enable.
	-	6	Reserved.
	D1_DDCW_PROTECT	5	DDC I2C bus Write Protect for DVI_1 port. 0: Not protect. 1: Protect.
	-	4:3	Reserved.
	D1_DDC_BUSY	2	DDC Busy status for DVI_1 (RO). 0: Not busy. 1: Busy.
	D1_LAST_RW	1	DDC last Read/Write status for DVI_1 (RO). 0: Write. 1: Read.

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description	
	D1_DIRTY_BIT	0	DDC SRAM Dirty status for DVI_1 (RO). 0: Not dirty. 1: Dirty.	
27h (3E4Eh)	**REG3E4E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	D1_LAST_ADR[6:0]	6:0	DDC Last R/W address for DVI_1 (RO).	
30h (3E60h)	**REG3E60**	**7:0**	**Default : 0x80**	**Access : R/W**
	HDMI_256_EN	7	HDMI SRAM 256 enable (allow DVI SRAM256x8 instead of SRAM128x8).	
	BYPASS_SEL_0	6	DDC bypass source port selection. If BYP_SEL_DVI=1, 0: Choose D1. 1: Choose D0.	
	-	5:0	Reserved.	
3Ah (3E74h)	**REG3E74**	**7:0**	**Default : 0x22**	**Access : RO, R/W**
	-	7:6	Reserved.	
	HDCP_EN	5	HDCP Enable for DDC. 0: Not enable. 1: Enable.	
	-	4:3	Reserved.	
	HDCP_MA_FINISH	2	HDCP master finish (RO).	
	ENWRITE_HDCP	1	Enable CPU write (for HDCP SRAM/74reg). 0: Not enable. 1: Enable.	
	HDCP_SRAM_ACCESS	0	HDCP SRAM access enable (1 for CPU; 0 for 74reg access). 0: Access HDCP 74reg. 1: Access HDCP SRAM.	
3Bh (3E76h)	**REG3E76**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_ADR_REG[7:0]	7:0	CPU R/W address (for HDCP_KEY_SRAM/74reg).	
3Bh (3E77h)	**REG3E77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CPU_ADR_REG[9:8]	1:0	See description of '3E76h'.	
3Ch (3E78h)	**REG3E78**	**7:0**	**Default : 0x00**	**Access : R/W**
	CPU_WDATA_REG[7:0]	7:0	CPU write data port (for HDCP_KEY_SRAM/74reg).	
3Ch	**REG3E79**	**7:0**	**Default : 0x00**	**Access : RO**

DDC Register (Bank = 3E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(3E79h)	HDCP_DATA_PORT_RD[7:0]	7:0	HDCP read data port (for HDCP_KEY_SRAM/74reg).	
3Dh (3E7Ah)	**REG3E7A**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:3	Reserved.	
	LOAD_ADR_P	2	HDCP address load pulse generate. 0: Not gen pulse. 1: Gen pulse.	
	HDCP_DATA_WR_P	1	HDCP data write port pulse generate. 0: Not gen pulse. 1: Gen pulse.	
	HDCP_DATA_RD_P	0	HDCP data read port pulse generate. 0: Not gen pulse. 1: Gen pulse.	
3Eh (3E7Ch)	**REG3E7C**	**7:0**	**Default : 0x80**	**Access : R/W**
	RSTZ_SW_DDC	7	Software resetz for DDC (active low).	
	-	6:0	Reserved.	

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
12/05/08		• Created first version.

This page is intended to be left blank.