项目名称：P60-X9 V6.0	开案日期：2012.8.14
开案规格：	
全功能版本： 名称	料号
规格	
公板版本： 名称	料号
规格	

版本更新记录

版本	更新记录	修订	审核	日期
P60-X9 V6.1 20130117				

Power Config:

Date	Modify Number	Modify By

深圳市鼎科实业有限公司

SheetName: 01.Page Cover

Size	Document Number	Rev
A3	P82-69ZR V6.0	A

Modify Date: Monday, May 04, 2015 | Designed By: chuizi | Sheet 1 of 10

GPIO CONFIG

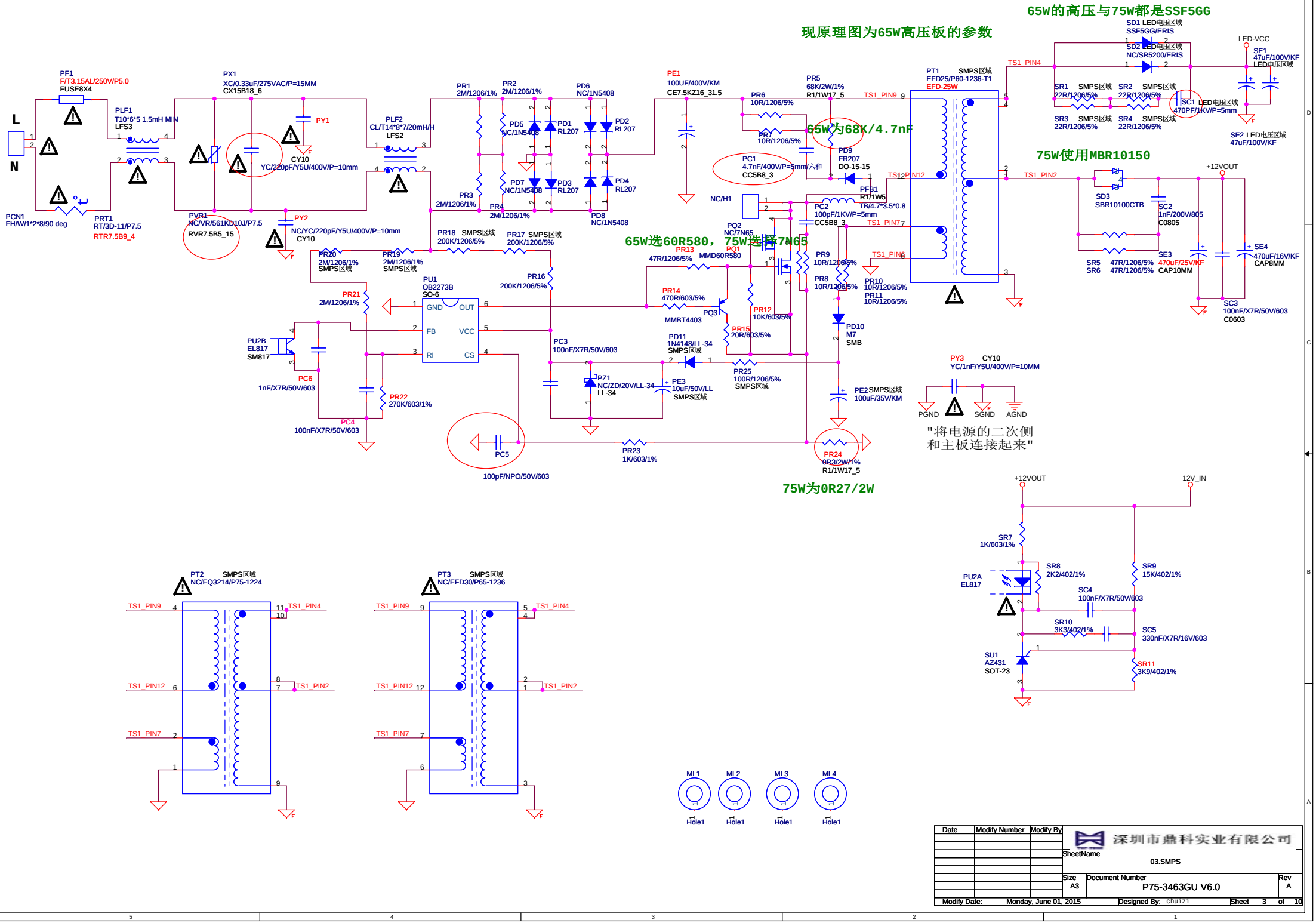
Date	Modify Number	Modify By

深圳市鼎科实业有限公司

SheetName: 02.GPIO CONFIG

Size: A3 | Document Number: P82-69ZR V6.0 | Rev: A

Modify Date: Monday, May 04, 2015 | Designed By: chuizi | Sheet 2 of 10



Date	Modify Number	Modify By

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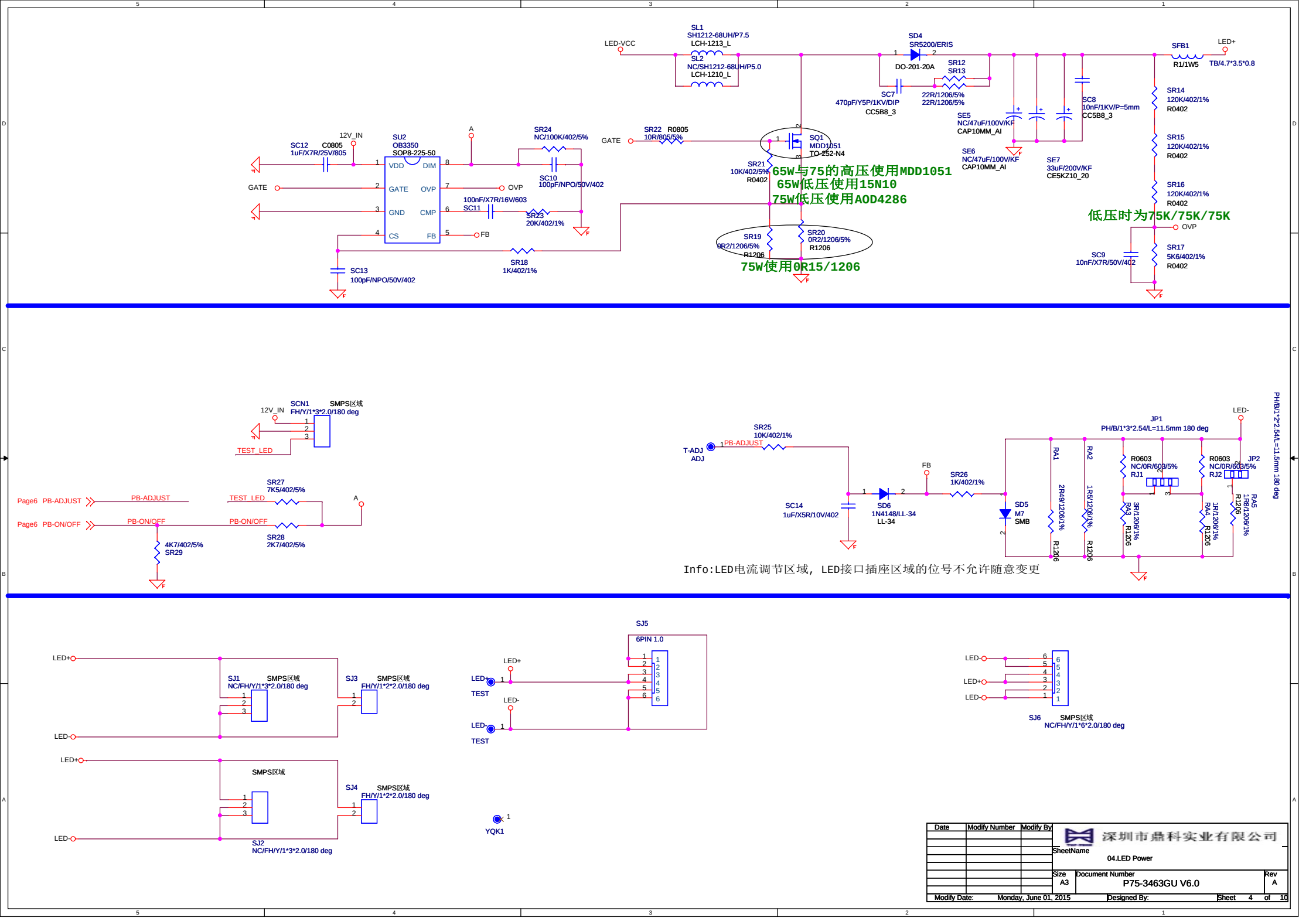
SheetName: 03.SMPS

Size	Document Number	Rev
A3	P75-3463GU V6.0	A

Modify Date: Monday, June 01, 2015 | Designed By: chuizi | Sheet 3 of 10



Date	Modify Number	Modify By

深圳市鼎科实业有限公司

SheetName: 04.LED Power

Size	Document Number	Rev
A3	P75-3463GU V6.0	A

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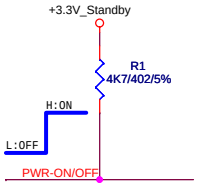
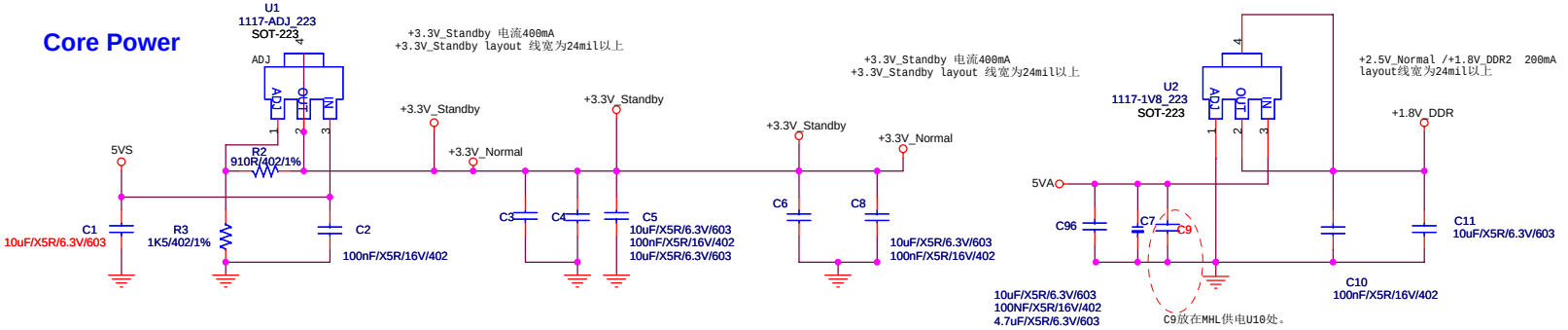
Power Input

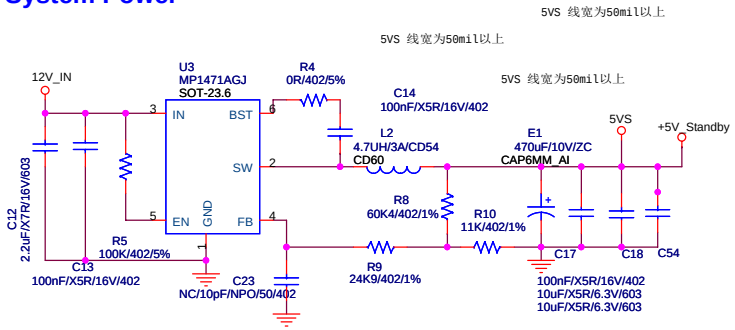
Standby controler



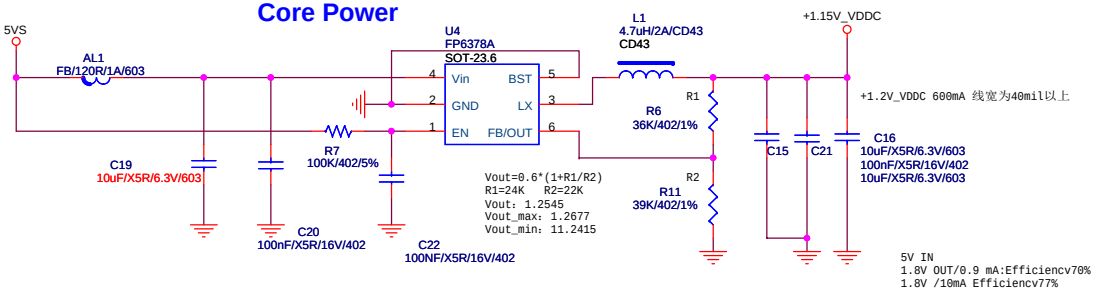
Core Power



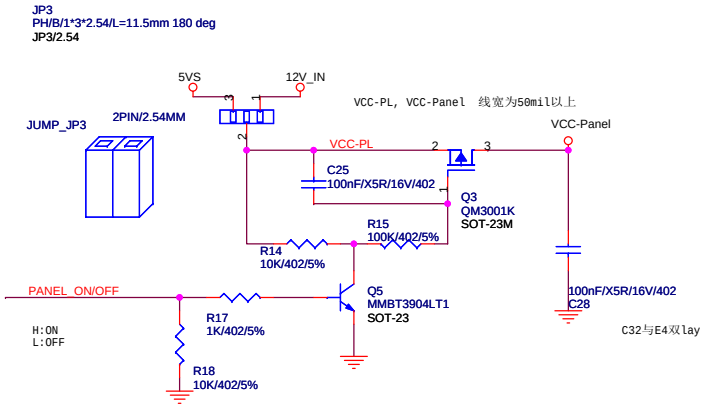
System Power



Core Power

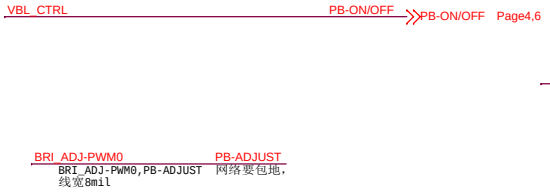


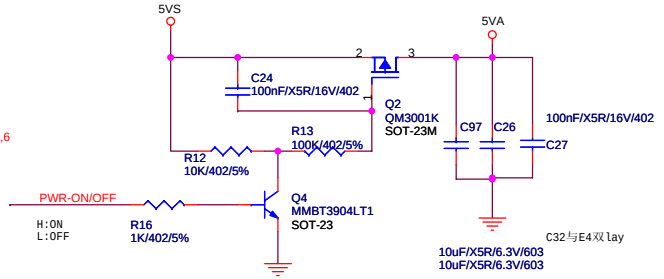
PANEL POWER

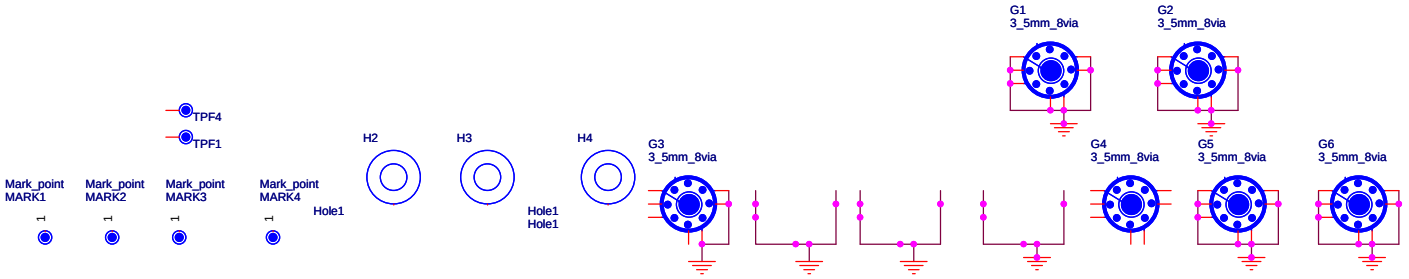


Inverter controler

VBL_CTRL	Panel Backlight
H	OFF
L	ON







VBL_CTRL Page4,6
BRI_ADJ-PWM0 Page4,6
PANEL_ON/OFF Page6
PWR-ON/OFF Page6
PB-ADJUST Page4,6

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SheetName: 05.System Power

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A3	P75-3463GU V6.0	A

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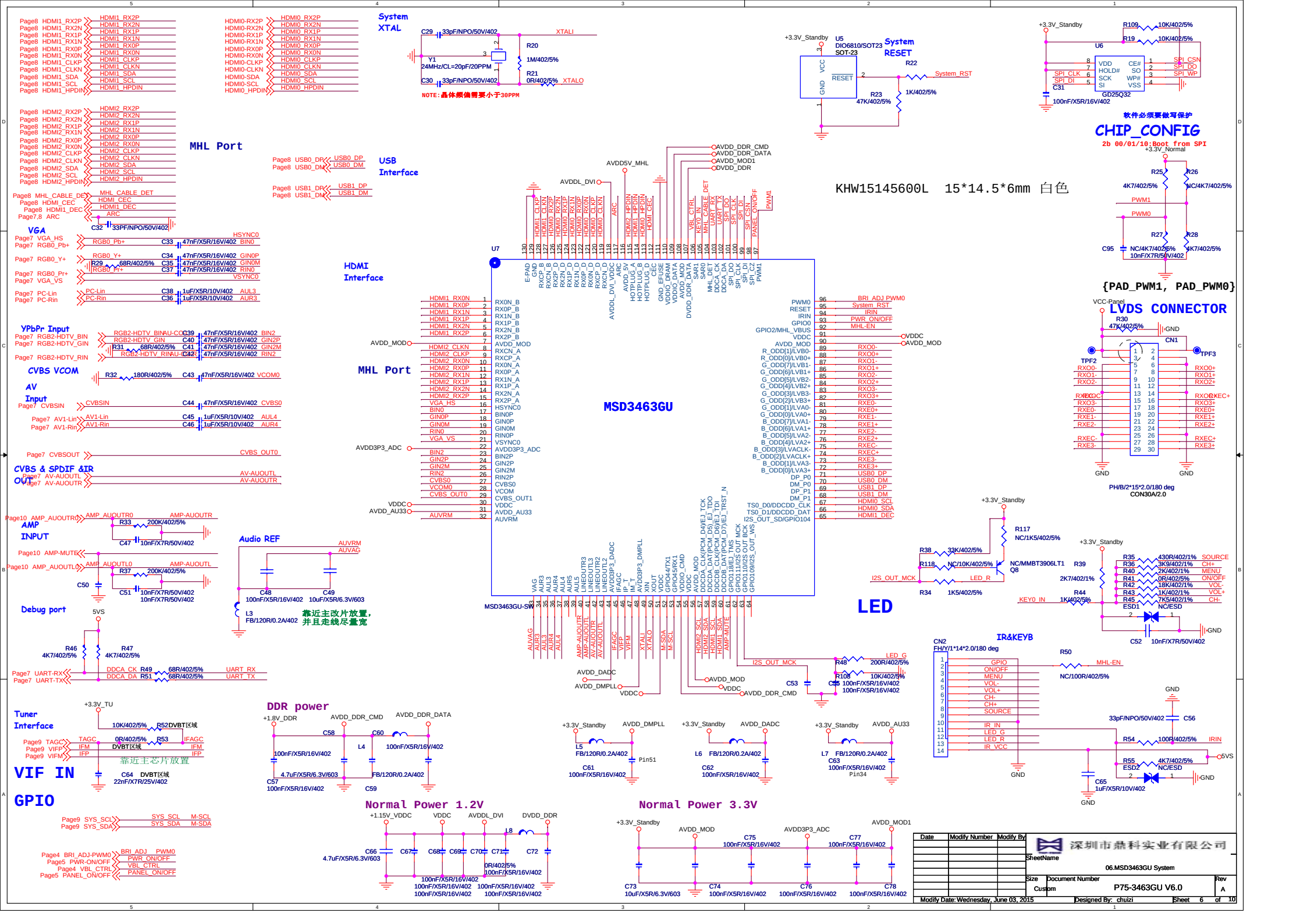
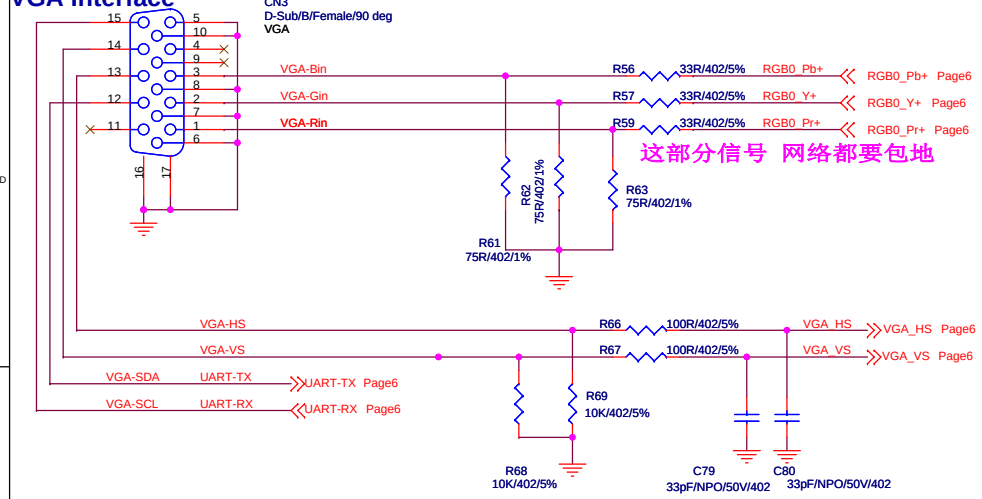
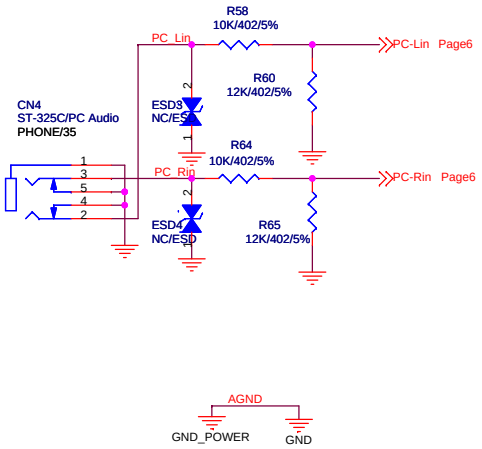

MHL Port
USB Interface
System XTAL
System RESET
CHIP_CONFIG
软件必须要做写保护
2b 00/01/10:Boot from SPI
KHW15145600L 15*14.5*6mm 白色
VGA
YPbPr Input
CVBS VCOM
AV Input
CVBS & SPDIF &IR OUT
AMP INPUT
Debug port
Audio REF
HDMI Interface
MSD3463GU
LED
LVDS CONNECTOR
IR&KEYB
Tuner Interface
VIF IN
GPIO
DDR power
Normal Power 1.2V
Normal Power 3.3V
靠近主芯片放置
靠近主芯片放置，并且走线尽量宽
DVBT区域
{PAD_PWM1, PAD_PWM0}
深圳市鼎科实业有限公司
06.MSD3463GU System
P75-3463GU V6.0
Modify Date: Wednesday, June 03, 2015
Designed By: chuizi

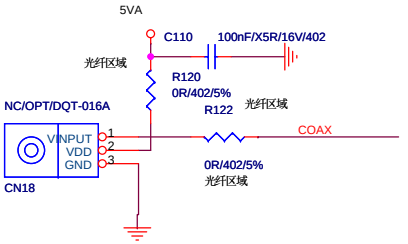
VGA Interface



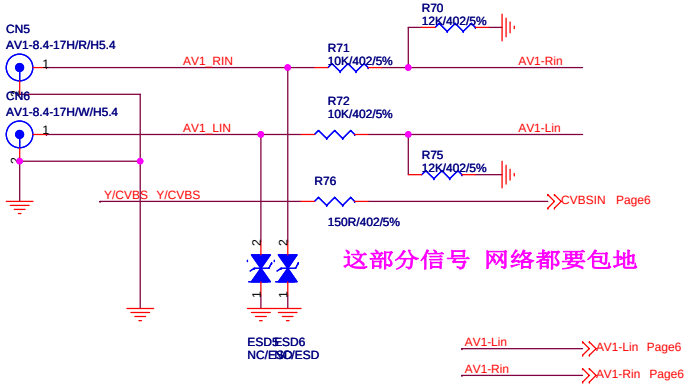
PC Audio In



光纤区域

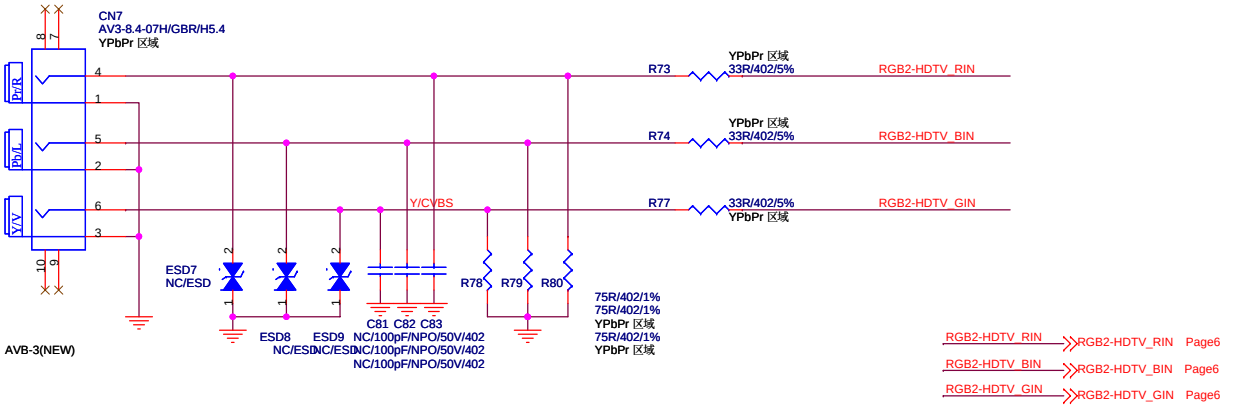


AV1 Interface

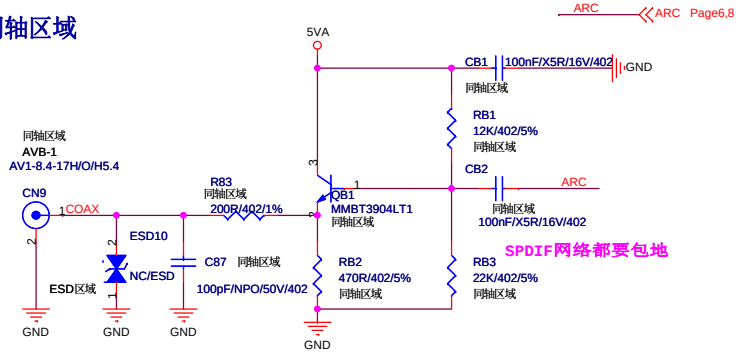


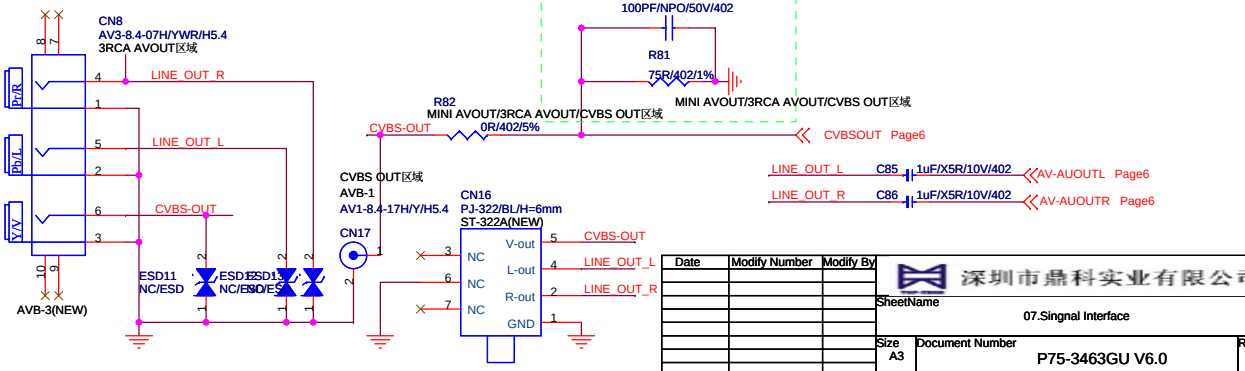
YPBPR_IN Interface

这部分信号 网络都要包地



同轴区域





Date	Modify Number	Modify By

深圳市鼎科实业有限公司

SheetName: 07.Singnal Interface

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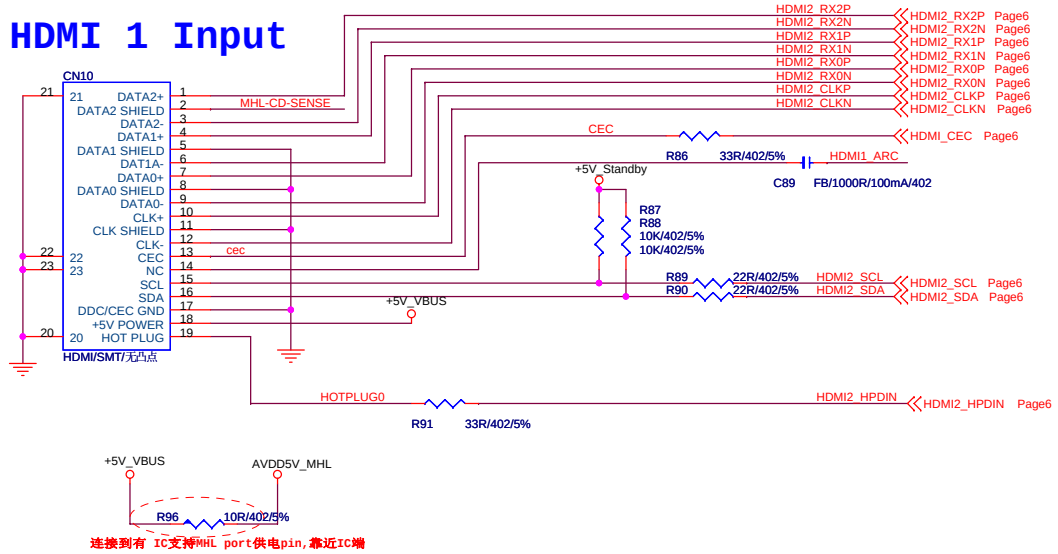
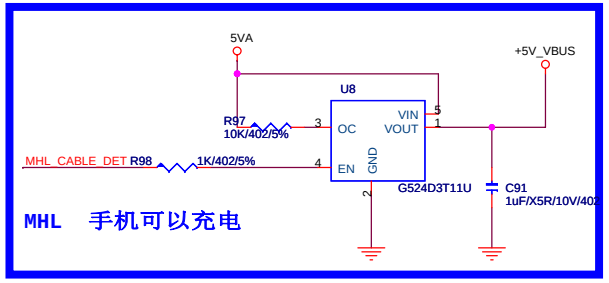
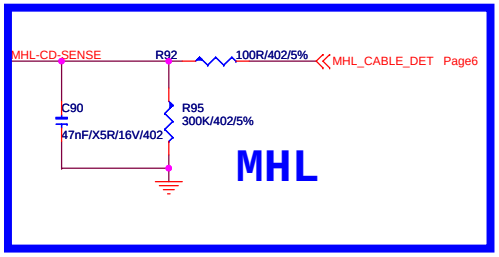
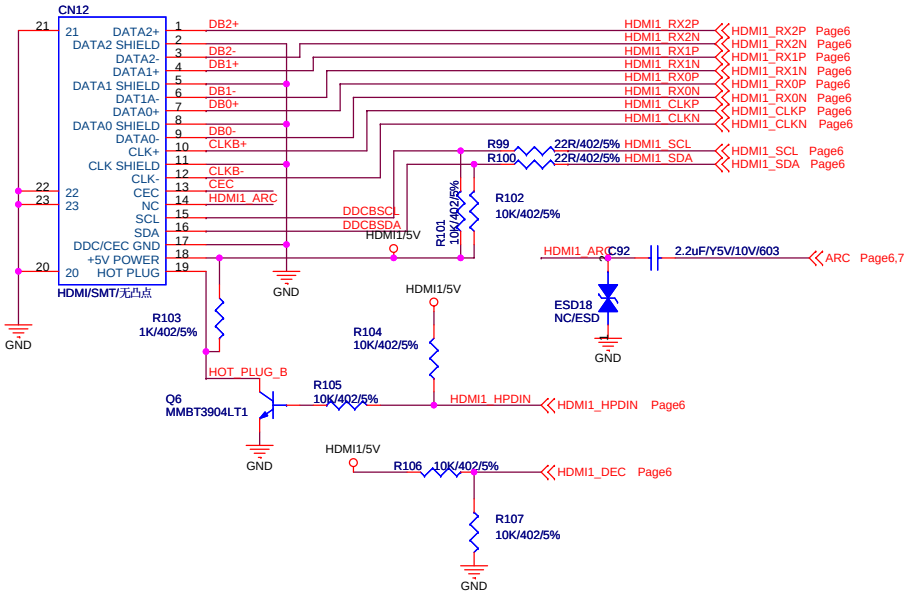
HDMI 1 Input

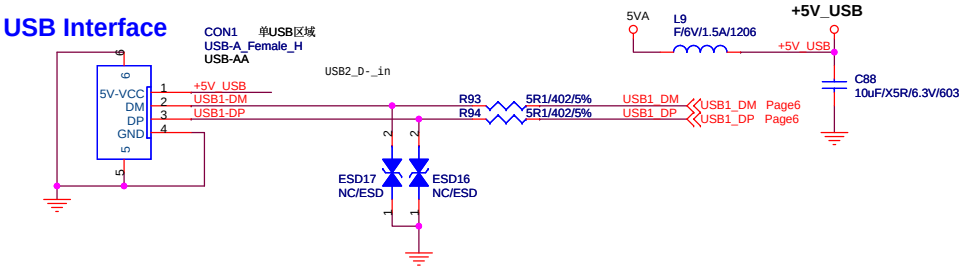


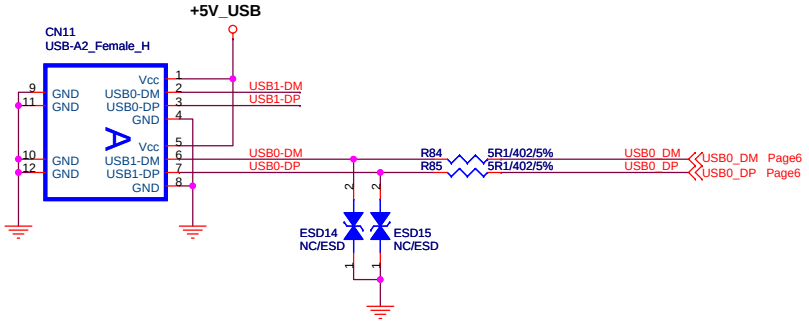


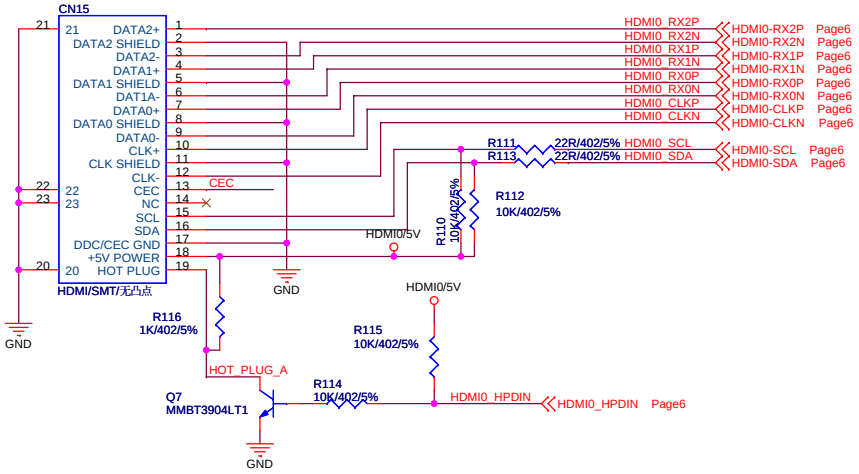




USB Interface







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SheetName: 08.HDMI & USB

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A3	P75-3463GU V6.0	A

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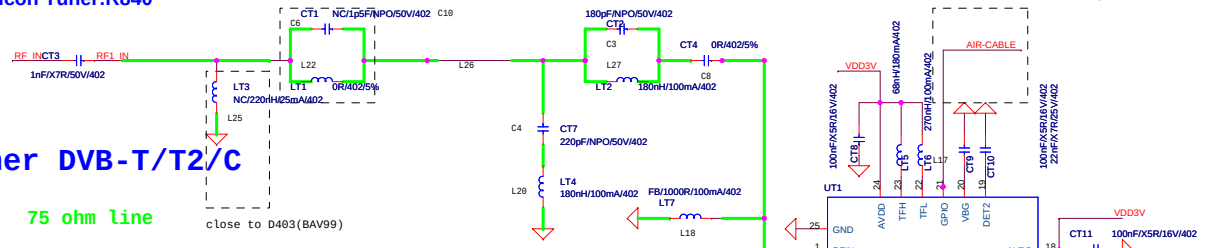
硅tuner DVB-T/C

Silicon Tuner:R840

optional component of WIFI filter,
if no need this option, pls short it

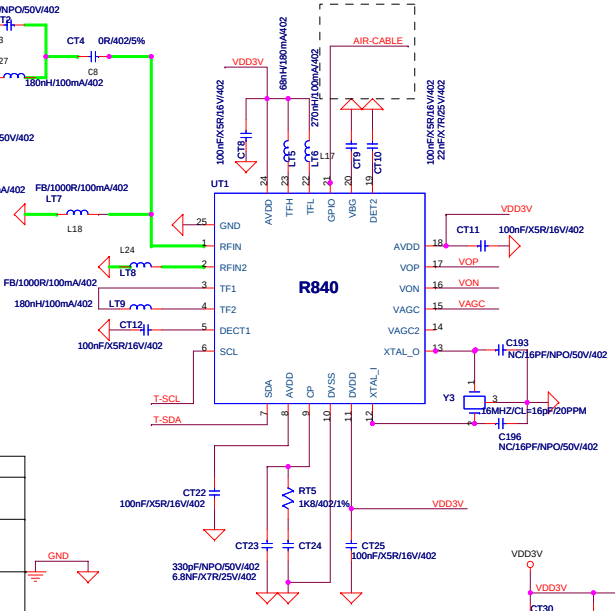
for GPIO purpose. R22=10kR for GPIO.
R22=NC if no need this option.

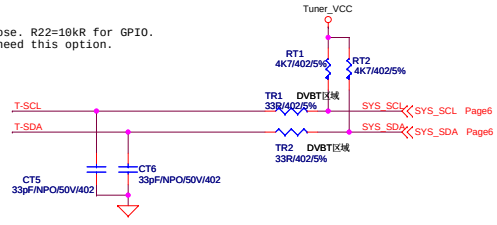
for GPIO purpose. R22=10kR for GPIO.
R22=NC if no need this option.

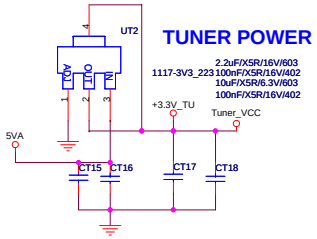


硅tuner DVB-T/T2/C

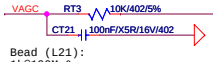
75 ohm line





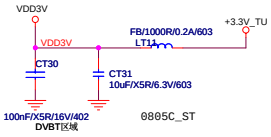


close to tuner



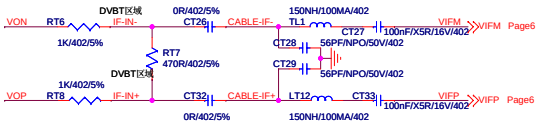
Bead (L21):
1k@100M &
400ohm@400M,300mA

Application
DTMB_bypass
L17=L18=GZ1005D102CTF, C3=C4=C10=L20=L25=NC, C8=L26=L27=0R
Other standard_bypass
L17=270nH, L18=GZ1005D102CTF, C3=C4=C10=L20=L25=NC, C8=L26=0R
Hybrid (with S1 filter for EN55020)
L17=L18=L20=L25=270nH, C8=82pF, C3=C10=270pF, C4=100pF, L27=180nH



if no need VAGC2, pls R111=C111=NC

IF Interface Filter

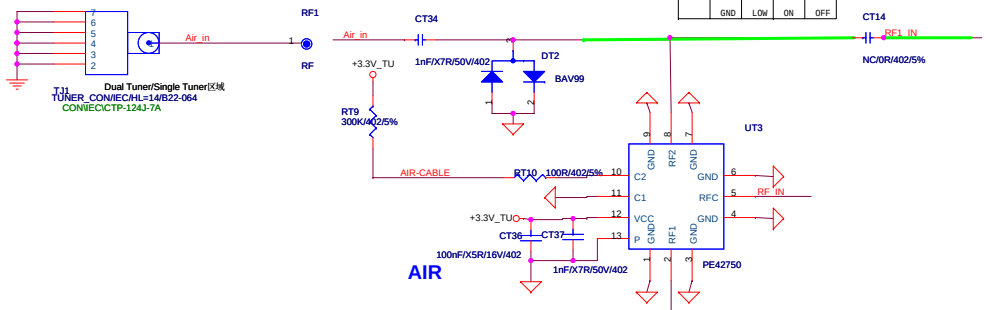


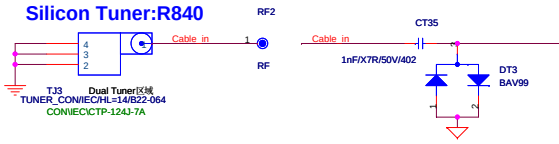
Silicon Tuner:R840

RF SWITCH

CABLE [DVB_T+ISDB]

	C1	C2	RF1	RF2
	GND	HIGH	OFF	ON
	GND	LOW	ON	OFF





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SheetName: 9.Front End

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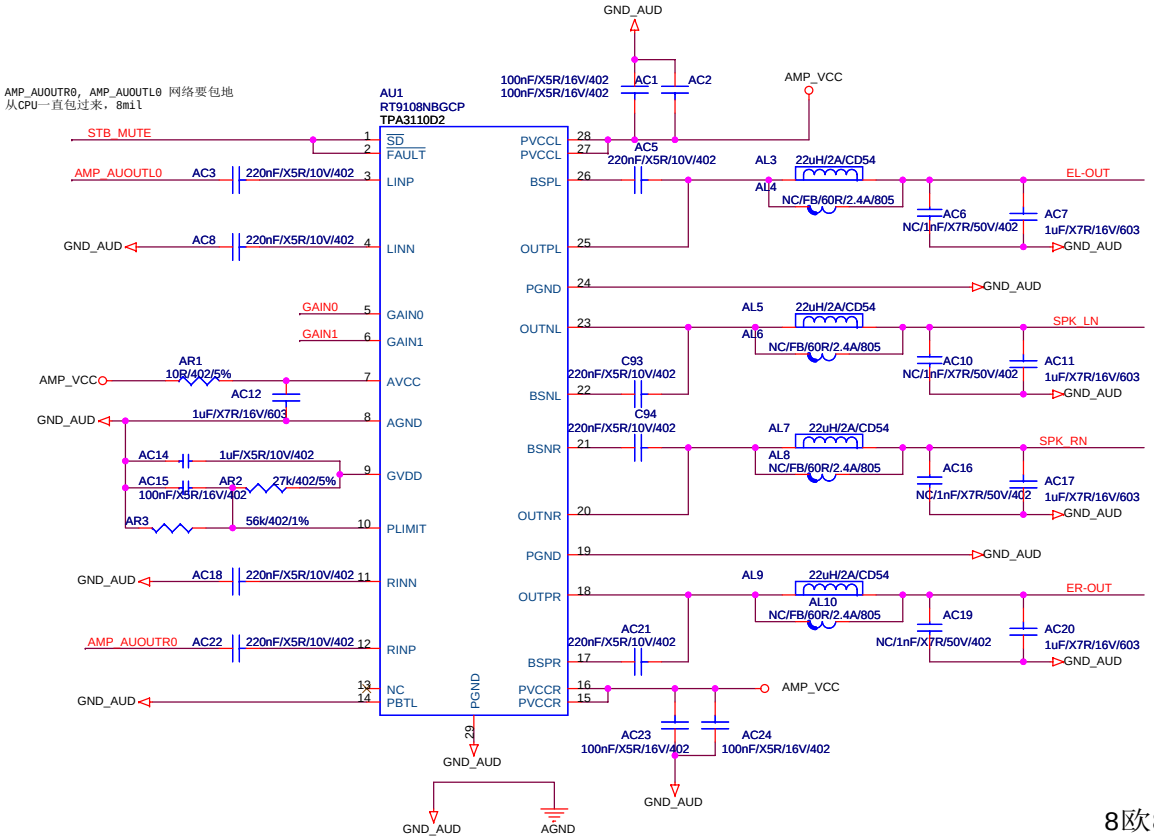
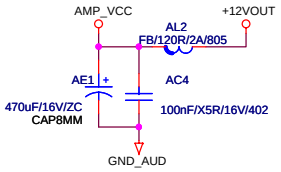
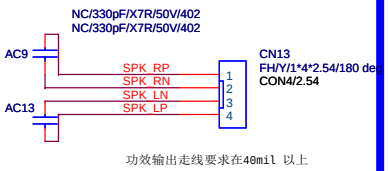
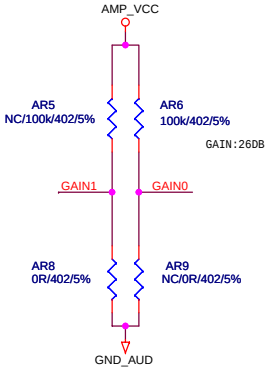
EARPHONE OUT





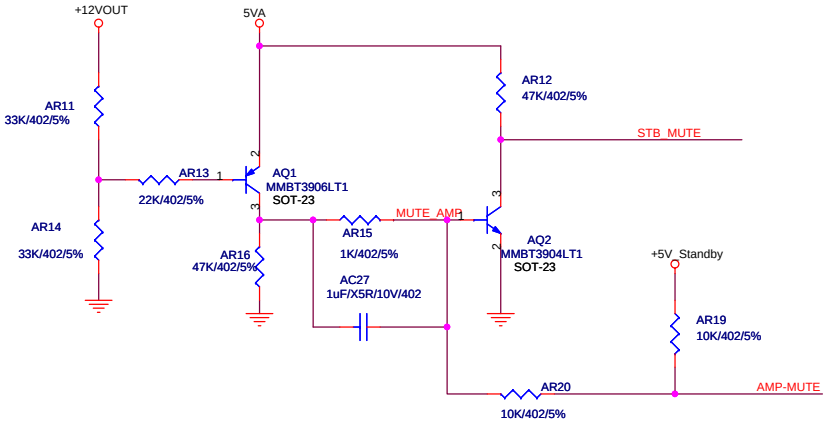


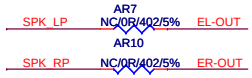
功效输出走线要求在40mil 以上

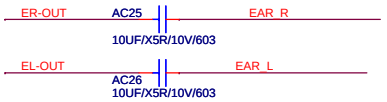


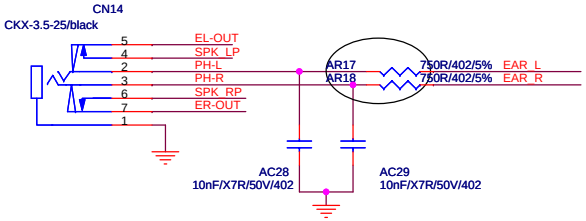
8欧8瓦

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9









PIN NAME	Pin #	I/O/P	DESCRIPTION
SD	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
FAULT	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULT pin to SD pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.

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SheetName: 10..Amplify

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