

FEATURES

n NTSC/PAL/SECAM Video Decoder

- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- 2D NTSC and PAL comb-filter for Y/C separation
- 4 configurable CVBS & Y/C S-video inputs
- Supports Closed-caption, and V-chip
- CVBS video output

n Video IF for Multi-Standard Analog TV

- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

n Multi-Standard TV Sound Decoding/Processing

- Supports BTSC/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, and P/G EQ
- Mstar surround sound effect

n Digital Audio Interface

- I²S digital audio output
- HDMI audio channel processing capability
- Audio Line-In L/R x3
- Audio Line-Out L/R x2
- Built-in audio DAC
- Built-in audio ADC
- SIF audio input

n Analog RGB Compliant Input Ports

- Two analog ports support up to UXGA
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

n DVI/HDCP/HDMI Compliant Input Port

- One DVI/HDMI input port
- Supports TMDS clock up to 225MHz @ 1080P 60Hz
- Single link on-chip DVI 1.0 compliant receiver

- High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver

- High Definition Multimedia Interface (HDMI) 1.3 compliant receiver with CEC support

- Long-cable tolerant robust receiving

- Support HDTV up to 1080P

n Auto-Configuration/Auto-Detection

- Auto input signal format and mode detection

- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection

- Sync detection for H/V Sync

n High-Performance Scaling Engines

- Fully programmable shrink/zoom capabilities

- Nonlinear video scaling supports various modes including Panorama

n Video Processing & Conversion

- 2-D motion adaptive video de-interlacer

- Automatic 3:2 pull-down & 2:2 pull-down detection and recovery

- Edge-oriented adaptive algorithm for smooth low-angle edges

- MStar 3rd Generation Advanced Color Engine (MStarACE-3) automatic picture enhancement gives:

- Brilliant and fresh color

- Intensified contrast and details

- Vivid skin tone

- Sharp edge

- Enhanced depth of field perception

- Accurate and independent color control

- sRGB compliance allows end-user to experience the same colors as viewed on CRTs and other displays

- Programmable 10-bit RGB gamma CLUT

n On-Screen OSD Controller

- 128/256 color palette
- 512 1/2/3-bit/pixel fonts
- Supports 2K attribute/code
- Horizontal and vertical stretch of OSD menus
- Pattern generator for production test
- Supports OSD MUX and alpha blending capability
- Supports blinking and scrolling for closed caption applications

n LVDS Panel Interface

- Supports 8-bit dual link LVDS up to full HD (1920x1080)
- Supports 2 data output formats: Thine & TI data mappings
- Compatible with TIA/EIA

- Dithering with 6/8 bits options
- Reduced swing for LVDS for low EMI
- Supports flexible spread spectrum frequency with 360Hz~11.8MHz and up to 25% modulation

n Integrated Micro Controller

- Embedded 8032 micro controller
- Configurable PWM's and GPIO's
- Low-speed ADC inputs for system control
- SPI bus for external flash

n Miscellaneous

- 128-pin LQFP package
- Integrated power management control with independent power plant to support deep sleep, and wake-up from various input

GENERAL DESCRIPTION

The TSUMV26KU is a high performance and all-in-one IC for multi-function LCD monitor/TV with resolutions up to full HD (1920x1080). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard A/V front-end and baseband decoder, a video de-interlacer, a scaling engine, the MStarACE-3 color engine, an on-screen display controller and a built-in output panel interface. An embedded audio DSP processor gives various of audio manipulation functions for greater audience experiences.

To further reduce system costs, the TSUMV26KU also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	165			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		165	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		15		ps/°C
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		1.5		V
Output High		2.0		V

Parameter	Min	Typ	Max	Unit
AUDIO				
ADC Input		2.0		V p-p
DAC Output		2.0		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p
FSSW Input ¹	0		1.8	V
SAR ADC Input	0		3.3	V
FB ADC Input ²	0		1.25	V

Specifications subject to change without notice.

Notes:

1. Input full scale is typically 1.8V, but input range is 0 ~ 3.3V.
2. Input full scale is 1.25V, but input range is 0 ~ 3.3V.

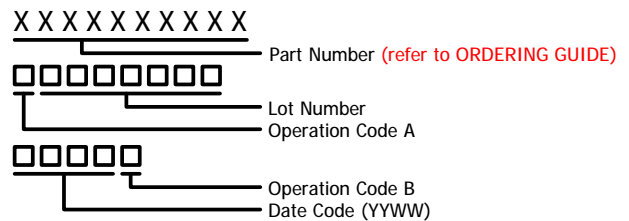
Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	3.14		3.6	V
1.26V Supply Voltages	V_{VDD_126}	1.2		1.32	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$			5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}			V_{VDD_33}	V
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Junction Temperature	T_J			150	°C

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
TSUMV26KU-LF	0°C to +70°C	LQFP	128

MARKING INFORMATION



DISCLAIMER

MSTAR SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. NO RESPONSIBILITY IS ASSUMED BY MSTAR SEMICONDUCTOR ARISING OUT OF THE APPLICATION OR USER OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.



Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. TSUMV26KU comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
TSUMV26KU_ds_v01	ÿ Initial release	May 2009

REGISTER DESCRIPTION

ISP Register (Bank = 08)

ISP Register (Bank = 08)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (0800h)	REG0800	7:0	Default : 0x55	Access : R/W
	ISP_PASSWORD[7:0]	7:0	ISP Password 0xAAAA. If password correct, enable ISP. If password incorrect, disable ISP.	
00h (0801h)	REG0801	7:0	Default : 0x55	Access : R/W
	ISP_PASSWORD[15:8]	7:0	See description of '0800h'.	
01h (0802h)	REG0802	7:0	Default : 0x00	Access : WO
	SPI_COMMAND[7:0]	7:0	SPI command. If write data to this port, ISP will start operation.	
02h (0804h)	REG0804	7:0	Default : 0x00	Access : R/W
	ADDRESS1[7:0]	7:0	SPI address 1, A[7:0].	
02h (0805h)	REG0805	7:0	Default : 0x00	Access : R/W
	ADDRESS2[7:0]	7:0	SPI address 2, A[15:8].	
03h (0806h)	REG0806	7:0	Default : 0x00	Access : R/W
	ADDRESS3[7:0]	7:0	SPI address 3, A[23:16].	
04h (0808h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
05h (080Ah)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
06h (080Ch)	REG080C	7:0	Default : 0x04	Access : R/W
	SPI_CLK_DIV16	7	SPI_CLOCK = MCU_CLOCK/16.	
	SPI_CLK_DIV8	6	SPI_CLOCK = MCU_CLOCK/8.	
	SPI_CLK_DIV7	5	Reserved.	
	SPI_CLK_DIV6	4	Reserved.	
	SPI_CLK_DIV5	3	Reserved.	
	SPI_CLK_DIV4	2	SPI_CLOCK = MCU_CLOCK/4.	
	SPI_CLK_DIV3	1	Reserved.	
	SPI_CLK_DIV2	0	SPI_CLOCK = MCU_CLOCK/2.	
06h (080Dh)	REG080D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPI_CLK_DIV128	2	SPI_CLOCK = MCU_CLOCK/128.	

ISP Register (Bank = 08)				
Index (Absolute)	Mnemonic	Bit	Description	
	SPI_CLK_DIV64	1	SPI_CLOCK = MCU_CLOCK/64.	
	SPI_CLK_DIV32	0	SPI_CLOCK = MCU_CLOCK/32.	
07h (080Eh)	REG080E	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DEVICE_SELECT[2:0]	2:0	Select Device. 000: PMC-MXIC. 001: NextFlash. 010: ST. 011: SST. 100: ATMEL.	
08h (0810h)	REG0810	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	SPI_CE_CLR	0	SPI chip enable clear. Software can force SPI chip disable at burst SPI read/write, this bit is write-then-clear register. 1: For clear. 0: For not clear.	
09h (0812h)	REG0812	7:0	Default : 0x01	Access : R/W
	TCES_TIME[7:0]	7:0	SPI Chip enable setup/hold time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delay 2 SPI clock.	
09h (0813h)	REG0813	7:0	Default : 0x00	Access : R/W
	TCES_TIME[15:8]	7:0	See description of '0812h'.	
0Ah (0814h)	REG0814	7:0	Default : 0xF3	Access : R/W
	TBP_TIME[7:0]	7:0	Byte-Program time for device SST. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delay 500 SPI clock. Assume SPI clock 40ns, Delay 500*40 = 20 us.	
0Ah (0815h)	REG0815	7:0	Default : 0x01	Access : R/W
	TBP_TIME[15:8]	7:0	See description of '0814h'.	
0Bh	REG0816	7:0	Default : 0x04	Access : R/W

ISP Register (Bank = 08)				
Index (Absolute)	Mnemonic	Bit	Description	
(0816h)	TCEH_TIME[7:0]	7:0	SPI Chip enable pulse high time. 0x0000: Delay 1 SPI clock. 0x0001: Delay 2 SPI clock. 0x000f: Delay 16 SPI clock. 0xffff: Delay 64k SPI clock. Default delay 5 SPI clock.	
0Bh (0817h)	REG0817	7:0	Default : 0x00	Access : R/W
	TCEH_TIME[15:8]	7:0	See description of '0816h'.	
0Ch (0818h)	REG0818	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	SPI_RD_REQ	0	SPI READ Data Request, For CPU read SPI data via RIU. If CPU read SPI data via XIU, request not needed.	
0Dh (081Ah)	REG081A	7:0	Default : 0x14	Access : R/W
	ISP_RP_ADR1[7:0]	7:0	Programmable ISP Read port address[15:0].	
0Dh (081Bh)	REG081B	7:0	Default : 0xC2	Access : R/W
	ISP_RP_ADR1[15:8]	7:0	See description of '081Ah'.	
0Eh (081Ch)	REG081C	7:0	Default : 0x81	Access : R/W
	ISP_RP_ADR2[7:0]	7:0	Programmable ISP Read port address[31:0].	
0Eh (081Dh)	REG081D	7:0	Default : 0x1F	Access : R/W
	ISP_RP_ADR2[15:8]	7:0	See description of '081Ch'.	
0Fh (081Eh)	REG081E	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	ENDIAN_SEL_SPI	0	0: Big_endian. 1: Little_endian.	
10h (0820h)	REG0820	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	ISP_ACTIVE	0	ISP ACTIVE FLAG.	
11h (0822h)	REG0822	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	CPU_ACTIVE	1	CPU_ACTIVE FLAG.	
	-	0	Reserved.	
12h (0824h)	REG0824	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	DMA_ACTIVE	2	DMA_ACTIVE FLAG.	

ISP Register (Bank = 08)				
Index (Absolute)	Mnemonic	Bit	Description	
	-	1:0	Reserved.	
13h (0826h)	REG0826	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	ISP_FSM[5:0]	5:0	ISP_FSM.	
14h (0828h)	REG0828	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	SPI_MASTER_FSM[2:0]	2:0	SPI_MASTER_FSM.	
15h (082Ah)	REG082A	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	SPI_RD_DATA_RDY	0	SPI Read Data Ready flag. 1: Read data ready. 0: Read data not ready.	
16h (082Ch)	REG082C	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	SPI_WR_DATA_RDY	0	SPI Write Ready flag. 1: Write data ready. 0: Write data not ready.	
17h (082Eh)	REG082E	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	SPI_WR_CM_RDY	0	SPI Write Command Ready flag. 1: Write command ready. 0: Write command not ready.	
18h (0830h)	REG0830	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	CPU_RST_FM_ISP	0	ISP generate reset to CUP. When ISP programming done, software maybe can. Issue a reset to CPU.	
19h (0832h)	REG0832	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	ISP_OLD_EN	0	Read flag, for ISP_OLD_EN.	
20h (0840h)	REG0840	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	FORCE_ISP_IDLE	0	FORCE_ISP_IDLE.	
21h	REG0842	7:0	Default : 0x00	Access : R/W

ISP Register (Bank = 08)				
Index (Absolute)	Mnemonic	Bit	Description	
(0842h)	AAI_NUM[7:0]	7:0	For SST SPI FLASH USE. At AAI mode, set how many data will be written. 0x0000: For 1 byte programming. 0x0001: For 2 byte programming. 0xFFFF: For 64k byte programming.	
21h	REG0843	7:0	Default : 0x00	Access : R/W
(0843h)	AAI_NUM[15:8]	7:0	See description of '0842h'.	
22h	REG0844	7:0	Default : 0x00	Access : R/W
(0844h)	PAGE_PRO_REG	7	FORCE SPI COMMAND. Force PAGE PROGRAMMING.	
	FAST_READ_REG	6	FORCE SPI COMMAND. Force FAST READ.	
	READ_REG	5	FORCE SPI COMMAND. Force READ.	
	WRCR_REG	4	FORCE SPI COMMAND. Force WRCR.	
	RDCR_REG	3	FORCE SPI COMMAND. Force RDCR.	
	WRSR_REG	2	FORCE SPI COMMAND. Force WRSR.	
	RDSR_REG	1	FORCE SPI COMMAND. Force RDSR.	
	AAI_REG	0	FORCE SPI COMMAND. Force AAI mode.	
22h	REG0845	7:0	Default : 0x00	Access : R/W
(0845h)	-	7:2	Reserved.	
	MAN_ID_REG	1	FORCE SPI COMMAND. Force READ MANUFACTURER ID.	
	B_ERASE_REG	0	FORCE SPI COMMAND. Force BLOCK ERASE.	
25h ~ 25h	-	7:0	Default : -	Access : -
(084Ah ~ 084Bh)	-	-	Reserved.	
26h	REG084C	7:0	Default : 0x01	Access : R/W
(084Ch)	-	7:1	Reserved.	
	TEST_SPI_CEB	0	User generate SPI chip enable waveform.	

ISP Register (Bank = 08)				
Index (Absolute)	Mnemonic	Bit	Description	
27h (084Eh)	REG084E	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	TEST_SPI_SCK	0	User generate SPI clock waveform.	
28h (0850h)	REG0850	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	TEST_SPI_SI	0	User generate SPI data waveform.	
29h (0852h)	REG0852	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	TEST_SPI_SO	0	SPI Data output. For RIU read. Please delay 1us for every setting(TEST MODE). EX1: W(0x21,0x0) --> delay 1us --> W(0x23,0x1) -->. Delay 1us --> W(0x22,0x1) --> delay 1us -->. W(0x22,0x0) --> delay 1us.....--> W(0x21,0x1). EX2: W(0x21,0x0) --> delay 1us --> W(0x22,0x1) -->. Delay 1us --> W(0x22,0x0) --> delay 1us -->. R(0x24) --> delay 1us.....> W(0x21,01).	
2Ah (0854h)	REG0854	7:0	Default : 0x00	Access : R/W
	TRIGGER_MODE[7:0]	7:0	TRIGGER_MODE,. 0x3333: Trigger mode. others: Not Trigger mode. Before entry Trigger mode, Please make sure. ISP/DMA disable.	
2Ah (0855h)	REG0855	7:0	Default : 0x00	Access : R/W
	TRIGGER_MODE[15:8]	7:0	See description of '0854h'.	
2Fh (085Eh)	REG085E	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SPI_ABORT_EN	1	Reserved.	
	SPI_PRE_FETCH_EN	0	Reserved.	
30h (0860h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
31h ~ 34h (0862h ~ 0868h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
35h ~ 35h	-	7:0	Default : -	Access : -

ISP Register (Bank = 08)				
Index (Absolute)	Mnemonic	Bit	Description	
(086Ah ~ 086Bh)	-	-	Reserved.	
36h (086Ch)	REG086C	7:0	Default : 0x01	Access : R/W
	CHIP_SELECT8	7	Chip_select for SPI Device6. 1: Enable. 0: Disable.	
	CHIP_SELECT7	6	Chip_select for SPI Device5. 1: Enable. 0: Disable.	
	CHIP_SELECT6	5	Chip_select for SPI Device4. 1: Enable. 0: Disable.	
	CHIP_SELECT5	4	Chip_select for SPI Device3. 1: Enable. 0: Disable.	
	CHIP_SELECT4	3	Chip_select for SPI Device2. 1: Enable. 0: Disable.	
	CHIP_SELECT3	2	Chip_select for SPI Device1. 1: Enable. 0: Disable.	
	-	1:0	Reserved.	
37h (086Eh)	REG086E	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	CPHA	1	Configures the data sampling point. When 0, data is sampled when "SCLK" goes to active state(see reg_cpol). When 1, data is sampled when "SCLK" goes to idle state(see reg_cpol).	
	CPOL	0	Clock Polarity. Configures the idle state of "SCLK" serial clock when SPI is enabled (when disabled, "SCLK" is in high level). When 1, the "SCLK" output is set (SCLK = 1) otherwise it is cleared(SCLK = 0).	
3Fh (087Eh)	REG087E	7:0	Default : 0x07	Access : R/W
	-	7:3	Reserved.	
	SPI_BURST_RESET_Z	2	Software reset spi_burst.	

ISP Register (Bank = 08)			
Index (Absolute)	Mnemonic	Bit	Description
			0: Reset. 1: Not reset.
	SPI_ARBITER_RESET_Z	1	Software reset spi arbiter. 0: Reset. 1 not reset.
	ISP_TOP_RESET_Z	0	Software reset isp_top. 0: Reset. 1: Not reset.

QSPI Register (Bank = 08)

QSPI Register (Bank = 08)				
Index (Absolute)	Mnemonic	Bit	Description	
70h (08E0h)	REG08E0	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CKG_SPI[5:0]	5:0	CKG_SPI[5:0]: for spi clock selection. Bit[0]: for gating clock. Bit[1]: for clock invert. Bit[5]: 0, select XTAL. 1, It is decided by Bit[4:2]. Bit [4:2]. 000: XTAL. 001: 27M. 010: 36M. 011: 43M. 100: 54M. 101: 72M. Others: Reserved.	
71h (08E2h)	REG08E2	7:0	Default : 0x1A	Access : R/W
	CSZ_SETUP[3:0]	7:4	CSZ setup time. (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
	CSZ_HIGH[3:0]	3:0	CSZ deselect time (SCZ = high). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
71h (08E3h)	REG08E3	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CSZ_HOLD[3:0]	3:0	CSZ hold time. (relative to SCK). 4'h0: 1 SPI clock cycle. 4.h1: 2 SPI clock cycles. 4'hf: 16 SPI clock cycles.	
72h (08E4h)	REG08E4	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CM2_ADR2_DATA2	3	Reserved.	
	CM1_ADR2_DATA2	2	Enable address & data dual mode, (SPI command is 0xBB).	

QSPI Register (Bank = 08)			
Index (Absolute)	Mnemonic	Bit	Description
	CM1_ADR1_DATA2	1	Enable data dual mode, (SPI command is 0x3B).
	FAST_MODE	0	Enable fast read mode, (SPI command is 0x0B).
72h (08E5h)	REG08E5	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	CM1_ADR4_DATA4	0	Enable address & data quad mode, (SPI command is 0xeB).
7Fh (08FEh)	REG08FE	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	ENDIA	0	For 32bit CPU read data.

ADC_PLL Register (Bank = 0A)

ADC_PLL Register (Bank = 0A)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (0A00h)	REG0A00	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	TAGC_PWR	6	Tuner AGC power control. 1: Power on. 0: Power off.	
	-	5	Reserved.	
	VIF_CBC_PWRS	4	Power on the sound path of central bias circuit. 1: Power on.(VIF_CBC_PWR must =1) 0:power off.	
	VIF_CBC_PWR	3	Power on central bias circuit. 1: Power on. 0: Power off.	
	VIF_PLL_PWR	2	Power on VIF PLL. 1: Power on. 0: Power off.	
	VIF_VCOREG_PWR	1	VCO regulator power on. 1: Power on. 0: Power off.	
	VIF_VCO_PWR	0	VCO power on, 1:power on. 0: Power off.	
00h (0A01h)	REG0A01	7:0	Default : 0x00	Access : R/W
	VIF_PGPWRV	7	PGA1_V power on. 1: Power on. 0: Power off.	
	VIF_MXPWRV	6	MX_V power on. 1: Power on. 0: Power off.	
	VIF_PWR_LPFV	5	LPF_V power on. 1: Power on. 0: Power off.	
	VIF_PWR_PGA2V	4	PGA2_V power on. 1: Power on. 0: Power off.	
	VIF_PGPWRS	3	PGA1_S power on. 1: Power on. 0: Power off.	

ADC_PLL Register (Bank = 0A)				
Index (Absolute)	Mnemonic	Bit	Description	
	VIF_MXPWRS	2	MX_S power on. 1: Power on. 0: Power off.	
	VIF_PWR_LPFS	1	LPF_S power on. 1: Power on. 0: Power off.	
	VIF_PWR_PGA2S	0	PGA2_S power on. 1: Power on. 0: Power off.	
01h (0A02h)	REG0A02	7:0	Default : 0x14	Access : R/W
	-	7:5	Reserved.	
	VIF_PLL_RSTZ	4	Reset the feedback divider. 0: Reset. 1: Normal operation.	
	-	3:2	Reserved.	
	VIF_PLL_R[1:0]	1:0	Regulator input source and output voltage setting. See Table 1.	
01h (0A03h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
02h (0A04h)	REG0A04	7:0	Default : 0x24	Access : R/W
	TAGC_ODMODE	7	TAGC DAC output open-drain mode. 1: Open-drain voltage output. 0: 1mA current sink output.	
	-	6	Reserved.	
	VIF_PLL_MSEL	5	Bypass feedback divider re-sync function. 1: Resync. 0: Bypass resync.	
	-	4	Reserved.	
	VIF_PLL_M[3:0]	3:0	PLL post divider (Divion ratio = 2~15).	
02h (0A05h)	REG0A05	7:0	Default : 0x59	Access : R/W
	VIF_PLL_RSEL	7	Bypass reference divider. 1: Bypass(divide-by-1). 0: Normal operation(divide-by-2 or 3).	
	VIF_PLL_RDIV	6	PLL reference divider. 1: Fxtal/3. 0: Fxtal/2.	

ADC_PLL Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
	VIF_PLL_N[5:0]	5:0	PLL feedback divider (Divion ratio = 2~63).default:divide-by-25.
03h (0A06h)	REG0A06	7:0	Default : 0x05
	-	7:4	Reserved.
	VIF_PLL_LPEX	3	Charge pump current power control. 1: Power off. 0: Power on.
	-	2:0	Reserved.
03h (0A07h)	REG0A07	7:0	Default : 0x08
	-	7:5	Reserved.
	VIF_PLL_SBIAS	4	VCO self bias enable. 1: Enable. 0: Disable.
	VIF_VCO_REF	3	VCO bandgap reference voltage selection. 1: 1.20V. 0: 1.10V.
	VIF_VCOREG_SBIAS	2	VCO self bias enable. 1: Enable. 0: Disable.
	-	1:0	Reserved.
04h (0A08h)	REG0A08	7:0	Default : 0x44
	VIF_CAL_START	7	VCO band calibration start. 1: Enable. 0: No operation. (self-clear).
	VIF_VCO_LK	6	Kvco control bit 1. 1: Kvco~170MHz/V. 0: Kvco~120MHz/V.
	-	5	Reserved.
	VIF_VCO_LP	4	VCO low power mode. 1: 4m. 0: 6mA.
	VIF_PLL_CPINIT_W	3	Override bit for charge pump output open and tied to 1.50V. 1: Charge pump output tied to 1.50V. 0: Normal operation.
	VIF_VCO_BANK_W[2:0]	2:0	Override bits for VCO bank selection.

ADC_PLL Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
			See Table 4.
04h (0A09h)	REG0A09	7:0	Default : 0x00
	VIF_PGA1GAINV_W[3:0]	7:4	Override bits for PGA1_S gain setting low byte. See Table 5.
	VIF_PGA1GAINS_W[3:0]	3:0	Override bits for PGA1_S gain setting low byte. See Table 5.
05h (0A0Ah)	REG0A0A	7:0	Default : 0x00
	VIF_GAIN_PGA2V_W[3:0]	7:4	Override bits for PGA2_V gain setting high byte. See Table 6.
	VIF_GAIN_PGA2S_W[3:0]	3:0	Override bits for PGA2_S gain setting low byte. See Table 6.
05h (0A0Bh)	REG0A0B	7:0	Default : 0xAA
	VIF_CALIB_TUNE	7	LPF calibration enable (power on). 1: Enable. 0: Disable.
	-	6	Reserved.
	VIF_RN_TUNE	5	Reset for LPF tuning circuit. 1: Normal operation. 0: Reset (restart calibration after reset finished).
	-	4:0	Reserved.
06h ~ 07h (0A0Ch ~ 0A0Fh)	-	7:0	Default : -
	-	-	Access : -
08h (0A10h)	REG0A10	7:0	Default : 0x00
	TAGC_TAFC_NRZDATA	7	TAGC/TAFC DAC NRZ input data selection. 1: NRZ input data. 0: RZ input data.
	-	6:0	Reserved.
08h (0A11h)	-	7:0	Default : -
	-	-	Access : -
09h (0A12h)	REG0A12	7:0	Default : 0x00
	TAGC_DATAXIN[7:0]	7:0	Access : R/W
09h (0A13h)	REG0A13	7:0	Default : 0x00
	TAGC_DATAXIN[15:8]	7:0	Access : R/W
0Ah ~ 0Ah	-	7:0	See description of '0A12h'.
	-	7:0	Default : -
	-	-	Access : -

ADC_PLL Register (Bank = 0A)				
Index (Absolute)	Mnemonic	Bit	Description	
(0A14h ~ 0A15h)	-	-	Reserved.	
0Bh (0A16h)	REG0A16	7:0	Default : 0x90	Access : R/W
	-	7:5	Reserved.	
	TAGC_POLARITY	4	Tuner AGC polarity control. 1: Positive logic. 0: Negative logic.	
	TAGC_TEST_EN	3	TAGC DAC input test enable. 1: Test mode. 0: Normal mode.	
	-	2:0	Reserved.	
0Bh (0A17h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Ch (0A19h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Dh (0A1Ah)	REG0A1A	7:0	Default : 0x00	Access : RO
	VCOCAL_FAIL	7	VCO bank calibration flag. 1: Fail. 0: Pass.	
	VCTRL_OVER	6	1: VCTRL larger than 2V. 0: VCTRL less than 2V.	
	VCTRL_UNDER	5	1: VCTRL less than 1V. 0: VCTRL larger than 1V.	
	LOCK	4	PLL LOCK detection, 1:LOCKed. 0: UnLOCKed.	
	VIF_PLL_CPINIT	3	Charge pump output open and tied to 1.5V. 1: Charge pump output tied to 1.5V. 0: Normal operation.	
	VIF_VCO_BANK[2:0]	2:0	VCO bank selection. See Table 4.	
0Eh (0A1Dh)	REG0A1D	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	VIF_CAL_FINISH	6	VCO Calibration Finish.	
	VIF_STOPCAL_TUNE	5	LPF calibration finished flag. 1: Finished (disbale LPF tuning circuit clock).	

ADC_PLL Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
			0: Under LPF calibrating.
	VIF_FCODE_OUT[4:0]	4:0	LPF cap bank calibration output code.
0Fh (0A1Eh)	REG0A1E	7:0	Default : 0x00 Access : RO
	VIF_CAL_GAP[7:0]	7:0	VIF VCO Calibration gap.
0Fh (0A1Fh)	REG0A1F	7:0	Default : 0x00 Access : RO
	-	7:2	Reserved.
	VIF_CAL_GAP[9:8]	1:0	See description of '0A1Eh'.
10h (0A20h)	REG0A20	7:0	Default : 0x03 Access : R/W
	-	7:2	Reserved.
	VSYNC_VD_POLARITY	1	It respects to the vsync polarity from VD; 0=low active; 1=high active.
	VSYNC_VD_MASK	0	1=mask vsync from VD.
10h (0A21h)	REG0A21	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	VSYNC_OVERRIDE	0	1=force generating a vsync pulse (gen shot).
11h ~ 14h (0A22h ~ 0A28h)	-	7:0	Default : - Access : -
	-	-	Reserved.
15h (0A2Ah)	REG0A2A	7:0	Default : 0x03 Access : R/W
	VIF_PGA2V_HG	7	Video path PGA2 high gain mode. 0: Low gain mode. 1: High gain mode(flat SAW).
	VIF_PGA2S_HG	6	Sound path PGA2 high gain mode. 0: Low gain mode. 1: High gain mode(flat SAW).
	VIF_PGA1GAINS_SRC	5	Sound path PGA1 control source. 0: By SIF DBB. 1: By VIF DBB(flat SAW).
	VIF_LPFTUNE_XSEL[1:0]	4:3	Crystal options for LPF tuning circuit. (12MHz/20.48MHz/25MHz/28.8MHz).
	VIF_LPFS_BW[2:0]	2:0	Sound path LPF bandwidth control. (3.2M/4.2M/5.2M/16M).
16h (0A2Ch)	REG0A2C	7:0	Default : 0x0E Access : R/W
	-	7:6	Reserved.
	VIF_FCAL_DIV[5:0]	5:0	Filter calibration clock divider(/N, from 2 to 63).

ADC_PLL Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
16h (0A2Dh)	REG0A2D	7:0	Default : 0x12 Access : R/W
	-	7:5	Reserved.
	VIF_TUNEC[4:0]	4:0	Fine tuning filter center frequency.
1Fh ~ 1Fh (0A3Eh ~ 0A3Fh)	-	7:0	Default : - Access : -
	-	-	Reserved.
20h (0A40h)	REG0A40	7:0	Default : 0x3E Access : R/W
	-	7:6	Reserved.
	PWDN_CORE	5	Power down both ADC reference and the associated biases.
	PWDN_ADC1REF	4	Power down ADC1 reference.
	PWDN_ADC0REF	3	Power down ADC0 reference.
	PWDNA1	2	1: Power down ADC1, 0: power on ADC1.
	PWDNA0	1	1: Power down ADC0, 0: power on ADC0.
	-	0	Reserved.
21h ~ 23h (0A42h ~ 0A46h)	-	7:0	Default : - Access : -
	-	-	Reserved.
24h (0A48h)	REG0A48	7:0	Default : 0x80 Access : R/W
	BMA0[4:0]	7:3	ADC0 PGA offset control.
	BP0_SW[2:0]	2:0	ADC0 PGA gain software overwrite control.
24h (0A49h)	REG0A49	7:0	Default : 0x80 Access : R/W
	BMA1[4:0]	7:3	ADC1 PGA offset control.
	BP1_SW[2:0]	2:0	ADC1 PGA gain software overwrite control.
25h (0A4Ah)	-	7:0	Default : - Access : -
	-	-	Reserved.
26h (0A4Ch)	REG0A4C	7:0	Default : 0x00 Access : R/W
	ADCREFO[7:0]	7:0	ADC0 reference adjustment.
26h (0A4Dh)	REG0A4D	7:0	Default : 0x0C Access : R/W
	-	7:4	Reserved.
	ADCREFO[11:8]	3:0	See description of '0A4Ch'.
27h (0A4Eh)	REG0A4E	7:0	Default : 0x00 Access : R/W
	ADCREFO[11:8]	7:0	ADC1 reference adjustment.
27h	REG0A4F	7:0	Default : 0x0C Access : R/W

ADC_PLL Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
(0A4Fh)	-	7:4	Reserved.
	ADCREF1[11:8]	3:0	See description of '0A4Eh'.
28h ~ 2Dh (0A50h ~ 0A5Bh)	-	7:0	Default : - Access : -
	-	-	Reserved.
2Eh (0A5Ch)	REG0A5C	7:0	Default : 0x01 Access : R/W
	-	7:3	Reserved.
	ADCIN_O_FIFO_BYPASS	2	[Digital] 1: bypass ADC0 sync fifo in SSIF mode.
	ADCIN_I_FIFO_BYPASS	1	[Digital] 1: bypass ADC0 sync fifo in CVBS mode.
	ADCIN_SIGN	0	[Digital] 0: for ADC out is unsigned 1: for ADC out is signed.
2Eh ~ 2Fh (0A5Dh ~ 0A5Eh)	-	7:0	Default : - Access : -
	-	-	Reserved.
30h (0A60h)	REG0A60	7:0	Default : 0xE0 Access : R/W
	GC_MPLL_ICTRL[2:0]	7:5	Charge pump current control register; 000:2.6uA; 001:5.2uA; 010:7.7uA; 011:10.3uA; 100:13uA; 101:15.5uA; 110:20.6uA; 111:41.2uA.
	-	4:3	Reserved.
	GC_MPLL_ADCLKSEL[2:0]	2:0	CLKRO_ADCCLK_HV selection, 000/DIV10; 001/DIV19; 010/DIV24; 011/DIV25; 1xx/XTAL.
31h (0A62h)	REG0A62	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	GC_MPLL_INDIV1ST[1:0]	1:0	First input divider register control 00:/1; 01:/2; 10:/4, 11:/8.
31h (0A63h)	REG0A63	7:0	Default : 0x00 Access : R/W
	GC_MPLL_INDIV2ND[7:0]	7:0	Second input divider register control, d0:/1, d1:/1, d2:/2, d3:/3, & d255/255.
32h (0A64h)	REG0A64	7:0	Default : 0x01 Access : R/W
	-	7:2	Reserved.
	GC_MPLL_LOOPDIV1ST[1:0]	1:0	First loop divider register control 00:/1; 01:/2; 10:/4, 11:/8; XTALI*loopdiv1st*loopdiv2nd=28.8*2*15=864MHz.
32h (0A65h)	REG0A65	7:0	Default : 0x0F Access : R/W
	GC_MPLL_LOOPDIV2ND[7:0]	7:0	Second loop divider register control, d0:/1, d1:/1, d2:/2, d3:/3, & d255/255. XTALI*loopdiv1st*loopdiv2nd=28.8*2*15=864MHz.

ADC_PLL Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
33h (0A66h)	REG0A66	7:0	Default : 0x02 Access : R/W
	-	7:2	Reserved.
	GC_MPLL_OUTDIV1ST[1:0]	1:0	First output divider register control 00:/1; 01:/2; 10:/4, 11:/8.
33h (0A67h)	REG0A67	7:0	Default : 0x00 Access : R/W
	GC_MPLL_OUTDIV2ND[7:0]	7:0	Second output divider register control, d0:/1, d1:/1, d2:/2, d3:/3, & d255/255.
34h (0A68h)	REG0A68	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	GC_XTALVIF_ENDIV2	3	Enable XTAL clock to VIF divider by 2.
	GC_MPLL_VCOOFFSET	2	Enable VCO free running; (Low active).
	GC_MPLL_RESET	1	Reset all flip-flops of input PLL.
	GC_MPLL_PORST	0	Power on reset signal to discharge loop filter voltage (High active).
35h (0A6Ah)	REG0A6A	7:0	Default : 0x84 Access : R/W
	PD_MPLL_USB_CLK	7	Power down USB clk divider (high active).
	PD_MPLL_DVB_DIV7	6	Power down MPLL_DVB_DIV7 clock (high active).
	PD_MPLL_DVB_DIV5	5	Power down MPLL_DVB_DIV5 clock (high active).
	PD_MPLL_DVB_DIV3P5	4	Power down MPLL_DVB_DIV3P5 clock (high active).
	PD_MPLL_DVB_DIV3	3	Power down MPLL_DVB_DIV3 clock (high active).
	PD_MPLL_DVB_DIV2	2	Power down MPLL_DVB_DIV2 clock (high active).
	PD_MPLL_ADCDIV	1	Power down the dividers for ADC clock (high active).
	PD_MPLLIN	0	Power down control of input PLL (high active).
36h ~ 3Fh (0A6Ch ~ 0A7Fh)	-	7:0	Default : - Access : -
	-	-	Reserved.
40h (0A80h)	REG0A80	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	GAIN1_OREN	5	ADD1 ADC GAIN software overwrite enable.
	GAIN0_OREN	4	ADD0 ADC GAIN software overwrite enable.
	AGAIN1_SW	3	ADD1 ADC GAIN software overwrite:. 0: Normal 1: add numerator of gain.
	AGAIN0_SW	2	ADC0 GAIN software overwrite:. 0: Normal 1: add numerator of gain.

ADC_PLL Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
	ACLK_SEL	1	ADC1 clock source select: 0: From MPLL 1: from ATOP.
	VCLK_SEL	0	ADC0 clock source select: 0: From MPLL 1: from ATOP.
41h (0A82h)	REG0A82	7:0	Default : 0x01
	SIF_AGC_GAIN_OV[3:0]	7:4	SIF AGC gain overwrite value.
	-	3:2	Reserved.
	SIF_AGC_GAIN_OREN	1	SIF AGC gain overwrite enable.
	SIF_AGC_PD	0	SIF AGC power down control.
41h (0A83h)	REG0A83	7:0	Default : 0x00
	SIF_AGC_TST[7:0]	7:0	SIF AGC test control.
42h (0A84h)	REG0A84	7:0	Default : 0x02
	-	7:3	Reserved.
	SIFCLP_SEL[2:0]	2:0	SIF / ATSC pad 's clamp. <2:0> configure SIF / ATSC path 's clamp. 000: No clamp. 001: Middle impedance clamp. 010: High impedance clamp. 011: No clamp. 1XX: No clamp.
43h (0A86h)	REG0A86	7:0	Default : 0x00
	GC_MPLL_DVB DIV5_END DIV8	7	Set mpll_dvb_div5 divider ratio DVB5. 0: DVB5 = 5. 1: DVB5 = 4.
	GC_MPLL_DVB DIV3_END DIV5	6	Set mpll_dvb_div3 divider ratio DVB3. 0: DVB3 = 3. 1: DVB3 = 2.5.
	GC_MPLL_CLK DIV_END DIV4	5	Set mpll_clk_div output divider ratio. 0: See gc_mpll_sel_div. 1: DIVSEL = 2 (1st priority).
	GC_MPLL_ENZ_CK DVB DIV2	4	Set DVB, MCU, DIV input clock = VCO/1 or VCO/2. 0: VCO/2. 1: VCO/1.
	GC_MPLL_MCU SEL[2:0]	3:1	Set mpll_mcu_clk_out. 000 MCUSEL = 4. 001 MCUSEL = 5.

ADC_PLL Register (Bank = 0A)

Index (Absolute)	Mnemonic	Bit	Description
			010 MCUSEL = 6. 011 MCUSEL = 7. 100 MCUSEL = 8. 101 MCUSEL = 16. else: Gated.
	GC_MPLL_SEL_DIV	0	Set mpll_clk_div output divider ratio. 0: DIVSEL = 3. 1: DIVSEL = 2.5.

PM_DDC Register (Bank = 0B)

PM_DDC Register (Bank = 0B)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (0B00h)	REG0B00	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	D2B_EN_D1	3	DDC2Bi enable for DVI_1. 0: Disable. 1: Enable.	
	D2B_EN_D0	2	DDC2Bi enable for DVI_0. 0: Disable. 1: Enable.	
	D2B_EN_A1	1	DDC2Bi enable for ADC_1. 0: Disable. 1: Enable.	
	D2B_EN_A0	0	DDC2Bi enable for ADC_0. 0: Disable. 1: Enable.	
00h (0B01h)	REG0B01	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DDC_EN_D1	3	DDC function enable for DVI_1. 0: Disable. 1: Enable.	
	DDC_EN_D0	2	DDC function enable for DVI_0. 0: Disable. 1: Enable.	
	DDC_EN_A1	1	DDC function enable for ADC_1. 0: Disable. 1: Enable.	
	DDC_EN_A0	0	DDC function enable for ADC_0. 0: Disable. 1: Enable.	
01h (0B02h)	REG0B02	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SLEW_SEL[1:0]	5:4	Slew Rate Control. 00: Bypass. 01: Drive 1 cycle. 10: Drive 2 cycles. 11: Drive 3 cycles.	
	PMDDC_FORCE_SEL	3	Force sel pmddc as edid read path.	

PM_DDC Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description
	A0_WKUP_EN	2	A0 wake up function enable. 0: Disable. 1: Enable.
	FILTER_ON	1	DDC Filter. 0: Disable. 1: Enable.
	FILTER_MSB	0	DDC Filter Msb.
01h (0B03h)	-	7:0	Default : - Access : -
	-	-	Reserved.
02h (0B04h)	REG0B04	7:0	Default : 0x00 Access : RO, R/W
	-	7:4	Reserved.
	D2B_MCCS_WKUP_FLAG_D0	3	PM_DDC2Bi MCCS wakeup flag for DVI_0. 0: No wakeup event occurred. 1: Wakeup event occurred.
	D2B_MCCS_CHKSUM_ERR_D0	2	PM_DDC2Bi MCCS wakeup check sum value error flag for DVI_0. 0: Check sum value is correct. 1: Check sum value error.
	D2B_MCCS_WKUP_FLAG_A0	1	PM_DDC2Bi MCCS wakeup flag for ADC_0. 0: No wakeup event occurred. 1: Wakeup event occurred.
	D2B_MCCS_CHKSUM_ERR_A0	0	PM_DDC2Bi MCCS wakeup check sum value error flag for ADC_0. 0: Check sum value is correct. 1: Check sum value error.
02h (0B05h)	-	7:0	Default : - Access : -
	-	-	Reserved.
03h (0B06h)	REG0B06	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	MCCS_WKUP_EN_D0	1	PM_DDC2Bi MCCS wakeup enable of DVI_0. 0: Disable. 1: Enable.
	MCCS_WKUP_EN_A0	0	PM_DDC2Bi MCCS wakeup enable of ADC_0. 0: Disable. 1: Enable.
03h	-	7:0	Default : - Access : -

PM_DDC Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description
(0B07h)	-	-	Reserved.
04h (0B08h)	REG0B08	7:0	Default : 0x00 Access : WO
	MCCS_WKUP_CLR_D0	7	PM_DDC2Bi MCCS wakeup clear for DVI_0. 1: Clear (write one clear, no need to toggle this bit). 0: No action.
	MCCS_WKUP_FLAG_CLR_D0	6	PM_DDC2Bi MCCS wakeup flag clear for DVI_0. 1: Clear (write one clear, no need to toggle this bit). 0: No action.
	MCCS_CHKSUM_CLR_D0	5	PM_DDC2Bi MCCS check sum flag clear for DVI_0. 1: Clear (write one clear, no need to toggle this bit). 0: No action.
	MCCS_PWRKEY_CLR_D0	4	PM_DDC2Bi MCCS wakeup power key status clear for DVI_0. 1: Clear (write one clear, no need to toggle this bit). 0: No action.
	MCCS_WKUP_CLR_A0	3	PM_DDC2Bi MCCS wakeup clear for ADC_0. 1: Clear (write one clear, no need to toggle this bit). 0: No action.
	MCCS_WKUP_FLAG_CLR_A0	2	PM_DDC2Bi MCCS wakeup flag clear for ADC_0. 1: Clear (write one clear, no need to toggle this bit). 0: No action.
	MCCS_CHKSUM_CLR_A0	1	PM_DDC2Bi MCCS check sum flag clear for ADC_0. 1: Clear (write one clear, no need to toggle this bit). 0: No action.
	MCCS_PWRKEY_CLR_A0	0	PM_DDC2Bi MCCS wakeup power key status clear for ADC_0. 1: Clear (write one clear, no need to toggle this bit). 0: No action.
04h (0B09h)	-	7:0	Default : - Access : -
	-	-	Reserved.
05h (0B0Ah)	REG0B0A	7:0	Default : 0x00 Access : RO
	MCCS_PWR_KEY_A0[7:0]	7:0	PM_DDC2Bi MCCS wakeup power key value of ADC_0.
05h (0B0Bh)	REG0B0B	7:0	Default : 0x00 Access : RO
	MCCS_PWR_KEY_D0[7:0]	7:0	PM_DDC2Bi MCCS wakeup power key value of DVI_0.
06h (0B0Ch)	REG0B0C	7:0	Default : 0x00 Access : RO
	-	7:6	Reserved.

PM_DDC Register (Bank = 0B)

Index (Absolute)	Mnemonic	Bit	Description
	INT_FINAL_STATUS[5:0]	5:0	[5:1] reserved. [0] A0_interrupt.
06h (0B0Dh)	REG0B0D	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	INT_MASK[5:0]	5:0	[5:1] reserved. [0] A0_interrupt_mask.
07h (0B0Eh)	REG0B0E	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	INT_FORCE[5:0]	5:0	Force the int_final_status to 1. By setting each of the related bit to 1.
07h (0B0Fh)	REG0B0F	7:0	Default : 0x00 Access : WO
	-	7:6	Reserved.
	INT_CLR[5:0]	5:0	Clear the int_final_status to 0. By setting each of the related bit to 1.
08h (0B10h)	REG0B10	7:0	Default : 0x80 Access : R/W
	RSTZ_SW_DDC	7	Software resetz for DDC (low active).
	-	6:0	Reserved.
09h ~ 07h (0B13h ~ 0B19h)	-	7:0	Default : - Access : -
	-	-	Reserved.

MCU Register (Bank = 10)

MCU Register (Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1000h)	REG1000	7:0	Default : 0x01	Access : R/W
	SRAM_START_ADDR_1[7:0]	7:0	SRAM Start Address[23:16].	
00h (1001h)	REG1001	7:0	Default : 0x00	Access : R/W
	SRAM_START_ADDR_1[15:8]	7:0	See description of '1000h'.	
01h (1002h)	REG1002	7:0	Default : 0x01	Access : R/W
	SRAM_END_ADDR_1[7:0]	7:0	SRAM End Address[23:16].	
01h (1003h)	REG1003	7:0	Default : 0x00	Access : R/W
	SRAM_END_ADDR_1[15:8]	7:0	See description of '1002h'.	
02h (1004h)	REG1004	7:0	Default : 0x00	Access : R/W
	SRAM_START_ADDR_0[7:0]	7:0	SRAM End Address[15:0].	
02h (1005h)	REG1005	7:0	Default : 0x00	Access : R/W
	SRAM_START_ADDR_0[15:8]	7:0	See description of '1004h'.	
03h (1006h)	REG1006	7:0	Default : 0x00	Access : R/W
	SRAM_END_ADDR_0[7:0]	7:0	SRAM End Address[15:0].	
03h (1007h)	REG1007	7:0	Default : 0x80	Access : R/W
	SRAM_END_ADDR_0[15:8]	7:0	See description of '1006h'.	
04h (1008h)	REG1008	7:0	Default : 0x01	Access : R/W
	DRAM_START_ADDR_1[7:0]	7:0	DRAM Start Address[23:16].	
04h (1009h)	REG1009	7:0	Default : 0x00	Access : R/W
	DRAM_START_ADDR_1[15:8]	7:0	See description of '1008h'.	
05h (100Ah)	REG100A	7:0	Default : 0x0F	Access : R/W
	DRAM_END_ADDR_1[7:0]	7:0	DRAM End Address[23:16].	
05h (100Bh)	REG100B	7:0	Default : 0x00	Access : R/W
	DRAM_END_ADDR_1[15:8]	7:0	See description of '100Ah'.	
06h (100Ch)	REG100C	7:0	Default : 0x00	Access : R/W
	DRAM_START_ADDR_0[7:0]	7:0	DRAM Start Address[15:0].	
06h (100Dh)	REG100D	7:0	Default : 0x80	Access : R/W
	DRAM_START_ADDR_0[15:8]	7:0	See description of '100Ch'.	
07h (100Eh)	REG100E	7:0	Default : 0xFF	Access : R/W
	DRAM_END_ADDR_0[7:0]	7:0	DRAM End Address[15:0].	
07h (100Fh)	REG100F	7:0	Default : 0xFF	Access : R/W
	DRAM_END_ADDR_0[15:8]	7:0	See description of '100Eh'.	

MCU Register (Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
08h (1010h)	REG1010	7:0	Default : 0x00	Access : R/W
	SPI_START_ADDR_1[7:0]	7:0	SPI Start Address[23:16].	
08h (1011h)	REG1011	7:0	Default : 0x00	Access : R/W
	SPI_START_ADDR_1[15:8]	7:0	See description of '1010h'.	
09h (1012h)	REG1012	7:0	Default : 0x00	Access : R/W
	SPI_END_ADDR_1[7:0]	7:0	SPI End Address[23:16].	
09h (1013h)	REG1013	7:0	Default : 0x00	Access : R/W
	SPI_END_ADDR_1[15:8]	7:0	See description of '1012h'.	
0Ah (1014h)	REG1014	7:0	Default : 0x00	Access : R/W
	SPI_START_ADDR_0[7:0]	7:0	SPI Start Address[15:0].	
0Ah (1015h)	REG1015	7:0	Default : 0x00	Access : R/W
	SPI_START_ADDR_0[15:8]	7:0	See description of '1014h'.	
0Bh (1016h)	REG1016	7:0	Default : 0xFF	Access : R/W
	SPI_END_ADDR_0[7:0]	7:0	SPI End Address[15:0].	
0Bh (1017h)	REG1017	7:0	Default : 0xFF	Access : R/W
	SPI_END_ADDR_0[15:8]	7:0	See description of '1016h'.	
0Ch (1018h)	REG1018	7:0	Default : 0x02	Access : R/W
	MCU_BANK_USE_XFR	7	Use XFR to switch bank.	
	TEST_SEL[2:0]	6:4	Test bus selection.	
	ICACHE_RSTZ	3	Icache enable.	
	DRAM_EN	2	DRAM enable.	
	SPI_EN	1	SPI enable.	
	SRAM_EN	0	SRAM enable.	
0Ch (1019h)	REG1019	7:0	Default : 0x00	Access : R/W
	MCU_BANK_XFR[7:0]	7:0	XFR bank (64KB).	
0Dh (101Ah)	REG101A	7:0	Default : 0x00	Access : R/W
	TWA[7:0]	7:0	TWA for RIU bridge.	
0Dh (101Bh)	REG101B	7:0	Default : 0x00	Access : R/W
	TAW[7:0]	7:0	TAW for RIU bridge.	
20h (1040h)	REG1040	7:0	Default : 0x00	Access : R/W
	P0_OV[7:0]	7:0	P0 override by P0_REG. 0: Disable. 1: Enable.	

MCU Register (Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
20h (1041h)	REG1041	7:0	Default : 0x00	Access : R/W
	P0_REG[7:0]	7:0	Data to override P0.	
21h (1042h)	REG1042	7:0	Default : 0x00	Access : R/W
	P1_OV[7:0]	7:0	P1 override by P1_REG. 0: Disable. 1: Enable.	
21h (1043h)	REG1043	7:0	Default : 0x00	Access : R/W
	P1_REG[7:0]	7:0	Data to override P1.	
22h (1044h)	REG1044	7:0	Default : 0x00	Access : R/W
	P2_OV[7:0]	7:0	P2 override by P2_REG. 0: Disable. 1: Enable.	
22h (1045h)	REG1045	7:0	Default : 0x00	Access : R/W
	P2_REG[7:0]	7:0	Data to override P2.	
23h (1046h)	REG1046	7:0	Default : 0x00	Access : R/W
	P3_OV[7:0]	7:0	P3 override by P3_REG. 0: Disable. 1: Enable.	
23h (1047h)	REG1047	7:0	Default : 0x00	Access : R/W
	P3_REG[7:0]	7:0	Data to override P3.	
24h (1048h)	REG1048	7:0	Default : 0x00	Access : R/W
	P0_CTRL[7:0]	7:0	MCU Port 0 output enable control.	
25h (104Ah)	REG104A	7:0	Default : 0x00	Access : R/W
	P0_OE[7:0]	7:0	MCU Port 0 output enable.	
26h (104Ch)	REG104C	7:0	Default : 0x00	Access : R/W
	P0_IN[7:0]	7:0	MCU Port 0 output enable from output data.	
27h (104Eh)	REG104E	7:0	Default : 0x00	Access : R/W
	P1_CTRL[7:0]	7:0	MCU Port 1 output enable control.	
28h (1050h)	REG1050	7:0	Default : 0x00	Access : R/W
	P1_OE[7:0]	7:0	MCU Port 1 output enable.	
29h (1052h)	REG1052	7:0	Default : 0x00	Access : R/W
	P1_IN[7:0]	7:0	MCU Port 1 output enable from output data.	
2Ah (1054h)	REG1054	7:0	Default : 0x00	Access : R/W
	P2_CTRL[7:0]	7:0	MCU Port 2 output enable control.	

MCU Register (Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
2Bh (1056h)	REG1056	7:0	Default : 0x00
	P2_OE[7:0]	7:0	MCU Port 2 output enable.
2Ch (1058h)	REG1058	7:0	Default : 0x00
	P2_IN[7:0]	7:0	MCU Port 2 output enable from output data.
2Dh (105Ah)	REG105A	7:0	Default : 0x00
	P3_CTRL[7:0]	7:0	MCU Port 3 output enable control.
2Eh (105Ch)	REG105C	7:0	Default : 0x00
	P3_OE[7:0]	7:0	MCU Port 3 output enable.
2Fh (105Eh)	REG105E	7:0	Default : 0x00
	P3_IN[7:0]	7:0	MCU Port 3 output enable from output data.
40h (1080h)	REG1080	7:0	Default : 0x55
	RESET_CPU0[7:0]	7:0	Reset CPU 0.
40h (1081h)	REG1081	7:0	Default : 0xAA
	RESET_CPU0[15:8]	7:0	See description of '1080h'.
41h (1082h)	REG1082	7:0	Default : 0x55
	RESET_CPU1[7:0]	7:0	Reset CPU 1.
41h (1083h)	REG1083	7:0	Default : 0xAA
	RESET_CPU1[15:8]	7:0	See description of '1082h'.
42h (1084h)	REG1084	7:0	Default : 0x00
	SW_RESET_CPU0[7:0]	7:0	S/W reset CPU 0 (8051).
42h (1085h)	REG1085	7:0	Default : 0x00
	SW_RESET_CPU0[15:8]	7:0	See description of '1084h'.
43h (1086h)	REG1086	7:0	Default : 0x00
	SW_RESET_CPU1[7:0]	7:0	S/W reset CPU 1 (32-bit MCU).
43h (1087h)	REG1087	7:0	Default : 0x00
	SW_RESET_CPU1[15:8]	7:0	See description of '1086h'.
58h (10B0h)	REG10B0	7:0	Default : 0x00
	IB_ADDR0[7:0]	7:0	HK MCU program counter.
58h (10B1h)	REG10B1	7:0	Default : 0x00
	IB_ADDR0[15:8]	7:0	See description of '10B0h'.
59h (10B2h)	REG10B2	7:0	Default : 0x00
	IB_ADDR0[23:16]	7:0	See description of '10B0h'.
59h	REG10B3	7:0	Default : 0x00

MCU Register (Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
(10B3h)	IB_DATAI0[7:0]	7:0	HK MCU inst return data.	
5Ah	REG10B4	7:0	Default : 0x00	Access : RO
(10B4h)	IB_ADDR1[7:0]	7:0	VD MCU program counter.	
5Ah	REG10B5	7:0	Default : 0x00	Access : RO
(10B5h)	IB_ADDR1[15:8]	7:0	See description of '10B4h'.	
5Bh	REG10B6	7:0	Default : 0x00	Access : RO
(10B6h)	IB_ADDR1[23:16]	7:0	See description of '10B4h'.	
5Bh	REG10B7	7:0	Default : 0x00	Access : RO
(10B7h)	IB_DATAI1[7:0]	7:0	VD MCU inst return data.	
5Ch	REG10B8	7:0	Default : 0x00	Access : RO
(10B8h)	IB_ADDR2[7:0]	7:0	TT MCU program counter.	
5Ch	REG10B9	7:0	Default : 0x00	Access : RO
(10B9h)	IB_ADDR2[15:8]	7:0	See description of '10B8h'.	
5Dh	REG10BA	7:0	Default : 0x00	Access : RO
(10BAh)	IB_ADDR2[23:16]	7:0	See description of '10B8h'.	
5Dh	REG10BB	7:0	Default : 0x00	Access : RO
(10BBh)	IB_DATAI2[7:0]	7:0	TT MCU inst return data.	
70h	REG10E0	7:0	Default : 0x00	Access : R/W
(10E0h)	XB_ERAM_LB[7:0]	7:0	ERAM map HK XDATA low boundary (unit: 1k). Recommended setting: 0x14.	
70h	REG10E1	7:0	Default : 0x00	Access : R/W
(10E1h)	XB_ERAM_HB[7:0]	7:0	ERAM map HK XDATA high boundary (unit: 1k). Recommended setting: 0x14.	
72h	REG10E4	7:0	Default : 0x00	Access : R/W
(10E4h)	XD2ERAM_ADRH[7:0]	7:0	ERAM base address (unit: 1k, 0x000-0x3FF).	
73h	REG10E6	7:0	Default : 0x00	Access : R/W
(10E6h)	-	7:1	Reserved.	
	XD2ERAM_EN	0	Enable ERAM mapping.	

MIU Register (Bank = 12)

MIU Register (Bank = 12)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1200h)	REG1200	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	NO_RQ_CTRL_EN	2	1: Enable MIU to keep servicing the timeouted client when there is no other requests to MIU.	
	ARBITER_OFF	1	Mask all clients' requests.	
	INIT_MIU	0	Issue initial DRAM cycle.	
00h (1201h)	REG1201	7:0	Default : 0x00	Access : RO, R/W
	INIT_DONE	7	DRAM has been initialized.	
	-	6	Reserved.	
	TRIG_DEEP_PD	5	Trigger DRAM into deep power down mode.	
	-	4:3	Reserved.	
	TRIG_REFRESH	2	Trigger one refresh command.	
	TRIG_PRECHARGE	1	Trigger one precharge all command.	
	SINGLE_STEP_ON	0	Turn on single step command mode.	
01h (1202h)	REG1202	7:0	Default : 0x00	Access : R/W
	DRAM_TYPE[1:0]	7:6	01: DDR2. 11: DDR.	
	DRAM_BUS[1:0]	5:4	Select external DRAM bus. 00: X16. 01: X32.	
	DYNAMIC_CK_ODT	3	Turn on DRAM clock and ODT only when there are DRAM accesses.	
	DYNAMIC_CKE	2	Turn on CKE only when there are DRAM accesses.	
	SELF_REFRESH	1	Enter/exit self refresh mode.	
	CKE	0	Enable CKE.	
01h (1203h)	REG1203	7:0	Default : 0x70	Access : R/W
	CS_Z	7	DRAM chip select, active low.	
	ADR_OENZ	6	Address output enable, active low.	
	DQ_OENZ	5	Data output enable, active low.	
	CKE_OENZ	4	CKE output enable, active low.	
	8BA	3	DRAM bank select. 0: 2/4 banks. 1: 8 banks.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
	COL_SIZE[1:0]	2:1	DRAM column bits select. 00: 8 bits. 01: 9 bits. 10: 10 bits.
	4BA	0	DRAM bank select. 0: 2 banks. 1: 4 banks.
02h (1204h)	REG1204	7:0	Default : 0x40 Access : R/W
	RD_TIMING[3:0]	7:4	Select read back data delay timing.
	ODT	3	Turn on ODT function.
	FORCE_DDR_RD_ACT	2	Force the access status to read, for analog design reference.
	RD_MCK_SEL	1	Select the source of read data from DRAM. 1: From DQ pad C pin. 0: Data latched by feedback clock.
	RD_IN_PHASE	0	1: Select read data strobed by negative edge of CLK. 0: Select read data strobed by positive edge of CLK.
02h (1205h)	REG1205	7:0	Default : 0x03 Access : R/W
	-	7:4	Reserved.
	4X_MODE	3	4X mode for DDR2 800 MHz.
	CAS_LATENCY[2:0]	2:0	CAS latency.
03h (1206h)	REG1206	7:0	Default : 0x08 Access : R/W
	TREFPERIOD[7:0]	7:0	Refresh cycle period, unit is 16 MCLKs.
03h (1207h)	REG1207	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	PRIORITY_SW	6	1: Group 1 priority > Group 0 priority. 0: Group 0 priority > Group 1 priority.
	-	5:4	Reserved.
	DRAM_SIZE[3:0]	3:0	Limited maximum DRAM access size. 0000: No limit. 0001: 2MB. 0010: 4MB. 0011: 8MB. 0100: 16MB. 0101: 32MB. 0110: 64MB.

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
04h (1208h)	REG1208	7:0	Default : 0xC8 Access : R/W
	TRC[3:0]	7:4	DRAM TRC timing.
	TRAS[3:0]	3:0	DRAM TRAS timing.
04h (1209h)	REG1209	7:0	Default : 0x33 Access : R/W
	TRP[3:0]	7:4	DRAM TRP timing.
	TRCD[3:0]	3:0	DRAM TRCD timing.
05h (120Ah)	REG120A	7:0	Default : 0x62 Access : R/W
	TWR[3:0]	7:4	DRAM TWR timing.
	TRRD[3:0]	3:0	DRAM TRRD timing.
05h (120Bh)	REG120B	7:0	Default : 0x12 Access : R/W
	TRTP[3:0]	7:4	DRAM TRTP timing, read to precharge time.
	TMRD[3:0]	3:0	DRAM TMRD timing.
06h (120Ch)	REG120C	7:0	Default : 0x63 Access : R/W
	W2R_OEN_DLY[3:0]	7:4	W2R_DLY + 3.
	W2R_DLY[3:0]	3:0	DRAM write to read delay.
06h (120Dh)	REG120D	7:0	Default : 0x86 Access : R/W
	R2W_OEN_DLY[3:0]	7:4	R2W_DLY + 2.
	R2W_DLY[3:0]	3:0	DRAM read to write delay.
07h (120Eh)	REG120E	7:0	Default : 0x0E Access : R/W
	TRC_4	7	DRAM tRC timing bit 4.
	TRAS_4	6	DRAM tRAS timing bit 4.
07h (120Fh)	REG120F	7:0	Default : 0x41 Access : R/W
	TCCD[1:0]	7:6	1: DDR. 2: DDR2.
	-	5:3	Reserved.
08h (1210h)	REG1210	7:0	Default : 0x00 Access : R/W
	DEB_SEL[7:0]	7:0	Select debug result.
	DEB_SEL[15:8]	7:0	See description of '1210h'.
09h (1212h)	REG1212	7:0	Default : 0x00 Access : RO
	DEB_BUS[7:0]	7:0	Debug port.

MIU Register (Bank = 12)				
Index (Absolute)	Mnemonic	Bit	Description	
09h (1213h)	REG1213	7:0	Default : 0x00	Access : RO
	DEB_BUS[15:8]	7:0	See description of '1212h'.	
0Ah (1214h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Ah (1215h)	REG1215	7:0	Default : 0x10	Access : R/W
	RESET_DLL	7	Reset DLL of DDR.	
	-	6:0	Reserved.	
0Bh ~ 0Eh (1216h ~ 121Ch)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Eh (121Dh)	REG121D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	MIU_SEL_PROTECT_SW	2	MIU0 or MIU1 select function is protected by software setting.	
	MIU_SEL_PROTECT_HW	1	MIU0 or MIU1 select function is protected by hardware (qualified by DRAM initialization done).	
	MIU_SEL_PROTECT_EN	0	Enable the protect function for selection of MIU0 or MIU1.	
0Fh (121Eh)	REG121E	7:0	Default : 0x00	Access : R/W
	SW_RST_G3	7	Software reset for group 3.	
	SW_RST_G2	6	Software reset for group 2.	
	SW_RST_G1	5	Software reset for group 1.	
	SW_RST_G0	4	Software reset for group 0.	
	-	3:2	Reserved.	
	DFT_ADRMD	1	DFT address mode.	
	SW_RST_MIU	0	Software reset.	
0Fh (121Fh)	REG121F	7:0	Default : 0x0C	Access : R/W
	-	7:5	Reserved.	
	SYNC_OUT_THRESHOLD[4:0]	4:0	Sync output FIFO full threshold.	
10h (1220h)	REG1220	7:0	Default : 0x09	Access : R/W
	DDFSET[3:0]	7:4	Set the clock frequency for DRAM.	
	DDRIP[1:0]	3:2	DDR clock generator charge pump current.	
	DDRRP[1:0]	1:0	DDR clock generator loop filter resistor.	
10h (1221h)	REG1221	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	DDFSET[9:4]	5:0	See description of '1220h'.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
11h (1222h)	REG1222	7:0	Default : 0x00 Access : R/W
	DDFSPAN[7:0]	7:0	DDR clock spread spectrum period.
11h (1223h)	REG1223	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	ENFRUNZ	4	VCO free run disable frequency.
	-	3:2	Reserved.
	DDFSPAN[9:8]	1:0	See description of '1222h'.
12h (1224h)	REG1224	7:0	Default : 0x00 Access : R/W
	DDFSTEP[7:0]	7:0	DDR clock spread spectrum step.
12h (1225h)	REG1225	7:0	Default : 0x40 Access : R/W
	DDRPLL_LOOP_DIV_FIRST[1:0]	7:6	Set the clock frequency for DRAM.
	DDRPLL_INPUT_DIV_FIRST[1:0]	5:4	Set the clock frequency for DRAM.
	DDRPLL_RESET	3	DDR PLL reset.
	DDRPLL_PORST	2	DDR PLL power-on reset.
	DDRPLL_PD	1	DDR PLL power down.
	DDR_SSC_EN	0	Spread Spectrum Enable.
13h (1226h)	REG1226	7:0	Default : 0x00 Access : R/W
	DDRPLL_INPUT_DIV_SECOND[7:0]	7:0	Set the clock frequency for DRAM.
13h (1227h)	REG1227	7:0	Default : 0x00 Access : R/W
	DDRPLL_LOOP_DIV_SECOND[7:0]	7:0	Set the clock frequency for DRAM.
14h ~ 14h (1228h ~ 1229h)	-	7:0	Default : - Access : -
	-	-	Reserved.
18h (1230h)	REG1230	7:0	Default : 0x00 Access : R/W
	DQSPH1[3:0]	7:4	For group 1 DQS phase.
	DQSPH0[3:0]	3:0	For group 0 DQS phase.
18h (1231h)	REG1231	7:0	Default : 0x00 Access : R/W
	DQSPH3[3:0]	7:4	For group 3 DQS phase.
	DQSPH2[3:0]	3:0	For group 2 DQS phase.
19h (1232h)	REG1232	7:0	Default : 0x00 Access : R/W
	DQSPH5[3:0]	7:4	For group 5 DQS phase.
	DQSPH4[3:0]	3:0	For group 4 DQS phase.
19h (1233h)	REG1233	7:0	Default : 0x00 Access : R/W
	DQSPH7[3:0]	7:4	For group 7 DQS phase.

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
	DQSPH6[3:0]	3:0	For group 6 DQS phase.
1Ah (1234h)	REG1234	7:0	Default : 0x00 Access : R/W
	DDR2_DQS_OEN_MASK[7:0]	7:0	Mask DDR2 DQS OENZ.
1Ah (1235h)	REG1235	7:0	Default : 0x00 Access : R/W
	DQS_OEN_MASK[7:0]	7:0	Mask DQS OENZ.
1Bh (1236h)	REG1236	7:0	Default : 0x60 Access : R/W
	CLK_DRV[2:0]	7:5	DRAM clock pad driving strength select.
	DDR_CLK_SWITCH[1:0]	4:3	Digital and analog MIU clock phase select.
	CLKPH[2:0]	2:0	Output clock to DRAM phase select.
1Bh (1237h)	REG1237	7:0	Default : 0x00 Access : R/W
	MD_DRV[1:0]	7:6	DRAM data pad driving strength select.
	ADR_DRV[1:0]	5:4	DRAM address pad driving strength select.
	DM_DRV[1:0]	3:2	DRAM DM pad driving strength select.
	-	1:0	Reserved.
1Ch (1238h)	REG1238	7:0	Default : 0x00 Access : R/W
	FB_CLK_SEL	7	Select feedback MCLK or CLK1XA0N to latch read data from DRAM.
	CLKPH1[2:0]	6:4	Select the clock phase for latching the read ESDR_DQ.
	-	3:2	Reserved.
	FORCE_D2A_FIFO_EN	1	Force d2A FIFO enable.
	FORCE_CKE_IN	0	Force cke in.
1Dh (123Ah)	REG123A	7:0	Default : 0x00 Access : R/W
	DDR2_CPL_EN	7	For analog logic use.
	REC_ENDF	6	For analog logic use.
	DDRIO_ODT[1:0]	5:4	DDR I/O ODT enable.
	TRGR_LVL[3:0]	3:0	Pad trigger level selection.
1Dh (123Bh)	REG123B	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	ANA_BIST_EN	1	Read speed BIST enable.
	DQSIN_TDLY_SW	0	DDR2/DDR DQS after delay string test output selection.
1Eh (123Ch)	REG123C	7:0	Default : 0x00 Access : R/W
	VRING_EN[3:0]	7:4	For analog logic use.
	DQ_DLY[1:0]	3:2	For analog logic use.

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
	CMD_DLY[1:0]	1:0	For analog logic use.
1Eh (123Dh)	REG123D	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MI_DRV_CAL_PD	6	For analog driving calibration use.
	MI_DRV_CAL_S[1:0]	5:4	For analog driving calibration use.
	MI_DRV_CAL_PN_SEL	3	For analog driving calibration use.
	MI_DRV_CAL_TEST[2:0]	2:0	For analog driving calibration use.
20h (1240h)	REG1240	7:0	Default : 0x00 Access : R/W
	RQ0_BA_MERGE_EN	7	Group 0 unexpected bank access mask.
	RQ0_RW_MERGE_EN	6	Group 0 unexpected read/write access mask.
	RQ0_GROUP_DEADLINE_EN	5	Group 0 deadline enable.
	RQ0_TIMEOUT_EN	4	Group 0 time out enable.
	RQ0_GROUP_LIMIT_EN	3	Group 0 group limit enable.
	RQ0_MEMBER_LIMIT_EN	2	Group 0 member limit enable.
	RQ0_SET_PRIORITY	1	Group 0 fixed priority enable.
	RQ0_ROUND_ROBIN	0	Group 0 round robin enable.
20h (1241h)	REG1241	7:0	Default : 0x80 Access : R/W
	RQ0_ARBITER_SKIP_ON	7	Re-arbitrate if there is no RQ0_RDY.
	RQ0_CUT_IN_LEVEL2_EN	6	Group 0 cut in function level2 enable.
	RQ0_LIMIT_LAST_ENZ	5	Group 0 insert limit last disable.
	RQ0_CUT_IN_EN	4	Group 0 ongoing client service terminate.
	-	3	Reserved.
	RQ0_CNT2_CTRL_EN	2	Group 0 time out control 2 counter enable.
	RQ0_CNT1_CTRL_EN	1	Group 0 time out control 1 counter enable.
	RQ0_CNT0_CTRL_EN	0	Group 0 time out control 0 counter enable.
21h (1242h)	REG1242	7:0	Default : 0x00 Access : R/W
	RQ0_MEMBER_MAX[7:0]	7:0	Group 0 member maximum service number, unit is 4.
21h (1243h)	REG1243	7:0	Default : 0x00 Access : R/W
	RQ0_GROUP_MAX[7:0]	7:0	Group 0 group maximum service number, unit is 4.
22h (1244h)	REG1244	7:0	Default : 0x00 Access : R/W
	RQ0_TIMEOUT[7:0]	7:0	Group 0 time out number.
22h (1245h)	REG1245	7:0	Default : 0x00 Access : R/W
	RQ0_TIMEOUT[15:8]	7:0	See description of '1244h'.

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
23h (1246h)	REG1246	7:0	Default : 0x00 Access : R/W
	RQ0_MASK[7:0]	7:0	Group 0 request mask.
23h (1247h)	REG1247	7:0	Default : 0x00 Access : R/W
	RQ0_MASK[15:8]	7:0	See description of '1246h'.
24h (1248h)	REG1248	7:0	Default : 0xFF Access : R/W
	RQ0_HMASK[7:0]	7:0	Group 0 high priority mask.
24h (1249h)	REG1249	7:0	Default : 0xFF Access : R/W
	RQ0_HMASK[15:8]	7:0	See description of '1248h'.
25h (124Ah)	REG124A	7:0	Default : 0x10 Access : R/W
	RQ01_PRIORITY[3:0]	7:4	Group 0 request 1 priority.
	RQ00_PRIORITY[3:0]	3:0	Group 0 request 0 priority.
25h (124Bh)	REG124B	7:0	Default : 0x32 Access : R/W
	RQ03_PRIORITY[3:0]	7:4	Group 0 request 3 priority.
	RQ02_PRIORITY[3:0]	3:0	Group 0 request 2 priority.
26h (124Ch)	REG124C	7:0	Default : 0x54 Access : R/W
	RQ05_PRIORITY[3:0]	7:4	Group 0 request 5 priority.
	RQ04_PRIORITY[3:0]	3:0	Group 0 request 4 priority.
26h (124Dh)	REG124D	7:0	Default : 0x76 Access : R/W
	RQ07_PRIORITY[3:0]	7:4	Group 0 request 7 priority.
	RQ06_PRIORITY[3:0]	3:0	Group 0 request 6 priority.
27h (124Eh)	REG124E	7:0	Default : 0x98 Access : R/W
	RQ09_PRIORITY[3:0]	7:4	Group 0 request 9 priority.
	RQ08_PRIORITY[3:0]	3:0	Group 0 request 8 priority.
27h (124Fh)	REG124F	7:0	Default : 0xBA Access : R/W
	RQ0B_PRIORITY[3:0]	7:4	Group 0 request 11 priority.
	RQ0A_PRIORITY[3:0]	3:0	Group 0 request 10 priority.
28h (1250h)	REG1250	7:0	Default : 0xDC Access : R/W
	RQ0D_PRIORITY[3:0]	7:4	Group 0 request 13 priority.
	RQ0C_PRIORITY[3:0]	3:0	Group 0 request 12 priority.
28h (1251h)	REG1251	7:0	Default : 0xFE Access : R/W
	RQ0F_PRIORITY[3:0]	7:4	Group 0 request 15 priority.
	RQ0E_PRIORITY[3:0]	3:0	Group 0 request 14 priority.
29h	REG1253	7:0	Default : 0x00 Access : R/W

MIU Register (Bank = 12)				
Index (Absolute)	Mnemonic	Bit	Description	
(1253h)	RQ0_GROUP_DEADLINE[7:0]	7:0	Group 0 group deadline counter, unit is 64.	
2Ah (1254h)	REG1254	7:0	Default : 0x00	Access : R/W
	RQ0_CNT0_ID1[3:0]	7:4	Group 0 1st flow control ID 1.	
	RQ0_CNT0_ID0[3:0]	3:0	Group 0 1st flow control ID 0.	
2Ah (1255h)	REG1255	7:0	Default : 0x00	Access : R/W
	RQ0_CNT0_PERIOD[7:0]	7:0	Group 0 1st flow control mask period, unit is 4.	
2Bh (1256h)	REG1256	7:0	Default : 0x00	Access : R/W
	RQ0_CNT1_ID1[3:0]	7:4	Group 0 2nd flow control ID 1.	
	RQ0_CNT1_ID0[3:0]	3:0	Group 0 2nd flow control ID 0.	
2Bh (1257h)	REG1257	7:0	Default : 0x00	Access : R/W
	RQ0_CNT1_PERIOD[7:0]	7:0	Group 0 2nd flow control mask period, unit is 4.	
2Ch (1258h)	REG1258	7:0	Default : 0x00	Access : R/W
	RQ0_CNT2_ID1[3:0]	7:4	Group 0 3rd flow control ID 1.	
	RQ0_CNT2_ID0[3:0]	3:0	Group 0 3rd flow control ID 0.	
2Ch (1259h)	REG1259	7:0	Default : 0x00	Access : R/W
	RQ0_CNT2_PERIOD[7:0]	7:0	Group 0 3rd flow control mask period, unit is 4.	
2Dh (125Ah)	REG125A	7:0	Default : 0x00	Access : R/W
	RQ0_LIMIT_MASK[7:0]	7:0	Group 0 client limit mask.	
2Dh (125Bh)	REG125B	7:0	Default : 0x00	Access : R/W
	RQ0_LIMIT_MASK[15:8]	7:0	See description of '125Ah'.	
60h (12C0h)	REG12C0	7:0	Default : 0x00	Access : R/W
	PROTECT3_INV	7	4th protection condition invert. 1: If the client ID is not equal to 4th protection client ID 0/1, DRAM access is allowed. If the client ID is equal to 4th protection client ID 0/1, DRAM access is denied. 0: If the client ID is not equal to 4th protection client ID 0/1, DRAM access is denied. If the client ID is equal to 4th protection client ID 0/1, DRAM access is allowed.	
	PROTECT2_INV	6	3rd protection condition invert. 1: If the client ID is not equal to 3rd protection client ID 0/1, DRAM access is allowed. If the client ID is equal to 3rd protection client ID 0/1, DRAM access is denied. 0: If the client ID is not equal to 3rd protection client ID	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
			0/1, DRAM access is denied. If the client ID is equal to 3rd protection client ID 0/1, DRAM access is allowed.
	PROTECT1_INV	5	2nd protection condition invert. 1: If the client ID is not equal to 2nd protection client ID 0/1, DRAM access is allowed. If the client ID is equal to 2nd protection client ID 0/1, DRAM access is denied. 0: If the client ID is not equal to 2nd protection client ID 0/1, DRAM access is denied. If the client ID is equal to 2nd protection client ID 0/1, DRAM access is allowed.
	PROTECT0_INV	4	1st protection condition invert. 1: If the client ID is not equal to 1st protection client ID 0/1/2/3, DRAM access is allowed. If the client ID is equal to 1st protection client ID 0/1/2/3, DRAM access is denied. 0: If the client ID is not equal to 1st protection client ID 0/1/2/3, DRAM access is denied. If the client ID is equal to 1st protection client ID 0/1/2/3, DRAM access is allowed.
	PROTECT3_EN	3	4th protection enable.
	PROTECT2_EN	2	3rd protection enable.
	PROTECT1_EN	1	2nd protection enable.
	PROTECT0_EN	0	1st protection enable.
61h (12C2h)	REG12C2	7:0	Default : 0x00Access : R/W
	-	7:6	Reserved.
	PROTECT0_ID0[5:0]	5:0	1st protection client ID 0.
61h (12C3h)	REG12C3	7:0	Default : 0x00Access : R/W
	-	7:6	Reserved.
	PROTECT0_ID1[5:0]	5:0	1st protection client ID 1.
62h (12C4h)	REG12C4	7:0	Default : 0x00Access : R/W
	-	7:6	Reserved.
	PROTECT0_ID2[5:0]	5:0	1st protection client ID 2.
62h (12C5h)	REG12C5	7:0	Default : 0x00Access : R/W
	-	7:6	Reserved.

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
	PROTECT0_ID3[5:0]	5:0	1st protection client ID 3.
63h (12C6h)	REG12C6	7:0	Default : 0x00 Access : R/W
	PROTECT0_START[7:0]	7:0	1st protect start address = {start,8'h0}.
63h (12C7h)	REG12C7	7:0	Default : 0x00 Access : R/W
	PROTECT0_START[15:8]	7:0	See description of '12C6h'.
64h (12C8h)	REG12C8	7:0	Default : 0x00 Access : R/W
	PROTECT0_END[7:0]	7:0	1st protect end address = {end,8'hff}.
64h (12C9h)	REG12C9	7:0	Default : 0x00 Access : R/W
	PROTECT0_END[15:8]	7:0	See description of '12C8h'.
65h (12CAh)	REG12CA	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	PROTECT1_ID0[5:0]	5:0	2nd protection client ID 0.
65h (12CBh)	REG12CB	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	PROTECT1_ID1[5:0]	5:0	2nd protection client ID 1.
66h (12CCh)	REG12CC	7:0	Default : 0x00 Access : R/W
	PROTECT1_START[7:0]	7:0	2nd protect start address = {start,8'h0}.
66h (12CDh)	REG12CD	7:0	Default : 0x00 Access : R/W
	PROTECT1_START[15:8]	7:0	See description of '12CCh'.
67h (12CEh)	REG12CE	7:0	Default : 0x00 Access : R/W
	PROTECT1_END[7:0]	7:0	2nd protect end address = {end,8'hff}.
67h (12CFh)	REG12CF	7:0	Default : 0x00 Access : R/W
	PROTECT1_END[15:8]	7:0	See description of '12CEh'.
68h (12D0h)	REG12D0	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	PROTECT2_ID0[5:0]	5:0	3rd protection client ID 0.
68h (12D1h)	REG12D1	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	PROTECT2_ID1[5:0]	5:0	3rd protection client ID 1.
69h (12D2h)	REG12D2	7:0	Default : 0x00 Access : R/W
	PROTECT2_START[7:0]	7:0	3rd protect start address = {start,8'h0}.
69h (12D3h)	REG12D3	7:0	Default : 0x00 Access : R/W
	PROTECT2_START[15:8]	7:0	See description of '12D2h'.

MIU Register (Bank = 12)				
Index (Absolute)	Mnemonic	Bit	Description	
6Ah (12D4h)	REG12D4	7:0	Default : 0x00	Access : R/W
	PROTECT2_END[7:0]	7:0	3rdprotect end address = {end,8'hff}.	
6Ah (12D5h)	REG12D5	7:0	Default : 0x00	Access : R/W
	PROTECT2_END[15:8]	7:0	See description of '12D4h'.	
6Bh (12D6h)	REG12D6	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT3_ID0[5:0]	5:0	4th protection client ID 0.	
6Bh (12D7h)	REG12D7	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PROTECT3_ID1[5:0]	5:0	4th protection client ID 1.	
6Ch (12D8h)	REG12D8	7:0	Default : 0x00	Access : R/W
	PROTECT3_START[7:0]	7:0	4th protect start address = {start,8'h0}.	
6Ch (12D9h)	REG12D9	7:0	Default : 0x00	Access : R/W
	PROTECT3_START[15:8]	7:0	See description of '12D8h'.	
6Dh (12DAh)	REG12DA	7:0	Default : 0x00	Access : R/W
	PROTECT3_END[7:0]	7:0	4th protect end address = {end,8'hff}.	
6Dh (12DBh)	REG12DB	7:0	Default : 0x00	Access : R/W
	PROTECT3_END[15:8]	7:0	See description of '12DAh'.	
6Fh (12DEh)	REG12DE	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	PROTECT_LOG_CLR	0	1: Turn on the log of protection function.	
70h (12E0h)	REG12E0	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	FORCE_IN	6	Force read data.	
	FORCE_OUT	5	Force write data.	
	-	4:0	Reserved.	
70h (12E1h)	REG12E1	7:0	Default : 0x00	Access : RO, R/W
	-	7:2	Reserved.	
	WRITE_ONLY	1	Only write command is sent to DRAM.	
	READ_ONLY	0	Only read command is sent to DRAM.	
71h ~ 75h (12E2h ~ 12EBh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
78h (12F0h)	REG12F0	7:0	Default : 0x00	Access : R/W
	MIU_SEL0[7:0]	7:0	Group 0 clients access MIU0 or MIU1. 1: MIU1. 0: MIU0.	

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
78h (12F1h)	REG12F1	7:0	Default : 0x00 Access : R/W
	MIU_SEL0[15:8]	7:0	See description of '12F0h'.
79h (12F2h)	REG12F2	7:0	Default : 0x00 Access : R/W
	MIU_SEL1[7:0]	7:0	Group 1 clients access MIU0 or MIU1. 1: MIU1. 0: MIU0.
79h (12F3h)	REG12F3	7:0	Default : 0x00 Access : R/W
	MIU_SEL1[15:8]	7:0	See description of '12F2h'.
7Ah (12F4h)	REG12F4	7:0	Default : 0x00 Access : R/W
	MIU_SEL2[7:0]	7:0	Group 2 clients access MIU0 or MIU1. 1: MIU1. 0: MIU0.
7Ah (12F5h)	REG12F5	7:0	Default : 0x00 Access : R/W
	MIU_SEL2[15:8]	7:0	See description of '12F4h'.
7Ch (12F8h)	REG12F8	7:0	Default : 0x00 Access : R/W
	RDCRC_DATA_SEL[1:0]	7:6	Read CRC pattern data select.
	WDCRC_DATA_SEL[1:0]	5:4	Write CRC pattern data select.
	RDPTG_EN	3	Read pattern generator enable.
	WDCRC_STOP	2	CRC end.
	WDCRC_START	1	CRC start.
7Ch (12F9h)	WDCRC_RST	0	Reset CRC.
	REG12F9	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
7Dh (12FAh)	RDCRC_DATA_SEL[2]	0	See description of '12F8h'.
	REG12FA	7:0	Default : 0x00 Access : R/W
7Dh (12FBh)	PTN_MODE[7:0]	7:0	Pattern mode.
	REG12FB	7:0	Default : 0x00 Access : R/W
7Eh (12FCh)	PTN_MODE[15:8]	7:0	See description of '12FAh'.
	REG12FC	7:0	Default : 0x00 Access : R/W
7Eh (12FDh)	PTN_DATA[7:0]	7:0	Pattern data.
	REG12FD	7:0	Default : 0x00 Access : R/W
7Fh (12FEh)	PTN_DATA[15:8]	7:0	See description of '12FCh'.
	REG12FE	7:0	Default : 0x00 Access : RO
	READ_CRC[7:0]	7:0	Read CRC data.

MIU Register (Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
7Fh (12FFh)	REG12FF	7:0	Default : 0x00 Access : RO
	READ_CRC[15:8]	7:0	See description of '12FEh'.

VD_MCU Register (Bank = 13)

VD_MCU Register (Bank = 13)				
Index (Absolute)	Mnemonic	Bit	Description	
00h ~ 05h	-	7:0	Default : -	Access : -
(1300h ~ 130Bh)	-	7:0	Reserved.	
06h (130Ch)	REG130C	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	HK2VD_INT	1	HK MCU interrupt to VDMCU.	
	VD_MCU_RESET	0	VD MCU reset.	
06h ~ 27h	-	7:0	Default : -	Access : -
(130Dh ~ 134Fh)	-	7:0	Reserved.	
28h (1350h)	REG1350	7:0	Default : 0x01	Access : R/W
	-	7:3	Reserved.	
	VD_SPI_EN	2	Code using SPI.	
	VD_DRAM_EN	1	Code using DRAM.	
	VD_SRAM_EN	0	Code using SRAM.	
29h (1352h)	REG1352	7:0	Default : 0x00	Access : R/W
	VD_ROM_BANK[7:0]	7:0	Code ROM bank.	

VIF_RF Register (Bank = 14)

VIF_RF Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1400h)	REG1400	7:0	Default : 0x1F	Access : R/W
	-	7	Reserved.	
	TAGC_PWR	6	Tuner AGC power control. 1: Power on. 0: Power off.	
	TAFC_PWR	5	Tuner AFC power control. 1: Power on. 0: Power off.	
	VIF_CBC_PWRS	4	Power on the sound path of central bias circuit. 1: Power on.(VIF_CBC_PWR must =1) 0:power off.	
	VIF_CBC_PWR	3	Power on central bias circuit. 1: Power on. 0: Power off.	
	VIF_PLL_PWR	2	Power on VIF PLL. 1: Power on. 0: Power off.	
	VIF_VCOREG_PWR	1	VCO regulator power on. 1: Power on. 0: Power off.	
	VIF_VCO_PWR	0	VCO power on, 1:power on. 0: Power off.	
00h (1401h)	REG1401	7:0	Default : 0xFF	Access : R/W
	VIF_PGPWRV	7	PGA1_V power on. 1: Power on. 0: Power off.	
	VIF_MXPWRV	6	MX_V power on. 1: Power on. 0: Power off.	
	VIF_PWR_LPFV	5	LPF_V power on. 1: Power on. 0: Power off.	
	VIF_PWR_PGA2V	4	PGA2_V power on. 1: Power on. 0: Power off.	
	VIF_PGPWRS	3	PGA1_S power on. 1: Power on.	

VIF_RF Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: Power off.	
	VIF_MXPWRS	2	MX_S power on. 1: Power on. 0: Power off.	
	VIF_PWR_LPFS	1	LPF_S power on. 1: Power on. 0: Power off.	
	VIF_PWR_PGA2S	0	PGA2_S power on. 1: Power on. 0: Power off.	
01h (1402h)	REG1402	7:0	Default : 0x14	Access : R/W
	-	7:5	Reserved.	
	VIF_PLL_RSTZ	4	Reset the feedback divider. 0: Reset. 1: Normal operation.	
	-	3:2	Reserved.	
	VIF_PLL_R[1:0]	1:0	Regulator input source and output voltage setting. See Table 1.	
01h (1403h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
02h (1404h)	REG1404	7:0	Default : 0x24	Access : R/W
	TAGC_ODMODE	7	TAGC DAC output open-drain mode. 1: Open-drain voltage output. 0: 1mA current sink output.	
	TAFC_ODMODE	6	TAFC DAC output open-drain mode. 1: Open-drain voltage output. 0: 1mA current sink output.	
	VIF_PLL_MSEL	5	Bypass feedback divider re-sync function. 1: Resync. 0: Bypass resync.	
	-	4	Reserved.	
	VIF_PLL_M[3:0]	3:0	PLL post divider (Divion ratio = 2~15).	
02h (1405h)	REG1405	7:0	Default : 0x59	Access : R/W
	VIF_PLL_RSEL	7	Bypass reference divider. 1: Bypass(divide-by-1). 0: Normal operation(divide-by-2 or 3).	

VIF_RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description
	VIF_PLL_RDIV	6	PLL reference divider. 1: Fxtal/3. 0: Fxtal/2.
	VIF_PLL_N[5:0]	5:0	PLL feedback divider (Division ratio = 2~63).default:divide-by-25.
03h (1406h)	REG1406	7:0	Default : 0x05
	-	7:4	Access : R/W Reserved.
	VIF_PLL_LPEX	3	Charge pump current power control. 1: Power off. 0: Power on.
	-	2:0	Reserved.
03h (1407h)	REG1407	7:0	Default : 0x08
	-	7:5	Access : R/W Reserved.
	VIF_PLL_SBIAS	4	VCO self bias enable. 1: Enable. 0: Disable.
	VIF_VCO_REF	3	VCO bandgap reference voltage selection. 1: 1.20V. 0: 1.10V.
	VIF_VCOREG_SBIAS	2	VCO self bias enable. 1: Enable. 0: Disable.
	-	1:0	Reserved.
04h (1408h)	REG1408	7:0	Default : 0x44
	VIF_CAL_START_MC	7	Access : R/W VCO band calibration start. 1: Enable. 0: No operation.(self-clear).
	VIF_VCO_LK	6	Kvco control bit 1. 1: Kvco~170MHz/V. 0: Kvco~120MHz/V.
	-	5	Reserved.
	VIF_VCO_LP	4	VCO low power mode. 1: 4m. 0: 6mA.
	-	3	Reserved.
	VIF_VCO_BANK_W[2:0]	2:0	Override bits for VCO bank selection.

VIF_RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description
			See Table 4.
04h ~ 05h (1409h ~ 140Ah)	-	7:0	Default : - Access : -
	-	-	Reserved.
05h (140Bh)	REG140B	7:0	Default : 0xAA Access : R/W
	VIF_CALIB_TUNE	7	LPF calibration enable (power on). 1: Enable. 0: Disable.
	-	6	Reserved.
	VIF_RN_TUNE	5	Reset for LPF tuning circuit. 1: Normal operation. 0: Reset (restart calibration after reset finished).
	-	4:0	Reserved.
06h ~ 07h (140Ch ~ 140Fh)	-	7:0	Default : - Access : -
	-	-	Reserved.
08h (1410h)	REG1410	7:0	Default : 0x00 Access : R/W
	TAGC_TAFC_NRZDATA	7	TAGC/TAFC DAC NRZ input data selection. 1: NRZ input data. 0: RZ input data.
	-	6:0	Reserved.
08h ~ 09h (1411h ~ 1413h)	-	7:0	Default : - Access : -
	-	-	Reserved.
0Bh (1416h)	REG1416	7:0	Default : 0x90 Access : R/W
	-	7:5	Reserved.
	TAGC_POLARITY	4	Tuner AGC polarity control. 1: Positive logic. 0: Negative logic.
	-	3:0	Reserved.
0Bh (1417h)	REG1417	7:0	Default : 0xD0 Access : R/W
	TAGC_DITHER_EN	7	Dither signal enable. 1: Enable. 0: Disable.
	TAGC_SEL_SECORDER	6	Select 2nd order delta-sigma modulator. 1: 2nd order.

VIF_RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description
			0: 1st order.
	TAGC_DITHER_SHIFT[2:0]	5:3	Dither signal gain setting. 0~7 -> 2 ⁰ ~2 ⁷ .
	-	2:0	Reserved.
0Ch (1419h)	-	7:0	Default : - Access : -
	-	-	Reserved.
0Dh (141Ah)	REG141A	7:0	Default : 0x00 Access : RO
	VCOCAL_FAIL	7	VCO bank calibration flag. 1: Fail. 0: Pass.
	VCTRL_OVER	6	1: VCTRL larger than 2V. 0: VCTRL less than 2V.
	VCTRL_UNDER	5	1: VCTRL less than 1V. 0: VCTRL larger than 1V.
	LOCK	4	PLL LOCK detection, 1:LOCKed. 0: UnLOCKed.
	VIF_PLL_CPINIT	3	Charge pump output open and tied to 1.5V. 1: Charge pump output tied to 1.5V. 0: Normal operation.
	VIF_VCO_BANK[2:0]	2:0	VCO bank selection. See Table 4.
0Dh (141Bh)	REG141B	7:0	Default : 0x00 Access : RO
	VIF_PGA1GAINV[3:0]	7:4	DBB PGA1_V gain setting low byte. See Table 5.
	VIF_PGA1GAINS[3:0]	3:0	DBB PGA1_S gain setting low byte. See Table 5.
0Eh (141Ch)	REG141C	7:0	Default : 0x00 Access : RO
	VIF_GAIN_PGA2V[3:0]	7:4	DBB PGA2_V gain setting high byte. See Table 6.
	VIF_GAIN_PGA2S[3:0]	3:0	DBB PGA2_S gain setting low byte. See Table 6.
0Eh (141Dh)	REG141D	7:0	Default : 0x00 Access : RO
	-	7	Reserved.
	VIF_CAL_FINISH	6	VCO Calibration Finish.
	VIF_STOPCAL_TUNE	5	LPF calibration finished flag.

VIF_RF Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
			1: Finished (disbale LPF tuning circuit clock). 0: Under LPF calibrating.	
	VIF_FCODE_OUT[4:0]	4:0	LPF cap bank calibration output code.	
0Fh (141Eh)	REG141E	7:0	Default : 0x00	Access : RO
	VIF_CAL_GAP[7:0]	7:0	VIF VCO Calibration gap.	
10h (1420h)	REG1420	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	VSYNC_VD_POLARITY	1	It respects to the vsync polarity from VD; 0=low active; 1=high active.	
	VSYNC_VD_MASK	0	1=mask vsync from VD.	
10h ~ 14h (1421h ~ 1428h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
20h (1440h)	REG1440	7:0	Default : 0x0B	Access : R/W
	-	7:5	Reserved.	
	CLAMPGAIN_STATUS_FREEZE	4	1=freeze clampgain status.	
	CLAMPGAIN_SEL	3	1=clamp select porch 0=clamp select sync bottom.	
	CLAMPGAIN_ENABLE	2	1=clampgain enable.	
	CLAMPGAIN_BYPASS	1	1=clampgain bypass.	
	CLAMPGAIN_RSTZ	0	0=clampgain reset.	
21h (1442h)	REG1442	7:0	Default : 0x00	Access : R/W
	CLAMPGAIN_REF[7:0]	7:0	Porch or syncbottom reference level.	
21h (1443h)	REG1443	7:0	Default : 0x00	Access : R/W
	CLAMPGAIN_SYNCHEIGHT_REF[7:0]	7:0	Syncheight reference level.	
22h (1444h)	REG1444	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CLAMPGAIN_KG[2:0]	6:4	Gain loop filter parameter 1~7->2 ⁻³ ~2 ⁻⁹ .	
	-	3	Reserved.	
22h (1445h)	CLAMPGAIN_KC[2:0]	2:0	Clamp loop filter parameter 1~7->2 ⁻³ ~2 ⁻⁹ .	
	REG1445	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	CLAMPGAIN_GAIN_OVERWRITE	1	1=gain override enable.	

VIF_RF Register (Bank = 14)

Index (Absolute)	Mnemonic	Bit	Description
	CLAMPGAIN_CLAMP_OVERWRITE	0	1=clamp override enable.
23h (1446h)	REG1446	7:0	Default : 0x00 Access : R/W
	CLAMPGAIN_CLAMP_VALUE[7:0]	7:0	Clamp override value(double load).
23h (1447h)	REG1447	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	CLAMPGAIN_CLAMP_VALUE[10:8]	2:0	See description of '1446h'.
24h (1448h)	REG1448	7:0	Default : 0x00 Access : R/W
	CLAMPGAIN_GAIN_VALUE[7:0]	7:0	Gain override value(double load).
24h (1449h)	REG1449	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	CLAMPGAIN_GAIN_VALUE[10:8]	2:0	See description of '1448h'.
25h (144Ah)	REG144A	7:0	Default : 0x80 Access : R/W
	CLAMPGAIN_CLAMP_MIN[7:0]	7:0	Clamp min.
25h (144Bh)	REG144B	7:0	Default : 0x7F Access : R/W
	CLAMPGAIN_CLAMP_MAX[7:0]	7:0	Clamp max.
26h (144Ch)	REG144C	7:0	Default : 0x40 Access : R/W
	CLAMPGAIN_GAIN_MIN[7:0]	7:0	Gain min.
26h (144Dh)	REG144D	7:0	Default : 0xFF Access : R/W
	CLAMPGAIN_GAIN_MAX[7:0]	7:0	Gain max.
27h (144Eh)	REG144E	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	CLAMPGAIN_SYNCBOTTOM_OFFSET[6:0]	6:0	Sync bottom offset.
27h (144Fh)	REG144F	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	CLAMPGAIN_RATIO[2:0]	2:0	Update ratio.
28h (1450h)	REG1450	7:0	Default : 0x00 Access : R/W
	CLAMPGAIN_SYNCBOTTOM_CNT[7:0]	7:0	Sync bottom counter max(double load).
28h (1451h)	REG1451	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	CLAMPGAIN_SYNCBOTTOM_CNT[11:8]	3:0	See description of '1450h'.

VIF_RF Register (Bank = 14)				
Index (Absolute)	Mnemonic	Bit	Description	
29h (1452h)	REG1452	7:0	Default : 0xF8	Access : R/W
	CLAMPGAIN_PORCH_CNT[7:0]	7:0	Porch counter max(double load).	
29h (1453h)	REG1453	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	CLAMPGAIN_PORCH_CNT[8]	0	See description of '1452h'.	
2Ah (1454h)	REG1454	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_PEAK_MEAN[7:0]	7:0	Peak mean.	
2Ah (1455h)	REG1455	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_PEAK_MEAN[15:8]	7:0	See description of '1454h'.	
2Bh (1456h)	REG1456	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_SYNCBOTTOM_MEAN[7:0]	7:0	Sync bottom mean.	
2Bh (1457h)	REG1457	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_SYNCBOTTOM_MEAN[15:8]	7:0	See description of '1456h'.	
2Ch (1458h)	REG1458	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_PORCH_MEAN[7:0]	7:0	Porch mean.	
2Ch (1459h)	REG1459	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_PORCH_MEAN[15:8]	7:0	See description of '1458h'.	
2Dh (145Ah)	REG145A	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_CLAMP[7:0]	7:0	Clamp.	
2Dh (145Bh)	REG145B	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_CLAMP[15:8]	7:0	See description of '145Ah'.	
2Eh (145Ch)	REG145C	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_GAIN[7:0]	7:0	Gain.	
2Eh (145Dh)	REG145D	7:0	Default : 0x00	Access : RO
	CLAMPGAIN_GAIN[15:8]	7:0	See description of '145Ch'.	
40h (1480h)	REG1480	7:0	Default : 0x05	Access : R/W
	-	7:5	Reserved.	
	VSYNC_DET_DATAIN_SEL	4	0: Vsync detector in from cvbs before clampgain 1: vsync detector in from cvbs after clampgain.	
	VSYNC_LPF_SEL[1:0]	3:2	Lpf leaky factor select -> 2 ⁻¹⁰ ~2 ⁻¹³ .	0~3

VIF_RF Register (Bank = 14)			
Index (Absolute)	Mnemonic	Bit	Description
	VSYNC_ENABLE	1	1=vsync detector enable.
	VSYNC_RSTZ	0	0=vsync detector reset.
41h (1482h)	REG1482	7:0	Default : 0x00 Access : R/W
	VSYNC_OFFSET[7:0]	7:0	Vsync offset.
41h (1483h)	REG1483	7:0	Default : 0xFF Access : R/W
	VSYNC_CNT[7:0]	7:0	Number of samples to calculate vsync.
42h (1484h)	REG1484	7:0	Default : 0x40 Access : R/W
	VSYNC_VSYNC_CNT[7:0]	7:0	Counter used to calculate vsync.
42h (1485h)	REG1485	7:0	Default : 0x80 Access : R/W
	VSYNC_BYPASS_CNT[7:0]	7:0	Counter used to bypass detecting two minimum.
43h (1486h)	REG1486	7:0	Default : 0x00 Access : RO
	VSYN_MIN_CNT[7:0]	7:0	Minimum point counter value.
55h ~ 7Ah (14Aah ~ 14F4h)	-	7:0	Default : -
	-	-	Reserved.

DBB1 Register (Bank = 15)

DBB1 Register (Bank = 15)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1500h)	REG1500	7:0	Default : 0x7F	Access : R/W
	-	7	Reserved.	
	ADAGC_SOFT_RSTZ	6	AAGC software reset (low active).	
	AAGC_SOFT_RSTZ	5	AAGC software reset (low active).	
	VDAGC2_SOFT_RSTZ	4	VDAGC2 software reset (low active).	
	VDAGC1_SOFT_RSTZ	3	VDAGC1 software reset (low active).	
	VAGC_SOFT_RSTZ	2	VAGC software reset (low active).	
	FILTER_SOFT_RSTZ	1	Filter software reset (low active).	
	AFC_SOFT_RSTZ	0	AFC software reset (low active).	
01h (1502h)	REG1502	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	MODULATION_TYPE[3:0]	3:0	Bit[0]: filter modulation type bit[1]: VAGC modulation type bit[2]: VDAGC1 modulation type bit[3]: VDAGC2 modulation type 0: negative modulation 1: positive modulation.	
02h (1504h)	REG1504	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	AUDIO_BYPASS[1:0]	1:0	00: Normal audio path mode. 01: Bypass audio mixer input data. 10: Bypass audio mixer output data. 11: Normal audio path mode.	
03h ~ 07h (1506h ~ 150Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Ah (1514h)	REG1514	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CR_DL_A[3:0]	3:0	(user-added) audio delay. Delay = delay_a*8. {4}.	
0Ah (1515h)	REG1515	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	

DBB1 Register (Bank = 15)				
Index (Absolute)	Mnemonic	Bit	Description	
	CR_F_OFFSET[5:0]	5:0	(user-added) frequency offset. (6,0).	
0Bh (1516h)	REG1516	7:0	Default : 0xFF	Access : R/W
	CR_PD_ERR_MAX[7:0]	7:0	Maximum phase error (absolute value). <14,15>. (double load).	
0Bh (1517h)	REG1517	7:0	Default : 0x3F	Access : R/W
	-	7:6	Reserved.	
	CR_PD_ERR_MAX[13:8]	5:0	See description of '1516h'.	
0Ch (1518h)	REG1518	7:0	Default : 0x00	Access : R/W
	CR_PD_KL[7:0]	7:0	Scaling factor for hard limiter. <14,15>. (double load).	
0Ch (1519h)	REG1519	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CR_PD_KL[13:8]	5:0	See description of '1518h'.	
0Dh (151Ah)	REG151A	7:0	Default : 0x00	Access : R/W
	CR_ANCO_NOTCH_A1[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).	
0Dh (151Bh)	REG151B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CR_ANCO_NOTCH_A1[11:8]	3:0	See description of '151Ah'.	
0Eh (151Ch)	REG151C	7:0	Default : 0x00	Access : R/W
	CR_ANCO_NOTCH_A2[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>.(double load).	
0Eh (151Dh)	REG151D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CR_ANCO_NOTCH_A2[11:8]	3:0	See description of '151Ch'.	
0Fh (151Eh)	REG151E	7:0	Default : 0x00	Access : R/W
	CR_ANCO_NOTCH_B1[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).	
0Fh	REG151F	7:0	Default : 0x00	Access : R/W

DBB1 Register (Bank = 15)				
Index (Absolute)	Mnemonic	Bit	Description	
(151Fh)	-	7:4	Reserved.	
	CR_ANCO_NOTCH_B1[11:8]	3:0	See description of '151Eh'.	
10h (1520h)	REG1520	7:0	Default : 0x7E	Access : R/W
	CR_PD_LIMITER	7	Hard limiter. 0: No hard limiter. 1: Hard limiter.	
	CR_K_SEL	6	Loop parameter select. 0: Kp1, ki1, kf1, kp2, ki2, kf2. 1: Kp, ki, kf.	
	-	5	Reserved.	
	CR_LPF_SEL	4	LPF select. 0: LPF1. 1: LPF2.	
	CR_VNCO_INV	3	Output inversion. 0: Not invert output. 1: Invert output based on in-phase component.	
	CR_PD_X2	2	(cordic). 0: Lock 0 degree. 1: Lock 0 or 180 degree.	
	CR_PD_MODE	1	0: Imaginary party. 1: Cordic.	
	CR_ANCO_SEL	0	Audio nco select. 0: Nco_ff. 1: Nco_ff_a.	
11h (1522h)	REG1522	7:0	Default : 0x00	Access : R/W
	CR_KI_SW[3:0]	7:4	Loop filter integral coefficient. 0 -> 0. 1~11 -> $2^{-12} \sim 2^{-22}$. 12~15 -> 0.	
	CR_KP_SW[3:0]	3:0	Loop filter proportional coefficient. 0 -> 0. 1~11 -> $2^{-2} \sim 2^{-12}$. 12~15 -> 0.	
11h (1523h)	REG1523	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CR_KF_SW[3:0]	3:0	Loop filter frequency coefficient.	

DBB1 Register (Bank = 15)				
Index (Absolute)	Mnemonic	Bit	Description	
			0 -> 0. 1~11 -> $2^{-8} \sim 2^{-18}$. 12~15 -> 0.	
12h (1524h)	REG1524	7:0	Default : 0x00	Access : R/W
	CR_RATE[7:0]	7:0	Rate = $F_c/(F_s/2) + f_{offset}$. Fs: Sampling frequency. Fc: Carrier frequency. <21,22> (double load).	
12h (1525h)	REG1525	7:0	Default : 0x00	Access : R/W
	CR_RATE[15:8]	7:0	See description of '1524h'.	
13h (1526h)	REG1526	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CR_RATE[20:16]	4:0	See description of '1524h'.	
14h (1528h)	REG1528	7:0	Default : 0x43	Access : R/W
	CR_KI1_HW[3:0]	7:4	Loop filter integral coefficient. 0 -> 0. 1~11 -> $2^{-12} \sim 2^{-22}$. 12~15 -> 0.	
	CR_KP1_HW[3:0]	3:0	Loop filter proportional coefficient. 0 -> 0. 1~11 -> $2^{-2} \sim 2^{-12}$. 12~15 -> 0.	
14h (1529h)	REG1529	7:0	Default : 0x08	Access : R/W
	-	7:4	Reserved.	
	CR_KF1_HW[3:0]	3:0	Loop filter frequency coefficient. 0 -> 0. 1~11 -> $2^{-8} \sim 2^{-18}$. 12~15 -> 0.	
15h (152Ah)	REG152A	7:0	Default : 0x64	Access : R/W
	CR_KI2_HW[3:0]	7:4	Loop filter integral coefficient. 0 -> 0. 1~11 -> $2^{-12} \sim 2^{-22}$. 12~15 -> 0.	
	CR_KP2_HW[3:0]	3:0	Loop filter proportional coefficient. 0 -> 0. 1~11 -> $2^{-2} \sim 2^{-12}$.	

DBB1 Register (Bank = 15)				
Index (Absolute)	Mnemonic	Bit	Description	
			12~15 -> 0.	
15h (152Bh)	REG152B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CR_KF2_HW[3:0]	3:0	Loop filter frequency coefficient. 0 -> 0. 1~11 -> $2^{-8} \sim 2^{-18}$. 12~15 -> 0.	
16h (152Ch)	REG152C	7:0	Default : 0x40	Access : R/W
	CR_LOCK_TH[7:0]	7:0	Lock threshold. <10,10>. (double load).	
16h (152Dh)	REG152D	7:0	Default : 0x00	Access : R/W
	CR_LOCK_TH[15:8]	7:0	See description of '152Ch'.	
17h (152Eh)	REG152E	7:0	Default : 0x60	Access : R/W
	CR_FOE_SCAL_FACTOR[7:0]	7:0	Frequency offset estimation scaling factor. Foe_scale_factor = (Fs/2)/(F_step/4). Fs: Sampling frequency. F_step: Tuner frequency step, e.g. 62.5 KHz, 50 KHz. (12,-2). (double load).	
17h (152Fh)	REG152F	7:0	Default : 0x03	Access : R/W
	-	7:4	Reserved.	
	CR_FOE_SCAL_FACTOR[11:8]	3:0	See description of '152Eh'.	
18h (1530h)	REG1530	7:0	Default : 0x00	Access : R/W
	CR_LOCK_NUM[7:0]	7:0	Lock number. <20,0>. (double load).	
18h (1531h)	REG1531	7:0	Default : 0x80	Access : R/W
	CR_LOCK_NUM[15:8]	7:0	See description of '1530h'.	
19h (1532h)	REG1532	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CR_LOCK_NUM[19:16]	3:0	See description of '1530h'.	
1Ah (1534h)	REG1534	7:0	Default : 0x40	Access : R/W
	CR_UNLOCK_NUM[7:0]	7:0	Unlock number.	

DBB1 Register (Bank = 15)				
Index (Absolute)	Mnemonic	Bit	Description	
			<20,0>. (double load).	
1Ah (1535h)	REG1535	7:0	Default : 0x00	Access : R/W
	CR_UNLOCK_NUM[15:8]	7:0	See description of '1534h'.	
1Bh (1536h)	REG1536	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CR_UNLOCK_NUM[19:16]	3:0	See description of '1534h'.	
1Ch (1538h)	REG1538	7:0	Default : 0x00	Access : RO
	CR_FOE[7:0]	7:0	Frequency offset estimation. (8,0).	
1Ch (1539h)	REG1539	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	CR_LOCK_STATUS	0	Lock status. 0: Unlock. 1: Lock.	
1Dh (153Ah)	REG153A	7:0	Default : 0x00	Access : RO
	CR_LOCK_LEAKY_FF_I[7:0]	7:0	(in-phase) lock leaky integrator flip-flop. (16,16).	
1Dh (153Bh)	REG153B	7:0	Default : 0x00	Access : RO
	CR_LOCK_LEAKY_FF_I[15:8]	7:0	See description of '153Ah'.	
1Eh (153Ch)	REG153C	7:0	Default : 0x00	Access : RO
	CR_LOCK_LEAKY_FF_Q[7:0]	7:0	(quadrature) lock leaky integrator flip-flop. (16,16).	
1Eh (153Dh)	REG153D	7:0	Default : 0x00	Access : RO
	CR_LOCK_LEAKY_FF_Q[15:8]	7:0	See description of '153Ch'.	
1Fh (153Eh)	REG153E	7:0	Default : 0x00	Access : R/W
	CR_ANCO_NOTCH2_A1[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).	
1Fh (153Fh)	REG153F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CR_ANCO_NOTCH2_A1[11:8]	3:0	See description of '153Eh'.	
20h (1540h)	REG1540	7:0	Default : 0x00	Access : R/W
	CR_ANCO_NOTCH2_A2[7:0]	7:0	Notch filter (denominator) coefficient.	

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
			<12,22>. (double load).
20h (1541h)	REG1541	7:0	Default : 0x00
	-	7:4	Reserved.
	CR_ANCO_NOTCH2_A2[11:8]	3:0	See description of '1540h'.
21h (1542h)	REG1542	7:0	Default : 0x00
	CR_ANCO_NOTCH2_B1[7:0]	7:0	Notch filter (denominator) coefficient. <12,22>. (double load).
21h (1543h)	REG1543	7:0	Default : 0x00
	-	7:4	Reserved.
	CR_ANCO_NOTCH2_B1[11:8]	3:0	See description of '1542h'.
22h ~ 40h (1544h ~ 1581h)	-	7:0	Default : -
	-	-	Reserved.
41h (1582h)	REG1582	7:0	Default : 0x10
	DC_C[7:0]	7:0	Coefficient of DC_Notch on video path.
41h (1583h)	REG1583	7:0	Default : 0x10
	A_DC_C[7:0]	7:0	Coefficient of A_DC_Notch on audio path.
42h (1584h)	REG1584	7:0	Default : 0x1F
	N_A1_C0[7:0]	7:0	Coefficient of Notch_A1 on video path(double load).
42h (1585h)	REG1585	7:0	Default : 0x03
	-	7:3	Reserved.
	N_A1_C0[10:8]	2:0	See description of '1584h'.
43h (1586h)	REG1586	7:0	Default : 0x3C
	N_A1_C1[7:0]	7:0	Coefficient of Notch_A1 on video path(double load).
43h (1587h)	REG1587	7:0	Default : 0x06
	-	7:3	Reserved.
	N_A1_C1[10:8]	2:0	See description of '1586h'.
44h (1588h)	REG1588	7:0	Default : 0xAE
	N_A1_C2[7:0]	7:0	Coefficient of Notch_A1 on video path(double load).
44h (1589h)	REG1589	7:0	Default : 0x04
	-	7:3	Reserved.

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
	N_A1_C2[10:8]	2:0	See description of '1588h'.
45h (158Ah)	REG158A	7:0	Default : 0x99
	N_A2_C0[7:0]	7:0	Coefficient of Notch_A2 on video path(double load).
45h (158Bh)	REG158B	7:0	Default : 0x03
	-	7:3	Reserved.
	N_A2_C0[10:8]	2:0	See description of '158Ah'.
46h (158Ch)	REG158C	7:0	Default : 0x3C
	N_A2_C1[7:0]	7:0	Coefficient of Notch_A2 on video path(double load).
46h (158Dh)	REG158D	7:0	Default : 0x06
	-	7:3	Reserved.
	N_A2_C1[10:8]	2:0	See description of '158Ch'.
47h (158Eh)	REG158E	7:0	Default : 0x2D
	N_A2_C2[7:0]	7:0	Coefficient of Notch_A2 on video path(double load).
47h (158Fh)	REG158F	7:0	Default : 0x04
	-	7:3	Reserved.
	N_A2_C2[10:8]	2:0	See description of '158Eh'.
48h (1590h)	REG1590	7:0	Default : 0xA7
	AN_C0[7:0]	7:0	Coefficient of A_NOTCH on audio path(double load).
48h (1591h)	REG1591	7:0	Default : 0x00
	-	7:3	Reserved.
	AN_C0[10:8]	2:0	See description of '1590h'.
49h (1592h)	REG1592	7:0	Default : 0x3C
	AN_C1[7:0]	7:0	Coefficient of A_NOTCH on audio path(double load).
49h (1593h)	REG1593	7:0	Default : 0x06
	-	7:3	Reserved.
	AN_C1[10:8]	2:0	See description of '1592h'.
4Ah (1594h)	REG1594	7:0	Default : 0x4F
	AN_C2[7:0]	7:0	Coefficient of A_NOTCH on audio path(double load).
4Ah (1595h)	REG1595	7:0	Default : 0x07
	-	7:3	Reserved.
	AN_C2[10:8]	2:0	See description of '1594h'.
4Bh	REG1596	7:0	Default : 0x00

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
(1596h)	GDE_C0[7:0]	7:0	Coefficient of sos11(double load).
4Bh (1597h)	REG1597	7:0	Default : 0x00
	-	7:3	Reserved.
	GDE_C0[10:8]	2:0	See description of '1596h'.
4Ch (1598h)	REG1598	7:0	Default : 0x00
	GDE_C1[7:0]	7:0	Coefficient of sos11(double load).
4Ch (1599h)	REG1599	7:0	Default : 0x00
	-	7:3	Reserved.
	GDE_C1[10:8]	2:0	See description of '1598h'.
4Dh (159Ah)	REG159A	7:0	Default : 0x00
	GDE_C2[7:0]	7:0	Coefficient of sos11(double load).
4Dh (159Bh)	REG159B	7:0	Default : 0x00
	-	7:3	Reserved.
	GDE_C2[10:8]	2:0	See description of '159Ah'.
4Eh (159Ch)	REG159C	7:0	Default : 0x00
	GDE_C3[7:0]	7:0	Coefficient of sos11(double load).
4Eh (159Dh)	REG159D	7:0	Default : 0x00
	-	7:3	Reserved.
	GDE_C3[10:8]	2:0	See description of '159Ch'.
4Fh (159Eh)	REG159E	7:0	Default : 0x00
	GDE_C4[7:0]	7:0	Coefficient of sos11(double load).
4Fh (159Fh)	REG159F	7:0	Default : 0x00
	-	7:3	Reserved.
	GDE_C4[10:8]	2:0	See description of '159Eh'.
50h (15A0h)	REG15A0	7:0	Default : 0x00
	GDE_C5[7:0]	7:0	Coefficient of sos12(double load).
50h (15A1h)	REG15A1	7:0	Default : 0x00
	-	7:3	Reserved.
	GDE_C5[10:8]	2:0	See description of '15A0h'.
51h (15A2h)	REG15A2	7:0	Default : 0x00
	GDE_C6[7:0]	7:0	Coefficient of sos12(double load).
51h	REG15A3	7:0	Default : 0x00
			Access : R/W

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
(15A3h)	-	7:3	Reserved.
	GDE_C6[10:8]	2:0	See description of '15A2h'.
52h (15A4h)	REG15A4	7:0	Default : 0x00 Access : R/W
	GDE_C7[7:0]	7:0	Coefficient of sos12(double load).
52h (15A5h)	REG15A5	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	GDE_C7[10:8]	2:0	See description of '15A4h'.
53h (15A6h)	REG15A6	7:0	Default : 0x9B Access : R/W
	N_A3_C0[7:0]	7:0	Coefficient of Notch_A3 on video path(double load).
53h (15A7h)	REG15A7	7:0	Default : 0x02 Access : R/W
	-	7:3	Reserved.
	N_A3_C0[10:8]	2:0	See description of '15A6h'.
54h (15A8h)	REG15A8	7:0	Default : 0x3C Access : R/W
	N_A3_C1[7:0]	7:0	Coefficient of Notch_A3 on video path(double load).
54h (15A9h)	REG15A9	7:0	Default : 0x06 Access : R/W
	-	7:3	Reserved.
	N_A3_C1[10:8]	2:0	See description of '15A8h'.
55h (15AAh)	REG15AA	7:0	Default : 0x3A Access : R/W
	N_A3_C2[7:0]	7:0	Coefficient of Notch_A3 on video path(double load).
55h (15ABh)	REG15AB	7:0	Default : 0x05 Access : R/W
	-	7:3	Reserved.
	N_A3_C2[10:8]	2:0	See description of '15AAh'.
56h (15ACh)	REG15AC	7:0	Default : 0x83 Access : R/W
	N_A4_C0[7:0]	7:0	Coefficient of Notch_A4 on video path(double load).
56h (15ADh)	REG15AD	7:0	Default : 0x02 Access : R/W
	-	7:3	Reserved.
	N_A4_C0[10:8]	2:0	See description of '15ACh'.
57h (15AEh)	REG15AE	7:0	Default : 0x3C Access : R/W
	N_A4_C1[7:0]	7:0	Coefficient of Notch_A4 on video path(double load).
57h (15AFh)	REG15AF	7:0	Default : 0x06 Access : R/W
	-	7:3	Reserved.
	N_A4_C1[10:8]	2:0	See description of '15AEh'.

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
58h (15B0h)	REG15B0	7:0	Default : 0x54 Access : R/W
	N_A4_C2[7:0]	7:0	Coefficient of Notch_A4 on video path(double load).
58h (15B1h)	REG15B1	7:0	Default : 0x05 Access : R/W
	-	7:3	Reserved.
	N_A4_C2[10:8]	2:0	See description of '15B0h'.
59h (15B2h)	REG15B2	7:0	Default : 0x00 Access : R/W
	SOS12_C3[7:0]	7:0	Coefficient of sos12(double load).
59h (15B3h)	REG15B3	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS12_C3[10:8]	2:0	See description of '15B2h'.
5Ah (15B4h)	REG15B4	7:0	Default : 0x00 Access : R/W
	SOS12_C4[7:0]	7:0	Coefficient of sos12(double load).
5Ah (15B5h)	REG15B5	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS12_C4[10:8]	2:0	See description of '15B4h'.
5Bh (15B6h)	REG15B6	7:0	Default : 0x00 Access : R/W
	SOS21_C0[7:0]	7:0	Coefficient of sos21(double load).
5Bh (15B7h)	REG15B7	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS21_C0[10:8]	2:0	See description of '15B6h'.
5Ch (15B8h)	REG15B8	7:0	Default : 0x00 Access : R/W
	SOS21_C1[7:0]	7:0	Coefficient of sos21(double load).
5Ch (15B9h)	REG15B9	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS21_C1[10:8]	2:0	See description of '15B8h'.
5Dh (15BAh)	REG15BA	7:0	Default : 0x00 Access : R/W
	SOS21_C2[7:0]	7:0	Coefficient of sos21(double load).
5Dh (15BBh)	REG15BB	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS21_C2[10:8]	2:0	See description of '15BAh'.
5Eh (15BCh)	REG15BC	7:0	Default : 0x00 Access : R/W
	SOS21_C3[7:0]	7:0	Coefficient of sos21(double load).

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
5Eh (15BDh)	REG15BD	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS21_C3[10:8]	2:0	See description of '15BCh'.
5Fh (15BEh)	REG15BE	7:0	Default : 0x00 Access : R/W
	SOS21_C4[7:0]	7:0	Coefficient of sos21(double load).
5Fh (15BFh)	REG15BF	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS21_C4[10:8]	2:0	See description of '15BEh'.
60h (15C0h)	REG15C0	7:0	Default : 0x00 Access : R/W
	SOS22_C0[7:0]	7:0	Coefficient of sos22(double load).
60h (15C1h)	REG15C1	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS22_C0[10:8]	2:0	See description of '15C0h'.
61h (15C2h)	REG15C2	7:0	Default : 0x00 Access : R/W
	SOS22_C1[7:0]	7:0	Coefficient of sos22(double load).
61h (15C3h)	REG15C3	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS22_C1[10:8]	2:0	See description of '15C2h'.
62h (15C4h)	REG15C4	7:0	Default : 0x00 Access : R/W
	SOS22_C2[7:0]	7:0	Coefficient of sos22(double load).
62h (15C5h)	REG15C5	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS22_C2[10:8]	2:0	See description of '15C4h'.
63h (15C6h)	REG15C6	7:0	Default : 0x00 Access : R/W
	SOS22_C3[7:0]	7:0	Coefficient of sos22(double load).
63h (15C7h)	REG15C7	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SOS22_C3[10:8]	2:0	See description of '15C6h'.
64h (15C8h)	REG15C8	7:0	Default : 0x00 Access : R/W
	SOS22_C4[7:0]	7:0	_b4tob0.
64h (15C9h)	REG15C9	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
	SOS22_C4[10:8]	2:0	See description of '15C8h'.
65h (15CAh)	REG15CA	7:0	Default : 0x00
	SOS31_C0[7:0]	7:0	Coefficient of sos31(double load).
65h (15CBh)	REG15CB	7:0	Default : 0x00
	-	7:3	Reserved.
	SOS31_C0[10:8]	2:0	See description of '15CAh'.
66h (15CCh)	REG15CC	7:0	Default : 0x00
	SOS31_C1[7:0]	7:0	Coefficient of sos31(double load).
66h (15CDh)	REG15CD	7:0	Default : 0x00
	-	7:3	Reserved.
	SOS31_C1[10:8]	2:0	See description of '15CCh'.
67h (15CEh)	REG15CE	7:0	Default : 0x00
	SOS31_C2[7:0]	7:0	Coefficient of sos31(double load).
67h (15CFh)	REG15CF	7:0	Default : 0x00
	-	7:3	Reserved.
	SOS31_C2[10:8]	2:0	See description of '15CEh'.
68h (15D0h)	REG15D0	7:0	Default : 0x00
	SOS31_C3[7:0]	7:0	Coefficient of sos31(double load).
68h (15D1h)	REG15D1	7:0	Default : 0x00
	-	7:3	Reserved.
	SOS31_C3[10:8]	2:0	See description of '15D0h'.
69h (15D2h)	REG15D2	7:0	Default : 0x00
	SOS31_C4[7:0]	7:0	Coefficient of sos31(double load).
69h (15D3h)	REG15D3	7:0	Default : 0x00
	-	7:3	Reserved.
	SOS31_C4[10:8]	2:0	See description of '15D2h'.
6Ah (15D4h)	REG15D4	7:0	Default : 0x00
	SOS32_C0[7:0]	7:0	Coefficient of sos32(double load).
6Ah (15D5h)	REG15D5	7:0	Default : 0x00
	-	7:3	Reserved.
	SOS32_C0[10:8]	2:0	See description of '15D4h'.
6Bh	REG15D6	7:0	Default : 0x00

DBB1 Register (Bank = 15)				
Index (Absolute)	Mnemonic	Bit	Description	
(15D6h)	SOS32_C1[7:0]	7:0	Coefficient of sos32(double load).	
6Bh (15D7h)	REG15D7	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SOS32_C1[10:8]	2:0	See description of '15D6h'.	
6Ch (15D8h)	REG15D8	7:0	Default : 0x00	Access : R/W
	SOS32_C2[7:0]	7:0	Coefficient of sos32(double load).	
6Ch (15D9h)	REG15D9	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SOS32_C2[10:8]	2:0	See description of '15D8h'.	
6Dh (15DAh)	REG15DA	7:0	Default : 0x00	Access : R/W
	SOS32_C3[7:0]	7:0	Coefficient of sos32(double load).	
6Dh (15DBh)	REG15DB	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SOS32_C3[10:8]	2:0	See description of '15DAh'.	
6Eh (15DCh)	REG15DC	7:0	Default : 0x00	Access : R/W
	SOS32_C4[7:0]	7:0	Coefficient of sos32(double load).	
6Eh (15DDh)	REG15DD	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SOS32_C4[10:8]	2:0	See description of '15DCh'.	
6Fh (15DEh)	REG15DE	7:0	Default : 0xF5	Access : R/W
	A_SOS1_C0[7:0]	7:0	Coefficient of a_sos1(double load).	
6Fh (15DFh)	REG15DF	7:0	Default : 0x01	Access : R/W
	-	7:3	Reserved.	
	A_SOS1_C0[10:8]	2:0	See description of '15DEh'.	
70h (15E0h)	REG15E0	7:0	Default : 0x3C	Access : R/W
	A_SOS1_C1[7:0]	7:0	Coefficient of a_sos1(double load).	
70h (15E1h)	REG15E1	7:0	Default : 0x06	Access : R/W
	-	7:3	Reserved.	
	A_SOS1_C1[10:8]	2:0	See description of '15E0h'.	
71h (15E2h)	REG15E2	7:0	Default : 0x00	Access : R/W
	A_SOS1_C2[7:0]	7:0	Coefficient of a_sos1(double load).	
71h	REG15E3	7:0	Default : 0x02	Access : R/W

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
(15E3h)	-	7:3	Reserved.
	A_SOS1_C2[10:8]	2:0	See description of '15E2h'.
72h (15E4h)	REG15E4	7:0	Default : 0xEC Access : R/W
	A_SOS1_C3[7:0]	7:0	Coefficient of a_sos1(double load).
72h (15E5h)	REG15E5	7:0	Default : 0x05 Access : R/W
	-	7:3	Reserved.
	A_SOS1_C3[10:8]	2:0	See description of '15E4h'.
73h (15E6h)	REG15E6	7:0	Default : 0x00 Access : R/W
	A_SOS1_C4[7:0]	7:0	Coefficient of a_sos1(double load).
73h (15E7h)	REG15E7	7:0	Default : 0x02 Access : R/W
	-	7:3	Reserved.
	A_SOS1_C4[10:8]	2:0	See description of '15E6h'.
74h (15E8h)	REG15E8	7:0	Default : 0x00 Access : R/W
	A_SOS2_C0[7:0]	7:0	Coefficient of a_sos2(double load).
74h (15E9h)	REG15E9	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_SOS2_C0[10:8]	2:0	See description of '15E8h'.
75h (15EAh)	REG15EA	7:0	Default : 0x00 Access : R/W
	A_SOS2_C1[7:0]	7:0	Coefficient of a_sos2(double load).
75h (15EBh)	REG15EB	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_SOS2_C1[10:8]	2:0	See description of '15EAh'.
76h (15ECh)	REG15EC	7:0	Default : 0x00 Access : R/W
	A_SOS2_C2[7:0]	7:0	Coefficient of a_sos2(double load).
76h (15EDh)	REG15ED	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_SOS2_C2[10:8]	2:0	See description of '15ECh'.
77h (15EEh)	REG15EE	7:0	Default : 0x00 Access : R/W
	A_SOS2_C3[7:0]	7:0	Coefficient of a_sos2(double load).
77h (15EFh)	REG15EF	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_SOS2_C3[10:8]	2:0	See description of '15EEh'.

DBB1 Register (Bank = 15)

Index (Absolute)	Mnemonic	Bit	Description
78h (15F0h)	REG15F0	7:0	Default : 0x00
	A_SOS2_C4[7:0]	7:0	Coefficient of a_sos2(double load).
78h (15F1h)	REG15F1	7:0	Default : 0x00
	-	7:3	Reserved.
	A_SOS2_C4[10:8]	2:0	See description of '15F0h'.
79h (15F2h)	REG15F2	7:0	Default : 0x00
	A_SOS3_C0[7:0]	7:0	Coefficient of a_sos3(double load).
79h (15F3h)	REG15F3	7:0	Default : 0x00
	-	7:3	Reserved.
	A_SOS3_C0[10:8]	2:0	See description of '15F2h'.
7Ah (15F4h)	REG15F4	7:0	Default : 0x00
	A_SOS3_C1[7:0]	7:0	Coefficient of a_sos3(double load).
7Ah (15F5h)	REG15F5	7:0	Default : 0x00
	-	7:3	Reserved.
	A_SOS3_C1[10:8]	2:0	See description of '15F4h'.
7Bh (15F6h)	REG15F6	7:0	Default : 0x00
	A_SOS3_C2[7:0]	7:0	Coefficient of a_sos3(double load).
7Bh (15F7h)	REG15F7	7:0	Default : 0x00
	-	7:3	Reserved.
	A_SOS3_C2[10:8]	2:0	See description of '15F6h'.
7Ch (15F8h)	REG15F8	7:0	Default : 0x00
	A_SOS3_C3[7:0]	7:0	Coefficient of a_sos3(double load).
7Ch (15F9h)	REG15F9	7:0	Default : 0x00
	-	7:3	Reserved.
	A_SOS3_C3[10:8]	2:0	See description of '15F8h'.
7Dh (15FAh)	REG15FA	7:0	Default : 0x00
	A_SOS3_C4[7:0]	7:0	Coefficient of a_sos3(double load).
7Dh (15FBh)	REG15FB	7:0	Default : 0x00
	-	7:3	Reserved.
	A_SOS3_C4[10:8]	2:0	See description of '15FAh'.
7Fh ~ 7Fh (15FEh ~ 15FFh)	-	7:0	Default : -
	-	-	Reserved.

DBB2 Register (Bank = 16)

DBB2 Register (Bank = 16)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1600h)	REG1600	7:0	Default : 0x04	Access : R/W
	VAGC_VSYNC_CTRL[2:0]	7:5	0: PGA1/PGA2 update in any time. 1: PGA1/PGA2 update in vsync blanking. 0: PGA1/PGA2 update in any time. 1: PGA1/PGA2 update in vsync blanking. 0: From vd. 1: From riu 0: low active. 1: High active.	
	VAGC_GAIN_SLOPE	4	0: Negative gain slope 1: positive gain slope.	
	VAGC_MEAN_SEL[1:0]	3:2	Select mean. 00: 1 line. 01: 16 line. 1x: 256 line.	
	VAGC_MODE	1	Mode for positive modulation. 0: Porch. 1: Sync height (from VDAGC). Ready.	
	VAGC_ENABLE	0	0: VAGC disable 1: VAGC enable VAGC_ENABLE turn on must after setting ready.	
00h (1601h)	REG1601	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	VAGC_VSYNC_CTRL[3]	0	See description of '1600h'.	
01h (1602h)	REG1602	7:0	Default : 0x40	Access : R/W
	VAGC_LINE_CNT[7:0]	7:0	Line counter max (double load).	
01h (1603h)	REG1603	7:0	Default : 0x00	Access : R/W
	VAGC_LINE_CNT[15:8]	7:0	See description of '1602h'.	
02h (1604h)	REG1604	7:0	Default : 0xE0	Access : R/W
	VAGC_PORCH_CNT[7:0]	7:0	Porch counter max (double load).	
02h (1605h)	REG1605	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	VAGC_PORCH_CNT[8]	0	See description of '1604h'.	
03h	REG1606	7:0	Default : 0x00	Access : R/W

DBB2 Register (Bank = 16)				
Index (Absolute)	Mnemonic	Bit	Description	
(1606h)	VAGC_PEAK_CNT[7:0]	7:0	Peak counter max (double load).	
03h (1607h)	REG1607	7:0	Default : 0x0C	Access : R/W
	-	7:4	Reserved.	
	VAGC_PEAK_CNT[11:8]	3:0	See description of '1606h'.	
04h (1608h)	REG1608	7:0	Default : 0x9A	Access : R/W
	VAGC_REF[7:0]	7:0	Reference level.	
05h (160Ah)	REG160A	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.	
	VAGC_K[2:0]	2:0	Loop filter parameter. 0 -> 0. 1~7 -> 2 ⁻² ~2 ⁻⁸ .	
05h (160Bh)	REG160B	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	VAGC_OFFSET[6:0]	6:0	Vagc porch counter offset.	
06h ~ 08h (160Ch ~ 1611h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
09h (1612h)	REG1612	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VAGC_PGA1_MIN[3:0]	3:0	Pga1 min.	
09h (1613h)	REG1613	7:0	Default : 0x0A	Access : R/W
	-	7:4	Reserved.	
	VAGC_PGA1_MAX[3:0]	3:0	Pga1 max.	
0Ah (1614h)	REG1614	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	VAGC_PGA2_MIN[4:0]	4:0	Pga2 min.	
0Ah (1615h)	REG1615	7:0	Default : 0x1F	Access : R/W
	-	7:5	Reserved.	
	VAGC_PGA2_MAX[4:0]	4:0	Pga2 max.	
0Bh (1616h)	REG1616	7:0	Default : 0x00	Access : R/W
	VAGC_VGA_MIN[7:0]	7:0	Vga min (double load).	
0Bh (1617h)	REG1617	7:0	Default : 0x80	Access : R/W
	VAGC_VGA_MIN[15:8]	7:0	See description of '1616h'.	

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description
0Ch (1618h)	REG1618	7:0	Default : 0xFF Access : R/W
	VAGC_VGA_MAX[7:0]	7:0	Vga max (double load).
0Ch (1619h)	REG1619	7:0	Default : 0x7F Access : R/W
	VAGC_VGA_MAX[15:8]	7:0	See description of '1618h'.
0Dh ~ 0Eh (161Ah ~ 161Dh)	-	7:0	Default : - Access : -
	-	-	Reserved.
10h (1620h)	REG1620	7:0	Default : 0x00 Access : RO
	VAGC_MEAN0[7:0]	7:0	mean: 1 line.
11h (1622h)	REG1622	7:0	Default : 0x00 Access : RO
	VAGC_MEAN16[7:0]	7:0	mean: 16 line.
12h (1624h)	REG1624	7:0	Default : 0x00 Access : RO
	VAGC_MEAN256[7:0]	7:0	mean: 256 line.
13h (1626h)	REG1626	7:0	Default : 0x00 Access : RO
	VAGC_DIFF[7:0]	7:0	Diff.
13h (1627h)	REG1627	7:0	Default : 0x00 Access : RO
	-	7:2	Reserved.
	VAGC_DIFF[9:8]	1:0	See description of '1626h'.
14h (1628h)	REG1628	7:0	Default : 0x00 Access : RO
	VAGC_VGA[7:0]	7:0	Tuner vga value.
14h (1629h)	REG1629	7:0	Default : 0x00 Access : RO
	VAGC_VGA[15:8]	7:0	See description of '1628h'.
15h (162Ah)	REG162A	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	VAGC_PGA1A[3:0]	3:0	PGA1a.
15h (162Bh)	REG162B	7:0	Default : 0x00 Access : RO
	-	7:5	Reserved.
	VAGC_PGA2A[4:0]	4:0	PGA2a.
16h (162Ch)	REG162C	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	VAGC_PGA1B[3:0]	3:0	PGA1b.
16h (162Dh)	REG162D	7:0	Default : 0x00 Access : RO
	-	7:5	Reserved.

DBB2 Register (Bank = 16)				
Index (Absolute)	Mnemonic	Bit	Description	
	VAGC_PGA2B[4:0]	4:0	PGA2b.	
17h (162Eh)	REG162E	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	VAGC_PGA1C[3:0]	3:0	PGA1c.	
17h (162Fh)	REG162F	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	VAGC_PGA2C[4:0]	4:0	PGA2c.	
18h ~ 18h (1630h ~ 1631h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
23h (1646h)	REG1646	7:0	Default : 0x00	Access : R/W
	VAGC_VGA_THR[7:0]	7:0	Vga thr (double load).	
23h (1647h)	REG1647	7:0	Default : 0x80	Access : R/W
	VAGC_VGA_THR[15:8]	7:0	See description of '1646h'.	
24h ~ 27h (1648h ~ 164Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
2Ch (1658h)	REG1658	7:0	Default : 0x00	Access : R/W
	IF_RATE[7:0]	7:0	If_mixer rate <21,22> (double load).	
2Ch (1659h)	REG1659	7:0	Default : 0x00	Access : R/W
	IF_RATE[15:8]	7:0	See description of '1658h'.	
2Dh (165Ah)	REG165A	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	IF_RATE[20:16]	4:0	See description of '1658h'.	
2Eh (165Ch)	REG165C	7:0	Default : 0x00	Access : R/W
	A_DAGC_SEL	7	1: Input from a_lpf_up, 0: input from a_sos.	
	A_LPF_BG_SEL	6	1: Input from a_bp_ntsc, 0: input from a_bp_pal.	
	ACI_REJ_NTSC_SEL[5:4]	5:4	0: Aci_rej_out 1: nyq_slp_out1 2: nyq_slp_out2 3: mixer_out_i.	
	-	3:2	Reserved.	
	A_DC_FREEZE	1	Freeze audio dc_notch.	
	V_DC_FREEZE	0	Freeze video dc_notch.	

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description
2Eh (165Dh)	REG165D	7:0	Default : 0x00
	-	7:5	Reserved.
	FILTER_DBG_SEL[12:8]	4:0	
2Fh (165Eh)	REG165E	7:0	Default : 0x00
	BYPASS_A_SOS1	7	
	BYPASS_A_NOTCH	6	
	BYPASS_CO_A_REJ_NTSC	5	
	BYPASS_CO_A_REJ	4	
	BYPASS_A_SOS_T1	3	Bypass audio sos.
	BYPASS_A_NOTCH_T1	2	Bypass audio notch.
	BYPASS_V_SOS_T1	1	Bypass video sos.
	BYPASS_V_NOTCH_T1	0	Bypass video notch.
2Fh (165Fh)	REG165F	7:0	Default : 0x00
	-	7:2	Reserved.
	BYPASS_A_LPF_BG	1	
	BYPASS_2ND_A_BP	0	
30h (1660h)	REG1660	7:0	Default : 0x00
	V_NOTCH_T1_COEF0[7:0]	7:0	Video notch coefficient (13,11) (double load).
30h (1661h)	REG1661	7:0	Default : 0x00
	-	7:5	Reserved.
	V_NOTCH_T1_COEF0[12:8]	4:0	See description of '1660h'.
31h (1662h)	REG1662	7:0	Default : 0x00
	V_NOTCH_T1_COEF1[7:0]	7:0	Video notch coefficient (13,11) (double load).
31h (1663h)	REG1663	7:0	Default : 0x00
	-	7:5	Reserved.
	V_NOTCH_T1_COEF1[12:8]	4:0	See description of '1662h'.
32h (1664h)	REG1664	7:0	Default : 0x00
	V_NOTCH_T1_COEF2[7:0]	7:0	Video notch coefficient (13,11) (double load).
32h (1665h)	REG1665	7:0	Default : 0x00
	-	7:5	Reserved.
	V_NOTCH_T1_COEF2[12:8]	4:0	See description of '1664h'.
33h (1666h)	REG1666	7:0	Default : 0x00
	V_SOS_T1_COEF0[7:0]	7:0	Video sos coefficient (13,11) (double load).

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description
33h (1667h)	REG1667	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	V_SOS_T1_COEF0[12:8]	4:0	See description of '1666h'.
34h (1668h)	REG1668	7:0	Default : 0x00 Access : R/W
	V_SOS_T1_COEF1[7:0]	7:0	Video sos coefficient (13,11) (double load).
34h (1669h)	REG1669	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	V_SOS_T1_COEF1[12:8]	4:0	See description of '1668h'.
35h (166Ah)	REG166A	7:0	Default : 0x00 Access : R/W
	V_SOS_T1_COEF2[7:0]	7:0	Video sos coefficient (13,11) (double load).
35h (166Bh)	REG166B	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	V_SOS_T1_COEF2[12:8]	4:0	See description of '166Ah'.
36h (166Ch)	REG166C	7:0	Default : 0x00 Access : R/W
	V_SOS_T1_COEF3[7:0]	7:0	Video sos coefficient (13,11) (double load).
36h (166Dh)	REG166D	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	V_SOS_T1_COEF3[12:8]	4:0	See description of '166Ch'.
37h (166Eh)	REG166E	7:0	Default : 0x00 Access : R/W
	V_SOS_T1_COEF4[7:0]	7:0	Video sos coefficient (13,11) (double load).
37h (166Fh)	REG166F	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	V_SOS_T1_COEF4[12:8]	4:0	See description of '166Eh'.
38h (1670h)	REG1670	7:0	Default : 0x00 Access : R/W
	A_NOTCH_T1_COEF0[7:0]	7:0	Audio notch coefficient (13,11) (double load).
38h (1671h)	REG1671	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	A_NOTCH_T1_COEF0[12:8]	4:0	See description of '1670h'.
39h (1672h)	REG1672	7:0	Default : 0x00 Access : R/W
	A_NOTCH_T1_COEF1[7:0]	7:0	Audio notch coefficient (13,11) (double load).
39h (1673h)	REG1673	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	A_NOTCH_T1_COEF1[12:8]	4:0	See description of '1672h'.

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description
3Ah (1674h)	REG1674	7:0	Default : 0x00
	A_NOTCH_T1_COEF2[7:0]	7:0	Audio notch coefficient (13,11) (double load).
3Ah (1675h)	REG1675	7:0	Default : 0x00
	-	7:5	Reserved.
	A_NOTCH_T1_COEF2[12:8]	4:0	See description of '1674h'.
3Bh (1676h)	REG1676	7:0	Default : 0x00
	A_SOS_T1_COEF0[7:0]	7:0	Audio sos coefficient (13,11) (double load).
3Bh (1677h)	REG1677	7:0	Default : 0x00
	-	7:5	Reserved.
	A_SOS_T1_COEF0[12:8]	4:0	See description of '1676h'.
3Ch (1678h)	REG1678	7:0	Default : 0x00
	A_SOS_T1_COEF1[7:0]	7:0	Audio sos coefficient (13,11) (double load).
3Ch (1679h)	REG1679	7:0	Default : 0x00
	-	7:5	Reserved.
	A_SOS_T1_COEF1[12:8]	4:0	See description of '1678h'.
3Dh (167Ah)	REG167A	7:0	Default : 0x00
	A_SOS_T1_COEF2[7:0]	7:0	Audio sos coefficient (13,11) (double load).
3Dh (167Bh)	REG167B	7:0	Default : 0x00
	-	7:5	Reserved.
	A_SOS_T1_COEF2[12:8]	4:0	See description of '167Ah'.
3Eh (167Ch)	REG167C	7:0	Default : 0x00
	A_SOS_T1_COEF3[7:0]	7:0	Audio sos coefficient (13,11) (double load).
3Eh (167Dh)	REG167D	7:0	Default : 0x00
	-	7:5	Reserved.
	A_SOS_T1_COEF3[12:8]	4:0	See description of '167Ch'.
3Fh (167Eh)	REG167E	7:0	Default : 0x00
	A_SOS_T1_COEF4[7:0]	7:0	Audio sos coefficient (13,11) (double load).
3Fh (167Fh)	REG167F	7:0	Default : 0x00
	-	7:5	Reserved.
	A_SOS_T1_COEF4[12:8]	4:0	See description of '167Eh'.
40h (1680h)	REG1680	7:0	Default : 0x00
	A_NOTCH_COEF0[7:0]	7:0	Audio notch coefficient (11,9) (double load).
40h	REG1681	7:0	Default : 0x00

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description
(1681h)	-	7:3	Reserved.
	A_NOTCH_COEF0[10:8]	2:0	See description of '1680h'.
41h (1682h)	REG1682	7:0	Default : 0x00 Access : R/W
	A_NOTCH_COEF1[7:0]	7:0	Audio notch coefficient (11,9) (double load).
41h (1683h)	REG1683	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_NOTCH_COEF1[10:8]	2:0	See description of '1682h'.
42h (1684h)	REG1684	7:0	Default : 0x00 Access : R/W
	A_NOTCH_COEF2[7:0]	7:0	Audio notch coefficient (11,9) (double load).
42h (1685h)	REG1685	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_NOTCH_COEF2[10:8]	2:0	See description of '1684h'.
43h (1686h)	REG1686	7:0	Default : 0x00 Access : R/W
	A_SOS1_COEF0[7:0]	7:0	Audio sos coefficient (11,9) (double load).
43h (1687h)	REG1687	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_SOS1_COEF0[10:8]	2:0	See description of '1686h'.
44h (1688h)	REG1688	7:0	Default : 0x00 Access : R/W
	A_SOS1_COEF1[7:0]	7:0	Audio sos coefficient (11,9) (double load).
44h (1689h)	REG1689	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_SOS1_COEF1[10:8]	2:0	See description of '1688h'.
45h (168Ah)	REG168A	7:0	Default : 0x00 Access : R/W
	A_SOS1_COEF2[7:0]	7:0	Audio sos coefficient (11,9) (double load).
45h (168Bh)	REG168B	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_SOS1_COEF2[10:8]	2:0	See description of '168Ah'.
46h (168Ch)	REG168C	7:0	Default : 0x00 Access : R/W
	A_SOS1_COEF3[7:0]	7:0	Audio sos coefficient (11,9) (double load).
46h (168Dh)	REG168D	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	A_SOS1_COEF3[10:8]	2:0	See description of '168Ch'.
47h	REG168E	7:0	Default : 0x00 Access : R/W

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description
(168Eh)	A_SOS1_COEF4[7:0]	7:0	Audio sos coefficient (11,9) (double load).
47h (168Fh)	REG168F	7:0	Default : 0x00
	-	7:3	Reserved.
	A_SOS1_COEF4[10:8]	2:0	See description of '168Eh'.
50h (16A0h)	REG16A0	7:0	Default : 0x00
	-	7:4	Reserved.
	AAGC_PEAK_MEAN_SEL	3	
	AAGC_PGA2_IGN_PGA1	2	
	AAGC_PGA1_IGN_PGA2	1	
	AAGC_ENABLE	0	0: AAGC disable 1: AAGC enable AAGC_ENABLE turn on must after setting ready.
51h (16A2h)	REG16A2	7:0	Default : 0x00
	-	7:6	Reserved.
	AAGC_LINE_CNT[5:0]	5:0	AAGC line counter max.
52h (16A4h)	-	7:0	Default : -
	-	-	Reserved.
52h (16A5h)	REG16A5	7:0	Default : 0x00
	AAGC_DEC[7:0]	7:0	Decimation (for mean). <8,0>.
53h ~ 53h (16A6h ~ 16A7h)	-	7:0	Default : -
	-	-	Reserved.
54h (16A8h)	REG16A8	7:0	Default : 0x00
	-	7:4	Reserved.
	AAGC_PGA1_MIN[3:0]	3:0	Pga1 min.
54h (16A9h)	REG16A9	7:0	Default : 0x0A
	-	7:4	Reserved.
	AAGC_PGA1_MAX[3:0]	3:0	Pga1 max.
55h (16AAh)	REG16AA	7:0	Default : 0x00
	-	7:5	Reserved.
	AAGC_PGA2_MIN[4:0]	4:0	Pga2 min.
55h (16ABh)	REG16AB	7:0	Default : 0x1F
	-	7:5	Reserved.

DBB2 Register (Bank = 16)				
Index (Absolute)	Mnemonic	Bit	Description	
	AAGC_PGA2_MAX[4:0]	4:0	Pga2 max.	
56h (16ACh)	REG16AC	7:0	Default : 0x18	Access : R/W
	-	7	Reserved.	
	AAGC_MEAN_MIN[6:0]	6:0	Mean min.	
56h (16ADh)	REG16AD	7:0	Default : 0x30	Access : R/W
	-	7	Reserved.	
	AAGC_MEAN_MAX[6:0]	6:0	Mean max.	
57h (16AEh)	REG16AE	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	AAGC_MEAN[6:0]	6:0	Mean.	
58h (16B0h)	REG16B0	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	AAGC_PEAKMEAN[6:0]	6:0	Peak mean.	
59h (16B2h)	REG16B2	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	AAGC_PGA1[3:0]	3:0	PGA1.	
59h (16B3h)	REG16B3	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	AAGC_PGA2[4:0]	4:0	PGA2.	
5Ah (16B4h)	REG16B4	7:0	Default : 0xFF	Access : R/W
	AAGC_CNT[7:0]	7:0	AAGC counter max (double load).	
5Ah (16B5h)	REG16B5	7:0	Default : 0x3F	Access : R/W
	AAGC_CNT[15:8]	7:0	See description of '16B4h'.	
5Bh (16B6h)	REG16B6	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	AAGC_CNT[20:16]	4:0	See description of '16B4h'.	
70h (16E0h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
70h (16E1h)	REG16E1	7:0	Default : 0x00	Access : R/W
	DEBUG2_EN	7		
	TESTBUS_INV	6		
	-	5:0	Reserved.	
71h ~ 71h (16E2h ~	-	7:0	Default : -	
	-	-	Reserved.	

DBB2 Register (Bank = 16)

Index (Absolute)	Mnemonic	Bit	Description
16E3h)			

DBB3 Register (Bank = 1B)

DBB3 Register (Bank = 1B)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1B00h)	REG1B00	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	VDAGC1_BYPASS	1	1=vdagc1 bypass.	
	VDAGC1_ENABLE	0	1=vdagc1 enable.	
00h (1B01h)	REG1B01	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	VDAGC2_BYPASS	1	1=vdagc2 bypass.	
	VDAGC2_ENABLE	0	1=vdagc2 enable.	
01h ~ 02h (1B02h ~ 1B05h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
03h (1B06h)	REG1B06	7:0	Default : 0x26	Access : R/W
	-	7:6	Reserved.	
	VDAGC1_REF[5:0]	5:0	Vdagc1 ref.	
03h (1B07h)	REG1B07	7:0	Default : 0x26	Access : R/W
	-	7:6	Reserved.	
	VDAGC2_REF[5:0]	5:0	Vdagc2 ref.	
04h (1B08h)	REG1B08	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.	
	VDAGC1_LEVEL_SHIFT[2:0]	2:0	Vdagc1 level shift.	
04h (1B09h)	REG1B09	7:0	Default : 0x04	Access : R/W
	-	7:3	Reserved.	
	VDAGC2_LEVEL_SHIFT[2:0]	2:0	Vdagc2 level shift.	
05h (1B0Ah)	REG1B0A	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	VDAGC1_RATIO[2:0]	2:0	Vdagc1 lpf update ratio.	
05h (1B0Bh)	REG1B0B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	VDAGC2_RATIO[2:0]	2:0	Vdagc2 lpf update ratio.	
06h (1B0Ch)	REG1B0C	7:0	Default : 0x00	Access : R/W
	VDAGC1_PEAK_CNT[7:0]	7:0	Vdagc1 peak counter max(double load).	
06h	REG1B0D	7:0	Default : 0x0C	Access : R/W

DBB3 Register (Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description
(1B0Dh)	-	7:4	Reserved.
	VDAGC1_PEAK_CNT[11:8]	3:0	See description of '1B0Ch'.
07h (1B0Eh)	REG1B0E	7:0	Default : 0x00 Access : R/W
	VDAGC2_PEAK_CNT[7:0]	7:0	Vdgc2 peak counter max(double load).
07h (1B0Fh)	REG1B0F	7:0	Default : 0x0C Access : R/W
	-	7:4	Reserved.
	VDAGC2_PEAK_CNT[11:8]	3:0	See description of '1B0Eh'.
08h (1B10h)	REG1B10	7:0	Default : 0xF8 Access : R/W
	VDAGC1_PORCH_CNT[7:0]	7:0	Vdgc1 porch counter max(double load).
08h (1B11h)	REG1B11	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	VDAGC1_PORCH_CNT[8]	0	See description of '1B10h'.
09h (1B12h)	REG1B12	7:0	Default : 0xF8 Access : R/W
	VDAGC2_PORCH_CNT[7:0]	7:0	Vdgc2 porch counter max(double load).
09h (1B13h)	REG1B13	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	VDAGC2_PORCH_CNT[8]	0	See description of '1B12h'.
0Ah (1B14h)	REG1B14	7:0	Default : 0x00 Access : RO
	VDAGC1_MEAN[7:0]	7:0	Vdgc1 mean.
0Ah (1B15h)	REG1B15	7:0	Default : 0x00 Access : RO
	VDAGC1_MEAN[15:8]	7:0	See description of '1B14h'.
0Bh (1B16h)	REG1B16	7:0	Default : 0x00 Access : RO
	VDAGC1_VAR[7:0]	7:0	Vdgc1 variance.
0Bh (1B17h)	REG1B17	7:0	Default : 0x00 Access : RO
	VDAGC1_VAR[15:8]	7:0	See description of '1B16h'.
0Ch (1B18h)	REG1B18	7:0	Default : 0x00 Access : RO
	VDAGC2_MEAN[7:0]	7:0	Vdgc2 mean.
0Ch (1B19h)	REG1B19	7:0	Default : 0x00 Access : RO
	VDAGC2_MEAN[15:8]	7:0	See description of '1B18h'.
0Dh (1B1Ah)	REG1B1A	7:0	Default : 0x00 Access : RO
	VDAGC2_VAR[7:0]	7:0	Vdgc2 variance.
0Dh (1B1Bh)	REG1B1B	7:0	Default : 0x00 Access : RO
	VDAGC2_VAR[15:8]	7:0	See description of '1B1Ah'.

DBB3 Register (Bank = 1B)				
Index (Absolute)	Mnemonic	Bit	Description	
0Eh (1B1Ch)	REG1B1C	7:0	Default : 0x00	Access : RO
	VDAGC1_GAIN[7:0]	7:0	Vdgc1 internal gain.	
0Eh (1B1Dh)	REG1B1D	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	VDAGC1_GAIN[13:8]	5:0	See description of '1B1Ch'.	
0Fh (1B1Eh)	REG1B1E	7:0	Default : 0x00	Access : RO
	VDAGC2_GAIN[7:0]	7:0	Vdgc2 internal gain.	
0Fh (1B1Fh)	REG1B1F	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	VDAGC2_GAIN[13:8]	5:0	See description of '1B1Eh'.	
10h (1B20h)	REG1B20	7:0	Default : 0x00	Access : RO
	VDAGC1_SYNCHEIGHT[7:0]	7:0	Vdgc1 sync height.	
10h (1B21h)	REG1B21	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	VDAGC1_VSYNC	4	Vdgc1 vsync coast pulse (high active).	
	-	3:1	Reserved.	
	VDAGC1_SYNCHEIGHT[8]	0	See description of '1B20h'.	
11h (1B22h)	REG1B22	7:0	Default : 0x00	Access : RO
	VDAGC2_SYNCHEIGHT[7:0]	7:0	Vdgc2 sync height.	
11h (1B23h)	REG1B23	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	VDAGC2_VSYNC	4	Vdgc2 vsync coast pulse (high active).	
	-	3:1	Reserved.	
	VDAGC2_SYNCHEIGHT[8]	0	See description of '1B22h'.	
12h (1B24h)	REG1B24	7:0	Default : 0x00	Access : RO
	VDAGC1_LPF_DELAY_0[7:0]	7:0	Vdgc1 lpf delay line first element.	
12h (1B25h)	REG1B25	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	VDAGC1_LPF_DELAY_0[8]	0	See description of '1B24h'.	
13h (1B26h)	REG1B26	7:0	Default : 0x00	Access : RO
	VDAGC2_LPF_DELAY_0[7:0]	7:0	Vdgc2 lpf delay line first element.	
13h (1B27h)	REG1B27	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	

DBB3 Register (Bank = 1B)				
Index (Absolute)	Mnemonic	Bit	Description	
	VDAGC2_LPF_DELAY_0[8]	0	See description of '1B26h'.	
14h (1B28h)	REG1B28	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	VDAGC1_OFFSET[6:0]	6:0	Vdgc1 porch counter offset.	
14h (1B29h)	REG1B29	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	VDAGC2_OFFSET[6:0]	6:0	Vdgc2 porch counter offset.	
24h ~ 27h (1B48h ~ 1B4Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
40h (1B80h)	REG1B80	7:0	Default : 0x02	Access : R/W
	-	7:3	Reserved.	
	ADAGC_PEAK_MEAN_SEL	2	1=select peak.	
	ADAGC_BYPASS	1	1=adagc1 bypass.	
	ADAGC_ENABLE	0	1=adagc1 enable.	
40h (1B81h)	REG1B81	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ADAGC_K[2:0]	2:0	1~7:2 ⁻¹ ~2 ⁻⁷ .	
41h (1B82h)	REG1B82	7:0	Default : 0x00	Access : R/W
	ADAGC_CNT[7:0]	7:0	Adagc counter max(double load).	
41h (1B83h)	REG1B83	7:0	Default : 0x01	Access : R/W
	ADAGC_CNT[15:8]	7:0	See description of '1B82h'.	
42h (1B84h)	REG1B84	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	ADAGC_CNT[20:16]	4:0	See description of '1B82h'.	
43h (1B86h)	REG1B86	7:0	Default : 0x00	Access : R/W
	ADAGC_DEC[7:0]	7:0	Adagc decimation.	
43h (1B87h)	REG1B87	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ADAGC_LINE_CNT[5:0]	5:0	Adagc line counter max.	
44h (1B88h)	REG1B88	7:0	Default : 0x50	Access : R/W
	ADAGC_REF[7:0]	7:0	Adagc ref.	
45h	REG1B8A	7:0	Default : 0x00	Access : R/W

DBB3 Register (Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description
(1B8Ah)	-	7:1	Reserved.
	ADAGC_GAIN_OREN	0	1=adagc gain overwrite enable.
46h (1B8Ch)	REG1B8C	7:0	Default : 0x00 Access : R/W
	ADAGC_GAIN_OV[7:0]	7:0	Adagc gain overwrite value(double load).
46h (1B8Dh)	REG1B8D	7:0	Default : 0x01 Access : R/W
	ADAGC_GAIN_OV[15:8]	7:0	See description of '1B8Ch'.
50h (1BA0h)	REG1BA0	7:0	Default : 0x00 Access : RO
	ADAGC_MEAN[7:0]	7:0	Adagc mean.
50h (1BA1h)	REG1BA1	7:0	Default : 0x00 Access : RO
	ADAGC_PEAK[7:0]	7:0	Adagc peak.
51h (1BA2h)	REG1BA2	7:0	Default : 0x00 Access : RO
	ADAGC_GAIN[7:0]	7:0	Adagc gain.
51h (1BA3h)	REG1BA3	7:0	Default : 0x00 Access : RO
	ADAGC_GAIN[15:8]	7:0	See description of '1BA2h'.

OSD Register (Bank = 1C)

OSD Register (Bank = 1C)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1C01h)	REG1C01	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	00A_DBFTYPEZ	2	DBL[1] 01[2]. [0]: DBL=Double Buffer Load. When h0000[9]=0. 0: Keep old register value. 1: Automatically load data at VSYNC blanking. When h0000[9]=1. 0: Load new data (auto reset to 00 when loading completes). 1: Reserved.	
	009_IDBFLOAD	1	DBL[0] 01[1]. [0]: DBL=Double Buffer Load. When h0000[10]=0. 0: Keep old register value. 1: Load new data (auto reset to 00 when loading completes). When h0000[10]=1. 0: Automatically load data at VSYNC blanking. 1: Reserved.	
	008_ENA_DBF	0	[0]: DB_EN=Double Buffer Enable. 01[0]. 0: Disable. 1: Enable.	
01h (1C02h)	REG1C02	7:0	Default : 0x00	Access : R/W
	010_IN_OHSTA_L[7:0]	7:0	[7:0]:OHSTA[7:0]=OSD windows Horizontal Start position (pixel) (lower 8bits). 02[7:0].	
01h (1C03h)	REG1C03	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	018_IN_OHSTA_H[2:0]	2:0	[2:0]:OHSTA[10:8]=OSD windows Horizontal Start position (pixel) (higher 3 bits). 03[2:0].	
02h (1C04h)	REG1C04	7:0	Default : 0x00	Access : R/W
	020_IN_OVSTA_L[7:0]	7:0	[7:0]:OVSTA[7:0]=OSD windows Vertical Start position (line) (lower 8bits).	

OSD Register (Bank = 1C)				
Index (Absolute)	Mnemonic	Bit	Description	
			04[7:0].	
02h (1C05h)	REG1C05	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	028_IN_OVSTA_H[1:0]	1:0	[1:0]:OVSTA[9:8]=OSD windows Vertical Start position (line) (higher 2bits). 05[2:0].	
03h (1C06h)	REG1C06	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	030_IN_OSDW[6:0]	6:0	[6:0]:OSDW[6:0]=OSD windows Width (OSDW + 1 (column)), maximum 128 columns. 06[6:0].	
03h (1C07h)	REG1C07	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	038_IN_OSDH[5:0]	5:0	[5:0]:OSDH[5:0]=OSD windows Height (OSDH + 1 (row)), maximum 64 rows. 07[5:0].	
04h (1C08h)	REG1C08	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	040_OHSPA[6:0]	6:0	[6:0]:OHSPA[6:0]=OSD windows Horizontal Space Start position (OHSPA + 1 (column)). 08[6:0].	
04h (1C09h)	REG1C09	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	048_OVSPA[5:0]	5:0	[5:0]:OVSPA[5:0]=OSD windows Vertical Space Start position. (OVSPA + 1 (row)). 09[5:0].	
05h (1C0Ah)	REG1C0A	7:0	Default : 0x00	Access : R/W
	050_OSPW[7:0]	7:0	[7:0]:OSPW[7:0]=OSD Space Width (8 * OSPW (line)). 0A[7:0].	
05h (1C0Bh)	REG1C0B	7:0	Default : 0x00	Access : R/W
	058_OSPH[7:0]	7:0	[7:0]:OSPH[7:0]=OSD Space Height (8 * OSPH (line)). 0B[7:0].	
06h (1C0Ch)	REG1C0C	7:0	Default : 0x00	Access : R/W
	060_IN_IOSDC1[7:0]	7:0	0C[7:0]: iosdc1.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>[7:6]:OVS[1:0]=OSD Vertical Scaling. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels. [5:4]:OHS[1:0]=OSD Horizontal Scaling. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels. [0]: MWIN=OSD Main Window display. 0: Main window off. 1: Main window on.</p>
06h (1C0Dh)	REG1C0D	7:0	Default : 0x00 Access : R/W
	068_IOSDC2[7:0]	7:0	<p>0D[7:0]:iosdc2. [7]: HDE_SEL=OSD position relation select. 0: OSD position relate to HSYNC. 1: OSD position relate to HDE. [5]: BDALL=OSD character Border Direction. 0: Border with all direction. 1: Border with bottom-right direction. [4]: BDW=OSD character Border Width control. 0: One pixel with for all scale. 1: Scale with OVS[1:0] and OHS[1:0]. [3:0]:BCLR[3:0]=OSD Border Color index. 0000: Color index 0. 0001: Color index 1. .. 1111: Color index 15.</p>
07h (1C0Eh)	REG1C0E	7:0	Default : 0x00 Access : R/W
	070_IOSDC3[7:0]	7:0	<p>Window Shadow information. 0E[7:0]. [5]: SHALL=OSD Shadow with All Direction. 0: Shadow with Bottom-Right direction (shadow). 1: Shadow with all direction (border). [4]: SDC=OSD Window Shadow Control. 0: Off. 1: On. [3:0]:SCLR[3:0]=OSD window Shaow Color index.</p>

OSD Register (Bank = 1C)				
Index (Absolute)	Mnemonic	Bit	Description	
			0000: Color index 0. 0001: Color index 1. .. 1111: Color index 15.	
07h (1C0Fh)	REG1C0F	7:0	Default : 0x00	Access : R/W
	078_OSHC[7:0]	7:0	Window Shadow Control. 0F[7:0]. [7:4]: vshad_bd_height=OSD Shadow Height. [3:0]: hshad_bd_width=OSD Shadow Width.	
08h (1C10h)	REG1C10	7:0	Default : 0x00	Access : R/W
	080_IOSDC4[7:0]	7:0	OSD control. 10[7:0]. [7]: Line_shift_en=OSD line shift Enable (Please refer to h0022 bit 12~10 LINE_SHIFT_VAL). [6]: Field_pol=OSD line shift Field polarity. [5]: Field_sub=. [4]: En_m4c=4 Color Font Enable. 0: Disable. 1: Enable. [3]: Font10h_sel=OSD font high control. 0: Font height is 18. 1: Font height is 10. [2]: En_m8c=8 Color Font Enable. 0: Disable. 1: Enable. [1]: Transp_en=OSD Transparency Enable. 0: No transparency. 1: Color index which hit OSD Color index for transparency[2:0] is transparent of 8 color palette/Color index which hit OSD Color index for transparency[3:0] is transparent of 16 color palette. (Please refer to h0021 bit 3~0 OSD Color index for transparency). [0]: T16c=OSD 16 Color Palette select. 0: 8 color palette. 1: 16 color palette.	
09h (1C12h)	REG1C12	7:0	Default : 0x00	Access : R/W
	090_OOFFSET[7:0]	7:0	[7]: COFFS_SEL: OSD Code buffer Offset Select. 12[7:0].	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			0: Use OSDW[6:0] as offset. 1: Use OOFFS[6:0] as offset. [6:0]:OOFFS[6:0]=OSD code buffer Offset value.
09h (1C13h)	REG1C13	7:0	Default : 0x00 Access : R/W
	098_IN_OSDBA_L[7:0]	7:0	[7:0]:OSDBA[7:0]=OSD code Base Address (lower 8 bits). 13[7:0].
0Ah (1C14h)	REG1C14	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	0A0_IN_OSDBA_H[2:0]	2:0	[2:0]:OSDBA[10:8]=OSD code Base Address (higher 3 bits). 14[2:0]. Please refer h0022 bit 15 CCRAM1024X2. When CCRAM1024X2 = 0, OSDBA[10:0] is programming from 0 to 7FFh. When CCRAM1024X2 = 1, OSDBA[9:0] is programming from 0 to 3FFh and OSDBA[10] is programming to select low or high part code/attribute SRAM).
0Ah (1C15h)	REG1C15	7:0	Default : 0x00 Access : R/W
	0AE_GVS[1:0]	7:6	[7:6]:GVS[1:0]=Gradually color Vertical Scaling. 15[7:6]. 00: Vertical normal size. 01: Vertical enlarged x2 by repeated pixels. 10: Vertical enlarged x3 by repeated pixels. 11: Vertical enlarged x4 by repeated pixels.
	0AC_GHS[1:0]	5:4	[5:4]:GHS[1:0]=Gradually color Horizontal Scaling. 15[5:4]. 00: Horizontal normal size. 01: Horizontal enlarged x2 by repeated pixels. 10: Horizontal enlarged x3 by repeated pixels. 11: Horizontal enlarged x4 by repeated pixels.
	0AB_EN_TG	3	[3]: GRAD=Enable OSD Gradually Color Function. 15[3]. 0: Disable. 1: Enable.
	0AA_ADC_PG	2	[2]: ADC_PG=ADC Pattern Generator Select.15[2]. 0: Normal. 1: ADC.
	0A8_SVM_SEL[1:0]	1:0	[1:0]:SVM_SEL=SVM Mask signal Select.15[1:0].

OSD Register (Bank = 1C)				
Index (Absolute)	Mnemonic	Bit	Description	
			00: Original active signal. 01: 2T early. 10: 4T early. 11: 6T early.	
0Bh (1C16h)	REG1C16	7:0	Default : 0x00	Access : R/W
	0B0_GCLRC_REG[7:0]	7:0	OSD Starting Gradually Color. 16[7:0]. [7]: GCS=Gradually Color Source. 0: Use this register bit[5:0] to define color. 1: Use Bank 00 background color to define color. [5:4]:RCLR[1:0]=Red starting gradually Color. 00: Red color is 00h. 01: Red color is 55h. 10: Red color is Aah. 11: Red color is FFh. [3:2]:GCLR[1:0]=Green starting gradually Color. 00: Green color is 00h. 01: Green color is 55h. 10: Green color is AAh. 11: Green color is FFh. [1:0]:BCLR[1:0]=Blue starting gradually Color. 00: Blue color is 00h. 01: Blue color is 55h. 10: Blue color is AAh. 11: Blue color is FFh.	
0Bh (1C17h)	REG1C17	7:0	Default : 0x00	Access : R/W
	0B8_HGCR_REG[7:0]	7:0	OSD H R Gradually Color. 17[7:0]. [15]: SR=Sign bit of Red color. 0: Increase. 1: Decrease. [14]: IRH=Inverse bit of Red color. 0: Normal. 1: Invert. [13:8]:R_GRADH[5:0]=Increase/Decrease value of Red color.	
0Ch (1C18h)	REG1C18	7:0	Default : 0x00	Access : R/W
	0C0_HGCG_REG[7:0]	7:0	OSD H G Gradually Color. 18[7:0].	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			[7]: SG=Sign bit of Green color. 0: Increase. 1: Decrease. [6]: IGH=Inverse bit of Green color. 0: Normal. 1: Invert. [5:0]:G_GRADH[5:0]=Increase/Decrease value of Green color.
0Ch (1C19h)	REG1C19	7:0	Default : 0x00 Access : R/W
	0C8_HGCB_REG[7:0]	7:0	OSD H B Gradually Color. 19[7:0]. [15]: SB=Sign bit of Blue color. 0: Increase. 1: Decrease. [14]: IBH=Inverse bit of Blue color. 0: Normal. 1: Invert. [13:8]:B_GRADH[5:0]=Increase/Decrease value of Blue color.
0Dh (1C1Ah)	REG1C1A	7:0	Default : 0x00 Access : R/W
	0D0_HRSTEP_REG[7:0]	7:0	OSD Horizontal R Step. 1a[7:0]. [7:0]:HGRADSR[7:0]=Horizontal Gradually Step of Red color.
0Dh (1C1Bh)	REG1C1B	7:0	Default : 0x00 Access : R/W
	0D8_HGSTEP_REG[7:0]	7:0	OSD Horizontal G Step. 1b[7:0]. [7:0]:HGRADSG[7:0]=Horizontal Gradually Step of Green color.
0Eh (1C1Ch)	REG1C1C	7:0	Default : 0x00 Access : R/W
	0E0_HBSTEP_REG[7:0]	7:0	OSD Horizontal B Step. 1c[7:0]. [7:0]:HGRADSB[7:0]=Horizontal Gradually Step of Blue color.
0Eh (1C1Dh)	REG1C1D	7:0	Default : 0x00 Access : R/W
	0E8_VGCR_REG[7:0]	7:0	OSD V R Gradually Color. 1d[7:0]. [7]: SR=Sign bit of Red color.

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			0: Increase. 1: Decrease. [6]: IRV=Inverse bit of Red color. 0: Normal. 1: Invert. [5:0]:R_GRADV[5:0]=Increase/Decrease value of Red color.
0Fh (1C1Eh)	REG1C1E	7:0	Default : 0x00
	0F0_VGCG_REG[7:0]	7:0	Access : R/W OSD V G Gradually Color. 1e[7:0]. [7]: SG=Sign bit of Green color. 0: Increase. 1: Decrease. [6]: IGV=Inverse bit of Green color. 0: Normal. 1: Invert. [5:0]:G_GRADV[5:0]=Increase/Decrease value of Green color.
0Fh (1C1Fh)	REG1C1F	7:0	Default : 0x00
	0F8_VGCB_REG[7:0]	7:0	Access : R/W OSD V B Gradually Color. 1f[7:0]. [7]: SB=Sign bit of Blue color. 0: Increase. 1: Decrease. [6]: IBV=Inverse bit of Blue color. 0: Normal. 1: Invert. [5:0]:B_GRADV[5:0]=Increase/Decrease value of Blue color.
10h (1C20h)	REG1C20	7:0	Default : 0x00
	100_VRSTEP_REG[7:0]	7:0	Access : R/W OSD Vertical R Step. 20[7:0]. [7:0]:VGRADSR[7:0]=Vertical Gradually Step of Red color.
10h (1C21h)	REG1C21	7:0	Default : 0x00
	108_VGSTEP_REG[7:0]	7:0	Access : R/W OSD Vertical G Step. 21[7:0]. [7:0]:VGRADSG[7:0]=Vertical Gradually Step of Green color.

OSD Register (Bank = 1C)				
Index (Absolute)	Mnemonic	Bit	Description	
11h (1C22h)	REG1C22	7:0	Default : 0x00	Access : R/W
	110_VBSTEP_REG[7:0]	7:0	OSD Vertical B Step. 22[7:0]. [7:0]:VGRADSB[7:0]=Vertical Gradually Step of Blue color.	
13h (1C26h)	REG1C26	7:0	Default : 0x00	Access : R/W
	130_TIME_REG[7:0]	7:0	Access Timing Control. 26[7:0]. [4]: FRG_EN=OSD Font RAM Gated Enable. 0: Disable. 1: Enable. [1]: OSD Vertical Start Delay. 0: Normal. 1: Vertical Delay 1 line.	
13h (1C27h)	REG1C27	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	138_REG_27H[2:0]	2:0	Noise generator. 27[2:0]. [2]: RTPT=OSD Random Test Pattern Type. 0: RGB is the same. 1: RGB is different. [1:0]:OSDRTP[1:0]=OSD Random Test Pattern. 00: Disable. 01: 1 random bit. 10: 2 random bit. 11: Reserved.	
20h (1C40h)	REG1C40	7:0	Default : 0x00	Access : R/W
	200_VSCROLL_SPD[7:0]	7:0	Vertical scroll speed.40[7:0]. [7:0]:SCRLSPD[7:0]=OSD Scroll function speed (the numbers of VSYNC).	
20h (1C41h)	REG1C41	7:0	Default : 0x00	Access : R/W
	20F_IN_VSCROLL_EN	7	[0]: SCREN=OSD Scroll function Enable.41[7]. 0: Disable. 1: Enable.	
	20E_VSCROLL_FAST	6	[0]: VSCR_FAST=Scroll at every VSYNC.41[6].	
	20D_VSCROLL_TRUN	5	[0]: TRUC_EN=Truncate code/attribute Enable.41[5]. 0: Disable. 1: Enable.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
	208_VSCROLL_LN[4:0]	4:0	[4:0]: SCROLLINE[4:0]=OSD Scroll function(the numbers of scan lines per scroll).41[4:0].
21h (1C42h)	REG1C42	7:0	Default : 0x0F Access : R/W
	217_REG_UNDER_9_17	7	[0]: UNDERLINE_1=OSD Underline at last line.42[7].
	216_REG_UNDER_8_16	6	[0]: UNDERLINE_2=OSD Underline at second last line.42[6].
	215_REG_SEL_UNDERLINE	5	[0]: UNDERLINE_MD=OSD Underline Mode enable.42[5]. 0: Attribute bit 3 is character border control for 8 color mode. 1: Attribute bit 3 is underline control for 8 color mode.
	214_REG_HALFTR_MODE	4	[0]: HALF_TRANEN=OSD Half-Transparency Enable (When this bit is asserted, OSD Attribute (8 Color) bit 9 (HALF_TRAN) is active).42[4].
	210_REG_TRAN_INDEX[3:0]	3:0	[3:0]:TRAN_INDEX[3:0]=OSD Color Index for Transparency.(Define which color index is transparent). 42[3:0].
21h (1C43h)	REG1C43	7:0	Default : 0x1D Access : R/W
	218_CA_TRUN_NUM[7:0]	7:0	Code/attribute truncate number. 43[7:0]. [7:0]:TRUNCATENUM=OSD Truncate number (Please refer h0022 bit 15 CCRAM1024X2. When CCRAM1024X2 = 0, final row=(11'h7ff-TRUNCATENUM). When CCRAM1024X2 = 1, final row=(11'h3ff-TRUNCATENUM)).
22h (1C44h)	REG1C44	7:0	Default : 0x00 Access : R/W
	226_SHIFT_OFFSET[1:0]	7:6	[1:0]:ITALIC_OFFSET=OSD Italic right shift Offset (Unit: pixel).44[7:6]. 00: 1. 01: 2. 10: 3. 11: 4.
	224_REG_ITA1ST_LN[1:0]	5:4	[1:0]:ITALIC_1ST_LINE=OSD Italic start scan Line (Unit: line).44[5:4]. 00: 0. 01: 1. 10: 2. 11: 3.
	222_SHIFT_STEP[1:0]	3:2	[1:0]:ITALIC_STEP=OSD Italic left shift Step (00: 0.001,

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			01: 0.010, 10: 0.011, 11:0.100 (pixel,binary)).44[3:2].
	221_REG_ITALIC_EN	1	[0]: OSD Italic function Enable.44[1]. 0: Disable. 1: Enable.
	-	0	Reserved.
22h (1C45h)	REG1C45	7:0	Default : 0x00 Access : R/W
	228_REG_45_NULL[7:0]	7:0	[7]: CCRAM1024X2=OSD 2 1024 code/attribute SRAM (When CCRAM1024X2 = 0, there is one 2048 code/attribute SRAM for using; when CCRAM1024X2 = 1, there are two 1024 code/attribute SRAM for using).45[7:0]. [4:2]:LINE_SHIFT_VAL[2:0]=OSD Line shift value (Line shift number, 000: 1..., 111: 8). [1]: CARHG_EN=OSD code/attribute high part ram gated Enable. 0: Diabile. 1: Enable.
23h (1C46h)	REG1C46	7:0	Default : 0x00 Access : R/W
	230_REG_46_NULL[7:0]	7:0	[7:0]:OSD4CFFA[7:0]=OSD 4 color Font RAM start Address (must be even number).46[7:0].
23h (1C47h)	REG1C47	7:0	Default : 0x00 Access : R/W
	238_REG_47_NULL[7:0]	7:0	[7:0]:OSD8CFFA[7:0]=OSD 8 Color Font RAM start Address.47[7:0].
24h (1C48h)	REG1C48	7:0	Default : 0x00 Access : R/W
	240_REG_48_NULL[7:0]	7:0	48[7:0]. [7]: M4c_start[8]=See description for OSD4CFFA[7:0] m4c_start[9]=BK1F_REG3C[3]. [6]: M8c_start[8]=See description for OSD8CFFA[7:0] m8c_start[9]=BK1F_REG3C[7]. [5]: Reg_force_bd=Force OSD Character Border. [4]: Reg_osd2ip=OSD Data Mux Path. 0: OSD mux with output data. 1: OSD mux with input data. [3]: Reg_sel_transp=Select attribute bit3 as Transparency when 8 color palette is used. 0: Border/underline. 1: Transparency. [2]: Reg_8ckey_mode=Use new 8 Color Key. 0: Use BK0 63h[7:4] as color key.

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			1: Use OSD BK 59h~5Ch as color key. [1]: Reg_db_width_en=Double Width Enable. 0: Disable. 1: Enable. [0]: Reg_db_high_en=Double High Enable. 0: Disable. 1: Enable.
24h (1C49h)	REG1C49	7:0	Default : 0x00 Access : R/W
	248_REG_49_NULL[7:0]	7:0	49[7:0]. [7:6]: frame_clr[3:2]. [5:3]: frame_clr[14:12]. [2:0]: frame_clr[24:22].
25h (1C4Ah)	REG1C4A	7:0	Default : 0x00 Access : R/W
	250_REG_4A_NULL[7:0]	7:0	4a[7:0]. [7]: VSCR_OPT=Vscroll Option. 0: Original. 1: Fixed. [5:4]: OVSTA[9:8]=OSD windows Vertical Start position (Read only). [2:0]: OHSDTA[10:8]=OSD windows Horizontal Start position. (Read only).
25h (1C4Bh)	REG1C4B	7:0	Default : 0x00 Access : R/W
	250_REG_4B_NULL[7:0]	7:0	[7]: Reg_ck256p_en: color key for 256 color palette enable. If CK256P_EN = 1 and 2bit/pix. Color key = AtrSRAM[1]=1 & Font[1:0] = 1. If CK256P_EN = 1 and 3bit/pix. Color key = AtrSRAM[1]=1 & Font[2:0] = 1. [6:3]: ckind = color key. [2:0]: abm = alpha blending mode. 0: No blend 1: backgnd blend 2: foregnd blend 3: color key blend 4: not color key blend. Others: All blend.
26h (1C4Ch)	-	7:0	Default : - Access : -
	-	-	Reserved.
26h (1C4Dh)	REG1C4D	7:0	Default : 0x00 Access : R/W
	268_REG_OSD_BRI[7:0]	7:0	OSD brightness Control. 4d[7:0].

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			[7]: OSDBRI_EN=OSD Brightness Enable. 0: Disable. 1: Enable. [6]: OSDBRI_DIR=OSD Brightness Control. 0: Add. 1: Subtract. [5:0]:OSDBRI_VAL[5:0]=OSD Brightness Value.
27h (1C4Eh)	REG1C4E	7:0	Default : 0x00 Access : R/W
	270_REG_4E_NULL[7:0]	7:0	[7:4]: reg_osd_def_char_high = OSD Font height. OSD font height = (270_REG_4E_NULL[7:4]+1)*2. [3]: Wr_16pal_mask: force 1 to write reg_3b8_reg_77, reg_3c0_reg_78 and reg_3c8_reg_79. [2]: T16p_transp_en = color F transparent enable as t256p = 1 and mfont_csel =1. 0: Disable 1: enable. [1]: Mfont_csel = OSD 256 color palette Mono Font Color Select. 0: Use 256 color palette select method. 1: Use 16 color palette select method. [0]: T256p = 256 color palette enable. 1: Enable 0: disable.
27h (1C4Fh)	REG1C4F	7:0	Default : 0x00 Access : R/W
	278_REG_4F[7:0]	7:0	4f[7:0]. [3:2]: osph_lsb. [1:0]: ospw_lsb.
28h (1C50h)	REG1C50	7:0	Default : 0x00 Access : R/W
	280_CLR_DATA_0[7:0]	7:0	Code clear data port 0. 50[7:0]. [7:0]:CODECLRDATA[7:0]=OSD Code Clear Data.
28h (1C51h)	REG1C51	7:0	Default : 0x00 Access : R/W
	288_CLR_DATA_1[7:0]	7:0	Code clear data port 1. 51[7:0]. [7:0]:ATRCLRDATA[7:0]=OSD Attribute Clear Data (lower 8bits).
29h (1C52h)	REG1C52	7:0	Default : 0x00 Access : R/W
	290_CLR_DATA_2[7:0]	7:0	Code clear data port 2. 52[7:0]. [6:4]:ATRCLRDATA[10:8]=OSD Attribute Clear data.

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			[3:0]:CODECLRDAT[11:8]=OSD Code Clear Data.
29h (1C53h)	REG1C53	7:0	Default : 0x00 Access : R/W
	298_REG_53[7:0]	7:0	Code clear addr L. 53[7:0]. [7:0]:OSDCLR_ADR[7:0]=OSD Clear Starting address (lower 8bits).
2Ah (1C54h)	REG1C54	7:0	Default : 0x00 Access : R/W
	2A0_REG_54[7:0]	7:0	Code clear addr H. 54[7:0]. [7]: ATR1_CLREN=OSD Attribute High Clear Enable. [6]: ATR0_CLREN=OSD Attribute Low Clear Enable. [5]: CODE1_CLREN=OSD Code High Clear Enable. [4]: CODE0_CLREN=OSD Code Low Clear Enable. [1:0]:OSDCLR_ADR[9:8]=OSD Clear Starting Address.
2Ah (1C55h)	REG1C55	7:0	Default : 0x00 Access : R/W
	2A8_REG_55[7:0]	7:0	Code clear offset. 55[7:0]. [6:0]:OSDCLR_OFST[6:0]=OSD Clear Offset.
2Bh (1C56h)	REG1C56	7:0	Default : 0x01 Access : R/W
	2B0_REG_56[7:0]	7:0	Code clear width. 56[7:0]. [6:0]:OSDCLR_WID[6:0]=OSD Clear Width.
2Bh (1C57h)	REG1C57	7:0	Default : 0x01 Access : R/W
	2B8_REG_57[7:0]	7:0	Code clear height. 57[7:0]. [6:0]:OSDCLR_HIGT[6:0]=OSD Clear Height.
2Ch (1C58h)	REG1C58	7:0	Default : 0x00 Access : R/W
	2C0_REG_58[7:0]	7:0	Code clear command. 58[7:0]. [0]: BLK_CLR_EN=OSD Block Clear Enable.
2Ch (1C59h)	REG1C59	7:0	Default : 0x00 Access : R/W
	2C8_REG_59[7:0]	7:0	Ckey01. 59[7:0]. [7:4]: ckey0=Color Key Index0. [3:0]: ckey1=Color Key Index1.
2Dh (1C5Ah)	REG1C5A	7:0	Default : 0x00 Access : R/W
	2D0_REG_5A[7:0]	7:0	Ckey23.

OSD Register (Bank = 1C)				
Index (Absolute)	Mnemonic	Bit	Description	
			5a[7:0]. [7:4]: ckey2=Color Key Index2. [3:0]: ckey3=Color Key Index3.	
2Dh (1C5Bh)	REG1C5B	7:0	Default : 0x00	Access : R/W
	2D8_REG_5B[7:0]	7:0	Ckey45. 5b[7:0]. [7:4]: ckey4=Color Key Index4. [3:0]: ckey5=Color Key Index5.	
2Eh (1C5Ch)	REG1C5C	7:0	Default : 0x00	Access : R/W
	2E0_REG_5C[7:0]	7:0	Ckey67. 5c[7:0]. [7:4]: ckey6=Color Key Index6 only for 16 cp. [3:0]: ckey7=Color Key Index7 only for 16 cp.	
3Bh (1C77h)	REG1C77	7:0	Default : 0x00	Access : R/W
	3B8_REG_77[7:0]	7:0	77[7:0], [1]: OSD DE INT MASK [2]: OSD DE INT CLEAR.	
3Ch ~ 3Ch (1C78h ~ 1C79h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
50h (1CA0h)	REG1CA0	7:0	Default : 0x00	Access : R/W
	507_ENIOBURST	7	A0[7]. [0]: TOSB_MD=OSD SRAM I/O Access Burst Mode. 0: Disable. 1: Enable.	
	506_CLEARCODE	6	A0[6]. [0]: CLR=OSD Clear Bit. (WO). 0: Normal. 1: Clear code with 00h, attribute with 00h.	
	505_IOCPRAMEN	5	A0[5].	
	504_IOFRAMEN	4	A0[4]. [0]: RF=OSD RAM Font I/O Access. 0: Disable. 1: Enable.	
	503_IOCGRAMEN	3	A0[3]. [0]: DC=OSD Display Code I/O Access. 0: Disable. 1: Enable.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
	502_IOARAMEN	2	A0[2]. [0]: DA=OSD Display Attribute I/O Access. 0: Disable. 1: Enable.
	501_IOREG_WBSTEN	1	A0[1]. [0]: ORBW_MD=OSD Register Burst Write Mode. 0: Disable. 1: Enable.
	500_IOREG_RBSTEN	0	A0[0]. [0]: ORBR_MD=OSD Register Burst Read Mode. 0: Disable. 1: Enable.
50h (1CA1h)	REG1CA1	7:0	Default : 0x00
	-	7:6	Reserved.
	508_OSDRA[5:0]	5:0	A1[5:0]. [5:0]:OSDRA=OSD Register Address Port.
51h (1CA2h)	REG1CA2	7:0	Default : 0x00
	510_OSDRD[7:0]	7:0	A2[7:0]. [7:0]:OSDRD=OSD Register Data Port.
51h (1CA3h)	REG1CA3	7:0	Default : 0x00
	518_OSDFA[7:0]	7:0	A3[7:0]. [7:0]:OSDFA=OSD RAM Font Address Port.
52h (1CA4h)	REG1CA4	7:0	Default : 0x00
	520_OSDFD[7:0]	7:0	A4[7:0]. [7:0]:OSDFD=OSD RAM Font Data Port.
52h (1CA5h)	REG1CA5	7:0	Default : 0x00
	528_DISPCA_L[7:0]	7:0	A5[7:0]. [7:0]:DISPCA[7:0]=OSD Display Code Address Port.
53h (1CA6h)	REG1CA6	7:0	Default : 0x00
	-	7:3	Reserved.
	530_DISPCA_H[2:0]	2:0	A6[2:0]. [2:0]:DISPCA[10:8]=See description for DISPCA[7:0].
53h (1CA7h)	REG1CA7	7:0	Default : 0x00
	538_DISPCWD_L[7:0]	7:0	A7[7:0]. Note: When BK0 h0057 bit 0=0. [7:0]:DISPCWD[7:0]=OSD Display Code Write Data Port.

OSD Register (Bank = 1C)				
Index (Absolute)	Mnemonic	Bit	Description	
			(R/W). Note: When BK0 h0057 bit 0=1. [7:0]:DISPCRD[7:0]=OSD Display Code Read Data Port. (RO).	
54h (1CA8h)	REG1CA8	7:0	Default : 0x00	Access : R/W
	540_DISPAA_L[7:0]	7:0	A8[7:0]. [7:0]:DISPAA[7:0]=OSD Display Attribute Address Port.	
54h (1CA9h)	REG1CA9	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	548_DISPAA_H[2:0]	2:0	A9[2:0]. [2:0]:DISPAA[10:8]=See description for DISPAA[7:0].	
55h (1CAAh)	REG1CAA	7:0	Default : 0x00	Access : R/W
	550_DISPAWD_L[7:0]	7:0	Aa[7:0]. Note: When BK0 h0057 bit 0=0. [7:0]:DISPAWD[7:0]=OSD Display Attribute Write Data Port. (R/W). Note: When BK0 h0057 bit 0=1. [7:0]:DISPARD[7:0]=OSD Display Attribute Read Data Port. (RO).	
56h (1CACH)	REG1CAC	7:0	Default : 0x00	Access : R/W
	560_256CPAWD[7:0]	7:0	Ac[7:0]. OSD 256 Color Palette Address port.	
56h (1CADh)	REG1CAD	7:0	Default : 0x00	Access : R/W
	568_256CPDWD[7:0]	7:0	Ad[7:0]. OSD 256 Color Palette Data port.	
57h (1CAEh)	REG1CAE	7:0	Default : 0x00	Access : R/W
	574_CODE_EXT_DATA[3:0]	7:4	Ae[7:4]. When BK0 h0057 bit 0=0. [2:0]:DISPCWD[11:9]=See description for DISPCWD. (R/W). When BK0 h0057 bit 0=1. [2:0]:DISPCWD[11:9]=See description for DISPCRD. (RO). Note: When OSD BK h0024 bit 1=1. DISPCWD[11:10]=Double Width Control. 0x: Disable.	

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			10: The 1st double width font. 11: The 2nd double width font. DISPCWD[9:0]=OSD Display Font Index. Note: When OSD BK h0024 bit 1=0. DISPCWD[10]=OSD Italic Control. 0: Disable. 1: Enable. DISPCWD[9:0]=OSD Display Font Index.
	573_FONT_INDEX8	3	Ae[3]. [0]: OSDFA[8]=See description for OSDFA[7:0] (R/W).
	573_FONT_INDEX9	2	Ae[2]. [0]: OSDFA[9]=See description for OSDFA[7:0] (R/W).
	571_CA_RD_RDY	1	Ae[1]. [0]: CA_RD_RDY=OSD Display Code and Attribute Read Ready. (RO).
	570_CA_NO_WRITE	0	Ae[0]. [0]: CA_RD_EN=OSD Display Code and Attribute Read Enable. (R/W).
57h (1CAh)	REG1CAF	7:0	Default : 0x00
	-	7	Access : R/W
	-	7	Reserved.
	57C_ATR_EXT_DATA[2:0]	6:4	Af[6:4]. When BK0 h0057 bit 0=0. [2:0]:DISPAWD[10:8]=See description for DISPAWD[7:0]. (R/W). When BK0 h0057 bit 0=1. [2:0]:DISPARD[10:8]=See description for DISPARD[7:0]. (RO). Note: When OSD BK h0008 bit 0=0, OSD BK h0024 bit 0=1 & OSD BK h0024 bit 3=1. [2:0]:DISPAWD[10:8]=Double High Control. 00x: Disable. 010: The 1st x2 high font. 011: The 2nd x2 high font. 100: The 1st x4 high font. 101: The 2nd x4 high font. 110: The 3rd x4 high font. 111: The 4th x4 high font. DISPAWD[7]=OSD Blink Control.

OSD Register (Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>0: Disable. 1: Enable.</p> <p>DISPAWD[6:4]=OSD Foreground Color Select. 000: Color index 0. 001: Color index 1. .. 111: Color index 7.</p> <p>DISPAWD[3]=OSD Transparency Control. 0: Disable. 1: Enable.</p> <p>DISPAWD[2:0]=OSD Background Color Select. 000: Color index 0. 001: Color index 1. .. 111: Color index 7.</p> <p>Note: When OSD BK h0008 bit 0=0, OSD BK h0021 bit 5, bit 4 =2'b11 & OSD BK h0024 bit 0=0.</p> <p>DISPAWD[8]=OSD Half-transparency Control. 0: Disable. 1: Enable.</p> <p>DISPAWD[7]=OSD Blink Control. 0: Disable. 1: Enable.</p> <p>DISPAWD[6:4]=OSD Foreground Color Select. 000: Color index 0. 001: Color index 1. .. 111: Color index 7.</p> <p>DISPAWD[3]=OSD Character Underline Control. 0: Disable. 1: Enable.</p> <p>DISPAWD[2:0]=OSD Background Color Select. 000: Color index 0. 001: Color index 1. .. 111: Color index 7.</p> <p>Note: When OSD BK h0008 bit 0=1, OSD BK h0021 bit 4=0 & OSD BK h0024 bit0=0.</p> <p>DISPAWD[10]=OSD Blink Control. 0: Disable.</p>

OSD Register (Bank = 1C)			
Index (Absolute)	Mnemonic	Bit	Description
			1: Enable. DISPAWD[9]=OSD Character Border Control. 0: Disable. 1: Enable. DISPAWD[8]=OSD Character Underline Control. 0: Disable. 1: Enable. DISPAWD[7:4]=OSD Foreground Color Select. 0000: Color index 0. 0001: Color index 1. .. 1111: Color index 15.
	-	3:0	Reserved.

CHIPTOP Register (Bank = 1E)

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (1E00h)	REG1E00	7:0	Default : 0x00	Access : R/W
	CHIP_CONFIG_OVERWRITE[7:0]	7:0	Chip config overwrite. [0]: Sel_sbus_oven. [1]: Sel_sbus_ov. [2]: Sel_dbus_oven. [3]: Sel_dbus_ov. others: Reserved.	
00h (1E01h)	REG1E01	7:0	Default : 0x00	Access : R/W
	CHIP_CONFIG_OVERWRITE[15:8]	7:0	See description of '1E00h'.	
01h (1E02h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
01h (1E03h)	REG1E03	7:0	Default : 0x00	Access : R/W
	SBSETL	7	Series bus pads set low.	
	SBSETH	6	Series bus pads set high.	
	SETL	5	Digital pads set low.	
	SETH	4	Digital pads set high.	
	-	3	Reserved.	
	UART_RX_ENABLE	2	1: Enable UART0 RX. 0: Disable UART0 RX.	
	JTAG_DISABLE	1	0: Enable jtag. 1: Disable jtag.	
02h (1E04h)	REG1E04	7:0	Default : 0x00	Access : R/W
	TEST_OUT_MODE[1:0]	7:6	Pad_sar[3:0] control. [0]: 0 controlled by pad_top. 1 controlled by sar_top. [1]: Reserved.	
	OSC_MODE[1:0]	5:4	Delay chain mode. 0: Low IR drop. 1: Whole chip. 2: High IR drop. 3: Audio dsp.	
	CARD_MS[1:0]	3:2	Specify 9 pads for card reader MS mode.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			0: Disable. others: See GPIO table.
	CARD_SD[1:0]	1:0	Specify 10 pads for card reader SD mode. 0: Disable. others: See GPIO table.
02h (1E05h)	REG1E05	7:0	Default : 0x00 Access : RO, R/W
	-	7:6	Reserved.
	GP_DDCR_CLK_IN	5	C readback when pad_ddcrom_clk use as GPIO.
	GP_DDCR_DA_IN	4	C readback when pad_ddcrom_dat use as GPIO.
	GP_DDCR_CLK_OEN	3	OEN control when pad_ddcrom_clk use as GPIO.
	GP_DDCR_CLK_OUT	2	I control when pad_ddcrom_clk use as GPIO.
	GP_DDCR_DA_OEN	1	OEN control when pad_ddcrom_dat use as GPIO.
	GP_DDCR_DA_OUT	0	I control when pad_ddcrom_dat use as GPIO.
03h (1E06h)	REG1E06	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	TCOM	6	0: Disable. 1: Specify pad_gpiob as tcon function.
	-	5:0	Reserved.
03h (1E07h)	REG1E07	7:0	Default : 0xE0 Access : R/W
	PWM_OEN[3:0]	7:4	Output enable_bar of PWM pads. Initial should be input for capturing CHIP_CONFIG while reset.
	-	3:2	Reserved.
	DDCROM_GPIO	1	0: Disable. 1: Specify pad_ddcrom_xx as gpio function.
	DDCROM_EN	0	0: Disable. 1: Specify pad_ddcrom_xx as ddcrom function.
04h (1E08h)	-	7:0	Default : - Access : -
	-	-	Reserved.
04h (1E09h)	REG1E09	7:0	Default : 0x00 Access : R/W
	IIC_MST[3:0]	7:4	Selection of specify 2 pads as iic master function. 0: Disable. others: See GPIO table.
	JTAG_8051[1:0]	3:2	Selection of specify 4 pads as JTAG_8051 function.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			0: Disable. 1: Pad_sar[3:0]. 2: Pad_pwm[1:0] + pad_ddcrom*. 3: Pad_gpiom[3:0].
	JTAG_AU[1:0]	1:0	Selection of specify 4 pads as JTAG_Audio function. 0: Disable. 1: Pad_gpiod[3:0]. 2: Pad_iclk + pad_di[2:0]. 3: Pad_di[7:4].
05h (1E0Ah)	REG1E0A	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	BT656_OUT[2:0]	6:4	Selection of specify 8 pads as bt656 out function. 0: Disable. others: See GPIO table.
	BT656_10BIT	3	Selection of specify 2 pads as bt656[9:8] function (for testing prupose). 0: Disable. 1: Pad_lvsync for bt656[8], pad_lvsync for bt656[9].
	BT656_IN[2:0]	2:0	Selection of specify 8 pads as bt656[7:0] function. 0: Disable. others: See GPIO table.
05h (1E0Bh)	REG1E0B	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	UART1[2:0]	6:4	Selection of specify 2 pads as UART1 function. 0: Disable. others: See GPIO table.
	UART0[3:0]	3:0	Selection of specify 2 pads as UART0 unction. 0: Disable. others: See GPIO table.
06h (1E0Ch)	REG1E0C	7:0	Default : 0x00 Access : R/W
	I2S_OUT1[3:0]	7:4	Selection of specify 4 pads as I2S out1 function. 0: Disable. others: See GPIO table.
	I2S_IN[3:0]	3:0	Selection of specify 3 pads as I2S in function. 0: Disable. others: See GPIO table.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
06h (1E0Dh)	REG1E0D	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	SB_DAT_OUT_OEN	4	Reserved.
	I2S_MUTE[3:0]	3:0	Selection of specify 1 pads as I2S mute function. 0: Disable. others: See GPIO table.
07h (1E0Eh)	REG1E0E	7:0	Default : 0x00 Access : R/W
	GPIO_A	7	0: Disable. 1: Specify pad_iclk + pad_di[7:0] as GPIOA.
	-	6:4	Reserved.
	HDMI_CEC[3:0]	3:0	Selection of specify 1 pads as HDMI_CEC function. 0: Disable. others: See GPIO table.
07h (1E0Fh)	REG1E0F	7:0	Default : 0x00 Access : R/W
	GPIO_T[1:0]	7:6	0: Disable. 1: Specify pad_gpiot[3:0] as GPIOT.
	GPIO_R	5	0: Disable. 1: Specify pad_gpior[10:0] as GPIOR.
	GPIO_M	4	Dbus pads setL (rev_c eco).
	GPIO_L	3	0: Disable. 1: Specify pad_gpiol[4:0] as GPIOL.
	GPIO_H	2	Dbus pads setH (rev_c eco).
	GPIO_D	1	0: Disable. 1: Specify pad_gpiod[18:0] as GPIOD.
	GPIO_B	0	0: Disable. 1: Specify pad_gpiob[13:0] as GPIOB.
08h (1E10h)	REG1E10	7:0	Default : 0x00 Access : R/W
	GPIOA_OUT[7:0]	7:0	I control when specify pad_iclk + pad_di[7:0] as GPIOA.
08h (1E11h)	REG1E11	7:0	Default : 0x00 Access : R/W
	GPIOL_OUT[4:0]	7:3	I control when specify pad_gpiol[4:0] as GPIOL.
	GPIOA_OUT[10:8]	2:0	See description of '1E10h'.
09h (1E12h)	REG1E12	7:0	Default : 0x00 Access : R/W
	GPIOA_OEN[7:0]	7:0	OEN control when specify pad_iclk + pad_di[7:0] as GPIOA.

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
09h (1E13h)	REG1E13	7:0	Default : 0xF8	Access : R/W
	GPIOL_OEN[4:0]	7:3	OEN control when specify pad_gpiol[4:0] as GPIOL.	
	GPIOA_OEN[10:8]	2:0	See description of '1E12h'.	
0Ah (1E14h)	REG1E14	7:0	Default : 0x00	Access : R/W
	GPIOB_OUT[7:0]	7:0	I control when specify pad_gpiob[15:0] as GPIOB.	
0Ah (1E15h)	REG1E15	7:0	Default : 0x00	Access : R/W
	GPIOB_OUT[15:8]	7:0	See description of '1E14h'.	
0Bh (1E16h)	REG1E16	7:0	Default : 0xFF	Access : R/W
	GPIOB_OEN[7:0]	7:0	OEN control when specify pad_gpiob[15:0] as GPIOB.	
0Bh (1E17h)	REG1E17	7:0	Default : 0xFF	Access : R/W
	GPIOB_OEN[15:8]	7:0	See description of '1E16h'.	
0Ch (1E18h)	REG1E18	7:0	Default : 0x00	Access : R/W
	GPIOD_OUT[7:0]	7:0	I control when specify pad_gpiod[18:0] as GPIOD.	
0Ch (1E19h)	REG1E19	7:0	Default : 0x00	Access : R/W
	GPIOD_OUT[15:8]	7:0	See description of '1E18h'.	
0Dh (1E1Ah)	REG1E1A	7:0	Default : 0x00	Access : R/W
	GPIOM_OUT[3:0]	7:4	I control when pad_gpiom[3:0] is GPIOM.	
	-	3	Reserved.	
	GPIOD_OUT[18:16]	2:0	See description of '1E18h'.	
0Dh (1E1Bh)	REG1E1B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	GPIOT_OUT[3:0]	3:0	I control when specify pad_gpiot[3:0] as GPIOT.	
0Eh (1E1Ch)	REG1E1C	7:0	Default : 0xFF	Access : R/W
	GPIOD_OEN[7:0]	7:0	OEN control when specify pad_gpiod[18:0] as GPIOD.	
0Eh (1E1Dh)	REG1E1D	7:0	Default : 0xFF	Access : R/W
	GPIOD_OEN[15:8]	7:0	See description of '1E1Ch'.	
0Fh (1E1Eh)	REG1E1E	7:0	Default : 0xF7	Access : R/W
	GPIOM_OEN[3:0]	7:4	OEN control when pad_gpiom[3:0] is GPIOM.	
	-	3	Reserved.	
	GPIOD_OEN[18:16]	2:0	See description of '1E1Ch'.	
0Fh (1E1Fh)	REG1E1F	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
	GPIOT_OEN[3:0]	3:0	OEN control when specify pad_gpiot[3:0] as GPIOT.
10h (1E20h)	REG1E20	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	MCU_QUICK_RST	2	0: Normal. 1: Mcu quick reset.
	MCU_RESET	1	1: Mcu reset by s/w.
	POFF_RST_EN	0	1: Power off reset enable.
11h (1E22h)	REG1E22	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	STC0SYN_RST	5	Stc0 synthesizer software reset, active high.
	USBSYN_RST	4	Usb synthesizer software reset, active high.
	DE_ONLY_F2	3	DE only mode for SC_TOP main window.
	DE_ONLY_F1	2	DE only mode for SC_TOP PIP window.
	CLK_VD_SEL	1	Select vd clock from adc1 or adc2. 0: Select VD_ADC_CLK. 1: Select ADC_CLK.
	SW_MCU_CLK	0	Mcu clock setting. 1'b0: DFT_live. 1'b1: select the output according to reg_ckg_mcu.
11h (1E23h)	REG1E23	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	UPDATE_DC0_SYNC_CW	6	Update the control words of DC0 synthesizer that is. Synchronized to STC0.
	-	5:4	Reserved.
	UPDATE_DC0_FREERUN_CW	3	Update the control words of DC0 free-running synthesizer.
	-	2	Reserved.
	UPDATE_STC0_CW	1	Update control word of the synthesizer STC0.
12h (1E24h)	REG1E24	7:0	Default : 0x01 Access : R/W
	CKG_RIU[3:0]	7:4	[0]: Select clk_vd_p from 8*fsc or vif_43m. 0: Clk_vd_p from 8*fsc. 1: Clk_vd_p from vif_43m. [1]: Clk_vif selection for clk_dac.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			0: Select 43m. 1: Select 86m. [2]: Sbm_sda_oez selection. 0: From sbm_sda_out (open drain). 1: From sbm_sda_oez. [3]: Di clock selection (ccir656 in). 0: From clk_idclk_f2 (main window). 1: From clk_idclk_f1(sub window).
	-	3:2	Reserved.
	CKG_USB30[1:0]	1:0	Clk_uhc clock setting. [0]: Disable clock. [1]: Invert clock.
12h (1E25h)	REG1E25	7:0	Default : 0x00 Access : R/W
	CKG_MIU[3:0]	7:4	Clk_miu clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 200MHz (memp11 out). 01: 170MHz. 10: 216MHz (rev_d eco). 11: 100MHz (memp11 div 2).
	CKG_DDR[3:0]	3:0	Clk_miu2 clock setting. [0]: Disable clock. [1]: Invert clock. Selection of test clk out for osd line buffer. [2]: 0 => select clk_ft0lb; 1 => select clk_ft1lb. [3]: 0 => select clk_ca0lb; 1 => select clk_ca1lb.
13h (1E26h)	REG1E26	7:0	Default : 0x00 Access : R/W
	CKG_AEON[1:0]	7:6	Clk_osdlb_p clock source setting. 2'b00: from odclk. 2'b01: from idclk1 with gating. 2'b10: from idclk2 with gating. 2'b11: reserved.
	CKG_TCK[1:0]	5:4	Clk_tck clock setting. [0]: Disable clock. [1]: Invert clock.
	CKG_TS0[3:0]	3:0	Clk_mini clock setting. [0]: Disable clock.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			[1]: Invert clock. [2]: Select clock source. 1: From clk_DFT. 0: From clk_mini_buf. Clk_miu2 clock setting. [3]: Force from clk_DFT.
13h (1E27h)	REG1E27	7:0	Default : 0x01 Access : R/W
	CKG_STC0[3:0]	7:4	Clk_mcp clock setting. [3]: 1 => from clk_DFT. 0 => from clk_mcp_p. Clk_usb clock setting. [2]: Select clock source. 1: From clk_DFT. 0: From clk_usb_buf. [1]: Invert clock. [0]: Disable clock.
	CKG_TSP[3:0]	3:0	Clk_ft0lb, clk_ft1lb, clk_ca0lb, clk_ca1lb. Clock source setting. [3]: 1=> from clk_DFT. 0 =>from clk_XXX_p. Clk_mload clock setting. [2]: Select clock source. 1: From clk_DFT. 0: From clk_mload_p. [1]: Invert clock. [0]: Disable clock.
14h (1E28h)	REG1E28	7:0	Default : 0x00 Access : R/W
	CKG_MAD_STC[3:0]	7:4	Clk_ca0lb clock setting. [0]: Disable clock. [1]: Invert clock. Clk_ca1lb clock setting. [2]: Disable clock. [3]: Invert clock.
	-	3:0	Reserved.
14h (1E29h)	REG1E29	7:0	Default : 0x18 Access : R/W
	CKG_MVD[3:0]	7:4	Clk_mcu_mail0/clk_mcu_mail1 clock setting. [0]: Disable clock. [1]: Invert clock.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			[3:2]: clock source select. For clk_mcu_mail0. 2'b00: from clk_hkmcu_p. 2'b01: from clk_vdmcu_p. For clk_mcu_mail1. 2'b00: from clk_vdmcu_p. 2'b01: from clk_hkmcu_p. 2'b10: reserved. 2'b11: from clk_DFT.
	CKG_MVD_BOOT[3:0]	3:0	Reserved.
15h (1E2Ah)	REG1E2A	7:0	Default : 0x11 Access : R/W
	CKG_DC0[3:0]	7:4	Clk_ft0lb clock setting. [0]: Disable clock. [1]: Invert clock. Clk_ft1lb clock setting. [2]: Disable clock. [3]: Invert clock.
	CKG_M4V[3:0]	3:0	Clk_mcp clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 200MHz (memp1l out). 01: 170MHz. 10: 123MHz. 11: 100MHz (memp1l div 2).
15h (1E2Bh)	REG1E2B	7:0	Default : 0x11 Access : R/W
	CKG_GE[3:0]	7:4	Clk_osd2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: Idclk. 01: Odclk1 with gating. 10: Odclk2 with gating. 11: Clk_DFT.
	CKG_DHC_SBM[3:0]	3:0	Clk_dhc_sbm clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			00: 12MHz. 01: 36MHz. 10: 62MHz. 11: Select XTAL.
16h (1E2Ch)	REG1E2C	7:0	Default : 0x11 Access : R/W
	CKG_GOPG1[3:0]	7:4	Clk_ca0lb2 clock setting. [0]: Disable clock. [1]: Invert clock. Clk_ca1lb2 clock setting. [2]: Disable clock. [3]: Invert clock.
	CKG_GOPG0[3:0]	3:0	Clk_ft0lb2 clock setting. [0]: Disable clock. [1]: Invert clock. Clk_ft1lb2 clock setting. [2]: Disable clock. [3]: Invert clock.
16h (1E2Dh)	REG1E2D	7:0	Default : 0x11 Access : R/W
	CKG_VD[3:0]	7:4	Clk_vd clock setting. [0]: Disable clock. [1]: Invert clock. [3:2] 2'b00: clk_vd_p. 01: Clk_vif_43m. 10: Test clk in. 11: Clk_DFT.
	CKG_GOPD[3:0]	3:0	Clk_miu clock setting. [3]: 1 => from clk_DFT. 0 => from clk_miu_p. Clk_ft0lb2, clk_ft1lb2, clk_ca0lb2, clk_ca1lb2 clock source setting. [2]: 1=> from clk_DFT. 0 =>from clk_XXX_p. Clk_osdlb2_p clock source. [1:0] 2'b00: from odclk. 2'b01: from idclk1 with gating. 2'b10: from idclk2 with gating. 2'b11: reserved.
17h	REG1E2E	7:0	Default : 0x21 Access : R/W

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
(1E2Eh)	CKG_VD200[2:0]	7:5	Clk_vd200 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 216MHz. 01: 216MHz. 10: 216MHz. 11: Select XTAL.	
	CKG_VDMCU[4:0]	4:0	Reserved.	
17h (1E2Fh)	REG1E2F	7:0	Default : 0x12	Access : R/W
	-	7	Reserved.	
	CKG_DHC[5:0]	6:1	Clk_dhc clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: select clock source. 0000: 12MHz. 0001: 54MHz. 0010: 62MHz. 0011: 72MHz. 0100: 86MHz. 0101: 108MHz. 0110: 0. 0111: 0. 1xxx: XTAL.	
	CKG_VD200[3]	0	See description of '1E2Eh'.	
18h (1E30h)	REG1E30	7:0	Default : 0x10	Access : R/W
	CKG_FICLK_F2[3:0]	7:4	Clk_fickl_f2 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 2b'00: select clk_idclk2. 01: Select clk_fclk. 10: 0. 11: Select XTAL.	
	CKG_FICLK_F1[3:0]	3:0	Clk_fickl_f1 clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			2b'00: select clk_idclk1. 01: Select clk_fclk. 10: 0. 11: Select XTAL.
18h (1E31h)	REG1E31	7:0	Default : 0x10 Access : R/W
	CKG_PCM[3:0]	7:4	Clk_pcm clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: 27MHz. 01: 27MHz. 10: XTAL. 11: XTAL.
	-	3:0	Reserved.
19h (1E32h)	REG1E32	7:0	Default : 0x00 Access : R/W
	CKG_PCI[3:0]	7:4	Reserved.
	CKG_PCIH[3:0]	3:0	Reserved.
19h (1E33h)	REG1E33	7:0	Default : 0x11 Access : R/W
	CKG_VIF0[3:0]	7:4	Clk_vif_43m clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: Select 43MHz. 01: Select 43MHz. 10: Select 43MHz. 11: Select XTAL.
	CKG_VIF1[3:0]	3:0	Clk_vif_86m clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: Select 86MHz. 01: Select 86MHz. 10: Select 86MHz. 11: Select XTAL.
1Ah (1E34h)	REG1E34	7:0	Default : 0x01 Access : R/W
	CKG_SDR[3:0]	7:4	Reserved.
	CKG_DAC[3:0]	3:0	Clk_dac clock setting.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			[0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: Select odclk. 01: Select clk_vif_43m. 10: Select clk_vd. 11: Select XTAL.
1Ah (1E35h)	REG1E35	7:0	Default : 0x01 Access : R/W
	-	7:6	Reserved.
	CKG_FCLK[5:0]	5:0	Clk_fclk clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: select clock source. 0000: Select FIX_CLK from MPLL. 0001: Select clk_miu. 0010: Select clk_odclk. 0011: Select 216MHz. 0100: Select clk_idclk2. 0101: Select 200MHz. 0110: 0. 0111: Select XTAL. 1xxx: Select XTAL.
1Bh (1E36h)	REG1E36	7:0	Default : 0x01 Access : R/W
	-	7:6	Reserved.
	CKG_FMCLK[5:0]	5:0	Clk_fmclk clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: select clock source. 0000: Select clk_miu. 0001: Select FIX_CLK from MPLL. 0010: Select clk_odclk. 0011: 0. 0100: Select clk_idclk2. 0101: 0. 0110: 0. 0111: 0. 1xxx: Select DFT_live.
1Bh	REG1E37	7:0	Default : 0x20 Access : R/W

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
(1E37h)	-	7:6	Reserved.	
	CKG_ODCLK[5:0]	5:0	Clk_odclk clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: select clock source. 0000: Select clk_adc. 0001: Select clk_dvi. 0010: Select clk_vd. 0011: 1. 0100: 1. 0101: Select external DI clock. 0110: Select clk_vd_adc. 0111: Select clk_lpll_buf. 1xxxx: Select XTAL.	
1Ch (1E38h)	REG1E38	7:0	Default : 0x0D	Access : R/W
	-	7:6	Reserved.	
	CKG_JPD[5:0]	5:0	Clk_jpd clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]: select clock source. 000: Select clk_mpll_div. 001: Select 160MHz. 010: Select 144MHz. 011: Select 123MHz. 100: Select 108MHz. 101: Mempll_clk_buf. 110: Mempll_clk_buf_div2. 111: Select 86MHz. [5]: Reserved.	
1Ch (1E39h)	REG1E39	7:0	Default : 0x01	Access : R/W
	-	7	Reserved.	
	CKG_FCIE[6:0]	6:0	Clk_fcie clock setting. [0]: Disable clock. [1]: Invert clock. [6:2]: select clock source. 5'b00000: clk86_div256. 5'b00001: clk86_div64. 5'b00010: clk86_div16.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			5'b00011: clk54_div4. 5'b00100: clk72_div4. 5'b00101: clk86_div4. 5'b00110: clk54_div2. 5'b00111: clk72_div2. 5'b01000: clk86_div2. 5'b01001: 54MHz. 5'b01010: 72MHz. 5'b01011: 0. 5'b01100: 0. 5'b01101: 0. 5'b01110: 0. 5'b01111: 0. 5'b1xxxx: select XTAL.
1Dh (1E3Ah)	REG1E3A	7:0	Default : 0x11
	CKG_TSOUT[3:0]	7:4	Reserved.
	CKG_TS2[3:0]	3:0	Reserved.
1Fh (1E3Eh)	REG1E3E	7:0	Default : 0x20
	-	7:6	Reserved.
	CKG_IDCLK1[5:0]	5:0	Clk_idclk_f1 clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: select clock source. 0000: Select clk_adc. 0001: Select clk_dvi. 0010: Select clk_vd. 0011: Select clk_odclk. 0100: 1. 0101: Select external DI clock. 0110: Select clk_vd_adc. 0111: 0. 1xxx: Select XTAL.
1Fh (1E3Fh)	REG1E3F	7:0	Default : 0x21
	-	7:6	Reserved.
	CKG_IDCLK2[5:0]	5:0	Clk_idclk_f2 clock setting. [0]: Disable clock. [1]: Invert clock. [5:2]: select clock source.

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
			0000: Select clk_adc. 0001: Select clk_dvi. 0010: Select clk_vd. 0011: Select clk_odclk. 0100: 1. 0101: Select external DI clock. 0110: Select clk_vd_adc. 0111: 0. 1xxx: Select XTAL.	
20h (1E40h)	REG1E40	7:0	Default : 0x00	Access : R/W
	DC0_NUM[7:0]	7:0	Numerator of the synthesizer of DC0.	
20h (1E41h)	REG1E41	7:0	Default : 0x00	Access : R/W
	DC0_NUM[15:8]	7:0	See description of '1E40h'.	
21h (1E42h)	REG1E42	7:0	Default : 0x00	Access : R/W
	DC0_DEN[7:0]	7:0	Denominator of the synthesizer of DC0.	
21h (1E43h)	REG1E43	7:0	Default : 0x00	Access : R/W
	DC0_DEN[15:8]	7:0	See description of '1E42h'.	
22h (1E44h)	REG1E44	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_STRLD[3:0]	3:0	Clk_osd clock setting. [0]: Disable clock. [1]: Invert clock. [3:2]: select clock source. 00: Idclk. 01: Odclk1 with gating. 10: Odclk2 with gating. 11: Clk_DFT.	
22h (1E45h)	REG1E45	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CKG_MCU[4:0]	4:0	Clk_mcu clock setting. [0]: Disable clock. [1]: Invert clock. [4:2]:. 000: 170MHz. 001: 160MHz. 010: 144MHz.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			011: 123MHz. 100: 108MHz. 101: Mem_clock. 110: Mem_clock div 2. 111: Xtal div 128.
24h (1E48h)	REG1E48	7:0	Default : 0x00
	USBSYN_CW[7:0]	7:0	Control word of the synthesizer for USB PHY.
24h (1E49h)	REG1E49	7:0	Default : 0x00
	USBSYN_CW[15:8]	7:0	See description of '1E48h'.
25h (1E4Ah)	REG1E4A	7:0	Default : 0x00
	USBSYN_CW[23:16]	7:0	See description of '1E48h'.
25h (1E4Bh)	REG1E4B	7:0	Default : 0x00
	USBSYN_CW[31:24]	7:0	See description of '1E48h'.
26h (1E4Ch)	REG1E4C	7:0	Default : 0x00
	STC0SYN_CW[7:0]	7:0	Control word of the synthesizer of STC0 clocks.
26h (1E4Dh)	REG1E4D	7:0	Default : 0x00
	STC0SYN_CW[15:8]	7:0	See description of '1E4Ch'.
27h (1E4Eh)	REG1E4E	7:0	Default : 0x00
	STC0SYN_CW[23:16]	7:0	See description of '1E4Ch'.
27h (1E4Fh)	REG1E4F	7:0	Default : 0x00
	STC0SYN_CW[31:24]	7:0	See description of '1E4Ch'.
2Ah (1E54h)	REG1E54	7:0	Default : 0x00
	DC0_FREERUN_CW[7:0]	7:0	Control word of the synthesizer of MPEG VOP0 clocks.
2Ah (1E55h)	REG1E55	7:0	Default : 0x00
	DC0_FREERUN_CW[15:8]	7:0	See description of '1E54h'.
2Bh (1E56h)	REG1E56	7:0	Default : 0x00
	DC0_FREERUN_CW[23:16]	7:0	See description of '1E54h'.
2Bh (1E57h)	REG1E57	7:0	Default : 0x00
	DC0_FREERUN_CW[31:24]	7:0	See description of '1E54h'.
2Ch (1E58h)	REG1E58	7:0	Default : 0x05
	-	7:6	Reserved.
	CKG_DHC_SYNTH[3:0]	5:2	Clk_dhc_synth clock setting. [0]: Gating.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			[1]: Inverse. [3:2] = 2_b00: MPLL_VCO_DIV2. [3:2] = 2_b01: MPLL_VCO_DIV2P5. [3:2] = 2_b10: MPLL_VCO_DIV3. [3:2] = 2_b11: MPLL_VCO_DIV4.
	CKG_DHC_DDR[1:0]	1:0	Clk_dhc_ddr clock setting. [0]: Gating. [1]: Inverse.
2Ch (1E59h)	REG1E59	7:0	Default : 0x21 Access : R/W
	CKG_DHC_LIVE[1:0]	7:6	Clk_dhc_live clock setting. [0]: Gating. [1]: Inverse.
	CKG_DHC_MCU[5:0]	5:0	Clk_dhc_mcu clock setting. [0]: Gating. [1]: Inverse. [5:2] = 4_b1xxx: xtali. [5:2] = 4_b0000: 43. [5:2] = 4_b0001: 54. [5:2] = 4_b0010: 62. [5:2] = 4_b0011: 72. [5:2] = 4_b0100: 86. [5:2] = 4_b0101: 108. [5:2] = others: reserved.
2Dh (1E5Ah)	REG1E5A	7:0	Default : 0x11 Access : R/W
	CKG_ADCD1[3:0]	7:4	Clock control of ADC_CLK1 for ana_misc. [0]: Gating. [1]: Inverse. [2]: DFT clock. [3]: Reserved.
	CKG_ADCD0[3:0]	3:0	Clock control of ADC_CLK0 for ana_misc. [0]: Gating. [1]: Inverse. [2]: DFT clock. [3]: Reserved.
2Dh (1E5Bh)	-	7:0	Default : - Access : -
	-	-	Reserved.
2Eh	REG1E5C	7:0	Default : 0x01 Access : R/W

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
(1E5Ch)	-	7:4	Reserved.	
	CKG_VIF_DAC[3:0]	3:0	Clock control of vif_dac for ana_misc. [0]: Gating. [1]: Inverse. [2]: DFT clock. [3]: Reserved.	
2Fh (1E5Eh)	REG1E5E	7:0	Default : 0x01	Access : R/W
	-	7:4	Reserved.	
	CKG_DOT_MINI_PRE[3:0]	3:0	Clock control for timing improvement of MOD output port. [0]: Gating. [1]: Inverse. [2]: 0:select lpll clk for lvds, 1: select fifo clk for tcon. [3]: 0: select bit2 source,1:DFT clock.	
32h (1E64h)	REG1E64	7:0	Default : 0x11	Access : R/W
	CKG_FT0LB2[3:0]	7:4		
	CKG_OSD2[3:0]	3:0		
32h (1E65h)	REG1E65	7:0	Default : 0x01	Access : R/W
	-	7	Reserved.	
	CKG_OSD2_SEL[2:0]	6:4		
	CKG_CA0LB2[3:0]	3:0		
33h (1E66h)	REG1E66	7:0	Default : 0x00	Access : RO
	FCIE_GPIO_IN[7:0]	7:0	Reserved.	
33h (1E67h)	REG1E67	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	FCIE_GPIO_IN[9:8]	1:0	See description of '1E66h'.	
34h (1E68h)	REG1E68	7:0	Default : 0x00	Access : R/W
	FCIE_GPIO_OUT[7:0]	7:0	Reserved.	
34h (1E69h)	REG1E69	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	FCIE_GPIO_OUT[9:8]	1:0	See description of '1E68h'.	
35h (1E6Ah)	REG1E6A	7:0	Default : 0xFF	Access : R/W
	FCIE_GPIO_OEN[7:0]	7:0	Reserved.	
35h	REG1E6B	7:0	Default : 0x03	Access : R/W

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
(1E6Bh)	-	7:2	Reserved.
	FCIE_GPIO_OEN[9:8]	1:0	See description of '1E6Ah'.
36h (1E6Ch)	REG1E6C	7:0	Default : 0x00 Access : RO
	TSO_GPIO_IN[7:0]	7:0	Readback when the dbus pads are used as GPIO. [3:0]: PAD_AD[3:0]_C. [4]: PAD_WRZ_C. [5]: PAD_RDZ_C. [6]: PAD_ALE_C. [10:7]: reserved.
36h (1E6Dh)	REG1E6D	7:0	Default : 0x00 Access : RO
	-	7:3	Reserved.
	TSO_GPIO_IN[10:8]	2:0	See description of '1E6Ch'.
37h (1E6Eh)	REG1E6E	7:0	Default : 0x00 Access : R/W
	TSO_GPIO_OUT[7:0]	7:0	[6:0]: oen control when the dbus pads are used as GPIO. [3:0]: PAD_AD[3:0]_OEN. [4]: PAD_WRZ_OEN. [5]: PAD_RDZ_OEN. [6]: PAD_ALE_OEN. [7]: Reserved. [8]: Reserved [PAD_AD*, PAD_WRZ, PAD_RDZ, PAD_ALE is used as GPIO (reg_GPIOECO_4)]. [9]: Reserved [PAD_SAR* is used as GPIO (reg_GPIOECO_2)]. [10]: Reserved [PAD_PWM* is used as GPIO(reg_GPIOECO_3)].
37h (1E6Fh)	REG1E6F	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	TSO_GPIO_OUT[10:8]	2:0	See description of '1E6Eh'.
38h (1E70h)	REG1E70	7:0	Default : 0x00 Access : R/W
	TSO_GPIO_OEN[7:0]	7:0	PAD_GPIOD[1:0] control. [0]: PAD_GPIOD0 drive. [1]: PAD_GPIOD0 pull down. [2]: PAD_GPIOD0 pull high. [3]: PAD_GPIOD0 pull high pci. [4]: PAD_GPIOD1 drv. [5]: PAD_GPIOD1 pull down. [6]: PAD_GPIOD1 pull high.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			[7]: PAD_GPIOD1 pull high pci.
38h (1E71h)	REG1E71	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	TS0_GPIO_OEN[10:8]	2:0	See description of '1E70h'.
39h (1E72h)	REG1E72	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	TS1_GPIO_IN[3:0]	3:0	[0]: PAD_INT_C readback when PAD_INT is used as GPIO. [3:1]: reserved.
3Ah (1E74h)	REG1E74	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	TS1_GPIO_OUT[3:0]	3:0	[0]: OEN control when PAD_INT is GPIO. [1]: I control when PAD_INT is GPIO. [3:2]: reserved.
3Bh (1E76h)	REG1E76	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	TS1_GPIO_OEN[3:0]	3:0	PAD_GPIOD2 control. [0]: PAD_GPIOD2 drive. [1]: PAD_GPIOD2 pull down. [2]: PAD_GPIOD2 pull high. [3]: PAD_GPIOD2 pull high pci.
3Ch (1E78h)	REG1E78	7:0	Default : 0x00 Access : RO
	DI_GPIO_IN[7:0]	7:0	Reserved.
3Ch (1E79h)	REG1E79	7:0	Default : 0x00 Access : RO
	-	7:1	Reserved.
	DI_GPIO_IN[8]	0	See description of '1E78h'.
3Dh (1E7Ah)	REG1E7A	7:0	Default : 0x00 Access : R/W
	DI_GPIO_OUT[7:0]	7:0	[6:0]: I control when the following pads use as GPIO. [3:0]: PAD_AD[3:0]_I. [4]: PAD_WRZ_I. [5]: PAD_RDZ_I. [6]: PAD_ALE_I. [7]: Reserved. [8]: Reserved [{PAD_LVSYNC, PAD_LHSYNC, PAD_LCK_ODD} is GPIO(reg_GPIOECO_5)].

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
3Dh (1E7Bh)	REG1E7B	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	DI_GPIO_OUT[8]	0	See description of '1E7Ah'.
3Eh (1E7Ch)	REG1E7C	7:0	Default : 0x00 Access : R/W
	DI_GPIO_OEN[7:0]	7:0	PAD_GPIOD[4:3] control. [0]: PAD_GPIOD3 drive. [1]: PAD_GPIOD3 pull down. [2]: PAD_GPIOD3 pull high. [3]: PAD_GPIOD3 pull high pci. [4]: PAD_GPIOD4 drv. [5]: PAD_GPIOD4 pull down. [6]: PAD_GPIOD4 pull high. [7]: PAD_GPIOD4 pull high pci. [8]: Reserved.
3Eh (1E7Dh)	REG1E7D	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	DI_GPIO_OEN[8]	0	See description of '1E7Ch'.
3Fh (1E7Eh)	REG1E7E	7:0	Default : 0x00 Access : RO
	I2S_GPIO_IN[7:0]	7:0	[3:0]: PAD_SAR[3:0]_C readback when PAD_SAR[3:0] is GPIO. [7:4]: reserved.
3Fh (1E7Fh)	REG1E7F	7:0	Default : 0x00 Access : RO
	-	7:1	Reserved.
	I2S_GPIO_IN[8]	0	See description of '1E7Eh'.
40h (1E80h)	REG1E80	7:0	Default : 0x00 Access : R/W
	I2S_GPIO_OUT[7:0]	7:0	[3:0]: OEN control when PAD_SAR[3:0] is GPIO. [7:4]: I control when PAD_SAR[3:0] is GPIO. [8]: PAD_INT is GPIO(reg_GPIOECO_1).
40h (1E81h)	REG1E81	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	I2S_GPIO_OUT[8]	0	See description of '1E80h'.
41h (1E82h)	REG1E82	7:0	Default : 0x00 Access : R/W
	I2S_GPIO_OEN[7:0]	7:0	PAD_GPIOD[6:5] control. [0]: PAD_GPIOD5 drive. [1]: PAD_GPIOD5 pull down.

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
			[2]: PAD_GPIOD5 pull high. [3]: PAD_GPIOD5 pull high pci. [4]: PAD_GPIOD6 drv. [5]: PAD_GPIOD6 pull down. [6]: PAD_GPIOD6 pull high. [7]: PAD_GPIOD6 pull high pci. [8]: Reserved.	
41h (1E83h)	REG1E83	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	I2S_GPIO_OEN[8]	0	See description of '1E82h'.	
42h (1E84h)	REG1E84	7:0	Default : 0x00	Access : RO
	PCI_GPIO_IN[7:0]	7:0	[3:0] PAD_PWM[3:0]_C readback when PAD_PWM is GPIO. [8]: PAD_LCK_ODD_C readback when PAD_LCK_ODD is GPIO. [9]: PAD_LHSYNC_C readback when PAD_LHSYNC is GPIO. [10]: PAD_LVSYNC_C readback when PAD_LVSYNC is GPIO. [11] PAD_LDE C readback when it is GPIO. others: Reserved.	
42h (1E85h)	REG1E85	7:0	Default : 0x00	Access : RO
	PCI_GPIO_IN[15:8]	7:0	See description of '1E84h'.	
43h (1E86h)	REG1E86	7:0	Default : 0x00	Access : RO
	PCI_GPIO_IN[23:16]	7:0	See description of '1E84h'.	
43h (1E87h)	REG1E87	7:0	Default : 0x00	Access : RO
	PCI_GPIO_IN[31:24]	7:0	See description of '1E84h'.	
44h (1E88h)	REG1E88	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	PCI_GPIO_IN[33:32]	1:0	See description of '1E84h'.	
45h (1E8Ah)	REG1E8A	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OUT[7:0]	7:0	[3:0]: OEN control when PAD_PWM[3:0] is GPIO. [7:4]: I control when PAD_PWM[3:0] is GPIO. [10:8]: OEN control when {PAD_LVSYNC,PAD_LHSYNC,PAD_LCK_ODD} is GPIO. [11] PAD_LDE OEN control when it is GPIO.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
			[14:12]: I control when {PAD_LVSYNC, PAD_LHSYNC, PAD_LCK_ODD} is GPIO. [15] PAD_LDE I control when it is GPIO. others: Reserved.
45h (1E8Bh)	REG1E8B	7:0	Default : 0x00 Access : R/W
	PCI_GPIO_OUT[15:8]	7:0	See description of '1E8Ah'.
46h (1E8Ch)	REG1E8C	7:0	Default : 0x00 Access : R/W
	PCI_GPIO_OUT[23:16]	7:0	See description of '1E8Ah'.
46h (1E8Dh)	REG1E8D	7:0	Default : 0x00 Access : R/W
	PCI_GPIO_OUT[31:24]	7:0	See description of '1E8Ah'.
47h (1E8Eh)	REG1E8E	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	PCI_GPIO_OUT[33:32]	1:0	See description of '1E8Ah'.
48h (1E90h)	REG1E90	7:0	Default : 0x00 Access : R/W
	PCI_GPIO_OEN[7:0]	7:0	PAD_GPIOD7 control. [0]: PAD_GPIOD7 drive. [1]: PAD_GPIOD7 pull down. [2]: PAD_GPIOD7 pull high. [3]: PAD_GPIOD7 pull high pci. PAD_AD0 control. [4]: PAD_AD0 drive. [5]: PAD_AD0 pull down. [6]: PAD_AD0 pull high. [7]: PAD_AD0 pull high pci. PAD_AD1 control. [8]: PAD_AD1 drive. [9]: PAD_AD1 pull down. [10]: PAD_AD1 pull high. [11]: PAD_AD1 pull high pci. PAD_AD2 control. [12]: PAD_AD2 drive. [13]: PAD_AD2 pull down. [14]: PAD_AD2 pull high. [15]: PAD_AD2 pull high pci. [33:16]: reserved.
48h (1E91h)	REG1E91	7:0	Default : 0x00 Access : R/W
	PCI_GPIO_OEN[15:8]	7:0	See description of '1E90h'.

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
49h (1E92h)	REG1E92	7:0	Default : 0x00	Access : R/W
	PCI_GPIO_OEN[23:16]	7:0	See description of '1E90h'.	
49h (1E93h)	REG1E93	7:0	Default : 0xFC	Access : R/W
	PCI_GPIO_OEN[31:24]	7:0	See description of '1E90h'.	
4Ah (1E94h)	REG1E94	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	PCI_GPIO_OEN[33:32]	1:0	See description of '1E90h'.	
4Bh ~ 4Bh (1E96h ~ 1E97h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
50h (1EA0h)	REG1EA0	7:0	Default : 0x00	Access : R/W
	I2S_OUT2[3:0]	7:4	Selection of specify 4 pads as I2S out2 function. 0: Disable. others: See GPIO table.	
	SPDIF[3:0]	3:0	Selection of specify 2 pads as SPDIF function. 0: Disable. others: See GPIO table.	
50h (1EA1h)	REG1EA1	7:0	Default : 0x00	Access : R/W
	USB2_DRVVBUS[3:0]	7:4	Selection of specify 1 pads as usb2.0 drvbus function. 0: Disable. others: See GPIO table.	
	USB1_DRVVBUS[3:0]	3:0	Selection of specify 1 pads as usb1.1 drvbus function. 0: Disable. others: See GPIO table.	
51h (1EA2h)	REG1EA2	7:0	Default : 0x00	Access : R/W
	TCON_DRV[7:0]	7:0	Tcon0~21 current driving control.	
51h (1EA3h)	REG1EA3	7:0	Default : 0x00	Access : R/W
	TCON_DRV[15:8]	7:0	See description of '1EA2h'.	
52h (1EA4h)	REG1EA4	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TCON_DRV[21:16]	5:0	See description of '1EA2h'.	
52h (1EA5h)	REG1EA5	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TCON_GPIO_GROUP[5:0]	5:0	Tcon gpio control (0:tcon, 1:gpio).	

CHIPTOP Register (Bank = 1E)				
Index (Absolute)	Mnemonic	Bit	Description	
			[0]: Control tcon0~3. [1]: Control tcon4~7. [2]: Control tcon8~11. [3]: Control tcon12~15. [4]: Control tcon16~19. [5]: Control tcon20, 21.	
53h (1EA6h)	REG1EA6	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DHC_RESET	2	DHC reset signal, active high.	
	-	1:0	Reserved.	
54h (1EA8h)	REG1EA8	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	DI_CLK_INV	5	DI_CLK invert.	
	SEL_DI_DDR	4	DIN ddr select.: 0: Select sdr signals. 1: Select ddr signals.	
	DI_CLK_SEL[3:0]	3:0	DI_CLK delay level selection.	
54h (1EA9h)	REG1EA9	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	DO_CLK_INV	5	DOUT_CLK invert.	
	DOUT_SRC_SEL	4	DOUT ddr select.: 0: Select sdr signals. 1: Select ddr signals.	
	DO_CLK_SEL[3:0]	3:0	DOUT_CLK delay level selection.	
55h (1EAAh)	REG1EAA	7:0	Default : 0x20	Access : R/W
	UART_SEL1[2:0]	7:5	Uart selection1. 0: Hk_51 uart0; 1: hk_51 uart1; 2: vd_51 uart0; 3: aeon; 4: tsp.	
	UART_SELO[2:0]	4:2	Uart selection0. 0: Hk_51 uart0; 1: hk_51 uart1; 2: vd_51 uart0; 3: aeon; 4: tsp.	
	JTAG_SEL[1:0]	1:0	Jtag selection. 0: 8051; 1: Aeon; 2: TSP.	
56h (1EACH)	REG1EAC	7:0	Default : 0x00	Access : RO
	GPIOA_IN[7:0]	7:0	Readback of GPIOA_C.	

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
56h (1EADh)	REG1EAD	7:0	Default : 0x00 Access : RO
	GPIOL_IN[4:0]	7:3	Readback of GPIOL_C.
	GPIOA_IN[10:8]	2:0	See description of '1EACH'.
57h (1EAEh)	REG1EAE	7:0	Default : 0x00 Access : RO
	GPIOB_IN[7:0]	7:0	Readback of GPIOB_C.
57h (1EAFh)	REG1EAF	7:0	Default : 0x00 Access : RO
	GPIOB_IN[15:8]	7:0	See description of '1EAEh'.
58h (1EB0h)	REG1EB0	7:0	Default : 0x00 Access : RO
	GPIOD_IN[7:0]	7:0	Readback of GPIOD_C.
58h (1EB1h)	REG1EB1	7:0	Default : 0x00 Access : RO
	GPIOD_IN[15:8]	7:0	See description of '1EB0h'.
59h (1EB2h)	REG1EB2	7:0	Default : 0x00 Access : RO
	GPIOM_IN[3:0]	7:4	Readback of GPIOM_C.
	-	3	Reserved.
	GPIOD_IN[18:16]	2:0	See description of '1EB0h'.
59h (1EB3h)	REG1EB3	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	GPIOT_IN[3:0]	3:0	Readback of GPIOT_C.
5Ah (1EB4h)	REG1EB4	7:0	Default : 0x00 Access : RO
	GPIOR_IN[7:0]	7:0	Readback of GPIOR_C.
5Ah (1EB5h)	REG1EB5	7:0	Default : 0x00 Access : RO
	-	7:3	Reserved.
	GPIOR_IN[10:8]	2:0	See description of '1EB4h'.
5Bh (1EB6h)	REG1EB6	7:0	Default : 0x00 Access : R/W
	GPIOK_OUT[7:0]	7:0	I control when specify pad_tcon as GPIOK.
5Bh (1EB7h)	REG1EB7	7:0	Default : 0x00 Access : R/W
	GPIOK_OUT[15:8]	7:0	See description of '1EB6h'.
5Ch (1EB8h)	REG1EB8	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	GPIOK_OUT[21:16]	5:0	See description of '1EB6h'.
5Dh (1EBAh)	REG1EBA	7:0	Default : 0x00 Access : R/W
	GPIOK_OEN[7:0]	7:0	OEN control when specify pad_tcon as GPIOK.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
5Dh (1EBBh)	REG1EBB	7:0	Default : 0x00 Access : R/W
	GPIOK_OEN[15:8]	7:0	See description of '1EBAh'.
5Eh (1EBCh)	REG1EBC	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	GPIOK_OEN[21:16]	5:0	See description of '1EBAh'.
5Fh (1EBEh)	REG1EBE	7:0	Default : 0x00 Access : RO
	GPIOK_IN[7:0]	7:0	Readback of GPIOK_C.
5Fh (1EBFh)	REG1EBF	7:0	Default : 0x00 Access : RO
	GPIOK_IN[15:8]	7:0	See description of '1EBEh'.
60h (1EC0h)	REG1EC0	7:0	Default : 0x00 Access : RO
	-	7:6	Reserved.
	GPIOK_IN[21:16]	5:0	See description of '1EBEh'.
62h (1EC4h)	REG1EC4	7:0	Default : 0x00 Access : R/W
	VDD2LOW_CTRL[7:0]	7:0	VDD2LOW_CTRL. [5:0]: power off period selection. 0 => pwroff with 2.2us. 1 => pwroff with 4.4us. 2 => pwroff with 9.0us. 3 => pwroff with 17.9us. 4 => pwroff with 39.8us. 5 => pwroff with 71.6us. [6]: Enable power too low reset. [7]: Clear interrupt of "pwr is no good".
63h (1EC6h)	REG1EC6	7:0	Default : 0x00 Access : R/W
	BOND_OV_KEY[7:0]	7:0	Set bonding overwrite key.
63h (1EC7h)	REG1EC7	7:0	Default : 0x00 Access : R/W
	BOND_OV_KEY[15:8]	7:0	See description of '1EC6h'.
65h (1ECAh)	REG1ECA	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	CHIP_CONFIG_STAT[3:0]	3:0	CHIP_CONFIG status.
66h (1ECCh)	REG1ECC	7:0	Default : 0x00 Access : RO
	DEVICE_ID[7:0]	7:0	Device id.
66h (1ECDh)	REG1ECD	7:0	Default : 0x00 Access : RO
	DEVICE_ID[15:8]	7:0	See description of '1ECCh'.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
67h (1ECEh)	REG1ECE	7:0	Default : 0x00 Access : RO
	CHIP_VERSION[7:0]	7:0	CHIP_VERSION.
67h (1ECFh)	REG1ECF	7:0	Default : 0x00 Access : RO
	CHIP_REVISION[7:0]	7:0	CHIP_REVISION.
68h (1ED0h)	REG1ED0	7:0	Default : 0x00 Access : R/W
	BOND_OV_EN[7:0]	7:0	Bonding overwrite enable.
68h (1ED1h)	REG1ED1	7:0	Default : 0x00 Access : R/W
	BOND_OV_EN[15:8]	7:0	See description of '1ED0h'.
69h (1ED2h)	REG1ED2	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	BOND_OV_EN[16]	0	See description of '1ED0h'.
6Ah (1ED4h)	REG1ED4	7:0	Default : 0x00 Access : R/W
	BOND_OV[7:0]	7:0	Bonding overwrite value.
6Ah (1ED5h)	REG1ED5	7:0	Default : 0x00 Access : R/W
	BOND_OV[15:8]	7:0	See description of '1ED4h'.
6Bh (1ED6h)	REG1ED6	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	BOND_OV[16]	0	See description of '1ED4h'.
6Ch (1ED8h)	REG1ED8	7:0	Default : 0x00 Access : RO
	STAT_BOND[7:0]	7:0	Bonding status readback.
6Ch (1ED9h)	REG1ED9	7:0	Default : 0x00 Access : RO
	STAT_BOND[15:8]	7:0	See description of '1ED8h'.
6Dh (1EDAh)	REG1EDA	7:0	Default : 0x00 Access : RO
	-	7:1	Reserved.
	STAT_BOND[16]	0	See description of '1ED8h'.
70h (1EE0h)	REG1EE0	7:0	Default : 0x00 Access : R/W
	GPIOR_OUT[7:0]	7:0	I control when specify pad_gpior as GPIOR.
70h (1EE1h)	REG1EE1	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	GPIOR_OUT[10:8]	2:0	See description of '1EE0h'.
71h (1EE2h)	REG1EE2	7:0	Default : 0xFF Access : R/W
	GPIOR_OEN[7:0]	7:0	OEN control when specify pad_gpior as GPIOR.

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
71h (1EE3h)	REG1EE3	7:0	Default : 0x07 Access : R/W
	-	7:3	Reserved.
	GPIOR_OEN[10:8]	2:0	See description of '1EE2h'.
72h ~ 75h (1EE4h ~ 1EEAh)	-	7:0	Default : - Access : -
	-	-	Reserved.
75h (1EEBh)	REG1EEB	7:0	Default : 0x00 Access : R/W
	ROSC_IN_SEL	7	Select the input source of ring oscillator in chip_conf. 1: Close-loop (enable ring oscillator). 0: Open-loop (input from external digital input).
	-	6:0	Reserved.
76h (1EECh)	REG1EEC	7:0	Default : 0x00 Access : R/W
	UART_INNER_LOOPBACK[4:0]	7:3	
	-	2:0	Reserved.
76h (1EEDh)	REG1EED	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	UART_PAD_INVERSE[1:0]	3:2	
	UART_OUTER_LOOPBACK[1:0]	1:0	
77h (1EEEh)	REG1EEE	7:0	Default : 0x00 Access : R/W
	BIST2_SEL[7:0]	7:0	Real speed BIST engine.
77h (1EEFh)	REG1EEF	7:0	Default : 0x00 Access : R/W
	BIST2_SEL[15:8]	7:0	See description of '1EEEh'.
78h (1EF0h)	REG1EF0	7:0	Default : 0x00 Access : R/W
	W_DUMMY0[7:0]	7:0	Dummy0 write value.
78h (1EF1h)	REG1EF1	7:0	Default : 0x00 Access : R/W
	W_DUMMY0[15:8]	7:0	See description of '1EF0h'.
79h (1EF2h)	REG1EF2	7:0	Default : 0x00 Access : R/W
	W_DUMMY1[7:0]	7:0	Dymmy1 write value.
79h (1EF3h)	REG1EF3	7:0	Default : 0x00 Access : R/W
	W_DUMMY1[15:8]	7:0	See description of '1EF2h'.
7Ah (1EF4h)	REG1EF4	7:0	Default : 0x00 Access : RO
	R_DUMMY0[7:0]	7:0	Dummy0 status readback.
7Ah	REG1EF5	7:0	Default : 0x00 Access : RO

CHIPTOP Register (Bank = 1E)

Index (Absolute)	Mnemonic	Bit	Description
(1EF5h)	R_DUMMY0[15:8]	7:0	See description of '1EF4h'.
7Bh (1EF6h)	REG1EF6	7:0	Default : 0x00
	R_DUMMY1[7:0]	7:0	Dummy1 status readback.
7Bh (1EF7h)	REG1EF7	7:0	Default : 0x00
	R_DUMMY1[15:8]	7:0	See description of '1EF6h'.
7Ch (1EF8h)	REG1EF8	7:0	Default : 0x00
	R_DUMMY2[7:0]	7:0	Dummy2 status readback.
7Ch (1EF9h)	REG1EF9	7:0	Default : 0x00
	R_DUMMY2[15:8]	7:0	See description of '1EF8h'.
7Dh (1EFAh)	REG1EFA	7:0	Default : 0x00
	R_DUMMY3[7:0]	7:0	Dummy3 status readback.
7Dh (1EFBh)	REG1EFB	7:0	Default : 0x00
	R_DUMMY3[15:8]	7:0	See description of '1EFAh'.

OSD_TST Register (Bank = 1F)

OSD_TST Register (Bank = 1F)				
Index (Absolute)	Mnemonic	Bit	Description	
02h (1F04h)	REG1F04	7:0	Default : 0x00	Access : R/W
	027_PAL_EXTEND	7	Osd palette extend.	
	-	6:0	Reserved.	
02h ~ 0Dh (1F05h ~ 1F1Ah)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Dh (1F1Bh)	REG1F1B	7:0	Default : 0x00	Access : R/W
	0DF_GATE_ODCLK	7	Power down OSD srams.	
	-	6	Reserved.	
	0DC_PDSRAM[1:0]	5:4	OSD sram power down mode.	
	0DB_CCTTRAN_EN	3	CC transparent enable.	
	-	2:0	Reserved.	
0Eh (1F1Ch)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Fh (1F1Eh)	REG1F1E	7:0	Default : 0x00	Access : RO
	0F0_OSD_BIST_FAIL[7:0]	7:0	OSD SRAM BIST FAIL. [0]: Caram. [1]: Fram. [2]: Cpram. [7]: OSD.	
0Fh (1F1Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Fh (1F1Fh)	REG1F1F	7:0	Default : 0x00	Access : R/W
	0F8_TEST_DUMMY1[7:0]	7:0	Test pattern dummy register 2. [0]: Ip hsync invert. [1]: Ip vsync invert. [2]: Internal OSD hsync invert. [3]: Internal OSD vsync invert. [4]: Field input select. 0=from OP; 1=from IP.	
11h (1F23h)	REG1F23	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	119_SOC	1	OSDSUB0C=OSD Sub window 0 Color select. 0: From OSD Sub window 0 attribute.	

OSD_TST Register (Bank = 1F)				
Index (Absolute)	Mnemonic	Bit	Description	
			1: From attribute RAM.	
	118_S0E	0	OSDSUB0E=Enable OSD Sub window 0. 0: Disable. 1: Enable.	
12h (1F24h)	REG1F24	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	120_SW0HST[6:0]	6:0	[6:0]:OSDSUB0HST[6:0]=OSD Sub Window 0 Horizontal Start Position.	
12h (1F25h)	REG1F25	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	128_SW0HEND[6:0]	6:0	[6:0]:OSDSUB0HEND[6:0]=OSD Sub Window 0 Horizontal End Position.	
13h (1F26h)	REG1F26	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	130_SW0VST[5:0]	5:0	[5:0]:OSDSUB0VST[5:0]=OSD Sub Window 0 Vertical Start Position.	
13h (1F27h)	REG1F27	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	138_SW0VEND[5:0]	5:0	[5:0]:OSDSUB0VEND[5:0]=OSD Sub Window 0 Vertical End Position.	
14h (1F28h)	REG1F28	7:0	Default : 0x00	Access : R/W
	140_SW0_ATR[7:0]	7:0	[7:4]:FGCLR[3:0]=OSD Sub window 0 Foreground Color select. 0000: Color index 0. 0001: Color index 1. 1110: Color index E. [3:0]:BGCLR[3:0]=OSD Sub window 0 Background Color select. 0000: Color index 0. 0001: Color index 1. 1110: Color index E. 1111: Color index F.	
14h (1F29h)	REG1F29	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	149_S1C	1	OSDSUB1C=OSD Sub window 1 Color select.	
	148_S1E	0	OSDSUB1E=Enable OSD Sub window 1.	

OSD_TST Register (Bank = 1F)				
Index (Absolute)	Mnemonic	Bit	Description	
15h (1F2Ah)	REG1F2A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	150_SW1HST[6:0]	6:0	[6:0]:OSDSUB1HST[6:0]=Sub Window 1 Horizontal Start Position.	
15h (1F2Bh)	REG1F2B	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	158_SW1HEND[6:0]	6:0	[6:0]:OSDSUB1HEND[6:0]=OSD Sub Window 1 Horizontal End Position.	
16h (1F2Ch)	REG1F2C	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	160_SW1VST[5:0]	5:0	[5:0]:OSDSUB1VST[5:0]=OSD Sub Window 1 Vertical Start Position.	
16h (1F2Dh)	REG1F2D	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	168_SW1VEND[5:0]	5:0	[5:0]:OSDSUB1VEND[5:0]=OSD Sub Window 1 Vertical End Position.	
17h (1F2Eh)	REG1F2E	7:0	Default : 0x00	Access : R/W
	170_SW1_ATR[7:0]	7:0	[7:4]:FGCLR[3:0]=OSD Sub window 1 Foreground Color select. 0000: Color index 0. 0001: Color index 1. 1111: Color index F. [3:0]:BGCLR[3:0]=OSD Sub window 1 Background Color select. 0000: Color index 0. 0001: Color index 1. 1110: Color index E. 1111: Color index F.	
17h (1F2Fh)	REG1F2F	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	179_S2C	1	OSDSUB2C=OSD Sub window 2 Color select.	
	178_S2E	0	OSDSUB2E=Enable OSD Sub window 2.	
18h (1F30h)	REG1F30	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	180_SW2HST[6:0]	6:0	[6:0]:OSDSUB2HST[6:0]=OSD Sub Window 2 Horizontal Start Position.	

OSD_TST Register (Bank = 1F)				
Index (Absolute)	Mnemonic	Bit	Description	
18h (1F31h)	REG1F31	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	188_SW2HEND[6:0]	6:0	[6:0]:OSDSUB2HEND[6:0]=OSD Sub Window 2 Horizontal End Position.	
19h (1F32h)	REG1F32	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	190_SW2VST[5:0]	5:0	[5:0]:OSDSUB2VST[5:0]=OSD Sub Window 2 Vertical Start Position.	
19h (1F33h)	REG1F33	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	198_SW2VEND[5:0]	5:0	[5:0]:OSDSUB2VEND[5:0]=OSD Sub Window 2 Vertical End Position.	
1Ah (1F34h)	REG1F34	7:0	Default : 0x00	Access : R/W
	1A0_SW2_ATR[7:0]	7:0	[7:4]:FGCLR[3:0]=OSD Sub window 2 Foreground Color select. 0000: Color index 0. 0001: Color index 1. 1111: Color index F. [3:0]:BGCLR[3:0]=OSD Sub window 2 Background Color select. 0000: Color index 0. 0001: Color index 1. 1110: Color index E. 1111: Color index F.	
1Ah (1F35h)	REG1F35	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	1A9_S3C	1	OSDSUB3C=OSD Sub window 3 Color select.	
	1A8_S3E	0	OSDSUB3E=Enable OSD Sub window 3.	
1Bh (1F36h)	REG1F36	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	1B0_SW3HST[6:0]	6:0	[6:0]:OSDSUB3HST[6:0]=OSD Sub Window 3 Horizontal Start Position.	
1Bh (1F37h)	REG1F37	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	1B8_SW3HEND[6:0]	6:0	[6:0]:OSDSUB3HEND[6:0]=OSD Sub Window 3 Horizontal End Position.	

OSD_TST Register (Bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description
1Ch (1F38h)	REG1F38	7:0	Default : 0x00
	-	7:6	Reserved.
	1C0_SW3VST[5:0]	5:0	[5:0]:OSDSUB3VST[5:0]=OSD Sub Window 3 Vertical Start Position.
1Ch (1F39h)	REG1F39	7:0	Default : 0x00
	-	7:6	Reserved.
	1C8_SW3VEND[5:0]	5:0	[5:0]:OSDSUB3VEND[5:0]=OSD Sub Window 3 Vertical End Position.
1Dh (1F3Ah)	REG1F3A	7:0	Default : 0x00
	1D0_SW3_ATR[7:0]	7:0	[7:4]:FGCLR[3:0]=OSD Sub window 3 Foreground Color select. 0000: Color index 0. 0001: Color index 1. 1111: Color index F. [3:0]:BGCLR[3:0]=OSD Sub window 3 Background Color select. 0000: Color index 0. 0001: Color index 1. 1110: Color index E. 1111: Color index F.
1Dh (1F3Bh)	REG1F3B	7:0	Default : 0x00
	1D8_CTRL0_REG[7:0]	7:0	3b[7:0]. [7]: OSD fwresetz. [2]: ltp_fscr. [1:0]: tg_win.
1Eh (1F3Ch)	REG1F3C	7:0	Default : 0x00
	1E8_CTRL1_REG[7:0]	7:0	3c[7:0]. [3]: M4c_start_bit9. [7]: M8c_start_bit9.

BK7 Register (Bank = 21)

BK7 Register (Bank = 21)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2100h)	REG2100	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CEC_TX_LEN[3:0]	3:0	The number byte of data that initiator want to send. Write this register to trigger a new TX request. 0: Only header block is to send.	
00h (2101h)	REG2101	7:0	Default : 0x03	Access : R/W
	CEC_SAMPLE_SEL[2:0]	7:5	Sample times select for CEC line high/low detection. 000: 1X. 001: 2X. 010: 4X. &&&. 110: 12X. 111: 14X.	
	TX_LOW_BIT_SEL[1:0]	4:3	The period select for follower generating a low bit period when the current received bit is too short to be a valid bit. 00: 1X nominal data bit period. 01: 1.4X nominal data bit period. 10: 1.5X nominal data bit period. 11: 1.6X nominal data bit period.	
	RETRY_CNT[2:0]	2:0	The retry times for re-transmitting a message (MAX).	
01h (2102h)	REG2102	7:0	Default : 0x00	Access : R/W
	CEC_CTRL_EN	7	Enable CEC controller. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	CEC_CLK_GATE	5	CEC main clock input is gated or not. 0: No gate. 1: Gate.	
	CANCEL_TX_REQ	4	Cancel current TX request. 0: Normal. 1: Cancel.	
	TX_FALLING_SHIFT_SEL[1:0]	3:2	TX falling edge is shifted backward. 00 = 0us. 01 = 50us. 10 = 100us. 11 = 200us.	

BK7 Register (Bank = 21)

Index (Absolute)	Mnemonic	Bit	Description
	TX_RISING_SHIFT_SEL[1:0]	1:0	TX rising edge is shifted backward. 00 = 0us. 01 = 50us. 10 = 100us. 11 = 200us.
01h (2103h)	REG2103	7:0	Default : 0x53
	CEC_FREE_CNT2[3:0]	7:4	The necessary free bit period when new initiator wants to send a frame.
	CEC_FREE_CNT1[3:0]	3:0	The necessary free bit period when pervious attempt to send frame unsuccessful.
02h (2104h)	REG2104	7:0	Default : 0x07
	CEC_LOGICAL_ADDR[3:0]	7:4	Device logical address.
	CEC_FREE_CNT3[3:0]	3:0	The necessary free bit period when present initiator wants to send another frame immediately after its previous frame.
02h (2105h)	REG2105	7:0	Default : 0x8C
	CNT_10US_VALUE[7:0]	7:0	Number of counts to achieve 10us (Integer part). 0: 256 clock cycles. 1: 1 clock cycle. 2: 2 clock cycles. &&. 255: 255 clock cycles. (Unit: clock cycle).
03h (2106h)	REG2106	7:0	Default : 0x03
	RX_BOUND_SHIFT[3:0]	7:4	RX upper/lower bound is shifted forward/backward N*10us.
	F_CNT_10US_VALUE[3:0]	3:0	Number of counts to achieve 10us (Fractional part). This part is useless when CNT_10US_VALUE=1 (clock cycle). (Unit: 0.0625 clock cycle).
03h (2107h)	REG2107	7:0	Default : 0x08
	IGNORE_UNEXP_OP_LEN	7	Ignore un-expected length for opcode0~3.
	NSUP_CMD_ACT[1:0]	6:5	Action for non-supported command. 00: Ignore and ACK. 01: NACK. 1x: Feature abort.
	CEC_CTRL_SEL	4	Select which CEC controller is active. 0: Normal CEC controller.

BK7 Register (Bank = 21)

Index (Absolute)	Mnemonic	Bit	Description
			1: Power down hardware CEC controller.
	LOST_AB_TSEL	3	Cancel TX request or retry if TX lost arbitration to a second initiator. 0: Retry. 1: Cancel.
	CEC_OVERRIDE_FUN	2	Force CEC line low. 0: Disable. 1: Enable.
	-	1	Reserved.
	DIS_EH	0	Disable CEC error handling. 0: Normal. 1: Disable.
04h (2108h)	REG2108	7:0	Default : 0x00 Access : RO
	HW_CEC_STS	7	Hardware CEC controller status. 0: Busy. 1: Idle.
	CEC_TX_REQ_STS	6	Indicate the TX request status. (Read only). 0: End. 1: On going.
	CEC_LINE	5	CEC line status.
	CEC_RX_LEN[4:0]	4:0	The length of received message. Read only. 0: Only header block is received.
04h (2109h)	REG2109	7:0	Default : 0x00 Access : RO
	-	7:1	Reserved.
	CHKSM_CMP_ERR_STS	0	The event status bit for checksum error.
05h ~ 06h (210Ah ~ 210Dh)	-	7:0	Default : - Access : -
	-	-	Reserved.
07h (210Eh)	REG210E	7:0	Default : 0x00 Access : R/W
	WAKEUP_INT_MASK	7	Mask wakeup event interrupt.
	OP3_OPERAND1_EN	6	Wakeup enable for the second operand specific to opcode 3.
	OP2_OPERAND1_EN	5	Wakeup enable for the second operand specific to opcode 2.

BK7 Register (Bank = 21)

Index (Absolute)	Mnemonic	Bit	Description
	OP_EN[4:0]	4:0	Wakeup enable for opcode 0~4.
07h (210Fh)	REG210F	7:0	Default : 0x00 Access : R/W
	EXP_OP4_LEN[3:0]	7:4	Expected RX length for opcode 4. Header and opcode are not included.
	OPERAND_EN[3:0]	3:0	Wakeup enable for operand specific to opcode 0~3.
08h (2110h)	REG2110	7:0	Default : 0x00 Access : R/W
	OPCODE0[7:0]	7:0	Revive opcode 0 to wakeup.
08h (2111h)	REG2111	7:0	Default : 0x00 Access : R/W
	OPCODE1[7:0]	7:0	Revive opcode 1 to wakeup.
09h (2112h)	REG2112	7:0	Default : 0x00 Access : R/W
	OPCODE2[7:0]	7:0	Revive opcode 2 to wakeup.
09h (2113h)	REG2113	7:0	Default : 0x00 Access : R/W
	OPCODE3[7:0]	7:0	Revive opcode 3 to wakeup.
0Ah (2114h)	REG2114	7:0	Default : 0x00 Access : R/W
	OPCODE4[7:0]	7:0	Revive opcode 4 to wakeup.
0Ah (2115h)	REG2115	7:0	Default : 0x00 Access : R/W
	OP0_OPERAND[7:0]	7:0	Revive the operand specific to opcode 0 to wakeup.
0Bh (2116h)	REG2116	7:0	Default : 0x00 Access : R/W
	OP1_OPERAND[7:0]	7:0	Revive the operand specific to opcode 1 to wakeup.
0Bh (2117h)	REG2117	7:0	Default : 0x00 Access : R/W
	OP2_OPERAND0[7:0]	7:0	Revive the operand specific to opcode 2 to wakeup.
0Ch (2118h)	REG2118	7:0	Default : 0x00 Access : R/W
	OP2_OPERAND1[7:0]	7:0	Revive the operand specific to opcode 2 to wakeup.
0Ch (2119h)	REG2119	7:0	Default : 0x00 Access : R/W
	OP3_OPERAND0[7:0]	7:0	Revive the operand specific to opcode 3 to wakeup.
0Dh (211Ah)	REG211A	7:0	Default : 0x00 Access : R/W
	OP3_OPERAND1[7:0]	7:0	Revive the operand specific to opcode 3 to wakeup.
0Dh (211Bh)	REG211B	7:0	Default : 0x04 Access : R/W
	OP_ACC_TYPE[4:0]	7:3	Access type for opcode0~4. 0: Direct. 1: Broadcast.
	CEC_VERSION[2:0]	2:0	CEC version. 000: Version 1.1.

BK7 Register (Bank = 21)				
Index (Absolute)	Mnemonic	Bit	Description	
			001: Version 1.2. 010: Version 1.2a. 011: Version 1.3. 1xx: Version 1.3a.	
0Eh (211Ch)	REG211C	7:0	Default : 0x00	Access : R/W
	PHYSICAL_ADDR[7:0]	7:0	Device physical address.	
0Eh (211Dh)	REG211D	7:0	Default : 0x00	Access : R/W
	PHYSICAL_ADDR[15:8]	7:0	See description of '211Ch'.	
0Fh (211Eh)	REG211E	7:0	Default : 0x00	Access : R/W
	VENDOR_ID[7:0]	7:0	Device vendor ID.	
0Fh (211Fh)	REG211F	7:0	Default : 0x00	Access : R/W
	VENDOR_ID[15:8]	7:0	See description of '211Eh'.	
10h (2120h)	REG2120	7:0	Default : 0x00	Access : R/W
	VENDOR_ID[23:16]	7:0	See description of '211Eh'.	
10h (2121h)	REG2121	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ABORT_REASON[2:0]	2:0	Feature abort reason. 000: _Unrecognized opcode_. 001: _Not in correct mode to respond_. 010: _Cannot provide source_. 011: _Invalid operand_. 100: _Refused_.	
11h (2122h)	REG2122	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	WAKEUP_INT	6	Wakeup interrupt event.	
	RX_BIT_TOO_LONG	5	RX bit too long.	
	RX_BIT_TOO_SHORT	4	RX bit too short.	
	HW_RX_EVENT_STS3	3	Receive Give_Device_Vendor ID message in power down mode.	
	HW_RX_EVENT_STS2	2	Receive Get_CEC_Version message in power down mode.	
	HW_RX_EVENT_STS1	1	Receive Give_Physical_Address message in power down mode.	
11h (2123h)	REG2123	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	

BK7 Register (Bank = 21)

Index (Absolute)	Mnemonic	Bit	Description
	CEC_EVENT_INT[4:0]	4:0	CEC event status. [0]: Receive a new message successfully. [1]: Send message successfully. [2]: Retry fail. [3]: Lost arbitration to the second initiator. [4]: Follower transmits NACK.
12h (2124h)	REG2124	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CEC_EVENT_INT_FORCE[4:0]	4:0	Force CEC event interrupt.
12h (2125h)	REG2125	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CEC_EVENT_INT_CLEAR[4:0]	4:0	Clear CEC event interrupt.
13h (2126h)	REG2126	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CEC_EVENT_INT_MASK[4:0]	4:0	Mask CEC event interrupt.
14h (2128h)	REG2128	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	CEC_SRC_CK_CTRL	5	Which kind of control way is selected for source clock select? 0: Depend on CEC_CTRL_SEL bit. If CEC_CTRL_SEL=0, external XTAL clock is selected. Or internal RC OSC is selected. 1: Depend on CEC_SRC_CK_SEL bit.
	CEC_SRC_CK_SEL	4	CEC source clock select. 0: External XTAL clock. 1: Internal RC OSC.
	CHKSUM_ERR_MASK	3	Checksum error wakeup interrupt mask.
	CLR_CHKSUM_ERR	2	Clear checksum error.
	-	1:0	Reserved.
14h (2129h)	REG2129	7:0	Default : 0x00 Access : R/W
	DEV_TYPE[7:0]	7:0	CEC device type for Get_Physical_Address message.
18h (2130h)	REG2130	7:0	Default : 0x00 Access : R/W
	TX_DATA0[7:0]	7:0	Data block 0 for TX.
18h (2131h)	REG2131	7:0	Default : 0x00 Access : R/W
	TX_DATA1[7:0]	7:0	Data block 1 for TX.

BK7 Register (Bank = 21)

Index (Absolute)	Mnemonic	Bit	Description
19h (2132h)	REG2132	7:0	Default : 0x00
	TX_DATA2[7:0]	7:0	Data block 2 for TX.
19h (2133h)	REG2133	7:0	Default : 0x00
	TX_DATA3[7:0]	7:0	Data block 3 for TX.
1Ah (2134h)	REG2134	7:0	Default : 0x00
	TX_DATA4[7:0]	7:0	Data block 4 for TX.
1Ah (2135h)	REG2135	7:0	Default : 0x00
	TX_DATA5[7:0]	7:0	Data block 5 for TX.
1Bh (2136h)	REG2136	7:0	Default : 0x00
	TX_DATA6[7:0]	7:0	Data block 6 for TX.
1Bh (2137h)	REG2137	7:0	Default : 0x00
	TX_DATA7[7:0]	7:0	Data block 7 for TX.
1Ch (2138h)	REG2138	7:0	Default : 0x00
	TX_DATA8[7:0]	7:0	Data block 8 for TX.
1Ch (2139h)	REG2139	7:0	Default : 0x00
	TX_DATA9[7:0]	7:0	Data block 9 for TX.
1Dh (213Ah)	REG213A	7:0	Default : 0x00
	TX_DATA10[7:0]	7:0	Data block 10 for TX.
1Dh (213Bh)	REG213B	7:0	Default : 0x00
	TX_DATA11[7:0]	7:0	Data block 11 for TX.
1Eh (213Ch)	REG213C	7:0	Default : 0x00
	TX_DATA12[7:0]	7:0	Data block 12 for TX.
1Eh (213Dh)	REG213D	7:0	Default : 0x00
	TX_DATA13[7:0]	7:0	Data block 13 for TX.
1Fh (213Eh)	REG213E	7:0	Default : 0x00
	TX_DATA14[7:0]	7:0	Data block 14 for TX.
1Fh (213Fh)	REG213F	7:0	Default : 0x00
	TX_DATA15[7:0]	7:0	Data block 15 for TX.
20h (2140h)	REG2140	7:0	Default : 0x00
	RX_DATA0[7:0]	7:0	Data block 0 for RX.
20h (2141h)	REG2141	7:0	Default : 0x00
	RX_DATA1[7:0]	7:0	Data block 1 for RX.

BK7 Register (Bank = 21)

Index (Absolute)	Mnemonic	Bit	Description
21h (2142h)	REG2142	7:0	Default : 0x00
	RX_DATA2[7:0]	7:0	Data block 2 for RX.
21h (2143h)	REG2143	7:0	Default : 0x00
	RX_DATA3[7:0]	7:0	Data block 3 for RX.
22h (2144h)	REG2144	7:0	Default : 0x00
	RX_DATA4[7:0]	7:0	Data block 4 for RX.
22h (2145h)	REG2145	7:0	Default : 0x00
	RX_DATA5[7:0]	7:0	Data block 5 for RX.
23h (2146h)	REG2146	7:0	Default : 0x00
	RX_DATA6[7:0]	7:0	Data block 6 for RX.
23h (2147h)	REG2147	7:0	Default : 0x00
	RX_DATA7[7:0]	7:0	Data block 7 for RX.
24h (2148h)	REG2148	7:0	Default : 0x00
	RX_DATA8[7:0]	7:0	Data block 8 for RX.
24h (2149h)	REG2149	7:0	Default : 0x00
	RX_DATA9[7:0]	7:0	Data block 9 for RX.
25h (214Ah)	REG214A	7:0	Default : 0x00
	RX_DATA10[7:0]	7:0	Data block 10 for RX.
25h (214Bh)	REG214B	7:0	Default : 0x00
	RX_DATA11[7:0]	7:0	Data block 11 for RX.
26h (214Ch)	REG214C	7:0	Default : 0x00
	RX_DATA12[7:0]	7:0	Data block 12 for RX.
26h (214Dh)	REG214D	7:0	Default : 0x00
	RX_DATA13[7:0]	7:0	Data block 13 for RX.
27h (214Eh)	REG214E	7:0	Default : 0x00
	RX_DATA14[7:0]	7:0	Data block 14 for RX.
27h (214Fh)	REG214F	7:0	Default : 0x00
	RX_DATA15[7:0]	7:0	Data block 15 for RX.

ATOP Register (Bank = 25)

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2500h)	REG2500	7:0	Default : 0x40	Access : R/W
	-	7	Reserved.	
	VD_AMUX	6	0/1=select ADC RGB/LNADC for VD.	
	VD_RGB_EN	5	1=enable ADC RGB for SCART RGB fast blanking function.	
	VD_YC_EN	4	1=enable S-Video input function.	
	VD_EN	3	1=enable VD function.	
	DVI_EN	2	1=enable DVI function.	
	-	1	Reserved.	
	ADC_ENA	0	1=enable ADC_A RGB function.	
01h (2502h)	REG2502	7:0	Default : 0xCC	Access : R/W
	SYNC_SELB[1:0]	7:6	Select ADC_B SYNC channel. 00: Select input channel 0. 01: Select input channel 1. 10: Select input channel 2.	
	SYNC_SELA[1:0]	5:4	Select ADC_A SYNC channel. 00: Select input channel 0. 01: Select input channel 1. 10: Select input channel 2.	
	AMUXB[1:0]	3:2	Select ADC_B RGB channel, VDA FB mode RGB channel. 00: Select input channel 0 for ADCB. 01: Select input channel 1 for ADCB. 10: Select input channel 2 for ADCB.	
	AMUXA[1:0]	1:0	Select ADC_A RGB channel, VDB FB mode RGB channel. 00: Select input channel 0 for ADCA. 01: Select input channel 1 for ADCA. 10: Select input channel 2 for ADCA.	
02h (2504h)	REG2504	7:0	Default : 0xFF	Access : R/W
	VD_CMUX[3:0]	7:4	Select VD SC channel; 0000=CVBS0; 0001=CVBS1; 0010=CVBS2; 0011=CVBS3; 0100=CVBS4(Y0); 0101=CVBS6(Y1); 0110=CVBS5(C0); 0111=CVBS7(C1); 1000=SOG0; 1001=SOG1; 1010=SOG2; other=none.	
	VD_YMUX[3:0]	3:0	Select VD CVBS/Y channel; 0000=CVBS0; 0001=CVBS1; 0010=CVBS2; 0011=CVBS3; 0100=CVBS4(Y0); 0101=CVBS6(Y1); 0110=CVBS5(C0); 0111=CVBS7(C1); 1000=SOG0; 1001=SOG1; 1010=SOG2; other=none.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
03h (2506h)	REG2506	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	GMC_BYPASS_C	1	1=enable GMC bypass C mode.	
	GMC_BYPASS_Y	0	1=enable GMC bypass Y mode.	
04h (2508h)	REG2508	7:0	Default : 0xFF	Access : R/W
	PDN_ADCREF	7	1=power down ADC voltage reference.	
	PDN_VREF	6	1=power down voltage reference.	
	PDN_ADCR	5	1=power down ADC_R.	
	PDN_ADCG	4	1=power down ADC_G.	
	PDN_ADCB	3	1=power down ADC_B.	
	PDN_PHD	2	1=power down phase digitizer.	
	PDN_PLL	1	1=power down ADC PLL.	
	PDN_DPLBG	0	1=power down DPL bandgap.	
04h (2509h)	REG2509	7:0	Default : 0xFF	Access : R/W
	PDN_ICLP_Y	7	1=power down I-clamp on Y channel.	
	PDN_ICLP_C	6	1=power down I-clamp on C channel.	
	PDN_ADCU	5	1=power down ADC_U.	
	PDN_ADCY	4	1=power down ADC_Y.	
	PDN_ADCC	3	1=power down ADC_C.	
	PDN_PHD2	2	1=power down VD PLL phase digitalizer.	
	PDN_PLL2	1	1=power down VD PLL.	
05h (250Ah)	REG250A	7:0	Default : 0xEF	Access : R/W
	PDN_HSYNC[2:0]	7:5	1=power down HSYNC[2:0] comparator.	
	-	4	Reserved.	
	PDN_GMC_TUNE	3	1=power down GMC tune.	
	PDN_GMC_BIAS	2	1=power down GMC bias circuit.	
	PDN_GMC_Y	1	1=power down GMC on Y channel.	
	PDN_GMC_C	0	1=power down GMC on C channel.	
06h (250Ch)	REG250C	7:0	Default : 0xFF	Access : R/W
	PD_CLK[7:0]	7:0	Clock power down control. [0]: PD_CLKXTAL. [1]: PD_CLK200.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
			[2]: PD_CLKPLLA. [3]: PD_CLKADCA. [4]: PD_CLKPLLB. [5]: PD_CLKADCB. [6]: PD_CLKD_VD. [7]: PD_CLKGMC. [8]: PD_CLK_DVI. [9]: PD_CLK_HDCP. [10]: PD_AUTO_HDCP. [11]: PD_CLK_HDMI. [12]: PD_AUTO_HDMI. [13]: PD_ICLK. [14]: PD_CLK200_FB. [15]: PD_DVIDETCLK.	
06h (250Dh)	REG250D	7:0	Default : 0xFF	Access : R/W
	PD_CLK[15:8]	7:0	See description of '250Ch'.	
07h (250Eh)	REG250E	7:0	Default : 0x00	Access : R/W
	SOFTIRST[7:0]	7:0	1=soft reset for adcdvpll blocks. [15:8]: reserved. [7]: Soft-reset atop control. [6]: Soft-reset hdmi. [5]: Soft-reset hdcp. [4]: Soft-reset dvi. [3]: Soft-reset pll_dig_b. [2]: Soft-reset adc_vd. [1]: Soft-reset pll_dig_a. [0]: Soft-reset adc_dig_a.	
07h (250Fh)	REG250F	7:0	Default : 0x00	Access : R/W
	SOFTIRST[15:8]	7:0	See description of '250Eh'.	
08h (2510h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
08h (2511h)	REG2511	7:0	Default : 0x0D	Access : RO, R/W
	-	7:6	Reserved.	
	MPLL_HV_FLAG	5	Mpll vco high supply voltage flag.	
	MPLL_LOCK	4	Mpll lock status.	
	-	3:0	Reserved.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
09h ~ 0Bh (2512h ~ 2517h)	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
0Ch (2518h)	REG2518	7:0	Default : 0x01	Access : R/W
	ADC_PLL_EXTCK	7	1=select external clock mode for ADC PLL.	
	ADC_PLL_SELBG	6	Select band-gap source for ADC PLL, 0=ADC bandgap, 1=GMC bandgap.	
	ADC_PLL_PDIV[2:0]	5:3	ADC PLL clock post divider. b000: Div1. b001: Div2. b011: Div4. b111: Div8. others: Reserved.	
	ADC_PLL_MULT[2:0]	2:0	ADC PLL clock multiplier = N+1.	
0Dh ~ 11h (251Ah ~ 2522h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
11h (2523h)	REG2523	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	ADC_PLL_STATUS[4:0]	4:0	Adc pll detector status. [4]: DPL_HV_FLAG. [3]: DPL_LOCK. [2]: DPL_FLAG. [1]: DPL_DUTYH. [0]: DPL_DUTYL.	
12h (2524h)	REG2524	7:0	Default : 0x01	Access : R/W
	VD_PLL_EXTCK	7	1=select external clock mode for VD(ADCB) PLL.	
	VD_PLL_SELBG	6	Select band-gap source for VD(ADCB) PLL, 0=GMC bandgap, 1=ADC bandgap.	
	VD_PLL_PDIV[2:0]	5:3	VD(ADCB) PLL clock post divider. b000: Div1. b001: Div2. b011: Div4. b111: Div8. others: Reserved.	
	VD_PLL_MULT[2:0]	2:0	VD(ADCB) PLL clock multiplier = N+1.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
13h ~ 17h (2526h ~ 252Eh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
17h (252Fh)	REG252F	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	VD_PLL_STATUS[4:0]	4:0	VD(ADCB) pll detector status. [4]: DPL_HV_FLAG. [3]: DPL_LOCK. [2]: DPL_FLAG. [1]: DPL_DUTYH. [0]: DPL_DUTYL.	
19h (2532h)	REG2532	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ADC_ENC[5:0]	5:0	Enable ADC offset cancel mode for VD; [5]=U; [4]=Y; [3]=C; [2]=B; [1]=G; [0]=R.	
19h (2533h)	REG2533	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ADC_GSHIFT[5:0]	5:0	Override enable ADC gain shift; [5]=U; [4]=Y; [3]=C; [2]=B; [1]=G; [0]=R.	
1Ah (2534h)	REG2534	7:0	Default : 0x1C	Access : R/W
	-	7:6	Reserved.	
	ADC_VCTRL_RGB[2:0]	5:3	ADC voltage control for ADC_RGB.	
	ADC_IBIAS_RGB[2:0]	2:0	Select ADC main bias current for ADC_RGB.	
1Bh (2536h)	REG2536	7:0	Default : 0x55	Access : R/W
	ADC_ICTRL_RGB[7:0]	7:0	ADC RGB bias current control. [13:12]: ADC reference buffer bias current control. [11:10]: ADC input buffer current control. [9:8]: ADC PGA bias current control. [7:6]: ADC 1st stage bias current control. [5:4]: ADC 2nd stage bias current control. [3:2]: ADC 3rd stage bias current control. [1:0]: ADC 4th stage bias current control.	
1Bh (2537h)	REG2537	7:0	Default : 0x15	Access : R/W
	-	7:6	Reserved.	
	ADC_ICTRL_RGB[13:8]	5:0	See description of '2536h'.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
1Ch (2538h)	REG2538	7:0	Default : 0x08	Access : R/W
	-	7:6	Reserved.	
	SOG_DISA	5	1=disable active SOG comparator.	
	SOG_THA[4:0]	4:0	Select SOG comparator threshold, step=10mv.	
1Ch (2539h)	REG2539	7:0	Default : 0x00	Access : R/W
	ADCBWA[3:0]	7:4	Select ADC input filter bandwidth. 0000: 260MHz. 0001: 190MHz. 0010: 150MHz. 0011: 120MHz. 0100: 60MHz. 0101: 30MHz. 0110: 25MHz. 0111: 23MHz. 1000: 21MHz. 1001: 20MHz. 1010: 18MHz. 1011: 17MHz. 1100: 16MHz. 1101: 15MHz. 1110: 14MHz. 1111: 6MHz.	
	SOG_OPTFIRA	3	0/1=disable/enable SOG input low bandwidth filter.	
	SOG_BWA[2:0]	2:0	Select SOG input filter bandwidth.	
1Fh (253Eh)	REG253E	7:0	Default : 0x08	Access : R/W
	-	7:5	Reserved.	
	SOG_THB[4:0]	4:0	Select SOG comparator threshold, step=10mv.	
1Fh (253Fh)	REG253F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SOG_OPTFIRB	3	0/1=disable/enable SOG input low bandwidth filter.	
	SOG_BWB[2:0]	2:0	Select SOG input filter bandwidth.	
20h (2540h)	REG2540	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TEST_HSYNC[2:0]	5:3	1=enable HSYNC analog test input.	
	HSYNC_LVL[2:0]	2:0	Select HSYNC trigger level.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
20h (2541h)	REG2541	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	TEST_SOG[2:0]	5:3	1=enable SOG analog test input.	
	TEST_VSYNC[2:0]	2:0	1=enable VSYNC analog test input.	
21h ~ 22h (2542h ~ 2545h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
23h (2546h)	REG2546	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CKEXT_SEL	6	0/1=select VSYNC0/VSYNC1 as pll external clock input.	
	-	5:3	Reserved.	
	VDD2LO_EN	2	1=enable vdd too low reset.	
	-	1:0	Reserved.	
23h (2547h)	REG2547	7:0	Default : 0x30	Access : R/W
	XTAL_FREQ[7:0]	7:0	Set XTAL frequency for timing detection normalization (default=12MHz, format=6.2 MHz).	
24h (2548h)	REG2548	7:0	Default : 0x00	Access : R/W
	REFDAC0[7:0]	7:0	ADC reference DAC0 output level override value.	
24h (2549h)	REG2549	7:0	Default : 0x0C	Access : R/W
	-	7:5	Reserved.	
	REFDAC0_OV	4	1=override ADC reference DAC0 output.	
	REFDAC0[11:8]	3:0	See description of '2548h'.	
25h (254Ah)	REG254A	7:0	Default : 0x00	Access : R/W
	REFDAC1[7:0]	7:0	ADC reference DAC1 output level override value.	
25h (254Bh)	REG254B	7:0	Default : 0x0C	Access : R/W
	-	7:5	Reserved.	
	REFDAC1_OV	4	1=override ADC reference DAC1 output.	
	REFDAC1[11:8]	3:0	See description of '254Ah'.	
26h (254Ch)	REG254C	7:0	Default : 0x40	Access : R/W
	-	7	Reserved.	
	REF_SEL_VD	6	Select ADC reference DAC for VD function (prefer DAC1 assigned to VD).	
	-	5:4	Reserved.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
	REF_SEL[3:0]	3:0	Select ADC reference DAC for ADC {Overwrite, B;G;R}; 0=DAC0; 1=DAC1.	
26h (254Dh)	REG254D	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	RDAC_ICTRL[1:0]	1:0	Select reference DAC bias current.	
27h (254Eh)	REG254E	7:0	Default : 0x00	Access : R/W
	REFDAC2[7:0]	7:0	ADC reference DAC1 output level override value.	
27h (254Fh)	REG254F	7:0	Default : 0x0C	Access : R/W
	-	7:5	Reserved.	
	REFDAC2_OV	4	1=override LNADC reference DAC output.	
	REFDAC2[11:8]	3:0	See description of '254Eh'.	
28h (2550h)	REG2550	7:0	Default : 0x80	Access : R/W
	VD_CGAIN[7:0]	7:0	VD ADC C channel gain control (override).	
28h (2551h)	REG2551	7:0	Default : 0x70	Access : R/W
	VD_COFFSET[7:0]	7:0	VD ADC C channel offset control.	
29h (2552h)	REG2552	7:0	Default : 0x80	Access : R/W
	VD_YGAIN[7:0]	7:0	VD ADC Y channel gain control (override).	
29h (2553h)	REG2553	7:0	Default : 0x70	Access : R/W
	VD_YOFFSET[7:0]	7:0	VD ADC Y channel offset control.	
2Ah (2554h)	REG2554	7:0	Default : 0x00	Access : RO, R/W, WO
	VD_YGAIN_OV	7	1=override VD ADC_Y gain control.	
	VD_CGAIN_OV	6	1=override VD ADC_C gain control.	
	-	5	Reserved.	
	CLROVF_YC	4	Write an 1 to clear ADC_YC overflow flags.	
	OVF_YC[3:0]	3:0	ADC overflow flags, {OVFY, UNFY, OVFC, UNFC}.	
2Bh ~ 2Bh (2556h ~ 2557h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
2Ch (2558h)	REG2558	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	VMID_SELA	6	Select vmid mode. 0=controlled by ADCB gain, 1=constant voltage.	
	BSEL_CVA[1:0]	5:4	Select vclamp voltage for ADC B input.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
			00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
	GSEL_CVA[1:0]	3:2	Select vclamp voltage for ADC G input. 00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
	RSEL_CVA[1:0]	1:0	Select vclamp voltage for ADC R input. 00=clamp to gnd, 01=clamp to VP3, 1x=clamp to Vmid.	
2Ch (2559h)	REG2559	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	VMID_SELB	6	Select vmid mode. 0=controlled by ADCU gain, 1=constant voltage.	
	-	5:0	Reserved.	
2Dh (255Ah)	REG255A	7:0	Default : 0x90	Access : R/W
	VMID_VP4	7	1=select new vmid vp4 mode.	
	-	6:5	Reserved.	
	ADC_INMSEL	4	0/1=select ADC INM pins, differential/shared mode.	
	SVCLP[3:0]	3:0	Select GMC VCLAMP voltage level; 0000=1.15V; 0001=1.2V; 0010=0.85V; 0011=0.90V; 0100=0.95V; 0101=1.00V; 0110=1.05V; 0111=1.10V; 1000=0.3V; 1001=0.4V; 1010=0.5V; 1011=0.6V; 1100=0.7V; 1101=0.8V; 111x=0.6V.	
2Dh (255Bh)	REG255B	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	FB_RGBCLP	6	0/1=select RGB clamp pulse from VD/ADC for FB mode.	
	CLAMP_YC_OV[1:0]	5:4	Override clamp control for YC, 0x=pulse; 10=disable; 11=force clamp.	
	-	3:2	Reserved.	
	CLAMP_RGB_OV[1:0]	1:0	Override clamp control for RGB, 0x=pulse; 10=disable; 11=force clamp.	
2Eh (255Ch)	REG255C	7:0	Default : 0x00	Access : R/W
	ICLP_M1[1:0]	7:6	Select I-clamp current range for Y channel.	
	ICLP_M0[1:0]	5:4	Select I-clamp current range for C channel.	
	SEL_ICLAMP[3:0]	3:0	Select I-clamp bias current.	
30h (2560h)	REG2560	7:0	Default : 0x01	Access : R/W
	GMC_UPD_SEL	7	Select GMC update during 0=VSYNC; 1=HSYNC.	
	GMC_STS_SEL	6	Select GMC status; 0=GMC control code; 1=GMC tuning	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
			code.	
	GMC_HOLD	5	1=hold current GMC control.	
	GMC_UPDA	4	1=always update GMC control.	
	GMC_HYS_TH[3:0]	3:0	Select GMC update hysteresis threshold.	
30h (2561h)	REG2561	7:0	Default : 0x08	Access : R/W
	GMC_ACC_TH[7:0]	7:0	Select accumulator threshold for GMC control update.	
31h (2562h)	REG2562	7:0	Default : 0x00	Access : RO
	GMC_STATUS[7:0]	7:0	GMC tuning status. [8]: Comparator output. [7:0]: GMC control/tuning code.	
31h (2563h)	REG2563	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	GMC_STATUS[8]	0	See description of '2562h'.	
32h ~ 33h (2564h ~ 2567h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
34h (2568h)	REG2568	7:0	Default : 0x1F	Access : R/W
	-	7:6	Reserved.	
	GMC_CKDIV[5:0]	5:0	Select divider down ratio for GMC clock, clock div=2N+2.	
34h (2569h)	REG2569	7:0	Default : 0x40	Access : R/W
	-	7	Reserved.	
	AGC_GMC_1ST	6	1=use GMC gain 2X first when tuning AGC.	
	GMC_YGAIN_OV[2:0]	5:3	1=override GMC gain on Y channel. 0xx: Auto; 100=1X; 101=2X; 11x=4X.	
	GMC_CGAIN_OV[2:0]	2:0	1=override GMC gain on C channel. 0xx: Auto; 100=1X; 101=2X; 11x=4X.	
35h ~ 37h (256Ah ~ 256Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
38h (2570h)	REG2570	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	CVBSO_MUXEN[2:0]	6:4	CVBS buffer input channel enable. [6]: 1=CP channel enable. [5]: 1=YN channel enable.	

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description
			[4]: 1=YP channel enable.
	PDN_CVBSO_CPOS	3	1=CP channel clamp power down.
	PDN_CVBSO_YPOS	2	1=YP channel clamp power down.
	PDN_CVBSO_LSH	1	1=power down CVBS output buffer level shift.
	PDN_CVBSO	0	1=power down CVBS output buffer.
39h (2572h)	REG2572	7:0	Default : 0x00 Access : R/W
	CVBSO_YNMUX[3:0]	7:4	Select YN channel input. 0000=VCOM0; 0001=VCOM1; 0010=VCOM1; 0011=VCOM1; 0100=VCOM2; 0101=VCOM2; 0110=VCOM2; 0111=VCOM2; 1000=VCOM2; 1001=VCOM2; 1010=VCOM2; 1011=CVBS_DACM.
	CVBSO_YPMUX[3:0]	3:0	Select YP channel input. 0000=CVBS0; 0001=CVBS1; 0010=CVBS2; 0011=CVBS3; 0100=CVBS4(Y0); 0101=CVBS5(C0); 0110=CVBS6(Y1); 0111=CVBS7(C1); 1000=SOG0; 1001=SOG1; 1010=SOG2; 1011=CVBS DAC.
39h (2573h)	REG2573	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	CVBSO_CPMUX[3:0]	3:0	Select CP channel input. 0000=CVBS0; 0001=CVBS1; 0010=CVBS2; 0011=CVBS3; 0100=CVBS4(Y0); 0101=CVBS5(C0); 0110=CVBS6(Y1); 0111=CVBS7(C1); 1000=SOG0; 1001=SOG1; 1010=SOG2; 1011=CVBS DAC.
3Ah (2574h)	REG2574	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	CVBSO_ISINK[2:0]	5:3	Select CVBSO clamp sink current.
	CVBSO_HISOURCE	2	1=enable CVBSO clamp high sourcing current.
	CVBSO_CBW[1:0]	1:0	C channel clamp bandwidth.
3Bh ~ 3Bh (2576h ~ 2577h)	-	7:0	Default : - Access : -
	-	-	Reserved.
3Ch (2578h)	REG2578	7:0	Default : 0x0F Access : R/W
	-	7	Reserved.
	CVBSO2_MUXEN[2:0]	6:4	CVBS buffer input channel enable. [6]: 1=CP channel enable.

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description
			[5]: 1=YN channel enable. [4]: 1=YP channel enable.
	PDN_CVBSO2_CPOS	3	1=CP channel clamp power down.
	PDN_CVBSO2_YPOS	2	1=YP channel clamp power down.
	PDN_CVBSO2_LSH	1	1=power down CVBS output buffer level shift.
	PDN_CVBSO2	0	1=power down CVBS output buffer.
3Dh (257Ah)	REG257A	7:0	Default : 0x00 Access : R/W
	CVBSO2_YNMUX[3:0]	7:4	Select YN channel input. 0000=VCOM0; 0001=VCOM1; 0010=VCOM1; 0011=VCOM1; 0100=VCOM2; 0101=VCOM2; 0110=VCOM2; 0111=VCOM2; 1000=VCOM2; 1001=VCOM2; 1010=VCOM2; 1011=CVBS_DACM.
	CVBSO2_YPMUX[3:0]	3:0	Select YP channel input. 0000=CVBS0; 0001=CVBS1; 0010=CVBS2; 0011=CVBS3; 0100=CVBS4(Y0); 0101=CVBS5(C0); 0110=CVBS6(Y1); 0111=CVBS7(C1); 1000=SOG0; 1001=SOG1; 1010=SOG2; 1011=CVBS DAC.
3Dh (257Bh)	REG257B	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	CVBSO2_CPMUX[3:0]	3:0	Select CP channel input. 0000=CVBS0; 0001=CVBS1; 0010=CVBS2; 0011=CVBS3; 0100=CVBS4(Y0); 0101=CVBS5(C0); 0110=CVBS6(Y1); 0111=CVBS7(C1); 1000=SOG0; 1001=SOG1; 1010=SOG2; 1011=CVBS DAC.
3Eh (257Ch)	REG257C	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	CVBSO2_ISINK[2:0]	5:3	Select CVBSO clamp sink current.
	CVBSO2_HISOURCE	2	1=enable CVBSO clamp high sourcing current.
	CVBSO2_CBW[1:0]	1:0	C channel clamp bandwidth.
3Fh ~ 3Fh (257Eh ~ 257Fh)	-	7:0	Default : - Access : -
	-	-	Reserved.
40h (2580h)	REG2580	7:0	Default : 0x40 Access : R/W
	FBLANK_CKINV	7	1=invert fast blanking ADC sampling clock.
	PDN_FBLANK	6	1=power down fast blanking ADC.

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description
	FBLANK_SEL[1:0]	5:4	Select fast blanking input 00=none; 01=FB input 0; 10=FB input 1; 11=FB input 2.
	FBLANK_GX[3:0]	3:0	Select fast blanking ADC gain.
41h ~ 41h (2582h ~ 2583h)	-	7:0	Default : - Access : -
	-	-	Reserved.
42h (2584h)	REG2584	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	FB_CSC_EN	5	1=enable RGB input color space conversion before fast flanking.
	FB_SRST	4	1=software reset fast blanking down sample block.
	CSDOWN_168	3	1=enable down sampling RGB input from 16 fsc to 8 fsc.
	CSDOWN_84	2	1=enable down sampling RGB input from 8 fsc to 4 fsc.
	FB_DTHR[1:0]	1:0	1=enable dither for down sampling. [1]: Dither for 16-to-8 down sample. [0]: Dither for 8-to-4 down sample.
43h (2586h)	REG2586	7:0	Default : 0x00 Access : R/W
	FB_FINE_DLY[1:0]	7:6	Select FB input fine delay.
	-	5:0	Reserved.
43h (2587h)	REG2587	7:0	Default : 0x00 Access : R/W
	RGB_FINE_DLY[1:0]	7:6	Select RGB input fine delay.
	RGB_PG_DLY[5:0]	5:0	Select RGB input pipe delay.
44h (2588h)	REG2588	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	FB_DOFFS[5:0]	5:0	Fast blanking input digital offset adjust (0.6).
44h (2589h)	REG2589	7:0	Default : 0x44 Access : R/W
	FB_DGAIN[7:0]	7:0	Fast blanking input digital gain adjust (2.6).
45h (258Ah)	REG258A	7:0	Default : 0x20 Access : R/W
	-	7:6	Reserved.
	FB_BILTH[5:0]	5:0	Select fast blanking active threshold for bi-level mode.
45h (258Bh)	REG258B	7:0	Default : 0x00 Access : RO, WO
	-	7:6	Reserved.
	FB_ACT_CLR	5	Write an 1 to clear FB_ACT flag.

ATOP Register (Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description
	FB_ACT_FLAG	4	Fast blanking input active status (sticky flag).
	FBLANK_DOUT[3:0]	3:0	Fast blank input value status.
46h (258Ch)	REG258C	7:0	Default : 0x00 Access : R/W
	CVBS_DAC_EN	7	1=enable CVBS DAC.
	CVBS_DAC_SEL	6	Select CVBS DAC input sources. 0: From video encoder. 1: From VIF decoder.
	CVBS_DAC_CLK_INV	5	CVBS DAC clock invert enable. 0: Disable clock invert. 1: Enable clock invert.
	-	4:0	Reserved.
46h (258Dh)	REG258D	7:0	Default : 0x00 Access : R/W
	CVBS_DAC_GAIN[3:0]	7:4	CVBS DAC gain control.
	CVBS_DAC_OFFSET[3:0]	3:0	CVBS DAC offset control.
47h (258Eh)	REG258E	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	ADCBW_RB_OREN	0	ADC RB input filter bandwidth overwrite enable. 0: ADC RB input filter bandwidth controlled by reg_adcbwa. 1: ADC RB input filter bandwidth controlled by reg_adcbw_rb_ov.
47h (258Fh)	REG258F	7:0	Default : 0x00 Access : R/W
	ADCBW_B_OV[3:0]	7:4	ADC B input filter bandwidth overwrite.
	ADCBW_R_OV[3:0]	3:0	ADC R input filter bandwidth overwrite.
48h (2590h)	REG2590	7:0	Default : 0x03 Access : R/W
	-	7:2	Reserved.
	PDN_MODULE	1	1: Power down 2nd reference module.
	PDN_VCLP	0	1: Power down vclp reference voltage.
48h ~ 49h (2591h ~ 2593h)	-	7:0	Default : - Access : -
	-	-	Reserved.
4Ch (2598h)	REG2598	7:0	Default : 0x00 Access : RO, R/W, WO
	SAR2_DONE	7	1=SAR one-shot mode done status.
	SAR2_TRIG	6	Write an 1 to restart SAR conversion.
	SAR2_EN	5	0/1=power-down/enable SAR ADC.

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
	SAR2_FREERUN	4	Select SAR ADC operation mode; 0=one-shot; 1=freerun mode.	
	SAR2_CH_EN[3:0]	3:0	Channel enable bit for SAR[3:0] inputs.	
4Ch (2599h)	REG2599	7:0	Default : 0x04	Access : R/W
	SAR2_PERIOD[7:0]	7:0	SAR ADC input sampling pulse duration.	
4Dh (259Ah)	REG259A	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	SAR2_DATA0[5:0]	5:0	SAR ADC channel 0 data.	
4Dh (259Bh)	REG259B	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	SAR2_DATA1[5:0]	5:0	SAR ADC channel 1 data.	
4Eh (259Ch)	REG259C	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	SAR2_DATA2[5:0]	5:0	SAR ADC channel 2 data.	
4Eh (259Dh)	REG259D	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	SAR2_DATA3[5:0]	5:0	SAR ADC channel 3 data.	
4Fh ~ 4Fh (259Eh ~ 259Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
50h (25A0h)	REG25A0	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ID_THL[5:0]	5:0	Select SCART function select switch (FSSW) low threshold.	
50h (25A1h)	REG25A1	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ID_THH[5:0]	5:0	Select SCART function select switch (FSSW) high threshold.	
51h (25A2h)	REG25A2	7:0	Default : 0x00	Access : R/W
	ID1_EN	7	1=enable ID1 change detect.	
	ID1_SEL[2:0]	6:4	0~3: reserved. 4~7: select SAR2[0:3] as ID1 source.	
	ID0_EN	3	1=enable ID0 change detect.	
	ID0_SEL[2:0]	2:0	0~3: reserved. 4~7: select SAR2[0:3] as ID0 source.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
51h (25A3h)	REG25A3	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	SCART_ID1[1:0]	3:2	SCART ID1 level status.	
	SCART_ID0[1:0]	1:0	SCART ID0 level status.	
54h (25A8h)	REG25A8	7:0	Default : 0xC8	Access : R/W
	ATTEN_CLPENR	7	1=force a clamp duration when attenuator on.	
	ATTEN_CLPENF	6	1=force a clamp duration when attenuator off.	
	ATTEN_CLPDUR[5:0]	5:0	Select clamp duration when switch from/to attenuator, N*1024 CLKFSC.	
54h (25A9h)	REG25A9	7:0	Default : 0x40	Access : R/W
	ATTEN_SWDLY[1:0]	7:6	Select enable attenuator to switch mux delay, N*64 CLKFSC.	
	ATTEN_OV[5:0]	5:0	Override CVBS input attenuator. [5]: Override attenuator Y enable. [4]: Enable attenuator Y input mux. [3]: Enable attenuator Y. [2]: Override attenuator C enable. [1]: Enable attenuator C input mux. [0]: Enable attenuator C.	
55h (25AAh)	REG25AA	7:0	Default : 0x08	Access : RO, R/W
	-	7	Reserved.	
	AGC_COARSE[2:0]	6:4	VD coarse gain status.	
	ATTEN_SVCLP[3:0]	3:0	Select clamp level when attenuator enable.	
56h ~ 56h (25ACh ~ 25ADh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
58h (25B0h)	REG25B0	7:0	Default : 0x00	Access : R/W
	CLK_EXTMD	7	1=enable external clock (function) test mode.	
	-	6:0	Reserved.	
58h ~ 59h (25B1h ~ 25B3h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
5Ah (25B4h)	REG25B4	7:0	Default : 0x00	Access : R/W
	RAMP_EN	7	1=enable ramp counter.	
	RAMP_VREF2	6	1=enable ramp counter to LNADC VREF.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
	RAMP_VREF1	5	1=enable ramp counter to VREF_DAC1.	
	RAMP_VREF0	4	1=enable ramp counter to VREF_DAC0.	
	RAMP_DIV[3:0]	3:0	Select ramp speed divider; $2^N - 1$.	
5Bh ~ 5Fh (25B6h ~ 25BEh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
60h (25C0h)	REG25C0	7:0	Default : 0xFF	Access : R/W
	PDN_DVIPLL	7	1=power down DVI PLL.	
	PDN_DVIPLLBG	6	1=power down DVI PLL band-gap.	
	PDN_DVIPLLREG	5	1=power down DVI PLL regulator.	
	PDN_DMIBEX	4	1=power down DVI output bias current.	
	PDN_DVICK	3	1=power down DVI clock receiver.	
	PDN_DM[2:0]	2:0	1=power down DVI de-multiplexer.	
60h (25C1h)	REG25C1	7:0	Default : 0x7F	Access : R/W
	-	7:3	Reserved.	
	PDN_DPLMXR[2:0]	2:0	1=power down DPL mixer [2:0].	
61h (25C2h)	REG25C2	7:0	Default : 0x35	Access : R/W
	-	7	Reserved.	
	BBEN	6	1=BBEN mode.	
	DM_MODE_OV[1:0]	5:4	Override DM operation mode. 0x=auto. 10=high speed option mode. 11=normal mode.	
	SWCKB	3	1=enable clkb input switch.	
	SWCKA	2	1=enable clka input switch.	
	SWB	1	1=enable data_b input switch.	
	SWA	0	1=enable data_a input switch.	
61h (25C3h)	REG25C3	7:0	Default : 0x10	Access : R/W
	HR_SEL[2:0]	7:5	Select dvi pull-up resistor.	
	DVI_RCTRL[4:0]	4:0	Dvi termination resistor control.	
62h ~ 67h (25C4h ~ 25CEh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
68h	REG25D0	7:0	Default : 0xC0	Access : RO, R/W

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
(25D0h)	-	7:4	Reserved.	
	DVI_DPL_STATUS[3:0]	3:0	DVI DPL detector status. [3]: DVIPLL_LOCK. [2]: DVIPLL_FLAG. [1]: DVIPLL_DUTYH. [0]: DVIPLL_DUTYL.	
68h (25D1h)	REG25D1	7:0	Default : 0x0C	Access : R/W
	-	7:4	Reserved.	
	GPIO_OEN[1:0]	3:2	0= GPIO[1:0] output enable.	
	GPIO[1:0]	1:0	Write GPIO[1:0] output value. Read GPIO[1:0] input value.	
70h (25E0h)	REG25E0	7:0	Default : 0x00	Access : RO
	ADCDVI_IRQ_STATUS[7:0]	7:0	Adcdvi irq status. {0, SCART_ID1_CHG, SCART_ID0_CHG, HDMI_MODE_CHG, DVI_CK_CHG}.	
70h (25E1h)	REG25E1	7:0	Default : 0x00	Access : R/W
	ADCDVI_IRQ_MASK[7:0]	7:0	Adcdvi irq mask control.	
71h (25E2h)	REG25E2	7:0	Default : 0x00	Access : R/W
	ADCDVI_IRQ_FORCE[7:0]	7:0	Adcdvi irq force control.	
71h (25E3h)	REG25E3	7:0	Default : 0x00	Access : R/W
	ADCDVI_IRQ_CLR[7:0]	7:0	Adcdvi irq clear control.	
72h (25E4h)	REG25E4	7:0	Default : 0x08	Access : R/W
	GAIN_AGC0[7:0]	7:0	Select ADC gain control for VD AGC_COARSE=0.	
72h (25E5h)	REG25E5	7:0	Default : 0x10	Access : R/W
	GAIN_AGC1[7:0]	7:0	Select ADC gain control for VD AGC_COARSE=1.	
73h (25E6h)	REG25E6	7:0	Default : 0x10	Access : R/W
	GAIN_AGC2[7:0]	7:0	Select ADC gain control for VD AGC_COARSE=2.	
73h (25E7h)	REG25E7	7:0	Default : 0xE0	Access : R/W
	GAIN_AGC3[7:0]	7:0	Select ADC gain control for VD AGC_COARSE=3.	
74h (25E8h)	REG25E8	7:0	Default : 0xC1	Access : R/W
	GMC_AGC[3:0]	7:4	Select GMC gain control for VD AGC_COARSE.	
	GSHIFT_AGC[3:0]	3:0	Select ADC gain shift control for VD AGC_COARSE.	
74h (25E9h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	

ATOP Register (Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
75h (25EAh)	REG25EA	7:0	Default : 0x51	Access : R/W
	CVBS_GAIN_AGC1[3:0]	7:4	Select LNADC gain control for VD AGC_COARSE=1.	
	CVBS_GAIN_AGC0[3:0]	3:0	Select LNADC gain control for VD AGC_COARSE=0.	
75h (25EBh)	REG25EB	7:0	Default : 0xF5	Access : R/W
	CVBS_GAIN_AGC3[3:0]	7:4	Select LNADC gain control for VD AGC_COARSE=3.	
	CVBS_GAIN_AGC2[3:0]	3:0	Select LNADC gain control for VD AGC_COARSE=2.	
76h ~ 79h (25ECh ~ 25F3h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
7Ah (25F4h)	REG25F4	7:0	Default : 0x00	Access : R/W
	HSYNC_DEGLITCH_TH[7:0]	7:0	Select HSYNC deglitch pulse width threshold (step size = MPLL clock).	
7Ah (25F5h)	REG25F5	7:0	Default : 0x00	Access : R/W
	SOG_DEGLITCH_TH[7:0]	7:0	Select SOG deglitch pulse width threshold (step size = MPLL clock).	
7Bh (25F6h)	REG25F6	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	IP_SOG_DEGLITCH	5	1: Enable SOG input deglitch for IP mode detection.	
	IP_HSYNC_DEGLITCH	4	1: Enable HSYNC input deglitch for IP mode detection.	
	PLL_SOG_DEGLITCH	3	1: Enable SOG input deglitch for PLL.	
	PLL_HSYNC_DEGLITCH	2	1: Enable HSYNC input deglitch for PLL.	
	ADC_SOG_DEGLITCH	1	1: Enable SOG input deglitch for ADC clamp.	
	ADC_HSYNC_DEGLITCH	0	1: Enable HSYNC input deglitch for ADC clamp.	
7Ch ~ 7Eh (25F8h ~ 25FCh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
7Eh (25FDh)	REG25FD	7:0	Default : 0x00	
	BT656_PLL_STATUS[1:0]	7:6	Bt656 output pll status.	
	-	5:0	Reserved.	

ADC Register (Bank = 26)

ADC Register (Bank = 26)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2600h)	REG2600	7:0	Default : 0x95	Access : R/W
	PLLDIV[7:0]	7:0	ADC PLL divider ratio (htotal-3), (write sequence LSB -> MSB).	
00h (2601h)	REG2601	7:0	Default : 0x06	Access : R/W
	-	7:5	Reserved.	
	PLLDIV[12:8]	4:0	See description of '2600h'.	
01h (2602h)	REG2602	7:0	Default : 0x82	Access : R/W
	BWCOEF[7:0]	7:0	ADC PLL bandwidth coefficient.	
01h (2603h)	REG2603	7:0	Default : 0x09	Access : R/W
	FREQCOEF[7:0]	7:0	ADC PLL frequency coefficient.	
02h (2604h)	REG2604	7:0	Default : 0x05	Access : R/W
	DAMPCOEF[7:0]	7:0	ADC PLL damping coefficient.	
03h (2606h)	REG2606	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PHASE_CC[5:0]	5:0	Select ADC sampling clock phase.	
03h (2607h)	REG2607	7:0	Default : 0x08	Access : R/W
	-	7:6	Reserved.	
	PHASE_DELTA[5:0]	5:0	Select ADC phase delta between clkcc & clkadc.	
04h (2608h)	REG2608	7:0	Default : 0x05	Access : R/W
	PLL_STATUS_SEL[2:0]	7:5	Select pll digital status.	
	PHD_CAL_DIS	4	Disable phase digitalizer calibration.	
	SETTLE_CNT[3:0]	3:0	Select phase digitalizer settling time.	
04h (2609h)	REG2609	7:0	Default : 0xC6	Access : R/W
	WDOG_TOL[1:0]	7:6	Select PLL watch dog reset tolerance.	
	IQCLR_TH[2:0]	5:3	PII lock to unlock threshold.	
	IQSET_TH[2:0]	2:0	PII unlock to lock threshold.	
05h (260Ah)	REG260A	7:0	Default : 0x00	Access : RO
	PLL_STATUS[7:0]	7:0	PII digital status. 000: {LOCK, IQ, SLOW, FAST, FREERUN, 000}.	
06h (260Ch)	REG260C	7:0	Default : 0x00	Access : R/W
	PLL_TESTD[7:0]	7:0	PII digital test registers.	
06h	REG260D	7:0	Default : 0x00	Access : R/W

ADC Register (Bank = 26)				
Index (Absolute)	Mnemonic	Bit	Description	
(260Dh)	PLL_TESTD[15:8]	7:0	See description of '260Ch'.	
07h (260Eh)	REG260E	7:0	Default : 0x8A	Access : R/W
	HSYNC_POL	7	Input HSYNC polarity. 0: Low active. 1: High active.	
	SOG_EN	6	Select pll locking source. 0: HSYNC. 1: SOG.	
	HSYNC_EDGE	5	Select pll locking edge. 0: HSYNC leading edge. 1: HSYNC trailing edge.	
	CLAMP_EDGE	4	Select clamp reference edge. 0: HSYNC trailing edge. 1: HSYNC leading edge.	
	CCDIS	3	1=disable clamp during coast region.	
	WDOG_DIS	2	1=disable ADC PLL watch dog.	
	COAST_POL	1	Select coast polarity. 0: Low active. 1: High active.	
	-	0	Reserved.	
07h (260Fh)	REG260F	7:0	Default : 0x00	Access : R/W
	HSOUT_PW[7:0]	7:0	Select extended HSOUT pulse width.	
08h (2610h)	REG2610	7:0	Default : 0x80	Access : R/W
	GAIN_R[7:0]	7:0	ADC R channel gain control.	
08h (2611h)	REG2611	7:0	Default : 0x80	Access : R/W
	OFFSET_R[7:0]	7:0	ADC R channel offset control.	
09h (2612h)	REG2612	7:0	Default : 0x80	Access : R/W
	GAIN_G[7:0]	7:0	ADC G channel gain control.	
09h (2613h)	REG2613	7:0	Default : 0x80	Access : R/W
	OFFSET_G[7:0]	7:0	ADC G channel offset control.	
0Ah (2614h)	REG2614	7:0	Default : 0x80	Access : R/W
	GAIN_B[7:0]	7:0	ADC B channel gain control.	
0Ah (2615h)	REG2615	7:0	Default : 0x80	Access : R/W
	OFFSET_B[7:0]	7:0	ADC B channel offset control.	

ADC Register (Bank = 26)				
Index (Absolute)	Mnemonic	Bit	Description	
0Bh (2616h)	REG2616	7:0	Default : 0x05	Access : R/W
	CLAMP_DLY[7:0]	7:0	Select clamp pulse start position relative to input HSYNC edge.	
0Bh (2617h)	REG2617	7:0	Default : 0x05	Access : R/W
	CLAMP_DUR[7:0]	7:0	Select clamp pulse duration.	
0Ch (2618h)	REG2618	7:0	Default : 0x24	Access : R/W
	HSOUT_GEN	7	1=enable HSOUT pulse extension.	
	CLAMP_VEN	6	1=enable clamp once per vsync mode.	
	RGB_SWAP[5:0]	5:0	Select rgb data to scalar, [1:0]=SEL R, [3:2]=SEL G, [5:4]=SEL B, 00=R, 01=G, 10=B, 11=blank.	
0Ch (2619h)	REG2619	7:0	Default : 0x00	Access : R/W
	CLAMP_VDLY[7:0]	7:0	Clamp pulse line delay from vsync.	
0Dh (261Ah)	REG261A	7:0	Default : 0x00	Access : R/W
	MASK_DUR[7:0]	7:0	Select blank ADC data duration after HSYNC.	
0Dh (261Bh)	REG261B	7:0	Default : 0x7A	Access : R/W
	-	7	Reserved.	
	MASK_EN[3:0]	6:3	Enable blank ADC for CAL.	
	MASK_COAST	2	1=blank ADC data during COAST.	
	MASK_CDIS	1	1=disable H blank ADC data during COAST.	
	MASK_EDGE	0	0/1=select blank ADC data from HSYNC leading/trailing edge.	
0Eh (261Ch)	REG261C	7:0	Default : 0x40	Access : R/W
	TIMEOUT_H[7:0]	7:0	HSYNC activity timeout period (100us).	
0Eh (261Dh)	REG261D	7:0	Default : 0x64	Access : R/W
	TIMEOUT_V[7:0]	7:0	VSYNC activity timeout period (ms).	
0Fh (261Eh)	REG261E	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	SOG_TOG	2	1=active channel sog toggle status.	
	VSYNC_TOG	1	1=active channel vsync toggle status.	
	HSYNC_TOG	0	1=active channel hsync toggle status.	
10h (2620h)	REG2620	7:0	Default : 0x00	Access : R/W, WO
	CALG_TRIG	7	Write an 1 to start gain CAL procedure.	
	CALO_TRIG	6	Write an 1 to start offset CAL procedure.	

ADC Register (Bank = 26)				
Index (Absolute)	Mnemonic	Bit	Description	
	CALG_EN	5	1=enable gain auto CAL procedure.	
	CALO_EN	4	1=enable offset auto CAL procedure.	
	CALO_MODE[1:0]	3:2	Select offset CAL procedure, 0x(normal), 10(live only), 11(normal=>live).	
	CALO_INPUT[1:0]	1:0	Select offset CAL reference, 0=CAL to internal vref, 1=CAL to input. [0]: Select for normal procedure. [1]: Select for live procedure.	
10h (2621h)	REG2621	7:0	Default : 0x04	Access : R/W
	CALO_BLK	7	Select offset CAL target DOUT code. 0: 0. 1: 16.	
	CAL_STOP	6	1=stop CAL procedure.	
	CAL_MANCH[1:0]	5:4	Select manual CAL channel. b00: R. b01: G. b10: B.	
	CAL_DB_HS	3	0/1=select VSYNC/HSYNC to update CAL display.	
	CALG_DISP	2	1=enable gain CAL for display.	
	CALG_DB_LD	1	1=force load gain CAL result to display.	
	CALG_DB_HOLD	0	1=hold current gain CAL result for display.	
11h (2622h)	REG2622	7:0	Default : 0x92	Access : R/W
	CALO_DISP	7	1=enable offset CAL for display.	
	CALO_DB_LD	6	1=force load CAL result to display.	
	CALO_DB_HOLD	5	1=hold current CAL result for display.	
	CALD_DISP	4	1=enable digital offset CAL for display.	
	CALD_DB_TH[3:0]	3:0	Select threshold level to update CAL result.	
11h (2623h)	REG2623	7:0	Default : 0x40	Access : R/W
	CALO_HOLDY	7	1=hold current ADC_Y offset CAL result.	
	CAL_LOCK	6	1=wait pll lock to start CAL for ADC mode.	
	CAL_LIVET	5	1=enable fast tracking in CAL live mode.	
	CAL_LMT	4	1=enable limit CAL result range for CAL live mode.	
	CAL_LMTV[3:0]	3:0	Select limited range for CAL result update.	
12h	REG2624	7:0	Default : 0x60	Access : R/W

ADC Register (Bank = 26)

Index (Absolute)	Mnemonic	Bit	Description
(2624h)	CAL_VS	7	1=CAL synchronize to VSYNC.
	CAL_BW	6	1=enable max ADC bandwidth during CAL.
	CAL_COREV[3:0]	5:2	Select error coring threshold for CAL fine mode.
	CAL_ERRCOEF[1:0]	1:0	Select CAL error coefficient; 00=1; 01=1/2; 10=1/4; 11=1/8.
12h (2625h)	REG2625	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	CALD_EN	6	1=enable digital offset calibration function.
	CALD_DIT_CAL	5	1=enable digital dither for CAL.
	CALD_DIT_DISP	4	1=enable digital dither for display.
	DGAIN_SEL[1:0]	3:2	Select digital gain of ADC data. b00: 1.0. b01: 1.004. b10: 1.008. b11: 1.016.
	CALD_MAX[1:0]	1:0	Select digital offset max range; 00=1; 01=2; 10=3; 11=4(8-bit LSB).
13h (2626h)	REG2626	7:0	Default : 0x0A Access : R/W
	RESERVED_13H[1:0]	7:6	Reserved.
	CAL_SWOV[1:0]	5:4	Override CAL switch control, 00=none, 01=CALO, 10=CALG_VL, 11=CALG_VH.
	CAL_A2D_STEP[3:0]	3:0	Define equivalent code of 1 ADC offset step (in 12-bit resolution).
13h (2627h)	REG2627	7:0	Default : 0x68 Access : R/W
	NORM_GAIN[7:0]	7:0	Select ADC normal gain of 0.7Vpp for CALG.
14h (2628h)	REG2628	7:0	Default : 0x00 Access : R/W
	CAL_EDGE0	7	0/1=select CAL start from HSYNC leading/trailing edge for CAL to reference.
	CAL_DLY0[6:0]	6:0	CAL pulse start delay (N+1).
15h (262Ah)	REG262A	7:0	Default : 0x10 Access : R/W
	CAL_SMPDLY0[7:0]	7:0	CAL sample data delay (N+1).
15h (262Bh)	REG262B	7:0	Default : 0x10 Access : R/W
	CAL_SMPDUR0[7:0]	7:0	CAL sample data duration (N+1).
16h	REG262C	7:0	Default : 0x90 Access : R/W

ADC Register (Bank = 26)				
Index (Absolute)	Mnemonic	Bit	Description	
(262Ch)	CAL_EDGE1	7	0/1=select CAL start from HSYNC leading/trailing edge for CAL live mode.	
	CAL_DLY1[6:0]	6:0	CAL pulse start delay (N+1).	
17h (262Eh)	REG262E	7:0	Default : 0x08	Access : R/W
	CAL_SMPDLY1[7:0]	7:0	CAL sample data delay (N+1).	
17h (262Fh)	REG262F	7:0	Default : 0x08	Access : R/W
	CAL_SMPDUR1[7:0]	7:0	CAL sample data duration (N+1).	
18h (2630h)	REG2630	7:0	Default : 0x00	Access : R/W
	CAL_SKIPLINE[7:0]	7:0	Skip lines for CAL pulse, [3:0]=normal mode, [7:4]=live mode.	
19h ~ 19h (2632h ~ 2633h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
1Ah (2634h)	REG2634	7:0	Default : 0x00	Access : R/W
	RESERVED_1AH[3:0]	7:4	Reserved.	
	CAL_STATUS_SEL[3:0]	3:0	Select CAL status report.	
1Bh (2636h)	REG2636	7:0	Default : 0x00	Access : RO
	CAL_STATUS[7:0]	7:0	Internal CAL status.	
1Bh (2637h)	REG2637	7:0	Default : 0x00	Access : RO
	CAL_STATUS[15:8]	7:0	See description of '2636h'.	
1Ch (2638h)	REG2638	7:0	Default : 0x00	Access : RO
	ADC_CLPERR[7:0]	7:0	ADC clamp error status (format=S3), [3:0]=R, [7:4]=G, [11:8]=B.	
1Ch (2639h)	REG2639	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	ADC_CLPERR[11:8]	3:0	See description of '2638h'.	
1Dh (263Ah)	REG263A	7:0	Default : 0x00	Access : RO, WO
	-	7	Reserved.	
	CLROVF_RGB	6	Write an 1 to clear ADC_RGB overflow flags.	
	OVF_RGB[5:0]	5:0	ADC overflow flags, {OVFB, UNFB, OVFG, UNFG, OVFR, UNFR}.	
1Eh (263Ch)	REG263C	7:0	Default : 0x00	Access : R/W
	DITV_R[1:0]	7:6	ADC_R dither dc level.	

ADC Register (Bank = 26)				
Index (Absolute)	Mnemonic	Bit	Description	
	DIT_CAL[2:0]	5:3	Select ADC dither mode for CAL. b000: Off. b001: 1-bit noise. b010: 2-bit noise. b011: 3-bit noise. b100: Seq2 1-bit toggle noise. b101: Seq2 2-bit toggle noise. b110: Seq4 2-bit toggle noise. b110: Seq4 3-bit toggle noise.	
	DIT_DISP[2:0]	2:0	Select ADC dither mode for display.	
1Eh (263Dh)	REG263D	7:0	Default : 0x49	Access : R/W
	-	7	Reserved.	
	DITV_B[2:0]	6:4	ADC_B dither dc level.	
	DITV_G[2:0]	3:1	ADC_G dither dc level.	
	DITV_R[2]	0	See description of '263Ch'.	

HDMI_CTRL Register (Bank = 27)

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
01h (2702h)	REG2702	7:0	Default : 0x00	Access : R/W
	VS_PKT	7	Vendor Specific Packet or user specified packet received. NOTE: All bits in HDMIST1 register represent, when reading back 1, one or more than one packets have been received by the HDMI receiver engine between the previous read and current read. No packet was received since last read if a bit is read back 0.	
	ACR_PKT	6	Audio Clock Regeneration Packet received.	
	ASAMPLE_PKT	5	Audio Sample Packet received.	
	GCP_PKT	4	General Control Packet received.	
	AVI_PKT	3	AVI InfoFrame Packet received.	
	SPD_PKT	2	SPD InfoFrame Packet received.	
	AUI_PKT	1	Audio InfoRame Packet received.	
	MPEG_PKT	0	MPEG InfoFrame Packet received.	
01h (2703h)	REG2703	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	GM_PKT	5	Gamut Metadata packet received. NOTE: Bits [13:0] in register represent, when reading back 1, one or more than one packets have been received by the HDMI receiver engine between the previous read and current read. No packet was received since last read if a bit is read back 0.	
	DSD_PKT	4	DSD packet received.	
	ACP_PKT	3	ACP Packet received.	
	ISRC1_PKT	2	ISRC1 Packet received.	
	ISRC2_PKT	1	ISRC2 Packet received.	
	NULL_PKT	0	Null Packet received.	
02h (2704h)	REG2704	7:0	Default : 0x00	Access : R/W
	VCLK_BIG_CHG	7	HDMI video clock frequency big change.	
	CTSN_OV_RANGE	6	Received CTS N over range.	
	PIX_DE_CNT_DIFF	5	The number of DE pixel changed. 0: No event.	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
			1: Changed.	
	-	4	Reserved.	
	AFIFO34_FULL	3	Audio FIFO 3/4 has been Full. (write 1 to clear).	
	AFIFO34_EMPTY	2	Audio FIFO 3/4 has been Empty. (write 1 to clear).	
	AFIFO12_FULL	1	Audio FIFO 1/2 has been Full. (Write to clear).	
	AFIFO12_EMPTY	0	Audio FIFO 1/2 has been Empty. (Write 1 to clear).	
02h (2705h)	REG2705	7:0	Default : 0x00	Access : RO, R/W
	-	7:5	Reserved.	
	VCLK_STABLE	4	HDMI video clock is stable or not. 0: Not stable. 1: Stable.	
	-	3:0	Reserved.	
04h (2708h)	REG2708	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	AS_PBIT_ERR	5	Audio sample Parity bit error detected. (write 1 to clear).	
	ASAMPLE_ERR	4	Audio Sample packet receive Error occurred; sample repeated.	
	UNSUPPKT	3	Unsupported Packet received. (Write 1 to clear).	
	CHECKSUM_ERR	2	Checksum Error occurred; packet discarded. (Write 1 to clear).	
	BCHPRTY_ERR	1	BCH parity Error occurred; packet discarded. (Write 1 to clear).	
	BCHERR_CORRECTED	0	Single bit BCH parity Error occurred and Corrected. (Write 1 to clear).	
04h (2709h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
05h (270Ah)	REG270A	7:0	Default : 0x00	Access : R/W
	CTS_FIFO_BYPASS	7	Bypass CTS FIFO. 0: Disable.	

HDMI_CTRL Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description
			1: Enable.
	RESET_CTS_FIFO	6	Reset CTS FIFO. 0: Enable. 1: Disable.
	AFIFO_TH[1:0]	5:4	Audio FIFO start operation threshold. 00: Immediately. 01: After 1/4 fullness. 10: After 1/2 fullness. 11: After 3/4 fullness.
	-	3:2	Reserved.
	EN_USPPKT	1	Enable User specified Packet based on header type defined at PKTTYPER register. 0: Disable. 1: Enable.
	-	0	Reserved.
05h ~ 06h (270Bh ~ 270Ch)	-	7:0	Default : -
	-	-	Reserved.
06h (270Dh)	REG270D	7:0	Default : 0xE0
	VIDEO_BLANK_SEL	7	Output black level in video blanking for YCbCr format. 0: Output Y=0, Cb=0, and Cr=0. 1: Output black level.
	GCP_OUT_SEL	6	Output current deep color information or new received GCP packet to GCONTROL register. 0: New received GCP packet. 1: Deep color information.
	ASFLAT_CHK	5	Audio sample flat bit check. 0: Disable. 1: Enable.
	AFIFO_RST	4	Reset Audio FIFO/ (clear FIFO contents); all channels. 0: Normal. 1: Reset audio FIFO.
	EN_AVMUTE	3	Enable video mute. 0: Disable. 1: Enable when AVMUTE signal is received.
	VMUTEBLANK	2	Blanking when AV mute is active. 0: Disbale.

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable.	
	HDMI_AUTO_EN	1	Enable HDMI/DVI mode detection. 0: HDMI/DVI mode is set by F/W. 1: HDMI/DVI mode is detected by hardware automatically.	
	EN_AVMUTEDET	0	Enable Auto Video Mute processing based on AVMUTE. 0: No action. 1: Entering video mute and free run automatically when AVMUTE is set. Free run is cleared back to normal mode by F/W.	
07h (270Eh)	REG270E	7:0	Default : 0x00	Access : R/W, WO
	MANUAL_AP_SEL	7	Manual adjust phase select. 0: Adjust phase by default phase. 1: Write reg_manual_adjust_phase bit to shift one phase.	
	MANUAL_ADJUST_PHASE	6	Write 1 to this bit to adjust pixel packing phase. It's valid only if reg_manual_color_depth`0 and reg_manual_ap_sel=1.	
	DIS_NO_GCP_QUIT	5	Disable auto exit deep color mode if the sink does not receive a GCP with non-zero CD for more than 4 consecutive video fields. 0: Enable. 1: Disable.	
	MANUAL_COLOR_DEPTH[1:0]	4:3	Manual color depth. 00: Disable. 01: 30 bits per pixel. 10: 36 bits per pixel. 11: Reserved.	
	EN_DF_ADJUST	2	Adjust phase by default phase in deep color mode. 0: Disable. 1: Enable.	
	AUTO_RST_DC_FIFO	1	Auto reset deep color FIFO if overflow or underflow occurs. 0: Disable. 1: Enable.	
	EN_DEEP_COLOR	0	Enable deep color mode. 0: Disable. 1: Enable.	
07h (270Fh)	REG270F	7:0	Default : 0x00	Access : R/W, WO
	-	7	Reserved.	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
	EN_CTSN_FILTER	6	Enable CTS N filter. 0: Disable. 1: Enable.	
	-	5:2	Reserved.	
	CD_ZERO_UPDATE	1	0: Update Deep Color information only if received CD value is not zero. 1: Update Deep Color information when any GCP packet is received.	
	WP_AUTO_ADJUST	0	Wrong phase auto adjustment in deep color mode. 0: Normal. 1: Auto adjust phase.	
08h ~ 09h (2710h ~ 2712h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
09h (2713h)	REG2713	7:0	Default : 0x00	Access : R/W
	N_LMT_1[3:0]	7:4	Limited N value [19:16].	
	CTS_LMT_1[3:0]	3:0	Limited CTS value [19:16].	
0Ah (2714h)	REG2714	7:0	Default : 0x00	Access : R/W
	CTS_LMT_0[7:0]	7:0	Limited CTS value [15:0].	
0Ah (2715h)	REG2715	7:0	Default : 0x00	Access : R/W
	CTS_LMT_0[15:8]	7:0	See description of '2714h'.	
0Bh (2716h)	REG2716	7:0	Default : 0x00	Access : R/W
	N_LMT_0[7:0]	7:0	Limited N value [15:0].	
0Bh (2717h)	REG2717	7:0	Default : 0x00	Access : R/W
	N_LMT_0[15:8]	7:0	See description of '2716h'.	
0Ch (2718h)	REG2718	7:0	Default : 0x0A	Access : R/W
	VLD_CTS_RANGE[7:0]	7:0	Program these bits to define valid CTS range. CTS_LMT- VLD_CTS_RANGE < Valid CTS < CTS_LMT+ VLD_CTS_RANGE.	
0Ch (2719h)	REG2719	7:0	Default : 0x0A	Access : R/W
	VLD_N_RANGE[7:0]	7:0	Program these bits to define valid N range. N_LMT- VLD_N_RANGE < Valid N < N_LMT+ VLD_N_RANGE.	
0Dh (271Ah)	REG271A	7:0	Default : 0x00	Access : R/W
	CMPVAL50[7:0]	7:0	50M Count Value.	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
0Dh (271Bh)	REG271B	7:0	Default : 0x00	Access : R/W
	CMPVAL50[15:8]	7:0	See description of '271Ah'.	
0Eh (271Ch)	REG271C	7:0	Default : 0x00	Access : R/W
	CMPVAL100[7:0]	7:0	100M Count Value.	
0Eh (271Dh)	REG271D	7:0	Default : 0x00	Access : R/W
	CMPVAL100[15:8]	7:0	See description of '271Ch'.	
0Fh (271Eh)	REG271E	7:0	Default : 0x00	Access : R/W
	CMPVAL200[7:0]	7:0	200M Count Value.	
0Fh (271Fh)	REG271F	7:0	Default : 0x00	Access : R/W
	CMPVAL200[15:8]	7:0	See description of '271Eh'.	
10h (2720h)	REG2720	7:0	Default : 0x00	Access : R/W
	PKT_TYPE[7:0]	7:0	Used for vendor specific packet capture.	
11h (2722h)	REG2722	7:0	Default : 0x00	Access : RO
	CNT_VAL[7:0]	7:0	Count value TMDS clock.	
11h (2723h)	REG2723	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	FIN[1:0]	6:5	TMDS clock frequency range detection. 00: Less than 50MHz. 01: Between 50 and 100 MHz. 10: Between 100 and 200MHz. 11: Greater than 200 MHz.	
	CNT_VAL[12:8]	4:0	See description of '2722h'.	
12h (2724h)	REG2724	7:0	Default : 0x00	Access : R/W
	CTS_0[7:0]	7:0	CTS[15:0] value received from Audio Clock regeneration packet. Write this register to update CTS and N value.	
12h (2725h)	REG2725	7:0	Default : 0x00	Access : R/W
	CTS_0[15:8]	7:0	See description of '2724h'.	
13h (2726h)	REG2726	7:0	Default : 0x00	Access : RO
	N_0[7:0]	7:0	N[15:0] value received from Audio Clock regeneration packet.	
13h (2727h)	REG2727	7:0	Default : 0x00	Access : RO
	N_0[15:8]	7:0	See description of '2726h'.	
14h	REG2728	7:0	Default : 0x00	Access : RO

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
(2728h)	N_1[7:4]	7:4	N[15:0] value received from Audio Clock regeneration packet.	
	CTS_1[3:0]	3:0	CTS[19:16] value received from Audio Clock regeneration packet.	
15h (272Ah)	REG272A	7:0	Default : 0x00	Access : RO
	GCONTROL[7:0]	7:0	[0]: AVMUTE received from general control packet. 0 = Clear AVMUTE. 1 = Set AVMUTE. [1]: Default_Phase in GCP subpacket byte 2. [4:2]: Reflects RX last packing phase for each video period. Read only. 000 = Phase 0 (10P0, 12P0, 16P0). 001 = Phase 1 (10P1, 12P1, 16P1). 010 = Phase 2 (10P2, 12P2). 011 = Phase 3 (10P3). 100 = Phase 4 (10P4). 101~111 = Reserved. [7:5]: Previous last packing phase. [11:8]: Color depth in GCP subpacket byte 1. [15:12]: Pixel packing phase in GCP subpacket byte 1.	
15h (272Bh)	REG272B	7:0	Default : 0x00	Access : RO
	GCONTROL[15:8]	7:0	See description of '272Ah'.	
16h (272Ch)	REG272C	7:0	Default : 0x00	Access : RO
	ACP_HDR1[7:0]	7:0	Content protection type field from Audio Content Protection (ACP) packet. 0x00 = Generic Audio. 0x01 = IEC 60958-Identified Audio. 0x02 = DVD-Audio. 0x03 = Reserved for Super Audio CD (SACD). 0x04&0xFF = Reserved.	
17h (272Eh)	REG272E	7:0	Default : 0x00	Access : RO
	ACP_PB0[7:0]	7:0	ACP packet payload byte 0.	
17h (272Fh)	REG272F	7:0	Default : 0x00	Access : RO
	ACP_PB1[7:0]	7:0	ACP packet payload byte 1.	
18h (2730h)	REG2730	7:0	Default : 0x00	Access : RO
	ACP_PB2[7:0]	7:0	ACP packet payload byte 2.	
18h	REG2731	7:0	Default : 0x00	Access : RO

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
(2731h)	ACP_PB3[7:0]	7:0	ACP packet payload byte 3.	
19h	REG2732	7:0	Default : 0x00	Access : RO
(2732h)	ACP_PB4[7:0]	7:0	ACP packet payload byte 4.	
19h	REG2733	7:0	Default : 0x00	Access : RO
(2733h)	ACP_PB5[7:0]	7:0	ACP packet payload byte 5.	
1Ah	REG2734	7:0	Default : 0x00	Access : RO
(2734h)	ACP_PB6[7:0]	7:0	ACP packet payload byte 6.	
1Ah	REG2735	7:0	Default : 0x00	Access : RO
(2735h)	ACP_PB7[7:0]	7:0	ACP packet payload byte 7.	
1Bh	REG2736	7:0	Default : 0x00	Access : RO
(2736h)	ACP_PB8[7:0]	7:0	ACP packet payload byte 8.	
1Bh	REG2737	7:0	Default : 0x00	Access : RO
(2737h)	ACP_PB9[7:0]	7:0	ACP packet payload byte 9.	
1Ch	REG2738	7:0	Default : 0x00	Access : RO
(2738h)	ACP_PB10[7:0]	7:0	ACP packet payload byte 10.	
1Ch	REG2739	7:0	Default : 0x00	Access : RO
(2739h)	ACP_PB11[7:0]	7:0	ACP packet payload byte 11.	
1Dh	REG273A	7:0	Default : 0x00	Access : RO
(273Ah)	ACP_PB12[7:0]	7:0	ACP packet payload byte 12.	
1Dh	REG273B	7:0	Default : 0x00	Access : RO
(273Bh)	ACP_PB13[7:0]	7:0	ACP packet payload byte 13.	
1Eh	REG273C	7:0	Default : 0x00	Access : RO
(273Ch)	ACP_PB14[7:0]	7:0	ACP packet payload byte 14.	
1Eh	REG273D	7:0	Default : 0x00	Access : RO
(273Dh)	ACP_PB15[7:0]	7:0	ACP packet payload byte 15.	
1Fh	REG273E	7:0	Default : 0x00	Access : R/W
(273Eh)	ISRC1_HDR1[7:0]	7:0	ISRC1 packet header byte 1. Write this register to update GM packet.	
1Fh	REG273F	7:0	Default : 0x00	Access : RO
(273Fh)	GBD_HDR2[7:0]	7:0	GM packet header byte 2.	
20h	REG2740	7:0	Default : 0x00	Access : RO
(2740h)	ISRC_PB0[7:0]	7:0	ISRC packet payload byte 0.	
20h	REG2741	7:0	Default : 0x00	Access : RO

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
(2741h)	ISRC_PB1[7:0]	7:0	ISRC packet payload byte 1.	
21h	REG2742	7:0	Default : 0x00	Access : RO
(2742h)	ISRC_PB2[7:0]	7:0	ISRC packet payload byte 2.	
21h	REG2743	7:0	Default : 0x00	Access : RO
(2743h)	ISRC_PB3[7:0]	7:0	ISRC packet payload byte 3.	
22h	REG2744	7:0	Default : 0x00	Access : RO
(2744h)	ISRC_PB4[7:0]	7:0	ISRC packet payload byte 4.	
22h	REG2745	7:0	Default : 0x00	Access : RO
(2745h)	ISRC_PB5[7:0]	7:0	ISRC packet payload byte 5.	
23h	REG2746	7:0	Default : 0x00	Access : RO
(2746h)	ISRC_PB6[7:0]	7:0	ISRC packet payload byte 6.	
23h	REG2747	7:0	Default : 0x00	Access : RO
(2747h)	ISRC_PB7[7:0]	7:0	ISRC packet payload byte 7.	
24h	REG2748	7:0	Default : 0x00	Access : RO
(2748h)	ISRC_PB8[7:0]	7:0	ISRC packet payload byte 8.	
24h	REG2749	7:0	Default : 0x00	Access : RO
(2749h)	ISRC_PB9[7:0]	7:0	ISRC packet payload byte 9.	
25h	REG274A	7:0	Default : 0x00	Access : RO
(274Ah)	ISRC_PB10[7:0]	7:0	ISRC packet payload byte 10.	
25h	REG274B	7:0	Default : 0x00	Access : RO
(274Bh)	ISRC_PB11[7:0]	7:0	ISRC packet payload byte 11.	
26h	REG274C	7:0	Default : 0x00	Access : RO
(274Ch)	ISRC_PB12[7:0]	7:0	ISRC packet payload byte 12.	
26h	REG274D	7:0	Default : 0x00	Access : RO
(274Dh)	ISRC_PB13[7:0]	7:0	ISRC packet payload byte 13.	
27h	REG274E	7:0	Default : 0x00	Access : RO
(274Eh)	ISRC_PB14[7:0]	7:0	ISRC packet payload byte 14.	
27h	REG274F	7:0	Default : 0x00	Access : RO
(274Fh)	ISRC_PB15[7:0]	7:0	ISRC packet payload byte 15.	
28h	REG2750	7:0	Default : 0x00	Access : RO
(2750h)	ISRC_PB16[7:0]	7:0	ISRC packet payload byte 16.	
28h	REG2751	7:0	Default : 0x00	Access : RO
(2751h)	ISRC_PB17[7:0]	7:0	ISRC packet payload byte 17.	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
29h (2752h)	REG2752	7:0	Default : 0x00	Access : RO
	ISRC_PB18[7:0]	7:0	ISRC packet payload byte 18.	
29h (2753h)	REG2753	7:0	Default : 0x00	Access : RO
	ISRC_PB19[7:0]	7:0	ISRC packet payload byte 19.	
2Ah (2754h)	REG2754	7:0	Default : 0x00	Access : RO
	ISRC_PB20[7:0]	7:0	ISRC packet payload byte 20.	
2Ah (2755h)	REG2755	7:0	Default : 0x00	Access : RO
	ISRC_PB21[7:0]	7:0	ISRC packet payload byte 21.	
2Bh (2756h)	REG2756	7:0	Default : 0x00	Access : RO
	ISRC_PB22[7:0]	7:0	ISRC packet payload byte 22.	
2Bh (2757h)	REG2757	7:0	Default : 0x00	Access : RO
	ISRC_PB23[7:0]	7:0	ISRC packet payload byte 23.	
2Ch (2758h)	REG2758	7:0	Default : 0x00	Access : RO
	ISRC_PB24[7:0]	7:0	ISRC packet payload byte 24.	
2Ch (2759h)	REG2759	7:0	Default : 0x00	Access : RO
	ISRC_PB25[7:0]	7:0	ISRC packet payload byte 25.	
2Dh (275Ah)	REG275A	7:0	Default : 0x00	Access : RO
	ISRC_PB26[7:0]	7:0	ISRC packet payload byte 26.	
2Dh (275Bh)	REG275B	7:0	Default : 0x00	Access : RO
	ISRC_PB27[7:0]	7:0	ISRC packet payload byte 27.	
2Eh (275Ch)	REG275C	7:0	Default : 0x00	Access : RO
	ISRC_PB28[7:0]	7:0	ISRC packet payload byte 28.	
2Eh (275Dh)	REG275D	7:0	Default : 0x00	Access : RO
	ISRC_PB29[7:0]	7:0	ISRC packet payload byte 29.	
2Fh (275Eh)	REG275E	7:0	Default : 0x00	Access : RO
	ISRC_PB30[7:0]	7:0	ISRC packet payload byte 30.	
2Fh (275Fh)	REG275F	7:0	Default : 0x00	Access : RO
	ISRC_PB31[7:0]	7:0	ISRC packet payload byte 31.	
30h (2760h)	REG2760	7:0	Default : 0x00	Access : RO
	VS_HDR0[7:0]	7:0	Vender Specific Packet header byte 0.	
30h (2761h)	REG2761	7:0	Default : 0x00	Access : RO
	VS_HDR1[7:0]	7:0	Vender Specific Packet header byte 1.	
31h	REG2762	7:0	Default : 0x00	Access : RO

HDMI_CTRL Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description
(2762h)	VS_HDR2[7:0]	7:0	Vender Specific Packet header byte 2.
32h (2764h)	REG2764 VS_IF1[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 1.
32h (2765h)	REG2765 VS_IF2[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 2.
33h (2766h)	REG2766 VS_IF3[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 3.
33h (2767h)	REG2767 VS_IF4[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 4.
34h (2768h)	REG2768 VS_IF5[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 5.
34h (2769h)	REG2769 VS_IF6[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 6.
35h (276Ah)	REG276A VS_IF7[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 7.
35h (276Bh)	REG276B VS_IF8[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 8.
36h (276Ch)	REG276C VS_IF9[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 9.
36h (276Dh)	REG276D VS_IF10[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 10.
37h (276Eh)	REG276E VS_IF11[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 11.
37h (276Fh)	REG276F VS_IF12[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 12.
38h (2770h)	REG2770 VS_IF13[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 13.
38h (2771h)	REG2771 VS_IF14[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 14.
39h (2772h)	REG2772 VS_IF15[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 15.
39h (2773h)	REG2773 VS_IF16[7:0]	7:0	Default : 0x00 Vendor Specific Packet payload byte 16.

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
3Ah (2774h)	REG2774	7:0	Default : 0x00	Access : RO
	VS_IF17[7:0]	7:0	Vendor Specific Packet payload byte 17.	
3Ah (2775h)	REG2775	7:0	Default : 0x00	Access : RO
	VS_IF18[7:0]	7:0	Vendor Specific Packet payload byte 18.	
3Bh (2776h)	REG2776	7:0	Default : 0x00	Access : RO
	VS_IF19[7:0]	7:0	Vendor Specific Packet payload byte 19.	
3Bh (2777h)	REG2777	7:0	Default : 0x00	Access : RO
	VS_IF20[7:0]	7:0	Vendor Specific Packet payload byte 20.	
3Ch (2778h)	REG2778	7:0	Default : 0x00	Access : RO
	VS_IF21[7:0]	7:0	Vendor Specific Packet payload byte 21.	
3Ch (2779h)	REG2779	7:0	Default : 0x00	Access : RO
	VS_IF22[7:0]	7:0	Vendor Specific Packet payload byte 22.	
3Dh (277Ah)	REG277A	7:0	Default : 0x00	Access : RO
	VS_IF23[7:0]	7:0	Vendor Specific Packet payload byte 23.	
3Dh (277Bh)	REG277B	7:0	Default : 0x00	Access : RO
	VS_IF24[7:0]	7:0	Vendor Specific Packet payload byte 24.	
3Eh (277Ch)	REG277C	7:0	Default : 0x00	Access : RO
	VS_IF25[7:0]	7:0	Vendor Specific Packet payload byte 25.	
3Eh (277Dh)	REG277D	7:0	Default : 0x00	Access : RO
	VS_IF26[7:0]	7:0	Vendor Specific Packet payload byte 26.	
3Fh (277Eh)	REG277E	7:0	Default : 0x00	Access : RO
	VS_IF27[7:0]	7:0	Vendor Specific Packet payload byte 27.	
3Fh (277Fh)	REG277F	7:0	Default : 0x00	Access : RO
	VS_IF28[7:0]	7:0	Vendor Specific Packet payload byte 28.	
40h (2780h)	REG2780	7:0	Default : 0x00	Access : RO
	AVI_IF1[7:0]	7:0	AVI InfoFrame byte 1. [1:0]: Scan info. [3:2]: Ban info. [4]: Active format info present. [6:5]: RGB or YCbCr. [7]: Version.	
40h (2781h)	REG2781	7:0	Default : 0x00	Access : RO
	AVI_IF2[7:0]	7:0	AVI InfoFrame byte 2. [3:0]: Active format aspect ratio.	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
			[5:4]: Picture aspect ratio. [7:6]: Colorimetry.	
41h (2782h)	REG2782	7:0	Default : 0x00	Access : RO
	AVI_IF3[7:0]	7:0	AVI InfoFrame byte 3. [1:0]: Non-conforming Picture Scaling. 00: No known non-uniform scaling. 01: Picture has been scaled horizontally. 10: Picture has been scaled vertically. 11: Picture has been scaled horizontally and vertically. [3:2]: Quantization range. [5:4]: Extended colorimetry. [7]: IT content.	
41h (2783h)	REG2783	7:0	Default : 0x00	Access : RO
	AVI_IF4[7:0]	7:0	AVI InfoFrame byte 4. Video Identification Code. Refer to EIA/CEA 861B specification.	
42h (2784h)	REG2784	7:0	Default : 0x00	Access : RO
	AVI_IF5[7:0]	7:0	AVI InfoFrame byte 5. [3:0]: Pixel repetition; pixel sent (PR+1) times.	
42h (2785h)	REG2785	7:0	Default : 0x00	Access : RO
	AVI_IF6[7:0]	7:0	AVI InfoFrame byte 6. Line Number of end of Top bar [7:0].	
43h (2786h)	REG2786	7:0	Default : 0x00	Access : RO
	AVI_IF7[7:0]	7:0	AVI InfoFrame byte 7. Line Number of end of Top bar [15:8].	
43h (2787h)	REG2787	7:0	Default : 0x00	Access : RO
	AVI_IF8[7:0]	7:0	AVI InfoFrame byte 8. Line Number of start of Bottom bar [7:0].	
44h (2788h)	REG2788	7:0	Default : 0x00	Access : RO
	AVI_IF9[7:0]	7:0	AVI InfoFrame byte 9. Line Number of start of Bottom bar [15:8].	
44h (2789h)	REG2789	7:0	Default : 0x00	Access : RO
	AVI_IF10[7:0]	7:0	AVI InfoFrame byte 10. Pixel Number of end of Left bar [7:0].	
45h (278Ah)	REG278A	7:0	Default : 0x00	Access : RO
	AVI_IF11[7:0]	7:0	AVI InfoFrame byte 11.	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
			Pixel Number of end of Left bar [15:8].	
45h (278Bh)	REG278B	7:0	Default : 0x00	Access : RO
	AVI_IF12[7:0]	7:0	AVI InfoFrame byte 12. Pixel Number of end of Right bar [7:0].	
46h (278Ch)	REG278C	7:0	Default : 0x00	Access : RO
	AVI_IF13[7:0]	7:0	AVI InfoFrame byte 13. Pixel Number of end of Left bar [15:8].	
47h (278Eh)	REG278E	7:0	Default : 0x00	Access : RO
	SPD_IF1[7:0]	7:0	SPD InfoFrame byte 1.	
47h (278Fh)	REG278F	7:0	Default : 0x00	Access : RO
	SPD_IF2[7:0]	7:0	SPD InfoFrame byte 2.	
48h (2790h)	REG2790	7:0	Default : 0x00	Access : RO
	SPD_IF3[7:0]	7:0	SPD InfoFrame byte 3.	
48h (2791h)	REG2791	7:0	Default : 0x00	Access : RO
	SPD_IF4[7:0]	7:0	SPD InfoFrame byte 4.	
49h (2792h)	REG2792	7:0	Default : 0x00	Access : RO
	SPD_IF5[7:0]	7:0	SPD InfoFrame byte 5.	
49h (2793h)	REG2793	7:0	Default : 0x00	Access : RO
	SPD_IF6[7:0]	7:0	SPD InfoFrame byte 6.	
4Ah (2794h)	REG2794	7:0	Default : 0x00	Access : RO
	SPD_IF7[7:0]	7:0	SPD InfoFrame byte 7.	
4Ah (2795h)	REG2795	7:0	Default : 0x00	Access : RO
	SPD_IF8[7:0]	7:0	SPD InfoFrame byte 8.	
4Bh (2796h)	REG2796	7:0	Default : 0x00	Access : RO
	SPD_IF9[7:0]	7:0	SPD InfoFrame byte 9.	
4Bh (2797h)	REG2797	7:0	Default : 0x00	Access : RO
	SPD_IF10[7:0]	7:0	SPD InfoFrame byte 10.	
4Ch (2798h)	REG2798	7:0	Default : 0x00	Access : RO
	SPD_IF11[7:0]	7:0	SPD InfoFrame byte 11.	
4Ch (2799h)	REG2799	7:0	Default : 0x00	Access : RO
	SPD_IF12[7:0]	7:0	SPD InfoFrame byte 12.	
4Dh (279Ah)	REG279A	7:0	Default : 0x00	Access : RO
	SPD_IF13[7:0]	7:0	SPD InfoFrame byte 13.	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
4Dh (279Bh)	REG279B	7:0	Default : 0x00	Access : RO
	SPD_IF14[7:0]	7:0	SPD InfoFrame byte 14.	
4Eh (279Ch)	REG279C	7:0	Default : 0x00	Access : RO
	SPD_IF15[7:0]	7:0	SPD InfoFrame byte 15.	
4Eh (279Dh)	REG279D	7:0	Default : 0x00	Access : RO
	SPD_IF16[7:0]	7:0	SPD InfoFrame byte 16.	
4Fh (279Eh)	REG279E	7:0	Default : 0x00	Access : RO
	SPD_IF17[7:0]	7:0	SPD InfoFrame byte 17.	
4Fh (279Fh)	REG279F	7:0	Default : 0x00	Access : RO
	SPD_IF18[7:0]	7:0	SPD InfoFrame byte 18.	
50h (27A0h)	REG27A0	7:0	Default : 0x00	Access : RO
	SPD_IF19[7:0]	7:0	SPD InfoFrame byte 19.	
50h (27A1h)	REG27A1	7:0	Default : 0x00	Access : RO
	SPD_IF20[7:0]	7:0	SPD InfoFrame byte 20.	
51h (27A2h)	REG27A2	7:0	Default : 0x00	Access : RO
	SPD_IF21[7:0]	7:0	SPD InfoFrame byte 21.	
51h (27A3h)	REG27A3	7:0	Default : 0x00	Access : RO
	SPD_IF22[7:0]	7:0	SPD InfoFrame byte 22.	
52h (27A4h)	REG27A4	7:0	Default : 0x00	Access : RO
	SPD_IF23[7:0]	7:0	SPD InfoFrame byte 23.	
52h (27A5h)	REG27A5	7:0	Default : 0x00	Access : RO
	SPD_IF24[7:0]	7:0	SPD InfoFrame byte 24.	
53h (27A6h)	REG27A6	7:0	Default : 0x00	Access : RO
	SPD_IF25[7:0]	7:0	SPD InfoFrame byte 25.	
54h (27A8h)	REG27A8	7:0	Default : 0x00	Access : RO
	AU_IF1[7:0]	7:0	Audio InfoFrame byte 1.	
54h (27A9h)	REG27A9	7:0	Default : 0x00	Access : RO
	AU_IF2[7:0]	7:0	Audio InfoFrame byte 2.	
55h (27AAh)	REG27AA	7:0	Default : 0x00	Access : RO
	AU_IF3[7:0]	7:0	Audio InfoFrame byte 3.	
55h (27ABh)	REG27AB	7:0	Default : 0x00	Access : RO
	AU_IF4[7:0]	7:0	Audio InfoFrame byte 4.	
56h	REG27AC	7:0	Default : 0x00	Access : RO

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
(27ACh)	AU_IF5[7:0]	7:0	Audio InfoFrame byte 5.	
57h	REG27AE	7:0	Default : 0x00	Access : RO
(27AEh)	MPEG_IF1[7:0]	7:0	MPEG InfoFrame byte 1.	
57h	REG27AF	7:0	Default : 0x00	Access : RO
(27AFh)	MPEG_IF2[7:0]	7:0	MPEG InfoFrame byte 2.	
58h	REG27B0	7:0	Default : 0x00	Access : RO
(27B0h)	MPEG_IF3[7:0]	7:0	MPEG InfoFrame byte 3.	
58h	REG27B1	7:0	Default : 0x00	Access : RO
(27B1h)	MPEG_IF4[7:0]	7:0	MPEG InfoFrame byte 4.	
59h	REG27B2	7:0	Default : 0x00	Access : RO
(27B2h)	MPEG_IF5[7:0]	7:0	MPEG InfoFrame byte 5.	
5Ah	REG27B4	7:0	Default : 0x00	Access : RO
(27B4h)	HDMI_CS[7:0]	7:0	HDMI audio Channel Status.	
5Ah	REG27B5	7:0	Default : 0x00	Access : RO
(27B5h)	HDMI_CS[15:8]	7:0	See description of '27B4h'.	
5Bh	REG27B6	7:0	Default : 0x00	Access : RO
(27B6h)	HDMI_CS[23:16]	7:0	See description of '27B4h'.	
5Bh	REG27B7	7:0	Default : 0x00	Access : RO
(27B7h)	HDMI_CS[31:24]	7:0	See description of '27B4h'.	
5Ch	REG27B8	7:0	Default : 0x00	Access : RO
(27B8h)	HDMI_CS[39:32]	7:0	See description of '27B4h'.	
5Ch	REG27B9	7:0	Default : 0x00	Access : R/W
(27B9h)	MANUAL_HPLL_DIV	7	Enable PLL divider is controlled by registers. 0: Disable. 1: Enable.	
	HPLL_PORST	6	HDMI PLL reset. 0: Normal. 4: Reset (all analog front-end & dividers).	
	HPLL_RESET_TP	5	HDMI PLL post clock divider reset. (KP). 0: Normal. 3: Reset.	
	HPLL_RESET_TF	4	HDMI PLL feedback clock divider reset. (FBDIV & KM).	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: Normal. 2: Reset.	
	HPLL_RESET_TI	3	HDMI PLL input clock divider reset. (DDIV & KN). 0: Normal. 1: Reset.	
	HPLL_VCO_OFFSET	2	Enable VCO free running. 0: Enable. 1: Disable.	
	HPLL_RESET	1	HDMI PLL reset. 0: No reset. 1: Reset.	
	HPLL_PDN	0	HDMI PLL power down. 0: No action. 1: Power down.	
5Dh (27BAh)	REG27BA	7:0	Default : 0x10	Access : R/W
	HPLL_KN[1:0]	7:6	HDMI PLL KN divider ratio for new mode. 00 = /1. 01 = /2. 10 = /4. 11 = /4.	
	HPLL_RCTRL[2:0]	5:3	HDMI PLL loop filter resistor control. 000 = 23.1K ohm. 001 = 26.4K ohm. 010 = 29.7K ohm. ... 111 = 42.9K ohm.	
	HPLL_ICTRL[2:0]	2:0	HDMI PLL charge pump current control. 000 = 0.65uA. 001 = 1.29uA. 010 = 1.935uA. 011 = 2.58uA. 100 = 3.225uA. 101 = 3.87uA. 110 = 5.16uA. 111 = 10.32uA.	
5Dh (27BBh)	REG27BB	7:0	Default : 0x00	Access : R/W
	HPLL_KP[3:0]	7:4	HDMI PLL Post divider ratio (KP) for new mode.	

HDMI_CTRL Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
			0000 = / 1. 0001 = / 2. 0010 = / 4. ... 1001 = / 512. 1010 = / 1024. 1011 = / 1024. ... 1111 = / 1024.	
	HPLL_KM[3:0]	3:0	HDMI PLL KM divider ratio for new mode. 0000 = / 1. 0001 = / 2. 0010 = / 4. ... 0111 = / 128. 1000 = / 256. 1001 = / 256. ... 1111 = / 256.	
5Eh (27BCh)	REG27BC	7:0	Default : 0x00	Access : R/W
	HPLL_DDIV[3:0]	7:4	HDMI PLL feedback overwrite divider value from noise-shape quantizer for new mode. 0000 = N.A. (/16). 0001 = N.A. (/17). 0010 = /2. 0011 = /3. ... 1111 = /15.	
	HPLL_FBDIV[3:0]	3:0	HDMI PLL input overwrite divider value from noise-shape quantizer for new mode. 0000 = N.A. (/16). 0001 = N.A. (/17). 0010 = /2. 0011 = /3. ...	

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
			1111 = /15.	
5Eh (27BDh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
5Fh (27BEh)	REG27BE	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	FRAME_RP_VAL[2:0]	5:3	Frame repetition value.	
	HPLL_LOCK_RAW	2	HDMI PLL lock raw flag.	
	HPLL_HIGH_FLAG	1	HDMI PLL output flag for vco supply voltage too high.	
	HPLL_LOCK	0	HDMI PLL lock flag.	
5Fh (27BFh)	REG27BF	7:0	Default : 0x00	Access : R/W
	PKT_RST[7:0]	7:0	[0]: Reset AVMUTE register at GCONTROL:AVMUTE. 0: No reset. 1: Reset AVMUTE to 0 (Clear AVMUTE). [1]: Reset Y (Color format) register at AVI_IF1:Y[1:0]. 0: No reset. 1: Reset Y to 00 (RGB format). [2]: Reset Pixel Repetition register at AVI_IF4:PR[3:0]. 0: No reset. 1: Reset PR to 0 (no repetition). [3]: Reset frame repetition to 0. 0: Output frame repetition information to video engine based on frame format. 1: Reset frame repetition to 0. [4]: Reset CD, PP, and default phase value of GCP packet. 0: No reset. 1: Reset. [5]: Reset deep color FIFO. 0: No reset. 1: Reset. [6]: Reserved. [7]: Reset HDMI status registers. Asserting this bit resets HDMIST1~HDMIST2, HDMI_ERR1, AVI_IF0~AVI_IF6, AUDIO_IF0~AUDIO_IF2, SPD_IF0~SPD_IF12, MPEG_IF0~MPEG_IF2, VS_HDR0~VS_HDR1, VS_IF0~VS_IF13, ACP_HB1, ACP_DATA0~ACP_DATA7, ISRC_HB1, ISRC_DATA0~ISRC_DATA15 registers. 0: No reset.	

HDMI_CTRL Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description
			1: Reset.
60h (27C0h)	REG27C0	7:0	Default : 0x00 Access : R/W
	INT_MASK[7:0]	7:0	Mask packet reception update interrupt (generate an interrupt when a new packet is received and it is different from the previous received packet). 0: Unmask. 1: Mask. [0]: General Control packet. [1]: AVI InfoFrame packet. [2]: Audio InfoFrame packet. [3]: MPEG InfoFrame packet. [4]: ACP packet. [5]: ISRC packet. [6]: BCH error. [7]: Gamut Metadata packet. [12]: CTS N over range. [13]: HDMI video clock frequency big change.
60h (27C1h)	REG27C1	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	INT_MASK[13:8]	5:0	See description of '27C0h'.
61h (27C2h)	REG27C2	7:0	Default : 0x00 Access : RO
	INT_STATUS[7:0]	7:0	Interrupt status. [0]: General Control packet. [1]: AVI InfoFrame packet. [2]: Audio InfoFrame packet. [3]: MPEG InfoFrame packet. [4]: ACP packet. [5]: ISRC packet. [6]: BCH error. [7]: Gamut Metadata packet. [12]: CTS N over range. [13]: HDMI video clock frequency big change.
61h (27C3h)	REG27C3	7:0	Default : 0x00 Access : RO
	-	7:6	Reserved.
	INT_STATUS[13:8]	5:0	See description of '27C2h'.
62h (27C4h)	REG27C4	7:0	Default : 0x00 Access : R/W
	INT_FORCE[7:0]	7:0	Force interrupt. [0]: General Control packet.

HDMI_CTRL Register (Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description
			[1]: AVI InfoFrame packet. [2]: Audio InfoFrame packet. [3]: MPEG InfoFrame packet. [4]: ACP packet. [5]: ISRC packet. [6]: BCH error. [7]: Gamut Metadata packet. [12]: CTS N over range. [13]: HDMI video clock frequency big change.
62h (27C5h)	REG27C5	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	INT_FORCE[13:8]	5:0	See description of '27C4h'.
63h (27C6h)	REG27C6	7:0	Default : 0x00 Access : R/W
	INT_CLR[7:0]	7:0	Clear interrupt. [0]: General Control packet. [1]: AVI InfoFrame packet. [2]: Audio InfoFrame packet. [3]: MPEG InfoFrame packet. [4]: ACP packet. [5]: ISRC packet. [6]: BCH error. [7]: Gamut Metadata packet. [12]: CTS N over range. [13]: HDMI video clock frequency big change.
63h (27C7h)	REG27C7	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	INT_CLR[13:8]	5:0	See description of '27C6h'.
64h (27C8h)	REG27C8	7:0	Default : 0x00 Access : R/W
	FRAME_RP_MODE[3:0]	7:4	[2:0]: Frame repetition value for manual mode. Allowed values: 1, 2, and 4. [3]: Frame repetition mode. 0: Auto mode. 1: Manual mode.
	AUDIO_MODE[3:0]	3:0	[0]: Manual non-PCM mode. [1]: Auto detect non-PCM mode. [2]: Manual DSD mode. [3]: Auto detect DSD mode.
64h	REG27C9	7:0	Default : 0x00 Access : R/W

HDMI_CTRL Register (Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
(27C9h)	-	7:5	Reserved.	
	HDMI_AU_FIFO_MUTE_EN[4:0]	4:0	Enable the following events to trigger audio controller to output mute audio (DC value). [0]: HDMI CTS/N over limited range (reg_ctsn_ov_range bit). [1]: HDMI video clock frequency big change (reg_vclk_big_chg bit). [2]: AVMute. [3]: Audio sample parity error (reg_as_pbit_err bit). [4]: Audio sample BCH error (reg_asample_err bit).	
65h (27CAh)	REG27CA	7:0	Default : 0x00	Access : RO
	PIX_DE_CNT[7:0]	7:0	Pixel DE count.	
65h (27CBh)	REG27CB	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	PIX_DE_CNT[12:8]	4:0	See description of '27CAh'.	

IRQ Register (Bank = 2B)

IRQ Register (Bank = 2B)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2B00h)	REG2B00	7:0	Default : 0xFF	Access : R/W
	C_FIQ_MASK[7:0]	7:0	Mask for FIQ, bit[31:0]. 1: Mask. 0: Not mask.	
00h (2B01h)	REG2B01	7:0	Default : 0xFF	Access : R/W
	C_FIQ_MASK[15:8]	7:0	See description of '2B00h'.	
01h (2B02h)	REG2B02	7:0	Default : 0xFF	Access : R/W
	C_FIQ_MASK[23:16]	7:0	See description of '2B00h'.	
01h (2B03h)	REG2B03	7:0	Default : 0xFF	Access : R/W
	C_FIQ_MASK[31:24]	7:0	See description of '2B00h'.	
02h (2B04h)	REG2B04	7:0	Default : 0x00	Access : R/W
	C_FIQ_FORCE[7:0]	7:0	Force for FIQ, bit[31:0]. 1: Force. 0: Not force.	
02h (2B05h)	REG2B05	7:0	Default : 0x00	Access : R/W
	C_FIQ_FORCE[15:8]	7:0	See description of '2B04h'.	
03h (2B06h)	REG2B06	7:0	Default : 0x00	Access : R/W
	C_FIQ_FORCE[23:16]	7:0	See description of '2B04h'.	
03h (2B07h)	REG2B07	7:0	Default : 0x00	Access : R/W
	C_FIQ_FORCE[31:24]	7:0	See description of '2B04h'.	
04h (2B08h)	REG2B08	7:0	Default : 0x00	Access : R/W
	C_FIQ_CLR[7:0]	7:0	Clear for FIQ, bit[31:0]. 1: Clear. 0: Not clear.	
04h (2B09h)	REG2B09	7:0	Default : 0x00	Access : R/W
	C_FIQ_CLR[15:8]	7:0	See description of '2B08h'.	
05h (2B0Ah)	REG2B0A	7:0	Default : 0x00	Access : R/W
	C_FIQ_CLR[23:16]	7:0	See description of '2B08h'.	
05h (2B0Bh)	REG2B0B	7:0	Default : 0x00	Access : R/W
	C_FIQ_CLR[31:24]	7:0	See description of '2B08h'.	
06h (2B0Ch)	REG2B0C	7:0	Default : 0x00	Access : RO
	FIQ_RAW_STATUS[7:0]	7:0	FIQ raw status, bit[31:0]. Interrupt source status for FIQ.	

IRQ Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description
06h (2B0Dh)	REG2B0D	7:0	Default : 0x00
	FIQ_RAW_STATUS[15:8]	7:0	See description of '2B0Ch'.
07h (2B0Eh)	REG2B0E	7:0	Default : 0x00
	FIQ_RAW_STATUS[23:16]	7:0	See description of '2B0Ch'.
07h (2B0Fh)	REG2B0F	7:0	Default : 0x00
	FIQ_RAW_STATUS[31:24]	7:0	See description of '2B0Ch'.
08h (2B10h)	REG2B10	7:0	Default : 0x00
	FIQ_FINAL_STATUS[7:0]	7:0	FIQ final status, bit[31:0]. Final interrupt status for FIQ.
08h (2B11h)	REG2B11	7:0	Default : 0x00
	FIQ_FINAL_STATUS[15:8]	7:0	See description of '2B10h'.
09h (2B12h)	REG2B12	7:0	Default : 0x00
	FIQ_FINAL_STATUS[23:16]	7:0	See description of '2B10h'.
09h (2B13h)	REG2B13	7:0	Default : 0x00
	FIQ_FINAL_STATUS[31:24]	7:0	See description of '2B10h'.
0Ah (2B14h)	REG2B14	7:0	Default : 0x00
	C_FIQ_SEL_HL_TRIGGER[7:0]	7:0	High or low trigger select, bit[31:0]. Inverse source polarity for FIQ.
0Ah (2B15h)	REG2B15	7:0	Default : 0x00
	C_FIQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '2B14h'.
0Bh (2B16h)	REG2B16	7:0	Default : 0x00
	C_FIQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '2B14h'.
0Bh (2B17h)	REG2B17	7:0	Default : 0x00
	C_FIQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '2B14h'.
0Ch (2B18h)	REG2B18	7:0	Default : 0xFF
	C_IRQ_MASK[7:0]	7:0	Mask for IRQ, bit[31:0]. 1: Mask. 0: Not mask.
0Ch (2B19h)	REG2B19	7:0	Default : 0xFF
	C_IRQ_MASK[15:8]	7:0	See description of '2B18h'.
0Dh (2B1Ah)	REG2B1A	7:0	Default : 0xFF
	C_IRQ_MASK[23:16]	7:0	See description of '2B18h'.
0Dh	REG2B1B	7:0	Default : 0xFF

IRQ Register (Bank = 2B)				
Index (Absolute)	Mnemonic	Bit	Description	
(2B1Bh)	C_IRQ_MASK[31:24]	7:0	See description of '2B18h'.	
0Eh (2B1Ch)	REG2B1C	7:0	Default : 0x00	Access : R/W
	C_IRQ_FORCE[7:0]	7:0	Force for IRQ, bit[31:0]. 1: Force. 0: Not force.	
0Eh (2B1Dh)	REG2B1D	7:0	Default : 0x00	Access : R/W
	C_IRQ_FORCE[15:8]	7:0	See description of '2B1Ch'.	
0Fh (2B1Eh)	REG2B1E	7:0	Default : 0x00	Access : R/W
	C_IRQ_FORCE[23:16]	7:0	See description of '2B1Ch'.	
0Fh (2B1Fh)	REG2B1F	7:0	Default : 0x00	Access : R/W
	C_IRQ_FORCE[31:24]	7:0	See description of '2B1Ch'.	
10h (2B20h)	REG2B20	7:0	Default : 0x00	Access : R/W
	C_IRQ_SEL_HL_TRIGGER[7:0]	7:0	High or low trigger select, bit[31:0]. Inverse source polarity for IRQ.	
10h (2B21h)	REG2B21	7:0	Default : 0x00	Access : R/W
	C_IRQ_SEL_HL_TRIGGER[15:8]	7:0	See description of '2B20h'.	
11h (2B22h)	REG2B22	7:0	Default : 0x00	Access : R/W
	C_IRQ_SEL_HL_TRIGGER[23:16]	7:0	See description of '2B20h'.	
11h (2B23h)	REG2B23	7:0	Default : 0x00	Access : R/W
	C_IRQ_SEL_HL_TRIGGER[31:24]	7:0	See description of '2B20h'.	
12h (2B24h)	REG2B24	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS[7:0]	7:0	IRQ raw status, bit[31:0]. Interrupt source status for IRQ.	
12h (2B25h)	REG2B25	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS[15:8]	7:0	See description of '2B24h'.	
13h (2B26h)	REG2B26	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS[23:16]	7:0	See description of '2B24h'.	
13h (2B27h)	REG2B27	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS[31:24]	7:0	See description of '2B24h'.	
14h (2B28h)	REG2B28	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS[7:0]	7:0	IRQ final status, bit[31:0]. Final interrupt status for IRQ.	
14h (2B29h)	REG2B29	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS[15:8]	7:0	See description of '2B28h'.	

IRQ Register (Bank = 2B)				
Index (Absolute)	Mnemonic	Bit	Description	
15h (2B2Ah)	REG2B2A	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS[23:16]	7:0	See description of '2B28h'.	
15h (2B2Bh)	REG2B2B	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS[31:24]	7:0	See description of '2B28h'.	
7Eh (2BFCh)	REG2BFC	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	CPU0_2_CPU1_IRQ	0	CPU0 to CPU1 interrupt.	
7Fh (2BFEh)	REG2BFE	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	CPU1_2_CPU0_IRQ	0	CPU1 to CPU0 interrupt.	

ICACHE Register (Bank = 2B)

ICACHE Register (Bank = 2B)				
Index (Absolute)	Mnemonic	Bit	Description	
40h (2B80h)	REG2B80	7:0	Default : 0x00	Access : R/W
	SDRAM_CODE_MAP[7:0]	7:0	SDRAM code map address, unit is 64-Kbyte.	
40h (2B81h)	REG2B81	7:0	Default : 0x00	Access : R/W
	SDRAM_CODE_MAP[15:8]	7:0	See description of '2B80h'.	
41h (2B82h)	REG2B82	7:0	Default : 0x00	Access : RO
	CPU_ADR_L[7:0]	7:0	CPU address[15:0].	
41h (2B83h)	REG2B83	7:0	Default : 0x00	Access : RO
	CPU_ADR_L[15:8]	7:0	See description of '2B82h'.	
42h (2B84h)	REG2B84	7:0	Default : 0x00	Access : RO
	CPU_ADR_H[7:0]	7:0	CPU address[23:0].	
42h (2B85h)	REG2B85	7:0	Default : 0x00	Access : RO
	CPU_ADR_H[15:8]	7:0	See description of '2B84h'.	
43h (2B86h)	REG2B86	7:0	Default : 0x00	Access : RO
	CPU_ROM_DATA0[7:0]	7:0	Icache return data[15:0] to CPU.	
43h (2B87h)	REG2B87	7:0	Default : 0x00	Access : RO
	CPU_ROM_DATA0[15:8]	7:0	See description of '2B86h'.	
44h (2B88h)	REG2B88	7:0	Default : 0x00	Access : RO
	CPU_ROM_DATA1[7:0]	7:0	Icache return data[31:16] to CPU.	
44h (2B89h)	REG2B89	7:0	Default : 0x00	Access : RO
	CPU_ROM_DATA1[15:8]	7:0	See description of '2B88h'.	
45h (2B8Ah)	REG2B8A	7:0	Default : 0x00	Access : RO
	CACHE_MISS_COUNT[7:0]	7:0	Cache Miss counter.	
45h (2B8Bh)	REG2B8B	7:0	Default : 0x00	Access : RO
	CACHE_MISS_COUNT[15:8]	7:0	See description of '2B8Ah'.	
46h (2B8Ch)	REG2B8C	7:0	Default : 0x00	Access : RO
	CACHE_HIT_COUNT[7:0]	7:0	Cache Hit counter.	
46h (2B8Dh)	REG2B8D	7:0	Default : 0x00	Access : RO
	CACHE_HIT_COUNT[15:8]	7:0	See description of '2B8Ch'.	
47h (2B8Eh)	REG2B8E	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	CPU_WAIT	1	CPU wait flag. 1: Wait.	

ICACHE Register (Bank = 2B)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: Hit.	
	CACHE_MISS_FLAG	0	Cache Miss flag. 1: Miss. 0: Hit.	
48h (2B90h)	REG2B90	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	CACHE_FSM[3:0]	3:0	Cache FSM.	
4Ah (2B94h)	REG2B94	7:0	Default : 0x00	Access : R/W
	DUMP[7:0]	7:0	Temp register.	
4Ah (2B95h)	REG2B95	7:0	Default : 0x00	Access : R/W
	DUMP[15:8]	7:0	See description of '2B94h'.	
50h (2BA0h)	REG2BA0	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	CACHE_BY_PASS	0	Cache bypass mode.	

XDMIU Register (Bank = 2B)

XDMIU Register (Bank = 2B)				
Index (Absolute)	Mnemonic	Bit	Description	
60h (2BC0h)	REG2BC0	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SOFTWARE_RST	0	Set 1 to reset HK_MCU XDATA to MIU.	
61h ~ 61h (2BC2h ~ 2BC3h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
62h (2BC4h)	REG2BC4	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	XB_SDR_MAP_EN	2	Set 1 to enable mapping of HK_MCU XDATA to MIU.	
	XD2MIU_WPRI	1	XDATA to MIU write priority.	
	XD2MIU_RPRI	0	XDATA to MIU read priority.	
63h (2BC6h)	REG2BC6	7:0	Default : 0x00	Access : R/W
	XB_ADDR[7:0]	7:0	Low bound address of MCU XDATA mapping to MIU. The unit is 1k bytes. The XDATA address is hit if (XB_ADDR[15:8] > XDATA_ADDR[15:10] >= XB_ADDR[7:0]).	
63h (2BC7h)	REG2BC7	7:0	Default : 0x00	Access : R/W
	XB_ADDR[15:8]	7:0	See description of '2BC6h'.	
64h (2BC8h)	REG2BC8	7:0	Default : 0x00	Access : R/W
	SDR_XD_MAP[7:0]	7:0	Low byte address to access XDATA from MIU. The granularity is 64k bytes. The actual address[23:0] to MIU would be {SDR_XD_MAP[10:8], SDR_XD_MAP[7:0], XDATA_ADDR[15:3]}, where XDATA_ADDR[15:0] are MCU XDATA addresses of 64k bytes.	
64h (2BC9h)	REG2BC9	7:0	Default : 0x00	Access : R/W
	SDR_XD_MAP[15:8]	7:0	See description of '2BC8h'.	
65h (2BCAh)	REG2BCA	7:0	Default : 0x00	Access : R/W
	XB_ADDR_1[7:0]	7:0	Low bound address of MCU XDATA mapping to MIU. The unit is 1k bytes. The XDATA address is hit if (XB_ADDR_1[15:8] > XDATA_ADDR[15:10] >= XB_ADDR_1[7:0]).	
65h (2BCBh)	REG2BCB	7:0	Default : 0x00	Access : R/W
	XB_ADDR_1[15:8]	7:0	See description of '2BCAh'.	

XDMIU Register (Bank = 2B)

Index (Absolute)	Mnemonic	Bit	Description
66h (2BCCh)	REG2BCC	7:0	Default : 0x00 Access : R/W
	SDR_XD_MAP_1_0[7:0]	7:0	Low byte address to access XDATA from MIU. The granularity is 1k bytes. The actual address[23:0] to MIU would be {SDR_XD_MAP_1_1[0], SDR_XD_MAP_1_0[15:8], SDR_XD_MAP_1_0[7:0], XDATA_ADDR[9:3]}, where XDATA_ADDR[15:0] are MCU XDATA addresses of 64k bytes.
66h (2BCDh)	REG2BCD	7:0	Default : 0x00 Access : R/W
	SDR_XD_MAP_1_0[15:8]	7:0	See description of '2BCCh'.
67h (2BCEh)	REG2BCE	7:0	Default : 0x00 Access : R/W
	SDR_XD_MAP_1_1[7:0]	7:0	Low byte address to access XDATA from MIU. The granularity is 1k bytes. The actual address[23:0] to MIU would be {SDR_XD_MAP_1_1[0], SDR_XD_MAP_1_0[15:8], SDR_XD_MAP_1_0[7:0], XDATA_ADDR[9:3]}, where XDATA_ADDR[15:0] are MCU XDATA addresses of 64k bytes.
67h (2BCFh)	REG2BCF	7:0	Default : 0x00 Access : R/W
	SDR_XD_MAP_1_1[15:8]	7:0	See description of '2BCEh'.

VIVALDI Register (Bank = 2C)

VIVALDI Register (Bank = 2C)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2C00h)	REG2C00	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	CLKGEN_RESET	1	0x2C00. Audio engine clkgen reset. 0 = normal. 1 = reset.	
	SOFTWARE_RESET	0	0x2C00. Audio engine software reset. 0 = normal. 1 = reset. Note: This command can't reset register value.	
01h (2C02h)	REG2C02	7:0	Default : 0x00	Access : R/W
	INPUT_CFG[7:0]	7:0	0x2C02. [14] REG_AUTO_CLEAR_PC_PD_BAR. 0: Enable. 1: Disable. [12] 768FS_PLL_ENABLE. Enable 768 Fs audio sample frequency synthesizer module. 0: Disable. 1: Enable. [11] Reserved. [10] DVB_PLL_LOCK_CURRENT_FREQ. Force lock current DVB SYNC synthesizer freq. 0: Disable. 1: Enable. [9] DVB_FREQ_GAIN. Audio DVB SYNC synthesizer Cs gain selection. 0: Normal. 1: Enhancement (smaller Cs). [8] DVB_PHASE_GAIN. Audio DVB SYNC synthesizer Cp gain selection. 0: Normal. 1: Enhancement (smaller Cp). [7] EN_CARD_READER_FIX_SYNTH. Enable card reader audio sample frequency fixed synthesizer module. 0: Disable. 1: Enable (256 Fs).	

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>[6] ENABLE_AUDIO_DVB1_FIX_SYNTH. Enable DVB audio sample frequency fixed synthesizer module. 0: Disable. 1: Enable (256 Fs).</p> <p>[5] REG_EN_ADC_SYNTH_1. [4] reserved. [3] EN_I2S_SYNTH. Enable I2S audio sample frequency synthesizer module. 0: Disable. 1: Enable (256 Fs).</p> <p>[2] EN_SIF_SYNTH. Enable SIF audio sample frequency synthesizer module. 0: Disable. 1: Enable (256 Fs). [1] reserved. [0] EN_ADC_SYNTH. Enable ADC audio sample frequency synthesizer module. 0: Disable. 1: Enable (256 Fs).</p>
01h (2C03h)	REG2C03	7:0	Default : 0x00
	INPUT_CFG[15:8]	7:0	See description of '2C02h'.
02h (2C04h)	REG2C04	7:0	Default : 0x00
	STATUS_DVB_FREQ[7:0]	7:0	<p>0x2C04. [15] DVB_PLL_NO_SIGNAL. Audio DVB SYNC synthesizer input signal detect. 0: Signal detected. 1: No signal input. [14:0] DVB_PLL_FREQ. Audio DVB SYNC synthesizer frequency value.</p>
02h (2C05h)	REG2C05	7:0	Default : 0x00
	STATUS_DVB_FREQ[15:8]	7:0	See description of '2C04h'.
03h (2C06h)	REG2C06	7:0	Default : 0x00
	STATUS_I2S_FREQ[7:0]	7:0	<p>0x2C06. [15] I2S_NO_SIGNAL. Audio I2S Clock Data Recovery input signal detect. 0: Signal detected.</p>

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			1: No signal input. [14:0] I2S_FREQ. Audio I2S Clock Data Recovery frequency value.
03h (2C07h)	REG2C07	7:0	Default : 0x00 Access : RO
	STATUS_I2S_FREQ[15:8]	7:0	See description of '2C06h'.
04h (2C08h)	REG2C08	7:0	Default : 0x00 Access : RO
	STATUS_SIF_FREQ[7:0]	7:0	0x2C08. [15] SIF_NO_SIGNAL. Audio SIF Clock Data Recovery input signal detect. 0: Signal detected. 1: No signal input. [14:0] SIF_FREQ. Audio SIF Clock Data Recovery frequency value.
04h (2C09h)	REG2C09	7:0	Default : 0x00 Access : RO
	STATUS_SIF_FREQ[15:8]	7:0	See description of '2C08h'.
05h ~ 05h (2C0Ah ~ 2C0Bh)	-	7:0	Default : - Access : -
	-	-	Reserved.
06h (2C0Ch)	REG2C0C	7:0	Default : 0x00 Access : RO
	STATUS_INPUT[7:0]	7:0	0x2C0C. [7:6] Status of audio stream from HDMI input interface. 00 = PCM audio. 01 = Non-PCM (Compressed) audio. 10 = One Bit Audio. 11 = N/A. [5] Status of HDMI audio decoder. (pre-setting error event). 0 = normal. 1 = mute. [4] Decoded AVMUTE bit from HDMI received General Control packet. 0 = clear AVMUTE. 1 = set AVMUTE.
07h ~ 08h (2C0Eh ~ 2C10h)	-	7:0	Default : - Access : -
	-	-	Reserved.
09h (2C12h)	-	7:0	Default : - Access : -
	-	-	Reserved.
0Ah	-	7:0	Default : - Access : -

VIVALDI Register (Bank = 2C)				
Index (Absolute)	Mnemonic	Bit	Description	
(2C14h)	-	-	Reserved.	
0Bh (2C16h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Ch (2C18h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Dh ~ 0Eh (2C1Ah ~ 2C1Dh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
10h (2C20h)	REG2C20	7:0	Default : 0xED	Access : R/W
	AUPLL_RST	7	HDMI audio PLL reset. 0 = no action. 1 = reset.	
	AUPLL_ICTRL[2:0]	6:4	Audio HDMI CODEC PLL charge pump current control.	
	AUPLL_PDN	3	DMI audio PLL power down. 0 = No action. 1 = Power down.	
	AUPLL_RCTRL[2:0]	2:0	Audio HDMI CODEC PLL loop filter resistor control. R = 15 + 5 * RCTRL (k ohm).	
11h (2C22h)	REG2C22	7:0	Default : 0x00	Access : R/W
	AUPLL_TEST_IN[7:0]	7:0	HDMI AUPLL test in.	
11h (2C23h)	REG2C23	7:0	Default : 0x00	Access : R/W
	AUPLL_TEST_IN[15:8]	7:0	See description of '2C22h'.	
12h (2C24h)	REG2C24	7:0	Default : 0x0F	Access : R/W
	AUPLL_VCO_OFFSET	7	Enable VCO free running. 0 = enable. 1 = disable.	
	AUPLL_INTDIVIDE	6	Enable intercept audio driver in HDMI PLL synthesizer. 0 = normal. 1 = enable.	
	EN_CLKPIX2X	5	Enable video clock 2x output clock. 0 = Disable. 1 = Enable.	
	AUPLL_LCKDCT	4	Enable TMDS PLL lock detection. 0 = Disable. 1 = Enable.	
	AUPLL_PORST	3	HDMI audio PLL reset.	

VIVALDI Register (Bank = 2C)				
Index (Absolute)	Mnemonic	Bit	Description	
			0 = normal. 1 = reset (all analog front-end & dividers).	
	AUPLL_RESETP	2	HDMI audio PLL post clock divider reset.(KP). 0 = normal. 1 = Reset.	
	AUPLL_RESETF	1	HDMI audio PLL feedback clock divider reset. (FBDIV & KM). 0 = normal. 1 = Reset.	
	-	0	Reserved.	
13h (2C26h)	REG2C26	7:0	Default : 0x00	Access : R/W
	AUPLL_KP[3:0]	7:4	HDMI PLL Post divider ratio (KP) for new mode. 0000 = / 1. 0001 = / 2. 0010 = / 4. ... 1001 = / 512. 1010 = / 1024. 1011 = / 1024. ... 1111 = / 1024.	
	AUPLL_KM[3:0]	3:0	HDMI PLL KM divider ratio for new mode. 0000 = / 1. 0001 = / 2. 0010 = / 4. ... 0111 = / 128. 1000 = / 256. 1001 = / 256. ... 1111 = / 256.	
13h (2C27h)	REG2C27	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	AUPLL_KN[1:0]	1:0	HDMI PLL KN divider ratio for new mode. 00 = /1. 01 = /2. 10 = /4. 11 = /4.	

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
14h (2C28h)	REG2C28	7:0	Default : 0x10 Access : R/W
	AUPLL_DDIV[3:0]	7:4	HDMI PLL input overwrite divider value from noise-shape quantizer for new mode. 0000 = N.A. (/16). 0001 = N.A. (/17). 0010 = /2. 0011 = /3. ... 1111 = /15.
	AUPLL_FBDIV[3:0]	3:0	HDMI PLL feedback overwrite divider value from noise-shape quantizer for new mode. 0000 = N.A. (/16). 0001 = N.A. (/17). 0010 = /2. 0011 = /3. ... 1111 = /15.
15h (2C2Ah)	REG2C2A	7:0	Default : 0x00 Access : R/W
	EN_CTS_N_SYNTH	7	Audio HDMI CTS-N synthesizer control. 0 = Idle. 1 = Enable. (Never disable CTS-N synthesizer after it is enabled).
	-	6	Reserved.
	SYNTH_PLL_LOCK_SEL	5	Audio HDMI CTS-N synthesizer lock function select. 0: Manual. 1: Auto.
	SYNTH_256FS_EXPANDER	4	S/PDIF 256 fs synthesizer clock pulse expander. 0 = normal (1T width). 1 = expander (2T width).
	SYNTH_PLL_LOCK_FREQ	3	Audio HDMI CTS-N synthesizer lock current frequency. 0 = normal. 1 = lock.
	SYNTH_FREQ_GAIN	2	Audio HDMI CTS-N synthesizer Cs gain selection. 0 = normal.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			1 = enhancement (smaller Cs).
	SYNTH_PH_GAIN	1	Audio HDMI CTS-N synthesizer Cp gain selection. 0 = normal. 1 = enhancement (smaller Cp).
	SYNTH_SEL_CTS_REF	0	Audio HDMI CTS-N synthesizer CTS REF selection. 0 = select CTS FIFO out valid. 1 = select CTS[19:0].
15h (2C2Bh)	REG2C2B	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	RST_CTSN_SYNTH	4	Reset HDMI CTS_N synthesizer. 0: Disable. 1: Enable.
	-	3	Reserved.
	SYNTH_NO_INPUT_LOCK_EN	2	Enable CTS N synthesizer to lock no input control signal output. 0: Unlock. 1: Lock.
	SYNTH_NO_INPUT_SEL	1	CTS N synthesizer select lock or unlock no input signal to control output 256fs. 0: Select unlock no input signal. 1: Select lock no input signal.
	CLR_SYNTH_LOCK	0	Clear synthesizer_s lock state. 0: Normal. 1: Clear.
16h (2C2Ch)	REG2C2C	7:0	Default : 0x00 Access : RO
	CTS_N_SYNTH_FREQ[7:0]	7:0	Audio HDMI CTS-N synthesizer Frequency value.
16h (2C2Dh)	REG2C2D	7:0	Default : 0x00 Access : RO
	DVI_NO_INPUT	7	Audio HDMI CTS-N synthesizer input signal detect. 0 = signal detected. 1 = no input signal.
	CTS_N_SYNTH_FREQ[14:8]	6:0	See description of '2C2Ch'.
17h (2C2Eh)	REG2C2E	7:0	Default : 0x00 Access : RO
	-	7:2	Reserved.
	AUPLL_HIGH_FLAG	1	HDMI AUPLL VCO too high flag.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
	AUPLL_LOCK	0	HDMI AUPLL lock indication.
18h (2C30h)	REG2C30	7:0	Default : 0x00 Access : R/W
	HDMI_DCLK_INV	7	Invert HDMI audio PLL DCLK clock. 0: Normal. 1: Invert.
	HDMI_DCLK_EN	6	Enable HDMI audio PLL DCLK clock. 0: Disable. 1: Enable.
	HDMI_FBCLK_INV	5	Invert HDMI audio PLL FBCLK clock. 0: Normal. 1: Invert.
	HDMI_FBCLK_EN	4	Enable HDMI audio PLL FBCLK clock. 0: Disable. 1: Enable.
	SYNTH_PLL_LOCK_EN[3:0]	3:0	Enable the following events to freeze audio HDMI CTS-N synthesizer. [0]: CTS-N big change. [1]: Video clock frequency big change. [3:2]: Reserved.
18h (2C31h)	REG2C31	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	AUPLL_ENFBDIV1	1	Feedback divider bypass. 0: Fbdiv!=1. 1: Fbdiv=1.
	AUPLL_ENINDIV1	0	Input divider bypass. 0: Ddiv!=1. 1: Ddiv=1.
20h (2C40h)	REG2C40	7:0	Default : 0x00 Access : RO
	STATUS_HDMI_PC[7:0]	7:0	0x2C40. HDMI input Non-PCM preamble Pc.
20h (2C41h)	REG2C41	7:0	Default : 0x00 Access : RO
	STATUS_HDMI_PC[15:8]	7:0	See description of '2C40h'.
21h (2C42h)	REG2C42	7:0	Default : 0x00 Access : RO
	STATUS_HDMI_PD[7:0]	7:0	0x2C42. HDMI input Non-PCM preamble Pd.
21h	REG2C43	7:0	Default : 0x00 Access : RO

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
(2C43h)	STATUS_HDMI_PD[15:8]	7:0	See description of '2C42h'.
22h (2C44h)	REG2C44	7:0	Default : 0x10 Access : R/W
	HDMI_MATRIX0[7:0]	7:0	<p>0x2C44.</p> <p>[15] Reserved.</p> <p>[14:12] HDMI_CH4_MATRIX.</p> <p>HDMI Audio channel 4 matrix.</p> <p>000: Mapped from channel 1.</p> <p>001: Mapped from channel 2.</p> <p>010: Mapped from channel 3.</p> <p>011: Mapped from channel 4.</p> <p>100: Mapped from channel 5.</p> <p>101: Mapped from channel 6.</p> <p>110: Mapped from channel 7.</p> <p>111: Mapped from channel 8.</p> <p>[11] Reserved.</p> <p>[10:8] HDMI_CH3_MATRIX.</p> <p>HDMI Audio channel 3 matrix.</p> <p>000: Mapped from channel 1.</p> <p>001: Mapped from channel 2.</p> <p>010: Mapped from channel 3.</p> <p>011: Mapped from channel 4.</p> <p>100: Mapped from channel 5.</p> <p>101: Mapped from channel 6.</p> <p>110: Mapped from channel 7.</p> <p>111: Mapped from channel 8.</p> <p>[7] Reserved.</p> <p>[6:4] HDMI_CH2_MATRIX.</p> <p>HDMI Audio channel 2 matrix.</p> <p>000: Mapped from channel 1.</p> <p>001: Mapped from channel 2.</p> <p>010: Mapped from channel 3.</p> <p>011: Mapped from channel 4.</p> <p>100: Mapped from channel 5.</p> <p>101: Mapped from channel 6.</p> <p>110: Mapped from channel 7.</p> <p>111: Mapped from channel 8.</p> <p>[3] Reserved.</p> <p>[2:0] HDMI_CH1_MATRIX.</p> <p>HDMI Audio channel 1 matrix.</p> <p>000: Mapped from channel 1.</p>

VIVALDI Register (Bank = 2C)			
Index (Absolute)	Mnemonic	Bit	Description
			001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8.
22h (2C45h)	REG2C45	7:0	Default : 0x32
	HDMI_MATRIX0[15:8]	7:0	Access : R/W See description of '2C44h'.
23h (2C46h)	REG2C46	7:0	Default : 0x54
	HDMI_MATRIX1[7:0]	7:0	Access : R/W 0x2C46. [15] Reserved. [14:12] HDMI_CH8_MATRIX. HDMI Audio channel 8 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8. [11] Reserved. [10:8] HDMI_CH7_MATRIX. HDMI Audio channel 7 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8. [7] Reserved. [6:4] HDMI_CH6_MATRIX. HDMI Audio channel 6 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8. [3] Reserved. [2:0] HDMI_CH5_MATRIX. HDMI Audio channel 5 matrix. 000: Mapped from channel 1. 001: Mapped from channel 2. 010: Mapped from channel 3. 011: Mapped from channel 4. 100: Mapped from channel 5. 101: Mapped from channel 6. 110: Mapped from channel 7. 111: Mapped from channel 8.
23h (2C47h)	REG2C47	7:0	Default : 0x76
	HDMI_MATRIX1[15:8]	7:0	See description of '2C46h'.
24h (2C48h)	REG2C48	7:0	Default : 0x00
	DOWN_SAMPLE[7:0]	7:0	0x2C48. [7:6] DOWN_SAMPLE_DVB1. Input DVB down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved. [5:4] DOWN_SAMPLE_I2S. Input I2S down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved. [3:2] DOWN_SAMPLE_SPDIF. Input SPDIF down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved. [1:0] DOWN_SAMPLE_HDMI.

VIVALDI Register (Bank = 2C)				
Index (Absolute)	Mnemonic	Bit	Description	
			Input HDMI down sampling ratio. 00: Normal (from 1x to 1x). 01: Down sample from 2x to 1x. 10: Down sample from 4x to 1x. 11: Reserved.	
24h (2C49h)	REG2C49	7:0	Default : 0x00	Access : R/W
	DOWN_SAMPLE[15:8]	7:0	See description of '2C48h'.	
28h (2C50h)	REG2C50	7:0	Default : 0x0F	Access : R/W
	DAC_CMP0[7:0]	7:0	0x2C50. Coefficient-0 of the DAC_s compensation filter.	
28h (2C51h)	REG2C51	7:0	Default : 0x00	Access : R/W
	DAC_CMP0[15:8]	7:0	See description of '2C50h'.	
29h (2C52h)	REG2C52	7:0	Default : 0xA4	Access : R/W
	DAC_CMP1[7:0]	7:0	0x2C52. Coefficient-1 of the DAC_s compensation filter.	
29h (2C53h)	REG2C53	7:0	Default : 0xFF	Access : R/W
	DAC_CMP1[15:8]	7:0	See description of '2C52h'.	
2Ah (2C54h)	REG2C54	7:0	Default : 0x40	Access : R/W
	DAC_CMP2[7:0]	7:0	0x2C54. Coefficient-2 of the DAC_s compensation filter.	
2Ah (2C55h)	REG2C55	7:0	Default : 0x7F	Access : R/W
	DAC_CMP2[15:8]	7:0	See description of '2C54h'.	
2Bh (2C56h)	REG2C56	7:0	Default : 0x22	Access : R/W
	ADC_CMP0[7:0]	7:0	0x2C56. Coefficient-0 of the ADC_s compensation filter.	
2Bh (2C57h)	REG2C57	7:0	Default : 0x00	Access : R/W
	ADC_CMP0[15:8]	7:0	See description of '2C56h'.	
2Ch (2C58h)	REG2C58	7:0	Default : 0xF9	Access : R/W
	ADC_CMP1[7:0]	7:0	0x2C58. Coefficient-1 of the ADC_s compensation filter.	
2Ch (2C59h)	REG2C59	7:0	Default : 0xFE	Access : R/W
	ADC_CMP1[15:8]	7:0	See description of '2C58h'.	
2Dh (2C5Ah)	REG2C5A	7:0	Default : 0x61	Access : R/W
	ADC_CMP2[7:0]	7:0	0x2C5A. Coefficient-2 of the ADC_s compensation filter.	

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
2Dh (2C5Bh)	REG2C5B	7:0	Default : 0x44 Access : R/W
	ADC_CMP2[15:8]	7:0	See description of '2C5Ah'.
2Eh (2C5Ch)	REG2C5C	7:0	Default : 0x34 Access : R/W
	ADC_GAIN[7:0]	7:0	0x2C5C. Pre-scale of the ADC_s decimation filter (Format: unsigned 2.14).
2Eh (2C5Dh)	REG2C5D	7:0	Default : 0x73 Access : R/W
	ADC_GAIN[15:8]	7:0	See description of '2C5Ch'.
2Fh ~ 2Fh (2C5Eh ~ 2C5Fh)	-	7:0	Default : - Access : -
	-	-	Reserved.
30h (2C60h)	REG2C60	7:0	Default : 0x00 Access : R/W
	DECODER1_CFG[7:0]	7:0	0x2C60. [2:0] SEL_DECODER1. DSP decoder1 clock selection (for DVB1). 000: DVB1. 001: DVB1. 010: SPDIF. 011: SPDIFx1. 100: HDMI. 101: HDMIx1. 110: Card Reader. 111: SIF.
31h (2C62h)	REG2C62	7:0	Default : 0x00 Access : R/W
	DECODER2_CFG[7:0]	7:0	0x2C62. [7:4] Reserved. [3] Bypass mode for AUDIO_SPDIF_PACKER. [2:0] SEL_DECODER2. DSP decoder2 clock selection (for DVB2). 000: DVB2. 001: DVB2. 010: SPDIF. 011: SPDIFx1. 100: HDMI. 101: HDMIx1. 110: Card Reader. 111: SIF.
32h	REG2C64	7:0	Default : 0x00 Access : R/W

VIVALDI Register (Bank = 2C)				
Index (Absolute)	Mnemonic	Bit	Description	
(2C64h)	CH1_CFG[7:0]	7:0	0x2C64. [7] Audio Output channel 1 enable setting. 0 = idle (power saving). 1 = enable. [6] Audio Output channel 1 source clock selection. 0 = normal. 1 = synchronous to codec PLL. (while codec PLL ref clock is the same as this channel). [5] Audio Output channel 1 Sampling Rate Converter setting. 0 = normal. 1 = SRC mode. [4] Audio Output channel 1 over sampling rate setting. 0 = 128 fs. 1 = 256 fs. [3] Audio Output channel 1 sigma delta modulator enable setting. 0 = idle (power saving). 1 = enable. [2:0] Audio Output channel 1 source selection. 000 = from DSP decoder1 output. 001 = from DSP decoder2 output. 010 = from Audio ADC. 011 = from SINE GEN. 100 = reserved. 101 = from HDMI (sample stream 1 & 2). 110 = Reserved.	
33h (2C66h)	REG2C66	7:0	Default : 0x00	Access : R/W
	CH2_CFG[7:0]	7:0	0x2C66. [7] Audio Output channel 2 enable setting. 0 = idle (power saving). 1 = enable. [6] Audio Output channel 2 source clock selection. 0 = normal. 1 = synchronous to codec PLL. (while codec PLL ref clock is the same as this channel). [5] Audio Output channel 2 Sampling Rate Converter setting. 0 = normal. 1 = SRC mode. [4] Audio Output channel 2 over sampling rate setting. 0 = 128 fs.	

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>1 = 256 fs.</p> <p>[3] Audio Output channel 2 sigma delta modulator enable setting.</p> <p>0 = idle (power saving).</p> <p>1 = enable.</p> <p>[2:0] Audio Output channel 1 source selection.</p> <p>000 = from DSP decoder1 output.</p> <p>001 = from DSP decoder2 output.</p> <p>010 = from Audio ADC.</p> <p>011 = from SINE GEN.</p> <p>100 = reserved.</p> <p>101 = from HDMI (sample stream 1 & 2).</p> <p>110 = Reserved.</p>
34h (2C68h)	REG2C68	7:0	Default : 0x00 Access : R/W
	CH3_CFG[7:0]	7:0	<p>0x2C68.</p> <p>[7] Audio Output channel 3 enable setting.</p> <p>0 = idle (power saving).</p> <p>1 = enable.</p> <p>[6] Audio Output channel 3 source clock selection.</p> <p>0 = normal.</p> <p>1 = synchronous to codec PLL.</p> <p>(while codec PLL ref clock is the same as this channel).</p> <p>[5] Audio Output channel 3 Sampling Rate Converter setting.</p> <p>0 = normal.</p> <p>1 = SRC mode.</p> <p>[4] Audio Output channel 3 over sampling rate setting.</p> <p>0 = 128 fs.</p> <p>1 = 256 fs.</p> <p>[3] Audio Output channel 3 sigma delta modulator enable setting.</p> <p>0 = idle (power saving).</p> <p>1 = enable.</p> <p>[2:0] Audio Output channel 1 source selection.</p> <p>000 = from DSP decoder1 output.</p> <p>001 = from DSP decoder2 output.</p> <p>010 = from Audio ADC.</p> <p>011 = from SINE GEN.</p> <p>100 = reserved.</p> <p>101 = from HDMI (sample stream 1 & 2).</p> <p>110 = Reserved.</p>

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
35h (2C6Ah)	REG2C6A	7:0	Default : 0x00 Access : R/W
	CH4_CFG[7:0]	7:0	0x2C6A. [7] Audio Output channel 4 enable setting. 0 = idle (power saving). 1 = enable. [6] Audio Output channel 4 source clock selection. 0 = normal. 1 = synchronous to codec PLL. (while codec PLL ref clock is the same as this channel). [5] Audio Output channel 4 Sampling Rate Converter setting. 0 = normal. 1 = SRC mode. [4] Audio Output channel 4 over sampling rate setting. 0 = 128 fs. 1 = 256 fs. [3] Audio Output channel 4 sigma delta modulator enable setting. 0 = idle (power saving). 1 = enable. [2:0] Audio Output channel 1 source selection. 000 = from DSP decoder1 output. 001 = from DSP decoder2 output. 010 = from Audio ADC. 011 = from SINE GEN. 100 = reserved. 101 = from HDMI (sample stream 1 & 2). 110 = Reserved.
36h (2C6Ch)	REG2C6C	7:0	Default : 0x00 Access : R/W
	INPUT_REGEN_CFG[7:0]	7:0	0x2C6C. [13] Timing_gen genshot selection. 0 = bypass genshot (recommend). 1 = using genshot. [12:9] Reserved. [8] Fix SPDIF, I2S & M-Link Extra PCM SRC mode. 0 = disable. 1 = enable (recommend). [7] HDMI clock auto re-generator function enable. 0 = disable. 1 = enable. [6] SIF clock auto re-generator function enable.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0 = disable. 1 = enable. [5] I2S clock auto re-generator function enable. 0 = disable. 1 = enable. [4] S/PDIF clock auto re-generator function enable. 0 = disable. 1 = enable. [3] DVB clock auto re-generator function enable. 0 = disable. 1 = enable. [2] SRC mode for SPDIF. 0 = normal. 1 = enable. [1] SRC mode for 1st I2S encoder. 0 = normal. 1 = enable. [0] Reserved.
36h (2C6Dh)	REG2C6D	7:0	Default : 0x00
	INPUT_REGEN_CFG[15:8]	7:0	See description of '2C6Ch'.
38h (2C70h)	REG2C70	7:0	Default : 0x00
	SPARE_R0[7:0]	7:0	0x2C70. [10]: BOND_AUDIO_0: (Dolby). [11]: BOND_AUDIO_1: (SRS, BBE, DTS &). [12]: BOND_AUDIO_2: (DivX). [13]: BOND_AUDIO_3: (Reserved).
38h (2C71h)	REG2C71	7:0	Default : 0x00
	SPARE_R0[15:8]	7:0	See description of '2C70h'.
39h (2C72h)	REG2C72	7:0	Default : 0x00
	SPARE_R1[7:0]	7:0	0x2C72.
39h (2C73h)	REG2C73	7:0	Default : 0x00
	SPARE_R1[15:8]	7:0	See description of '2C72h'.
3Ah (2C74h)	REG2C74	7:0	Default : 0x00
	SPARE_RW0[7:0]	7:0	0x2C74. [15]: REG_GPA_SRC_SYNTH_UPD. After write N.F then toggle this bit for update N.F. [13]: PCM_1R_ENABLE. 1: Enable.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0: Disable. [12]: PCM_1L_ENABLE. 1: Enable. 0: Disable. [11:8]: PCM_1R_FREQ_SEL. 4'h0: 250Hz. 4'h1: 500Hz. 4'h2: 1KHz. 4'h3: 1.5KHz. 4'h4: 2KHz. 4'h5: 3KHz. 4'h6: 4KHz. 4'h7: 6KHz. 4'h8: 8KHz. 4'h9: 12KHz. other: 16KHz. [7:4]: L&R both gain control. Gain = -6dB*[7:4].. [3:0]: PCM_1L_FREQ_SEL. Reference [11:8].
3Ah (2C75h)	REG2C75	7:0	Default : 0x00
	SPARE_RW0[15:8]	7:0	Access : R/W See description of '2C74h'.
3Bh (2C76h)	REG2C76	7:0	Default : 0x00
	SPARE_RW1[7:0]	7:0	Access : R/W 0x2C76. [13]: REG_INV_CLK_AUPLL_INV_FORDIV. [12]: REG_INV_CLK_AUPLL_FORDIV. [11]: REG_INV_CLK.CG_AUPLL_DCLK. [10]: REG_INV_CLK.CG_AUPLL_FBCLK. [6]: REG_ENABLE_CLK_AUPLL_INV_FORDIV. [5]: REG_ENABLE_CLK_AUPLL_FORDIV. [4]: REG_ENABLE_CLK.CG_AUPLL_DCLK. [3]: REG_ENABLE_CLK.CG_AUPLL_FBCLK.
3Bh (2C77h)	REG2C77	7:0	Default : 0x00
	SPARE_RW1[15:8]	7:0	Access : R/W See description of '2C76h'.
3Ch (2C78h)	REG2C78	7:0	Default : 0x00
	SPARE_RW2[7:0]	7:0	Access : R/W 0x2C78.
3Ch (2C79h)	REG2C79	7:0	Default : 0x00
	SPARE_RW2[15:8]	7:0	Access : R/W See description of '2C78h'.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
3Dh (2C7Ah)	REG2C7A	7:0	Default : 0x00
	SPARE_RW3[7:0]	7:0	0x2C7A.
3Dh (2C7Bh)	REG2C7B	7:0	Default : 0x00
	SPARE_RW3[15:8]	7:0	See description of '2C7Ah'.
3Eh (2C7Ch)	REG2C7C	7:0	Default : 0x00
	SPARE_RW4[7:0]	7:0	0x2C7C. [15:0]: GPA_SRC_256_SYNTH_M[15:0]: num.
3Eh (2C7Dh)	REG2C7D	7:0	Default : 0x00
	SPARE_RW4[15:8]	7:0	See description of '2C7Ch'.
3Fh (2C7Eh)	REG2C7E	7:0	Default : 0x00
	SPARE_RW5[7:0]	7:0	0x2C7E. [15:0]: GPA_SRC_256_SYNTH_N[15:0]. den: Synth_out = synth_in * num/den /2. (216000*2048/18000)/512 = 48KHz. (216000*2048/19592)/512 = 44.0996325030625KHz. (216000*2048/27000)/512 = 32KHz. (216000*1024/54000)/512 = 8KHz.
3Fh (2C7Fh)	REG2C7F	7:0	Default : 0x00
	SPARE_RW5[15:8]	7:0	See description of '2C7Eh'.
40h (2C80h)	REG2C80	7:0	Default : 0x00
	SPDIF_OUT_CS0[7:0]	7:0	0x2C80. S/PDIF Output Channel Status [0:7] (refer to CR04.4).
41h (2C82h)	REG2C82	7:0	Default : 0x00
	SPDIF_OUT_CS1[7:0]	7:0	0x2C82. S/PDIF Output Channel Status [8:15] (refer to CR04.4).
42h (2C84h)	REG2C84	7:0	Default : 0x00
	SPDIF_OUT_CS2[7:0]	7:0	0x2C84. S/PDIF Output Channel Status [16:23] (refer to CR04.4).
43h (2C86h)	REG2C86	7:0	Default : 0x00
	SPDIF_OUT_CS3[7:0]	7:0	0x2C86. S/PDIF Output Channel Status [24:31] (refer to CR04.4).
44h (2C88h)	REG2C88	7:0	Default : 0x00
	SPDIF_OUT_CS4[7:0]	7:0	0x2C88. S/PDIF Output Channel Status [32:39] (refer to CR04.4).
45h	REG2C8A	7:0	Default : 0x00

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
(2C8Ah)	SPDIF_OUT_CFG[7:0]	7:0	<p>0x2C8A.</p> <p>[15] Insert Validity Bit. 0 = disable. 1 = enable.</p> <p>[14] SPDIF source selection. 0 = Data after Sound Effect. 1 = Data before Sound Effect.</p> <p>[13:11] Reserved.</p> <p>[10] Counter reset value selection. 0 = counter value set 0. 1 = counter value set 64 (recommend).</p> <p>[9] Automatically synchronize input and output timing of the S/PDIF encoders. Set to 0 in SRC mode. 0 = disable. 1 = enable (recommend).</p> <p>[8] Automatically synchronize input and output timing of the S/PDIF encoders. Set to 0 in SRC mode. 0 = disable. 1 = enable.</p> <p>[7] Audio Output channel S/PDIF enable setting. 0 = idle (power saving). 1 = enable.</p> <p>[6] Reset S/PDIF output modules. This bit shall be toggled after data or clock is changed for S/PDIF output modules. 0 = normal. 1 = reset (synchronous input Fs and output Fs).</p> <p>[5] Audio Output channel S/PDIF Sampling Rate Converter setting. 0 = normal. 1 = SRC mode.</p> <p>[4] Enable channel status insertion for output S/PDIF module. 0 = disable (refer from S/PDIF / HDMI input channel status). 1 = enable (refer from SPDIF_OUT_CS0..4).</p> <p>[3] Audio output channel 1/2/3/4 test source selection. 0 = normal (16 bits). 1 = from DSP output 24 bit interface (only without SRC). (only for SEL_SPDIF_CH[1:0]).</p>

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			[2:0] Audio output channel S/PDIF source selection (16/24 bits). 000 = from audio output channel 1. 001 = from audio output channel 2. 010 = from audio output channel 3. 011 = from audio output channel 4. 100 = HDMI bypass. 101 = DVB non-PCM output. 110 = N.A. 111 = N.A.
45h (2C8Bh)	REG2C8B	7:0	Default : 0x00
	SPDIF_OUT_CFG[15:8]	7:0	See description of '2C8Ah'.
46h (2C8Ch)	REG2C8C	7:0	Default : 0x00
	I2S_OUT1_CFG[7:0]	7:0	0x2C8C. [15] Audio Output channel I2S enable setting. 0 = idle (power saving). 1 = enable. [14] Reset I2S output modules. This bit shall be toggled after data or clock is changed for I2S output modules. 0 = normal. 1 = reset (synchronous input Fs and output Fs). [13] Automatically synchronize input and output timing of the I2S encoders. Set to 0 in SRC mode. 0 = disable. 1 = enable (recommend). [12] Counter reset value selection. 0 = counter value set 0. 1 = counter value set 16 (recommend). [11] Audio output channel 1/2/3/4 test source selection. 0 = normal (16 bits). 1 = from DSP output 24 bit interface (only without SRC). (only for SEL_I2S_CH[1:0]). [10] Audio output channel I2S source selection (24 bits). 0 = normal (following SEL_I2S_CH[1:0]). 1 = from HDMI audio link. [9:8] Audio output channel I2S source selection (16/24 bits). 00 = from audio output channel 1.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>01 = from audio output channel 2. 10 = from audio output channel 3. 11 = from audio output channel 4. [7] Automatically synchronize input and output timing of the I2S encoders. Set to 0 in SRC mode. 0 = disable. 1 = enable. [6:4] Clock frequency select for AUMCKO output pin. (I2S MCLK). 000 = synthesizer 64 Fs. 001 = synthesizer 128 Fs. 010 = synthesizer 256 Fs. 011 = test clock (only for VLSI designer). 100 = PLL 64 Fs. 101 = PLL 128 Fs. 110 = PLL 256 Fs. 111 = PLL 384 Fs. [3] Output I2S interface format. 0 = I2S-justified (standard format). 1 = Left-justified. [2:0] Output I2S interface encoder word width. (bit rate). 000 = synthesizer 16 clock cycles per sample word (16 bit). 001 = Reserved. 010 = synthesizer 32 clock cycles per sample word (32 bit). 011 = Reserved. 100 = PLL 16 clock cycles per sample word (16 bit). 101 = PLL 24 clock cycles per sample word (24 bit). 110 = PLL 32 clock cycles per sample word (32 bit). 111 = Reserved.</p>
46h (2C8Dh)	REG2C8D	7:0	Default : 0x00
	I2S_OUT1_CFG[15:8]	7:0	See description of '2C8Ch'.
48h (2C90h)	REG2C90	7:0	Default : 0x0F
	PAD_CFG[7:0]	7:0	<p>0x2C90. [15:12] Reserved. [12:10] SPDIF PAD output source selection. 000 = SPDIF output. 001 = I2S SD1 output.</p>

VIVALDI Register (Bank = 2C)				
Index (Absolute)	Mnemonic	Bit	Description	
			010 = I2S SD2 output. 011 = I2S SD3 output. 100 = I2S_WCK (bypass mode). 101 = I2S_SD (bypass mode). 110 = Reserved. 111 = Reserved. [9:8] I2S MCLK PAD output source selection. 00 = I2S MCLK output. 01 = I2S SD1 output. 10 = I2S SD2 output. 11 = I2S SD3 output. [7:6] I2S output mux control. 2 = DSD output interface. Others = I2S output interfaces. [5:2] Reserved. [1] Output enable for the first I2S interface pins. 0 = enable. 1 = tri-stated. [0] Output enable for SPDIFO output pin. (S/PDIF Output). 0 = enable. 1 = tri-stated.	
48h (2C91h)	REG2C91	7:0	Default : 0x00	Access : R/W
	PAD_CFG[15:8]	7:0	See description of '2C90h'.	
49h (2C92h)	REG2C92	7:0	Default : 0x00	Access : R/W
	MUTE_CFG[7:0]	7:0	0x2C92. [7:6] Output selection for the MUTE output pin. 00 = MUTE. 01 = SD_1. 10 = SD_2. 11 = SD_3. [5:4] Select source for output AUMUTE pin (Audio Mute). 00 = from audio DSP channel 1 mute control. 01 = from audio DSP channel 2 mute control. 10 = from audio DSP channel 3 mute control. 11 = from audio DSP channel 4 mute control. [3] Reserved. [2] Mute function setting on AUMUTE pin. (Audio Mute).	

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0 = disable. 1 = output is active. [1] Configure AUMUTE output polarity. (Audio Mute). 0 = active-low for mute. 1 = active-high for mute. [0] Output enable for AUMUTE output pin. (Audio Mute). 0 = enable. 1 = tri-stated.
4Ah (2C94h)	REG2C94	7:0	Default : 0x00
	MUTE_CTRL1[7:0]	7:0	Access : R/W 0x2C94. [7] Enable Audio DSP channel 1 mute from SIF mute. 0 = disable. 1 = enable. [6] Enable Audio DSP channel 1 mute when DSD audio stream received from HDMI receiver. 0 = disable. 1 = enable. [5] Enable Audio DSP channel 1 mute from HDMI (flat sample, decode error, PLL unlock, etc). 0 = disable. 1 = enable. [4] Enable Audio DSP channel 1 mute when AVMUTE signal received from HDMI receiver. 0 = disable. 1 = enable. [3] Enable Audio DSP channel 1 mute when non-PCM audio stream received from HDMI receiver. 0 = disable. 1 = enable. [2] Enable Audio DSP channel 1 mute when SPDIF input decoding error occurs. 0 = disable. 1 = enable. [1] Enable Audio DSP channel 1 mute when non-PCM audio stream received from SPDIF input. 0 = disable. 1 = enable. [0] Enable Audio DSP channel 1 force Mute control.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0 = mute. 1 = normal.
4Bh (2C96h)	REG2C96	7:0	Default : 0x00 Access : R/W
	MUTE_CTRL2[7:0]	7:0	0x2C96. [7] Enable Audio DSP channel 2 mute from SIF mute. 0 = disable. 1 = enable. [6] Enable Audio DSP channel 2 mute when DSD audio stream received from HDMI receiver. 0 = disable. 1 = enable. [5] Enable Audio DSP channel 2 from HDMI (flat sample, decode error, PLL unlock, etc). 0 = disable. 1 = enable. [4] Enable Audio DSP channel 2 mute when AVMUTE signal received from HDMI receiver. 0 = disable. 1 = enable. [3] Enable Audio DSP channel 2 mute when non-PCM audio stream received from HDMI receiver. 0 = disable. 1 = enable. [2] Enable Audio DSP channel 2 mute when SPDIF input decoding error occurs. 0 = disable. 1 = enable. [1] Enable Audio DSP channel 2 mute when non-PCM audio stream received from SPDIF input. 0 = disable. 1 = enable. [0] Enable Audio DSP channel 2 force Mute. 0 = mute. 1 = normal.
4Ch (2C98h)	REG2C98	7:0	Default : 0x00 Access : R/W
	MUTE_CTRL3[7:0]	7:0	0x2C98. [7] Enable Audio DSP channel 3 mute from SIF mute. 0 = disable. 1 = enable.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>[6] Enable Audio DSP channel 3 mute when DSD audio stream received from HDMI receiver. 0 = disable. 1 = enable.</p> <p>[5] Enable Audio DSP channel 3 from HDMI (flat sample, decode error, PLL unlock, etc). 0 = disable. 1 = enable.</p> <p>[4] Enable Audio DSP channel 3 mute when AVMUTE signal received from HDMI receiver. 0 = disable. 1 = enable.</p> <p>[3] Enable Audio DSP channel 3 mute when non-PCM audio stream received from HDMI receiver. 0 = disable. 1 = enable.</p> <p>[2] Enable Audio DSP channel 3 mute when SPDIF input decoding error occurs. 0 = disable. 1 = enable.</p> <p>[1] Enable Audio DSP channel 3 mute when non-PCM audio stream received from SPDIF input. 0 = disable. 1 = enable.</p> <p>[0] Enable Audio DSP channel 3 force Mute. 0 = mute. 1 = normal.</p>
4Dh (2C9Ah)	REG2C9A	7:0	Default : 0x00
	MUTE_CTRL4[7:0]	7:0	<p>Access : R/W</p> <p>0x2C9A.</p> <p>[7] Enable Audio DSP channel 4 mute from SIF mute. 0 = disable. 1 = enable.</p> <p>[6] Enable Audio DSP channel 4 mute when DSD audio stream received from HDMI receiver. 0 = disable. 1 = enable.</p> <p>[5] Enable Audio DSP channel 4 from HDMI (flat sample, decode error, PLL unlock, etc). 0 = disable. 1 = enable.</p>

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>[4] Enable Audio DSP channel 4 mute when AVMUTE signal received from HDMI receiver. 0 = disable. 1 = enable.</p> <p>[3] Enable Audio DSP channel 4 mute when non-PCM audio stream received from HDMI receiver. 0 = disable. 1 = enable.</p> <p>[2] Enable Audio DSP channel 4 mute when SPDIF input decoding error occurs. 0 = disable. 1 = enable.</p> <p>[1] Enable Audio DSP channel 4 mute when non-PCM audio stream received from SPDIF input. 0 = disable. 1 = enable.</p> <p>[0] Enable Audio DSP channel 4 force Mute. 0 = mute. 1 = normal.</p>
50h (2CA0h)	REG2CA0	7:0	Default : 0xA9
	CODEC_SYNTH[7:0]	7:0	Access : R/W 0x2CA0. CODEC synthesizer N.f = 6.10. 256fs = 214 / N.f. EX: MPLL:214MHZ, FS:48K. CODEC_SYNTH_NF_1 = dec2hex(round(214000000*2^10/256/48000)). = 16'h45a9.
50h (2CA1h)	REG2CA1	7:0	Default : 0x45
	CODEC_SYNTH[15:8]	7:0	Access : R/W See description of '2CA0h'.
51h (2CA2h)	REG2CA2	7:0	Default : 0x00
	PLL_REF_CFG[7:0]	7:0	Access : R/W 0x2CA2. [6:4] SRC 256FS clock selection. 000 = from DSP decoder1 input. 001 = from DSP decoder2 input. 010 = from Audio ADC. 011 = from input S/PDIF interface. 100 = from input I2S interface. 101 = from HDMI. 110 = from HDMI.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>111 = from MPLL/15 or AU_PLL. [3] Audio codec PLL reference clock control. 0 = stop. 1 = enable. [2:0] Audio codec PLL reference clock selection. 000 = from DSP decoder1 input. 001 = from DSP decoder2 input. 010 = from Audio ADC. 011 = from input S/PDIF interface. 100 = from input I2S interface. 101 = from GPA_SRC_256_FS. 110 = from HDMI. 111 = from HDMI.</p>
52h (2CA4h)	REG2CA4	7:0	Default : 0x00
	CLK_CFG0[7:0]	7:0	<p>Access : R/W</p> <p>0x2CA4. [15] Audio CLK_150MHZ_ZR_MAC selection. 0 = MPLL /4 (recommend). 1 = MPLL /8. [14:13] Audio CLK_256FS_ADC_IN selection. 00 = codec synthesizer 128 FS. 01 = codec synthesizer 256 FS. 10 = codec PLL 128 FS. 11 = codec PLL 256 FS. [12] Audio CLK_SPDIF_SYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [11] Audio CLK_I2S_SYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [10] Audio CLK_SIF_SYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [9] Audio CLK_CODECSYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [8] Audio CLK_HDMI_SYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [7:6] Audio SIF FM demodulator clock source selection. 00 = MPLL / 4.</p>

VIVALDI Register (Bank = 2C)				
Index (Absolute)	Mnemonic	Bit	Description	
			01 = MPLL / 2 (recommend). 10 = VIF-ADC Clock. 11 = SIF-ADC Clock. . [3] Audio SIF channel relative clock enable setting. 0 = idle (power saving). 1 = enable. [2] Audio HDMI ACR engine selection. 0 = normal mode. 1 = test mode (CTS_N digital synthesizer). [5:4] [1:0] Audio codec PLL divider selection. 0000 = divide by 1. 0001 = divide by 2. 0010 = divide by 3. 0011 = divide by 4. 01xx = divide by 5. 10xx = divide by 16. 11xx = divide by 17.	
52h (2CA5h)	REG2CA5	7:0	Default : 0x00	Access : R/W
	CLK_CFG0[15:8]	7:0	See description of '2CA4h'.	
53h (2CA6h)	REG2CA6	7:0	Default : 0x00	Access : R/W
	CLK_CFG1[7:0]	7:0	0x2CA6. [15] Audio CLK_MCLK_I2S_ENCODER invert setting. 0 = normal. 1 = invert. [14] Audio CLK_SPDIF_ENCODER invert setting. 0 = normal. 1 = invert. [13] Audio CLK_SPDIF_DECODER invert setting. 0 = normal. 1 = invert. [12] Audio CLK_SPDIF_SYNTH invert setting. 0 = normal. 1 = invert. [11] Audio CLK_I2S_SYNTH invert setting. 0 = normal. 1 = invert. [10] Audio CLK_SIF_SYNTH invert setting. 0 = normal.	

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			1 = invert. [9] Audio CLK_CODECSYNTH invert setting. 0 = normal. 1 = invert. [8] Audio CLK_HDMI_SYNTH invert setting. 0 = normal. 1 = invert. [7] Audio CLK_SIF_ADC_R2B invert setting. 0 = normal. 1 = invert. [6] Audio CLK_SIF_ADC_R2B_FIFO invert setting. 0 = normal. 1 = invert. [5] Audio CLK_SIF_ADC_CIC invert setting. 0 = normal. 1 = invert. [4] Audio CLK_DSP_230 invert setting. 0 = normal. 1 = invert. [3] Audio CLK_HDMI_DECODER invert setting. 0 = normal. 1 = invert. [2] Audio CLK_64FS_HDMI_DSD invert setting. 0 = normal. 1 = invert. [1] Audio CLK_BCLK_I2S_DECODER invert setting. 0 = normal. 1 = invert. [0] Audio CLK_BCLK_I2S_ENCODER invert setting. 0 = normal. 1 = invert.
53h (2CA7h)	REG2CA7	7:0	Default : 0x00
	CLK_CFG1[15:8]	7:0	See description of '2CA6h'.
54h (2CA8h)	REG2CA8	7:0	Default : 0x00
	CLK_CFG2[7:0]	7:0	0x2CA8. [15] Audio CLK_256FS_CH4_OUT invert setting. 0 = normal. 1 = invert. [14] Audio CLK_256FS_CH3_OUT invert setting.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0 = normal. 1 = invert. [13] Audio CLK_256FS_CH2_OUT invert setting. 0 = normal. 1 = invert. [12] Audio CLK_256FS_CH1_OUT invert setting. 0 = normal. 1 = invert. [11] Audio CLK_214M_I2S_SRC invert setting. 0 = normal. 1 = invert. [10] Audio CLK_214M_SPDIF_SRC invert setting. 0 = normal. 1 = invert. [9] Audio CLK_256FS_ADC_IN invert setting. 0 = normal. 1 = invert. [8] Audio CLK_CODEC_PLL_REF invert setting. 0 = normal. 1 = invert. [7] Audio CLK_256FS_CH4_IN invert setting. 0 = normal. 1 = invert. [6] Audio CLK_256FS_CH3_IN invert setting. 0 = normal. 1 = invert. [5] Audio CLK_256FS_CH2_IN invert setting. 0 = normal. 1 = invert. [4] Audio CLK_256FS_CH1_IN invert setting. 0 = normal. 1 = invert. [3] Audio CLK_214M_CH4_SRC invert setting. 0 = normal. 1 = invert. [2] Audio CLK_214M_CH3_SRC invert setting. 0 = normal. 1 = invert. [1] Audio CLK_214M_CH2_SRC invert setting. 0 = normal.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			1 = invert. [0] Audio CLK_214M_CH1_SRC invert setting. 0 = normal. 1 = invert.
54h (2CA9h)	REG2CA9	7:0	Default : 0x00 Access : R/W
	CLK_CFG2[15:8]	7:0	See description of '2CA8h'.
55h (2CAAh)	REG2CAA	7:0	Default : 0x00 Access : R/W
	CLK_CFG3[7:0]	7:0	0x2CAA. [15] Audio CLK_DSP_230 enable setting. 0 = idle (power saving). 1 = enable. [14] Audio CLK_HDMI_DECODER enable setting. 0 = idle (power saving). 1 = enable. [13] Audio CLK_64FS_HDMI_DSD enable setting. 0 = idle (power saving). 1 = enable. [12] Audio CLK_BCLK_I2S_DECODER enable setting. 0 = idle (power saving). 1 = enable. [11] Audio CLK_150MHZ_ZR_MAC enable setting. 0 = idle (power saving). 1 = enable. [10] Audio CLK_256FS_ADC_IN enable setting. 0 = idle (power saving). 1 = enable. [9] Reserved. [8] Audio test clock enable setting. 0 = idle (power saving). 1 = enable. [7] Audio CLK_ICE_DSP_230 enable setting. 0 = idle (power saving). 1 = enable. [6] Reserved. [5] Audio CLK_SPDIF_DECODER enable setting. 0 = idle (power saving). 1 = enable. [4] Audio CLK_SPDIF_SYNTH enable setting. 0 = idle (power saving).

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			1 = enable. [3] Audio CLK_I2S_SYNTH enable setting. 0 = idle (power saving). 1 = enable. [2] Audio CLK_SIF_SYNTH enable setting. 0 = idle (power saving). 1 = enable. [1] Audio CLK_CODECSYNTH enable setting. 0 = idle (power saving). 1 = enable. [0] Audio CLK_HDMI_SYNTH enable setting. 0 = idle (power saving). 1 = enable.
55h (2CABh)	REG2CAB	7:0	Default : 0x00
	CLK_CFG3[15:8]	7:0	See description of '2CAAh'.
56h (2CACH)	REG2CAC	7:0	Default : 0x00
	CLK_CFG4[7:0]	7:0	0x2CAC. [15] Audio CH4 SRC clock system source selection. 0 = analog codec PLL. 1 = PLL reference. [14] Audio 768fs clock system source selection. 0 = analog codec PLL. 1 = digital 768fs synthesizer. [13] Audio DAC CH1~3 SRC clock 256fs selection. 0 = from 768fs clock system. 1 = from MPLL/15. [12] Audio CLK_768FS_PLL_SYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [11] Audio CLK_DVB_FIX_SYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [10] Audio CLK_DVB_SYNC_SYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [9] Audio CLK_27MHZ_DVB_REF source selection. 0 = 27 MHz. 1 = 13.5 MHz. [8] Audio DVB clock source selection.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0 = sync mode (following system clock). 1 = fix mode (DSP N.f mode). [7] Reserved. [6] Audio CLK_CARD_READER_SYNTH selection. 0 = 214 MHz. 1 = 107 MHz. [5] Audio CLK_CARD_READER_SYNTH invert setting. 0 = normal. 1 = invert. [4] Audio CLK_CARD_READER_SYNTH enable setting. 0 = idle (power saving). 1 = enable. [3] Audio DAC output SRC clock source selection. 0 = select codec PLL output clock 256 fs. 1 = select codec PLL reference clock 256 fs. [2:0] Reserved.
56h (2CADh)	REG2CAD	7:0	Default : 0x00
	CLK_CFG4[15:8]	7:0	Access : R/W See description of '2CACH'.
57h (2CAEh)	REG2CAE	7:0	Default : 0x00
	CLK_CFG5[7:0]	7:0	Access : R/W 0x2CAE. [15] Enable external clock. 0 = disable. 1 = enable. [14] Audio CLK_14318KHZ_FREE enable setting. 0 = idle (power saving). 1 = enable. [13] Reserved. [12] Audio CLK_ALL_768FS_SYNTH enable setting. 0 = idle (power saving). 1 = enable. [11] Audio CLK_214MHZ_DVB_FIX_SYNTH enable setting. 0 = idle (power saving). 1 = enable. [10] K118 CLK_ALL_DVB_SYNC_SYNTH enable setting. (214 Mhz / 256 fs feedback / 270 Mhz). 0 = idle (power saving). 1 = enable. [9] Audio CLK_256FS_DVB_TIMING_GEN enable setting. (Audio CLK_DSP_DECODER1_TIMING_GEN enable setting).

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>0 = idle (power saving). 1 = enable.</p> <p>[8] Audio CLK_256FS_SIF_TIMING_GEN enable setting. (Audio CLK_ DSP_DECODER2_TIMING_GEN enable setting). 0 = idle (power saving). 1 = enable.</p> <p>[7] Audio INV_CLK_185MHZ_CORDIC invert setting. 0 = normal. 1 = invert.</p> <p>[6] Audio CLK_768FS_PLL_SYNTH invert setting. 0 = normal. 1 = invert.</p> <p>[5] Audio CLK_128FS_SPDIF_NON_PCM_TRUE invert setting. 0 = normal. 1 = invert.</p> <p>[4] Audio CLK_256FS_DVB_SYNC_SYNTH_TRUE invert setting. 0 = normal. 1 = invert.</p> <p>[3] Audio CLK_214MHZ_DVB_FIX_SYNTH invert setting. 0 = normal. 1 = invert.</p> <p>[2] Audio CLK_214MHZ_DVB_SYNC_SYNTH invert setting. 0 = normal. 1 = invert.</p> <p>[1] Audio CLK_256FS_DVB_TIMING_GEN invert setting. (INV_DSP_DECODER1_ TIMING_GEN). 0 = normal. 1 = invert.</p> <p>[0] Audio CLK_256FS_SIF_TIMING_GEN invert setting. (INV_DSP_DECODER2_ TIMING_GEN). 0 = normal. 1 = invert.</p>
57h (2CAFh)	REG2CAF	7:0	Default : 0x00 Access : R/W
	CLK_CFG5[15:8]	7:0	See description of '2CAEh'.
58h (2CB0h)	REG2CB0	7:0	Default : 0x00 Access : R/W
	CLK_CFG6[7:0]	7:0	<p>0x2CB0. [15:14] Reserved. [13] Audio CLK_185MHZ_CORDIC source selection.</p>

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0 = MPLL 144MHz. 1 = MPLL 72MHz. [12] Reserved. [11:10] Audio SIF DSP 216 clock source selection. 00 = MPLL 172MHz. 01 = MIU 200MHz. 10 = UTMI 192MHz. 11 = MPLL 216MHz. [9:8] Audio SRC_FIX_XTAL_CH4 source selection. 00 = Codec PLL (SEL_SRC_SOURCE_SYNTH_CH4 = 0). Or Codec PLL ref. (SEL_SRC_SOURCE_SYNTH_CH4 =1). 01 = MPLL /15. 10 = SYNTH_DVB_FIX_256_FS. 11= SYNTH_CARD_READER_256_FS. [7:6] Audio test clock post divider selection. 00 = /1. 01 = /2. 10 = /4. 11 = /8. [5:0] Audio test clock selection. 00h = CLK_50MHZ_SIF_ADC_R2B_Z. 01h = CLK_50MHZ_SIF_ADC_R2B_FIFO_OUT_Z. 02h = CLK_100MHZ_SIF_ADC_CIC_Z. 03h = CLK_150MHZ_DSP_230_Z. 04h = CLK_ICE_DSP_230_Z. 05h = CLK_25MHZ_I_CLAMP_Z. 06h = CLK_150MHZ_ZR_MAC_GATE_Z. 07h = CLK_BCLK_I2S_DECODER_Z. 08h = CLK_BCLK_I2S_ENCODER_Z. 09h = CLK_150MHZ_ZR_MAC_FREE_Z. 0Ah = CLK_128FS_SPDIF_ENCODER_Z. 0Bh = CLK_128FS_SPDIF_DECODER_Z. 0Ch = CLK_214MHZ_SPDIF_SYNTH_Z. 0Dh = CLK_214MHZ_I2S_SYNTH_Z. 0Eh = CLK_214MHZ_SIF_SYNTH_Z. 0Fh = CLK_214MHZ_CODEC_SYNTH_Z. 10h = CLK_256FS_CHANNEL_1_IN_Z. 11h = CLK_256FS_CHANNEL_2_IN_Z. 12h = CLK_256FS_CHANNEL_3_IN_Z.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			13h = CLK_256FS_CHANNEL_4_IN_Z. 14h = CLK_214MHZ_CHANNEL_1_SRC_Z. 15h = CLK_214MHZ_CHANNEL_2_SRC_Z. 16h = CLK_214MHZ_CHANNEL_3_SRC_Z. 17h = CLK_214MHZ_CHANNEL_4_SRC_Z. 18h = CLK_256FS_CHANNEL_1_OUT_Z. 19h = CLK_256FS_CHANNEL_2_OUT_Z. 1Ah = CLK_256FS_CHANNEL_3_OUT_Z. 1Bh = CLK_256FS_CHANNEL_4_OUT_Z. 1Ch = CLK_256FS_ADC_IN_Z. 1Dh = CLK_256FS_REF_CODECS_PLL_Z. 1Eh = CLK_128FS_HDMI_Z. 1Fh = CLK_100MHZ_BIU_WR9_GATE_Z. 20h = CLK_100MHZ_FREE_Z. 21h = CLK_214MHZ_CHANNEL_I2S_SRC_Z. 22h = CLK_214MHZ_CHANNEL_SPDIF_SRC_Z. 23h = CLK_214MHZ_HDMI_SYNTH_Z. 24h = CLK_64FS_HDMI_DSD_Z. 25h = CLK_128FS_HDMI_TRUE_Z. 26h = CLK_128FS_SPDIF_DECODER_TRUE_Z. 27h = CLK_256FS_PCM_DELAY_Z. 28h = CLK_FM_DEMODULATOR_Z. 29h = CLK_BCLK_I2S_OUT2_ENCODER_Z. 2Ah = CLK_MCLK_I2S_OUT2_ENCODER_Z. 2Bh = CLK_214MHZ_CHANNEL_I2S_OUT2_SRC_Z. 2Ch = CLK_214MHZ_DVB_FIX_SYNTH_Z. 2DH = CLK_214MHZ_DVB_SYNC_SYNTH_Z. 2EH = CLK_256FS_DVB_SYNC_SYNTH_TRUE_Z. 2FH = CLK_256FS_DVB_TIMING_GEN_Z. 30H = CLK_256FS_SIF_TIMING_GEN_Z. 31H = CLK_256FS_CHANNEL_2_OUT_DAC_X1_Z. 32H = CLK_128FS_SPDIF_NON_PCM_TRUE_Z. 33h = CLK_270MHZ_DVB_REF_Z. 34h = CLK_14318KHZ_FREE_Z. 35h = CLK_214MHZ_768FS_PLL_SYNTH_Z. 36h = CLK_768FS_SYNTH_FEED_BACK_256_FS_DIV6_Z. 37h = CLK_768FS_PLL_REF_128_Z. 38h = CLK_128FS_CTS_N_SYNTH_FEED_BACK_Z. 39h = CLK_214MHZ_CARD_READER_FIX_SYNTH_Z. 3Ah = N.A.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			3Bh = N.A. 3Ch = N.A. 3Dh = N.A. 3Eh = N.A. 3Fh = N.A.
58h (2CB1h)	REG2CB1	7:0	Default : 0x00 Access : R/W
	CLK_CFG6[15:8]	7:0	See description of '2CB0h'.
59h (2CB2h)	REG2CB2	7:0	Default : 0x00 Access : R/W
	SYNTH_EXPANDER[7:0]	7:0	0x2CB2. [7] Lock current frequency of I2S synthesizer. 0 = normal. 1 = lock current frequency. [6] CARD_READER 256 fs synthesizer clock pulse expander. 0 = normal (1T width). 1 = expander (2T width). [5] DVB_FIX 256 fs synthesizer clock pulse expander. 0 = normal (1T width). 1 = expander (2T width). [4] DVB_SYNC 256 fs synthesizer clock pulse expander. 0 = normal (1T width). 1 = expander (2T width). [3] Band width of I2S synthesizer. 0 = low band width. 1 = high band width. [2] S/PDIF 256 fs synthesizer clock pulse expander. 0 = normal (1T width). 1 = expander (2T width). [1] CODEC 256 fs synthesizer clock pulse expander. 0 = normal (1T width). 1 = expander (2T width). [0] Band width of SIF 32k synthesizer. 0 = low band width. 1 = high band width.
5Ah (2CB4h)	REG2CB4	7:0	Default : 0x00 Access : R/W
	SYNTH_768_CONFIG_0[7:0]	7:0	0x2CB4. Synthesizer 768 fs PDF frequency setting. X=M=N.
5Ah	REG2CB5	7:0	Default : 0x00 Access : R/W

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
(2CB5h)	SYNTH_768_CONFIG_0[15:8]	7:0	See description of '2CB4h'.
5Bh (2CB6h)	REG2CB6	7:0	Default : 0x00 Access : R/W
	SYNTH_768_CONFIG_1[7:0]	7:0	0x2CB6. [7:3] Reserved. [2] Lock current frequency of SYNTH_768 synthesizer. 0 = normal. 1 = lock current frequency. [1] Audio SYNTH_768 synthesizer Cs gain selection. 0 = normal. 1 = enhancement (smaller Cs). [0] Audio SYNTH_768 synthesizer Cp gain selection. 0 = normal. 1 = enhancement (smaller Cp).
5Ch (2CB8h)	REG2CB8	7:0	Default : 0x00 Access : RO
	STATUS_SYNTH_768_FREQ[7:0]	7:0	0x2CB8. [15] Audio SYNTH_768 input signal detect. 0 = signal detected. 1 = no signal input. [14:0] Audio SYNTH_768 Frequency value.
5Ch (2CB9h)	REG2CB9	7:0	Default : 0x00 Access : RO
	STATUS_SYNTH_768_FREQ[15:8]	7:0	See description of '2CB8h'.
5Fh (2CBEh)	REG2CBE	7:0	Default : 0x00 Access : R/W
	TMXCTRL[7:0]	7:0	0x2CBE. Internal debug port selection (Only for VLSI designer). (refer to TEST MUX detail description).
61h ~ 62h (2CC2h ~ 2CC5h)	-	7:0	Default : - Access : -
	-	-	Reserved.
66h ~ 66h (2CCCh ~ 2CCDh)	-	7:0	Default : - Access : -
	-	-	Reserved.
6Ch ~ 6Ch (2CD8h ~ 2CD9h)	-	7:0	Default : - Access : -
	-	-	Reserved.
6Eh ~ 6Eh	-	7:0	Default : - Access : -

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
(2CDCh ~ 2CDDh)	-	-	Reserved.
70h (2CE0h)	REG2CE0	7:0	Default : 0x00
	CODEC_CFG0[7:0]	7:0	Access : R/W 0x2CE0. [15:4] Reserved.
70h (2CE1h)	REG2CE1	7:0	Default : 0x00
	CODEC_CFG0[15:8]	7:0	Access : R/W See description of '2CE0h'.
71h (2CE2h)	REG2CE2	7:0	Default : 0x40
	CODEC_CFG1[7:0]	7:0	Access : R/W 0x2CE2. [15:14] Line-Out (AA) OPamp Bias Current. 00 = 20uA. 01 = 15uA. 10 = 30uA. 11 = 25uA. [13:12] ADC Input Mixer (Anti aliasing filter) OPamp Bias Current. 00 = 20uA. 01 = 15uA. 10 = 30uA. 11 = 25uA. [11:10] ADC Integrator OPamp Bias Current. 00 = 20uA. 01 = 15uA. 10 = 30uA. 11 = 25uA. [9:8] Audio DAC OPamp Bias Current. 00 = 20uA. 01 = 15uA. 10 = 30uA. 11 = 25uA. [7:6] Audio Reference Voltage Generator OPamp Bias Control. 00 = 20uA. 01 = 15uA. 10 = 30uA. 11 = 25uA. [5:4] Reserved Current Control (for future). 00 = 20uA. 01 = 15uA. 10 = 30uA.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			11 = 25uA. [3:2] Audio ADC Output Duty Cycle Test. 00 = Select AVSS. 01 = Select AVSS. 10 = Select Left Channel ADC Output. 11 = Select Right Channel ADC Output. [1] Reserved. [0] Reset FF 16 in DAC. 0 = Normal Function. 1 = Reset.
71h (2CE3h)	REG2CE3	7:0	Default : 0x00
	CODEC_CFG1[15:8]	7:0	Access : R/W See description of '2CE2h'.
72h (2CE4h)	REG2CE4	7:0	Default : 0xA0
	CODEC_CFG2[7:0]	7:0	Access : R/W 0x2CE4. [15] Power Down Right Channel ADC. 0 = normal. 1 = power down. [14] Power Down Left Channel ADC. 0 = normal. 1 = power down. [13] Power Down Audio ADC input Clock. 0 = normal. 1 = Power Down. [12] Select Audio ADC Input Clock Source. 0 = From Clock Generator. 1 = From External PAD (Video VSYNC_0). [11:9] SDMADC Clock Delay (unit = inverter buffer 70ps). 000 = Delay 0 time unit. 001 = Delay 4 time unit. 010 = Delay 8 time unit. 011 = Delay 12 time unit. 100 = Delay 16 time unit. 101 = Delay 20 time unit. 110 = Delay 24 time unit. 111 = Delay 28 time unit. [8] Reserved. [7:6] Audio SDMADC Left Channel Internal Feedback Coefficient. 00 = 0.300 pF.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			01 = 0.225 pF. 10 = 0.270 pF. 11 = 0.345 pF. [5:4] Audio SDMADC Right Channel Internal Feedback Coefficient. 00 = 0.300 pF. 01 = 0.225 pF. 10 = 0.270 pF. 11 = 0.345 pF. [3:0] Reserved.
72h (2CE5h)	REG2CE5	7:0	Default : 0xE0
	CODEC_CFG2[15:8]	7:0	Access : R/W See description of '2CE4h'.
73h (2CE6h)	REG2CE6	7:0	Default : 0x80
	CODEC_CFG3[7:0]	7:0	Access : R/W 0x2CE6. [15] DE_POP Line-Out[0] Amplifier Control (feedback R = 0). 0 = normal. 1 = mute. [14:11] Audio Line-Out[0] (AA_0) Input Source Selection. 0000 = Line-in [0]. 0001 = Line-in [1]. 0010 = Line-in [2]. 0011 = Line-in [3]. 0100 = MONOIN. 0101 = AVSS. 0110 = DACL1 & DACR1 out. 0111 = DACL0 & DACR0 out. 1000 = DACL2 & DACR2 out. 1001 = DACL3 & DACR3 out. 1010 = AVSS. 1011 = AVSS. 1100 = AVSS. Others = N.A. [10:9] Audio Line-Out[0] (AA_0) Gain Control. 00 = 0 dB. 01 = -3 dB. 10 = -6 dB. 11 = +3 dB. [8] Audio ADC input Mixer (Anti alias Filter) OPamp Control. 0 = normal Anti alias Filter OPamp.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>1 = Mute Anti alias Filter OPamp (feedback R = 0). [7] Power Down Audio ADC input Mixer (Anti alias Filter) OPamp. 0 = normal. 1 = Power Down. [6:3] Audio ADC Input Mixer Source Selection. 0000 => Line-in[0]. 0001 => Line-in[1]. 0010 => Line-in[2]. 0011 => Line-in[3]. 0100 => MONOIN. 0101 => AVSS. 0110 => DAL1 & DAR1. 0111 => DAL0 & DAR0. 1000 => DAL2 & DAR2. 1001 => DAL3 & DAR3. 1010 => AVSS. 1011 => AVSS. 1100 => Line-Out[0] left & right (AA0). 1101 => Line-Out[1] left & right (AA1). Others => N.A. [2:0] Audio ADC Input Mixer (Anti alias Filter) Gain Control. 000 = 0 dB. 001 = -3 dB. 010 = -6 dB. 011 = +3 dB. 100 = +6 dB. 101 = +9 dB. 110 = +12 dB.</p>
73h (2CE7h)	REG2CE7	7:0	Default : 0x28
	CODEC_CFG3[15:8]	7:0	See description of '2CE6h'.
74h (2CE8h)	REG2CE8	7:0	Default : 0x00
	CODEC_CFG4[7:0]	7:0	<p>Access : R/W</p> <p>0x2CE8. [15] DE_POP Line-Out[1] (AA_1). Amplifier Control (feedback R = 0). 0 = normal. 1 = mute. [14:11] Audio Line-Out[1] (AA_1) Input Source Selection. 0000 = Line-in [0].</p>

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0001 = Line-in [1]. 0010 = Line-in [2]. 0011 = Line-in [3]. 0100 = MONOIN. 0101 = AVSS. 0110 = DACL1 & DACR1 out. 0111 = DACL0 & DACR0 out. 1000 = DACL2 & DACR2 out. 1001 = DACL3 & DACR3 out. 1010 = AVSS. 1011 = AVSS. 1100 = Line-Out[0] left & right (AA0). 1101 = Line-Out[1] left & right (AA1). Others = N.A. [10:9] Audio Line-Out[1] (AA_1) Gain Control. 00 = 0 dB. 01 = -3 dB. 10 = -6 dB. 11 = +3 dB. [8] Reserved. [7] Audio Line-Out[0] (AA_0) Right Channel Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%. [6] Audio Line-Out[0] (AA_0) Left Channel Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%. [5] Audio Line-Out[0] (AA_0) Right Channel Amplifier Low Power Mode. 0 = normal. 1 = Low Power Mode (50% Bias Current). [4] Audio Line-Out[0] (AA_0) Left Channel Amplifier Low Power Mode. 0 = normal. 1 = Low Power Mode (50% Bias Current). [3] Reserved. [2] Disable DAC[2] Re-latch Clock. 0 = Normal. 1 = Clock Disabled.

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			[1] Disable DAC[0] Re-latch Clock. 0 = Normal. 1 = Clock Disabled. [0] Disable DAC[1] Re-latch Clock. 0 = Normal. 1 = Clock Disabled.
74h (2CE9h)	REG2CE9	7:0	Default : 0x28
	CODEC_CFG4[15:8]	7:0	Access : R/W See description of '2CE8h'.
75h (2CEAh)	REG2CEA	7:0	Default : 0x00
	CODEC_CFG5[7:0]	7:0	Access : R/W 0x2CEA. [15] Audio DAC Right Channel[1] low power mode. 0 = normal. 1 = low power mode (50%). [14] Audio DAC Right Channel[1] Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%. [13] Audio DAC Left Channel[1] low power mode. 0 = normal. 1 = low power mode (50%). [12] Audio DAC Left Channel[1] Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%. [11] Reset DAC[3] Re-latch Flip-flip. 0 = Normal. 1 = Reset (.OR. Gated with DSP). [10] Reset DAC[2] Re-latch Flip-flip. 0 = Normal. 1 = Reset (.OR. Gated with DSP). [9] Reset DAC[0] Re-latch Flip-flip. 0 = Normal. 1 = Reset (.OR. Gated with DSP). [8] Reset DAC[1] Re-latch Flip-flip. 0 = Normal. 1 = Reset (.OR. Gated with DSP). [7] Audio Line-Out[1] (AA_1) Right Channel Amplifier Driving

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>Strength.</p> <p>0 = normal.</p> <p>1 = Reduce to 1%.</p> <p>[6] Audio Line-Out[1] (AA_1) left Channel Amplifier Driving Strength.</p> <p>0 = normal.</p> <p>1 = Reduce to 1%.</p> <p>[5] Audio Line-Out[1] (AA_1) Right Channel Amplifier Low Power Mode.</p> <p>0 = normal.</p> <p>1 = Low Power Mode (50% Bias Current).</p> <p>[4] Audio Line-Out[1] (AA_1) left Channel Amplifier Low Power Mode.</p> <p>0 = normal.</p> <p>1 = Low Power Mode (50% Bias Current).</p> <p>[3] Mute Audio Line-Out[1] (AA_1) (Input Floating).</p> <p>0 = normal.</p> <p>1 = mute.</p> <p>[2] Mute Audio Line-Out[0] (Input Floating).</p> <p>0 = normal.</p> <p>1 = mute.</p> <p>[1] Power Down Audio Line-Out[1] (AA_1).</p> <p>0 = power on.</p> <p>1 = power down (.OR. Gated with DSP).</p> <p>[0] Power Down Audio Line-Out[0] (AA_0).</p> <p>0 = power on.</p> <p>1 = power down (.OR. Gated with DSP).</p>
75h (2CEBh)	REG2CEB	7:0	Default : 0x00
	CODEC_CFG5[15:8]	7:0	See description of '2CEAh'.
76h (2CECh)	REG2CEC	7:0	Default : 0x00
	CODEC_CFG6[7:0]	7:0	<p>0x2CEC.</p> <p>[15] Audio DAC Right Channel[0] low power mode.</p> <p>0 = normal.</p> <p>1 = low power mode (50%).</p> <p>[14] Audio DAC Right Channel[0] Amplifier Driving Strength.</p> <p>0 = normal.</p> <p>1 = Reduce to 1%.</p>

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>[13] Power Down Audio DAC Right Channel[1] L Driving OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[12] Power Down Audio DAC Right Channel[1] L Vref OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[11] Audio DAC Left Channel[0] low power mode. 0 = normal. 1 = low power mode (50%).</p> <p>[10] Audio DAC Left Channel[0] Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%.</p> <p>[9] Power Down Audio DAC Channel[0] Driving OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[8] Power Down Audio DAC Channel[0] Vref OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[7:6] Reserved.</p> <p>[5] Power Down Audio DAC Channel[1] R Driving OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[4] Power Down Audio DAC Channel[1] R Vref OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[3] Audio DAC Data Latching Mode Select. 0 = negative edge select. 1 = positive edge select.</p> <p>[2] Power Down Audio DAC Reference Current Generator. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[1] Audio DAC Reference Current Test Mode.</p>

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			0 = normal. 1 = Bypass test current to PAD (SOG_[1:0] = Test [1:0]). [0] Reserved.
76h (2CEDh)	REG2CED	7:0	Default : 0x00 Access : R/W
	CODEC_CFG6[15:8]	7:0	See description of '2CECh'.
77h (2CEEh)	REG2CEE	7:0	Default : 0x00 Access : R/W
	CODEC_CFG7[7:0]	7:0	0x2CEE. [15] Audio DAC Right Channel[3] low power mode. 0 = normal. 1 = low power mode (50%). [14] Audio DAC Right Channel[3] Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%. [13] Power Down Audio DAC Right Channel[3] L Driving OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP). [12] Power Down Audio DAC Right Channel[3] L Vref OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP). [11] Audio DAC Left Channel[3] low power mode. 0 = normal. 1 = low power mode (50%). [10] Audio DAC Left Channel[3] Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%. [9] DAC Discharge Control. 0 = Disable. 1 = Enable (.OR. Gated with DSP). [8] VREF Discharge Control. 0 = Disable. 1 = Enable (.OR. Gated with DSP). [7] Audio DAC Right Channel[2] low power mode. 0 = normal. 1 = low power mode (50%).

VIVALDI Register (Bank = 2C)

Index (Absolute)	Mnemonic	Bit	Description
			<p>[6] Audio DAC Right Channel[2] Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%.</p> <p>[5] Power Down Audio DAC Right Channel[2] L Driving OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[4] Power Down Audio DAC Right Channel[2] L Vref OPamp. 0 = power on. 1 = power down (.OR. Gated with DSP).</p> <p>[3] Audio DAC Left Channel[2] low power mode. 0 = normal. 1 = low power mode (50%).</p> <p>[2] Audio DAC Left Channel[2] Amplifier Driving Strength. 0 = normal. 1 = Reduce to 1%.</p> <p>[1:0] Reserved.</p>
77h (2CEFh)	REG2CEF	7:0	Default : 0x00 Access : R/W
	CODEC_CFG7[15:8]	7:0	See description of '2CEEh'.
78h (2CF0h)	REG2CF0	7:0	Default : 0x00 Access : RO
	BONDING_INFO[7:0]	7:0	<p>[13:10] Bonding Information.</p> <p>[10] : BOND_AUDIO_0.</p> <p>[11] : BOND_AUDIO_1.</p> <p>[12] : BOND_AUDIO_2.</p> <p>[13] : BOND_AUDIO_3.</p>
78h (2CF1h)	REG2CF1	7:0	Default : 0x00 Access : RO
	BONDING_INFO[15:8]	7:0	See description of '2CF0h'.
79h (2CF2h)	REG2CF2	7:0	Default : 0x00 Access : R/W
	RESERVED_2CF2[7:0]	7:0	<p>0x2CF2.</p> <p>[8]: REG_HDMI_NONPCM_RESET. 1: Hdmi nonpcm sft reset enable. 0: Hdmi nonpcm sft reset disable.</p> <p>[7:6] : REG_TIMEOUT_SEL. 00: 2^15 *FS. 01: 2^13 *FS. 10: 2^12 *FS.</p>

VIVALDI Register (Bank = 2C)				
Index (Absolute)	Mnemonic	Bit	Description	
			11: 2 ¹¹ *FS. [5]: REG_FAST_LOCK. [4]: REG_NEW_MODE. [3]: REG_INPUT_NONPCM_BYPASS. [1]: REG_SPDIF_OPEN_DRAIN_MODE. 1: Enable open-drain mode. 0: Disable. [0]: REG_SPDIF_CFG. 1: Inverse spdif output waveform. 0: No inverse.	
79h (2CF3h)	REG2CF3	7:0	Default : 0x00	Access : R/W
	RESERVED_2CF2[15:8]	7:0	See description of '2CF2h'.	
7Bh (2CF6h)	REG2CF6	7:0	Default : 0x00	Access : R/W
	TEST_CTRL1[7:0]	7:0	0x2CF6.	
7Bh (2CF7h)	REG2CF7	7:0	Default : 0x00	Access : R/W
	TEST_CTRL1[15:8]	7:0	See description of '2CF6h'.	
7Ch (2CF8h)	REG2CF8	7:0	Default : 0x00	Access : R/W
	TEST_CTRL2[7:0]	7:0	0x2CF8.	
7Ch (2CF9h)	REG2CF9	7:0	Default : 0x00	Access : R/W
	TEST_CTRL2[15:8]	7:0	See description of '2CF8h'.	
7Dh (2CFAh)	REG2CFA	7:0	Default : 0x00	Access : R/W
	TEST_CTRL3[7:0]	7:0	0x3CFA.	
7Dh (2CFBh)	REG2CFB	7:0	Default : 0x00	Access : R/W
	TEST_CTRL3[15:8]	7:0	See description of '2CFAh'.	
7Eh (2CFCh)	REG2CFC	7:0	Default : 0x00	Access : RO
	TEST_BUS_OUT_L[7:0]	7:0	0x2CFC test bus output LSB.	
7Eh (2CFDh)	REG2CFD	7:0	Default : 0x00	Access : RO
	TEST_BUS_OUT_L[15:8]	7:0	See description of '2CFCh'.	
7Fh (2CFEh)	REG2CFE	7:0	Default : 0x00	Access : RO
	TEST_BUS_OUT_H[7:0]	7:0	0x2CFE test bus output MSB.	

AUDIO1 Register (Bank = 2D)

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2D00h)	REG2D00	7:0	Default : 0x03	Access : RO, R/W
	-	7	Reserved.	
	DSP16K_BANK_SEL	6	DSP16K Bank Select. 0: IDMA access memory 0~16K. 1: IDMA access memory > 16K.	
	INT_TRIGGER	5	MIPS-triggered DSP PIO[8] interrupt. 0: De-assert DSP PIO[8] interrupt. 1: Assert DSP PIO[8] interrupt.	
	IDMA_WR_CMD_STA	4	IDMA write command status. 0: IDMA write command finish. 1: IDMA write ongoing (busy).	
	IDMA_RD_CMD_STA	3	IDMA Read Command / Status. Command: 0: N.A. 1: Set IDMA read command, auto-clear when finished. Status: 0: Read command finished. 1: Read command busy.	
	IDMA_WR2ND	2	IDMA needs to write 2nd Data Set. 0: IDMA write data finished. 1: IDMA needs to write 2nd data set. Note: Write 0 to clear.	
	IDMA_BOOT_MODE	1	DSP IDMA Boot Mode Enable. 0: Disable. 1: Enable.	
01h (2D02h)	DSP_SOFT_RST	0	DSP Audio Software Reset. 0: Reset. 1: Normal.	
	REG2D02	7:0	Default : 0x00	Access : WO
01h (2D03h)	DSP_BRG_DATA[7:0]	7:0	Host Download DSP Data Port. 24-bit mode: 1: Write high 2 bytes {DATA[23:8]}. 2: Write low byte {8'b0, DATA[7:0]}. 3: Loop to step 1.	
	REG2D03	7:0	Default : 0x00	Access : WO
01h (2D03h)	DSP_BRG_DATA[15:8]	7:0	See description of '2D02h'.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
02h (2D04h)	REG2D04	7:0	Default : 0x00	Access : R/W
	IDMA_WRBASE_ADDR[7:0]	7:0	Channel 1 IDMA address base IAD.	
02h (2D05h)	REG2D05	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH1_MEM_SEL	6	Channel 1 IDMA address base PM/CM/DM control. 0: Select PM/CM. 1: Select DM.	
	IDMA_WRBASE_ADDR[13:8]	5:0	See description of '2D04h'.	
03h (2D06h)	REG2D06	7:0	Default : 0x00	Access : R/W
	CH1IDMA_ATR_SIZE[7:0]	7:0	IDMAtrSize.	
03h (2D07h)	REG2D07	7:0	Default : 0x00	Access : RO, R/W
	-	7	Reserved.	
	CH1IDMA_CIRCULAR_BUF	6	Disable IDMA CH2 circular buffer. 0: Enable circular buffer. 1: Disable circular buffer.	
	CH1IDMA_ATR_SIZE[13:8]	5:0	See description of '2D06h'.	
04h (2D08h)	REG2D08	7:0	Default : 0x00	Access : R/W
	IDMA_RDBASE_ADDR[7:0]	7:0	Channel 2 IDMA address base IAD.	
04h (2D09h)	REG2D09	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH2_MEM_SEL	6	Channel 2 IDMA address base PM/CM/DM control. 0: Select PM/CM. 1: Select DM.	
	IDMA_RDBASE_ADDR[13:8]	5:0	See description of '2D08h'.	
05h (2D0Ah)	REG2D0A	7:0	Default : 0x00	Access : R/W
	CH2IDMA_ATR_SIZEH[7:0]	7:0	IDMAtrSize.	
05h (2D0Bh)	REG2D0B	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH2IDMA_ATR_SIZEH_DIS	6	Disable IDMA CH2 circular buffer. 0: Enable circular buffer. 1: Disable circular buffer.	
	CH2IDMA_ATR_SIZEH[13:8]	5:0	See description of '2D0Ah'.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
06h (2D0Ch)	REG2D0C	7:0	Default : 0x00 Access : RO
	IDMA_RDDATA_H[7:0]	7:0	IDMA CH2 MIPS Read DSP Data Port [23:8], for transferring data from DSP to MIPS.
06h (2D0Dh)	REG2D0D	7:0	Default : 0x00 Access : RO
	IDMA_RDDATA_H[15:8]	7:0	See description of '2D0Ch'.
07h (2D0Eh)	REG2D0E	7:0	Default : 0x00 Access : RO
	IDMA_RDDATA_L[7:0]	7:0	IDMA CH2 MIPS Read DSP Data Port [7:0], for transferring data from DSP to MIPS.
08h (2D10h)	REG2D10	7:0	Default : 0x00 Access : R/W
	DSP_ICACHE_BASE[7:0]	7:0	[15:8] FD230 I-Cache MIU base address [23:16]. [7:0] ICU base address = {DSP_ICH_BASE[15:0], 8'b0} + ICU_MIU_ADDR[15:0].
08h (2D11h)	REG2D11	7:0	Default : 0x00 Access : R/W
	DSP_ICACHE_BASE[15:8]	7:0	See description of '2D10h'.
09h (2D12h)	REG2D12	7:0	Default : 0x00 Access : R/W
	MCU2DSP_MAILBOX_CFG[3:0]	7:4	MCU to DSP mailbox configuration. 0000: M2D_MAILBOX_0 (0x7000). 0001: M2D_MAILBOX_1 (0x7001). 0010: M2D_MAILBOX_2 (0x7002). 0011: M2D_MAILBOX_3 (0x7003). 0100: M2D_MAILBOX_4 (0x7004). 0101: M2D_MAILBOX_5 (0x7005). 0110: M2D_MAILBOX_6 (0x7006). 0111: M2D_MAILBOX_7 (0x7007). 1000: M2D_MAILBOX_8 (0x7008). 1001: M2D_MAILBOX_9 (0x7009).
	DSP2MCU_MAILBOX_CFG[3:0]	3:0	DSP to MCU mailbox configuration. 0000: D2M_MAILBOX_0. 0001: D2M_MAILBOX_1. 0010: D2M_MAILBOX_2. 0011: D2M_MAILBOX_3. 0100: D2M_MAILBOX_4. 0101: D2M_MAILBOX_5. 0110: D2M_MAILBOX_6. 0111: D2M_MAILBOX_7.
0Ah (2D14h)	REG2D14	7:0	Default : 0x00 Access : R/W
	MCU2DSP_MAILBOX[7:0]	7:0	MCU to DSP Mailbox.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			Indirect Mailbox Write to DSP Port.
0Ah (2D15h)	REG2D15	7:0	Default : 0x00
	MCU2DSP_MAILBOX[15:8]	7:0	Access : R/W See description of '2D14h'.
0Bh (2D16h)	REG2D16	7:0	Default : 0x00
	DSP2MCU_MAILBOX[7:0]	7:0	Access : RO DSP to MCU Mailbox. Indirect Mailbox Read from DSP Port.
0Bh (2D17h)	REG2D17	7:0	Default : 0x00
	DSP2MCU_MAILBOX[15:8]	7:0	Access : RO See description of '2D16h'.
0Ch (2D18h)	REG2D18	7:0	Default : 0x00
	-	7:1	Access : R/W Reserved.
	RIU2DSP_INFO	0	UP interrupt DSP signal, software controlled H/L.
10h (2D20h)	REG2D20	7:0	Default : 0x00
	STD_SEL_SET	7	Access : R/W Audio SIF Standard Set Command. 0: Manual. 1: Auto.
	STD_SEL[6:0]	6:0	SIF audio standard Selection. For PAL DSP code: [7:4]: Mode Selection. 0x10: FM mono hideviation mode.
11h (2D22h)	REG2D22	7:0	Default : 0x00
	-	7:3	Access : R/W Reserved.
	STD_PRE45[1:0]	2:1	Preference in automatic standard Selection of 4.5MHz carrier. 00: Standard M (Korea). 01: Standard M (BTSC). 10: Standard M (Japan). 11: Not a sound carrier.
	STD_PRE65	0	Preference in automatic standard Selection of 6.5MHz carrier. 0: Standard L (SECAM). 1: Standard D/K.
12h (2D24h)	REG2D24	7:0	Default : 0x00
	SIF_SOUND_MOD1[7:0]	7:0	Access : R/W SIF BTSC/A2 demodulator automatic/manual sound mode output select. 0xxxxxxx: Manual sound select. 0000-0000: BTSC Mono. 00000001: BTSC Stereo. 00000010: BTSC SAP.

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
			00000100: A2 Mono. 00000101: A2 Stereo. 00000110: A2 Dual B. 00000111: A2 Dual A+B. 1xxxxxxx: Auto sound select. 10000000: BTSC Mono <-> Mute. 10000001: BTSC Stereo <-> Mono <-> Mute. 10000010: BTSC SAP <-> Mono <-> Mute. 10000100: A2 Mono <-> Mute. 10000101: A2 Stereo <-> Mono <-> Mute. 10000110: A2 Dual B <-> Mono <-> Mute. 10000111: A2 Dual B <-> Stereo->Mono <-> Mute.	
13h (2D26h)	REG2D26	7:0	Default : 0x00	Access : R/W
	SIF_SOUND_MOD2[7:0]	7:0	SIF NICAM demodulator sound mode output select. 00000000: NICAM Auto Mode. NICAM Sound (Auto) FM/AM Mono Mute. 0x01: FM/AM Mono (OSD). 0x02: Stereo L/R FM/AM Mono (OSD). 0x03: Stereo L/L FM/AM Mono (OSD). 0x04: Stereo R/R FM/AM Mono (OSD). 0x05: Dual A/B FM/AM Mono. 0x06: Dual A/A FM/AM Mono. 0x07: Dual B/B FM/AM Mono. 0x08: NICAM Mono FM/AM Mono. 0x80: Force NICAM Sound.	
14h (2D28h)	REG2D28	7:0	Default : 0x00	Access : R/W
	AVC_CLIP[7:0]	7:0	Fine Tune AVC Clip Level.	
15h (2D2Ah)	REG2D2A	7:0	Default : 0x00	Access : R/W
	DBG_CMD[7:0]	7:0	SIF common command set: 0x00: No action. 0x01: Common command - get firmware version. 0x02: Common command - set memory data. 0x03: Common command - set DM memory address. 0x04: Common command - set PM memory address. 0x05: Common command - read DM memory address. BTSC command: 0x10: BTSC_CMD_UPDATE_PILOT_ON_THR. Pilot Off to On Threshold Update Command. 0x11: BTSC_CMD_UPDATE_PILOT_OFF_THR.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			Pilot On to Off Threshold Update Command. 0x12: BTSC_CMD_UPDATE_CARRIER_ON_THR. Carrier Off to On Threshold Update Command. 0x13: BTSC_CMD_UPDATE_CARRIER_OFF_THR. Carrier On to Off Threshold Update Command. 0x14: BTSC_CMD_UPDATE_SAP_ON_THR. SAP Off to On Threshold Update Command. 0x15: BTSC_CMD_UPDATE_SAP_OFF_THR. SAP On to Off Threshold Update Command. A2 Command: 0x20: A2_CMD_UPDATE_CARRIER_ON_THR. Carrier Off to On Threshold Update Command. 0x21: A2_CMD_UPDATE_CARRIER_OFF_THR. Carrier On to Off Threshold Update Command. 0x22: A2_CMD_UPDATE_MONO_ON_THR. Mono Off to On Threshold Update Command. 0x23: A2_CMD_UPDATE_MONO_OFF_THR. Mono On to Off Threshold Update Command. 0x24: A2_CMD_UPDATE_STEREO_DUAL_THR. Stereo / Dual Threshold Update Command. 0x30: A2_CMD_GET_CARRIER_1_AMP. Carrier 1 Amplitude Output Command. 0x31: A2_CMD_GET_CARRIER_1_VAR. 0x32: A2_CMD_GET_CARRIER_2_AMP. Carrier 2 Amplitude Output Command. 0x33: A2_CMD_GET_CARRIER_2_VAR. 0x34: A2_CMD_GET_MONO_AMP. Mono Amplitude Output Command. 0x35: A2_CMD_GET_STEREO_AMP. Stereo Amplitude Output Command. 0x36: A2_CMD_GET_DUAL_AMP. Dual Amplitude Output Command.
16h (2D2Ch)	REG2D2C	7:0	Default : 0x00
	DBG_DATA_H[7:0]	7:0	Data-high, from 8051 to DSP, which needs to match cmd (0x85).
17h (2D2Eh)	REG2D2E	7:0	Default : 0x00
	DBG_DATA_L[7:0]	7:0	Data-low, from 8051 to DSP, which needs to match cmd (0x85).
18h	REG2D30	7:0	Default : 0x00
			Access : R/W

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
(2D30h)	DEBUG_REG_0[7:0]	7:0	8 bytes for software utilization.	
19h	REG2D32	7:0	Default : 0x00	Access : R/W
(2D32h)	DEBUG_REG_1[7:0]	7:0	8 bytes for software utilization.	
1Ah	REG2D34	7:0	Default : 0x00	Access : R/W
(2D34h)	DEBUG_REG_2[7:0]	7:0	8 bytes for software utilization.	
1Bh	REG2D36	7:0	Default : 0x00	Access : R/W
(2D36h)	DEBUG_REG_3[7:0]	7:0	8 bytes for software utilization.	
1Ch	REG2D38	7:0	Default : 0x00	Access : R/W
(2D38h)	DEBUG_REG_4[7:0]	7:0	8 bytes for software utilization.	
1Dh	REG2D3A	7:0	Default : 0x00	Access : R/W
(2D3Ah)	DEBUG_REG_5[7:0]	7:0	8 bytes for software utilization.	
1Eh	REG2D3C	7:0	Default : 0x00	Access : R/W
(2D3Ch)	DEBUG_REG_6[7:0]	7:0	8 bytes for software utilization.	
1Fh	REG2D3E	7:0	Default : 0x00	Access : R/W
(2D3Eh)	DEBUG_REG_7[7:0]	7:0	8 bytes for software utilization.	
20h	REG2D40	7:0	Default : 0x00	Access : RO
(2D40h)	STD_RESULT_FINISH	7	Audio SIF Standard Detection Flag. 0: Standard detection finished. 1: Standard detection not finished.	
	STD_RESULT[6:0]	6:0	SIF Standard Detect Result. 00h: Standard not found. 01h: AU_SYS_M_BTSC. 02h: AU_SYS_M_KOREA. 03h: AU_SYS_M_JAPAN. 04h: AU_SYS_BG_A2. 05h: AU_SYS_DK1_A2. 06h: AU_SYS_DK2_A2. 07h: AU_SYS_DK3_A2. 08h: AU_SYS_BG_NICAM. 09h: AU_SYS_DK_NICAM. 0ah: AU_SYS_I_NICAM. 0bh: AU_SYS_L_NICAM. 0ch: AU_SYS_FM_RADIO.	
22h	REG2D44	7:0	Default : 0x00	Access : RO
(2D44h)	STATUS_MOD[7:0]	7:0	Sound Mode Status. [0]: BTSC Mono existing.	

AUDIO1 Register (Bank = 2D)			
Index (Absolute)	Mnemonic	Bit	Description
			[1]: BTSC Stereo existing. [2]: BTSC Sap existing. [3]: A2 Carrier 1 existing. [4]: A2 Carrier 2 existing. [5]: A2 Stereo existing. [6]: A2 Dual existing. [7]: A2 Mono existing.
25h (2D4Ah)	REG2D4A	7:0	Default : 0x00 Access : RO
	DBG_OUTPUT_L[7:0]	7:0	Debugging Data Port. Directly output data from DSP230 I/O Write Command.
26h (2D4Ch)	REG2D4C	7:0	Default : 0x00 Access : RO
	DBG_OUTPUT_H[7:0]	7:0	Debugging Data Port. Directly output data from DSP230 I/O Write Command.
27h (2D4Eh)	REG2D4E	7:0	Default : 0x00 Access : RO
	INC_COUNTER[7:0]	7:0	DSP Sample Counter. SIF PCM output sample counter.
28h (2D50h)	REG2D50	7:0	Default : 0x00 Access : RO
	MAIL_BOX_0[7:0]	7:0	DSP to MCU Mailbox Data.
29h (2D52h)	REG2D52	7:0	Default : 0x00 Access : RO
	MAIL_BOX_1[7:0]	7:0	DSP to MCU Mailbox Data.
2Ah (2D54h)	REG2D54	7:0	Default : 0x00 Access : RO
	MAIL_BOX_2[7:0]	7:0	DSP to MCU Mailbox Data.
2Bh (2D56h)	REG2D56	7:0	Default : 0x00 Access : RO
	MAIL_BOX_3[7:0]	7:0	DSP to MCU Mailbox Data.
2Ch (2D58h)	REG2D58	7:0	Default : 0x00 Access : RO
	MAIL_BOX_4[7:0]	7:0	DSP to MCU Mailbox Data.
2Dh (2D5Ah)	REG2D5A	7:0	Default : 0x00 Access : RO
	MAIL_BOX_5[7:0]	7:0	DSP to MCU Mailbox Data.
2Eh (2D5Ch)	REG2D5C	7:0	Default : 0x00 Access : RO
	MAIL_BOX_6[7:0]	7:0	DSP to MCU Mailbox Data.
2Fh (2D5Eh)	REG2D5E	7:0	Default : 0x00 Access : RO
	MAIL_BOX_7[7:0]	7:0	DSP to MCU Mailbox Data.
30h (2D60h)	REG2D60	7:0	Default : 0x00 Access : RO, R/W
	DWA_RST	7	Reset DWA. 0: Normal.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			1: DWA outputs all ZERO to analog.
	INIT_DATA_SRAM	6	Initial Data SRAM (8051 software control). 0: Normal. 1: Initial time (> 512 * MAC_CLK).
	MAC_OVL	5	MAC is overloaded. 0: Normal. 1: Overloaded.
	MOD_ENABLE	4	Modulator input Test Mode setting. 1: Normal. 0: Input 16h8000 to Modulator.
	DAC_TEST	3	DAC Test Mode. 0: Normal. 1: Test Mode for mass production.
	-	2	Reserved.
	DAC_EN_BIU	1	CH1~4 clock enable. 0: Disable. 1: Enable.
	DSD_IRQ_MASK	0	DSD IRQ Mask.
31h (2D62h)	REG2D62	7:0	Default : 0x00 Access : R/W
	DAC_CH4_MAC_IRQ_MASK	7	CH4 IRQ Mask. 0: IRQ valid. 1: Mask.
	DAC_CH3_MAC_IRQ_MASK	6	CH3 IRQ Mask. 0: IRQ valid. 1: Mask.
	DAC_CH2_MAC_IRQ_MASK	5	CH2 IRQ Mask. 0: IRQ valid. 1: Mask.
	DAC_CH1_MAC_IRQ_MASK	4	CH1 IRQ Mask. 0: IRQ valid. 1: Mask.
	DAC_CH4_FD230_BYPASS	3	CH4 FD230 Bypass Mode (Hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	DAC_CH3_FD230_BYPASS	2	CH3 FD230 Bypass Mode (Hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
	DAC_CH2_FD230_BYPASS	1	CH2 FD230 Bypass Mode (Hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	DAC_CH1_FD230_BYPASS	0	CH1 FD230 Bypass Mode (Hardware). 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
32h (2D64h)	REG2D64	7:0	Default : 0x00 Access : R/W
	ADC1_MAC_IRQ_MASK	7	ADC1 IRQ Mask. 0: IRQ valid. 1: Mask.
	ADC1_FD230_BYPASS	6	ADC1 FD230 Bypass Mode. 0: Normal. 1: Mask FD230 IRQ & hardware bypass.
	-	5:3	Reserved.
	SRC_OSZOH_TEST	2	SRC interpolation function control. 0: Normal (linear interpolation). 1: Sample and hold (disable interpolation).
	SRC_FS_TEST	1	SRC interpolation ratio Selection. 0: Normal SRC Interpolation Mode (8fs to 256fs). 1: SRC Interpolation Test Mode (fs to 256fs).
	ZRMAC_CLKON_ALWAYS	0	0: MAC clock auto power down mode. 1: Disable MAC clock auto power down mode.
33h (2D66h)	REG2D66	7:0	Default : 0x00 Access : R/W
	DWA_SHIFT_DIS	7	Disable DWA's shift function. 0: Normal. 1: Disable.
	DITHER_SEL[1:0]	6:5	Dither energy Selection. DITHER_EXTRA_SEL=0: 00: 1 delta. 01: 2 delta. 10: 1/2 delta. 11: 1/4 delta. DITHER_EXTRA_SEL=1: 00: 1/8 delta. 01: 1/16 delta. 10: 1/32 delta. 11: 1/64 delta.
	SDM_MODE	4	SDM Mode (2nd order).

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			0: 1st order. 1: 2nd order.
	-	3	Reserved.
	DITHER_EXTRA_SEL	2	See "DITHER_SEL".
	DWAOUT_FIX_MID	1	Fix DWA's output. 0: Disable. 1: Enable.
	-	0	Reserved.
34h (2D68h)	REG2D68	7:0	Default : 0x00 Access : RO, R/W
	CLEAR_FIFO_STATUS	7	Clear FIFO Status bits. 0: Normal. 1: Clear FIFO Status.
	FIFO_STATUS_6	6	ADC Right FIFO Status. 0: Balance. 1: Overflow or under-run.
	FIFO_STATUS_5	5	ADC Left FIFO Status. 0: Balance. 1: Overflow or under-run.
	FIFO_STATUS_4	4	DAC CH3 Left FIFO Status. 0: Balance. 1: Overflow or under-run.
	FIFO_STATUS_3	3	DAC CH2 Right FIFO Status. 0: Balance. 1: Overflow or under-run.
	FIFO_STATUS_2	2	DAC CH2 Left FIFO Status. 0: Balance. 1: Overflow or under-run.
	FIFO_STATUS_1	1	DAC CH1 Right FIFO Status. 0: Balance. 1: Overflow or under-run.
	FIFO_STATUS_0	0	DAC CH1 Left FIFO Status. 0: Balance. 1: Overflow or under-run.
35h (2D6Ah)	REG2D6A	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	SEL_ADCOUT	6	Select ADC source for SPDIF/IIS output. 0: Select channel 1.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			1: Select channel 2.
	-	5:1	Reserved.
	DAC2_SEL	0	Analog DAC2 select DWA source. 0: Select source from DWA 2 (channel 2). 1: Select DWA from DWA 1 (channel 1). Note: Channel 2 Left = Sub-woofer / Right = Channel 1 Right.
36h (2D6Ch)	REG2D6C	7:0	Default : 0x00
	-	7:3	Access : R/W Reserved.
	FS_SRC_EN	2	New FS SRC Mode. 0: Disable. 1: Enable.
	CMP_SEL	1	Selection for the compensation filter's coefficient. 0: Default value. 1: Customer setting.
	-	0	Reserved.
37h (2D6Eh)	REG2D6E	7:0	Default : 0x00
	PRI_SEL2[3:0]	7:4	Access : R/W CODEC Filter Priority Selection 2.
	PRI_SEL1[3:0]	3:0	CODEC Filter Priority Selection 1.
38h (2D70h)	REG2D70	7:0	Default : 0x00
	PRI_SEL4[3:0]	7:4	Access : R/W CODEC Filter Priority Selection 4.
	PRI_SEL3[3:0]	3:0	CODEC Filter Priority Selection 3.
39h (2D72h)	REG2D72	7:0	Default : 0x00
	PRI_SEL6[3:0]	7:4	Access : R/W CODEC Filter Priority Selection 6.
	PRI_SEL5[3:0]	3:0	CODEC Filter Priority Selection 5.
3Bh (2D76h)	REG2D76	7:0	Default : 0x00
	-	7:4	Access : R/W Reserved.
	DEBUG_CTRL1	3	Swap DAC4 L & R.
	DEBUG_CTRL2	2	Swap DAC3 L & R.
	DEBUG_CTRL3	1	Swap DAC2 L & R.
	DEBUG_CTRL4	0	Swap DAC1 L & R.
3Fh (2D7Eh)	REG2D7E	7:0	Default : 0x00
	DAC0_INV_LR[7:0]	7:0	Access : R/W [7] DAC FIFO auto reset enable for channel 1, 2, 3 & 4. 0: Disable. 1: Enable. [6] DAC FIFO reset bundle with channel enable.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			0: Disable. 1: Enable. [5:4] Reserved. [3:0] RIU control DAC FIFO manual reset. DAC FIFO channel 1 Reset: (RIU_DACFIFO_RESET[0] == 1) or (DSP_DM_IO418F[0] == 1). DAC FIFO channel 2 Reset: (RIU_DACFIFO_RESET[1] == 1) or (DSP_DM_IO418F[1] == 1). DAC FIFO channel 3 Reset: (RIU_DACFIFO_RESET[2] == 1) or (DSP_DM_IO418F[2] == 1). DAC FIFO channel 4 Reset: (RIU_DACFIFO_RESET[3] == 1) or (DSP_DM_IO418F[3] == 1).
40h (2D80h)	REG2D80	7:0	Default : 0x00 Access : R/W
	CH1_PRESCALE[7:0]	7:0	Pre-scale value for channel 1 gain control. 00h: Off (mute). ... 19h: 0 dB (recommended). ... 7Fh: +14 dB (-0.13725 dB per step).
41h (2D82h)	REG2D82	7:0	Default : 0x00 Access : R/W
	STEREO_SOURCE	7	Audio source setting (combined with CRB1.2). 0: Mono. 1: Stereo.
	SNDEFFECT_ON	6	Sound effect function for channel 1 global control. 0: Disable (software bypass). 1: Enable.
	-	5	Reserved.
	AVC	4	Auto Volume Control function setting. 0: Disable. 1: Enable.
	TONE	3	TONE (Bass/Treble) effect control. 0: Disable. 1: Enable.
	SPATIAL	2	SPATIAL Surround function control.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			0: Disable. 1: Enable. Note: 1) Dependent on bit 7 while enabled. 2) Bit 7 = 0, do mono to stereo. 3) Bit 7 = 1, do surrounding effect.
	VOLUME_BALANCE	1	Volume and Balance function control. 0: Disable. 1: Enable.
	SUBWOOFER	0	Enable SUBWOOFER function. 0: Disable.
42h (2D84h)	REG2D84	7:0	Default : 0x00 Access : R/W
	CH1_GRAPHICEQ	7	Enable CH1 Graphic EQ. 0: Disable. 1: Enable (priority higher than tone effect).
	CH1_LOUDNESS	6	Enable CH1 Loudness. 0: Disable. 1: Enable.
	GEO_BAND_SEL	5	Graphic EQ Band Select. 0: 5-Band EQ. 1: 7-Band EQ.
	-	4	Reserved.
	CH1_LOUDNES_MODE[1:0]	3:2	Loudness mode (valid while 0x2D84[5] = 1). 00: Mode 0 (low slope). 01: Mode 1. 10: Mode 2. 11: Mode 3 (high slope).
	CH1_AVC_MODE[1:0]	1:0	Response Time Selection for Auto Volume Control function. 00: Mode 0 (-20dB/-6dB). 01: Mode 1 (-20dB/-6dB). 10: Mode 2 (-20dB/-6dB). 11: Mode 3 (-20dB/-6dB).
43h (2D86h)	REG2D86	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CH1_BASS[4:0]	4:0	Bass Effect Selection. 0-0000: +00db. 0-0001: +01db. 0-0010: +02db.

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
			0-0011: +03db. 0-0100: +04db. 0-0101: +05db. 0-0110: +06db. 0-0111: +07db. 0-1000: +08db. 0-1001: +09db. 0-1010: +10db. 0-1011: +11db. 0-1100: +12db. 0-1101: +13db. 0-1110: +14db. 0-1111: +15db. 1-0000: -16db. 1-0001: -15db. 1-0010: -14db. 1-0011: -13db. 1-0100: -12db. 1-0101: -11db. 1-0110: -10db. 1-0111: -09db. 1-1000: -08db. 1-1001: -07db. 1-1010: -06db. 1-1011: -05db. 1-1100: -04db. 1-1101: -03db. 1-1110: -02db. 1-1111: -01db.	
44h (2D88h)	REG2D88	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_TREBLE[4:0]	4:0	Treble Effect Selection. 0-0000: +00db. 0-0001: +01db. 0-0010: +02db. 0-0011: +03db. 0-0100: +04db. 0-0101: +05db. 0-0110: +06db. 0-0111: +07db.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			0-1000: +08db. 0-1001: +09db. 0-1010: +10db. 0-1011: +11db. 0-1100: +12db. 0-1101: +13db. 0-1110: +14db. 0-1111: +15db. 1-0000: -16db. 1-0001: -15db. 1-0010: -14db. 1-0011: -13db. 1-0100: -12db. 1-0101: -11db. 1-0110: -10db. 1-0111: -09db. 1-1000: -08db. 1-1001: -07db. 1-1010: -06db. 1-1011: -05db. 1-1100: -04db. 1-1101: -03db. 1-1110: -02db. 1-1111: -01db.
45h (2D8Ah)	REG2D8A	7:0	Default : 0x01
	-	7:6	Reserved.
	CH1_MONO2STEREO_MODE[1:0]	5:4	Mode Selection for Mono to Stereo. 00: Virtual 40 degree source. 01: Virtual 20 degree source. 10: Virtual -20 degree source. 11: Virtual -40 degree source.
	-	3:2	Reserved.
	CH1_SURROUND_MODE[1:0]	1:0	Mode Selection for Surround. 00: Mountain Mode. 01: Champaign Mode. 10: City Mode. 11: Theater Mode.
46h (2D8Ch)	REG2D8C	7:0	Default : 0x81
	CH1_SOFTMUTE	7	Software Mute Channel 1.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			0: Normal. 1: Mute.
	CH1_VOLUME[6:0]	6:0	Volume control. Gain setting = 12db _ N*1.0 dB (+12db ~ -114db). N = 0 ~ 11 (+12 ~ +1db). N = 12 (0db). N = 13 ~ 126 (-1 ~ -114db). N = 127, mute.
47h (2D8Eh)	REG2D8E	7:0	Default : 0x00
	-	7:4	Reserved.
	CH1_BALANCE[3:0]	3:0	Left channel attenuation level. 0000: 0 db. 0001: -1 db. 0010: -2 db. 0011: -3 db. 0100: -4 db. 0101: -5 db. 0110: -6 db. 0111: -7 db. 1000: -8 db. 1001: -9 db. 1010: -10 db. 1011: -11 db. 1100: -12 db. 1101: -13 db. 1110: -14 db. 1111: Mute.
48h (2D90h)	REG2D90	7:0	Default : 0x00
	-	7:4	Reserved.
	CH1_BALANCER[3:0]	3:0	Right channel attenuation level. 0000: 0 db. 0001: -1 db. 0010: -2 db. 0011: -3 db. 0100: -4 db. 0101: -5 db. 0110: -6 db. 0111: -7 db. 1000: -8 db.

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
			1001: -9 db. 1010: -10 db. 1011: -11 db. 1100: -12 db. 1101: -13 db. 1110: -14 db. 1111: Mute.	
49h (2D92h)	REG2D92	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	CH1_SUBWOOFER[3:0]	3:0	Cut-frequency Selection for Sub-woofer. 0000: 50 Hz. 0001: 100 Hz. 0010: 150 Hz. 0011: 200 Hz. 0100: 250 Hz. 0101: 300 Hz. 0110: 350 Hz. 0111: 400 Hz. 1000: 450 Hz. 1001: 500 Hz. 1010: 550 Hz. 1011: 600 Hz. 1100: 650 Hz. 1101: 700 Hz. 1110: 750 Hz. 1111: 800 Hz.	
4Ah (2D94h)	REG2D94	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND1 [4:0]	4:0	Center frequency is 120Hz. 00000: -12 db. 00001: -11 db. 00010: -10 db. 00011: - 9 db. 00100: - 8 db. 00101: - 7 db. 00110: - 6 db. 00111: - 5 db. 01000: - 4 db. 01001: - 3 db.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
			01010: - 2 db. 01011: - 1 db. 01100: 0 db. 01101: 1 db. 01110: 2 db. 01111: 3 db. 10000: 4 db. 10001: 5 db. 10010: 6 db. 10011: 7 db. 10100: 8 db. 10101: 9 db. 10110: 10 db. 10111: 11 db. 11000: 12 db.	
4Bh (2D96h)	REG2D96	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND2 [4:0]	4:0	Center frequency is 500Hz. Gain setting is the same as 0xBA.	
4Ch (2D98h)	REG2D98	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND3 [4:0]	4:0	Center frequency is 1.5KHz. Gain setting is the same as 0xBA.	
4Dh (2D9Ah)	REG2D9A	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND4 [4:0]	4:0	Center frequency is 5KHz. Gain setting is the same as 0xBA.	
4Eh (2D9Ch)	REG2D9C	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CH1_GRAPHIC_EQ_BAND5 [4:0]	4:0	Center frequency is 10KHz. Gain setting is the same as 0xBA.	
50h (2DA0h)	REG2DA0	7:0	Default : 0x00	Access : R/W
	CH2_SOFTMUTE	7	Software Mute Channel 2. 0: Normal. 1: Mute.	
	-	6	Reserved.	
	CH3_SOFTMUTE	5	Software Mute Channel 3.	

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: Normal. 1: Mute.	
	-	4	Reserved.	
	CH4_SOFTMUTE	3	Software Mute Channel 4. 0: Normal. 1: Mute.	
	-	2:0	Reserved.	
51h (2DA2h)	REG2DA2	7:0	Default : 0x00	Access : R/W
	CH2_PRESCALE[7:0]	7:0	Pre-scale value for channel 2 gain control. 00h: Off (mute). ... 19h: 0 dB (recommended). ... 7Fh: +14 dB (-0.13725 dB per step).	
52h (2DA4h)	REG2DA4	7:0	Default : 0x00	Access : R/W
	CH3_PRESCALE[7:0]	7:0	Pre-scale value for channel 3 gain control. 00h: Off (mute). ... 19h: 0 dB (recommended). ... 7Fh: +14 dB (-0.13725 dB per step).	
53h (2DA6h)	REG2DA6	7:0	Default : 0x00	Access : R/W
	CH4_PRESCALE[7:0]	7:0	Pre-scale value for channel 4 gain control. 00h: Off (mute). ... 19h: 0 dB (recommended). ... 7Fh: +14 dB (-0.13725 dB per step).	
54h (2DA8h)	REG2DA8	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CH1_VOLUME_FRAC[2:0]	6:4	Fraction volume control of CH1. Gain setting = 0.125db * N (0~0.875db). N = 000, 0db. N = 001, 0.125db. N = 010, 0.250db. N = 011, 0.375db. N = 100, 0.500db. N = 101, 0.625db.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			N = 110, 0.750db. N = 111, 0.875db.
	-	3:0	Reserved.
56h (2DACH)	REG2DAC	7:0	Default : 0x00 Access : R/W
	CH1_DAC_POWER_DOWN	7	DAC power down enable. 0: Normal mode. 1: Power down mode.
	CH1_SWITCH_SOURCE	6	Channel switch. 0: Channel not switched. 1: Channel switched.
	CH2_DAC_POWER_DOWN	5	DAC power down enable. 0: Normal mode. 1: Power down mode.
	CH2_SWITCH_SOURCE	4	Channel switch. 0: Channel not switched. 1: Channel switched.
	CH3_DAC_POWER_DOWN	3	DAC power down enable. 0: Normal mode. 1: Power down mode.
	CH3_SWITCH_SOURCE	2	Channel switch. 0: Channel not switched. 1: Channel switched.
	CH4_DAC_POWER_DOWN	1	DAC power down enable. 0: Normal mode. 1: Power down mode.
	CH4_SWITCH_SOURCE	0	Channel switch. 0: Channel not switched. 1: Channel switched.
57h (2DAEH)	REG2DAE	7:0	Default : 0x00 Access : R/W
	FM_RESERVED_REG[7:0]	7:0	For firmware application.
60h (2DC0h)	REG2DC0	7:0	Default : 0x00 Access : RO
	-	7:5	Reserved.
	DSP_DAC_CURRENT[4:0]	4:0	Audio DAC Current Selection (L/R/LFE). 0-0000: Minimum current. ... 1-1111: Maximum current.
61h	REG2DC2	7:0	Default : 0x00 Access : RO

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
(2DC2h)	DSP_FD230_CODE_VER[7:0]	7:0	DSP FD230 code version.
64h (2DC8h)	REG2DC8	7:0	Default : 0x00 Access : RO
	EN_AUDIO_L_VMID	7	Enable control of L-channel Vmid buffer. 0: Power-down L-channel Vmid buffer. 1: Power-up L-channel Vmid buffer.
	EN_AUDIO_S_VMID	6	Enable control of S-channel Vmid buffer. 0: Power-down of S-channel Vmid buffer. 1: Power-up of S-channel Vmid buffer.
	EN_AUDIO_R_BUFFER	5	Enable control of R-channel Output buffer. 0: Power-down R-channel Output buffer. 1: Power-up R-channel Output buffer.
	EN_AUDIO_L_BUFFER	4	Enable control of L-channel Output buffer. 0: Power-down L-channel Output buffer. 1: Power-up L-channel Output buffer.
	EN_AUDIO_S_BUFFER	3	Enable control of LFE-channel Output buffer. 0: Power-down LFE-channel Output buffer. 1: Power-up LFE-channel Output buffer.
	EN_AUDIO_VREF	2	Enable control of Vref generator. 0: Power-down Vref generator. 1: Power-up Vref generator.
	EN_AUDIO_VREF_BIAS	1	Enable control of bias current generator. 0: Power-down bias current generator. 1: Power-up bias current generator.
	EN_AUDIO_BANDGAP	0	Enable control of audio bandgap. 0: Power-down audio bandgap. 1: Power-up audio bandgap.
65h (2DCAh)	REG2DCA	7:0	Default : 0x00 Access : RO
	-	7:5	Reserved.
	EN_AUDIO_I_REF	4	Enable control of audio current mirror. 0: Power-down audio current mirror. 1: Power-up audio current mirror.
	-	3:2	Reserved.
	EN_AUDIO_DAC_BIAS	1	Enable control of audio DAC bias circuit. 0: Power-down audio DAC bias circuit. 1: Power-up audio DAC bias circuit.
	EN_AUDIO_R_VMID	0	Enable control of R-channel Vmid buffer.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			0: Power-down R-channel Vmid buffer. 1: Power-up R-channel Vmid buffer.
67h (2DCEh)	REG2DCE	7:0	Default : 0x00 Access : RO, R/W
	CH1_DWA_RST	7	Reset DWA. 0: Normal. 1: DWA outputs all ZERO to analog.
	CH1_DAC_CLK_ENABLE	6	DAC clock gate. 0: Normal. 1: Enable DAC clock.
	CH1_FORCE_2ND_ORDER	5	Modulator Order. 0: 1st Order. 1: 2nd Order.
	CH1_DAC_MODULATOR_ENABLE	4	DAC modulation enable. 0: Enable. 1: Disable.
	CH2_DWA_RST	3	Reset DWA. 0: Normal. 1: DWA outputs all ZERO to analog.
	CH2_DAC_CLK_ENABLE	2	DAC clock gate. 0: Normal. 1: Enable DAC clock.
	CH2_FORCE_2ND_ORDER	1	Modulator Order. 0: 1st Order. 1: 2nd Order.
	CH2_DAC_MODULATOR_ENABLE	0	DAC modulation enable. 0: Enable. 1: Disable.
68h (2DD0h)	REG2DD0	7:0	Default : 0x00 Access : RO, R/W
	CH3_DWA_RST	7	Reset DWA. 0: Normal. 1: DWA outputs all ZERO to analog.
	CH3_DAC_CLK_ENABLE	6	DAC clock gate. 0: Normal. 1: Enable DAC clock.
	CH3_FORCE_2ND_ORDER	5	Modulator Order. 0: 1st Order. 1: 2nd Order.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
	CH3_DAC_MODULATOR_ENABLE	4	DAC modulation enable. 0: Enable. 1: Disable.
	CH4_DWA_RST	3	Reset DWA. 0: Normal. 1: DWA outputs all ZERO to analog.
	CH4_DAC_CLK_ENABLE	2	DAC clock gate. 0: Normal. 1: Enable DAC clock.
	CH4_FORCE_2ND_ORDER	1	Modulator Order. 0: 1st Order. 1: 2nd Order.
	CH4_DAC_MODULATOR_ENABLE	0	DAC modulation enable. 0: Enable. 1: Disable.
70h (2DE0h)	REG2DE0	7:0	Default : 0x00 Access : R/W
	AUD_RST_MAD	7	Reset MPEG Audio Decoder Module. 0: Normal. 1: Software reset MAD module.
	AUD_DIS_DMA	6	Disable MIU DMA request. 0: Normal. 1: Disable (stop accessing DRAM).
	AUD_CLR_FIFO_STA	5	Clear ES/PCMI/PCMO FIFO Status (combined with DSP). 0: Normal. 1: Clear.
	AUD_SEL	4	0: MPEG. 1: AC3.
	-	3:1	Reserved.
	AUD_MADBASE_SEL	0	MCU sets this bit to identify whether MCU or DSP is to configure MAD_OFFSET_BASE. 0: MCU. 1: DSP.
70h (2DE1h)	REG2DE1	7:0	Default : 0x00 Access : RO, R/W
	CTRL_15	7	ES1_MLINK_MODE, M-link allows for modification of ES1_CNT.
	CTRL_14	6	ES2_MLINK_MODE, M-link allows for modification of ES2_CNT.

AUDIO1 Register (Bank = 2D)				
Index (Absolute)	Mnemonic	Bit	Description	
	CTRL_13	5	MCU1_ES1_MODE, MCU1 allows for modification of ES1_CNT.	
	CTRL_12	4	MCU2_ES2_MODE, MCU2 allows for modification of ES1_CNT.	
	AUD_ES1R_STA	3	ES1R channel status. 0: Idle. 1: Ongoing.	
	AUD_MASK_ES1R	2	CPU mask DSP doing ES1R. 0: Normal. 1: Mask ES1R.	
	AUD_RST_PAS	1	MIPS reset Audio PAS. 0: Normal. 1: Software reset Audio PAS.	
	AUD_SEL_INTR	0	Select interrupt PIO[7] interrupt source. 0: Stream type change. 1: SAR detect.	
71h (2DE2h)	REG2DE2	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	STR_TYPE	0	DVB audio stream type, to DSP.	
72h (2DE4h)	REG2DE4	7:0	Default : 0x00	Access : R/W
	MAD_OFFSET_BASE[7:0]	7:0	MAD memory (including ES, SIF and PCM) buffer base[31:16].	
72h (2DE5h)	REG2DE5	7:0	Default : 0x00	Access : R/W
	MAD_OFFSET_BASE[15:8]	7:0	See description of '2DE4h'.	
73h (2DE6h)	REG2DE6	7:0	Default : 0x00	Access : R/W
	MBASE[7:0]	7:0	Indirect configuration memory buffer base[23:16]. Must set MEM_CFG first.	
74h (2DE8h)	REG2DE8	7:0	Default : 0xFF	Access : R/W
	MSIZE_H[7:0]	7:0	Indirect configuration memory buffer end [15:8]. Must set MEM_CFG first. Memory buffer end [7:0] = 0xff. Actual buffer size = MSIZE + 1.	
75h (2DEAh)	REG2DEA	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	MEM_CFG[2:0]	2:0	Indirect configured 0x03 and 0x04 memory space. 000: SIF-ch1 memory configuration. 001 =SIF-ch2 memory configuration. 010: ES-ch1 memory configuration.	

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			011: ES-ch2 memory configuration. 100: PCM-ch1 memory configuration. 101: PCM-ch2 memory configuration. 11x: DSP data memory configuration.
76h (2DECh)	REG2DEC	7:0	Default : 0xFF Access : R/W
	P_AUD_OUT_MODE[1:0]	7:6	DVB audio PCM output mode. 00: Stereo. 01: Left Channel. 10: Right Channel. 11: Mute.
	P_AUD_TYPE	5	1: Free run. 0: AV sync.
	P_AUD_MODE_CMD[4:0]	4:0	System command. 0-0000: Stop (mute). 0-0001: Play. 0-0010: Play file (MHEG5/MP3). Others: Reserved.
77h (2DEEh)	REG2DEE	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	DSPDMA_CMD_STA	5	Command/Status. 0: Idle/Finish. 1: Assert to start DMA, auto-clear when work is finished.
	DSPDMA_CLR_CNT	4	Clear memory counter. Clear read/write pointer. Update DMA address to base address.
	DSPDMA_SET_PRIORITY	3	MIU Priority. 0: Low priority. 1: High priority.
	DSPDMA_WIDTH_SEL	2	Data width. 0: 16 bits. 1: 24 bits.
	DSPDMA_BURST_LENGTH[1:0]	1:0	Burst length. 00: Reserved. 01: 2 * 64 bits. 10: 3 * 64 bits. 11: 6 * 64 bits. In 24-bit mode, it must align to 3 burst length.
78h	REG2DF0	7:0	Default : 0x00 Access : R/W

AUDIO1 Register (Bank = 2D)			
Index (Absolute)	Mnemonic	Bit	Description
(2DF0h)	DSPDMA_MIU_ADDR[7:0]	7:0	MIU start address for DMA transfer. Auto-increasing when DMA is working. Auto-wrap to base address when counting to end address.
78h (2DF1h)	REG2DF1	7:0	Default : 0x00
	DSPDMA_MIU_ADDR[15:8]	7:0	See description of '2DF0h'.
79h (2DF2h)	REG2DF2	7:0	Default : 0x00
	DSPDMA_DSP_ADDR[7:0]	7:0	IDMA address IAD.
79h (2DF3h)	REG2DF3	7:0	Default : 0x00
	DSPDMA_DSP_RW	7	DSP IDMA read/write DRAM. 0: Read. 1: Write.
	DSPDMA_DSP_MEM_SEL	6	DSP IDMA start address for DMA transfer. Auto-increasing when DMA is working. 0: Select PM / CM. 1: Select DM.
	DSPDMA_DSP_ADDR[13:8]	5:0	See description of '2DF2h'.
7Ah (2DF4h)	REG2DF4	7:0	Default : 0x00
	DSPDMA_DMA_SIZE[7:0]	7:0	DMA transfer size in unit of 128 bits. It must align to burst length.
7Ah (2DF5h)	REG2DF5	7:0	Default : 0x00
	-	7:4	Reserved.
	DSPDMA_DMA_SIZE[11:8]	3:0	See description of '2DF4h'.
7Bh (2DF6h)	REG2DF6	7:0	Default : 0x00
	-	7:2	Reserved.
	DSPDMA_CFG[1:0]	1:0	0x58F7 ~ 0x58FA configuration. 00: DMA1. 01: DMA2. 10: DMA3. 11: DMA4.
7Ch (2DF8h)	REG2DF8	7:0	Default : 0x00
	ES1_CNT[7:0]	7:0	Allow CPU to control ES1 MIU counter. Steps are as follows: 1: Mask DSP ES1 read (AUD_CTRL[10]). 2: Double read and check ES1R status (AUD_CTRL[11]). 3: Read ES1_CNT. 4: Modify it and write back.

AUDIO1 Register (Bank = 2D)

Index (Absolute)	Mnemonic	Bit	Description
			5: Unmask ES1 read.
7Ch (2DF9h)	REG2DF9	7:0	Default : 0x00
	ES1_CNT[15:8]	7:0	See description of '2DF8h'.
7Dh (2DFAh)	REG2DFA	7:0	Default : 0x00
	-	7:5	Reserved.
	AD_CFG[2:0]	4:2	Indirect access select. 0: AD_BUF_BASE[23:8]. 1: AD_BUF_BASE[7:0]. 2: AD_BUF_SIZE[15:0]. 3: AD_SUB_ES2_CNT[7:0]. 4: AD_ADD_AD_CNT[7:0].
	ES2_CNT_MASK	1	MIPS read ES2_CNT, must be masked first to avoid meta-stable issue.
	AD_MODE	0	Audio Description Mode Enable.
7Eh (2DFCh)	REG2DFC	7:0	Default : 0x00
	INDIR_WR_DATA[7:0]	7:0	Indirect Write Data when writing OP, or. Indirect Read Data when reading OP.
7Eh (2DFDh)	REG2DFD	7:0	Default : 0x00
	INDIR_WR_DATA[15:8]	7:0	See description of '2DFCh'.
7Fh (2DFEh)	REG2DFE	7:0	Default : 0x00
	ES2_CNT[7:0]	7:0	ES2_CNT for AD mode.
7Fh (2DFFh)	REG2DFF	7:0	Default : 0x00
	ES2_CNT[15:8]	7:0	See description of '2DFEh'.

IPMUX Register (Bank = 2E)

IPMUX Register (Bank = 2E)				
Index (Absolute)	Mnemonic	Bit	Description	
01h (2E02h)	REG2E02	7:0	Default : 0x00	Access : R/W
	IPMUX_SEL2[3:0]	7:4	Input source select. 0: ADC A. 1: DVI_1. 2: VD. 7: Capture. Others: Debug mode.	
	-	3:0	Reserved.	
01h ~ 1Fh (2E03h ~ 2E3Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	

Scaler 1 Register (Bank = 2F)

GOP_INT Register (Bank = 2F, Sub-Bank =00)

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]:. SWRST1[4]: IP, include F1 and F2. SWRST1[3]: OP include OP1, VIP and VOP. SWRST1[2]: IP_F2.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
			SWRST1[1]: IP_F1. SWRST1[0]: All engines.
03h (2F06h)	REG2F06	7:0	Default : 0x00
	-	7:2	Reserved.
	PDMD[1:0]	1:0	PowerDown mode:. 01: IDCLK. Others: IDCLK and ODCLK.
04h (2F08h)	REG2F08	7:0	Default : 0x00
	-	7:2	Reserved.
	VSINT_EDGE	1	OP2 VS INT Edge. 1: Tailing. 0: Leading.
	IPVSINT_EDGE	0	IP VS INT Edge. 1: Tailing. 0: Leading.
04h (2F09h)	REG2F09	7:0	Default : 0x00
	-	7:1	Reserved.
	CHG_HMD	0	CHG_HMD: H Change Mode for INT. 0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00
	IP_SYNC_TO_GOP_SEL[1:0]	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.
	GOP2IP_EN	5	GOP blending to IP enable.
	-	4:0	Reserved.
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00
	-	7:6	Reserved.
	GOP2IP_DATA_SEL[1:0]	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.
	-	3:0	Reserved.
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00
	COP_EN	7	Enable cop for VOP2.
	GOP2_EN	6	Enable GOP_2 for VOP2.

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	Mnemonic	Bit	Description	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS_7_0[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (2F22h)	REG2F22	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : RO
	IRQ_FINAL_STATUS_31_24[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	Mnemonic	Bit	Description	
			D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : R/W
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : R/W
	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
13h	REG2F27	7:0	Default : 0x00	Access : R/W

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F27h)	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (2F28h)	REG2F28	7:0	Default : 0xFF	Access : R/W
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
14h (2F29h)	REG2F29	7:0	Default : 0xFF	Access : R/W
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0xFF	Access : R/W
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
15h (2F2Bh)	REG2F2B	7:0	Default : 0xFF Access : R/W
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00 Access : R/W
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00 Access : R/W
	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00 Access : R/W
	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1.

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	Mnemonic	Bit	Description	
			D[0]: IPHCs1_DET_INT_F2.	
17h (2F2Fh)	REG2F2F	7:0	Default : 0x00	Access : R/W
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (2F30h)	REG2F30	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS_7_0[7:0]	7:0	The raw status of interrupt source. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
18h (2F31h)	REG2F31	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS_15_8[7:0]	7:0	The raw status of interrupt source. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
19h (2F32h)	REG2F32	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS_23_16[7:0]	7:0	The raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)				
Index (Absolute)	Mnemonic	Bit	Description	
			D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
19h (2F33h)	REG2F33	7:0	Default : 0x00	Access : RO
	IRQ_RAW_STATUS_31_24[7:0]	7:0	The raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : RO
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (2F41h)	REG2F41	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	See description of '2F40h'.	
21h (2F42h)	REG2F42	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : RO
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (2F45h)	REG2F45	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '2F44h'.	
23h (2F46h)	REG2F46	7:0	Default : 0x00	Access : RO
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '2F46h'.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : RO
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	

GOP_INT Register (Bank = 2F, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
	BIST_FAIL_4[13:8]	5:0	See description of '2F48h'.
33h (2F66h)	REG2F66	7:0	Default : 0xE1 Access : R/W
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.
33h (2F67h)	REG2F67	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	WDT_EN	0	H/V sync lose watch dog timer count enable.

IP1_M Register (Bank = 2F, Sub-Bank =01)

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
02h (2F04h)	REG2F04	7:0	Default : 0x83	Access : R/W
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.	
	CSC_EN	3	Input CSC function. 0: Disable (RGB -> RGB, default). 1: Enable (RGB -> YCbCr).	

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	Mnemonic	Bit	Description	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: HDTV. 111: HDMI.	
02h (2F05h)	REG2F05	7:0	Default : 0x00	Access : R/W
	FVDO_DIVSEL	7	Force Input Clock Divide Function. 0: Disable (Auto selected by h/W, used when input is video, default). 1: Enable (use 02h[14:12] as divider).	
	-	6	Reserved.	
	VD_PORT_SEL	5	External VD Port. 0: Port 0. 1: Port 1.	
	VD_ITU	4	VD ITU656 out, and Digital In for scaler.	
	VDEXT_SYNMD	3	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Format.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. 00: External 8/10 bits video port. 01: Internal video decoder mode A. 10: External 16/20 bits video port. 11: Internal video decoder mode B.	
03h (2F06h)	REG2F06	7:0	Default : 0x18	Access : R/W
	DIRECT_DE	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. 0: Delay 1/4 input HSYNC.	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
			1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. 0: Disable. 1: Enable.	
	HWRAP	0	Input image Horizontal wrap. 0: Disable. 1: Enable.	
03h (2F07h)	REG2F07	7:0	Default : 0x80	Access : R/W
	FRCV	7	Source Sync Enable. 1: Display will adaptive follow the Source. If Display Select this source. 0: Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change. The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	FREE_FOLLOW	5	No memory bank control (used when FRCV=1).	
	FRC_FREEMD	4	Force output odd/even toggle when. 2DDi for interlace input..	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	RESERVED	0		
04h (2F08h)	REG2F08	7:0	Default : 0x01	Access : R/W
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	See description of '2F08h'.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x01	Access : R/W
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	See description of '2F0Ah'.	
06h (2F0Ch)	REG2F0C	7:0	Default : 0x10	Access : R/W
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_VDC[10:8]	2:0	See description of '2F0Ch'.	
07h (2F0Eh)	REG2F0E	7:0	Default : 0x10	Access : R/W
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (2F0Fh)	REG2F0F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	SPRANGE_HDC[10:8]	2:0	See description of '2F0Eh'.	
08h (2F10h)	REG2F10	7:0	Default : 0x20	Access : R/W
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. 0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. 0: Mask. 1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC).	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. 1: Use Hsync only. When ISEL = 011:(DVI). 0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). 0: Normal. 1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. 0: Normal. 1: MSB/LSB swap.	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. 0: Use Separate Hs for Coast Period. 1: Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. 0: Leading edge. 1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. 0: Auto Switch VST(04), VDC (06). 1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. 0000: 8 Line Ahead from SPRange_Vst.	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
			0001: 1 Line Ahead from SPRange_Vst. 0010: 2 Line Ahead from SPRange_Vst. 0011: 3 Line Ahead from SPRange_Vst. .. 1111: 15 Line Ahead from SPRange_Vst.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Bh (2F17h)	REG2F17	7:0	Default : 0x00	Access : R/W
	H_MIR	7	H Mirror Enable.	
	-	6:0	Reserved.	
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (2F19h)	REG2F19	7:0	Default : 0x00	Access : R/W
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. 0: HW Auto Decide. 1: SW Program.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00	Access : R/W
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5 tap support. 1: Down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5 tap. 1: 2 to 1 down, 11 tap. else: Reserved. For ExtVD is CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00	Access : RO, R/W
	ATG_HIR	7	Max value flag for R channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_Data_MD = 0.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	Mnemonic	Bit	Description	
			Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. 0: Disable. 1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATG_En = 0).	
	ATG_READY	1	Auto Gain Result Ready. 0: Result not ready. 1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. 0: Disable. 1: Enable.	
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00	Access : RO, R/W
	ATG_10BIT	7	Auto gain 10bits mode.	
	AV_DET	6	AV Detect for Cb Cr. 0: CbCr Range is define by 03[2]. YCbCr_En. 1: Cb Cr Min is define in 89 ATP_GTH. Cb Cr Max is define in 8A ATP_TH.	
	-	5:3	Reserved.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	Mnemonic	Bit	Description	
	ATG_UPR	2	Min value flag for R channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. 0: Normal. 1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x00	Access : R/W
	AUTO_COAST	7	Auto Coast enable when mode change. 0: Disable. 1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). 0: Coast is inactive. 1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. 1. VD. 2. Ext VD 656 Format. 3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. 000: Minimum R value. 001: Minimum G value. 010: Minimum G value.	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
			011: Maximum R value. 100: Maximum G value. 101: Maximum B value. 11x: Reserved.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : RO, R/W
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: Right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. 0: Not clear. 1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. 0: Update every frame. 1: Keep the history value.	
	JITTER	3	JITTER function Result. 0: No JITTER. 1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. 0: Result ready. 1: Result not ready.	
	ATS_EN	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	THOLD[3:0]	7:4	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. &. 1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
	ATS_PIXMD	0	Auto Position Force Pixel Mode. 0: DE or Pixel decide by the Source. 1: Force Pixel Mode.	
11h (2F22h)	REG2F22	7:0	Default : 0x00	Access : RO
	ATGSEL_VALUE[7:0]	7:0	Auto Gain Value. (selected by register 0Fh[2:0]).	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : RO
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '2F22h'.	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : RO
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	ATS_VSTDBUF[10:8]	2:0	See description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : RO
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (2F27h)	REG2F27	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	ATS_HSTDBUF[11:8]	3:0	See description of '2F26h'.	
14h (2F28h)	REG2F28	7:0	Default : 0x00	Access : RO
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (2F29h)	REG2F29	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	ATS_VEDDBUF[10:8]	2:0	See description of '2F28h'.	
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00	Access : RO
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	ATS_HEDDBUF[11:8]	3:0	See description of '2F2Ah'.	
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00	Access : RO
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h	REG2F2D	7:0	Default : 0x00	Access : RO

IP1_M Register (Bank = 2F, Sub-Bank = 01)			
Index (Absolute)	Mnemonic	Bit	Description
(2F2Dh)	-	7:4	Reserved.
	REG_JLST[11:8]	3:0	See description of '2F2Ch'.
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	L12_LIMIT_EN	5	Background Noise reduction Enable. 0: Disable. 1: Enable.
	HIPX_LIMIT_EN	4	High level Noise reduction Enable. 0: Disable. 1: Enable.
	-	3	Reserved.
	PIX_TH[2:0]	2:0	Auto Noise Level. 111: Noise level = 16.
18h (2F30h)	REG2F30	7:0	Default : 0x01 Access : R/W
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.
18h (2F31h)	REG2F31	7:0	Default : 0x10 Access : R/W
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24].
19h (2F32h)	REG2F32	7:0	Default : 0x00 Access : RO, R/W
	-	7	Reserved.
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).
	ATP_TXT	5	Auto Phase Text detect (Read Only).
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.
	ATP_READY	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.
	ATP_EN	0	Auto Phase function Enable. 0: Disable.

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description
			1: Enable.
1Ah (2F34h)	REG2F34	7:0	Default : 0x00
	ATP[7:0]	7:0	Auto Phase Value.
1Ah (2F35h)	REG2F35	7:0	Default : 0x00
	ATP[15:8]	7:0	See description of '2F34h'.
1Bh (2F36h)	REG2F36	7:0	Default : 0x00
	ATP[23:16]	7:0	See description of '2F34h'.
1Bh (2F37h)	REG2F37	7:0	Default : 0x00
	ATP[31:24]	7:0	See description of '2F34h'.
1Ch (2F38h)	REG2F38	7:0	Default : 0x00
	LB_TUNE_READY	7	Input VSYNC Blanking Status. 0: In display. 1: In blanking.
	DELAYLN_NUM[2:0]	6:4	Delay Line After Sample V Start for Input Trigger Point.
	-	3:2	Reserved.
	UNDERRUN	1	Under run status for FIFO.
	OVERRUN	0	Over run status for FIFO.
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x05
	-	7	Reserved.
	DE_LOCKH_MD	6	DE Lock H Postion Mode.
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. 5: Default value.
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x01
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Separator.
	HTT_FILTERMD	5	Auto No signal Filter mode. 0: Disable. 1: Enable (update Htt after 4 sequential lines over tolerance).
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. 1: Default value.
1Eh	REG2F3C	7:0	Default : 0x00

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description
(2F3Ch)	SOG_OFFMUX[1:0]	7:6	Off Line SOG source select. 00: Select analog 1 SOG. 01: Select analog 2 SOG. 10: Select analog 3 SOG.
	IPHCS0_ACT	5	Analog 1 HSYNC Pin Active.
	IPHCS1_ACT	4	Analog 2 HSYNC Pin Active.
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00 Access : RO
	IPVS_ACT	7	Input On Line Source VSYNC Active. 0: Not active. 1: Active.
	IPHS_ACT	6	Input On Line Source HSYNC Active. 0: Not active. 1: Active.
	CS_DET	5	Composite Sync Detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.
	SOG_DET	4	Sync-On-Green Detected status. 0: Input is not SOG. 1: Input is detected as SOG.
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.
	FIELD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00	Access : R/W
	VTT[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00	Access : R/W
	VS_PW_VDOMD	7	VSYNC Raw Pulse Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	-	4:3	Reserved.	
	VTT[10:8]	2:0	See description of '2F3Eh'.	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (2F41h)	REG2F41	7:0	Default : 0x00	Access : R/W
	LN4_DETMD	7	Input HSYNC period Detect Mode. 0: 1 line. 1: 8 lines.	
	TEST_CSHTT	6	Report Sync Separator Htt by E5, E4. 0: Htt Report by Mode Detector. 1: Htt Report by Sync Separator.	
	HTT_FOR_READ[13:8]	5:0	See description of '2F40h'.	
21h (2F42h)	REG2F42	7:0	Default : 0x00	Access : R/W
	FIELD_SWMD	7	Shift Line Method When Field Switch. 0: Old method. 1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1.	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: Active low. 1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_VsPol).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD = 1. 0: Active low. 1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (Usr_IntLac).	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. 00: Sample V End. 01: Sample V Start. 10: Sample V Start Ahead by Current Bank 09[3:0]. 11: Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. 0: Mode Change Provide in data clock Domain. 1: Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. 0: Form Input DE. 1: From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. 0: Normal. 1: Invert.	
	EXT_FIELDMD	2	Video External Field. 0: Use result of internal circuit detection.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	Mnemonic	Bit	Description	
			1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. 0: Normal. 1: Invert.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : RO
	HSPW[7:0]	7:0	Pulse Width Report. If Current Bank HSPW_sel (1F[13]) = 0, Report HSYNC. If Current Bank HSPW_sel (1F[13]) = 1, Report VSYNC.	
23h (2F46h)	REG2F46	7:0	Default : 0x1E	Access : R/W
	DVICK_WIDTH[7:0]	7:0	DVI clock detection threshold, see Cah for usage (default 0x1E). Cah[6] = 0: DVI clock is OK, Freq(DVI) > Freq(xtal) * 23h/128. Cah[6] = 1: DVI clock is missing, Freq(DVI) < Freq(xtal) * 23h/128. Where Ebh default to 0x1E(30).	
23h (2F47h)	REG2F47	7:0	Default : 0x00	Access : RO, R/W
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (2F48h)	REG2F48	7:0	Default : 0x00	Access : R/W
	VS_SEP_SEL	7	SYNC Separator VSYNC for Mode Detect. 0: RAW VSYNC (H / V Relationship is Keep for Interlace Detect). 1: HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = . 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select.	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: PC Source. 1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = . 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). 0: Disable. 1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. 0: Internal Separated VSYNC.(Default). 1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. &. 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. &. 254: Coast end at 255 HSYNC leading edge. 255: Coast end at 256 HSYNC leading edge.	
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00	Access : R/W
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. 0: Disable. 1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range.	

IP1_M Register (Bank = 2F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description
			Analog: 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI: 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPV _s _Act, IPH _s _Act (E1[7:6]). (recommend).
	IDCLK_INV	0	Capture Port Sample CLK Invert. 0: Normal. 1: Invert.
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00 Access : R/W
	AFT	7	ATP Filter for Text (4 frames). 0: Disable. 1: Enable.
	IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.
	VSGR	5	VSYNC glitch removal with line less than 2 (DE Only). 0: Disable. 1: Enable.

IP1_M Register (Bank = 2F, Sub-Bank = 01)				
Index (Absolute)	Mnemonic	Bit	Description	
	VSP	4	VSYNC Protect with V total (DE Only). 0: Disable. 1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable. 1: Enable.	
	-	1:0	Reserved.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : RO, R/W
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. 00: Off. 01: Only for line total number is even. 10: All case. 11: Off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : RO, R/W
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. 0: Define Automatically. 1: Define by Current Bank 2a-2b.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_VST[10:8]	2:0	See description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point,	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
			count by input dot clock.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_HST[10:8]	2:0	See description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_VDC[10:8]	2:0	See description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x00	Access : R/W
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	ATRANGE_HDC[10:8]	2:0	See description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. 0: Can gate the GOP clock. 1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. 0: Don't gate the idclk. 1: Can gate the idclk.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (2F61h)	REG2F61	7:0	Default : 0x00	Access : R/W
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '2F60h'.	
31h (2F62h)	REG2F62	7:0	Default : 0x00	Access : R/W
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (2F63h)	REG2F63	7:0	Default : 0x00	Access : R/W
	LOCK_SEL	7	Vsync lock_number_offset enable.	

IP1_M Register (Bank = 2F, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '2F62h'.	
32h (2F64h)	REG2F64	7:0	Default : 0x00	Access : R/W
	VLOCK[7:0]	7:0	VLOCK.	
32h (2F65h)	REG2F65	7:0	Default : 0x00	Access : R/W
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. 0x: Reference 21[15:14]. 10: Sample V end delay 3 line. 11: Sample V end delay 4 line.	
	-	5:3	Reserved.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	

IP2_M Register (Bank = 2F, Sub-Bank =02)

IP2_M Register (Bank = 2F, Sub-Bank =02)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h	REG2F05	7:0	Default : 0x00	Access : R/W

IP2_M Register (Bank = 2F, Sub-Bank =02)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F05h)	HFAC_SET_IP[15:8]	7:0	See description of '2F04h'.	
03h (2F06h)	REG2F06	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '2F04h'.	
04h (2F08h)	REG2F08	7:0	Default : 0x00	Access : R/W
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (2F09h)	REG2F09	7:0	Default : 0x00	Access : R/W
	HFACIN[15:8]	7:0	See description of '2F08h'.	
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '2F08h'.	
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00	Access : R/W
	IP2HSDEN	7	H Scaling Down enable.	
	-	6:0	Reserved.	
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00	Access : R/W
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00	Access : R/W
	VFAC_INI_T[15:8]	7:0	See description of '2F0Ch'.	
07h (2F0Eh)	REG2F0E	7:0	Default : 0x00	Access : R/W
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (2F0Fh)	REG2F0F	7:0	Default : 0x00	Access : R/W
	VFAC_INI_B[15:8]	7:0	See description of '2F0Eh'.	
08h (2F10h)	REG2F10	7:0	Default : 0x00	Access : R/W
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	VFACIN[15:8]	7:0	See description of '2F10h'.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '2F10h'.	
09h (2F13h)	REG2F13	7:0	Default : 0x00	Access : R/W
	PRE_VDOWN	7	V Scaling Down enable.	
	-	6	Reserved.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	

IP2_M Register (Bank = 2F, Sub-Bank =02)				
Index (Absolute)	Mnemonic	Bit	Description	
	-	4:0	Reserved.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP	6	Cb/Cr swap for 444 to 422.	
	-	5	Reserved.	
	YDELAY_EN	4	Y delay enable.	
	YCDelay_STEP[3:0]	3:0	Y/C delay pipe step.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:4	Reserved.	
	PRE_ALIGN_WIDTH[3:0]	3:0	Insert pixel number for mirror mode.	
34h (2F68h)	REG2F68	7:0	Default : 0x81	Access : R/W
	IP2_STATUS_CLR	7	IP2 status clear.	
	-	6:1	Reserved.	
	Dlast_ALIGN_EN	0	Data last signal align with IPM fetch number.	
34h (2F69h)	REG2F69	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	IP2_FLOW_CTRL_EN	4	IP2 flow control enable.	
	FLOW_CTRL_VALUE[3:0]	3:0	IP2 flow control count.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00	Access : R/W
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	VIN_CTRL_EN	4	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	3	IP2 VSD input line count number setting enable.	
	VSD_IN_NUM_USR[10:8]	2:0	See description of '2F6Ch'.	
37h (2F6Eh)	REG2F6E	7:0	Default : 0x00	Access : R/W
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (2F6Fh)	REG2F6F	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	VOU_CTRL_EN	4	IP2 VSD output line count control enable.	
	-	3	Reserved.	
	VSD_OUT_NUMBER[10:8]	2:0	See description of '2F6Eh'.	

IP2_M Register (Bank = 2F, Sub-Bank =02)				
Index (Absolute)	Mnemonic	Bit	Description	
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00	Access : RO
	MAX_LBUF_CNT[7:0]	7:0	IP2 line buffer max pixels count.	
3Dh (2F7Bh)	REG2F7B	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	BW_NOT_ENOUGH	0	IP2 line buffer full.	
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0x00	Access : RO
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (2F7Dh)	REG2F7D	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	READ_HSD_OUT_CNT[11:8]	3:0	See description of '2F7Ch'.	
3Fh (2F7Eh)	REG2F7E	7:0	Default : 0x00	Access : RO
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (2F7Fh)	REG2F7F	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	READ_VSD_OUT_CNT[10:8]	2:0	See description of '2F7Eh'.	
40h (2F80h)	REG2F80	7:0	Default : 0x08	Access : R/W
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	

PNR_REG Register (Bank = 2F, Sub-Bank =05)

PNR_REG Register (Bank = 2F, Sub-Bank =05)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
06h (2F0Ch)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
07h (2F0Eh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
08h (2F10h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
09h (2F12h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Ah (2F14h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Bh (2F16h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
11h	REG2F22	7:0	Default : 0x00	Access : R/W

PNR_REG Register (Bank = 2F, Sub-Bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
(2F22h)	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_FB2[1:0]	1:0	Main Window Motion Ratio.	
11h (2F23h)	REG2F23	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for noc_sel.	
12h (2F24h)	REG2F24	7:0	Default : 0x18	Access : R/W
	-	7:5	Reserved.	
	DITH_MODE_F2[1:0]	4:3	Main Window PNR dither mode, 00: no process, 01: truncate, 10: rounding, 11: dither.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (2F28h)	REG2F28	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for c.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window c motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window y motion divide mode.	
16h (2F2Ch)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
17h	-	7:0	Default : -	Access : -

PNR_REG Register (Bank = 2F, Sub-Bank = 05)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F2Eh)	-	-	Reserved.	
18h	-	7:0	Default : -	Access : -
(2F30h)	-	-	Reserved.	
19h	-	7:0	Default : -	Access : -
(2F32h)	-	-	Reserved.	
1Ah	-	7:0	Default : -	Access : -
(2F34h)	-	-	Reserved.	
1Bh	REG2F36	7:0	Default : 0x00	Access : R/W
(2F36h)	RESERVED_0[7:0]	7:0		
1Bh	REG2F37	7:0	Default : 0x00	Access : R/W
(2F37h)	RESERVED_0[15:8]	7:0	See description of '2F36h'.	
1Ch	REG2F38	7:0	Default : 0x00	Access : R/W
(2F38h)	RESERVED_1[7:0]	7:0		
1Ch	REG2F39	7:0	Default : 0x00	Access : R/W
(2F39h)	RESERVED_1[15:8]	7:0	See description of '2F38h'.	
50h	REG2FA0	7:0	Default : 0x22	Access : R/W
(2FA0h)	PNR_TABLECCS_15_0[7:0]	7:0	PNR CCS Table, smooth_en, smooth_step, mv_gain.	
50h	REG2FA1	7:0	Default : 0x08	Access : R/W
(2FA1h)	PNR_TABLECCS_15_0[15:8]	7:0	See description of '2FA0h'.	
51h	REG2FA2	7:0	Default : 0x00	Access : R/W
(2FA2h)	PNR_TABLECCS_31_16[7:0]	7:0	PNR CCS Table, mv_offset, ev_gain_cc, ev_weight_cc.	
51h	REG2FA3	7:0	Default : 0x86	Access : R/W
(2FA3h)	PNR_TABLECCS_31_16[15:8]	7:0	See description of '2FA2h'.	
52h	REG2FA4	7:0	Default : 0x0A	Access : R/W
(2FA4h)	PNR_TABLECCS_47_32[7:0]	7:0	PNR CCS Table, pre_weight_c, pre_weight_y.	
52h	REG2FA5	7:0	Default : 0x0A	Access : R/W
(2FA5h)	PNR_TABLECCS_47_32[15:8]	7:0	See description of '2FA4h'.	
53h	REG2FA6	7:0	Default : 0x03	Access : R/W
(2FA6h)	PNR_TABLECCS_63_48[7:0]	7:0	PNR CCS Table, post_weight_c, post_weight_y.	
53h	REG2FA7	7:0	Default : 0x04	Access : R/W
(2FA7h)	PNR_TABLECCS_63_48[15:8]	7:0	See description of '2FA6h'.	
54h	REG2FA8	7:0	Default : 0x08	Access : R/W
(2FA8h)	PNR_TABLECCS_79_64[7:0]	7:0	PNR CCS Table, y_ev_weight_y, y_ev_offset_y.	

PNR_REG Register (Bank = 2F, Sub-Bank =05)

Index (Absolute)	Mnemonic	Bit	Description
54h (2FA9h)	REG2FA9	7:0	Default : 0x20
	PNR_TABLECCS_79_64[15:8]	7:0	Access : R/W
55h (2FAAh)	REG2FAA	7:0	Default : 0x08
	PNR_TABLECCS_95_80[7:0]	7:0	Access : R/W
55h (2FABh)	REG2FAB	7:0	Default : 0x20
	PNR_TABLECCS_95_80[15:8]	7:0	Access : R/W
56h (2FACH)	REG2FAC	7:0	Default : 0x02
	-	7:4	Access : R/W
	PNR_TABLECCS_99_96[3:0]	3:0	Reserved.
57h (2FAEh)	REG2FAE	7:0	Default : 0x0C
	PCCS_CORING_Y[7:0]	7:0	Access : R/W
57h (2FAFh)	REG2FAF	7:0	Default : 0x0C
	PCCS_CORING_C[7:0]	7:0	Access : R/W
60h (2FC0h)	REG2FC0	7:0	Default : 0x00
	PCCS_TABLE_15_0[7:0]	7:0	Access : R/W
60h (2FC1h)	REG2FC1	7:0	Default : 0x00
	PCCS_TABLE_15_0[15:8]	7:0	Access : R/W
61h (2FC2h)	REG2FC2	7:0	Default : 0x00
	PCCS_TABLE_31_16[7:0]	7:0	Access : R/W
61h (2FC3h)	REG2FC3	7:0	Default : 0x00
	PCCS_TABLE_31_16[15:8]	7:0	Access : R/W
62h (2FC4h)	REG2FC4	7:0	Default : 0x31
	PCCS_TABLE_47_32[7:0]	7:0	Access : R/W
62h (2FC5h)	REG2FC5	7:0	Default : 0x75
	PCCS_TABLE_47_32[15:8]	7:0	Access : R/W
63h (2FC6h)	REG2FC6	7:0	Default : 0x00
	PCCS_TABLE_63_48[7:0]	7:0	Access : R/W
63h (2FC7h)	REG2FC7	7:0	Default : 0x00
	PCCS_TABLE_63_48[15:8]	7:0	Access : R/W
70h (2FE0h)	REG2FE0	7:0	Default : 0x00
	RESERVED_TABLE_15_0[7:0]	7:0	Access : R/W
70h (2FE1h)	REG2FE1	7:0	Default : 0x00
	RESERVED_TABLE_15_0[15:8]	7:0	Access : R/W

PNR_REG Register (Bank = 2F, Sub-Bank =05)

Index (Absolute)	Mnemonic	Bit	Description
71h (2FE2h)	REG2FE2	7:0	Default : 0x00 Access : R/W
	RESERVED_TABLE_31_16[7:0]	7:0	Reserved Table.
71h (2FE3h)	REG2FE3	7:0	Default : 0x00 Access : R/W
	RESERVED_TABLE_31_16[15:8]	7:0	See description of '2FE2h'.
72h (2FE4h)	REG2FE4	7:0	Default : 0x00 Access : R/W
	RESERVED_TABLE_47_32[7:0]	7:0	Reserved Table.
72h (2FE5h)	REG2FE5	7:0	Default : 0x00 Access : R/W
	RESERVED_TABLE_47_32[15:8]	7:0	See description of '2FE4h'.
73h (2FE6h)	REG2FE6	7:0	Default : 0x00 Access : R/W
	RESERVED_TABLE_63_48[7:0]	7:0	Reserved Table.
73h (2FE7h)	REG2FE7	7:0	Default : 0x00 Access : R/W
	RESERVED_TABLE_63_48[15:8]	7:0	See description of '2FE6h'.
74h (2FE8h)	REG2FE8	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	BLEND_LPF_TURN_OFF	1	Turn off PCCS blend LPF.
	MEDIAN_TURN_OFF	0	Turn off PCCS 5tap median filter.

DNR_REG Register (Bank = 2F, Sub-Bank =06)

DNR_REG Register (Bank = 2F, Sub-Bank =06)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
21h (2F42h)	REG2F42	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	F2_MR_SOURCE_NRY	4	F2 Motion Source Cur Select. 0: Cur after NR. 1: Cur non-NR.	
	-	3:2	Reserved.	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION EN.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	F2_LUT_SOURCE_C[1:0]	7:6	F2 DNR Table C source select. x1: From Y-diff. 10: From MED. 00: From C-diff.	
	F2_LUT_SOURCE_Y[1:0]	5:4	F2 DNR Table Y source select.	

DNR_REG Register (Bank = 2F, Sub-Bank = 06)				
Index (Absolute)	Mnemonic	Bit	Description	
			x1: From C-diff. 10: From MED. 00: From Y-diff.	
	F2_DNR_TABLEC_LSB_EN	3	F2 DNR Table C LSB Mapping EN.	
	F2_DNR_TABLEY_LSB_EN	2	F2 DNR Table Y LSB Mapping EN.	
	F2_NR_TABLE_SEL_C	1	F2 DNR Table C Mapping Select. 0: Non-linear. 1: Linear.	
	F2_NR_TABLE_SEL_Y	0	F2 DNR Table Y Mapping Select. 0: Non-linear. 1: Linear.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F2_SNR_METHOD_SEL	2	Reserved.	
	F2_SNR_MD_MODE_EN	1	F2 SNR Motion Mode EN.	
	F2_SNR_EN	0	F2 SNR FUNCTION EN.	
24h ~ 24h (2F48h ~ 2F49h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	F2_NR_ROUND_BIT_C	5	Set C_ROUND described as above.	
	F2_NR_ROUND_BIT_Y	4	Set Y_ROUND described as above.	
	F2_ROUND_MODE_C[1:0]	3:2	F2 DNR C blend rounding select. 00: Add {C_ROUND,1'b0}. 01: Add {dither.1'b0}. 10: Add frame-base dither. 11: Add {dither[1:0]}.	
	F2_ROUND_MODE_Y[1:0]	1:0	F2 DNR Y blend rounding select. 00: Add {Y_ROUND,1'b0}. 01: Add {dither.1'b0}. 10: Add frame-base dither. 11: Add {dither[1:0]}.	
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	F2_MAX_MOT_ENABLE_C	3	F2_MAX_MOT_ENABLE_C.	

DNR_REG Register (Bank = 2F, Sub-Bank =06)				
Index (Absolute)	Mnemonic	Bit	Description	
	F2_MAX_MOT_ENABLE_Y	2	F2_MAX_MOT_ENABLE_Y.	
	F2_DNR_FILTER_EN_C	1	F2_DNR_FILTER_EN_C.	
	F2_DNR_FILTER_EN_Y	0	F2_DNR_FILTER_EN_Y.	
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W
	F2_DNR_FILTER_DIV0_C[2:0]	7:5	F2_DNR_FILTER_DIV0_C.	
	F2_DNR_FILTER_DIV0_Y[2:0]	4:2	F2_DNR_FILTER_DIV0_Y.	
	F2_DNR_FILTER_SIGN_C	1	F2_DNR_FILTER_SIGN_C.	
	F2_DNR_FILTER_SIGN_Y	0	F2_DNR_FILTER_SIGN_Y.	
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00	Access : R/W
	F2_DNR_FILTER_MODE_C[1:0]	7:6	F2_DNR_FILTER_MODE_C.	
	F2_DNR_FILTER_MODE_Y[1:0]	5:4	F2_DNR_FILTER_MODE_Y.	
	F2_DNR_FILTER_DIV1_C[1:0]	3:2	F2_DNR_FILTER_DIV1_C.	
	F2_DNR_FILTER_DIV1_Y[1:0]	1:0	F2_DNR_FILTER_DIV1_Y.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x08	Access : R/W
	F2_SHARP_LEVEL[7:0]	7:0	F2 SNR sharpness level.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x07	Access : R/W
	-	7:4	Reserved.	
	F2_POW_NUM[3:0]	3:0	F2 SNR power number.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	F2_SNR_MDIFF_WT[2:0]	2:0	F2 MED motion different shift.	
40h (2F80h)	REG2F80	7:0	Default : 0xBD	Access : R/W
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (2F81h)	REG2F81	7:0	Default : 0x79	Access : R/W
	DNR_TABLEY_0[15:8]	7:0	See description of '2F80h'.	
41h (2F82h)	REG2F82	7:0	Default : 0x56	Access : R/W
	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (2F83h)	REG2F83	7:0	Default : 0x34	Access : R/W
	DNR_TABLEY_1[15:8]	7:0	See description of '2F82h'.	
42h (2F84h)	REG2F84	7:0	Default : 0x12	Access : R/W
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (2F85h)	REG2F85	7:0	Default : 0x00	Access : R/W
	DNR_TABLEY_2[15:8]	7:0	See description of '2F84h'.	

DNR_REG Register (Bank = 2F, Sub-Bank = 06)

Index (Absolute)	Mnemonic	Bit	Description
43h (2F86h)	REG2F86	7:0	Default : 0x00
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.
43h (2F87h)	REG2F87	7:0	Default : 0x00
	DNR_TABLEY_3[15:8]	7:0	See description of '2F86h'.
44h (2F88h)	REG2F88	7:0	Default : 0xBD
	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.
44h (2F89h)	REG2F89	7:0	Default : 0x79
	DNR_TABLEC_0[15:8]	7:0	See description of '2F88h'.
45h (2F8Ah)	REG2F8A	7:0	Default : 0x56
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.
45h (2F8Bh)	REG2F8B	7:0	Default : 0x34
	DNR_TABLEC_1[15:8]	7:0	See description of '2F8Ah'.
46h (2F8Ch)	REG2F8C	7:0	Default : 0x12
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.
46h (2F8Dh)	REG2F8D	7:0	Default : 0x00
	DNR_TABLEC_2[15:8]	7:0	See description of '2F8Ch'.
47h (2F8Eh)	REG2F8E	7:0	Default : 0x00
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.
47h (2F8Fh)	REG2F8F	7:0	Default : 0x00
	DNR_TABLEC_3[15:8]	7:0	See description of '2F8Eh'.
48h (2F90h)	REG2F90	7:0	Default : 0x70
	DNR_TABLEY_LSB[7:0]	7:0	DNR TABLEY_LSB.
48h (2F91h)	REG2F91	7:0	Default : 0x07
	-	7:4	Reserved.
49h (2F92h)	REG2F92	7:0	Default : 0x70
	DNR_TABLEC_LSB[7:0]	7:0	DNR TABLEC_LSB.
49h (2F93h)	REG2F93	7:0	Default : 0x07
	-	7:4	Reserved.
54h ~ 5Dh (2FA8h ~ 2FBBh)	-	7:0	Default : -
	-	-	Reserved.
70h ~ 71h	-	7:0	Default : -

DNR_REG Register (Bank = 2F, Sub-Bank =06)				
Index (Absolute)	Mnemonic	Bit	Description	
(2FE0h ~ 2FE3h)	-	-	Reserved.	
74h (2FE8h)	REG2FE8	7:0	Default : 0x08	Access : R/W
	RESERVED_TABLE_0[7:0]	7:0	Reserved.	
74h (2FE9h)	REG2FE9	7:0	Default : 0x18	Access : R/W
	RESERVED_TABLE_0[15:8]	7:0	See description of '2FE8h'.	
75h (2FEAh)	REG2FEA	7:0	Default : 0x04	Access : R/W
	RESERVED_TABLE_1[7:0]	7:0	Reserved.	
75h (2FEBh)	REG2FEB	7:0	Default : 0x0C	Access : R/W
	RESERVED_TABLE_1[15:8]	7:0	See description of '2FEAh'.	
76h (2FECh)	REG2FEC	7:0	Default : 0x00	Access : R/W
	RESERVED_TABLE_2[7:0]	7:0	Reserved.	
76h (2FEDh)	REG2FED	7:0	Default : 0x00	Access : R/W
	RESERVED_TABLE_2[15:8]	7:0	See description of '2FECh'.	
77h (2FEEh)	REG2FEE	7:0	Default : 0x00	Access : R/W
	RESERVED_TABLE_3[7:0]	7:0	Reserved.	
77h (2FEFh)	REG2FEF	7:0	Default : 0x00	Access : R/W
	RESERVED_TABLE_3[15:8]	7:0	See description of '2FEEh'.	
7Ah (2FF4h)	REG2FF4	7:0	Default : 0x00	Access : RO
	STATUS_HCNT_F2[7:0]	7:0	F2 hcnt for debug.	
7Ah (2FF5h)	REG2FF5	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	STATUS_HCNT_F2[10:8]	2:0	See description of '2FF4h'.	
7Bh (2FF6h)	REG2FF6	7:0	Default : 0x00	Access : RO
	STATUS_VCNT_F2[7:0]	7:0	F2 vcnt for debug.	
7Bh (2FF7h)	REG2FF7	7:0	Default : 0x00	Access : RO, R/W
	STATUS_CLR_F2	7	F2 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F2[10:8]	2:0	See description of '2FF6h'.	

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:1	Reserved.	
	MW_BD_REG_EN	0	Main Window Border Register Enable. 0: Sub window Border register enable. 1: Main window Border register Enable.	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (2F05h)	REG2F05	7:0	Default : 0x00	Access : R/W
	BDLO_BO[3:0]	7:4	Main window border outside height of Left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h	REG2F06	7:0	Default : 0x00	Access : R/W

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
(2F06h)	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.
03h (2F07h)	REG2F07	7:0	Default : 0x00 Access : R/W
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.
04h (2F08h)	REG2F08	7:0	Default : 0x00 Access : R/W
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.
04h (2F09h)	REG2F09	7:0	Default : 0x00 Access : R/W
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00 Access : R/W
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00 Access : R/W
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.
	-	3:2	Reserved.
	181FWINSEL[1:0]	1:0	18h~1Fh Display Window Select. 00: 1st window. 01: 2nd window. 10: 3rd window. 11: 4th window.
07h	REG2F0E	7:0	Default : 0x00 Access : R/W

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
(2F0Eh)	S_HDEST[7:0]	7:0	Sub window Horizontal Start.
07h (2F0Fh)	REG2F0F	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_HDEST[11:8]	3:0	See description of '2F0Eh'.
08h (2F10h)	REG2F10	7:0	Default : 0x00 Access : R/W
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.
08h (2F11h)	REG2F11	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_HDEEND[11:8]	3:0	See description of '2F10h'.
09h (2F12h)	REG2F12	7:0	Default : 0x00 Access : R/W
	S_VDEST[7:0]	7:0	Sub window Vertical Star.
09h (2F13h)	REG2F13	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_VDEST[11:8]	3:0	See description of '2F12h'.
0Ah (2F14h)	REG2F14	7:0	Default : 0x00 Access : R/W
	S_VDEEND[7:0]	7:0	Sub window Vertical End.
0Ah (2F15h)	REG2F15	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_VDEEND[11:8]	3:0	See description of '2F14h'.
0Bh (2F16h)	REG2F16	7:0	Default : 0x00 Access : R/W
	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.
0Bh (2F17h)	REG2F17	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_HDEST_2ND[11:8]	3:0	See description of '2F16h'.
0Ch (2F18h)	REG2F18	7:0	Default : 0x00 Access : R/W
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.
0Ch (2F19h)	REG2F19	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_HDEEND_2ND[11:8]	3:0	See description of '2F18h'.
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00 Access : R/W
	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.
0Dh (2F1Bh)	REG2F1B	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
	S_VDEST_2ND[11:8]	3:0	See description of '2F1Ah'.
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00 Access : R/W
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_VDEEND_2ND[11:8]	3:0	See description of '2F1Ch'.
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x00 Access : R/W
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.
0Fh (2F1Fh)	REG2F1F	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_HDEST_3RD[11:8]	3:0	See description of '2F1Eh'.
10h (2F20h)	REG2F20	7:0	Default : 0x00 Access : R/W
	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.
10h (2F21h)	REG2F21	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_HDEEND_3RD[11:8]	3:0	See description of '2F20h'.
11h (2F22h)	REG2F22	7:0	Default : 0x00 Access : R/W
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.
11h (2F23h)	REG2F23	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_VDEST_3RD[11:8]	3:0	See description of '2F22h'.
12h (2F24h)	REG2F24	7:0	Default : 0x00 Access : R/W
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.
12h (2F25h)	REG2F25	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_VDEEND_3RD[11:8]	3:0	See description of '2F24h'.
13h (2F26h)	REG2F26	7:0	Default : 0x00 Access : R/W
	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.
13h (2F27h)	REG2F27	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_HDEST_4TH[11:8]	3:0	See description of '2F26h'.
14h (2F28h)	REG2F28	7:0	Default : 0x00 Access : R/W
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
14h (2F29h)	REG2F29	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_HDEEND_4TH[11:8]	3:0	See description of '2F28h'.
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00 Access : R/W
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_VDEST_4TH[11:8]	3:0	See description of '2F2Ah'.
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00 Access : R/W
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	S_VDEEND_4TH[11:8]	3:0	See description of '2F2Ch'.
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00 Access : R/W
	SWBCOL[7:0]	7:0	Sub Window Border Color.
17h (2F2Fh)	REG2F2F	7:0	Default : 0x00 Access : R/W
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.
18h (2F30h)	REG2F30	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.
	-	3:1	Reserved.
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.
18h (2F31h)	REG2F31	7:0	Default : 0x00 Access : R/W
	S_HBC_GAIN[3:0]	7:4	HBC gain for sub window.
	S_HBC_EN	3	HBC function enable for sub window.
	S_HBC_ROUNDING	2	HBC rounding enable for sub window.
	-	1	Reserved.
	BRC	0	Brightness function. 0: Off.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
			1: On.
19h ~ 1Ah (2F32h ~ 2F35h)	-	7:0	Default : - Access : -
	-	-	Reserved.
1Bh (2F36h)	REG2F36	7:0	Default : 0x00 Access : R/W
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.
1Bh (2F37h)	REG2F37	7:0	Default : 0x00 Access : R/W
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.
	KST_HOFFS[14:8]	6:0	See description of '2F36h'.
1Ch (2F38h)	REG2F38	7:0	Default : 0x00 Access : R/W
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.
1Ch (2F39h)	REG2F39	7:0	Default : 0x00 Access : R/W
	KSTPD[15:8]	7:0	See description of '2F38h'.
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x00 Access : R/W
	CM11[7:0]	7:0	Color Matrix Coefficient 11.
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CM11[12:8]	4:0	See description of '2F3Ah'.
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x00 Access : R/W
	CM12[7:0]	7:0	Color Matrix Coefficient 12.
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CM12[12:8]	4:0	See description of '2F3Ch'.
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00 Access : R/W
	CM13[7:0]	7:0	Color Matrix Coefficient 13.
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CM13[12:8]	4:0	See description of '2F3Eh'.
20h (2F40h)	REG2F40	7:0	Default : 0x00 Access : R/W
	CM21[7:0]	7:0	Color Matrix Coefficient 21.
20h	REG2F41	7:0	Default : 0x00 Access : R/W

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
(2F41h)	-	7:5	Reserved.
	CM21[12:8]	4:0	See description of '2F40h'.
21h (2F42h)	REG2F42	7:0	Default : 0x00 Access : R/W
	CM22[7:0]	7:0	Color Matrix Coefficient 22.
21h (2F43h)	REG2F43	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CM22[12:8]	4:0	See description of '2F42h'.
22h (2F44h)	REG2F44	7:0	Default : 0x00 Access : R/W
	CM23[7:0]	7:0	Color Matrix Coefficient 23.
22h (2F45h)	REG2F45	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CM23[12:8]	4:0	See description of '2F44h'.
23h (2F46h)	REG2F46	7:0	Default : 0x00 Access : R/W
	CM31[7:0]	7:0	Color Matrix Coefficient 31.
23h (2F47h)	REG2F47	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CM31[12:8]	4:0	See description of '2F46h'.
24h (2F48h)	REG2F48	7:0	Default : 0x00 Access : R/W
	CM32[7:0]	7:0	Color Matrix Coefficient 32.
24h (2F49h)	REG2F49	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CM32[12:8]	4:0	See description of '2F48h'.
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00 Access : R/W
	CM33[7:0]	7:0	Color Matrix Coefficient 33.
25h (2F4Bh)	REG2F4B	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CM33[12:8]	4:0	See description of '2F4Ah'.
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.
	CMC	4	Color Matrix Control.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
			0: Disable. 1: Enable.
	-	3	Reserved.
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00 Access : R/W
	SMEN	7	SVM Main window Enable.
	SMTE	6	SVM Main window Tap Enable.
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.
	SSWEN	3	SVM Sub window Enable.
	SSWETE	2	SVM Sub window Tap Enable.
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00 Access : R/W
	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.
	SVMBYS[1:0]	5:4	SVM Bypass Y Select. 0x: SMV data. 10: Original Y data.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
			11: Y with tap filter.
	SCORING[3:0]	3:0	SVM Coring.
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00 Access : R/W
	SVMLMT[7:0]	7:0	SVM Limit.
28h (2F50h)	REG2F50	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	SMSTP[2:0]	6:4	SVM Main window Step.
	SMGAIN[3:0]	3:0	SVM Main window Gain.
28h (2F51h)	REG2F51	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	SSWSTP[2:0]	6:4	SVM Sub window Step.
	SWGAIN[3:0]	3:0	SVM Sub window Gain.
29h (2F52h)	REG2F52	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	SPAJ[1:0]	6:5	SVM Pipe Adjust.
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.
29h (2F53h)	REG2F53	7:0	Default : 0x00 Access : RO, R/W
	SVM_SEP_DLY	7	SVM Separate Delay Enable.
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.
2Ah (2F54h)	REG2F54	7:0	Default : 0x00 Access : R/W
	C1080I	7	1080i mode. 0: Follow DE. 1: Follow HSYNC.
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.
	IPFI	5	To Pad Field Invert enable.
	I1440	4	Interlace 1440 mode. This bit works at frame SBPCM=0. 0: Disable, horizontal valid pixel = 720; SVM

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
			support. 1: Enable, horizontal valid pixel = 1440; does not support SVM.
	IRDEN	3	Random 10 bit DAC Enable.
	IHSRE	2	HSYNC Shift control. 0: Shift left. 1: Shift right.
	IOFI	1	Interlace Output Field Invert.
	IOEN	0	Interlace Output Enable.
2Bh (2F56h)	REG2F56	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.
	-	3:0	Reserved.
2Bh (2F57h)	REG2F57	7:0	Default : 0x00 Access : R/W
	IP_FINV	7	IP Field Inverse.
	IP_ITLC	6	IP Interlace.
	SIM	5	Single Interlace Mode. 0: Disable. 1: Enable.
	LPM	4	LVDS 10-bit Mode. 0: Disable. 1: Enable.
	BES[1:0]	3:2	Border Extend for SVM.
	OES[1:0]	1:0	OSD Extend for SVM.
2Ch (2F58h)	REG2F58	7:0	Default : 0x00 Access : R/W
	HSOFFS[7:0]	7:0	HYSNC Shift Offset.
2Ch (2F59h)	REG2F59	7:0	Default : 0x00 Access : R/W
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.
	RESERVED[1:0]	6:5	RESERVED.
	-	4	Reserved.
	HSOFFS[11:8]	3:0	See description of '2F58h'.
2Dh ~ 2Fh (2F5Ah ~ 2F5Fh)	-	7:0	Default : - Access : -
	-	-	Reserved.
30h	REG2F60	7:0	Default : 0x00 Access : R/W

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
(2F60h)	R_BRI_OFFSET[7:0]	7:0	Offset for R data.
30h (2F61h)	REG2F61	7:0	Default : 0x00 Access : R/W
	BRI_EN	7	Brightness enable (after gamma).
	CON_EN	6	Contrast enable (after gamma).
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.
	-	4:3	Reserved.
	R_BRI_OFFSET[10:8]	2:0	See description of '2F60h'.
31h (2F62h)	REG2F62	7:0	Default : 0x00 Access : R/W
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.
31h (2F63h)	REG2F63	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	G_BRI_OFFSET[10:8]	2:0	See description of '2F62h'.
32h (2F64h)	REG2F64	7:0	Default : 0x00 Access : R/W
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.
32h (2F65h)	REG2F65	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	B_BRI_OFFSET[10:8]	2:0	See description of '2F64h'.
33h (2F66h)	REG2F66	7:0	Default : 0x00 Access : R/W
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.
33h (2F67h)	REG2F67	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	R_CON_GAIN[11:8]	3:0	See description of '2F66h'.
34h (2F68h)	REG2F68	7:0	Default : 0x00 Access : R/W
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.
34h (2F69h)	REG2F69	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	G_CON_GAIN[11:8]	3:0	See description of '2F68h'.
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00 Access : R/W
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	B_CON_GAIN[11:8]	3:0	See description of '2F6Ah'.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00 Access : R/W
	M_BRI_R[7:0]	7:0	Brightness offset (bri_function) for main window R.
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00 Access : R/W
	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.
	-	6:3	Reserved.
	M_BRI_R[10:8]	2:0	See description of '2F6Ch'.
37h (2F6Eh)	REG2F6E	7:0	Default : 0x00 Access : R/W
	M_BRI_G[7:0]	7:0	Brightness offset (bri_function) for main window G.
37h (2F6Fh)	REG2F6F	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	M_BRI_G[10:8]	2:0	See description of '2F6Eh'.
38h (2F70h)	REG2F70	7:0	Default : 0x00 Access : R/W
	M_BRI_B[7:0]	7:0	Brightness offset (bri_function) for main window B.
38h (2F71h)	REG2F71	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	M_BRI_B[10:8]	2:0	See description of '2F70h'.
39h (2F72h)	REG2F72	7:0	Default : 0x00 Access : R/W
	S_BRI_R[7:0]	7:0	Brightness offset (bri_function) for sub window R.
39h (2F73h)	REG2F73	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	S_BRI_R[10:8]	2:0	See description of '2F72h'.
3Ah (2F74h)	REG2F74	7:0	Default : 0x00 Access : R/W
	S_BRI_G[7:0]	7:0	Brightness offset (bri_function) for sub window G.
3Ah (2F75h)	REG2F75	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	S_BRI_G[10:8]	2:0	See description of '2F74h'.
3Bh (2F76h)	REG2F76	7:0	Default : 0x00 Access : R/W
	S_BRI_B[7:0]	7:0	Brightness offset (bri_function) for sub window B.
3Bh	REG2F77	7:0	Default : 0x00 Access : R/W

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
(2F77h)	-	7:3	Reserved.
	S_BRI_B[10:8]	2:0	See description of '2F76h'.
3Ch (2F78h)	REG2F78	7:0	Default : 0x00 Access : R/W
	GAMMA_MLOAD_CHECK_R_BASE0[7:0]	7:0	Check value for auto mload base0 R channel.
3Ch (2F79h)	REG2F79	7:0	Default : 0x00 Access : RO, R/W
	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.
	-	6:4	Reserved.
	GAMMA_MLOAD_CHECK_R_BASE0[11:8]	3:0	See description of '2F78h'.
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00 Access : R/W
	GAMMA_MLOAD_CHECK_R_BASE1[7:0]	7:0	Check value for auto mload base1 R channel.
3Dh (2F7Bh)	REG2F7B	7:0	Default : 0x00 Access : RO, R/W
	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.
	-	6:4	Reserved.
	GAMMA_MLOAD_CHECK_R_BASE1[11:8]	3:0	See description of '2F7Ah'.
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0x00 Access : R/W
	GAMMA_MLOAD_CHECK_G_BASE0[7:0]	7:0	Check value for auto mload base0 G channel.
3Eh (2F7Dh)	REG2F7D	7:0	Default : 0x00 Access : RO, R/W
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.
	-	6:4	Reserved.
	GAMMA_MLOAD_CHECK_G_BASE0[11:8]	3:0	See description of '2F7Ch'.
3Fh (2F7Eh)	REG2F7E	7:0	Default : 0x00 Access : R/W
	GAMMA_MLOAD_CHECK_G_BASE1[7:0]	7:0	Check value for auto mload base1 G channel.
3Fh (2F7Fh)	REG2F7F	7:0	Default : 0x00 Access : RO, R/W
	GAMMA_MLOAD_CHECK_G_ERR_1	7	Base1 G channel check error.
	-	6:4	Reserved.
	GAMMA_MLOAD_CHECK_G_BASE1[11:8]	3:0	See description of '2F7Eh'.
40h (2F80h)	REG2F80	7:0	Default : 0x00 Access : R/W
	GAMMA_MLOAD_CHECK_B_BASE0[7:0]	7:0	Check value for auto mload base0 B channel.
40h (2F81h)	REG2F81	7:0	Default : 0x00 Access : RO, R/W
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.
	-	6:4	Reserved.
	GAMMA_MLOAD_CHECK_B_BASE0[11:8]	3:0	See description of '2F80h'.
41h	REG2F82	7:0	Default : 0x00 Access : R/W

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
(2F82h)	GAMMA_MLOAD_CHECK_B_BASE1[7:0]	7:0	Check value for auto mload base1 B channel.
41h (2F83h)	REG2F83	7:0	Default : 0x00 Access : RO, R/W
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.
	-	6:4	Reserved.
	GAMMA_MLOAD_CHECK_B_BASE1[11:8]	3:0	See description of '2F82h'.
42h ~ 45h (2F84h ~ 2F8Bh)	-	7:0	Default : - Access : -
	-	-	Reserved.
46h (2F8Ch)	REG2F8C	7:0	Default : 0x00 Access : R/W
	CAP_STAGE[3:0]	7:4	Capture stage selection. 0: VOP2_dp input data. 1: BRI output. 2: HBC output. 3: CON_BRI output. 4: FWC output. 5: Gamma output. 6: Noise dither output.
	-	3:0	Reserved.
46h (2F8Dh)	-	7:0	Default : - Access : -
	-	-	Reserved.
47h (2F8Eh)	REG2F8E	7:0	Default : 0x00 Access : R/W
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.
47h (2F8Fh)	REG2F8F	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '2F8Eh'.
48h (2F90h)	REG2F90	7:0	Default : 0x00 Access : R/W
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.
48h (2F91h)	REG2F91	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '2F90h'.
49h (2F92h)	REG2F92	7:0	Default : 0x00 Access : R/W
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.
49h (2F93h)	REG2F93	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '2F92h'.
4Ah (2F94h)	REG2F94	7:0	Default : 0x00 Access : R/W
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.
4Ah (2F95h)	REG2F95	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SUB_R_CON_GAIN[11:8]	3:0	See description of '2F94h'.
4Bh (2F96h)	REG2F96	7:0	Default : 0x00 Access : R/W
	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.
4Bh (2F97h)	REG2F97	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SUB_G_CON_GAIN[11:8]	3:0	See description of '2F96h'.
4Ch (2F98h)	REG2F98	7:0	Default : 0x00 Access : R/W
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.
4Ch (2F99h)	REG2F99	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SUB_B_CON_GAIN[11:8]	3:0	See description of '2F98h'.
4Dh (2F9Ah)	REG2F9A	7:0	Default : 0x00 Access : R/W
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.
4Dh (2F9Bh)	REG2F9B	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '2F9Ah'.
4Eh (2F9Ch)	REG2F9C	7:0	Default : 0x00 Access : R/W
	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.
4Eh (2F9Dh)	REG2F9D	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '2F9Ch'.
4Fh (2F9Eh)	REG2F9E	7:0	Default : 0x00 Access : R/W
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.
4Fh (2F9Fh)	REG2F9F	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '2F9Eh'.
50h (2FA0h)	REG2FA0	7:0	Default : 0x00 Access : R/W
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
50h (2FA1h)	REG2FA1	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '2FA0h'.
51h (2FA2h)	REG2FA2	7:0	Default : 0x00 Access : R/W
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.
51h (2FA3h)	REG2FA3	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '2FA2h'.
52h (2FA4h)	REG2FA4	7:0	Default : 0x00 Access : R/W
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.
52h (2FA5h)	REG2FA5	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '2FA4h'.
53h (2FA6h)	REG2FA6	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma CON_BRI.
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.
53h (2FA7h)	REG2FA7	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.
54h (2FA8h)	REG2FA8	7:0	Default : 0x00 Access : R/W
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.
54h (2FA9h)	REG2FA9	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	FREEZ_VCNT_VALUE[10:8]	2:0	See description of '2FA8h'.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
55h (2FAAh)	REG2FAA	7:0	Default : 0x00 Access : R/W
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when REG_NEW_LOCK_POINT is set high.
55h (2FABh)	REG2FAB	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	LOCK_VCNT_VALUE[10:8]	2:0	See description of '2FAAh'.
56h (2FACH)	REG2FAC	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	PSEUDO_VS_EN	6	Enable pseudo vsync for freeze region.
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.
	OUTPUT_FIELD_INV	4	Invert field for output reference signal.
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.
	IVS_SEL	2	Select insert_end point as input reference for frame PLL.
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.
	INPUT_FREEZ	0	V-counter freeze enable.
56h (2FADh)	REG2FAD	7:0	Default : 0x00 Access : RO, R/W
	VCNT_FREEZ_REGION	7	In V-counter freeze status.
	-	6:2	Reserved.
	IVS_CNT[9:8]	1:0	Frame number for input reference generate.
57h (2FAEh)	REG2FAE	7:0	Default : 0x00 Access : R/W
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for CCIR656 format.
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for CCIR656 format.
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
57h (2FAFh)	REG2FAF	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.
	NOISE_DITH_EN	5	Noise dither enable.
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.
	CAP_EN	3	Capture image to IP enable.
	-	2:0	Reserved.
58h (2FB0h)	REG2FB0	7:0	Default : 0x00 Access : R/W
	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. REG_MAIN_R_MIN_SIGN = 1:. MAIN_R_MIN = -MAIN_R_MIN_LIMIT. REG_MAIN_R_MIN_SIGN = 0:. MAIN_R_MIN = MAIN_R_MIN_LIMIT.
58h (2FB1h)	REG2FB1	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '2FB0h'.
59h (2FB2h)	REG2FB2	7:0	Default : 0x00 Access : R/W
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.
59h (2FB3h)	REG2FB3	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '2FB2h'.
5Ah (2FB4h)	REG2FB4	7:0	Default : 0x00 Access : R/W
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_MAIN_G_MIN_SIGN = 1:. MAIN_G_MIN = -MAIN_G_MIN_LIMIT. REG_MAIN_G_MIN_SIGN = 0:. MAIN_G_MIN = MAIN_G_MIN_LIMIT.
5Ah (2FB5h)	REG2FB5	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '2FB4h'.
5Bh (2FB6h)	REG2FB6	7:0	Default : 0x00 Access : R/W
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
5Bh (2FB7h)	REG2FB7	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '2FB6h'.
5Ch (2FB8h)	REG2FB8	7:0	Default : 0x00 Access : R/W
	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_MAIN_B_MIN_SIGN = 1:. MAIN_R_MIN = -MAIN_B_MIN_LIMIT. REG_MAIN_B_MIN_SIGN = 0:. MAIN_R_MIN = MAIN_B_MIN_LIMIT.
5Ch (2FB9h)	REG2FB9	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '2FB8h'.
5Dh (2FBAh)	REG2FBA	7:0	Default : 0x00 Access : R/W
	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.
5Dh (2FBBh)	REG2FBB	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '2FBAh'.
5Eh (2FBCh)	REG2FBC	7:0	Default : 0x00 Access : R/W
	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value. S.12 format sign bit is bit-12. REG_SUB_R_MIN_SIGN = 1: MAIN_R_MIN = -SUB_R_MIN_LIMIT. REG_SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.
5Eh (2FBDh)	REG2FBD	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '2FBCh'.
5Fh (2FBEh)	REG2FBE	7:0	Default : 0x00 Access : R/W
	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.
5Fh (2FBFh)	REG2FBF	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '2FBEh'.
60h (2FC0h)	REG2FC0	7:0	Default : 0x00 Access : R/W
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
			bit-12. REG_SUB_G_MIN_SIGN = 1:.. MAIN_G_MIN = -SUB_G_MIN_LIMIT. REG_SUB_G_MIN_SIGN = 0:.. MAIN_G_MIN = SUB_G_MIN_LIMIT.
60h (2FC1h)	REG2FC1	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '2FC0h'.
61h (2FC2h)	REG2FC2	7:0	Default : 0x00 Access : R/W
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.
61h (2FC3h)	REG2FC3	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '2FC2h'.
62h (2FC4h)	REG2FC4	7:0	Default : 0x00 Access : R/W
	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_SUB_B_MIN_SIGN = 1:.. MAIN_R_MIN = -SUB_B_MIN_LIMIT. REG_SUB_B_MIN_SIGN = 0:.. MAIN_R_MIN = SUB_B_MIN_LIMIT.
62h (2FC5h)	REG2FC5	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '2FC4h'.
63h (2FC6h)	REG2FC6	7:0	Default : 0x00 Access : R/W
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.
63h (2FC7h)	REG2FC7	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '2FC6h'.
64h ~ 69h (2FC8h ~ 2FD3h)	-	7:0	Default : - Access : -
	-	-	Reserved.
6Ch (2FD8h)	REG2FD8	7:0	Default : 0x00 Access : R/W
	RGB_COMPRESSION_MODE[7:0]	7:0	New add function for RGB_compression.
6Ch (2FD9h)	REG2FD9	7:0	Default : 0x00 Access : R/W
	RGB_COMPRESSION_MODE[15:8]	7:0	See description of '2FD8h'.

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
70h (2FE0h)	REG2FE0	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	FWC_SUB_EN	4	
	-	3:2	Reserved.
	FWC_DITHER_EN	1	
	FWC_MAIN_EN	0	
70h (2FE1h)	REG2FE1	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	FWC_STRENGTH[3:0]	3:0	
71h (2FE2h)	REG2FE2	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	FWC_SLOPE[5:0]	5:0	
71h (2FE3h)	REG2FE3	7:0	Default : 0x00 Access : R/W
	FWC_CTH[7:0]	7:0	
72h (2FE4h)	REG2FE4	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[7:0]	7:0	
72h (2FE5h)	REG2FE5	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[15:8]	7:0	See description of '2FE4h'.
73h (2FE6h)	REG2FE6	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[23:16]	7:0	See description of '2FE4h'.
73h (2FE7h)	REG2FE7	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[31:24]	7:0	See description of '2FE4h'.
74h (2FE8h)	REG2FE8	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[39:32]	7:0	See description of '2FE4h'.
74h (2FE9h)	REG2FE9	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[47:40]	7:0	See description of '2FE4h'.
75h (2FEAh)	REG2FEA	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[55:48]	7:0	See description of '2FE4h'.
75h (2FEBh)	REG2FEB	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[63:56]	7:0	See description of '2FE4h'.
76h (2FECh)	REG2FEC	7:0	Default : 0x80 Access : R/W
	FWC_DELTA_R[71:64]	7:0	See description of '2FE4h'.
76h	REG2FED	7:0	Default : 0x80 Access : R/W

S_VOPREG Register (Bank = 2F, Sub-Bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description
(2FEDh)	FWC_DELTA_R[79:72]	7:0	See description of '2FE4h'.
77h (2FEEh)	REG2FEE	7:0	Default : 0x80
	FWC_DELTA_R[87:80]	7:0	See description of '2FE4h'.
77h (2FEFh)	REG2FEF	7:0	Default : 0x80
	FWC_DELTA_R[95:88]	7:0	See description of '2FE4h'.
7Ah (2FF4h)	REG2FF4	7:0	Default : 0x80
	FWC_DELTA_B[7:0]	7:0	
7Ah (2FF5h)	REG2FF5	7:0	Default : 0x80
	FWC_DELTA_B[15:8]	7:0	See description of '2FF4h'.
7Bh (2FF6h)	REG2FF6	7:0	Default : 0x80
	FWC_DELTA_B[23:16]	7:0	See description of '2FF4h'.
7Bh (2FF7h)	REG2FF7	7:0	Default : 0x80
	FWC_DELTA_B[31:24]	7:0	See description of '2FF4h'.
7Ch (2FF8h)	REG2FF8	7:0	Default : 0x80
	FWC_DELTA_B[39:32]	7:0	See description of '2FF4h'.
7Ch (2FF9h)	REG2FF9	7:0	Default : 0x80
	FWC_DELTA_B[47:40]	7:0	See description of '2FF4h'.
7Dh (2FFAh)	REG2FFA	7:0	Default : 0x80
	FWC_DELTA_B[55:48]	7:0	See description of '2FF4h'.
7Dh (2FFBh)	REG2FFB	7:0	Default : 0x80
	FWC_DELTA_B[63:56]	7:0	See description of '2FF4h'.
7Eh (2FFCh)	REG2FFC	7:0	Default : 0x80
	FWC_DELTA_B[71:64]	7:0	See description of '2FF4h'.
7Eh (2FFDh)	REG2FFD	7:0	Default : 0x80
	FWC_DELTA_B[79:72]	7:0	See description of '2FF4h'.
7Fh (2FFEh)	REG2FFE	7:0	Default : 0x80
	FWC_DELTA_B[87:80]	7:0	See description of '2FF4h'.
7Fh (2FFFh)	REG2FFF	7:0	Default : 0x80
	FWC_DELTA_B[95:88]	7:0	See description of '2FF4h'.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h (2F03h)	REG2F03	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	DB_MASK	0	Double buffer register mask signal. The double buffer register is updated when DB_MASK and DB_LOAD.	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	VSST[7:0]	7:0	Output VSYNC start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
02h (2F05h)	REG2F05	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h - 23h are used to define output VSYNC.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
			1: Registers 20h and 21h are used to define No Signal VSYNC. Registers 22h and 23h are used to define minimum H total.
	VSST[10:8]	2:0	See description of '2F04h'.
03h (2F06h)	REG2F06	7:0	Default : 0x00 Access : R/W
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOV=1). 304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.
03h (2F07h)	REG2F07	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	VSEND[10:8]	2:0	See description of '2F06h'.
04h (2F08h)	REG2F08	7:0	Default : 0x00 Access : R/W
	DEHST[7:0]	7:0	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.
04h (2F09h)	REG2F09	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	DEHST[11:8]	3:0	See description of '2F08h'.
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00 Access : R/W
	DEHEND[7:0]	7:0	Output DE Horizontal END. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	DEHEND[11:8]	3:0	See description of '2F0Ah'.
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00 Access : R/W
	DEVST[7:0]	7:0	Output DE Vertical Start. 00: Default value.
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00 Access : R/W
	VSTSEL	7	Vertical Start Select. 0: DEVST[10:0] is Output DE vertical start. 1: DEVST[10:0] is Scaling Image Window vertical start.
	-	6:4	Reserved.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	DEVST[11:8]	3:0	See description of '2F0Ch'.
07h (2F0Eh)	REG2F0E	7:0	Default : 0x00 Access : R/W
	DEVEND[7:0]	7:0	Output DE Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.
07h (2F0Fh)	REG2F0F	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	DEVEND[11:8]	3:0	See description of '2F0Eh'.
08h (2F10h)	REG2F10	7:0	Default : 0x00 Access : R/W
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start. 48h: Recommended value (power on default is 0).
08h (2F11h)	REG2F11	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SIHST[11:8]	3:0	See description of '2F10h'.
09h (2F12h)	REG2F12	7:0	Default : 0x00 Access : R/W
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.
09h (2F13h)	REG2F13	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SIHEND[11:8]	3:0	See description of '2F12h'.
0Ah (2F14h)	REG2F14	7:0	Default : 0x00 Access : R/W
	SIVST[7:0]	7:0	Scaling Image window Vertical Start.
0Ah (2F15h)	REG2F15	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SIVST[11:8]	3:0	See description of '2F14h'.
0Bh (2F16h)	REG2F16	7:0	Default : 0x00 Access : R/W
	SIVEND[7:0]	7:0	Scaling Image window Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.
0Bh (2F17h)	REG2F17	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
	SIVEND[11:8]	3:0	See description of '2F16h'.	
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	HDTOT[7:0]	7:0	Output Horizontal Total. 53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.	
0Ch (2F19h)	REG2F19	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HDTOT[11:8]	3:0	See description of '2F18h'.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00	Access : R/W
	VDTOT[7:0]	7:0	Output Vertical Total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output.	
0Dh (2F1Bh)	REG2F1B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	VDTOT[11:8]	3:0	See description of '2F1Ah'.	
10h (2F20h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
10h (2F21h)	REG2F21	7:0	Default : 0x4C	Access : R/W
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 - 0x23).	
	OUTM	6	Output Mode. 0: Mode 0. 1: Mode 1.	
	HRSM	5	HSYNC Remove Mode. 0: Normal. 1: Remove HSYNC when GPOA (Bank 2 register 0x62 - 0x6A) is low.	
	VSGP	4	VSYNC use GPO9. 0: Disable. 1: Enable (using Bank 2 register 0x59 - 0x61 to define OVSYNC).	
	EHTT	3	Even H Total. 0: Enable, Output H Total is always even pixels.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
			1: Disable, Output H Total is always odd pixels.
	MOD2	2	Mode 2. 0: Disable. 1: Enable.
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.
11h (2F22h)	REG2F22	7:0	Default : 0x00 Access : R/W
	FPLMD0	7	Frame PLL Mode 0.
	SL_TUNE_EN	6	Short line tune enable.
	AUTO_H_TOTAL_UPDATE_EN	5	Enable update AUTO_H_TOTAL value to H_TOTAL.
	-	4:2	Reserved.
	SSC_SHIFT	1	0: Enable. 1: Disable.
	CLKDIV2_POINT_SELECT	0	0: Original. 1: New.
11h (2F23h)	-	7:0	Default : - Access : -
	-	-	Reserved.
12h (2F24h)	REG2F24	7:0	Default : 0x20 Access : R/W
	LCK_TH[7:0]	7:0	Frame PLL Lock Threshold.
12h (2F25h)	REG2F25	7:0	Default : 0x08 Access : R/W
	LCK_TH[15:8]	7:0	See description of '2F24h'.
13h (2F26h)	REG2F26	7:0	Default : 0x10 Access : R/W
	FTNF[7:0]	7:0	Frame Tune Number of Frame.
13h (2F27h)	REG2F27	7:0	Default : 0x10 Access : R/W
	FTNS[3:0]	7:4	Tune Frame Number of Short-line tune.
	-	3	Reserved.
	PIP_REG_EN	2	PIP Register Enable.
	FPLL_REP_EN	1	Frame PLL Report Enable.
	NOISY_GEN	0	Noise Generator.
14h	REG2F28	7:0	Default : 0x00 Access : R/W

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
(2F28h)	PPLL_LMT1[7:0]	7:0	Frame PLL Limit.
14h (2F29h)	REG2F29 PPLL_LMT0[7:0]	7:0	Default : 0x00 Frame PLL Limit.
15h (2F2Ah)	REG2F2A PPLL_LMT[7:0]	7:0	Default : 0x00 Frame PLL Limit.
15h (2F2Bh)	REG2F2B FPLL_LMT_OFST0[7:0]	7:0	Default : 0x00 Frame PLL Limit Offset low byte.
16h (2F2Ch)	REG2F2C FPLL_LMT_OFST1[7:0]	7:0	Default : 0x00 Frame PLL Limit Offset high byte.
16h (2F2Dh)	REG2F2D M_HBC_GAIN[3:0] M_HBC_EN M_HBC_ROUNDING - BRC	7:0 7:4 3 2 1 0	Default : 0xF0 Main window High brightness gain. Main window High brightness enable. Main window High brightness enable. Reserved. Brightness function. 0: Off. 1: On.
19h (2F32h)	REG2F32 ADEAD_EN SWBLBK SWBLUE S_FMCLR_EN - MBD_EN MBLK NOSC_EN	7:0 7 6 5 4 3 2 1 0	Default : 0x00 Ahead mode enable. Sub window Blue screen color. 0: Black color. 1: Blue color. Sub window Blue screen control. 0: Off. 1: On. Sub window frame color enable. Reserved. Main window Border Enable. Main window Black screen control. 0: Off. 1: On. No Signal Color Enable.
19h (2F33h)	REG2F33 FCL_R[7:0]	7:0 7:0	Default : 0x00 Frame Color - Red.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
1Ah (2F34h)	REG2F34	7:0	Default : 0x00 Access : R/W
	FCL_G[7:0]	7:0	Frame Color - Green.
1Ah (2F35h)	REG2F35	7:0	Default : 0x00 Access : R/W
	FCL_B[7:0]	7:0	Frame Color - Blue.
1Bh (2F36h)	REG2F36	7:0	Default : 0x02 Access : R/W
	DITHG[1:0]	7:6	Dither coefficient for G channel.
	DITHB[1:0]	5:4	Dither coefficient for B channel.
	SROT	3	Spatial coefficient Rotate. 0: Disable. 1: Enable.
	TROT	2	Temporal coefficient Rotate. 0: Disable. 1: Enable.
	OBN	1	Output Bits Number (used for 8/10-bit gamma). 0: 8-bit output. 1: 6-bit output (power on default value).
	DITH	0	Dither function. 0: Off. 1: On.
1Bh (2F37h)	REG2F37	7:0	Default : 0x2D Access : R/W
	TL[1:0]	7:6	Top - Left dither coefficient.
	TR[1:0]	5:4	Top - Right dither coefficient.
	BL[1:0]	3:2	Bottom - Left dither coefficient.
	BR[1:0]	1:0	Bottom - Right dither coefficient.
1Ch (2F38h)	REG2F38	7:0	Default : 0x00 Access : R/W
	RST_E_4_FRAME	7	Reset noise generator by frames enable.
	NDMD	6	Noise Dithering Method.
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.
	DT3	3	Dither Type 2 control. 0: Disable dither type 2.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Enable dither type 2.	
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.	
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.	
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SHORT_1LINE_DISABLE	6	1: Disable. 0: Enable.	
	-	5	Reserved.	
	EGWT	4	Encode Gamma Write.	
	HTOTAL	3	H Total End 11.	
	HDE_END	2	HDE End 11.	
	HFDE_END	1	HFDE END 11.	
	OUTFRR_EN0	0	Output Free-run Enable.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x03	Access : R/W
	IVS_DIFF_THR[7:0]	7:0	Input vs Different Thresholds.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x07	Access : R/W
	TUNE_FIELD_IP	7	Select insert point of one field for VOP_DISP inset signal.	
	IVS_STB_THR[6:0]	6:0	Input vs Stable Thresholds.	
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x00	Access : R/W
	LMT_ADD_NMB[7:0]	7:0	Limit adjust Number in ACC_FPLL mode.	
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00	Access : R/W
	FPLL_MD1	7	FPLL Mode 1.	
	FPLL_DIS	6	FPLL Stop.	
	ACC1_SEL[1:0]	5:4	Select modify numbers. 00: 3/4 diff numbers. 01: 1/2 diff numbers. Others: 1/4 diff numbers.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	-	3	Reserved.
	ADD_LINE_SEL	2	Select Add Line into frame or pixel into line.
	CH_CH_MD1	1	ACC FPLL Mode 1.
	CH_CH_MD0	0	ACC FPLL Mode 0.
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00
	IVS_PRD_NUM[7:0]	7:0	Count Number per Input v.s.
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00
	-	7:4	Reserved.
	IVS_PRD_NUM[11:8]	3:0	See description of '2F3Eh'.
21h (2F42h)	REG2F42	7:0	Default : 0x00
	LCPS	7	LVDS Channel Polarity Swap (P/N swap). 0: Disable. 1: Enable.
	LCS	6	LVDS Channel Swap. 0: Disable. 1: Enable. When enabled in dual LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap, LVB0M/LVB3M swap, LVB0P/LVB3P swap, LVB1M/LVBCKM swap, LVB1P/LVBCKP swap. When enabled in single LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap.
	MLXT0	5	MSB/LSB Exchange Type for 6/8/10-bit.
	LTIM	4	LVDS TI Mode. 0: Normal. 1: TI Mode.
	OMLX	3	Odd channel MSB/LSB Exchange. 0: Normal. 1: Exchange.
	EMLX	2	Even channel MSB/LSB Exchange. 0: Normal. 1: Exchange.
	ORBX	1	Odd channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
	ERBX	0	Even channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.	
21h (2F43h)	REG2F43	7:0	Default : 0x00	Access : R/W
	MLXT1	7	MSB/LSB Exchange Type for 6/8/10-bit.	
	DOT	6	Differential Output Type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/Increased-swing RSDS.	
	WHTS	5	White Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	BLSK	4	Black Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	REVERSE	3	REVERSE luminosity. 0: Off. 1: On.	
	STO	2	Stagger Output (only used when DPO=1). 0: Disable. 1: Enable.	
	DPX	1	A/B Port Swap (only used when DPO=1). 0: Disable. 1: Enable.	
	DUAL_PIXEL_OUTPUT	0	Dual Pixel Output. 0: Single pixel. 1: Dual pixel.	
22h (2F44h)	REG2F44	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	AB_SWAP	5	LVDS AB Port Swap.	
	CKSEL[4:0]	4:0	Enable clock of internal control. 00h: TTL output. 11H: Single LVDS output. 13h: Dual LVDS output.	
22h (2F45h)	REG2F45	7:0	Default : 0x00	Access : R/W
	FBLALL_SET	7	Frame buffer less all set.	
	PUT_REG_PTT1	6	Register overwrite 0 bit 1.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	PDP10BIT	5	PDP 10 bits mode, support single 10 bit LVDS PDP.
	TTL_LVDS	4	TTL LVDS mode, let single TTL and LVDS use same board.
	BRGS	3	B port pixel R/G Swap. 0: Disable. 1: Enable.
	ARGS	2	A port pixel R/G Swap. 0: Disable. 1: Enable.
	BGBS	1	B port pixel G/B Swap. 0: Disable. 1: Enable.
	AGBS	0	A port pixel G/B Swap. 0: Disable. 1: Enable.
23h (2F46h)	REG2F46	7:0	Default : 0x00 Access : R/W
	OSDCHBLEND	7	OSD Character Blending mode.
	-	6	Reserved.
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).
	-	4	Reserved.
	GATP	3	Gamma Automatically On/Off based on Auto Phase value. 0: Disable. 1: Enable.
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.
24h (2F48h)	REG2F48	7:0	Default : 0x00 Access : R/W
	MNS_COL[7:0]	7:0	Main Window No Signal Color.

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
24h (2F49h)	REG2F49	7:0	Default : 0x00	Access : R/W
	MBCOL[7:0]	7:0	Main Window Border Color.	
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00	Access : R/W
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	SLOW_RAW_LIM[3:0]	6:3	Raw_threshold in FPLL_tune_slow.	
	SLOW_CNT_LIM[2:0]	2:0	Count threshold.	
25h (2F4Bh)	REG2F4B	7:0	Default : 0x00	Access : R/W
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLOCK_DL_LN[2:0]	5:3	Delay line number in Flock mode.	
	FLOCK_AH_LN[2:0]	2:0	Ahead line in Flock mode.	
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00	Access : R/W
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '2F4Ch'.	
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '2F4Eh'.	
28h (2F50h)	REG2F50	7:0	Default : 0x00	Access : R/W
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '2F50h'.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : R/W
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '2F52h'.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
2Ah	REG2F55	7:0	Default : 0x00	Access : R/W

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F55h)	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x00	Access : R/W
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x00	Access : R/W
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
2Eh (2F5Dh)	REG2F5D	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '2F5Ch'.	
2Fh (2F5Eh)	REG2F5E	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
	RRAN	2	Red Range. 0: 0~255. 1: -128~127.	
	GRAN	1	Green Range. 0: 0~255.1: -128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: -128~127.	
2Fh (2F5Fh)	REG2F5F	7:0	Default : 0x00	Access : R/W
	SSFD	7	Sub window Shift Field. 0: Shift even field. 0: Shift odd field.	
	SSLN[1:0]	6:5	Sub window Shift Line Numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.	
	ILIM	4	Insert Line when Interlace Mode. 0: Do not insert. 1: Insert.	
	MSFD	3	Main window Shift Field. 0: Shift even field. 1: Shift odd field.	
	MSLN[2:0]	2:0	Main window Shift Line Numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 lines between odd and even field. 010: Shift 2 lines between odd and even field. 011: Shift 3 lines between odd and even field. 1xx: Shift 4 lines between odd and even field.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : RO
	IFVP[7:0]	7:0	Insert Fraction Vertical Position.	
30h (2F61h)	REG2F61	7:0	Default : 0x00	Access : RO
	IFVP[15:8]	7:0	See description of '2F60h'.	
31h (2F62h)	REG2F62	7:0	Default : 0x00	Access : RO
	IFRACTW[7:0]	7:0	Insert Fraction Width. PD Down value.	
31h	REG2F63	7:0	Default : 0x00	Access : RO

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
(2F63h)	IFRACTW[15:8]	7:0	See description of '2F62h'.
32h (2F64h)	REG2F64	7:0	Default : 0x00 Access : RO
	OVSTAT[7:0]	7:0	Output Vertical Total Status. Lock status. Equal to 1 when phase error less than 29h/2Ah.
32h (2F65h)	REG2F65	7:0	Default : 0x00 Access : RO
	-	7	Reserved.
	OVERDESTAT	6	Output Vertical DE Status.
	-	5:3	Reserved.
	OVSTAT[10:8]	2:0	See description of '2F64h'.
33h (2F66h)	REG2F66	7:0	Default : 0x00 Access : R/W
	OHTSTAT0[7:0]	7:0	OHSTAT initial value.
34h (2F68h)	REG2F68	7:0	Default : 0x00 Access : RO
	OHTSTAT1[7:0]	7:0	Output H Total Status.
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.
37h (2F6Eh)	REG2F6E	7:0	Default : 0x00 Access : R/W
	FRACST0[7:0]	7:0	Fraction initial value.
38h (2F70h)	REG2F70	7:0	Default : 0x00 Access : RO
	FRACST1[7:0]	7:0	Fraction Status.
39h (2F72h)	REG2F72	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	FRACST2[2:0]	2:0	Fraction Status.
3Ah (2F74h)	REG2F74	7:0	Default : 0x00 Access : RO
	-	7:3	Reserved.
	FRACST3[2:0]	2:0	Fraction Status.
3Bh (2F76h)	REG2F76	7:0	Default : 0x00 Access : R/W
	HTTMGN[7:0]	7:0	H Total Margin.
3Bh	REG2F77	7:0	Default : 0x00 Access : R/W

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
(2F77h)	SSCMGN[7:0]	7:0	SSC Margin.
3Ch (2F78h)	REG2F78	7:0	Default : 0x00
	RSTVALUE0[7:0]	7:0	Read Start initial value.
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00
	RSTVALUE1[7:0]	7:0	Read Start Value.
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0x00
	-	7:5	Reserved.
	RSTVALUE2[4:0]	4:0	Read Start initial value.
3Fh (2F7Eh)	REG2F7E	7:0	Default : 0x00
	-	7:5	Reserved.
	RSTVALUE3[4:0]	4:0	Read Start Value.
40h (2F80h)	REG2F80	7:0	Default : 0x00
	-	7:6	Reserved.
	FRONT_BACK	5	Set front back mode.
	-	4:0	Reserved.
41h (2F82h)	REG2F82	7:0	Default : 0x00
	INP8	7	This bit with REG_INE_DRV3 to enable G replace R and B for gamma mapping.
	ONE_DRV3	6	Gamma use G replace R and B for gamma mapping.
	GABYP	5	By pass gamma function.
	-	4:3	Reserved.
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.
41h (2F83h)	REG2F83	7:0	Default : 0x00
	TSTDATA[7:0]	7:0	Reserved.
42h (2F84h)	REG2F84	7:0	Default : 0x00
	LFCOEF1[2:0]	7:5	Loop filter coefficient 1.
	LFCOEF2[4:0]	4:0	Loop filter coefficient 2.
42h (2F85h)	REG2F85	7:0	Default : 0x00
	TUNE_SLOW[7:0]	7:0	Tune number for OVDE lock value fine tune.
43h (2F86h)	REG2F86	7:0	Default : 0x00
	TFRACN[7:0]	7:0	Target Fraction Number. / Frame PLL limit RK[7:0].
45h	REG2F8A	7:0	Default : 0x00
			Access : RO, R/W

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
2F8Ah	-	7	Reserved.
	PDP_MASK_EN	6	Reserved.
	-	5	Reserved.
	FX_PROT	4	Frame Change Protect.
	-	3:0	Reserved.
45h (2F8Bh)	REG2F8B	7:0	Default : 0x40 Access : R/W
	-	7	Reserved.
	EOCK	6	Use External Clock (pin) as Output Dot Clock. 0: Disable (use internal dot clock). 1: Enable (use external dot clock).
	SEE_DEBUG_SEL[2:0]	5:3	See Debug bus output byte enable, bit0=DI[7:0], bit1=DI[15:8], bit2=DI[23:16].
	BPM	2	Bypass clock Mode (IDCLK as ODCLK). 0: Disable. 1: Enable.
	PTEN	1	PLL Test register protect bit. 0: Disable. 1: Enable.
	LRTM	0	LVDS/RSDS Test Mode enable. 0: Disable. 1: Enable.
46h (2F8Ch)	REG2F8C	7:0	Default : 0x00 Access : R/W
	CLKDLYSEL[3:0]	7:4	OCLKDLY[3:0]: OCLK Delay adjustment (TCON feature only). 0: 16 step to adjust. 1: Typical 0.8ns delay/step.
	OCLK	3	Output CLK control. 0: Normal. 1: Invert.
	ODE	2	Output DE control. 0: Active high. 1: Active low.
	OVS	1	Output VSYNC control. 0: Active high. 1: Active low.
	OHS	0	Output HSYNC control.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
			0: Active high. 1: Active low.
46h (2F8Dh)	REG2F8D	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	OEDB	5	Output Even Data Bus pin control. 0: Normal. 1: Tri-state.
	OODB	4	Output Odd Data Bus pin control. 0: Normal. 1: Tri-state.
	OVS0	3	OVSYNC pin control. 0: Normal. 1: Tri-state.
	OHS0	2	OHSYNC pin control. 0: Normal. 1: Tri-state.
	ODE0	1	ODE pin control. 0: Normal. 1: Tri-state.
	OCLK0	0	OCLK pin control. 0: Normal. 1: Tri-state.
47h (2F8Eh)	REG2F8E	7:0	Default : 0x00 Access : R/W
	DEDRV[1:0]	7:6	Output DE Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.
	CLKDRV[1:0]	5:4	Output Clock Driving current select. 00: 4mA.01: 6mA. 10: 8mA. 11: 12mA.
	ODDDRV[1:0]	3:2	Output data Odd channel Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	EVENDRV[1:0]	1:0	Output data Even channel Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.
48h (2F90h)	REG2F90	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	SKEW[1:0]	5:4	Output data SKEW.
	ECLKDLY[3:0]	3:0	ECLK Delay adjustment (TCON feature only). 0: 16 steps to adjust. 1: Typical 0.8ns delay/step.
48h (2F91h)	REG2F91	7:0	Default : 0x00 Access : R/W
	TEST_CLK_MODE	7	0: Disable. 1: Enable.
	PLL_DIV2	6	0: Normal. 1: Test clock output divided by 2.
	DDR_TEST	5	1: Select DDR 29est bus.
	TEST_MD_D	4	1: Enable 24-bit test bus output.
	TEST_MD[3:0]	3:0	Reserved.
49h (2F92h)	REG2F92	7:0	Default : 0x00 Access : R/W
	BIST_STS[7:0]	7:0	Reserved.
49h (2F93h)	REG2F93	7:0	Default : 0x00 Access : R/W
	CHIPID[7:0]	7:0	Chip ID.
4Ah (2F94h)	REG2F94	7:0	Default : 0x00 Access : RO
	BOND_STS[7:0]	7:0	Reserved.
4Bh (2F96h)	REG2F96	7:0	Default : 0x44 Access : R/W
	LP_SET0[7:0]	7:0	Output PLL Set.
4Bh (2F97h)	REG2F97	7:0	Default : 0x55 Access : R/W
	LP_SET0[15:8]	7:0	See description of '2F96h'.
4Ch (2F98h)	REG2F98	7:0	Default : 0x00 Access : R/W
	LP_SET1[7:0]	7:0	Output PLL Set.
50h (2FA0h)	REG2FA0	7:0	Default : 0x00 Access : R/W
	OBN10	7	10-bit Bus enable.
	DITHER_MINUS	6	1: Enable.

VOPREG Register (Bank = 2F, Sub-Bank = 10)				
Index (Absolute)	Mnemonic	Bit	Description	
	GPODDC	5	GPO, GPO[3] use for DDC DAT/CLK.	
	M_GRG	4	Main window Gamma Rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	
52h (2FA4h)	REG2FA4	7:0	Default : 0x00	Access : R/W
	OSD_HS_ST[7:0]	7:0	Osd new reference h start.	
52h (2FA5h)	REG2FA5	7:0	Default : 0x00	Access : R/W
	OSD_NEW_REF	7	Osd new reference enable.	
	-	6:4	Reserved.	
	OSD_HS_ST[11:8]	3:0	See description of '2FA4h'.	
53h (2FA6h)	REG2FA6	7:0	Default : 0x00	Access : R/W
	OSD_HS_END[7:0]	7:0	Osd new reference h end.	
53h (2FA7h)	REG2FA7	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	OSD_HS_END[11:8]	3:0	See description of '2FA6h'.	
54h (2FA8h)	REG2FA8	7:0	Default : 0x00	Access : R/W
	OSD_VFDE_ST[7:0]	7:0	Osd new reference v start.	
54h (2FA9h)	REG2FA9	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	OSD_VFDE_ST[10:8]	2:0	See description of '2FA8h'.	
55h (2FAAh)	REG2FAA	7:0	Default : 0x00	Access : R/W
	OSD_VFDE_END[7:0]	7:0	Osd new reference v end.	
55h (2FABh)	REG2FAB	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	OSD_VFDE_END[10:8]	2:0	See description of '2FAAh'.	
56h (2FACH)	REG2FAC	7:0	Default : 0x00	Access : R/W
	LIM_HS	7	Limit Htotal by PWM counter enable.	
	NEW_FIELD_SEL	6	Select field created method. 0: Created by Vsync and Hsync. 1: Created by VFDE.	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end.	

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
			1: Vsync end.
	-	4:0	Reserved.
57h (2FAEh)	REG2FAE	7:0	Default : 0x00 Access : RO
	REM[7:0]	7:0	Htoal REMainder value.
57h (2FAFh)	REG2FAF	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	REM[11:8]	3:0	See description of '2FAEh'.
58h (2FB0h)	REG2FB0	7:0	Default : 0x00 Access : R/W
	PWM5DIV[7:0]	7:0	PWM5 CLK div factor.
58h (2FB1h)	REG2FB1	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	PWM5DIV[8]	0	See description of '2FB0h'.
59h (2FB2h)	REG2FB2	7:0	Default : 0x00 Access : R/W
	PWM5DUTY[7:0]	7:0	PWM5 period.
5Ah (2FB4h)	REG2FB4	7:0	Default : 0x00 Access : R/W
	TRACE_PHASE_HTOTAL[7:0]	7:0	New Htotal for fast phase offset reduce, only active when REG_TRACE_PHASE_EN is set to 1.
5Ah (2FB5h)	REG2FB5	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	NEW_HBC_CLAMP	6	Clamp function for HBC gain.
	NEW_HBC_GAIN	5	HBC gain mode. 0: 0.4. 1: 0.04.
	TRACE_PHASE_EN	4	Enable modify Htotal for fast phase offset reduce.
	TRACE_PHASE_HTOTAL[11:8]	3:0	See description of '2FB4h'.
64h (2FC8h)	REG2FC8	7:0	Default : 0x07 Access : R/W
	BIUCLK_DIV[7:0]	7:0	Calculate VDE ratio BIUCLK divider.
64h (2FC9h)	REG2FC9	7:0	Default : 0x00 Access : R/W
	-	7:1	Reserved.
	RPT_VRATIO_EN	0	Report VDE Vtotal ratio enable.
65h (2FCAh)	REG2FCA	7:0	Default : 0x00 Access : R/W
	PIP_OP2_0_REG[7:0]	7:0	
65h	REG2FCB	7:0	Default : 0x00 Access : R/W

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
(2FCBh)	PIP_OP2_1_REG[7:0]	7:0	
66h (2FCCh)	REG2FCC	7:0	Default : 0x00
	PIP_OP2_2_REG[7:0]	7:0	Access : R/W
66h (2FCDh)	REG2FCD	7:0	Default : 0x00
	PIP_OP2_3_REG[7:0]	7:0	Access : R/W
67h (2FCEh)	REG2FCE	7:0	Default : 0x00
	PIP_OP2_4_REG[7:0]	7:0	Access : R/W
67h (2FCFh)	REG2FCF	7:0	Default : 0x00
	PIP_OP2_5_REG[7:0]	7:0	Access : R/W
68h (2FD0h)	REG2FD0	7:0	Default : 0x00
	VDE_PRD_VALUE[7:0]	7:0	Access : RO Input VDE PRD value.
68h (2FD1h)	REG2FD1	7:0	Default : 0x00
	VDE_PRD_VALUE[15:8]	7:0	Access : RO See description of '2FD0h'.
69h (2FD2h)	REG2FD2	7:0	Default : 0x00
	VTT_PRD_VALUE[7:0]	7:0	Access : RO Input Vtt PRD value.
69h (2FD3h)	REG2FD3	7:0	Default : 0x00
	VTT_PRD_VALUE[15:8]	7:0	Access : RO See description of '2FD2h'.
6Ah (2FD4h)	REG2FD4	7:0	Default : 0x00
	HIFRC_SROT	7	Access : R/W Enable HIFRC spatial rotation.
	RAN[1:0]	6:5	Enable HIFRC Random noise latch for rotation.
	F2_EN	4	Enable noise repeats 2 frames.
	NEW_DITH_M	3	New dither method select.
	-	2	Reserved.
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.
6Ah (2FD5h)	REG2FD5	7:0	Default : 0x00
	-	7	Access : R/W Reserved.
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.
	H_RAN_EN	3	H direction using random noise enable for HIFRC.
	NEW_ACBD	2	Swap HIFRC probability sequence.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	OLD_HIFRC	1	Select old HIFRC dither method.
	RAN_DIR_EN	0	Enable noise as rotate direction.
6Ch (2FD8h)	REG2FD8	7:0	Default : 0x00
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table r/w address.
6Dh (2FDAh)	REG2FDA	7:0	Default : 0x00
	LUT_W_FLAG2	7	LUT table blue write command.
	LUT_W_FLAG1	6	LUT table green write command.
	LUT_W_FLAG0	5	LUT table red write command.
	-	4:0	Reserved.
6Dh (2FDBh)	REG2FDB	7:0	Default : 0x00
	LUT_R_FLAG2	7	LUT table blue read command.
	LUT_R_FLAG1	6	LUT table green read command.
	LUT_R_FLAG0	5	LUT table red read command.
	-	4:0	Reserved.
6Eh (2FDCh)	REG2FDC	7:0	Default : 0x00
	WR_R[7:0]	7:0	Data write to R LUT SRAM.
6Eh (2FDDh)	REG2FDD	7:0	Default : 0x00
	-	7:4	Reserved.
	WR_R[11:8]	3:0	See description of '2FDCh'.
6Fh (2FDEh)	REG2FDE	7:0	Default : 0x00
	WR_G[7:0]	7:0	Data write to G LUT SRAM.
6Fh (2FDFh)	REG2FDF	7:0	Default : 0x00
	-	7:4	Reserved.
	WR_G[11:8]	3:0	See description of '2FDEh'.
70h (2FE0h)	REG2FE0	7:0	Default : 0x00
	WR_B[7:0]	7:0	Data write to B LUT SRAM.
70h (2FE1h)	REG2FE1	7:0	Default : 0x00
	-	7:4	Reserved.
	WR_B[11:8]	3:0	See description of '2FE0h'.
71h (2FE2h)	REG2FE2	7:0	Default : 0x00
	RD_R[7:0]	7:0	Data read from R LUT SRAM.
71h (2FE3h)	REG2FE3	7:0	Default : 0x00
	-	7:4	Reserved.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	RD_R[11:8]	3:0	See description of '2FE2h'.
72h (2FE4h)	REG2FE4	7:0	Default : 0x00 Access : RO
	RD_G[7:0]	7:0	Data read from G LUT SRAM.
72h (2FE5h)	REG2FE5	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	RD_G[11:8]	3:0	See description of '2FE4h'.
73h (2FE6h)	REG2FE6	7:0	Default : 0x00 Access : RO
	RD_B[7:0]	7:0	Data read from B LUT SRAM.
73h (2FE7h)	REG2FE7	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	RD_B[11:8]	3:0	See description of '2FE6h'.
74h (2FE8h)	REG2FE8	7:0	Default : 0x00 Access : RO, R/W
	-	7:4	Reserved.
	CLR_MLOAD_TOO_SLOW	3	Clear auto mload gamma too slow flag.
	MLOAD_TOO_SLOW	2	Auto mload gamma too slow flag.
	AUTO_MLOAD_SWITCH	1	Enable auto mload gamma switch gamma table by frame.
	AUTO_MLOAD_GAMMA	0	Enable auto mload gamma function.
75h (2FEAh)	REG2FEA	7:0	Default : 0x00 Access : R/W
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.
75h (2FEBh)	REG2FEB	7:0	Default : 0x00 Access : R/W
	MLOAD_GAMMA_BASE0[15:8]	7:0	See description of '2FEAh'.
76h (2FEC h)	REG2FEC	7:0	Default : 0x00 Access : R/W
	MLOAD_GAMMA_BASE0[23:16]	7:0	See description of '2FEAh'.
77h (2FEEh)	REG2FEE	7:0	Default : 0x00 Access : R/W
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.
77h (2FEFh)	REG2FEF	7:0	Default : 0x00 Access : R/W
	MLOAD_GAMMA_BASE1[15:8]	7:0	See description of '2FEEh'.
78h (2FF0h)	REG2FF0	7:0	Default : 0x00 Access : R/W
	MLOAD_GAMMA_BASE1[23:16]	7:0	See description of '2FEEh'.
79h (2FF2h)	REG2FF2	7:0	Default : 0x00 Access : R/W
	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.
7Ah (2FF4h)	REG2FF4	7:0	Default : 0x00 Access : R/W
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.

VOPREG Register (Bank = 2F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
7Ah (2FF5h)	REG2FF5	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	R_MAX_BASE0[11:8]	3:0	See description of '2FF4h'.
7Bh (2FF6h)	REG2FF6	7:0	Default : 0x00 Access : R/W
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.
7Bh (2FF7h)	REG2FF7	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	R_MAX_BASE1[11:8]	3:0	See description of '2FF6h'.
7Ch (2FF8h)	REG2FF8	7:0	Default : 0x00 Access : R/W
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.
7Ch (2FF9h)	REG2FF9	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	G_MAX_BASE0[11:8]	3:0	See description of '2FF8h'.
7Dh (2FFAh)	REG2FFA	7:0	Default : 0x00 Access : R/W
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.
7Dh (2FFBh)	REG2FFB	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	G_MAX_BASE1[11:8]	3:0	See description of '2FFAh'.
7Eh (2FFCh)	REG2FFC	7:0	Default : 0x00 Access : R/W
	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.
7Eh (2FFDh)	REG2FFD	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	B_MAX_BASE0[11:8]	3:0	See description of '2FFCh'.
7Fh (2FFEh)	REG2FFE	7:0	Default : 0x00 Access : R/W
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.
7Fh (2FFFh)	REG2FFF	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	B_MAX_BASE1[11:8]	3:0	See description of '2FFEh'.

SCMI Register (Bank = 2F, Sub-Bank = 12)

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data config from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data config from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data config from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data config from mode 5 change to mode 4.	
01h (2F03h)	REG2F03	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	

SCMI Register (Bank = 2F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
	STILL_MODE_F2	3	F2 image freeze enable.
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.
02h (2F04h)	REG2F04	7:0	Default : 0x00 Access : R/W
	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.
02h (2F05h)	REG2F05	7:0	Default : 0x04 Access : R/W
	CAPTURE_START_F2	7	F2 image capture start.
	IPM_READ_OFF_F2	6	F2 force IP read request disable.
	MADI_FORCE_OFF_F2	5	F2 force madi off.
	MADI_FORCE_ON_F2	4	F2 force madi on.
	FBL_25D	3	F2 frame buffer less de-interlace mode.
	YC_SEPARATE_F2	2	F2 YC separate in FB.
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.
03h (2F06h)	REG2F06	7:0	Default : 0x00 Access : R/W
	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.
	DUMMY03_6_6	6	
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.
	IPM_LINEAR_EN_F2	4	F2 IP linear address enable.
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.
03h (2F07h)	REG2F07	7:0	Default : 0x08 Access : R/W
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.
	DOT_LN_PON_SEL_F2	1	F2 OP MADi dot line data select.
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.
04h	REG2F08	7:0	Default : 0x00 Access : R/W

SCMI Register (Bank = 2F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
(2F08h)	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.
	-	6:4	Reserved.
	DUMMY04_2_3[1:0]	3:2	
	BOB_YMR_10_EN_F2	1	F2 10-bits Bob mode with Y motion.
	BOB_YMR_8_EN_F2	0	F2 8-bits Bob mode with Y motion.
04h (2F09h)	REG2F09	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	Y8_ONLY_MODE_F2	6	F2 FB store Y-8bits only.
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.
	IP_2FRAME_BYPASS_F2	4	F2 IP bypass two frames data to OPM.
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00 Access : R/W
	DUMMY05_4_15[3:0]	7:4	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00 Access : R/W
	DUMMY05_4_15[11:4]	7:0	See description of '2F0Ah'.
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00 Access : R/W
	DUMMY06_0_15[7:0]	7:0	
06h (2F0Dh)	REG2F0D	7:0	Default : 0x00 Access : R/W
	DUMMY06_0_15[15:8]	7:0	See description of '2F0Ch'.
07h (2F0Eh)	REG2F0E	7:0	Default : 0x88 Access : R/W
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.
07h	REG2F0F	7:0	Default : 0x00 Access : R/W

SCMI Register (Bank = 2F, Sub-Bank = 12)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F0Fh)	RW_BANK_MAP_F2[1:0]	7:6	F2 read/write bank mapping mode.	
	4FRAME_MODE_F2	5	F2 4 frames buffer for progressive mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	
08h (2F10h)	REG2F10	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (2F11h)	REG2F11	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '2F10h'.	
09h (2F12h)	REG2F12	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '2F10h'.	
0Ah (2F14h)	REG2F14	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR1_F2[7:0]	7:0	F2 IP frame buffer base address 1.	
0Ah (2F15h)	REG2F15	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR1_F2[15:8]	7:0	See description of '2F14h'.	
0Bh (2F16h)	REG2F16	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR1_F2[23:16]	7:0	See description of '2F14h'.	
0Ch (2F18h)	REG2F18	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR2_F2[7:0]	7:0	F2 IP frame buffer base address 2.	
0Ch (2F19h)	REG2F19	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR2_F2[15:8]	7:0	See description of '2F18h'.	
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00	Access : R/W
	IPM_BASE_ADDR2_F2[23:16]	7:0	See description of '2F18h'.	
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00	Access : R/W
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IPM_OFFSET_F2[11:8]	3:0	See description of '2F1Ch'.	
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x00	Access : R/W
	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (2F1Fh)	REG2F1F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IPM_FETCH_NUM_F2[11:8]	3:0	See description of '2F1Eh'.	

SCMI Register (Bank = 2F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
10h (2F20h)	REG2F20	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.
10h (2F21h)	REG2F21	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '2F20h'.
11h (2F22h)	REG2F22	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '2F20h'.
12h (2F24h)	REG2F24	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.
12h (2F25h)	REG2F25	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '2F24h'.
13h (2F26h)	REG2F26	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '2F24h'.
14h (2F28h)	REG2F28	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR2_F2[7:0]	7:0	F2 OP frame buffer base address 2.
14h (2F29h)	REG2F29	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR2_F2[15:8]	7:0	See description of '2F28h'.
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00 Access : R/W
	OPM_BASE_ADDR2_F2[23:16]	7:0	See description of '2F28h'.
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00 Access : R/W
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).
16h (2F2Dh)	REG2F2D	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	OPM_OFFSET_F2[11:8]	3:0	See description of '2F2Ch'.
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00 Access : R/W
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.
17h (2F2Fh)	REG2F2F	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '2F2Eh'.
18h (2F30h)	REG2F30	7:0	Default : 0x00 Access : R/W
	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.
18h (2F31h)	REG2F31	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	IPM_VCNT_LIMIT_EN_F2	4	F2 IP line count limit enable.

SCMI Register (Bank = 2F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
	IPM_VCNT_LIMIT_NUM_F2[11:8]	3:0	See description of '2F30h'.
1Ah (2F34h)	REG2F34	7:0	Default : 0x00
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.
1Ah (2F35h)	REG2F35	7:0	Default : 0x00
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '2F34h'.
1Bh (2F36h)	REG2F36	7:0	Default : 0x00
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '2F34h'.
1Bh (2F37h)	REG2F37	7:0	Default : 0x00
	-	7:2	Reserved.
	IPM_W_LIMIT_EN_F2	1	F2 IP write limit enable.
	IPM_W_LIMIT_MIN_F2	0	F2 IP write limit flag 0: maximum 1: minimum.
1Ch (2F38h)	REG2F38	7:0	Default : 0x00
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.
1Ch (2F39h)	REG2F39	7:0	Default : 0x00
	-	7:5	Reserved.
	SW_HMIR_OFFSET_EN_F2	4	F2 IP H mirror line offset software setting enable.
	SW_HMIR_OFFSET_F2[11:8]	3:0	See description of '2F38h'.
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x00
	DUMMY1D_0_15[7:0]	7:0	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x00
	DUMMY1D_0_15[15:8]	7:0	See description of '2F3Ah'.
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x00
	DUMMY1E_0_15[7:0]	7:0	
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00
	DUMMY1E_0_15[15:8]	7:0	See description of '2F3Ch'.
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0x00
	DUMMY1F_0_15[7:0]	7:0	
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00
	DUMMY1F_0_15[15:8]	7:0	See description of '2F3Eh'.
20h (2F40h)	REG2F40	7:0	Default : 0x10
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.
20h (2F41h)	REG2F41	7:0	Default : 0x10
	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.

SCMI Register (Bank = 2F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
21h (2F42h)	REG2F42	7:0	Default : 0x10 Access : R/W
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.
21h (2F43h)	REG2F43	7:0	Default : 0x10 Access : R/W
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.
22h (2F44h)	REG2F44	7:0	Default : 0x10 Access : R/W
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.
22h (2F45h)	REG2F45	7:0	Default : 0x10 Access : R/W
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.
23h (2F46h)	REG2F46	7:0	Default : 0x10 Access : R/W
	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.
23h (2F47h)	REG2F47	7:0	Default : 0x10 Access : R/W
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.
24h (2F48h)	REG2F48	7:0	Default : 0x20 Access : R/W
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.
24h (2F49h)	REG2F49	7:0	Default : 0x00 Access : R/W
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.
25h (2F4Ah)	REG2F4A	7:0	Default : 0x20 Access : R/W
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.
25h (2F4Bh)	REG2F4B	7:0	Default : 0x20 Access : R/W
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00 Access : R/W
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.
26h (2F4Dh)	REG2F4D	7:0	Default : 0x00 Access : R/W
	DUMMY26_13_15[2:0]	7:5	
	-	4:0	Reserved.
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00 Access : R/W
	DUMMY27_0_15[7:0]	7:0	
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00 Access : R/W
	DUMMY27_0_15[15:8]	7:0	See description of '2F4Eh'.
28h (2F50h)	REG2F50	7:0	Default : 0x00 Access : R/W
	DUMMY28_0_15[7:0]	7:0	
28h	REG2F51	7:0	Default : 0x00 Access : R/W

SCMI Register (Bank = 2F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
(2F51h)	DUMMY28_0_15[15:8]	7:0	See description of '2F50h'.
34h (2F68h)	REG2F68	7:0	Default : 0x00 Access : R/W
	DUMMY34_7_7	7	
	-	6:5	Reserved.
	IPM_CHK_SUM_EN	4	F2 check sum test enable.
	IPM_CHK_SUM_VCNT[3:0]	3:0	F2 check sum v count.
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00 Access : RO
	STATUS_READ_35_F2[7:0]	7:0	F2 status read out for debug.
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00 Access : RO
	STATUS_READ_35_F2[15:8]	7:0	See description of '2F6Ah'.
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00 Access : RO
	STATUS_READ_36_F2[7:0]	7:0	F2 status read out for debug.
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00 Access : RO
	STATUS_READ_36_F2[15:8]	7:0	See description of '2F6Ch'.
38h (2F70h)	REG2F70	7:0	Default : 0x00 Access : RO
	STATUS_READ_38_F2[7:0]	7:0	F2 status read out for debug.
38h (2F71h)	REG2F71	7:0	Default : 0x00 Access : RO
	STATUS_READ_38_F2[15:8]	7:0	See description of '2F70h'.
39h (2F72h)	REG2F72	7:0	Default : 0x00 Access : RO
	STATUS_READ_39_F2[7:0]	7:0	F2 status read out for debug.
39h (2F73h)	REG2F73	7:0	Default : 0x00 Access : RO
	STATUS_READ_39_F2[15:8]	7:0	See description of '2F72h'.
3Ah (2F74h)	REG2F74	7:0	Default : 0x00 Access : RO
	STATUS_READ_3A_F2[7:0]	7:0	F2 status read out for debug.
3Ah (2F75h)	REG2F75	7:0	Default : 0x00 Access : RO
	STATUS_READ_3A_F2[15:8]	7:0	See description of '2F74h'.
3Bh (2F76h)	REG2F76	7:0	Default : 0x00 Access : RO
	STATUS_READ_3B_F2[7:0]	7:0	F2 status read out for debug.
3Bh (2F77h)	REG2F77	7:0	Default : 0x00 Access : RO
	STATUS_READ_3B_F2[15:8]	7:0	See description of '2F76h'.
3Ch (2F78h)	REG2F78	7:0	Default : 0x00 Access : RO
	STATUS_READ_3C_F2[7:0]	7:0	F2 status read out for debug.
3Ch	REG2F79	7:0	Default : 0x00 Access : RO

SCMI Register (Bank = 2F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description
(2F79h)	STATUS_READ_3C_F2[15:8]	7:0	See description of '2F78h'.
3Dh (2F7Ah)	REG2F7A	7:0	Default : 0x00
	STATUS_READ_3D_F2[7:0]	7:0	F2 status read out for debug.
3Dh (2F7Bh)	REG2F7B	7:0	Default : 0x00
	STATUS_READ_3D_F2[15:8]	7:0	See description of '2F7Ah'.
3Eh (2F7Ch)	REG2F7C	7:0	Default : 0x00
	STATUS_READ_3E_F2[7:0]	7:0	F2 status read out for debug.
3Eh (2F7Dh)	REG2F7D	7:0	Default : 0x00
	STATUS_READ_3E_F2[15:8]	7:0	See description of '2F7Ch'.
40h (2F80h)	REG2F80	7:0	Default : 0x04
	DUMMY40_3_15[4:0]	7:3	
	UPDATE_MEM_CONFIG_EN	2	Update memory format enable.
	IP_REG_DBF_EN	1	Register latch with input V sync enable.
	OP_REG_DBF_EN	0	Register latch with output V sync enable.
40h (2F81h)	REG2F81	7:0	Default : 0x00
	DUMMY40_3_15[12:5]	7:0	See description of '2F80h'.

ACE Register (Bank = 2F, Sub-Bank = 18)

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
10h ~ 11h (2F20h ~ 2F23h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
13h ~ 22h (2F26h ~ 2F44h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
24h ~ 28h (2F48h ~ 2F51h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
30h (2F60h)	REG2F60	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:3	Reserved.	
	SUB_ICC_EN	2	Sub window ICC enable.	

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	Mnemonic	Bit	Description	
	-	1:0	Reserved.	
31h (2F62h)	REG2F62	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_R[3:0]	7:4	Sub window ICC saturation adjustment of R.	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (2F63h)	REG2F63	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_G[3:0]	7:4	Sub window ICC saturation adjustment of G.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (2F64h)	REG2F64	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_B[3:0]	7:4	Sub window ICC saturation adjustment of B.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	
32h (2F65h)	REG2F65	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_C[3:0]	7:4	Sub window ICC saturation adjustment of C.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	
33h (2F66h)	REG2F66	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_M[3:0]	7:4	Sub window ICC saturation adjustment of M.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h (2F67h)	REG2F67	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_Y[3:0]	7:4	Sub window ICC saturation adjustment of Y.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (2F68h)	REG2F68	7:0	Default : 0x00	Access : R/W
	SUB_SA_USER_F[3:0]	7:4	Sub window ICC saturation adjustment of F.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00	Access : R/W
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00	Access : R/W
	SUB_SIGN_SA_USER[7:0]	7:0	Sub window ICC decrease saturation.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold.	
37h	-	7:0	Default : -	Access : -

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description
(2F6Eh)	-	-	Reserved.
38h (2F70h)	-	7:0	Default : -
	-	-	Access : -
	-	-	Reserved.
39h ~ 3Bh (2F72h ~ 2F77h)	-	7:0	Default : -
	-	-	Access : -
	-	-	Reserved.
3Ch (2F78h)	REG2F78	7:0	Default : 0xFF
	WPL_WHITE_PEAK_LIMIT_THRD[7:0]	7:0	Access : R/W
			White peak limit threshold.
40h (2F80h)	REG2F80	7:0	Default : 0x00
	MAIN_IBC_EN	7	Access : R/W
			Main window IBC enable.
	SUB_IBC_EN	6	Sub window IBC enable.
	-	5:0	Reserved.
41h (2F82h)	REG2F82	7:0	Default : 0x20
	-	7:6	Access : R/W
	-		Reserved.
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.
41h (2F83h)	REG2F83	7:0	Default : 0x20
	-	7:6	Access : R/W
	-		Reserved.
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.
42h (2F84h)	REG2F84	7:0	Default : 0x20
	-	7:6	Access : R/W
	-		Reserved.
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.
42h (2F85h)	REG2F85	7:0	Default : 0x20
	-	7:6	Access : R/W
	-		Reserved.
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.
43h (2F86h)	REG2F86	7:0	Default : 0x20
	-	7:6	Access : R/W
	-		Reserved.
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.
43h (2F87h)	REG2F87	7:0	Default : 0x20
	-	7:6	Access : R/W
	-		Reserved.
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.
44h (2F88h)	REG2F88	7:0	Default : 0x20
	-	7:6	Access : R/W
	-		Reserved.
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	Mnemonic	Bit	Description	
45h (2F8Ah)	REG2F8A	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YR_ADJ[5:0]	5:0	Sub window IBC Y adjustment of R.	
45h (2F8Bh)	REG2F8B	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YG_ADJ[5:0]	5:0	Sub window IBC Y adjustment of G.	
46h (2F8Ch)	REG2F8C	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YB_ADJ[5:0]	5:0	Sub window IBC Y adjustment of B.	
46h (2F8Dh)	REG2F8D	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YC_ADJ[5:0]	5:0	Sub window IBC Y adjustment of C.	
47h (2F8Eh)	REG2F8E	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YM_ADJ[5:0]	5:0	Sub window IBC Y adjustment of M.	
47h (2F8Fh)	REG2F8F	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YY_ADJ[5:0]	5:0	Sub window IBC Y adjustment of Y.	
48h (2F90h)	REG2F90	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	SUB_YF_ADJ[5:0]	5:0	Sub window IBC Y adjustment of F.	
48h (2F91h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
50h (2FA0h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
50h (2FA1h)	REG2FA1	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	MAIN_WHITE_PEAK_LIMIT_EN	3	Main window white peak limit enable.	
	-	2:0	Reserved.	
51h ~ 58h (2FA2h ~ 2FB0h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
58h	REG2FB1	7:0	Default : 0x00	Access : R/W

ACE Register (Bank = 2F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description
(2FB1h)	-	7:4	Reserved.
	SUB_WHITE_PEAK_LIMIT_EN	3	Sub window white peak limit enable.
	-	2:0	Reserved.
59h ~ 5Fh (2FB2h ~ 2FBFh)	-	7:0	Default : - Access : -
	-	-	Reserved.
60h (2FC0h)	REG2FC0	7:0	Default : 0x00 Access : R/W
	MAIN_IHC_EN	7	Main window IHC enable.
	SUB_IHC_EN	6	Sub window IHC enable.
	-	5:0	Reserved.
60h (2FC1h)	-	7:0	Default : - Access : -
	-	-	Reserved.
61h (2FC2h)	REG2FC2	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.
61h (2FC3h)	REG2FC3	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.
62h (2FC4h)	REG2FC4	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.
62h (2FC5h)	REG2FC5	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.
63h (2FC6h)	REG2FC6	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.
63h (2FC7h)	REG2FC7	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.
64h (2FC8h)	REG2FC8	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	Mnemonic	Bit	Description	
65h (2FCAh)	REG2FCA	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_R[6:0]	6:0	Sub window IHC hue adjustment of R.	
65h (2FCBh)	REG2FCB	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_G[6:0]	6:0	Sub window IHC hue adjustment of G.	
66h (2FCCh)	REG2FCC	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_B[6:0]	6:0	Sub window IHC hue adjustment of B.	
66h (2FCDh)	REG2FCD	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_C[6:0]	6:0	Sub window IHC hue adjustment of C.	
67h (2FCEh)	REG2FCE	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_M[6:0]	6:0	Sub window IHC hue adjustment of M.	
67h (2FCFh)	REG2FCF	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_Y[6:0]	6:0	Sub window IHC hue adjustment of Y.	
68h (2FDOh)	REG2FDO	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_HUE_USER_F[6:0]	6:0	Sub window IHC hue adjustment of F.	
6Eh (2FDCh)	REG2FDC	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	SUB_R2Y_EN	4	Sub window RGB to YCbCr enable.	
	-	3:2	Reserved.	
	R2Y_DITHER_EN	1	RGB to YCbCr dither enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr enable.	
6Eh (2FDDh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
6Fh (2FDEh)	REG2FDE	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_R2Y_EQ_SEL[1:0]	5:4	Sub window RGB to YCbCr equation selection.	
	-	3:2	Reserved.	

ACE Register (Bank = 2F, Sub-Bank = 18)				
Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_R2Y_EQ_SEL[1:0]	1:0	Main window RGB to YCbCr equation selection.	
70h ~ 74h (2FE0h ~ 2FE9h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
74h ~ 74h (2FE8h ~ 2FE9h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
08h ~ 0Ah (2F10h ~ 2F15h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
10h (2F20h)	REG2F20	7:0	Default : 0x00	Access : R/W
	VPS_SRAM_ACT	7	2D peaking line-buffer sram active.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2:1	Reserved.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
10h (2F21h)	REG2F21	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	

PEAKING Register (Bank = 2F, Sub-Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.
11h (2F22h)	REG2F22	7:0	Default : 0x00 Access : R/W
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.
13h (2F26h)	REG2F26	7:0	Default : 0x00 Access : R/W
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.
13h (2F27h)	REG2F27	7:0	Default : 0x10 Access : R/W
	-	7:6	Reserved.
	MAIN_OSD_SHARPNESS_CTRL[5:0]	5:0	Main window user sharpness adjust.
14h (2F28h)	REG2F28	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	SUB_Y_LPF_COEF[2:0]	6:4	Sub window horizontal Y LPF coefficient.
	-	3:1	Reserved.
	SUB_POST_PEAKING_EN	0	Sub window 2D peaking enable.
14h (2F29h)	REG2F29	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SUB_BAND4_PEAKING_EN	3	Sub window band4 peaking enable.
	SUB_BAND3_PEAKING_EN	2	Sub window band3 peaking enable.
	SUB_BAND2_PEAKING_EN	1	Sub window band2 peaking enable.
	SUB_BAND1_PEAKING_EN	0	Sub window band1 peaking enable.
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00 Access : R/W
	SUB_BAND4_COEF_STEP[1:0]	7:6	Sub window band4 coefficient step.
	SUB_BAND3_COEF_STEP[1:0]	5:4	Sub window band3 coefficient step.
	SUB_BAND2_COEF_STEP[1:0]	3:2	Sub window band2 coefficient step.
	SUB_BAND1_COEF_STEP[1:0]	1:0	Sub window band1 coefficient step.
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00 Access : R/W
	SUB_CORING_THRD_2[3:0]	7:4	Sub window coring threshold 2.
	SUB_CORING_THRD_1[3:0]	3:0	Sub window coring threshold 1.
17h	REG2F2F	7:0	Default : 0x10 Access : R/W

PEAKING Register (Bank = 2F, Sub-Bank = 19)

Index (Absolute)	Mnemonic	Bit	Description
(2F2Fh)	-	7:6	Reserved.
	SUB_OSD_SHARPNESS_CTRL[5:0]	5:0	Sub window user sharpness adjust.
18h (2F30h)	REG2F30	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.
18h (2F31h)	REG2F31	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.
19h (2F32h)	REG2F32	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.
19h (2F33h)	REG2F33	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.
1Ch (2F38h)	-	7:0	Default : - Access : -
	-	-	Reserved.
20h ~ 21h (2F40h ~ 2F43h)	-	7:0	Default : - Access : -
	-	-	Reserved.
24h ~ 25h (2F48h ~ 2F4Bh)	-	7:0	Default : - Access : -
	-	-	Reserved.
28h (2F50h)	REG2F50	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	SUB_BAND1_COEF[5:0]	5:0	Sub window band1 coefficient.
28h (2F51h)	REG2F51	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	SUB_BAND2_COEF[5:0]	5:0	Sub window band2 coefficient.
29h (2F52h)	REG2F52	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	SUB_BAND3_COEF[5:0]	5:0	Sub window band3 coefficient.
29h (2F53h)	REG2F53	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.

PEAKING Register (Bank = 2F, Sub-Bank = 19)				
Index (Absolute)	Mnemonic	Bit	Description	
	SUB_BAND4_COEF[5:0]	5:0	Sub window band4 coefficient.	
2Ch (2F58h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
30h (2F60h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
30h (2F61h)	REG2F61	7:0	Default : 0x33	Access : R/W
	-	7:6	Reserved.	
	MAIN_CORING_THRD_STEP[1:0]	5:4	Main window coring step.	
	-	3:2	Reserved.	
	SUB_CORING_THRD_STEP[1:0]	1:0	Sub window coring step.	
31h ~ 32h (2F62h ~ 2F64h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
33h (2F66h)	REG2F66	7:0	Default : 0x00	Access : R/W
	MAIN_BAND2_CORING_THRD[3:0]	7:4	Main window band2 coring threshold.	
	MAIN_BAND1_CORING_THRD[3:0]	3:0	Main window band1 coring threshold.	
33h (2F67h)	REG2F67	7:0	Default : 0x00	Access : R/W
	MAIN_BAND4_CORING_THRD[3:0]	7:4	Main window band4 coring threshold.	
	MAIN_BAND3_CORING_THRD[3:0]	3:0	Main window band3 coring threshold.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0x00	Access : R/W
	SUB_BAND2_CORING_THRD[3:0]	7:4	Sub window band2 coring threshold.	
	SUB_BAND1_CORING_THRD[3:0]	3:0	Sub window band1 coring threshold.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00	Access : R/W
	SUB_BAND4_CORING_THRD[3:0]	7:4	Sub window band4 coring threshold.	
	SUB_BAND3_CORING_THRD[3:0]	3:0	Sub window band3 coring threshold.	
37h ~ 5Fh (2F6Eh ~ 2FBFh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
58h ~ 5Fh (2FB0h ~ 2FBFh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	

DLC Register (Bank = 2F, Sub-Bank = 1A)

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h ~ 01h (2F02h ~ 2F03h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
03h ~ 08h (2F06h ~ 2F10h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
09h ~ 0Ah (2F12h ~ 2F15h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Bh (2F16h)	REG2F16	7:0	Default : 0x00	Access : RO
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximum pixel.	
0Bh (2F17h)	REG2F17	7:0	Default : 0x00	Access : RO
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Ch	REG2F18	7:0	Default : 0x00	Access : RO

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
(2F18h)	SUB_MAX_PIXEL[7:0]	7:0	Sub window maximum pixel.
0Ch (2F19h)	REG2F19	7:0	Default : 0x00
	SUB_MIN_PIXEL[7:0]	7:0	Sub window minimum pixel.
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00
	-	7:2	Reserved.
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00
	-	7:2	Reserved.
	SUB_BRI_ADJUST_LSB[1:0]	1:0	Sub window Y adjust low bit.
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x00
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust.
0Fh (2F1Fh)	REG2F1F	7:0	Default : 0x00
	SUB_BRI_ADJUST[7:0]	7:0	Sub window Y adjust.
10h (2F20h)	REG2F20	7:0	Default : 0x00
	-	7	Reserved.
	MAIN_BLACK_START[6:0]	6:0	Main window black start.
10h (2F21h)	REG2F21	7:0	Default : 0x80
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.
11h (2F22h)	REG2F22	7:0	Default : 0x00
	-	7	Reserved.
	MAIN_WHITE_START[6:0]	6:0	Main window white start.
11h (2F23h)	REG2F23	7:0	Default : 0x80
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.
12h (2F24h)	REG2F24	7:0	Default : 0x00
	-	7	Reserved.
	SUB_BLACK_START[6:0]	6:0	Sub window black start.
12h (2F25h)	REG2F25	7:0	Default : 0x80
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.
13h (2F26h)	REG2F26	7:0	Default : 0x00
	-	7	Reserved.
	SUB_WHITE_START[6:0]	6:0	Sub window white start.
13h (2F27h)	REG2F27	7:0	Default : 0x80
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
14h (2F28h)	REG2F28	7:0	Default : 0x40 Access : R/W
	MAIN_Y_GAIN[7:0]	7:0	Main window Y gain.
14h (2F29h)	REG2F29	7:0	Default : 0x40 Access : R/W
	MAIN_C_GAIN[7:0]	7:0	Main window C gain.
15h (2F2Ah)	REG2F2A	7:0	Default : 0x40 Access : R/W
	SUB_Y_GAIN[7:0]	7:0	Sub window Y gain.
15h (2F2Bh)	REG2F2B	7:0	Default : 0x40 Access : R/W
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.
16h ~ 18h (2F2Ch ~ 2F31h)	-	7:0	Default : - Access : -
	-	-	Reserved.
1Ah ~ 1Bh (2F34h ~ 2F37h)	-	7:0	Default : - Access : -
	-	-	Reserved.
1Ch (2F38h)	REG2F38	7:0	Default : 0x20 Access : R/W
	HISTOGRAM_RANGE1[7:0]	7:0	Variable 8 section of histogram range 1.
1Ch (2F39h)	REG2F39	7:0	Default : 0x40 Access : R/W
	HISTOGRAM_RANGE2[7:0]	7:0	Variable 8 section of histogram range 2.
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x60 Access : R/W
	HISTOGRAM_RANGE3[7:0]	7:0	Variable 8 section of histogram range 3.
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x80 Access : R/W
	HISTOGRAM_RANGE4[7:0]	7:0	Variable 8 section of histogram range 4.
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0xA0 Access : R/W
	HISTOGRAM_RANGE5[7:0]	7:0	Variable 8 section of histogram range 5.
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0xC0 Access : R/W
	HISTOGRAM_RANGE6[7:0]	7:0	Variable 8 section of histogram range 6.
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0xE0 Access : R/W
	HISTOGRAM_RANGE7[7:0]	7:0	Variable 8 section of histogram range 7.
20h ~ 27h (2F40h ~ 2F4Fh)	-	7:0	Default : - Access : -
	-	-	Reserved.
28h (2F50h)	REG2F50	7:0	Default : 0x00 Access : RO
	TOTAL_1F_00[7:0]	7:0	Histogram report section1.
28h	REG2F51	7:0	Default : 0x00 Access : RO

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F51h)	TOTAL_1F_00[15:8]	7:0	See description of '2F50h'.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : RO
	TOTAL_3F_20[7:0]	7:0	Histogram report section2.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : RO
	TOTAL_3F_20[15:8]	7:0	See description of '2F52h'.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : RO
	TOTAL_5F_40[7:0]	7:0	Histogram report section3.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : RO
	TOTAL_5F_40[15:8]	7:0	See description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : RO
	TOTAL_7F_60[7:0]	7:0	Histogram report section4.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : RO
	TOTAL_7F_60[15:8]	7:0	See description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : RO
	TOTAL_9F_80[7:0]	7:0	Histogram report section5.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : RO
	TOTAL_9F_80[15:8]	7:0	See description of '2F58h'.	
2Dh (2F5Ah)	REG2F5A	7:0	Default : 0x00	Access : RO
	TOTAL_BF_A0[7:0]	7:0	Histogram report section6.	
2Dh (2F5Bh)	REG2F5B	7:0	Default : 0x00	Access : RO
	TOTAL_BF_A0[15:8]	7:0	See description of '2F5Ah'.	
2Eh (2F5Ch)	REG2F5C	7:0	Default : 0x00	Access : RO
	TOTAL_DF_C0[7:0]	7:0	Histogram report section7.	
2Eh (2F5Dh)	REG2F5D	7:0	Default : 0x00	Access : RO
	TOTAL_DF_C0[15:8]	7:0	See description of '2F5Ch'.	
2Fh (2F5Eh)	REG2F5E	7:0	Default : 0x00	Access : RO
	TOTAL_FF_E0[7:0]	7:0	Histogram report section8.	
2Fh (2F5Fh)	REG2F5F	7:0	Default : 0x00	Access : RO
	TOTAL_FF_E0[15:8]	7:0	See description of '2F5Eh'.	
30h (2F60h)	REG2F60	7:0	Default : 0x08	Access : R/W
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (2F61h)	REG2F61	7:0	Default : 0x18	Access : R/W
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
31h (2F62h)	REG2F62	7:0	Default : 0x28	Access : R/W
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (2F63h)	REG2F63	7:0	Default : 0x38	Access : R/W
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (2F64h)	REG2F64	7:0	Default : 0x48	Access : R/W
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (2F65h)	REG2F65	7:0	Default : 0x58	Access : R/W
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h (2F66h)	REG2F66	7:0	Default : 0x68	Access : R/W
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (2F67h)	REG2F67	7:0	Default : 0x78	Access : R/W
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (2F68h)	REG2F68	7:0	Default : 0x88	Access : R/W
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (2F69h)	REG2F69	7:0	Default : 0x98	Access : R/W
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (2F6Ah)	REG2F6A	7:0	Default : 0xA8	Access : R/W
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h (2F6Bh)	REG2F6B	7:0	Default : 0x00	Access : R/W
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (2F6Ch)	REG2F6C	7:0	Default : 0xC8	Access : R/W
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (2F6Dh)	REG2F6D	7:0	Default : 0xD8	Access : R/W
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (2F6Eh)	REG2F6E	7:0	Default : 0xE8	Access : R/W
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (2F6Fh)	REG2F6F	7:0	Default : 0xF8	Access : R/W
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
38h (2F70h)	REG2F70	7:0	Default : 0x08	Access : R/W
	SUB_CURVE_FIT_TABLE_0[7:0]	7:0	Sub window curve table 0.	
38h (2F71h)	REG2F71	7:0	Default : 0x18	Access : R/W
	SUB_CURVE_FIT_TABLE_1[7:0]	7:0	Sub window curve table 1.	
39h	REG2F72	7:0	Default : 0x28	Access : R/W

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
(2F72h)	SUB_CURVE_FIT_TABLE_2[7:0]	7:0	Sub window curve table 2.
39h (2F73h)	REG2F73 SUB_CURVE_FIT_TABLE_3[7:0]	7:0	Default : 0x38 Sub window curve table 3.
3Ah (2F74h)	REG2F74 SUB_CURVE_FIT_TABLE_4[7:0]	7:0	Default : 0x48 Sub window curve table 4.
3Ah (2F75h)	REG2F75 SUB_CURVE_FIT_TABLE_5[7:0]	7:0	Default : 0x58 Sub window curve table 5.
3Bh (2F76h)	REG2F76 SUB_CURVE_FIT_TABLE_6[7:0]	7:0	Default : 0x68 Sub window curve table 6.
3Bh (2F77h)	REG2F77 SUB_CURVE_FIT_TABLE_7[7:0]	7:0	Default : 0x78 Sub window curve table 7.
3Ch (2F78h)	REG2F78 SUB_CURVE_FIT_TABLE_8[7:0]	7:0	Default : 0x88 Sub window curve table 8.
3Ch (2F79h)	REG2F79 SUB_CURVE_FIT_TABLE_9[7:0]	7:0	Default : 0x98 Sub window curve table 9.
3Dh (2F7Ah)	REG2F7A SUB_CURVE_FIT_TABLE_10[7:0]	7:0	Default : 0xA8 Sub window curve table 10.
3Dh (2F7Bh)	REG2F7B SUB_CURVE_FIT_TABLE_11[7:0]	7:0	Default : 0x00 Sub window curve table 11.
3Eh (2F7Ch)	REG2F7C SUB_CURVE_FIT_TABLE_12[7:0]	7:0	Default : 0xC8 Sub window curve table 12.
3Eh (2F7Dh)	REG2F7D SUB_CURVE_FIT_TABLE_13[7:0]	7:0	Default : 0xD8 Sub window curve table 13.
3Fh (2F7Eh)	REG2F7E SUB_CURVE_FIT_TABLE_14[7:0]	7:0	Default : 0xE8 Sub window curve table 14.
3Fh (2F7Fh)	REG2F7F SUB_CURVE_FIT_TABLE_15[7:0]	7:0	Default : 0xF8 Sub window curve table 15.
40h (2F80h)	REG2F80 TOTAL_32_0[7:0]	7:0	Default : 0x00 Histogram report section 32_0.
40h (2F81h)	REG2F81 TOTAL_32_0[15:8]	7:0	Default : 0x00 See description of '2F80h'.
41h (2F82h)	REG2F82 TOTAL_32_1[7:0]	7:0	Default : 0x00 Histogram report section 32_1.

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
41h (2F83h)	REG2F83	7:0	Default : 0x00 Access : RO
	TOTAL_32_1[15:8]	7:0	See description of '2F82h'.
42h (2F84h)	REG2F84	7:0	Default : 0x00 Access : RO
	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.
42h (2F85h)	REG2F85	7:0	Default : 0x00 Access : RO
	TOTAL_32_2[15:8]	7:0	See description of '2F84h'.
43h (2F86h)	REG2F86	7:0	Default : 0x00 Access : RO
	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.
43h (2F87h)	REG2F87	7:0	Default : 0x00 Access : RO
	TOTAL_32_3[15:8]	7:0	See description of '2F86h'.
44h (2F88h)	REG2F88	7:0	Default : 0x00 Access : RO
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.
44h (2F89h)	REG2F89	7:0	Default : 0x00 Access : RO
	TOTAL_32_4[15:8]	7:0	See description of '2F88h'.
45h (2F8Ah)	REG2F8A	7:0	Default : 0x00 Access : RO
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.
45h (2F8Bh)	REG2F8B	7:0	Default : 0x00 Access : RO
	TOTAL_32_5[15:8]	7:0	See description of '2F8Ah'.
46h (2F8Ch)	REG2F8C	7:0	Default : 0x00 Access : RO
	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.
46h (2F8Dh)	REG2F8D	7:0	Default : 0x00 Access : RO
	TOTAL_32_6[15:8]	7:0	See description of '2F8Ch'.
47h (2F8Eh)	REG2F8E	7:0	Default : 0x00 Access : RO
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.
47h (2F8Fh)	REG2F8F	7:0	Default : 0x00 Access : RO
	TOTAL_32_7[15:8]	7:0	See description of '2F8Eh'.
48h (2F90h)	REG2F90	7:0	Default : 0x00 Access : RO
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.
48h (2F91h)	REG2F91	7:0	Default : 0x00 Access : RO
	TOTAL_32_8[15:8]	7:0	See description of '2F90h'.
49h (2F92h)	REG2F92	7:0	Default : 0x00 Access : RO
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.
49h	REG2F93	7:0	Default : 0x00 Access : RO

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
(2F93h)	TOTAL_32_9[15:8]	7:0	See description of '2F92h'.
4Ah (2F94h)	REG2F94	7:0	Default : 0x00
	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.
4Ah (2F95h)	REG2F95	7:0	Default : 0x00
	TOTAL_32_10[15:8]	7:0	See description of '2F94h'.
4Bh (2F96h)	REG2F96	7:0	Default : 0x00
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.
4Bh (2F97h)	REG2F97	7:0	Default : 0x00
	TOTAL_32_11[15:8]	7:0	See description of '2F96h'.
4Ch (2F98h)	REG2F98	7:0	Default : 0x00
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.
4Ch (2F99h)	REG2F99	7:0	Default : 0x00
	TOTAL_32_12[15:8]	7:0	See description of '2F98h'.
4Dh (2F9Ah)	REG2F9A	7:0	Default : 0x00
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.
4Dh (2F9Bh)	REG2F9B	7:0	Default : 0x00
	TOTAL_32_13[15:8]	7:0	See description of '2F9Ah'.
4Eh (2F9Ch)	REG2F9C	7:0	Default : 0x00
	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.
4Eh (2F9Dh)	REG2F9D	7:0	Default : 0x00
	TOTAL_32_14[15:8]	7:0	See description of '2F9Ch'.
4Fh (2F9Eh)	REG2F9E	7:0	Default : 0x00
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.
4Fh (2F9Fh)	REG2F9F	7:0	Default : 0x00
	TOTAL_32_15[15:8]	7:0	See description of '2F9Eh'.
50h (2FA0h)	REG2FA0	7:0	Default : 0x00
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.
50h (2FA1h)	REG2FA1	7:0	Default : 0x00
	TOTAL_32_16[15:8]	7:0	See description of '2FA0h'.
51h (2FA2h)	REG2FA2	7:0	Default : 0x00
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.
51h (2FA3h)	REG2FA3	7:0	Default : 0x00
	TOTAL_32_17[15:8]	7:0	See description of '2FA2h'.

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
52h (2FA4h)	REG2FA4	7:0	Default : 0x00 Access : RO
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.
52h (2FA5h)	REG2FA5	7:0	Default : 0x00 Access : RO
	TOTAL_32_18[15:8]	7:0	See description of '2FA4h'.
53h (2FA6h)	REG2FA6	7:0	Default : 0x00 Access : RO
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.
53h (2FA7h)	REG2FA7	7:0	Default : 0x00 Access : RO
	TOTAL_32_19[15:8]	7:0	See description of '2FA6h'.
54h (2FA8h)	REG2FA8	7:0	Default : 0x00 Access : RO
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.
54h (2FA9h)	REG2FA9	7:0	Default : 0x00 Access : RO
	TOTAL_32_20[15:8]	7:0	See description of '2FA8h'.
55h (2FAAh)	REG2FAA	7:0	Default : 0x00 Access : RO
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.
55h (2FABh)	REG2FAB	7:0	Default : 0x00 Access : RO
	TOTAL_32_21[15:8]	7:0	See description of '2FAAh'.
56h (2FACH)	REG2FAC	7:0	Default : 0x00 Access : RO
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.
56h (2FADh)	REG2FAD	7:0	Default : 0x00 Access : RO
	TOTAL_32_22[15:8]	7:0	See description of '2FACH'.
57h (2FAEh)	REG2FAE	7:0	Default : 0x00 Access : RO
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.
57h (2FAFh)	REG2FAF	7:0	Default : 0x00 Access : RO
	TOTAL_32_23[15:8]	7:0	See description of '2FAEh'.
58h (2FB0h)	REG2FB0	7:0	Default : 0x00 Access : RO
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.
58h (2FB1h)	REG2FB1	7:0	Default : 0x00 Access : RO
	TOTAL_32_24[15:8]	7:0	See description of '2FB0h'.
59h (2FB2h)	REG2FB2	7:0	Default : 0x00 Access : RO
	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.
59h (2FB3h)	REG2FB3	7:0	Default : 0x00 Access : RO
	TOTAL_32_25[15:8]	7:0	See description of '2FB2h'.
5Ah	REG2FB4	7:0	Default : 0x00 Access : RO

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
(2FB4h)	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.
5Ah (2FB5h)	REG2FB5 TOTAL_32_26[15:8]	7:0 7:0	Default : 0x00 Access : RO See description of '2FB4h'.
5Bh (2FB6h)	REG2FB6 TOTAL_32_27[7:0]	7:0 7:0	Default : 0x00 Access : RO Histogram report section 32_27.
5Bh (2FB7h)	REG2FB7 TOTAL_32_27[15:8]	7:0 7:0	Default : 0x00 Access : RO See description of '2FB6h'.
5Ch (2FB8h)	REG2FB8 TOTAL_32_28[7:0]	7:0 7:0	Default : 0x00 Access : RO Histogram report section 32_28.
5Ch (2FB9h)	REG2FB9 TOTAL_32_28[15:8]	7:0 7:0	Default : 0x00 Access : RO See description of '2FB8h'.
5Dh (2FBAh)	REG2FBA TOTAL_32_29[7:0]	7:0 7:0	Default : 0x00 Access : RO Histogram report section 32_29.
5Dh (2FBBh)	REG2FBB TOTAL_32_29[15:8]	7:0 7:0	Default : 0x00 Access : RO See description of '2FBAh'.
5Eh (2FBCh)	REG2FBC TOTAL_32_30[7:0]	7:0 7:0	Default : 0x00 Access : RO Histogram report section 32_30.
5Eh (2FBDh)	REG2FBD TOTAL_32_30[15:8]	7:0 7:0	Default : 0x00 Access : RO See description of '2FBCh'.
5Fh (2FBEh)	REG2FBE TOTAL_32_31[7:0]	7:0 7:0	Default : 0x00 Access : RO Histogram report section 32_31.
5Fh (2FBFh)	REG2FBF TOTAL_32_31[15:8]	7:0 7:0	Default : 0x00 Access : RO See description of '2FBEh'.
60h ~ 60h (2FC0h ~ 2FC1h)	- -	7:0 -	Default : - Access : - Reserved.
61h (2FC2h)	REG2FC2 MAIN_MAX_PIXEL_SAT[7:0]	7:0 7:0	Default : 0x00 Access : RO Main window minimum pixel saturation.
61h (2FC3h)	REG2FC3 MAIN_MIN_PIXEL_SAT[7:0]	7:0 7:0	Default : 0x00 Access : RO Main window maximum pixel saturation.
62h (2FC4h)	REG2FC4 SUB_MAX_PIXEL_SAT[7:0]	7:0 7:0	Default : 0x00 Access : RO Sub window minimum pixel saturation.
62h	REG2FC5	7:0	Default : 0x00 Access : RO

DLC Register (Bank = 2F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description
(2FC5h)	SUB_MIN_PIXEL_SAT[7:0]	7:0	Sub window maximum pixel saturation.
63h ~ 63h (2FC6h ~ 2FC7h)	-	7:0	Default : - Access : -
	-	-	Reserved.
68h (2FD0h)	-	7:0	Default : - Access : -
	-	-	Reserved.
69h ~ 6Dh (2FD2h ~ 2FDBh)	-	7:0	Default : - Access : -
	-	-	Reserved.
6Fh (2FDEh)	-	7:0	Default : - Access : -
	-	-	Reserved.
70h ~ 75h (2FE0h ~ 2FEBh)	-	7:0	Default : - Access : -
	-	-	Reserved.
76h (2FECh)	REG2FEC	7:0	Default : 0x08 Access : R/W
	MAIN_CURVE_FIT_TABLE_N0[7:0]	7:0	Main window curve table left point.
76h (2FEDh)	REG2FED	7:0	Default : 0x01 Access : R/W
	-	7:1	Reserved.
	MAIN_CURVE_FIT_TABLE_N0[8]	0	See description of '2FECh'.
77h (2FEEh)	REG2FEE	7:0	Default : 0x08 Access : R/W
	MAIN_CURVE_FIT_TABLE_16[7:0]	7:0	Main window curve table 16.
77h (2FEFh)	REG2FEF	7:0	Default : 0x01 Access : R/W
	-	7:1	Reserved.
	MAIN_CURVE_FIT_TABLE_16[8]	0	See description of '2FEEh'.
78h ~ 7Dh (2FF0h ~ 2FFBh)	-	7:0	Default : - Access : -
	-	-	Reserved.
7Eh (2FFCh)	REG2FFC	7:0	Default : 0x08 Access : R/W
	SUB_CURVE_FIT_TABLE_N0[7:0]	7:0	Sub window curve table left point.
7Eh (2FFDh)	REG2FFD	7:0	Default : 0x01 Access : R/W
	-	7:1	Reserved.
	SUB_CURVE_FIT_TABLE_N0[8]	0	See description of '2FFCh'.
7Fh (2FFEh)	REG2FFE	7:0	Default : 0x08 Access : R/W
	SUB_CURVE_FIT_TABLE_16[7:0]	7:0	Sub window curve table 16.

DLC Register (Bank = 2F, Sub-Bank = 1A)				
Index (Absolute)	Mnemonic	Bit	Description	
7Fh (2FFFh)	REG2FFF	7:0	Default : 0x01	Access : R/W
	-	7:1	Reserved.	
	SUB_CURVE_FIT_TABLE_16[8]	0	See description of '2FFEh'.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
10h (2F20h)	REG2F20	7:0	Default : 0x01	Access : R/W
	PIP_DISABLE	7	Disable PIP Function.	
	-	6:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	SW_SUB_EN	1	Enable sub window shown on the scree.	
	MAIN_EN	0	Enable main window shown on the scree.	
10h (2F21h)	REG2F21	7:0	Default : 0x20	Access : R/W
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	
	FBL_MASK_OVERLAP	5	Do not write overlapped portion of FBL channel to line buffer.	
	FBL_SEL	4	Select FBL source. b0: Source F2 is FBL.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
			b1: Source F1 is FBL.	
	VBLANK_SUB	3	Fill the sub windows line buffer in vertical blanking.	
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.	
	F2_IS_SUB	1	Set main window display on the foreground.	
	MAIN_IS_TOP	0	Set second channel display in sub-window.	
11h (2F22h)	REG2F22	7:0	Default : 0x70	Access : R/W
	-	7	Reserved.	
	EXTRA_POS[2:0]	6:4	Enable extra request at specified region. [0] Enable at bottom B session. [1] Enable at bottom A session. [2] Enable at top session.	
	EXTRA_TH_LN[3:0]	3:0	Enable extra request for overlapping when the jumping line less than this threshold.	
11h (2F23h)	REG2F23	7:0	Default : 0x07	Access : R/W
	EXTRA_EN	7	Enable extra request engine.	
	VBLANK_OVL	6	Doing the extra request in vertical blanking.	
	EXTRA_Y_HALF	5	Reduce the extra_y to half.	
	-	4:3	Reserved.	
	BO_LENGTH[2:0]	2:0	Select the length of extra request. h0: 16 pixel. h1: 32 pixel. h2: 64 pixel. h3: 128 pixel. h4: (overlap length) / 8. h5: (overlap length) / 4. h6: (overlap length) / 2. h7: (overlap length).	
12h (2F24h)	REG2F24	7:0	Default : 0x00	Access : R/W
	SCLB_BASE_F2[7:0]	7:0	The starting address of f2 stored at line buffer.	
12h (2F25h)	REG2F25	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SCLB_BASE_F2[11:8]	3:0	See description of '2F24h'.	
13h (2F26h)	REG2F26	7:0	Default : 0x00	Access : R/W
	SCLB_BASE_F1[7:0]	7:0	The starting address of f1 stored at line buffer.	
13h	REG2F27	7:0	Default : 0x04	Access : R/W

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description
(2F27h)	-	7:4	Reserved.
	SCLB_BASE_F1[11:8]	3:0	See description of '2F26h'.
14h (2F28h)	REG2F28	7:0	Default : 0x08
	HEXT_BA_RIGHT[7:0]	7:0	Extend the pixel of bottom A session at the right side.
14h (2F29h)	REG2F29	7:0	Default : 0x08
	HEXT_BB_LEFT[7:0]	7:0	Extend the pixel of bottom B session at the left side.
15h (2F2Ah)	REG2F2A	7:0	Default : 0xFF
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.
15h (2F2Bh)	REG2F2B	7:0	Default : 0x0F
	-	7:4	Reserved.
	VLEN_F2[11:8]	3:0	See description of '2F2Ah'.
16h (2F2Ch)	REG2F2C	7:0	Default : 0xFF
	VLEN_F1[7:0]	7:0	Set the maximum request lines for first channel.
16h (2F2Dh)	REG2F2D	7:0	Default : 0x0F
	-	7:4	Reserved.
	VLEN_F1[11:8]	3:0	See description of '2F2Ch'.
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00
	EXT_SUB_BORDER[3:0]	7:4	Extend the specified line in sub window to insert additional border.
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional border.
17h (2F2Fh)	REG2F2F	7:0	Default : 0x02
	EXTRA_ADV_LINE[3:0]	7:4	Advance the specified lines of extra end line (2's complement).
	EXTRA_FETCH_LINE[3:0]	3:0	How many line will be fetched by extra request. Minimum is 1.
18h (2F30h)	REG2F30	7:0	Default : 0x00
	-	7:1	Reserved.
	ATP_EN	0	Manual tune parameter.
19h (2F32h)	REG2F32	7:0	Default : 0x38
	-	7	Reserved.
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter. 0: Vsync of SC_TOP. 1: Delay one line of vfde.

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SEL_DISP[1:0]	5:4	Select the trig point to start op1 engine. h0: Down_eq7. h1: Down_eq8. h2: Down_eq9. h3: Delay lines set by reg_disp_trig_dly.	
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. h0: Falling edge of vsync. h1: Nearly raising edge of vsync. h2: Delay line set by reg_atp_trig_dly. h3: Manual trig by set reg_atp_en.	
	SEL_SYNC[1:0]	1:0	Select the trig point for sync to initial engine. h0: Falling edge of vfde. h1: Raising edge of vsync. h2: Reserved. h3: Reserved.	
19h (2F33h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
1Ah (2F34h)	REG2F34	7:0	Default : 0x03	Access : R/W
	ATP_TRIG_DLY[7:0]	7:0	Generate train_trig_p from delayed line of vsync.	
1Ah (2F35h)	REG2F35	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	ATP_TRIG_DLY[11:8]	3:0	See description of '2F34h'.	
1Bh (2F36h)	REG2F36	7:0	Default : 0x05	Access : R/W
	DISP_TRIG_DLY[7:0]	7:0	Generate disp_trig_p from delayed line of vsync.	
1Bh (2F37h)	REG2F37	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '2F36h'.	
1Ch (2F38h)	REG2F38	7:0	Default : 0x00	Access : R/W
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (2F39h)	REG2F39	7:0	Default : 0x00	Access : R/W
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (2F3Ah)	REG2F3A	7:0	Default : 0x00	Access : R/W
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Dh (2F3Bh)	REG2F3B	7:0	Default : 0x00	Access : R/W
	HOVERSCAN_F1[7:0]	7:0	Offset line buffer position of F1 in right direction.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description
1Eh (2F3Ch)	REG2F3C	7:0	Default : 0x10 Access : R/W
	MIN_OVERLAP_TH[7:0]	7:0	Threshold of overlapped length. Extra_eq will be disabled when overlapped length less then this threshold.
1Eh (2F3Dh)	REG2F3D	7:0	Default : 0x00 Access : R/W
	MIN_OVERLAP_CNT[7:0]	7:0	Stop count between two extra request.
1Fh (2F3Eh)	REG2F3E	7:0	Default : 0xC2 Access : R/W
	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. h0: 2 pixel. h1: 4 pixel. h2: 8 pixel. h3: 16 pixel.
	DISP_START_MODE	5	Select the display line buffer start mode. 0: Start at advance 1 display line. 1: Start at faling edge of vsync_init.
	DISP_LB_MODE	4	Select the trig mode. 0: Line base. 1: Fill line buffer.
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. h0: Before 8 pixel. h1: Before 16 pixel. h2: Before 32 pixel. h3: Before 64 pixel.
	DISP_RLN_MODE[1:0]	1:0	Select the under_run value of display level. h0: Update by hsync (not optimum performance). h1: Update when session done(may error). h2: Update when line done(reg_disp_trig_mode = 1'b0). h3: Reserved.
1Fh (2F3Fh)	REG2F3F	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	DISP_UNDER_MODE	3	Select the under_run value of display level. 0: 16'h0000. 1: 16'hffff.
	DISP_PAT_EN	2	Enable internal pattern of op1_disp.
	DISP_LB_WEZ	1	Disable wen of display line buffer.
	DISP_TRIG_MODE	0	Select the trig mode. 0: Triggered by self_counter.

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description
			1: Triggered by op2.
20h (2F40h)	REG2F40	7:0	Default : 0xFF Access : R/W
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.
20h (2F41h)	REG2F41	7:0	Default : 0x07 Access : R/W
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '2F40h'.
30h (2F60h)	REG2F60	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	FLAG_BB_ADR_INI	2	Status of cnt_bb_adr_ini, write 1 to switch back to hardware. h0: Calculated by hardware. h1: Written by software.
	FLAG_BO_END_LN	1	Status of line_base_bot, write 1 to switch back to hardware. h0: Calculated by hardware. h1: Written by software.
	-	0	Reserved.
31h (2F62h)	REG2F62	7:0	Default : 0x00 Access : R/W
	SW_BO_END_LN[7:0]	7:0	Software mode to set the line_base_bot for extra request.
31h (2F63h)	REG2F63	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SW_BO_END_LN[11:8]	3:0	See description of '2F62h'.
32h (2F64h)	REG2F64	7:0	Default : 0x00 Access : R/W
	SW_BB_ADR_INI[7:0]	7:0	Software mode to set the cnt_bb_adr_ini.
32h (2F65h)	REG2F65	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SW_BB_ADR_INI[11:8]	3:0	See description of '2F64h'.
40h (2F80h)	REG2F80	7:0	Default : 0x00 Access : RO
	-	7:1	Reserved.
	DISPLAY_UNDERRUN	0	Indicate that the display line buffer is underrun in previous frame.
41h (2F82h)	REG2F82	7:0	Default : 0x00 Access : RO
	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line cnt of first display position.
41h (2F83h)	REG2F83	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '2F82h'.

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description
42h (2F84h)	REG2F84	7:0	Default : 0x00 Access : RO
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line cnt of minimum display level occure.
42h (2F85h)	REG2F85	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	MIN_DISP_LINE[11:8]	3:0	See description of '2F84h'.
43h (2F86h)	REG2F86	7:0	Default : 0x00 Access : RO
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.
43h (2F87h)	REG2F87	7:0	Default : 0x00 Access : RO
	MIN_DISP_CNT[15:8]	7:0	See description of '2F86h'.
44h (2F88h)	REG2F88	7:0	Default : 0x00 Access : RO
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.
44h (2F89h)	REG2F89	7:0	Default : 0x00 Access : RO
	MAX_DISP_CNT[15:8]	7:0	See description of '2F88h'.
50h (2FA0h)	REG2FA0	7:0	Default : 0x00 Access : RO
	SCLB_TF_ADR_INI[7:0]	7:0	Read SCLB_TF_ADR_INI.
50h (2FA1h)	REG2FA1	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	SCLB_TF_ADR_INI[11:8]	3:0	See description of '2FA0h'.
51h (2FA2h)	REG2FA2	7:0	Default : 0x00 Access : RO
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.
51h (2FA3h)	REG2FA3	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '2FA2h'.
52h (2FA4h)	REG2FA4	7:0	Default : 0x00 Access : RO
	SCLB_BB_ADR_INI[7:0]	7:0	Read SCLB_BB_ADR_INI.
52h (2FA5h)	REG2FA5	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	SCLB_BB_ADR_INI[11:8]	3:0	See description of '2FA4h'.
53h (2FA6h)	REG2FA6	7:0	Default : 0x00 Access : RO
	SCLB_BO_ADR_INI[7:0]	7:0	Read SCLB_BO_ADR_INI.
53h (2FA7h)	REG2FA7	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description
	SCLB_BO_ADR_INI[11:8]	3:0	See description of '2FA6h'.
54h (2FA8h)	REG2FA8	7:0	Default : 0x00
	SCLB_TF_LEN[7:0]	7:0	Read SCLB_TF_LEN.
54h (2FA9h)	REG2FA9	7:0	Default : 0x00
	-	7:4	Reserved.
	SCLB_TF_LEN[11:8]	3:0	See description of '2FA8h'.
55h (2FAAh)	REG2FAA	7:0	Default : 0x00
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.
55h (2FABh)	REG2FAB	7:0	Default : 0x00
	-	7:4	Reserved.
	SCLB_BF_LEN[11:8]	3:0	See description of '2FAAh'.
56h (2FACH)	REG2FAC	7:0	Default : 0x00
	SCLB_BA_LEN[7:0]	7:0	Read SCLB_BA_LEN.
56h (2FADh)	REG2FAD	7:0	Default : 0x00
	-	7:4	Reserved.
	SCLB_BA_LEN[11:8]	3:0	See description of '2FACH'.
57h (2FAEh)	REG2FAE	7:0	Default : 0x00
	SCLB_BB_LEN[7:0]	7:0	Read SCLB_BB_LEN.
57h (2FAFh)	REG2FAF	7:0	Default : 0x00
	-	7:4	Reserved.
	SCLB_BB_LEN[11:8]	3:0	See description of '2FAEh'.
58h (2FB0h)	REG2FB0	7:0	Default : 0x00
	FETCH_NUM_F1A[7:0]	7:0	Read FETCH_NUM_F1A.
58h (2FB1h)	REG2FB1	7:0	Default : 0x00
	-	7:4	Reserved.
	FETCH_NUM_F1A[11:8]	3:0	See description of '2FB0h'.
59h (2FB2h)	REG2FB2	7:0	Default : 0x00
	FETCH_NUM_F1B[7:0]	7:0	Read FETCH_NUM_F1B.
59h (2FB3h)	REG2FB3	7:0	Default : 0x00
	-	7:4	Reserved.
	FETCH_NUM_F1B[11:8]	3:0	See description of '2FB2h'.
5Ah (2FB4h)	REG2FB4	7:0	Default : 0x00
	FETCH_NUM_F2A[7:0]	7:0	Read FETCH_NUM_F2A.

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)				
Index (Absolute)	Mnemonic	Bit	Description	
5Ah (2FB5h)	REG2FB5	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	FETCH_NUM_F2A[11:8]	3:0	See description of '2FB4h'.	
5Bh (2FB6h)	REG2FB6	7:0	Default : 0x00	Access : RO
	FETCH_NUM_F2B[7:0]	7:0	Read FETCH_NUM_F2B.	
5Bh (2FB7h)	REG2FB7	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	FETCH_NUM_F2B[11:8]	3:0	See description of '2FB6h'.	
5Ch (2FB8h)	REG2FB8	7:0	Default : 0x00	Access : RO
	FETCH_OFFSET_B[7:0]	7:0	Read FETCH_OFFSET_B.	
5Ch (2FB9h)	REG2FB9	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	FETCH_OFFSET_B[11:8]	3:0	See description of '2FB8h'.	
5Dh (2FBAh)	REG2FBA	7:0	Default : 0x00	Access : RO
	BO_LENGTH_RD[7:0]	7:0	Read bo_length.	
5Dh (2FBBh)	REG2FBB	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	BO_LENGTH_RD[11:8]	3:0	See description of '2FBAh'.	
5Eh (2FBCh)	REG2FBC	7:0	Default : 0x00	Access : RO
	BO_START_LN[7:0]	7:0	Read BO_START_LN.	
5Eh (2FBDh)	REG2FBD	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	BO_START_LN[11:8]	3:0	See description of '2FBCh'.	
5Fh (2FBEh)	REG2FBE	7:0	Default : 0x00	Access : RO
	BO_END_LN[7:0]	7:0	Read BO_END_LN.	
5Fh (2FBFh)	REG2FBF	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	BO_END_LN[11:8]	3:0	See description of '2FBEh'.	
60h (2FC0h)	REG2FC0	7:0	Default : 0x00	Access : RO
	DISP_TF_ADR_INI[7:0]	7:0	Read DISP_TF_ADR_INI.	
60h (2FC1h)	REG2FC1	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	DISP_TF_ADR_INI[11:8]	3:0	See description of '2FC0h'.	

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)				
Index (Absolute)	Mnemonic	Bit	Description	
61h (2FC2h)	REG2FC2	7:0	Default : 0x00	Access : RO
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (2FC3h)	REG2FC3	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '2FC2h'.	
62h (2FC4h)	REG2FC4	7:0	Default : 0x00	Access : RO
	DISP_BB_ADR_INI[7:0]	7:0	Read DISP_BB_ADR_INI.	
62h (2FC5h)	REG2FC5	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	DISP_BB_ADR_INI[11:8]	3:0	See description of '2FC4h'.	
63h (2FC6h)	REG2FC6	7:0	Default : 0x00	Access : RO
	DISP_TF_LEN[7:0]	7:0	Read DISP_TF_LEN.	
63h (2FC7h)	REG2FC7	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	DISP_TF_LEN[11:8]	3:0	See description of '2FC6h'.	
64h (2FC8h)	REG2FC8	7:0	Default : 0x00	Access : RO
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h (2FC9h)	REG2FC9	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '2FC8h'.	
65h (2FCAh)	REG2FCA	7:0	Default : 0x00	Access : RO
	DISP_BA_LEN[7:0]	7:0	Read DISP_BA_LEN.	
65h (2FCBh)	REG2FCB	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	DISP_BA_LEN[11:8]	3:0	See description of '2FCAh'.	
66h (2FCCh)	REG2FCC	7:0	Default : 0x00	Access : RO
	DISP_BB_LEN[7:0]	7:0	Read DISP_BB_LEN.	
66h (2FCDh)	REG2FCD	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	DISP_BB_LEN[11:8]	3:0	See description of '2FCCh'.	
67h (2FCEh)	REG2FCE	7:0	Default : 0x00	Access : RO
	HSPR_BB_ADR_INI[7:0]	7:0	Read HSPR_BB_ADR_INI.	
67h	REG2FCF	7:0	Default : 0x00	Access : RO

OP1_TOP Register (Bank = 2F, Sub-Bank = 20)			
Index (Absolute)	Mnemonic	Bit	Description
(2FCFh)	-	7:4	Reserved.
	HSPR_BB_ADR_INI[11:8]	3:0	See description of '2FCEh'.

ELA Register (Bank = 2F, Sub-Bank = 21)

ELA Register (Bank = 2F, Sub-Bank = 21)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h ~ 02h (2F02h ~ 2F04h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Ch ~ 0Fh (2F18h ~ 2F1Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
10h (2F20h)	REG2F20	7:0	Default : 0x02	Access : R/W
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. 1: Enable. 0: Disable.	
11h ~ 12h (2F22h ~ 2F24h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
13h	-	7:0	Default : -	Access : -

ELA Register (Bank = 2F, Sub-Bank = 21)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F26h)	-	-	Reserved.	
14h	-	7:0	Default : -	Access : -
(2F28h)	-	-	Reserved.	
15h ~ 17h	-	7:0	Default : -	Access : -
(2F2Ah ~ 2F2Eh)	-	-	Reserved.	
30h ~ 31h	-	7:0	Default : -	Access : -
(2F60h ~ 2F63h)	-	-	Reserved.	
70h ~ 71h	-	7:0	Default : -	Access : -
(2FE0h ~ 2FE2h)	-	-	Reserved.	
72h ~ 72h	-	7:0	Default : -	Access : -
(2FE4h ~ 2FE5h)	-	-	Reserved.	
7Fh ~ 7Fh	-	7:0	Default : -	
(2FFEh ~ 2FFFh)	-	-	Reserved.	

TDDI Register (Bank = 2F, Sub-Bank = 22)

TDDI Register (Bank = 2F, Sub-Bank = 22)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h (2F02h)	REG2F02	7:0	Default : 0x04	Access : R/W
	RATIO_DIV_YCSEP_F2	7	Main window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F2[2:0]	2:0	Main window ratio divide mode when Y/C separate.	
01h (2F03h)	REG2F03	7:0	Default : 0x14	Access : R/W
	-	7:6	Reserved.	
	RATIO_DIV_MD_F2[2:0]	5:3	Main window ratio divide mode.	
	RATIO_MD_F2[2:0]	2:0	Main window ratio filter mode.	
02h (2F04h)	REG2F04	7:0	Default : 0x80	Access : R/W
	RATIO_C_INDEP_F2	7	Main window C ratio independent mode. 0: Disable C ratio filter. 1: Enable C ratio filter.	
	RATIO_C_LOWBOUND_F2	6	Main window C ratio lower bound enable.	

TDDI Register (Bank = 2F, Sub-Bank = 22)

Index (Absolute)	Mnemonic	Bit	Description
02h (2F05h)	RSV_02_2_F2[1:0]	5:4	Reserved.
	RATIO_C_MIN_F2[3:0]	3:0	Main window C minimum ratio in independent mode.
	REG2F05	7:0	Default : 0x02 Access : R/W
	RSV_02_0_F2[2:0]	7:5	Reserved.
	-	4	Reserved.
	RSV_02_1_F2[1:0]	3:2	Reserved.
	RATIO_C_YMAX_SEL_F2	1	Main window C ratio takes Y ratio mode. 0: Select Y ratio before SST. 1: Select Y ratio after SST.
08h (2F10h)	RATIO_C_YMAX_DIS_F2	0	Main window C ratio takes Y ratio mode disable. 0: Enable. 1: Disable.
	REG2F10	7:0	Default : 0x00 Access : R/W
	PRE_MOT_FILTER_EN_F2	7	Main Window LPF enable of DNR motion calculation.
	-	6	Reserved.
08h (2F11h)	PRE_MOT_OFFSET_F2[5:0]	5:0	Main Window pre-memory motion offset for motion calculation.
	REG2F11	7:0	Default : 0x08 Access : R/W
	-	7:4	Reserved.
09h (2F12h)	PRE_MOT_GAIN_F2[3:0]	3:0	Main Window pre-memory motion gain for motion calculation.
	REG2F12	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
09h (2F13h)	POST_MOT_OFFSET_F2[5:0]	5:0	Main Window post-memory motion offset for motion calculation.
	REG2F13	7:0	Default : 0x88 Access : R/W
	POST_MOT_CGAIN_F2[3:0]	7:4	Main Window post-memory motion gain for Y motion calculation.
0Ah (2F14h)	POST_MOT_YGAIN_F2[3:0]	3:0	Main Window post-memory motion gain for C motion calculation.
	REG2F14	7:0	Default : 0x86 Access : R/W
	POST_MOT_YMAX_EN_F2	7	Main Window pre-/post-memory Y motion maximum enable.
	-	6:3	Reserved.
	HIS_WT_F2[2:0]	2:0	Main Window history weighting.

TDDI Register (Bank = 2F, Sub-Bank =22)

Index (Absolute)	Mnemonic	Bit	Description
0Ah (2F15h)	REG2F15	7:0	Default : 0x04 Access : R/W
	HIS_FILTER_MODE_F2	7	Main Window history filter mode.
	-	6:4	Reserved.
	HIS_RATIO_OFFSET_F2[3:0]	3:0	Main Window history ratio offset.
0Ch (2F18h)	REG2F18	7:0	Default : 0x07 Access : R/W
	RSV_STAT_0_F2[1:0]	7:6	Reserved.
	STAT_INC_MODE_F2	5	Main window ratio statistics: ratio incremental mode.
	STAT_SEL_C_F2	4	Main window ratio statistics: ratio selection.
	STAT_CORE_F2[3:0]	3:0	Main window ratio statistics: coring threshold.
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00 Access : RO
	MOTION_STATUS_F2[7:0]	7:0	Main window ratio statistics: motion status.
0Dh (2F1Bh)	REG2F1B	7:0	Default : 0x00 Access : RO
	MOTION_STATUS_F2[15:8]	7:0	See description of '2F1Ah'.
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00 Access : RO
	MOTION_STATUS_F2[23:16]	7:0	See description of '2F1Ah'.
10h (2F20h)	REG2F20	7:0	Default : 0x4A Access : R/W
	ADAPT_MED_EN_F2	7	Main window adaptive DFK enable.
	WEGT_MED_EN_F2	6	Main window weighted DFK enable.
	RSV_MED_0_F2	5	Reserved.
	MED_MANUAL_EN_F2	4	Main window DFK manual mode enable.
	MED_MANUAL_WEIGHT_F2[3:0]	3:0	Main window DFK manual weighting.
11h (2F22h)	REG2F22	7:0	Default : 0x08 Access : R/W
	-	7:5	Reserved.
	MED_LF_BEGIN_F2[4:0]	4:0	Main window weighted DFK low-frequency begin.
11h (2F23h)	REG2F23	7:0	Default : 0x04 Access : R/W
	-	7:4	Reserved.
	MED_LF_SLOPE_F2[3:0]	3:0	Main window weighted DFK low-frequency slope adjustment.
12h (2F24h)	REG2F24	7:0	Default : 0x14 Access : R/W
	-	7:5	Reserved.
	MED_HF_BEGIN_F2[4:0]	4:0	Main window weighted DFK high-frequency begin.
12h (2F25h)	REG2F25	7:0	Default : 0x04 Access : R/W
	-	7:4	Reserved.

TDDI Register (Bank = 2F, Sub-Bank =22)

Index (Absolute)	Mnemonic	Bit	Description
	MED_HF_SLOPE_F2[3:0]	3:0	Main window weighted DFK high-frequency slope adjustment.
13h (2F26h)	REG2F26	7:0	Default : 0x30 Access : R/W
	-	7:6	Reserved.
	MED_MOT_TH_F2[5:0]	5:0	Main window adaptive DFK motion threshold.
14h ~ 15h (2F28h ~ 2F2Ah)	-	7:0	Default : - Access : -
	-	-	Reserved.
18h (2F30h)	REG2F30	7:0	Default : 0x13 Access : R/W
	SST_EN_F2	7	Main window SST enable.
	FILM_SST_EN_F2	6	Main window enable SST in film mode.
	RSV_SST_0_F2	5	Reserved.
	SST_MOTION_LPF_EN_F2	4	Main window SST low-pass on motion enable.
	SST_MOTION_TH_F2[3:0]	3:0	Main window SST motion threshold.
18h (2F31h)	REG2F31	7:0	Default : 0x27 Access : R/W
	RSV_SST_1_F2[1:0]	7:6	Reserved.
	SST_ERODE_MODE_F2[1:0]	5:4	Main window SST motion area erosion mode.
	RSV_SST_2_F2	3	Reserved.
	SST_DILATE_MODE_F2[2:0]	2:0	Main window SST motion area dilation mode.
19h (2F32h)	REG2F32	7:0	Default : 0xDF Access : R/W
	SST_POSTLPF_EN_F2	7	Main window SST post-LPF enable.
	SST_POSTLPF_MAX_F2	6	Main window SST post-LPF maximum function enable.
	SST_DYNAMIC_CORE_TH_F2[5:0]	5:0	Main window SST dynamic motion coring threshold.
19h (2F33h)	REG2F33	7:0	Default : 0x85 Access : R/W
	SST_DYNAMIC_SGAIN_F2[3:0]	7:4	Main window SST dynamic motion spatial difference gain.
	SST_DYNAMIC_TGAIN_F2[3:0]	3:0	Main window SST dynamic motion temporal difference gain.
1Ah (2F34h)	REG2F34	7:0	Default : 0x00 Access : R/W
	RSV_SST_3_F2[1:0]	7:6	Reserved.
	SST_STATIC_CORE_TH_F2[5:0]	5:0	Main window SST static motion coring threshold.
1Ah (2F35h)	REG2F35	7:0	Default : 0x22 Access : R/W
	SST_STATIC_SGAIN_F2[3:0]	7:4	Main window SST static motion spatial difference gain.
	SST_STATIC_TGAIN_F2[3:0]	3:0	Main window SST static motion temporal difference gain.

TDDI Register (Bank = 2F, Sub-Bank =22)

Index (Absolute)	Mnemonic	Bit	Description
1Bh (2F36h)	REG2F36	7:0	Default : 0x00 Access : R/W
	RSV_SST_4_F2[7:0]	7:0	Reserved.
78h ~ 7Fh (2FF0h ~ 2FFFh)	-	7:0	Default : -
	-	-	Reserved.

HVSP Register (Bank = 2F, Sub-Bank = 23)

HVSP Register (Bank = 2F, Sub-Bank = 23)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (2F03h)	REG2F03	7:0	Default : 0x00	Access : R/W
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '2F02h'.	
02h (2F04h)	REG2F04	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '2F02h'.	
03h (2F06h)	REG2F06	7:0	Default : 0x00	Access : R/W
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h (2F07h)	REG2F07	7:0	Default : 0x00	Access : R/W
	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '2F06h'.	
04h (2F08h)	REG2F08	7:0	Default : 0x00	Access : R/W
	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '2F06h'.	

HVSP Register (Bank = 2F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description
05h (2F0Ah)	REG2F0A	7:0	Default : 0x00
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.
05h (2F0Bh)	REG2F0B	7:0	Default : 0x00
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '2F0Ah'.
06h (2F0Ch)	REG2F0C	7:0	Default : 0x00
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '2F0Ah'.
07h (2F0Eh)	REG2F0E	7:0	Default : 0x00
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.
07h (2F0Fh)	REG2F0F	7:0	Default : 0x00
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '2F0Eh'.
08h (2F10h)	REG2F10	7:0	Default : 0x00
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '2F0Eh'.
08h (2F11h)	REG2F11	7:0	Default : 0x00
	-	7:1	Reserved.
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.
09h (2F12h)	REG2F12	7:0	Default : 0x00
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.
09h (2F13h)	REG2F13	7:0	Default : 0x00
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '2F12h'.
0Ah (2F14h)	REG2F14	7:0	Default : 0x00
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '2F12h'.
0Ah (2F15h)	REG2F15	7:0	Default : 0x80
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.
	-	6:1	Reserved.
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.
0Bh (2F16h)	REG2F16	7:0	Default : 0x00
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: Y SRAM 0. 1: Y SRAM 1.
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: Y SRAM 0. 1: Y SRAM 1.

HVSP Register (Bank = 2F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: C SRAM 0. 3: C SRAM 1.
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.
0Bh (2F17h)	REG2F17	7:0	Default : 0x00 Access : R/W
	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: Y SRAM 0. 1: Y SRAM 1.
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: Y SRAM 0. 1: Y SRAM 1.
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: C SRAM 0. 3: C SRAM 1.
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.
0Ch (2F18h)	REG2F18	7:0	Default : 0xC0 Access : R/W
	FORMAT_422_F2	7	Main window data format is 422.
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.
	CR_LOAD_INI_F2	5	Main Cr_load initial value.
	-	4:2	Reserved.
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.
0Ch (2F19h)	REG2F19	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.

HVSP Register (Bank = 2F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.
0Dh (2F1Ah)	REG2F1A	7:0	Default : 0x00 Access : R/W
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.
0Dh (2F1Bh)	REG2F1B	7:0	Default : 0x00 Access : R/W
	HSP_CORING_TH_Y_F2[7:0]	7:0	Main window horizontal Y coring threshold.
0Eh (2F1Ch)	REG2F1C	7:0	Default : 0x00 Access : R/W
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.
0Eh (2F1Dh)	REG2F1D	7:0	Default : 0x00 Access : R/W
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.
0Fh (2F1Eh)	REG2F1E	7:0	Default : 0x38 Access : R/W
	HSP_DE_RING_G_ON_F2	7	Main window horizontal Y de-ringing enable.
	HSP_DE_RING_TH1_F2[2:0]	6:4	Main window horizontal de-ringing threshold1.
	HSP_DE_RING_TH0_F2[3:0]	3:0	Main window horizontal de-ringing threshold0.
0Fh (2F1Fh)	REG2F1F	7:0	Default : 0x58 Access : R/W
	HSP_DE_RING_RB_ON_F2	7	Main window horizontal C de-ringing enable.
	HSP_DE_RING_TH3_F2[2:0]	6:4	Main window horizontal de-ringing threshold3.
	HSP_DE_RING_TH2_F2[3:0]	3:0	Main window horizontal de-ringing threshold2.
10h (2F20h)	REG2F20	7:0	Default : 0x00 Access : R/W
	HSP_OFFSET_F2[7:0]	7:0	Main window horizontal de-ringing offset.
10h (2F21h)	REG2F21	7:0	Default : 0x00 Access : R/W
	HSP_OFFSET2_F2[7:0]	7:0	Main window horizontal de-ringing offset2.
11h (2F22h)	REG2F22	7:0	Default : 0x38 Access : R/W
	VSP_DE_RING_G_ON_F2	7	Main window vertical Y de-ringing enable.
	VSP_DE_RING_TH1_F2[2:0]	6:4	Main window vertical de-ringing threshold1.
	VSP_DE_RING_TH0_F2[3:0]	3:0	Main window vertical de-ringing threshold0.
11h (2F23h)	REG2F23	7:0	Default : 0x58 Access : R/W
	VSP_DE_RING_RB_ON_F2	7	Main window vertical C de-ringing enable.
	VSP_DE_RING_TH3_F2[2:0]	6:4	Main window vertical de-ringing threshold3.
	VSP_DE_RING_TH2_F2[3:0]	3:0	Main window vertical de-ringing threshold2.
12h	REG2F24	7:0	Default : 0x00 Access : R/W

HVSP Register (Bank = 2F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description
(2F24h)	VSP_OFFSET_F2[7:0]	7:0	Main window vertical de-ringing offset.
12h (2F25h)	REG2F25	7:0	Default : 0x00
	VSP_OFFSET2_F2[7:0]	7:0	Main window vertical de-ringing offset2.
13h (2F26h)	REG2F26	7:0	Default : 0x00
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.
	-	5:4	Reserved.
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.
	FIELD_POL_F2	1	Main window field polarity switch.
	2_INIFAC_MD_F2	0	Main window two initial factors mode.
13h (2F27h)	REG2F27	7:0	Default : 0x00
	VSP_3TAP_EN_F2	7	Main window vertical 3tap scaling enable.
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width2 LSB.
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width1 LSB.
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width0 LSB.
	-	3	Reserved.
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width2 LSB.
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width1 LSB.
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width0 LSB.
14h (2F28h)	REG2F28	7:0	Default : 0x00
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width0.
14h (2F29h)	REG2F29	7:0	Default : 0x00
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width1.
15h (2F2Ah)	REG2F2A	7:0	Default : 0x00
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width2.
15h (2F2Bh)	REG2F2B	7:0	Default : 0x00
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.
16h (2F2Ch)	REG2F2C	7:0	Default : 0x00
	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.
16h	REG2F2D	7:0	Default : 0x00

HVSP Register (Bank = 2F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description
(2F2Dh)	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.
17h (2F2Eh)	REG2F2E	7:0	Default : 0x00
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width0.
17h (2F2Fh)	REG2F2F	7:0	Default : 0x00
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width1.
18h (2F30h)	REG2F30	7:0	Default : 0x00
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width2.
18h (2F31h)	REG2F31	7:0	Default : 0x00
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.
19h (2F32h)	REG2F32	7:0	Default : 0x00
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.
19h (2F33h)	REG2F33	7:0	Default : 0x00
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.
41h (2F82h)	REG2F82	7:0	Default : 0x00
	-	7:2	Reserved.
	CRAM_RW_EN	1	C SRAM read/write enable.
	YRAM_RW_EN	0	Y SRAM read/write enable.
41h (2F83h)	REG2F83	7:0	Default : 0x00
	-	7:1	Reserved.
	RAM_W_PULSE	0	SRAM write data pulse.
42h (2F84h)	REG2F84	7:0	Default : 0x00
	RAM_ADDR[7:0]	7:0	SRAM read/write address. (Only support max address to 0x7f).
43h (2F86h)	REG2F86	7:0	Default : 0x00
	RAM_WDATA[7:0]	7:0	SRAM write data.
43h (2F87h)	REG2F87	7:0	Default : 0x00
	RAM_WDATA[15:8]	7:0	See description of '2F86h'.
44h (2F88h)	REG2F88	7:0	Default : 0x00
	RAM_WDATA[23:16]	7:0	See description of '2F86h'.
44h (2F89h)	REG2F89	7:0	Default : 0x00
	RAM_WDATA[31:24]	7:0	See description of '2F86h'.
45h (2F8Ah)	REG2F8A	7:0	Default : 0x00
	RAM_WDATA[39:32]	7:0	See description of '2F86h'.

HVSP Register (Bank = 2F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description
46h (2F8Ch)	REG2F8C	7:0	Default : 0x00 Access : RO
	RAM_RDATA[7:0]	7:0	SRAM read data.
46h (2F8Dh)	REG2F8D	7:0	Default : 0x00 Access : RO
	RAM_RDATA[15:8]	7:0	See description of '2F8Ch'.
47h (2F8Eh)	REG2F8E	7:0	Default : 0x00 Access : RO
	RAM_RDATA[23:16]	7:0	See description of '2F8Ch'.
47h (2F8Fh)	REG2F8F	7:0	Default : 0x00 Access : RO
	RAM_RDATA[31:24]	7:0	See description of '2F8Ch'.
48h (2F90h)	REG2F90	7:0	Default : 0x00 Access : RO
	RAM_RDATA[39:32]	7:0	See description of '2F8Ch'.
51h (2FA2h)	REG2FA2	7:0	Default : 0x41 Access : R/W
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.
	FACTOR_MANUAL	6	Vertical factor manual mode.
	VDOWN_SEL	5	Vertical scaling down selection. 0: Bottom. 1: Top.
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.
	-	3	Reserved.
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.
52h (2FA5h)	REG2FA5	7:0	Default : 0x00 Access : R/W
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish. 1: DE end.
	-	6:0	Reserved.
53h (2FA7h)	-	7:0	Default : - Access : -
	-	-	Reserved.
58h ~ 5Fh (2FB0h ~ 2FBFh)	-	7:0	Default : - Access : -
	-	-	Reserved.
60h (2FC0h)	REG2FC0	7:0	Default : 0x40 Access : R/W
	CTI_AUTO_NO_MED_F2	7	Main window CTI auto no median.
	CTI_STEP_F2[2:0]	6:4	Main window CTI step.

HVSP Register (Bank = 2F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description
	-	3	Reserved.
	CTI_LPF_COEF_F2[2:0]	2:0	Main window CTI LPF coefficients.
60h (2FC1h)	REG2FC1	7:0	Default : 0x3F Access : R/W
	-	7:6	Reserved.
	CTI_BAND_COEF_F2[5:0]	5:0	Main window CTI BPF coefficients.
61h (2FC2h)	REG2FC2	7:0	Default : 0x88 Access : R/W
	CTI_MEDIAN_EN_F2	7	Main window CTI Median enable.
	-	6:4	Reserved.
	CTI_CORING_THRD_F2[3:0]	3:0	Main window CTI coring threshold.
61h (2FC3h)	REG2FC3	7:0	Default : 0x00 Access : R/W
	CTI_EN_F2	7	Main window CTI enable.
	-	6:0	Reserved.
62h (2FC4h)	REG2FC4	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	LEVEL_SLOPE_F2[2:0]	2:0	Main window CTI gray patch level slope.
62h (2FC5h)	REG2FC5	7:0	Default : 0x00 Access : R/W
	LEVEL_OFFSET_F2[7:0]	7:0	Main window CTI gray patch level offset.
67h (2FCEh)	REG2FCE	7:0	Default : 0x02 Access : R/W
	-	7:2	Reserved.
	GAIN_ADJ_EN_F2	1	Main window CTI gain adjust enable.
	-	0	Reserved.

FRC Register (Bank = 2F, Sub-Bank = 24)

FRC Register (Bank = 2F, Sub-Bank = 24)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
3Fh (2F7Eh)	REG2F7E	7:0	Default : 0x13	Access : R/W
	-	7:5	Reserved.	
	TAILCUT	4	TAILCUT enable.	
	NOISE_DITH_DISABLE	3	PAFRC mixed with noise dither disable. 0: Disable. 1: Enable.	
	DITH_BITS	2	Dithering bits. 0: 2-bits. 1: 4-bits.	
	TCON_OFF_EN	1	TCON FRC_GAMMA function off signal enable. 0: Ignore TCON gamma/dither turn off signal. 1: Gamma/dither function turn off by TCON FRC_GAMMA_OFF signal.	
	FRC_ON	0	PAFRC enable.	

FRC Register (Bank = 2F, Sub-Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
40h (2F80h)	REG2F80	7:0	Default : 0x00 Access : R/W
	BOX_ROTATE_EN	7	Box A/B/C/D relation rotation enable.
	TOP_BOX_UNIT_FLAG[1:0]	6:5	Top box A/B/C/D swap flag. 00: Per 2x2 box. 01: Per 4x4 box. 1x: Per 8x8 box.
	TOP_BOX_FREEZE	4	Top box freeze.
	TOP_BOX_SHRINK	3	Top box shrink to 2x2 from 4x4.
	FR_C2_BIT	2	Top box frame rotation step bit location for codexx10. 0: Bit[0]. 1: Bit[1].
	C2X2_ROT_B_DIR_S	1	C 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise, 2nd.
	D2X2_ROT_B_DIR_S	0	D 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise, 2nd.
40h (2F81h)	REG2F81	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	G_V_SWAP	6	Green channel vertical swap, avoid polarity not consistent.
	G_H_SWAP	5	Green channel horizontal swap, avoid polarity not consistent.
	B_D_SWAP	4	Blue channel diagonal swap.
	BOX_FR_SW	3	FRAME_CNT bit [1:0] swap for box rotate.
	BOX4X4_FR_SW	2	FRAME_CNT bit [1:0] swap for box4x4 rotate.
	BOX8X8_ROT_UNIT	1	0: Rotate step under per A, B, C or D. 1: Rotate step between A/B/C/D.
41h (2F82h)	REG2F82	7:0	Default : 0x00 Access : R/W
	C2X2_ROT_G_DIR	7	C 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	D2X2_ROT_G_DIR	6	D 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	C2X2_ROT_G_DIR_S	5	C 2x2 block rotation direction.

FRC Register (Bank = 2F, Sub-Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
			0: Clockwise. 1: Anti-Clockwise, 2nd.
	D2X2_ROT_G_DIR_S	4	D 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise, 2nd.
	A2X2_ROT_B_DIR	3	A 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	B2X2_ROT_B_DIR	2	B 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	C2X2_ROT_B_DIR	1	C 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	D2X2_ROT_B_DIR	0	D 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
41h (2F83h)	REG2F83	7:0	Default : 0x00 Access : R/W
	A2X2_ROT_R_DIR	7	A 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	B2X2_ROT_R_DIR	6	B 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	C2X2_ROT_R_DIR	5	C 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	D2X2_ROT_R_DIR	4	D 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.
	C2X2_ROT_R_DIR_S	3	C 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise, 2nd.
	D2X2_ROT_R_DIR_S	2	D 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise, 2nd.
	A2X2_ROT_G_DIR	1	A 2x2 block rotation direction.

FRC Register (Bank = 2F, Sub-Bank = 24)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: Clockwise. 1: Anti-Clockwise.	
	B2X2_ROT_G_DIR	0	B 2x2 block rotation direction. 0: Clockwise. 1: Anti-Clockwise.	
42h (2F84h)	REG2F84	7:0	Default : 0x00	Access : R/W
	TOP_BOX_FR_SEQ2[7:0]	7:0	Top box frame 2nd 4 frame rotation step.	
42h (2F85h)	REG2F85	7:0	Default : 0x00	Access : R/W
	TOP_BOX_FR_SEQ1[7:0]	7:0	Top box frame 1st 4 frame rotation step.	
43h (2F86h)	REG2F86	7:0	Default : 0x00	Access : R/W
	TOP_BOX_FR_SEQ4[7:0]	7:0	Top box frame 4th 4 frame rotation step.	
43h (2F87h)	REG2F87	7:0	Default : 0x00	Access : R/W
	TOP_BOX_FR_SEQ3[7:0]	7:0	Top box frame 3rd 4 frame rotation step.	
44h (2F88h)	REG2F88	7:0	Default : 0x00	Access : R/W
	TOP_BOX_FR_C2_SEQ34[7:0]	7:0	Top box frame 3rd/4th 4 frame rotation step for codexx10.	
44h (2F89h)	REG2F89	7:0	Default : 0x00	Access : R/W
	TOP_BOX_FR_C2_SEQ12[7:0]	7:0	Top box frame 1st/2nd 4 frame rotation step for codexx10.	
45h (2F8Ah)	REG2F8A	7:0	Default : 0x00	Access : R/W
	BOX_A_ROT_DIR	7	Location A frame counter direction. 0: Clockwise. 1: Back.	
	BOX_B_ROT_DIR	6	Location B frame counter direction. 0: Clockwise. 1: Back.	
	BOX_C_ROT_DIR	5	Location C frame counter direction. 0: Clockwise. 1: Back.	
	BOX_D_ROT_DIR	4	Location D frame counter direction. 0: Clockwise. 1: Back.	
	-	3:0	Reserved.	
45h (2F8Bh)	REG2F8B	7:0	Default : 0x00	Access : R/W
	BOX8X8_ROT_00[1:0]	7:6	Box8x8 entity 00 rotation step by reference.	
	BOX8X8_ROT_01[1:0]	5:4	Box8x8 entity 01 rotation step by reference.	
	BOX8X8_ROT_11[1:0]	3:2	Box8x8 entity 11 rotation step by reference.	

FRC Register (Bank = 2F, Sub-Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
	BOX8X8_ROT_10[1:0]	1:0	Box8x8 entity 10 rotation step by reference.
46h (2F8Ch)	REG2F8C	7:0	Default : 0x00 Access : R/W
	B_LU_00[1:0]	7:6	B 2x2 block left up entity.
	B_RU_01[1:0]	5:4	B 2x2 block right up entity.
	B_RD_11[1:0]	3:2	B 2x2 block right down entity.
	B_LD_10[1:0]	1:0	B 2x2 block left down entity.
46h (2F8Dh)	REG2F8D	7:0	Default : 0x00 Access : R/W
	A_LU_00[1:0]	7:6	A 2x2 block left up entity.
	A_RU_01[1:0]	5:4	A 2x2 block right up entity.
	A_RD_11[1:0]	3:2	A 2x2 block right down entity.
	A_LD_10[1:0]	1:0	A 2x2 block left down entity.
47h (2F8Eh)	REG2F8E	7:0	Default : 0x00 Access : R/W
	D_LU_00[1:0]	7:6	D 2x2 block left up entity.
	D_RU_01[1:0]	5:4	D 2x2 block right up entity.
	D_RD_11[1:0]	3:2	D 2x2 block right down entity.
	D_LD_10[1:0]	1:0	D 2x2 block left down entity.
47h (2F8Fh)	REG2F8F	7:0	Default : 0x00 Access : R/W
	C_LU_00[1:0]	7:6	C 2x2 block left up entity.
	C_RU_01[1:0]	5:4	C 2x2 block right up entity.
	C_RD_11[1:0]	3:2	C 2x2 block right down entity.
	C_LD_10[1:0]	1:0	C 2x2 block left down entity.
48h (2F90h)	REG2F90	7:0	Default : 0x00 Access : R/W
	D_LU_00_S[1:0]	7:6	D 2x2 block left up entity, 2nd.
	D_RU_01_S[1:0]	5:4	D 2x2 block right up entity, 2nd.
	D_RD_11_S[1:0]	3:2	D 2x2 block right down entity, 2nd.
	D_LD_10_S[1:0]	1:0	D 2x2 block left down entity, 2nd.
48h (2F91h)	REG2F91	7:0	Default : 0x00 Access : R/W
	C_LU_00_S[1:0]	7:6	C 2x2 block left up entity, 2nd.
	C_RU_01_S[1:0]	5:4	C 2x2 block right up entity, 2nd.
	C_RD_11_S[1:0]	3:2	C 2x2 block right down entity, 2nd.
	C_LD_10_S[1:0]	1:0	C 2x2 block left down entity, 2nd.
49h (2F92h)	REG2F92	7:0	Default : 0x00 Access : R/W
	BOX_B_LU_00[1:0]	7:6	Location B block A LSB 2 bits plus value.

FRC Register (Bank = 2F, Sub-Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description
	BOX_B_RU_01[1:0]	5:4	Location B block B LSB 2 bits plus value.
	BOX_B_RD_11[1:0]	3:2	Location B block C LSB 2 bits plus value.
	BOX_B_LD_10[1:0]	1:0	Location B block D LSB 2 bits plus value.
49h (2F93h)	REG2F93	7:0	Default : 0x00 Access : R/W
	BOX_A_LU_00[1:0]	7:6	Location A block A LSB 2 bits plus value.
	BOX_A_RU_01[1:0]	5:4	Location A block B LSB 2 bits plus value.
	BOX_A_RD_11[1:0]	3:2	Location A block C LSB 2 bits plus value.
	BOX_A_LD_10[1:0]	1:0	Location A block D LSB 2 bits plus value.
4Ah (2F94h)	REG2F94	7:0	Default : 0x00 Access : R/W
	BOX_D_LU_00[1:0]	7:6	Location D block A LSB 2 bits plus value.
	BOX_D_RU_01[1:0]	5:4	Location D block B LSB 2 bits plus value.
	BOX_D_RD_11[1:0]	3:2	Location D block C LSB 2 bits plus value.
	BOX_D_LD_10[1:0]	1:0	Location D block D LSB 2 bits plus value.
4Ah (2F95h)	REG2F95	7:0	Default : 0x00 Access : R/W
	BOX_C_LU_00[1:0]	7:6	Location C block A LSB 2 bits plus value.
	BOX_C_RU_01[1:0]	5:4	Location C block B LSB 2 bits plus value.
	BOX_C_RD_11[1:0]	3:2	Location C block C LSB 2 bits plus value.
	BOX_C_LD_10[1:0]	1:0	Location C block D LSB 2 bits plus value.

XV_YCC Register (Bank = 2F, Sub-Bank = 25)

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
01h (2F02h)	REG2F02	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	-	3:0	Reserved.	
01h ~ 10h (2F03h ~ 2F21h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
11h (2F22h)	REG2F22	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	

XV_YCC Register (Bank = 2F, Sub-Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description
	POST_SUB_BRI_EN	4	Sub window post brightness enable.
	-	3:0	Reserved.
11h ~ 20h (2F23h ~ 2F41h)	-	7:0	Default : - Access : -
	-	-	Reserved.
21h (2F42h)	REG2F42	7:0	Default : 0x00 Access : R/W
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post r channel offset.
21h (2F43h)	REG2F43	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '2F42h'.
22h (2F44h)	REG2F44	7:0	Default : 0x00 Access : R/W
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post g channel offset.
22h (2F45h)	REG2F45	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '2F44h'.
23h (2F46h)	REG2F46	7:0	Default : 0x00 Access : R/W
	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post b channel offset.
23h (2F47h)	REG2F47	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '2F46h'.
24h (2F48h)	REG2F48	7:0	Default : 0x00 Access : R/W
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post r channel gain.
24h (2F49h)	REG2F49	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '2F48h'.
25h (2F4Ah)	REG2F4A	7:0	Default : 0x00 Access : R/W
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post g channel gain.
25h (2F4Bh)	REG2F4B	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '2F4Ah'.
26h (2F4Ch)	REG2F4C	7:0	Default : 0x00 Access : R/W
	POST_MAIN_B_CON_GAIN[7:0]	7:0	Main window post b channel gain.
26h	REG2F4D	7:0	Default : 0x00 Access : R/W

XV_YCC Register (Bank = 2F, Sub-Bank = 25)				
Index (Absolute)	Mnemonic	Bit	Description	
(2F4Dh)	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN[11:8]	3:0	See description of '2F4Ch'.	
27h (2F4Eh)	REG2F4E	7:0	Default : 0x00	Access : R/W
	POST_SUB_R_BRI_OFFSET[7:0]	7:0	Sub window post r channel offset.	
27h (2F4Fh)	REG2F4F	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET[10:8]	2:0	See description of '2F4Eh'.	
28h (2F50h)	REG2F50	7:0	Default : 0x00	Access : R/W
	POST_SUB_G_BRI_OFFSET[7:0]	7:0	Sub window post g channel offset.	
28h (2F51h)	REG2F51	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET[10:8]	2:0	See description of '2F50h'.	
29h (2F52h)	REG2F52	7:0	Default : 0x00	Access : R/W
	POST_SUB_B_BRI_OFFSET[7:0]	7:0	Sub window post b channel offset.	
29h (2F53h)	REG2F53	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	POST_SUB_B_BRI_OFFSET[10:8]	2:0	See description of '2F52h'.	
2Ah (2F54h)	REG2F54	7:0	Default : 0x00	Access : R/W
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post r channel gain.	
2Ah (2F55h)	REG2F55	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[11:8]	3:0	See description of '2F54h'.	
2Bh (2F56h)	REG2F56	7:0	Default : 0x00	Access : R/W
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post g channel gain.	
2Bh (2F57h)	REG2F57	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '2F56h'.	
2Ch (2F58h)	REG2F58	7:0	Default : 0x00	Access : R/W
	POST_SUB_B_CON_GAIN[7:0]	7:0	Sub window post b channel gain.	
2Ch (2F59h)	REG2F59	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[11:8]	3:0	See description of '2F58h'.	
2Dh ~	-	7:0	Default : -	

XV_YCC Register (Bank = 2F, Sub-Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description
6Ah (2F5Ah ~ 2FD4h)	-	-	Reserved.

ACE2 Register (Bank = 2F, Sub-Bank = 27)

ACE2 Register (Bank = 2F, Sub-Bank = 27)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (2F00h)	REG2F00	7:0	Default : 0xFF	
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler. 00: Register of OSD/Interrupt 01: Register of IP1 Main Window 02: Register of IP2 Main Window 05: Register of OPM 06: Register of DNR 0A: Reserved 0C: Reserved 0F: Register of S_VOP 10: Register of VOP 12: Register of SCMI 18: Register of ACE 19: Register of PEAKING 1A: Register of DLC 20: Register of OP1_TOP 21: Register of ELA 22: Register of TDDI 23: Register of HVSP 24: Register of PAFRC 25: Register of xVYCC 26: Reserved 27: Register of ACE2	
20h (2F40h)	REG2F40	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_CTI_MEDIAN_EN	5	Sub window CTI median enable.	
	SUB_CTI_EN	4	Sub window CTI enable.	
	-	3:2	Reserved.	
	MAIN_CTI_MEDIAN_EN	1	Main window CTI median enable.	
	MAIN_CTI_EN	0	Main window CTI enable.	
21h (2F42h)	REG2F42	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	MAIN_CTI_STEP[1:0]	5:4	Main window CTI step.	
	-	3	Reserved.	
	MAIN_CTI_LPF_COEF[2:0]	2:0	Main window CTI low pass filter coefficient.	
21h	REG2F43	7:0	Default : 0x00	Access : R/W

ACE2 Register (Bank = 2F, Sub-Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description
(2F43h)	-	7:4	Reserved.
	MAIN_CTI_CORING_THRD[3:0]	3:0	Main window CTI coring threshold.
22h (2F44h)	REG2F44	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	MAIN_CTI_BAND_COEF[5:0]	5:0	Main window CTI band pass filter coefficient.
23h (2F46h)	REG2F46	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	SUB_CTI_STEP[1:0]	5:4	Sub window CTI step.
	-	3	Reserved.
	SUB_CTI_LPF_COEF[2:0]	2:0	Sub window CTI low pass filter enable.
23h (2F47h)	REG2F47	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SUB_CTI_CORING_THRD[3:0]	3:0	Sub window CTI coring threshold.
24h (2F48h)	REG2F48	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	SUB_CTI_BAND_COEF[5:0]	5:0	Sub window CTI band pass filter coefficient.
25h ~ 26h (2F4Ah ~ 2F4Dh)	-	7:0	Default : -
	-	-	Reserved.

DISP_TC Register (Bank = 30)

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
03h (3006h)	REG3006	7:0	Default : 0x00	Access : R/W
	OE_POL	7	OE polarity.	
	MAKEGPO_INTERLACE	6	Make GPO interlace.	
	-	5	Reserved.	
	ONE_FRAME_TOGGLE	4	One frame toggle mode.	
	GATE_DE	3	DE gating.	
	-	2	Reserved.	
	SYNC_FIELD	1	Sync field.	
	TG_SEL	0	TG select.	
03h (3007h)	REG3007	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	TC_CNT_EN	6	Enable tc_cnt.	
	SEP_PUA	5	Enable separate pua.	
	GATE_HS	4	Gate HS.	
	POLB	3	POLB.	
	-	2:0	Reserved.	
04h (3008h)	REG3008	7:0	Default : 0xFF	Access : R/W
	TC_H1END_ODD[7:0]	7:0	Odd mode hend of GPO1 / 2nd horizontal end of GPO1.	
04h (3009h)	REG3009	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	OVER_MODE_1	6	Special over mode enable of GPO1.	
	HEAD_PROC_EN_1	5	Head process enable of GPO1.	
	HEAD_MODE_1	4	Head mode enable of GPO1.	
	TC_H1END_ODD[11:8]	3:0	See description of '3008h'.	
05h (300Ah)	REG300A	7:0	Default : 0xFF	Access : R/W
	TC_H2END_ODD[7:0]	7:0	Odd mode hend of GPO2 / 2nd horizontal end of GPO2.	
05h (300Bh)	REG300B	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	OVER_MODE_2	6	Special over mode enable of GPO2.	
	HEAD_PROC_EN_2	5	Head process enable of GPO2.	
	HEAD_MODE_2	4	Head mode enable of GPO2.	

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
	TC_H2END_ODD[11:8]	3:0	See description of '300Ah'.	
06h (300Ch)	REG300C	7:0	Default : 0xFF	Access : R/W
	TC_H3END_ODD[7:0]	7:0	Odd mode hend of GPO3 / 2nd horizontal end of GPO3.	
06h (300Dh)	REG300D	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	OVER_MODE_3	6	Special over mode enable of GPO3.	
	HEAD_PROC_EN_3	5	Head process enable of GPO3.	
	HEAD_MODE_3	4	Head mode enable of GPO3.	
	TC_H3END_ODD[11:8]	3:0	See description of '300Ch'.	
07h (300Eh)	REG300E	7:0	Default : 0xFF	Access : R/W
	TC_H4END_ODD[7:0]	7:0	Odd mode hend of GPO4 / 2nd horizontal end of GPO4.	
07h (300Fh)	REG300F	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	OVER_MODE_4	6	Special over mode enable of GPO4.	
	HEAD_PROC_EN_4	5	Head process enable of GPO4.	
	HEAD_MODE_4	4	Head mode enable of GPO4.	
	TC_H4END_ODD[11:8]	3:0	See description of '300Eh'.	
08h (3010h)	REG3010	7:0	Default : 0xFF	Access : R/W
	TC_H5END_ODD[7:0]	7:0	Odd mode hend of GPO5 / 2nd horizontal end of GPO5.	
08h (3011h)	REG3011	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	OVER_MODE_5	6	Special over mode enable of GPO5.	
	HEAD_PROC_EN_5	5	Head process enable of GPO5.	
	HEAD_MODE_5	4	Head mode enable of GPO5.	
	TC_H5END_ODD[11:8]	3:0	See description of '3010h'.	
09h (3012h)	REG3012	7:0	Default : 0xFF	Access : R/W
	TC_H6END_ODD[7:0]	7:0	Odd mode hend of GPO6 / 2nd horizontal end of GPO9.	
09h (3013h)	REG3013	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	OVER_MODE_6	6	Special over mode enable of GPO6.	
	HEAD_PROC_EN_6	5	Head process enable of GPO6.	
	HEAD_MODE_6	4	Head mode enable of GPO6.	
	TC_H6END_ODD[11:8]	3:0	See description of '3012h'.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description
0Ah (3014h)	REG3014	7:0	Default : 0xFF Access : R/W
	TC_H7END_ODD[7:0]	7:0	Odd mode hend of GPO7 / 2nd horizontal end of GPOa.
0Ah (3015h)	REG3015	7:0	Default : 0x0F Access : R/W
	-	7	Reserved.
	OVER_MODE_7	6	Special over mode enable of GPO7.
	HEAD_PROC_EN_7	5	Head process enable of GPO7.
	HEAD_MODE_7	4	Head mode enable of GPO7.
	TC_H7END_ODD[11:8]	3:0	See description of '3014h'.
0Bh (3016h)	REG3016	7:0	Default : 0xFF Access : R/W
	TC_H8END_ODD[7:0]	7:0	Odd mode hend of GPO8 / 2nd horizontal end of GPOb.
0Bh (3017h)	REG3017	7:0	Default : 0x0F Access : R/W
	-	7	Reserved.
	OVER_MODE_8	6	Special over mode enable of GPO8.
	HEAD_PROC_EN_8	5	Head process enable of GPO8.
	HEAD_MODE_8	4	Head mode enable of GPO8.
	TC_H8END_ODD[11:8]	3:0	See description of '3016h'.
0Dh (301Ah)	REG301A	7:0	Default : 0xFF Access : R/W
	TC_V0ST[7:0]	7:0	Vertical start of GPO0.
0Dh (301Bh)	REG301B	7:0	Default : 0x0F Access : R/W
	FRAME_TOGO_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO0.
	TC_V0ST[11:8]	3:0	See description of '301Ah'.
0Eh (301Ch)	REG301C	7:0	Default : 0xFF Access : R/W
	TC_V0END[7:0]	7:0	Vertical end of GPO0.
0Eh (301Dh)	REG301D	7:0	Default : 0x0F Access : R/W
	FRAME_TOGO_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO0.
	TC_V0END[11:8]	3:0	See description of '301Ch'.
0Fh (301Eh)	REG301E	7:0	Default : 0xFF Access : R/W
	TC_H0ST[7:0]	7:0	Horizontal start of GPO0.
0Fh (301Fh)	REG301F	7:0	Default : 0x0F Access : R/W
	LINE_TOGO_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO0.
	TC_H0ST[11:8]	3:0	See description of '301Eh'.
10h (3020h)	REG3020	7:0	Default : 0xFF Access : R/W
	TC_H0END[7:0]	7:0	Horizontal end of GPO0.

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
10h (3021h)	REG3021	7:0	Default : 0x0F	Access : R/W
	LINE_TOG0_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO0.	
	TC_H0END[11:8]	3:0	See description of '3020h'.	
11h (3022h)	REG3022	7:0	Default : 0xFF	Access : R/W
	TC_V1ST[7:0]	7:0	Vertical start of GPO1.	
11h (3023h)	REG3023	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG1_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO1.	
	TC_V1ST[11:8]	3:0	See description of '3022h'.	
12h (3024h)	REG3024	7:0	Default : 0xFF	Access : R/W
	TC_V1END[7:0]	7:0	Vertical end of GPO1.	
12h (3025h)	REG3025	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG1_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO1.	
	TC_V1END[11:8]	3:0	See description of '3024h'.	
13h (3026h)	REG3026	7:0	Default : 0xFF	Access : R/W
	TC_H1ST[7:0]	7:0	Horizontal start of GPO1.	
13h (3027h)	REG3027	7:0	Default : 0x0F	Access : R/W
	LINE_TOG1_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO1.	
	TC_H1ST[11:8]	3:0	See description of '3026h'.	
14h (3028h)	REG3028	7:0	Default : 0xFF	Access : R/W
	TC_H1END[7:0]	7:0	Horizontal end of GPO1.	
14h (3029h)	REG3029	7:0	Default : 0x0F	Access : R/W
	LINE_TOG1_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO1.	
	TC_H1END[11:8]	3:0	See description of '3028h'.	
15h (302Ah)	REG302A	7:0	Default : 0xFF	Access : R/W
	TC_V2ST[7:0]	7:0	Vertical start of GPO2.	
15h (302Bh)	REG302B	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG2_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO2.	
	TC_V2ST[11:8]	3:0	See description of '302Ah'.	
16h (302Ch)	REG302C	7:0	Default : 0xFF	Access : R/W
	TC_V2END[7:0]	7:0	Vertical end of GPO2.	
16h (302Dh)	REG302D	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG2_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO2.	
	TC_V2END[11:8]	3:0	See description of '302Ch'.	

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
17h (302Eh)	REG302E	7:0	Default : 0xFF	Access : R/W
	TC_H2ST[7:0]	7:0	Horizontal start of GPO2.	
17h (302Fh)	REG302F	7:0	Default : 0x0F	Access : R/W
	LINE_TOG2_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO2.	
	TC_H2ST[11:8]	3:0	See description of '302Eh'.	
18h (3030h)	REG3030	7:0	Default : 0xFF	Access : R/W
	TC_H2END[7:0]	7:0	Horizontal end of GPO2.	
18h (3031h)	REG3031	7:0	Default : 0x0F	Access : R/W
	LINE_TOG2_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO2.	
	TC_H2END[11:8]	3:0	See description of '3030h'.	
19h (3032h)	REG3032	7:0	Default : 0xFF	Access : R/W
	TC_V3ST[7:0]	7:0	Vertical start of GPO3.	
19h (3033h)	REG3033	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG3_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO3.	
	TC_V3ST[11:8]	3:0	See description of '3032h'.	
1Ah (3034h)	REG3034	7:0	Default : 0xFF	Access : R/W
	TC_V3END[7:0]	7:0	Vertical end of GPO3.	
1Ah (3035h)	REG3035	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG3_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO3.	
	TC_V3END[11:8]	3:0	See description of '3034h'.	
1Bh (3036h)	REG3036	7:0	Default : 0xFF	Access : R/W
	TC_H3ST[7:0]	7:0	Horizontal start of GPO3.	
1Bh (3037h)	REG3037	7:0	Default : 0x0F	Access : R/W
	LINE_TOG3_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO3.	
	TC_H3ST[11:8]	3:0	See description of '3036h'.	
1Ch (3038h)	REG3038	7:0	Default : 0xFF	Access : R/W
	TC_H3END[7:0]	7:0	Horizontal end of GPO3.	
1Ch (3039h)	REG3039	7:0	Default : 0x0F	Access : R/W
	LINE_TOG3_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO3.	
	TC_H3END[11:8]	3:0	See description of '3038h'.	
1Dh (303Ah)	REG303A	7:0	Default : 0xFF	Access : R/W
	TC_V4ST[7:0]	7:0	Vertical start of GPO4.	
1Dh	REG303B	7:0	Default : 0x0F	Access : R/W

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
(303Bh)	FRAME_TOG4_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO4.	
	TC_V4ST[11:8]	3:0	See description of '303Ah'.	
1Eh (303Ch)	REG303C	7:0	Default : 0xFF	Access : R/W
	TC_V4END[7:0]	7:0	Vertical end of GPO4.	
1Eh (303Dh)	REG303D	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG4_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO4.	
	TC_V4END[11:8]	3:0	See description of '303Ch'.	
1Fh (303Eh)	REG303E	7:0	Default : 0xFF	Access : R/W
	TC_H4ST[7:0]	7:0	Horizontal start of GPO4.	
1Fh (303Fh)	REG303F	7:0	Default : 0x0F	Access : R/W
	LINE_TOG4_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO4.	
	TC_H4ST[11:8]	3:0	See description of '303Eh'.	
20h (3040h)	REG3040	7:0	Default : 0xFF	Access : R/W
	TC_H4END[7:0]	7:0	Horizontal end of GPO4.	
20h (3041h)	REG3041	7:0	Default : 0x0F	Access : R/W
	LINE_TOG4_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO4.	
	TC_H4END[11:8]	3:0	See description of '3040h'.	
21h (3042h)	REG3042	7:0	Default : 0xFF	Access : R/W
	TC_V5ST[7:0]	7:0	Vertical start of GPO5.	
21h (3043h)	REG3043	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG5_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO5.	
	TC_V5ST[11:8]	3:0	See description of '3042h'.	
22h (3044h)	REG3044	7:0	Default : 0xFF	Access : R/W
	TC_V5END[7:0]	7:0	Vertical end of GPO5.	
22h (3045h)	REG3045	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG5_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO5.	
	TC_V5END[11:8]	3:0	See description of '3044h'.	
23h (3046h)	REG3046	7:0	Default : 0xFF	Access : R/W
	TC_H5ST[7:0]	7:0	Horizontal start of GPO5.	
23h (3047h)	REG3047	7:0	Default : 0x0F	Access : R/W
	LINE_TOG5_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO5.	
	TC_H5ST[11:8]	3:0	See description of '3046h'.	
24h	REG3048	7:0	Default : 0xFF	Access : R/W

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
(3048h)	TC_H5END[7:0]	7:0	Horizontal end of GPO5.	
24h	REG3049	7:0	Default : 0x0F	Access : R/W
(3049h)	LINE_TOG5_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO5.	
	TC_H5END[11:8]	3:0	See description of '3048h'.	
25h	REG304A	7:0	Default : 0xFF	Access : R/W
(304Ah)	TC_V6ST[7:0]	7:0	Vertical start of GPO6.	
25h	REG304B	7:0	Default : 0x0F	Access : R/W
(304Bh)	FRAME_TOG6_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO6.	
	TC_V6ST[11:8]	3:0	See description of '304Ah'.	
26h	REG304C	7:0	Default : 0xFF	Access : R/W
(304Ch)	TC_V6END[7:0]	7:0	Vertical end of GPO6.	
26h	REG304D	7:0	Default : 0x0F	Access : R/W
(304Dh)	FRAME_TOG6_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO6.	
	TC_V6END[11:8]	3:0	See description of '304Ch'.	
27h	REG304E	7:0	Default : 0xFF	Access : R/W
(304Eh)	TC_H6ST[7:0]	7:0	Horizontal start of GPO6.	
27h	REG304F	7:0	Default : 0x0F	Access : R/W
(304Fh)	LINE_TOG6_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO6.	
	TC_H6ST[11:8]	3:0	See description of '304Eh'.	
28h	REG3050	7:0	Default : 0xFF	Access : R/W
(3050h)	TC_H6END[7:0]	7:0	Horizontal end of GPO6.	
28h	REG3051	7:0	Default : 0x0F	Access : R/W
(3051h)	LINE_TOG6_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO6.	
	TC_H6END[11:8]	3:0	See description of '3050h'.	
29h	REG3052	7:0	Default : 0xFF	Access : R/W
(3052h)	TC_V7ST[7:0]	7:0	Vertical start of GPO7.	
29h	REG3053	7:0	Default : 0x0F	Access : R/W
(3053h)	FRAME_TOG7_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO7.	
	TC_V7ST[11:8]	3:0	See description of '3052h'.	
2Ah	REG3054	7:0	Default : 0xFF	Access : R/W
(3054h)	TC_V7END[7:0]	7:0	Vertical end of GPO7.	
2Ah	REG3055	7:0	Default : 0x0F	Access : R/W
(3055h)	FRAME_TOG7_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO7.	

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
	TC_V7END[11:8]	3:0	See description of '3054h'.	
2Bh (3056h)	REG3056	7:0	Default : 0xFF	Access : R/W
	TC_H7ST[7:0]	7:0	Horizontal start of GPO7.	
2Bh (3057h)	REG3057	7:0	Default : 0x0F	Access : R/W
	LINE_TOG7_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO7.	
	TC_H7ST[11:8]	3:0	See description of '3056h'.	
2Ch (3058h)	REG3058	7:0	Default : 0xFF	Access : R/W
	TC_H7END[7:0]	7:0	Horizontal end of GPO7.	
2Ch (3059h)	REG3059	7:0	Default : 0x0F	Access : R/W
	LINE_TOG7_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO7.	
	TC_H7END[11:8]	3:0	See description of '3058h'.	
2Dh (305Ah)	REG305A	7:0	Default : 0xFF	Access : R/W
	TC_V8ST[7:0]	7:0	Vertical start of GPO8.	
2Dh (305Bh)	REG305B	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG8_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO8.	
	TC_V8ST[11:8]	3:0	See description of '305Ah'.	
2Eh (305Ch)	REG305C	7:0	Default : 0xFF	Access : R/W
	TC_V8END[7:0]	7:0	Vertical end of GPO8.	
2Eh (305Dh)	REG305D	7:0	Default : 0x0F	Access : R/W
	FRAME_TOG8_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO8.	
	TC_V8END[11:8]	3:0	See description of '305Ch'.	
2Fh (305Eh)	REG305E	7:0	Default : 0xFF	Access : R/W
	TC_H8ST[7:0]	7:0	Horizontal start of GPO8.	
2Fh (305Fh)	REG305F	7:0	Default : 0x0F	Access : R/W
	LINE_TOG8_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO8.	
	TC_H8ST[11:8]	3:0	See description of '305Eh'.	
30h (3060h)	REG3060	7:0	Default : 0xFF	Access : R/W
	TC_H8END[7:0]	7:0	Horizontal end of GPO8.	
30h (3061h)	REG3061	7:0	Default : 0x0F	Access : R/W
	LINE_TOG8_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO8.	
	TC_H8END[11:8]	3:0	See description of '3060h'.	
31h (3062h)	REG3062	7:0	Default : 0xFF	Access : R/W
	TC_V9ST[7:0]	7:0	Vertical start of GPO9.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description
31h (3063h)	REG3063	7:0	Default : 0x0F Access : R/W
	FRAME_TOG9_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO9.
	TC_V9ST[11:8]	3:0	See description of '3062h'.
32h (3064h)	REG3064	7:0	Default : 0xFF Access : R/W
	TC_V9END[7:0]	7:0	Vertical end of GPO9.
32h (3065h)	REG3065	7:0	Default : 0x0F Access : R/W
	FRAME_TOG9_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO9.
	TC_V9END[11:8]	3:0	See description of '3064h'.
33h (3066h)	REG3066	7:0	Default : 0xFF Access : R/W
	TC_H9ST[7:0]	7:0	Horizontal start of GPO9.
33h (3067h)	REG3067	7:0	Default : 0x0F Access : R/W
	LINE_TOG9_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO9.
	TC_H9ST[11:8]	3:0	See description of '3066h'.
34h (3068h)	REG3068	7:0	Default : 0xFF Access : R/W
	TC_H9END[7:0]	7:0	Horizontal end of GPO9.
34h (3069h)	REG3069	7:0	Default : 0x0F Access : R/W
	LINE_TOG9_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO9.
	TC_H9END[11:8]	3:0	See description of '3068h'.
35h (306Ah)	REG306A	7:0	Default : 0xFF Access : R/W
	TC_VAST[7:0]	7:0	Vertical start of GPOA.
35h (306Bh)	REG306B	7:0	Default : 0x0F Access : R/W
	FRAME_TOGA_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPOA.
	TC_VAST[11:8]	3:0	See description of '306Ah'.
36h (306Ch)	REG306C	7:0	Default : 0xFF Access : R/W
	TC_VAEND[7:0]	7:0	Vertical end of GPOA.
36h (306Dh)	REG306D	7:0	Default : 0x0F Access : R/W
	FRAME_TOGA_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPOA.
	TC_VAEND[11:8]	3:0	See description of '306Ch'.
37h (306Eh)	REG306E	7:0	Default : 0xFF Access : R/W
	TC_HAST[7:0]	7:0	Horizontal start of GPOA.
37h (306Fh)	REG306F	7:0	Default : 0x0F Access : R/W
	LINE_TOGA_H4[3:0]	7:4	Line tog number MSB 4 bit of GPOA.
	TC_HAST[11:8]	3:0	See description of '306Eh'.

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
38h (3070h)	REG3070	7:0	Default : 0xFF	Access : R/W
	TC_HAEND[7:0]	7:0	Horizontal end of GPOA.	
38h (3071h)	REG3071	7:0	Default : 0x0F	Access : R/W
	LINE_TOGA_L4[3:0]	7:4	Line tog number LSB 4 bit of GPOA.	
	TC_HAEND[11:8]	3:0	See description of '3070h'.	
39h (3072h)	REG3072	7:0	Default : 0x00	Access : R/W
	G0OP	7	OP setting of GPO0.	
	G0TC	6	TC setting of GPO0.	
	G0ES	5	ES setting of GPO0.	
	G0TS[1:0]	4:3	TS setting of GPO0.	
	G0CS[2:0]	2:0	CS setting of GPO0.	
39h (3073h)	REG3073	7:0	Default : 0x00	Access : R/W
	G1OP	7	OP setting of GPO1.	
	G1TC	6	TC setting of GPO1.	
	G1ES	5	ES setting of GPO1.	
	G1TS[1:0]	4:3	TS setting of GPO1.	
	G1CS[2:0]	2:0	CS setting of GPO1.	
3Ah (3074h)	REG3074	7:0	Default : 0x00	Access : R/W
	G2OP	7	OP setting of GPO2.	
	G2TC	6	TC setting of GPO2.	
	G2ES	5	ES setting of GPO2.	
	G2TS[1:0]	4:3	TS setting of GPO2.	
	G2CS[2:0]	2:0	CS setting of GPO2.	
3Ah (3075h)	REG3075	7:0	Default : 0x00	Access : R/W
	G3OP	7	OP setting of GPO3.	
	G3TC	6	TC setting of GPO3.	
	G3ES	5	ES setting of GPO3.	
	G3TS[1:0]	4:3	TS setting of GPO3.	
	G3CS[2:0]	2:0	CS setting of GPO3.	
3Bh (3076h)	REG3076	7:0	Default : 0x00	Access : R/W
	G4OP	7	OP setting of GPO4.	
	G4TC	6	TC setting of GPO4.	
	G4ES	5	ES setting of GPO4.	

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
	G4TS[1:0]	4:3	TS setting of GPO4.	
	G4CS[2:0]	2:0	CS setting of GPO4.	
3Bh (3077h)	REG3077	7:0	Default : 0x00	Access : R/W
	G5OP	7	OP setting of GPO5.	
	G5TC	6	TC setting of GPO5.	
	G5ES	5	ES setting of GPO5.	
	G5TS[1:0]	4:3	TS setting of GPO5.	
	G5CS[2:0]	2:0	CS setting of GPO5.	
3Ch (3078h)	REG3078	7:0	Default : 0x00	Access : R/W
	G6OP	7	OP setting of GPO6.	
	G6TC	6	TC setting of GPO6.	
	G6ES	5	ES setting of GPO6.	
	G6TS[1:0]	4:3	TS setting of GPO6.	
	G6CS[2:0]	2:0	CS setting of GPO6.	
3Ch (3079h)	REG3079	7:0	Default : 0x00	Access : R/W
	G7OP	7	OP setting of GPO7.	
	G7TC	6	TC setting of GPO7.	
	G7ES	5	ES setting of GPO7.	
	G7TS[1:0]	4:3	TS setting of GPO7.	
	G7CS[2:0]	2:0	CS setting of GPO7.	
3Dh (307Ah)	REG307A	7:0	Default : 0x00	Access : R/W
	G8OP	7	OP setting of GPO8.	
	G8TC	6	TC setting of GPO8.	
	G8ES	5	ES setting of GPO8.	
	G8TS[1:0]	4:3	TS setting of GPO8.	
	G8CS[2:0]	2:0	CS setting of GPO8.	
3Dh (307Bh)	REG307B	7:0	Default : 0x00	Access : R/W
	G9OP	7	OP setting of GPO9.	
	G9TC	6	TC setting of GPO9.	
	G9ES	5	ES setting of GPO9.	
	G9TS[1:0]	4:3	TS setting of GPO9.	
	G9CS[2:0]	2:0	CS setting of GPO9.	
3Eh	REG307C	7:0	Default : 0x00	Access : R/W

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
(307Ch)	GAOP	7	OP setting of GPOA.	
	GATC	6	TC setting of GPOA.	
	GAES	5	ES setting of GPOA.	
	GATS[1:0]	4:3	TS setting of GPOA.	
	GACS[2:0]	2:0	CS setting of GPOA.	
3Eh (307Dh)	REG307D	7:0	Default : 0x00	Access : R/W
	GBOP	7	OP setting of GPOB.	
	GBTC	6	TC setting of GPOB.	
	GBES	5	ES setting of GPOB.	
	GBTS[1:0]	4:3	TS setting of GPOB.	
	GBCS[2:0]	2:0	CS setting of GPOB.	
3Fh (307Eh)	REG307E	7:0	Default : 0x00	Access : R/W
	GPO5_EN	7	GPO5 enable.	
	GPO4_EN	6	GPO4 enable.	
	GPO3_EN	5	GPO3 enable.	
	GPO2_EN	4	GPO2 enable.	
	GPO1_EN	3	GPO1 enable.	
	GPO0_EN	2	GPO0 enable.	
	-	1:0	Reserved.	
3Fh (307Fh)	REG307F	7:0	Default : 0x00	Access : R/W
	GPOD_EN	7	GPOD enable.	
	GPOC_EN	6	GPOC enable.	
	GPOB_EN	5	GPOB enable.	
	GPOA_EN	4	GPOA enable.	
	GPO9_EN	3	GPO9 enable.	
	GPO8_EN	2	GPO8 enable.	
	GPO7_EN	1	GPO7 enable.	
	GPO6_EN	0	GPO6 enable.	
40h (3080h)	REG3080	7:0	Default : 0xFF	Access : R/W
	TC_VBST[7:0]	7:0	Vertical start of GPOB.	
40h (3081h)	REG3081	7:0	Default : 0x0F	Access : R/W
	FRAME_TOGB_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPOB.	
	TC_VBST[11:8]	3:0	See description of '3080h'.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description
41h (3082h)	REG3082	7:0	Default : 0xFF
	TC_VBEND[7:0]	7:0	Vertical end of GPOB.
41h (3083h)	REG3083	7:0	Default : 0x0F
	FRAME_TOGB_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPOB.
	TC_VBEND[11:8]	3:0	See description of '3082h'.
42h (3084h)	REG3084	7:0	Default : 0xFF
	TC_HBST[7:0]	7:0	Horizontal start of GPOB.
42h (3085h)	REG3085	7:0	Default : 0x0F
	LINE_TOGB_H4[3:0]	7:4	Line tog number MSB 4 bit of GPOB.
	TC_HBST[11:8]	3:0	See description of '3084h'.
43h (3086h)	REG3086	7:0	Default : 0xFF
	TC_HBEND[7:0]	7:0	Horizontal end of GPOB.
43h (3087h)	REG3087	7:0	Default : 0x0F
	LINE_TOGB_L4[3:0]	7:4	Line tog number LSB 4 bit of GPOB.
	TC_HBEND[11:8]	3:0	See description of '3086h'.
44h (3088h)	REG3088	7:0	Default : 0xFF
	TC_VCST[7:0]	7:0	Vertical start of GPOC.
44h (3089h)	REG3089	7:0	Default : 0x0F
	FRAME_TOGC_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPOC.
	TC_VCST[11:8]	3:0	See description of '3088h'.
45h (308Ah)	REG308A	7:0	Default : 0xFF
	TC_VCEND[7:0]	7:0	Vertical end of GPOC.
45h (308Bh)	REG308B	7:0	Default : 0x0F
	FRAME_TOGC_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPOC.
	TC_VCEND[11:8]	3:0	See description of '308Ah'.
46h (308Ch)	REG308C	7:0	Default : 0xFF
	TC_HCST[7:0]	7:0	Horizontal start of GPOC.
46h (308Dh)	REG308D	7:0	Default : 0x0F
	LINE_TOGC_H4[3:0]	7:4	Line tog number MSB 4 bit of GPOC.
	TC_HCST[11:8]	3:0	See description of '308Ch'.
47h (308Eh)	REG308E	7:0	Default : 0xFF
	TC_HCEND[7:0]	7:0	Horizontal end of GPOC.
47h	REG308F	7:0	Default : 0x0F

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
(308Fh)	LINE_TOGC_L4[3:0]	7:4	Line tog number LSB 4 bit of GPOC.	
	TC_HCEND[11:8]	3:0	See description of '308Eh'.	
48h (3090h)	REG3090	7:0	Default : 0xFF	Access : R/W
	TC_VDST[7:0]	7:0	Vertical start of GPOD.	
48h (3091h)	REG3091	7:0	Default : 0x0F	Access : R/W
	FRAME_TOGD_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPOD.	
	TC_VDST[11:8]	3:0	See description of '3090h'.	
49h (3092h)	REG3092	7:0	Default : 0xFF	Access : R/W
	TC_VDEND[7:0]	7:0	Vertical end of GPOD.	
49h (3093h)	REG3093	7:0	Default : 0x0F	Access : R/W
	FRAME_TOGD_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPOD.	
	TC_VDEND[11:8]	3:0	See description of '3092h'.	
4Ah (3094h)	REG3094	7:0	Default : 0xFF	Access : R/W
	TC_HDST[7:0]	7:0	Horizontal start of GPOD.	
4Ah (3095h)	REG3095	7:0	Default : 0x0F	Access : R/W
	LINE_TOGD_H4[3:0]	7:4	Line tog number MSB 4 bit of GPOD.	
	TC_HDST[11:8]	3:0	See description of '3094h'.	
4Bh (3096h)	REG3096	7:0	Default : 0xFF	Access : R/W
	TC_HDEND[7:0]	7:0	Horizontal end of GPOD.	
4Bh (3097h)	REG3097	7:0	Default : 0x0F	Access : R/W
	LINE_TOGD_L4[3:0]	7:4	Line tog number LSB 4 bit of GPOD.	
	TC_HDEND[11:8]	3:0	See description of '3096h'.	
4Ch (3098h)	REG3098	7:0	Default : 0xFF	Access : R/W
	TC_H1ST2[7:0]	7:0	2nd horizontal start of GPO1.	
4Ch (3099h)	REG3099	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H1ST2[11:8]	3:0	See description of '3098h'.	
4Dh (309Ah)	REG309A	7:0	Default : 0xFF	Access : R/W
	TC_H1ST3[7:0]	7:0	3rd horizontal start of GPO1.	
4Dh (309Bh)	REG309B	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H1ST3[11:8]	3:0	See description of '309Ah'.	
4Eh	REG309C	7:0	Default : 0xFF	Access : R/W

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
(309Ch)	TC_H1END3[7:0]	7:0	3rd horizontal end of GPO1.	
4Eh (309Dh)	REG309D	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H1END3[11:8]	3:0	See description of '309Ch'.	
4Fh (309Eh)	REG309E	7:0	Default : 0xFF	Access : R/W
	TC_H2ST2[7:0]	7:0	2nd horizontal start of GPO2.	
4Fh (309Fh)	REG309F	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H2ST2[11:8]	3:0	See description of '309Eh'.	
50h (30A0h)	REG30A0	7:0	Default : 0xFF	Access : R/W
	TC_H2ST3[7:0]	7:0	3rd horizontal start of GPO2.	
50h (30A1h)	REG30A1	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H2ST3[11:8]	3:0	See description of '30A0h'.	
51h (30A2h)	REG30A2	7:0	Default : 0xFF	Access : R/W
	TC_H2END3[7:0]	7:0	3rd horizontal end of GPO2.	
51h (30A3h)	REG30A3	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H2END3[11:8]	3:0	See description of '30A2h'.	
52h (30A4h)	REG30A4	7:0	Default : 0xFF	Access : R/W
	TC_H3ST2[7:0]	7:0	2nd horizontal start of GPO3.	
52h (30A5h)	REG30A5	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H3ST2[11:8]	3:0	See description of '30A4h'.	
53h (30A6h)	REG30A6	7:0	Default : 0xFF	Access : R/W
	TC_H3ST3[7:0]	7:0	3rd horizontal start of GPO3.	
53h (30A7h)	REG30A7	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H3ST3[11:8]	3:0	See description of '30A6h'.	
54h (30A8h)	REG30A8	7:0	Default : 0xFF	Access : R/W
	TC_H3END3[7:0]	7:0	3rd horizontal end of GPO3.	
54h (30A9h)	REG30A9	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
	TC_H3END3[11:8]	3:0	See description of '30A8h'.	
55h (30AAh)	REG30AA	7:0	Default : 0xFF	Access : R/W
	TC_H4ST2[7:0]	7:0	2nd horizontal start of GPO4.	
55h (30ABh)	REG30AB	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H4ST2[11:8]	3:0	See description of '30AAh'.	
56h (30ACh)	REG30AC	7:0	Default : 0xFF	Access : R/W
	TC_H4ST3[7:0]	7:0	3rd horizontal start of GPO4.	
56h (30ADh)	REG30AD	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H4ST3[11:8]	3:0	See description of '30ACh'.	
57h (30AEh)	REG30AE	7:0	Default : 0xFF	Access : R/W
	TC_H4END3[7:0]	7:0	3rd horizontal end of GPO4.	
57h (30AFh)	REG30AF	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H4END3[11:8]	3:0	See description of '30AEh'.	
58h (30B0h)	REG30B0	7:0	Default : 0xFF	Access : R/W
	TC_H5ST2[7:0]	7:0	2nd horizontal start of GPO5.	
58h (30B1h)	REG30B1	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H5ST2[11:8]	3:0	See description of '30B0h'.	
59h (30B2h)	REG30B2	7:0	Default : 0xFF	Access : R/W
	TC_H5ST3[7:0]	7:0	3rd horizontal start of GPO5.	
59h (30B3h)	REG30B3	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H5ST3[11:8]	3:0	See description of '30B2h'.	
5Ah (30B4h)	REG30B4	7:0	Default : 0xFF	Access : R/W
	TC_H5END3[7:0]	7:0	3rd horizontal end of GPO5.	
5Ah (30B5h)	REG30B5	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H5END3[11:8]	3:0	See description of '30B4h'.	
5Bh (30B6h)	REG30B6	7:0	Default : 0xFF	Access : R/W
	TC_H9ST2[7:0]	7:0	2nd horizontal start of GPO9.	

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
5Bh (30B7h)	REG30B7	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H9ST2[11:8]	3:0	See description of '30B6h'.	
5Ch (30B8h)	REG30B8	7:0	Default : 0xFF	Access : R/W
	TC_H9ST3[7:0]	7:0	3rd horizontal start of GPO9.	
5Ch (30B9h)	REG30B9	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H9ST3[11:8]	3:0	See description of '30B8h'.	
5Dh (30BAh)	REG30BA	7:0	Default : 0xFF	Access : R/W
	TC_H9END3[7:0]	7:0	3rd horizontal end of GPO9.	
5Dh (30BBh)	REG30BB	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_H9END3[11:8]	3:0	See description of '30BAh'.	
5Eh (30BCh)	REG30BC	7:0	Default : 0xFF	Access : R/W
	TC_HAST2[7:0]	7:0	2nd horizontal start of GPOA.	
5Eh (30BDh)	REG30BD	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_HAST2[11:8]	3:0	See description of '30BCh'.	
5Fh (30BEh)	REG30BE	7:0	Default : 0xFF	Access : R/W
	TC_HAST3[7:0]	7:0	3rd horizontal start of GPOA.	
5Fh (30BFh)	REG30BF	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_HAST3[11:8]	3:0	See description of '30BEh'.	
60h (30C0h)	REG30C0	7:0	Default : 0xFF	Access : R/W
	TC_HAEND3[7:0]	7:0	3rd horizontal end of GPOA.	
60h (30C1h)	REG30C1	7:0	Default : 0x0F	Access : R/W
	-	7:4	Reserved.	
	TC_HAEND3[11:8]	3:0	See description of '30C0h'.	
61h (30C2h)	REG30C2	7:0	Default : 0x00	Access : R/W
	GPO7_FF_OEN	7	GPO7_FF output enable.	
	GPO6_FF_OEN	6	GPO6_FF output enable.	
	GPO5_FF_OEN	5	GPO5_FF output enable.	
	GPO4_FF_OEN	4	GPO4_FF output enable.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description
	GPO3_FF_OEN	3	GPO3_FF output enable.
	GPO2_FF_OEN	2	GPO2_FF output enable.
	GPO1_FF_OEN	1	GPO1_FF output enable.
	GPO0_FF_OEN	0	GPO0_FF output enable.
61h (30C3h)	REG30C3	7:0	Default : 0x00
	-	7:6	Reserved.
	GPOD_FF_OEN	5	GPOD_FF output enable.
	GPOC_FF_OEN	4	GPOC_FF output enable.
	GPOB_FF_OEN	3	GPOB_FF output enable.
	GPOA_FF_OEN	2	GPOA_FF output enable.
	GPO9_FF_OEN	1	GPO9_FF output enable.
	GPO8_FF_OEN	0	GPO8_FF output enable.
62h (30C4h)	REG30C4	7:0	Default : 0x00
	GPO_CS8_EN	7	GPO_CS8 enable.
	GPO_CS7_EN	6	GPO_CS7 enable.
	GPO_CS6_EN	5	GPO_CS6 enable.
	GPO_CS5_EN	4	GPO_CS5 enable.
	GPO_CS4_EN	3	GPO_CS4 enable.
	GPO_CS3_EN	2	GPO_CS3 enable.
	GPO_CS2_EN	1	GPO_CS2 enable.
	GPO_CS1_EN	0	GPO_CS1 enable.
62h (30C5h)	REG30C5	7:0	Default : 0x00
	-	7:2	Reserved.
	GPO_CS10_EN	1	GPO_CS10 enable.
	GPO_CS9_EN	0	GPO_CS9 enable.
63h (30C6h)	REG30C6	7:0	Default : 0x00
	TCYCLE_ST_V[7:0]	7:0	Active cycle start vertical position.
63h (30C7h)	REG30C7	7:0	Default : 0x00
	-	7:3	Reserved.
	TCYCLE_ST_V[10:8]	2:0	See description of '30C6h'.
64h (30C8h)	REG30C8	7:0	Default : 0x00
	TBLANK_ST_V[7:0]	7:0	Blank cycle start vertical position.
64h	REG30C9	7:0	Default : 0x00

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description
(30C9h)	-	7:3	Reserved.
	TBLANK_ST_V[10:8]	2:0	See description of '30C8h'.
65h (30CAh)	REG30CA	7:0	Default : 0x00
	TOG_H[7:0]	7:0	Line increment start horizontal position.
65h (30CBh)	REG30CB	7:0	Default : 0x00
	-	7:4	Reserved.
	TOG_H[11:8]	3:0	See description of '30CAh'.
66h (30CCh)	REG30CC	7:0	Default : 0x00
	TCYCLE_TOG_RATE[7:0]	7:0	Active cycle CS toggle rate.
67h (30CEh)	REG30CE	7:0	Default : 0x00
	TBLANK_LENGTH[7:0]	7:0	Blank cycle length.
67h (30CFh)	REG30CF	7:0	Default : 0x00
	-	7:1	Reserved.
	TBLANK_LENGTH[8]	0	See description of '30CEh'.
68h (30D0h)	REG30D0	7:0	Default : 0x00
	SET2_DELAY[3:0]	7:4	CS5, 6 to CS1, 2 line delay.
	SET1_DELAY[3:0]	3:0	CS3, 4 to CS1, 2 line delay.
68h (30D1h)	REG30D1	7:0	Default : 0x00
	SET4_DELAY[3:0]	7:4	CS9, 10 to CS1, 2 line delay.
	SET3_DELAY[3:0]	3:0	CS7, 8 to CS1, 2 line delay.
69h (30D2h)	REG30D2	7:0	Default : 0x00
	GPO_CS8_FF_OEN	7	GPO_CS8_FF output enable.
	GPO_CS7_FF_OEN	6	GPO_CS7_FF output enable.
	GPO_CS6_FF_OEN	5	GPO_CS6_FF output enable.
	GPO_CS5_FF_OEN	4	GPO_CS5_FF output enable.
	GPO_CS4_FF_OEN	3	GPO_CS4_FF output enable.
	GPO_CS3_FF_OEN	2	GPO_CS3_FF output enable.
	GPO_CS2_FF_OEN	1	GPO_CS2_FF output enable.
	GPO_CS1_FF_OEN	0	GPO_CS1_FF output enable.
69h (30D3h)	REG30D3	7:0	Default : 0x00
	-	7:2	Reserved.
	GPO_CS10_FF_OEN	1	GPO_CS10_FF output enable.
	GPO_CS9_FF_OEN	0	GPO_CS9_FF output enable.

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description
6Ah (30D4h)	REG30D4	7:0	Default : 0xFF Access : R/W
	TC_HBST2[7:0]	7:0	2nd horizontal start of GPOB.
6Ah (30D5h)	REG30D5	7:0	Default : 0x0F Access : R/W
	-	7:4	Reserved.
	TC_HBST2[11:8]	3:0	See description of '30D4h'.
6Bh (30D6h)	REG30D6	7:0	Default : 0xFF Access : R/W
	TC_HBST3[7:0]	7:0	3rd horizontal start of GPOB.
6Bh (30D7h)	REG30D7	7:0	Default : 0x0F Access : R/W
	-	7:4	Reserved.
	TC_HBST3[11:8]	3:0	See description of '30D6h'.
6Ch (30D8h)	REG30D8	7:0	Default : 0xFF Access : R/W
	TC_HBEND3[7:0]	7:0	3rd horizontal end of GPOB.
6Ch (30D9h)	REG30D9	7:0	Default : 0x0F Access : R/W
	-	7:4	Reserved.
	TC_HBEND3[11:8]	3:0	See description of '30D8h'.
6Dh (30DAh)	REG30DA	7:0	Default : 0x00 Access : R/W
	GCOP	7	OP setting of GPOC.
	GCTC	6	TC setting of GPOC.
	GCES	5	ES setting of GPOC.
	GCTS[1:0]	4:3	TS setting of GPOC.
	GCCS[2:0]	2:0	CS setting of GPOC.
6Dh (30DBh)	REG30DB	7:0	Default : 0x00 Access : R/W
	GDOP	7	OP setting of GPOD.
	GDTC	6	TC setting of GPOD.
	GDES	5	ES setting of GPOD.
	GDTS[1:0]	4:3	TS setting of GPOD.
	GDCS[2:0]	2:0	CS setting of GPOD.
6Eh (30DCh)	REG30DC	7:0	Default : 0x00 Access : R/W
	GPO7_N_1_SEL	7	GPO7 n 1 select.
	GPO6_N_1_SEL	6	GPO6 n 1 select.
	GPO5_N_1_SEL	5	GPO5 n 1 select.
	GPO4_N_1_SEL	4	GPO4 n 1 select.
	GPO3_N_1_SEL	3	GPO3 n 1 select.

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
	GPO2_N_1_SEL	2	GPO2 n 1 select.	
	GPO1_N_1_SEL	1	GPO1 n 1 select.	
	GPO0_N_1_SEL	0	GPO0 n 1 select.	
6Eh (30DDh)	REG30DD	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	GPOD_N_1_SEL	5	GPOd n 1 select.	
	GPOC_N_1_SEL	4	GPOc n 1 select.	
	GPOB_N_1_SEL	3	GPOb n 1 select.	
	GPOA_N_1_SEL	2	GPOa n 1 select.	
	GPO9_N_1_SEL	1	GPO9 n 1 select.	
	GPO8_N_1_SEL	0	GPO8 n 1 select.	
6Fh (30DEh)	REG30DE	7:0	Default : 0x00	Access : R/W
	GPO3_EN_3HV[1:0]	7:6	GPO3 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.	
	GPO2_EN_3HV[1:0]	5:4	GPO2 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.	
	GPO1_EN_3HV[1:0]	3:2	GPO1 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.	
	GPO0_EN_3HV[1:0]	1:0	GPO0 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.	
6Fh (30DFh)	REG30DF	7:0	Default : 0x00	Access : R/W
	GPO7_EN_3HV[1:0]	7:6	GPO7 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.	
	GPO6_EN_3HV[1:0]	5:4	GPO6 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.	
	GPO5_EN_3HV[1:0]	3:2	GPO5 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.	
	GPO4_EN_3HV[1:0]	1:0	GPO4 3hv enable. Bit[0]:enable 2nd hv.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description
			Bit[1]:enable 3rd hv.
70h (30E0h)	REG30E0	7:0	Default : 0x00 Access : R/W
	GPOB_EN_3HV[1:0]	7:6	GPOB 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.
	GPOA_EN_3HV[1:0]	5:4	GPOA 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.
	GPO9_EN_3HV[1:0]	3:2	GPO9 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.
	GPO8_EN_3HV[1:0]	1:0	GPO8 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.
70h (30E1h)	REG30E1	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	GPOD_EN_3HV[1:0]	3:2	GPOD 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.
	GPOC_EN_3HV[1:0]	1:0	GPOC 3hv enable. Bit[0]:enable 2nd hv. Bit[1]:enable 3rd hv.
71h (30E2h)	REG30E2	7:0	Default : 0x00 Access : R/W
	FRAME_TOG7_MD	7	GPO7 frame toggle mode enable.
	FRAME_TOG6_MD	6	GPO6 frame toggle mode enable.
	FRAME_TOG5_MD	5	GPO5 frame toggle mode enable.
	FRAME_TOG4_MD	4	GPO4 frame toggle mode enable.
	FRAME_TOG3_MD	3	GPO3 frame toggle mode enable.
	FRAME_TOG2_MD	2	GPO2 frame toggle mode enable.
	FRAME_TOG1_MD	1	GPO1 frame toggle mode enable.
	FRAME_TOG0_MD	0	GPO0 frame toggle mode enable.
71h (30E3h)	REG30E3	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	FRAME_TOGD_MD	5	GPOD frame toggle mode enable.
	FRAME_TOGC_MD	4	GPOC frame toggle mode enable.

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
	FRAME_TOGB_MD	3	GPOB frame toggle mode enable.	
	FRAME_TOGA_MD	2	GPOA frame toggle mode enable.	
	FRAME_TOG9_MD	1	GPO9 frame toggle mode enable.	
	FRAME_TOG8_MD	0	GPO8 frame toggle mode enable.	
72h (30E4h)	REG30E4	7:0	Default : 0x00	Access : R/W
	LINE_TOG7_MD	7	GPO7 line toggle mode enable.	
	LINE_TOG6_MD	6	GPO6 line toggle mode enable.	
	LINE_TOG5_MD	5	GPO5 line toggle mode enable.	
	LINE_TOG4_MD	4	GPO4 line toggle mode enable.	
	LINE_TOG3_MD	3	GPO3 line toggle mode enable.	
	LINE_TOG2_MD	2	GPO2 line toggle mode enable.	
	LINE_TOG1_MD	1	GPO1 line toggle mode enable.	
	LINE_TOG0_MD	0	GPO0 line toggle mode enable.	
72h (30E5h)	REG30E5	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	LINE_TOGD_MD	5	GPOD line toggle mode enable.	
	LINE_TOGC_MD	4	GPOC line toggle mode enable.	
	LINE_TOGB_MD	3	GPOB line toggle mode enable.	
	LINE_TOGA_MD	2	GPOA line toggle mode enable.	
	LINE_TOG9_MD	1	GPO9 line toggle mode enable.	
	LINE_TOG8_MD	0	GPO8 line toggle mode enable.	
73h (30E6h)	REG30E6	7:0	Default : 0x00	Access : R/W
	FIRST_2H7_MD	7	GPO7 first 2H mode enable.	
	FIRST_2H6_MD	6	GPO6 first 2H mode enable.	
	FIRST_2H5_MD	5	GPO5 first 2H mode enable.	
	FIRST_2H4_MD	4	GPO4 first 2H mode enable.	
	FIRST_2H3_MD	3	GPO3 first 2H mode enable.	
	FIRST_2H2_MD	2	GPO2 first 2H mode enable.	
	FIRST_2H1_MD	1	GPO1 first 2H mode enable.	
	FIRST_2H0_MD	0	GPO0 first 2H mode enable.	
73h (30E7h)	REG30E7	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	FIRST_2HD_MD	5	GPOD first 2H mode enable.	

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description
	FIRST_2HC_MD	4	GPOC first 2H mode enable.
	FIRST_2HB_MD	3	GPOB first 2H mode enable.
	FIRST_2HA_MD	2	GPOA first 2H mode enable.
	FIRST_2H9_MD	1	GPO9 first 2H mode enable.
	FIRST_2H8_MD	0	GPO8 first 2H mode enable.
74h (30E8h)	REG30E8	7:0	Default : 0x00 Access : R/W
	GPO7_PUA	7	GPO7 pua.
	GPO6_PUA	6	GPO6 pua.
	GPO5_PUA	5	GPO5 pua.
	GPO4_PUA	4	GPO4 pua.
	GPO3_PUA	3	GPO3 pua.
	GPO2_PUA	2	GPO2 pua.
	GPO1_PUA	1	GPO1 pua.
	GPO0_PUA	0	GPO0 pua.
74h (30E9h)	REG30E9	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	GPOD_PUA	5	GPOD pua.
	GPOC_PUA	4	GPOC pua.
	GPOB_PUA	3	GPOB pua.
	GPOA_PUA	2	GPOA pua.
	GPO9_PUA	1	GPO9 pua.
	GPO8_PUA	0	GPO8 pua.
75h (30EAh)	REG30EA	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	TCON_TYPE[2:0]	5:3	Tcon type. 0: Normal. 1: LTD. 2: GIP.
	TCON_GRP2_CLK_GATE_EN	2	Enable gate of tcon group 2.
	TCON_GRP1_CLK_GATE_EN	1	Enable gate of tcon group 1.
	TCON_GRP0_CLK_GATE_EN	0	Enable gate of tcon group 0.
76h (30ECh)	REG30EC	7:0	Default : 0x00 Access : R/W
	GPO_STH_SEL3[1:0]	7:6	Gpo3 sth pulse width select.

DISP_TC Register (Bank = 30)

Index (Absolute)	Mnemonic	Bit	Description	
	GPO_STH_SEL2[1:0]	5:4	Gpo2 sth pulse width select.	
	GPO_STH_SEL1[1:0]	3:2	Gpo1 sth pulse width select.	
	GPO_STH_SEL0[1:0]	1:0	Gpo0 sth pulse width select. 00: 1T. 01: 1T negative sample. 10: 1.5T. 11: 1.5T negative sample.	
	76h (30EDh)	REG30ED	7:0	Default : 0x00
	GPO_STH_SEL7[1:0]	7:6	Gpo7 sth pulse width select.	
	GPO_STH_SEL6[1:0]	5:4	Gpo6 sth pulse width select.	
	GPO_STH_SEL5[1:0]	3:2	Gpo5 sth pulse width select.	
	GPO_STH_SEL4[1:0]	1:0	Gpo4 sth pulse width select.	
	77h (30EEh)	REG30EE	7:0	Default : 0x00
	GPO_STH_SELB[1:0]	7:6	Gpob sth pulse width select.	
	GPO_STH_SELA[1:0]	5:4	Gpoa sth pulse width select.	
	GPO_STH_SEL9[1:0]	3:2	Gpo9 sth pulse width select.	
	GPO_STH_SEL8[1:0]	1:0	Gpo8 sth pulse width select.	
	77h (30EFh)	REG30EF	7:0	Default : 0x00
	-	7:4	Reserved.	
	GPO_STH_SELD[1:0]	3:2	Gpod sth pulse width select.	
	GPO_STH_SELC[1:0]	1:0	Gpoc sth pulse width select.	
	79h (30F2h)	REG30F2	7:0	Default : 0x00
	G7AT	7	G7AT.	
	G6AT	6	G6AT.	
	G5AT	5	G5AT.	
	G4AT	4	G4AT.	
	G3AT	3	G3AT.	
	G2AT	2	G2AT.	
	G1AT	1	G1AT.	
	G0AT	0	G0AT.	
	79h (30F3h)	REG30F3	7:0	Default : 0x00
	-	7:6	Reserved.	
	GDAT	5	GDAT.	

DISP_TC Register (Bank = 30)				
Index (Absolute)	Mnemonic	Bit	Description	
	GCAT	4	GCAT.	
	GBAT	3	GBAT.	
	GAAT	2	GAAT.	
	G9AT	1	G9AT.	
	G8AT	0	G8AT.	
7Ah (30F4h)	REG30F4	7:0	Default : 0x00	Access : R/W
	MINI_GPO_OEN[7:0]	7:0	GPO OEN of mini-LVDS.	
7Ah (30F5h)	REG30F5	7:0	Default : 0x00	Access : R/W
	MINI_GPO[7:0]	7:0	GPO of mini -LVDS.	
7Eh (30FCh)	REG30FC	7:0	Default : 0x00	Access : R/W
	TC_DUMMY0[7:0]	7:0	TCON dummy register 0.	
7Eh (30FDh)	REG30FD	7:0	Default : 0x00	Access : R/W
	TC_DUMMY0[15:8]	7:0	See description of '30FCh'.	
7Fh (30FEh)	REG30FE	7:0	Default : 0xFF	Access : R/W
	TC_DUMMY1[7:0]	7:0	TCON dummy register 1.	
7Fh (30FFh)	REG30FF	7:0	Default : 0xFF	Access : R/W
	TC_DUMMY1[15:8]	7:0	See description of '30FEh'.	

LPLL_REG Register (Bank = 31)

LPLL_REG Register (Bank = 31)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3100h)	REG3100	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	LPLL_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control:. 00: /1. 01: /2. 10: /4. 11: /8.	
00h (3101h)	REG3101	7:0	Default : 0x00	Access : R/W
	LPLL_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N). 0: Divide 1 . 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4&.	
01h (3102h)	REG3102	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	LPLL_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control:. 00: /1. 01: /2. 10: /4. 11: /8.	
01h (3103h)	REG3103	7:0	Default : 0x01	Access : R/W
	LPLL_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio=(1/N). Default ratio=8. 0: Divide 1 . 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4&.	
02h (3104h)	REG3104	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	LPLL_EN_DCCM	2	Enable duty cycle correction for divider M, high active.	
	LPLL_EN_DCCN	1	Enable duty cycle correction for divider N, high active.	
	LPLL_EN_MINILVDS	0	Enable mini-LVDS control, high active.	
02h	REG3105	7:0	Default : 0x22	Access : R/W

LPLL_REG Register (Bank = 31)				
Index (Absolute)	Mnemonic	Bit	Description	
(3105h)	LPLL_DIVM_S[3:0]	7:4	Divider M ratio control. 0010: Div1. 0011: Div1p5. 0100: Div2. 0101: Div2p5. 0110: Div3. 0111: Div3p5. 1000: Div4. 1001: Div4p5. 1010: Div5. 1100: Div6. others: Power down.	
	LPLL_DIVN_S[3:0]	3:0	Divider N ratio control. 0010: Div1. 0011: Div1p5. 0100: Div2. 0101: Div2p5. 0110: Div3. 0111: Div3p5. 1000: Div4. 1001: Div4p5. 1010: Div5. 1100: Div6. others: Power down.	
03h (3106h)	REG3106	7:0	Default : 0x23	Access : R/W
	LPLL_MODE	7	LPLL_MDE. 0: Single mode. 1: Dual mode.	
	LPLL_TYPE	6	LPLL_TYPE. 0: LVDS mode. 1: RSDS mode.	
	LPLL_PD	5	Power down control to PLL (active high).	
	LPLL_RESET	4	Reset digital circuit in LPLL.	
	LPLL_VCO_OFFSET	3	Enable VCO free running (active low).	
	LPLL_ICTRL[2:0]	2:0	Charge pump current control register.	
03h (3107h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
04h	REG3108	7:0	Default : 0x00	Access : RO

LPLL_REG Register (Bank = 31)				
Index (Absolute)	Mnemonic	Bit	Description	
(3108h)	-	7:2	Reserved.	
	HIGH_FLAG	1	Output flag for vco supply voltage too high (need monitor for mass production).	
	LOCK	0	PLL LOCK Flag.	
05h (310Ah)	REG310A	7:0	Default : 0x22	Access : R/W
	PRD_LOCK_THRESH[3:0]	7:4	Prd lock thresh.	
	PRD_STABLE_THRESH[3:0]	3:0	Clock stable thresh.	
05h (310Bh)	REG310B	7:0	Default : 0x02	Access : R/W
	PHASE_LOCK_THRESH[7:0]	7:0	Phase lock thresh.	
06h (310Ch)	REG310C	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7[7:0]	7:0	Limit for clock freq correction modification.	
06h (310Dh)	REG310D	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7[15:8]	7:0	See description of '310Ch'.	
07h (310Eh)	REG310E	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7[23:16]	7:0	See description of '310Ch'.	
08h (3110h)	REG3110	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7_RK[7:0]	7:0	Limit for phase correction modification.	
08h (3111h)	REG3111	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7_RK[15:8]	7:0	See description of '3110h'.	
09h (3112h)	REG3112	7:0	Default : 0x00	Access : R/W
	LIMIT_D5D6D7_RK[23:16]	7:0	See description of '3110h'.	
0Ah (3114h)	REG3114	7:0	Default : 0x00	Access : R/W
	LIMIT_LPLL_OFFSET[7:0]	7:0	Limit for LPLL phase offset.	
0Ah (3115h)	REG3115	7:0	Default : 0x00	Access : R/W
	LIMIT_LPLL_OFFSET[15:8]	7:0	See description of '3114h'.	
0Bh (3116h)	REG3116	7:0	Default : 0x10	Access : R/W
	P_GAIN_PRD[3:0]	7:4	P_gain for prd_lock, gain setting is same as i_gain_prd.	
	I_GAIN_PRD[3:0]	3:0	I_gain for prd lock. 0: >> 5. 1: >> 4. 2: >> 3. 3: >> 2. 4: >> 1. 5: Same.	

LPLL_REG Register (Bank = 31)

Index (Absolute)	Mnemonic	Bit	Description
			6: << 1. 7: << 2. 8: << 3. 9: << 4. 10: << 5. 11: << 6. 12: << 7. 13: << 8. 14: << 9. 15: << 10.
0Bh (3117h)	REG3117	7:0	Default : 0x10
	P_GAIN_PHASE[3:0]	7:4	P_gain for phase lock, gain setting is same as i_gain_prd.
	I_GAIN_PHASE[3:0]	3:0	I_gain for phase lock, game setting is same as i_gain_prd.
0Ch (3118h)	REG3118	7:0	Default : 0x00
	P_GAIN_PHASE_ZERO	7	Disable p_gain for lock phase.
	I_GAIN_PHASE_ZERO	6	Disable i_gain for lock phase.
	P_GAIN_PRD_ZERO	5	Disable p_gain for lock prd.
	I_GAIN_PRD_ZERO	4	Disable i_gain for lock prd.
	FRAME_LPLL_EN	3	Frame LPLL enable.
	-	2	Reserved.
0Ch (3119h)	REG3119	7:0	Default : 0x00
	OVS_FRAME_DIV[3:0]	7:4	Output fame div for frame sync.
	IVS_FRAME_DIV[3:0]	3:0	Input frame div for frame sync.
0Dh (311Ah)	REG311A	7:0	Default : 0x00
	-	7:4	Reserved.
	FORCE_PHASE_CLOSE_DONE	3	S.W. Force phase close done.
	FORCE_PHASE_REDUCE_DONE	2	S.W. Force phase reduce done.
	FORCE_PRD_LOCK_DONE	1	S.W. Force prd lock done.

LPLL_REG Register (Bank = 31)				
Index (Absolute)	Mnemonic	Bit	Description	
	FORCE_PRD_STABLE	0	S.W. Force prd stable check ok.	
0Dh (311Bh)	REG311B	7:0	Default : 0x03	Access : R/W
	-	7:4	Reserved.	
	SSC_EN	3	SSC mode enable.	
	PRD_SEL_ORI_VS	2	Select ori ovs as lock prd reference.	
	NON_STABLE_EN	1	Frame PLL disable when non_stable flag high.	
	NO_SIGNAL_EN	0	Frame PLL disable when no_signal flag high.	
0Fh (311Eh)	REG311E	7:0	Default : 0x44	Access : R/W
	LPLL_SET[7:0]	7:0	PLL initial setting value.	
0Fh (311Fh)	REG311F	7:0	Default : 0x55	Access : R/W
	LPLL_SET[15:8]	7:0	See description of '311Eh'.	
10h (3120h)	REG3120	7:0	Default : 0x22	Access : R/W
	LPLL_SET[23:16]	7:0	See description of '311Eh'.	
11h (3122h)	REG3122	7:0	Default : 0x00	Access : RO
	PHASE_DIF[7:0]	7:0	Phase dif value.	
11h (3123h)	REG3123	7:0	Default : 0x00	Access : RO
	PHASE_DIF[15:8]	7:0	See description of '3122h'.	
12h (3124h)	REG3124	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	PHASE_UP	0	Ovs leading or lagging related to ivs. 0: Leading. 1: Lagging.	
13h (3126h)	REG3126	7:0	Default : 0x00	Access : RO
	PRD_DIF[7:0]	7:0	Reference signal prd difference value.	
13h (3127h)	REG3127	7:0	Default : 0x00	Access : RO
	PRD_DIF[15:8]	7:0	See description of '3126h'.	
14h (3128h)	REG3128	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	PRD_UP	0	Ovs prd related to ivs prd. 0: Faster. 1: Slower.	
16h ~ 16h (312Ch ~	-	7:0	Default : -	Access : -
	-	-	Reserved.	

LPLL_REG Register (Bank = 31)

Index (Absolute)	Mnemonic	Bit	Description
312Dh)			
17h (312Eh)	REG312E	7:0	Default : 0x20
	LPLL_STEP[7:0]	7:0	Output PLL spread spectrum step.
17h (312Fh)	REG312F	7:0	Default : 0x00
	-	7:2	Reserved.
	LPLL_STEP[9:8]	1:0	See description of '312Eh'.
18h (3130h)	REG3130	7:0	Default : 0x00
	LPLL_SPAN[7:0]	7:0	Output PLL spread spectrum span.
18h (3131h)	REG3131	7:0	Default : 0x00
	-	7:6	Reserved.
	LPLL_SPAN[13:8]	5:0	See description of '3130h'.
19h (3132h)	REG3132	7:0	Default : 0x00
	IDCLK_DIV[7:0]	7:0	Input clock divider for prd sync.
19h (3133h)	REG3133	7:0	Default : 0x00
	IDCLK_DIV[15:8]	7:0	See description of '3132h'.
1Ah (3134h)	REG3134	7:0	Default : 0x00
	IDCLK_DIV[23:16]	7:0	See description of '3132h'.
1Bh (3136h)	REG3136	7:0	Default : 0x00
	ODCLK_DIV[7:0]	7:0	Output dlock divider for prd sync.
1Bh (3137h)	REG3137	7:0	Default : 0x00
	ODCLK_DIV[15:8]	7:0	See description of '3136h'.
1Ch (3138h)	REG3138	7:0	Default : 0x00
	ODCLK_DIV[23:16]	7:0	See description of '3136h'.
1Dh (313Ah)	REG313A	7:0	Default : 0x00
	DEC_V_LIMIT[7:0]	7:0	Reduce phase error by reduce v_total limit. This setting is effective when reg_fix_dec_en is 1.
1Dh (313Bh)	REG313B	7:0	Default : 0x00
	FIX_DEC_EN	7	Enable reduce phase error by reduce v_total.
	-	6:3	Reserved.
	DEC_V_LIMIT[10:8]	2:0	See description of '313Ah'.
1Eh (313Ch)	REG313C	7:0	Default : 0x00
	INC_V_LIMIT[7:0]	7:0	Reduce phase error by increasing v_total limit.
1Eh	REG313D	7:0	Default : 0x00
			Access : R/W

LPLL_REG Register (Bank = 31)				
Index (Absolute)	Mnemonic	Bit	Description	
(313Dh)	-	7:3	Reserved.	
	INC_V_LIMIT[10:8]	2:0	See description of '313Ch'.	
1Fh (313Eh)	REG313E	7:0	Default : 0x80	Access : R/W
	PHASE_CLOSE_PHASE[7:0]	7:0	Phase reduce done thresh.	
1Fh (313Fh)	REG313F	7:0	Default : 0x30	Access : R/W
	REDUCE_DONE_THRESH[3:0]	7:4	Phase close done thresh.	
	PHASE_CLOSE_PHASE[11:8]	3:0	See description of '313Eh'.	
20h (3140h)	REG3140	7:0	Default : 0x52	Access : R/W
	-	7	Reserved.	
	HIS_CNT_HIGH_THRESH[2:0]	6:4	History counter high thresh.	
	-	3	Reserved.	
	HIS_CNT_LOW_THRESH[2:0]	2:0	History counter low thresh.	
21h (3142h)	REG3142	7:0	Default : 0x00	Access : RO
	IVS_PRD_VALUE[7:0]	7:0	Ivs prd value.	
21h (3143h)	REG3143	7:0	Default : 0x00	Access : RO
	IVS_PRD_VALUE[15:8]	7:0	See description of '3142h'.	
22h (3144h)	REG3144	7:0	Default : 0x00	Access : RO
	IVS_PRD_VALUE[23:16]	7:0	See description of '3142h'.	
23h (3146h)	REG3146	7:0	Default : 0x00	Access : RO
	OVS_PRD_VALUE[7:0]	7:0	Ovs prd value.	
23h (3147h)	REG3147	7:0	Default : 0x00	Access : RO
	OVS_PRD_VALUE[15:8]	7:0	See description of '3146h'.	
24h (3148h)	REG3148	7:0	Default : 0x00	Access : RO
	OVS_PRD_VALUE[23:16]	7:0	See description of '3146h'.	
26h (314Ch)	REG314C	7:0	Default : 0x00	Access : RO
	FIX_V_TOTAL[7:0]	7:0	Reduce phase modify v_total value.	
26h (314Dh)	REG314D	7:0	Default : 0x00	Access : RO
	FIX_V_DEC	7	Reduce phase method. 0: Increasing v_total. 1: Decreasing v_total.	
	-	6:3	Reserved.	
	FIX_V_TOTAL[10:8]	2:0	See description of '314Ch'.	
27h	REG314E	7:0	Default : 0x00	Access : RO

LPLL_REG Register (Bank = 31)				
Index (Absolute)	Mnemonic	Bit	Description	
(314Eh)	FIX_H_TOTAL[7:0]	7:0	FIX_H_TOTAL value.	
27h (314Fh)	REG314F	7:0	Default : 0x00	Access : RO
	-	7:4	Reserved.	
	FIX_H_TOTAL[11:8]	3:0	See description of '314Eh'.	
28h (3150h)	REG3150	7:0	Default : 0x00	Access : RO
	PLL_SET_USING[7:0]	7:0	Pll_set value for using.	
28h (3151h)	REG3151	7:0	Default : 0x00	Access : RO
	PLL_SET_USING[15:8]	7:0	See description of '3150h'.	
29h (3152h)	REG3152	7:0	Default : 0x00	Access : RO
	PLL_SET_USING[23:16]	7:0	See description of '3150h'.	
2Ah (3154h)	REG3154	7:0	Default : 0x00	Access : RO
	PHASE_REDUCE_DONE	7	Phase reduce done flag.	
	PRD_LOCK_DONE	6	Prd lock done flag.	
	IVS_PRD_STABLE	5	Idclk stable flag.	
	OVS_PRD_STABLE	4	Odclk stable flag.	
	-	3	Reserved.	
	CS_STATE[2:0]	2:0	Frame PLL FSM state. 3'h0: free run. 3'h1: lock_freq. 3'h2: reduce_phase. 3'h3: wait phase_close. 3'h4: lock_phase. others: Reserved.	
2Ah (3155h)	REG3155	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	PHASE_LOCK_DONE	0	Phase lock done flag.	
40h (3180h)	REG3180	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	SC_SSC_EN	0	SSC Engine Enable 1: Enable.	
41h (3182h)	REG3182	7:0	Default : 0x00	Access : R/W
	SSC_SET[7:0]	7:0	Fine tune frequency as ddfs. format: Xxx.xxxxxxx (3.7). formula: Fout = fin/SSC_SET. note: Write low byte first.	

LPLL_REG Register (Bank = 31)				
Index (Absolute)	Mnemonic	Bit	Description	
41h (3183h)	REG3183	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	SSC_SET[9:8]	1:0	See description of '3182h'.	
42h (3184h)	REG3184	7:0	Default : 0x00	Access : R/W
	SSC_STEP[7:0]	7:0	SSC step.	
43h (3186h)	REG3186	7:0	Default : 0x00	Access : R/W
	SSC_SPAN[7:0]	7:0	SSC span.	
43h (3187h)	REG3187	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SSC_SPAN[9:8]	1:0	See description of '3186h'.	
44h (3188h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
50h (31A0h)	REG31A0	7:0	Default : 0x00	Access : R/W
	AUPLL_PD	7	Power down control to PLL (Active High).	
	AUPLL_PORST	6	Power on reset signal to discharge loop filter voltage (High active).	
	AUPLL_RESET	5	Reset digital circuit flip flop.	
	AUPLL_VCO_OFFSET	4	Enable VCO free running; (active low).	
	-	3	Reserved.	
	AUPLL_RESETP	2	Reset post counter.	
	AUPLL_RESETF	1	Reset feedback counter.	
	AUPLL_RESETI	0	Reset input counter.	
50h (31A1h)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
51h (31A2h)	REG31A2	7:0	Default : 0x33	Access : R/W
	AUPLL_FBDIV[3:0]	7:4	First feedback divider register control 0000:/16(NA) ; 0001:/17(NA); 0010:/2 0011:/3 & 1111:/15 (divide N).	
	AUPLL_DDIV[3:0]	3:0	First input divider register control 0000:/16 (NA); 0001:/17(NA); 0010:/2 0011:/3 & 1111:/15 (divide N).	
52h (31A4h)	REG31A4	7:0	Default : 0x10	Access : R/W
	AUPLL_KM[3:0]	7:4	Second feedback divider register control 0000:/1 ; 0001:/2; 0010:/4 0011:/8 & 0111:/128; 1000:/256; 1001/256; &1111/256 (divide 2^N).	
	-	3:2	Reserved.	

LPLL_REG Register (Bank = 31)

Index (Absolute)	Mnemonic	Bit	Description
	AUPLL_KN[1:0]	1:0	Second input divider register control 00:/1; 01:/2; 10:/4; 11:/4.
52h (31A5h)	REG31A5	7:0	Default : 0x00
	-	7:4	Reserved.
	AUPLL_KP[3:0]	3:0	Post divider register control 0000:/1 ; 0001:/2; 0010:/4 0011:/8 & 0111:/128; 1000:/256; 1001/512; 1010:/1024; &1111/1024 (divide 2 ^N).
53h (31A6h)	REG31A6	7:0	Default : 0x11
	-	7	Reserved.
	AUPLL_RCTRL[2:0]	6:4	Loop Filter Resistor Setting; Default value=26.4K; 000:23.1K; 001:26.4K; 010:29.7; &111:42.9K.
	-	3	Reserved.
	AUPLL_ICTRL[2:0]	2:0	Charge pump current control register; Default=001, ICP=1.29uA; 000:0.65uA; 010:1.935uA; 011:2.58uA;100:3.225uA;101:3.87uA;110:5.16uA;111:10.32uA.
54h (31A8h)	REG31A8	7:0	Default : 0x00
	AUPLL_TEST[7:0]	7:0	Test mode configuration.

MOD Register (Bank = 32, Sub-Bank = 00)

MOD Register (Bank = 32, Sub-Bank = 00)				
Index (Absolute)	Mnemonic	Bit	Description	
01h ~ 07h (3203h ~ 320Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
20h (3241h)	REG3241	7:0	Default : 0x11	Access : R/W
	CKG_DOT_MINI_PRE[3:0]	7:4	Clock gen register of clk_dot_mini_pre. Bit[0]: gating. Bit[1]: invert. Bit[3:2]: 00, clk_lpll_buf. 01, clk_fifo_clk_buf.	
	CKG_DOT_MINI[3:0]	3:0	Clock gen register of clk_dot_mini. Bit[0]: gating. Bit[1]: invert. Bit[3:2]: 00, clk_lpll_buf. 01, clk_fifo_clk_buf.	
21h (3242h)	REG3242	7:0	Default : 0x00	Access : R/W
	WD_DIV3[7:0]	7:0	Blank width/3 for TRD.	
21h (3243h)	REG3243	7:0	Default : 0x00	Access : R/W
	EN_FMT_TRD	7	Enable TRD format output.	
	REF_SEL	6	Sync reference signal select 0:/3 1:org.	
	-	5:2	Reserved.	
	WD_DIV3[9:8]	1:0	See description of '3242h'.	
22h (3244h)	REG3244	7:0	Default : 0x00	Access : R/W
	HBK[7:0]	7:0	H blank width for TRD.	
22h (3245h)	REG3245	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	HBK[9:8]	1:0	See description of '3244h'.	
23h (3246h)	REG3246	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	OUTPUT_CONF_51_48[3:0]	3:0	Output configure for 18-pair output. 00: TTL. 01: LVDS/RSDS/mini-LVDS data differential pair. 10: Mini-LVDS clock output. 11: RSDS clock output.	
23h	REG3247	7:0	Default : 0x00	Access : R/W

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
(3247h)	GCR_CH14_19_RSCK_SKEWEN	7	Enable RSDS clock output skew adjust for ch14_19.
	GCR_CH14_19_RSCK_SKEW[1:0]	6:5	RSDS clock output skew adjust for ch14_19 when enabled. 00: 0.09ns. 01: 0.27ns. 10: 0.45ns. 11: 0.63ns.
	GCR_CH20_25_RSCK_SKEWEN	4	Enable RSDS clock output skew adjust for ch20_25.
	GCR_CH20_25_RSCK_SKEW[1:0]	3:2	RSDS clock output skew adjust for ch20_25 when enabled. 00: 0.09ns. 01: 0.27ns. 10: 0.45ns. 11: 0.63ns.
	-	1:0	Reserved.
24h (3248h)	REG3248	7:0	Default : 0x00
	EXT_DATA_EN_51_36[7:0]	7:0	EXT_DATA_EN[51: 36].
24h (3249h)	REG3249	7:0	Default : 0x00
	EXT_DATA_EN_51_36[15:8]	7:0	See description of '3248h'.
25h (324Ah)	REG324A	7:0	Default : 0x00
	GPO_SEL_51_36[7:0]	7:0	REG_GPO_SEL[51:36].
25h (324Bh)	REG324B	7:0	Default : 0x00
	GPO_SEL_51_36[15:8]	7:0	See description of '324Ah'.
26h (324Ch)	REG324C	7:0	Default : 0x00
	GPO_DATAIN_51_36[7:0]	7:0	REG_GPO_DATAIN[51:36].
26h (324Dh)	REG324D	7:0	Default : 0x00
	GPO_DATAIN_51_36[15:8]	7:0	See description of '324Ch'.
27h (324Eh)	REG324E	7:0	Default : 0x00
	GPO_OEZ_51_36[7:0]	7:0	REG_GPO_OEZ[51:36].
27h (324Fh)	REG324F	7:0	Default : 0x00
	GPO_OEZ_51_36[15:8]	7:0	See description of '324Eh'.
28h (3250h)	REG3250	7:0	Default : 0x00
	MOD_GPI_51_36[7:0]	7:0	General purpose input.
28h (3251h)	REG3251	7:0	Default : 0x00
	MOD_GPI_51_36[15:8]	7:0	See description of '3250h'.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
30h (3260h)	REG3260	7:0	Default : 0x01 Access : R/W
	DLY_VS_REF[7:0]	7:0	Dly value set for mft vsync reference to tcon.
30h (3261h)	REG3261	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	DLY_VS_REF[11:8]	3:0	See description of '3260h'.
31h (3262h)	REG3262	7:0	Default : 0x01 Access : R/W
	DLY_HS_REF[7:0]	7:0	Dly value set for mft hsync reference to tcon.
31h (3263h)	REG3263	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	DLY_HS_REF[11:8]	3:0	See description of '3262h'.
32h (3264h)	REG3264	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	MINI_CLK_GATE_EN	1	Gate mini fifo clk enable.
	MOD_CLK_GATE_EN	0	Gate mod clk enable.
37h (326Eh)	REG326E	7:0	Default : 0x00 Access : R/W
	GCR_TST_VDB[1:0]	7:6	Tst vdb.
	GCR_CLK_VDB	5	Clk vdb.
	GCR_PRE_TCTRL	4	Pre ctrl.
	-	3:0	Reserved.
37h (326Fh)	REG326F	7:0	Default : 0x01 Access : R/W
	-	7:2	Reserved.
	GCR_EN_RINT	1	Enable rint.
	GCR_PD_VDB	0	Opd vdb.
38h (3270h)	REG3270	7:0	Default : 0x00 Access : R/W
	TTL_TEST_DATA[7:0]	7:0	Test data for all ttl pin.
38h (3271h)	REG3271	7:0	Default : 0x00 Access : R/W
	TTL_TEST_DATA[15:8]	7:0	See description of '3270h'.
39h (3272h)	REG3272	7:0	Default : 0x00 Access : R/W
	TTL_TEST_DATA[23:16]	7:0	See description of '3270h'.
39h (3273h)	REG3273	7:0	Default : 0x00 Access : R/W
	TTL_TEST_DATA[31:24]	7:0	See description of '3270h'.
3Ah (3274h)	REG3274	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
	TTL_TEST_EN	5	Enable ttl pin test.
	TTL_TEST_CTRL	4	Test ctrl by registers.
	TTL_TEST_DATA[35:32]	3:0	See description of '3270h'.
40h (3280h)	REG3280	7:0	Default : 0x08 Access : R/W
	LVDS_OSD_A	7	Lvds osd enable for Channel A.
	CH_SWAP	6	Channel swapping.
	CH_POLARITY	5	Channel polarity.
	LVDS_PLASMA_A	4	LVDS_PLASMA for Channel A.
	PDP_10BIT	3	PDP_10BIT.
	LVDS_TI	2	LVDS_TI.
	-	1	Reserved.
	CLKB	0	CLKB.
40h (3281h)	REG3281	7:0	Default : 0x00 Access : R/W
	ECLKDLYSEL[3:0]	7:4	ECLKDLYSEL.
	CLKDLYSEL[3:0]	3:0	Clock delay.
41h (3282h)	-	7:0	Default : - Access : -
	-	-	Reserved.
41h (3283h)	REG3283	7:0	Default : 0x00 Access : R/W
	PDP_MASK_EN_A	7	PDP_MASK_EN DE channel A.
	PDP_MASK_SET_A	6	PDP_MASK_SET DE channel A.
	PDP_CH3_EN_A	5	PDP_CH3_EN channel A.
	PDP_CH3_SET_A	4	PDP_CH3_SET channel A.
	PDP_CH4_EN_A	3	PDP_CH4_EN channel A.
	PDP_CH4_SET_A	2	PDP_CH4_SET for channel A.
	SKEW[1:0]	1:0	ODD Red TTL data SKEW.
42h (3284h)	REG3284	7:0	Default : 0x00 Access : R/W
	SHIFT_LVDS_PAIR[1:0]	7:6	Shift lvds pair 1 pair space.
	PDP_10BIT_MOR[1:0]	5:4	Mode pdp 10bit mode.
	-	3	Reserved.
	EN_VS_ON_OSD	2	Vsync on osd enable.
	PAIR_SWAP_MOR[1:0]	1:0	More pair swap.
42h (3285h)	REG3285	7:0	Default : 0x10 Access : R/W
	OSD_DE_INV	7	Inverse OSD DE.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description	
	OSD_ON_DE_B	6	PDP osd de on DE channel B.	
	OSD_ON_DE_A	5	PDP osd de on DE channel A.	
	SW_RST	4	Software reset.	
	LVDS_OSD_B	3	Lvds osd enable for Channel B.	
	LVDS_PLASMA_B	2	LVDS_PLASMA for Channel B.	
	EN_TEST_LVDS	1	Enable test path to lvds output.	
	EN_MORE_PAIR_SWAP	0	Enable more pair swap.	
43h (3286h)	REG3286	7:0	Default : 0xC6	Access : R/W
	LVDS_CLOCK_PHASE[6:0]	7:1	Clock phase could be set by register.	
	-	0	Reserved.	
43h (3287h)	REG3287	7:0	Default : 0x00	Access : R/W
	PDP_MASK_EN_B	7	PDP_MASK_EN DE channel B.	
	PDP_MASK_SET_B	6	PDP_MASK_SET DE channel B.	
	PDP_CH3_EN_B	5	PDP_CH3_EN channel B.	
	PDP_CH3_SET_B	4	PDP_CH3_SET channel B.	
	PDP_CH4_EN_B	3	PDP_CH4_EN channel B.	
	PDP_CH4_SET_B	2	PDP_CH4_SET for channel B.	
	-	1:0	Reserved.	
44h (3288h)	REG3288	7:0	Default : 0x00	Access : R/W
	SKEW_OTHER[7:0]	7:0	Ttl skew for others. [1:0]: ODD Green. [3:2]: ODD Blue. [5:4]: EVEN Red. [7:6]: EVEN Green. [9:8]: EVEN Blue.	
44h (3289h)	REG3289	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	SKEW_OTHER[9:8]	1:0	See description of '3288h'.	
45h (328Ah)	REG328A	7:0	Default : 0x3F	Access : R/W
	BOUND_RS_DS	7	Bond RS_DS.	
	-	6	Reserved.	
	LVDS_LA_OEZ	5	LVDS_LA_OEZ.	
	LVDS_LB_OEZ	4	LVDS_LB_OEZ.	
	CK_OEZ	3	TTL-CK_OEZ.	

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
	DE_OEZ	2	TTL-DE_OEZ.
	HS_OEZ	1	TTL-HS_OEZ.
	VS_OEZ	0	TTL-VS_OEZ.
45h (328Bh)	REG328B	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	BOUNDING	1	Bonding.
	BOUND_MINI	0	Bond mini.
46h (328Ch)	REG328C	7:0	Default : 0x00 Access : R/W
	EXT_DATA_EN[7:0]	7:0	EXT_DATA_EN[31:0].
46h (328Dh)	REG328D	7:0	Default : 0x00 Access : R/W
	EXT_DATA_EN[15:8]	7:0	See description of '328Ch'.
47h (328Eh)	REG328E	7:0	Default : 0x00 Access : R/W
	EXT_DATA_EN[23:16]	7:0	See description of '328Ch'.
47h (328Fh)	REG328F	7:0	Default : 0x00 Access : R/W
	EXT_DATA_EN[31:24]	7:0	See description of '328Ch'.
48h (3291h)	-	7:0	Default : - Access : -
	-	-	Reserved.
49h (3292h)	REG3292	7:0	Default : 0x00 Access : R/W
	MLX_METHOD[1:0]	7:6	Output format selection. 10: 8-bit. 01: 6-bit. Other: 10-bit.
	ERGX	5	Even channel red and green channel swap.
	EGBX	4	Even channel green and blue channel swap.
	ORGX	3	Odd channel red and green channel swap.
	OGBX	2	Odd channel green and blue channel swap.
	FRONT_BACK	1	FRONT_BACK.
	INTERLACE_OUT	0	Interlace output.
49h (3293h)	REG3293	7:0	Default : 0x00 Access : R/W
	GATE_DE	7	Output de gating.
	EMLX	6	Even LSB and MSB swapping.
	ERBX	5	Even channel red and blue channel swap.
	OMLX	4	Odd LSB and MSB swapping.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
	ORBX	3	Odd channel red and blue channel swap.
	OBX	2	Reserved.
	WDG	1	Blanking time data become all 1.
	REVL	0	Reverse output pix.
4Ah (3294h)	REG3294	7:0	Default : 0x00 Access : R/W
	SVM_HALF_STEP	7	SVM half step.
	TTL_LVDS	6	TTL dual clock output.
	CLKB_TC_REG	5	GPOA clock gating.
	CLK_INVERT	4	Output clock invert.
	VS_INVERT	3	Output Vsync invert.
	DE_INVERT	2	Output DE invert.
	DUALMODE	1	Dual channel selection.
	ABSWITCH	0	Odd -even channel switch.
4Ah (3295h)	REG3295	7:0	Default : 0x00 Access : R/W
	AUTOVS_EARLY	7	Auto Vsync early DE.
	INTER_HS	6	Interlace Hsync.
	INTERLACE_HS_GATE	5	Interlace Hsync gate.
	HS_INVERT	4	Hsync invert.
	HS_REMO	3	GPO or original Hsync selection.
	OCP	2	TC clock invert.
	ECP	1	TC clock invert.
	PUA	0	GPO gating.
4Bh (3296h)	REG3296	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	MASK_TTL_DUAL	2	Mask dual channel de output.
	TI_BITMODE[1:0]	1:0	TI bitmode. 0x: 10-bit. 10: 8-bit. 11: 6-bit.
4Ch (3298h)	REG3298	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	CHANNEL_SEL[2:0]	2:0	CRC testing channel selection.
4Dh	REG329A	7:0	Default : 0x00 Access : R/W

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
(329Ah)	GPO_SEL[7:0]	7:0	General purpose output[31:0].
4Dh (329Bh)	REG329B GPO_SEL[15:8]	7:0 7:0	Default : 0x00 See description of '329Ah'.
4Eh (329Ch)	REG329C GPO_SEL[23:16]	7:0 7:0	Default : 0x00 See description of '329Ah'.
4Eh (329Dh)	REG329D GPO_SEL[31:24]	7:0 7:0	Default : 0x00 See description of '329Ah'.
4Fh (329Eh)	REG329E GPO_DATAIN[7:0]	7:0 7:0	Default : 0x00 General purpose datain[31:0].
4Fh (329Fh)	REG329F GPO_DATAIN[15:8]	7:0 7:0	Default : 0x00 See description of '329Eh'.
50h (32A0h)	REG32A0 GPO_DATAIN[23:16]	7:0 7:0	Default : 0x00 See description of '329Eh'.
50h (32A1h)	REG32A1 GPO_DATAIN[31:24]	7:0 7:0	Default : 0x00 See description of '329Eh'.
51h (32A2h)	REG32A2 GPO_OEZ[7:0]	7:0 7:0	Default : 0x00 General purpose pad direction. 0: Output. 1: Input.
51h (32A3h)	REG32A3 GPO_OEZ[15:8]	7:0 7:0	Default : 0x00 See description of '32A2h'.
52h (32A4h)	REG32A4 GPO_OEZ[23:16]	7:0 7:0	Default : 0x00 See description of '32A2h'.
52h (32A5h)	REG32A5 GPO_OEZ[31:24]	7:0 7:0	Default : 0x00 See description of '32A2h'.
53h (32A6h)	REG32A6 -	7:0 7:1	Default : 0x00 Reserved.
	DISABLE_BOND_DHC	0	Bond REG_DHC_MODE to 01 (DHC_DDR output mode) disable. This bit is valid when IC bond for DHC. When BOND_DHC is true, this bit must be set to 0 to change REG_DHC_MODE.
53h (32A7h)	REG32A7 VBI_EN	7:0 7	Default : 0x00 Vbi information on lvs enable.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
	-	6:0	Reserved.
54h ~ 54h (32A8h ~ 32A9h)	-	7:0	Default : - Access : -
	-	-	Reserved.
55h (32AAh)	REG32AA	7:0	Default : 0x00 Access : RO
	MOD_GPI[7:0]	7:0	General purpose input.
55h (32ABh)	REG32AB	7:0	Default : 0x00 Access : RO
	MOD_GPI[15:8]	7:0	See description of '32AAh'.
56h (32ACh)	REG32AC	7:0	Default : 0x00 Access : RO
	MOD_GPI[23:16]	7:0	See description of '32AAh'.
56h (32ADh)	REG32AD	7:0	Default : 0x00 Access : RO
	MOD_GPI[31:24]	7:0	See description of '32AAh'.
57h (32AEh)	REG32AE	7:0	Default : 0x00 Access : R/W
	ATCON_OEN[7:0]	7:0	ATCON output enable.
57h (32AFh)	REG32AF	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	ATCON_OEN[14:8]	6:0	See description of '32AEh'.
58h (32B0h)	REG32B0	7:0	Default : 0x00 Access : R/W
	DTCON_OEN[7:0]	7:0	DTCON output enable.
58h (32B1h)	REG32B1	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	DTCON_OEN[9:8]	1:0	See description of '32B0h'.
59h (32B2h)	REG32B2	7:0	Default : 0x00 Access : R/W
	ATCON_SEL[3:0]	7:4	Selection ATCON pad.
	DTCON_SEL[3:0]	3:0	Selection DTCON pad.
59h (32B3h)	REG32B3	7:0	Default : 0x30 Access : R/W
	DHC_MODE_0	7	DHC mode selection.
	DHC_MODE_1	6	DHC mode selection.
	AHSYNC_OEN	5	Oen for ahsync.
	AVSYNC_OEN	4	Oen for avsync.
	PWM_SEL[3:0]	3:0	Selection PWM pad.
5Ah (32B4h)	REG32B4	7:0	Default : 0x30 Access : R/W
	SWAP_CHANNEL_R	7	Mini-LVDS settings.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
	SWAP_CHANNEL_L	6	Mini-LVDS settings.
	SWAP_PN_R	5	Mini-LVDS settings.
	SWAP_PN_L	4	Mini-LVDS settings.
	SWAP_ML_R	3	Mini-LVDS settings.
	SWAP_ML_L	2	Mini-LVDS settings.
	-	1:0	Reserved.
5Ah (32B5h)	REG32B5	7:0	Default : 0x01 Access : R/W
	-	7:5	Reserved.
	SWAP_RL	4	Mini-LVDS settings.
	ENDDATA	3	Mini-LVDS settings.
	TP_MOD	2	Mini-LVDS settings.
	-	1	Reserved.
	SOFT_RSTZ	0	Mini-LVDS settings.
5Bh (32B6h)	REG32B6	7:0	Default : 0x00 Access : R/W
	SWAP_ORDER_L[5:0]	7:2	Mini-LVDS settings.
	-	1:0	Reserved.
5Bh (32B7h)	REG32B7	7:0	Default : 0x00 Access : R/W
	SWAP_ORDER_R[5:0]	7:2	Mini-LVDS settings.
	-	1:0	Reserved.
5Ch (32B8h)	REG32B8	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CKDATA_ASSIGN[2:0]	4:2	Mini-LVDS settings.
	-	1:0	Reserved.
5Ch (32B9h)	REG32B9	7:0	Default : 0x1C Access : R/W
	MOD_MINI[2:0]	7:5	Mini-LVDS settings.
	DELAY_PROG[2:0]	4:2	Mini-LVDS settings.
	-	1:0	Reserved.
5Dh (32BAh)	REG32BA	7:0	Default : 0x00 Access : R/W
	LVD1_CHASSIGN[2:0]	7:5	Mini-LVDS settings.
	LVD2_CHASSIGN[2:0]	4:2	Mini-LVDS settings.
	-	1:0	Reserved.
5Dh (32BBh)	REG32BB	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
	LVD0_CHASSIGN[2:0]	2:0	Mini-LVDS settings.
5Eh (32BCh)	REG32BC	7:0	Default : 0x00 Access : R/W
	LVD4_CHASSIGN[2:0]	7:5	Mini-LVDS settings.
	LVD5_CHASSIGN[2:0]	4:2	Mini-LVDS settings.
	DELY_EN_INV	1	Mini-LVDS settings.
	-	0	Reserved.
5Eh (32BDh)	REG32BD	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	LVD3_CHASSIGN[2:0]	2:0	Mini-LVDS settings.
5Fh (32BEh)	REG32BE	7:0	Default : 0x18 Access : R/W
	TP1RISE_CNT[7:0]	7:0	Mini-LVDS settings.
60h (32C0h)	REG32C0	7:0	Default : 0xFF Access : R/W
	EN_MINI_RST_L[7:0]	7:0	Enable miniLVDS rst on data of channel L.
60h (32C1h)	REG32C1	7:0	Default : 0xFF Access : R/W
	EN_MINI_RST_R[7:0]	7:0	Enable miniLVDS rst on data of channel R.
6Ah ~ 6Ah (32D4h ~ 32D5h)	-	7:0	Default : - Access : -
	-	-	Reserved.
6Bh (32D6h)	REG32D6	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	LVD6_CHASSIGN[2:0]	5:3	Minilvds pair 6 assign.
	LVD7_CHASSIGN[2:0]	2:0	Minilvds pair 7 assign.
6Bh (32D7h)	REG32D7	7:0	Default : 0x00 Access : R/W
	LG_MINI_10BIT	7	Special 10 bit mini-LVDS mode enable.
	-	6:4	Reserved.
	SWAP_ORDER_UR[1:0]	3:2	Swap upper 2 bit of right.
	SWAP_ORDER_UL[1:0]	1:0	Swap upper 2 bit or left.
6Ch (32D9h)	REG32D9	7:0	Default : 0x00 Access : R/W
	TTL_10BIT	7	To support 10bit TTL output panel.
	-	6:0	Reserved.
6Dh (32DAh)	REG32DA	7:0	Default : 0x00 Access : R/W
	OUTPUT_CONF[7:0]	7:0	Output configure for 18-pair output. 00: TTL.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
			01: LVDS/RSDS/mini-LVDS data differential pair. 10: Mini-LVDS clock output. 11: RSDS clock output.
6Dh (32DBh)	REG32DB	7:0	Default : 0x00 Access : R/W
	OUTPUT_CONF[15:8]	7:0	See description of '32DAh'.
6Eh (32DCh)	REG32DC	7:0	Default : 0x00 Access : R/W
	OUTPUT_CONF[23:16]	7:0	See description of '32DAh'.
6Eh (32DDh)	REG32DD	7:0	Default : 0x00 Access : R/W
	OUTPUT_CONF[31:24]	7:0	See description of '32DAh'.
6Fh (32DEh)	REG32DE	7:0	Default : 0x00 Access : R/W
	OUTPUT_CONF[39:32]	7:0	See description of '32DAh'.
6Fh (32DFh)	REG32DF	7:0	Default : 0x00 Access : R/W
	OUTPUT_CONF[47:40]	7:0	See description of '32DAh'.
71h (32E2h)	REG32E2	7:0	Default : 0x00 Access : R/W
	GCR_PE_EN_CH[7:0]	7:0	Differential output pre-emphasis enable for channel [17:0].
71h (32E3h)	REG32E3	7:0	Default : 0x00 Access : R/W
	GCR_PE_EN_CH[15:8]	7:0	See description of '32E2h'.
72h (32E4h)	REG32E4	7:0	Default : 0x00 Access : R/W
	GCR_PE_EN_CH[23:16]	7:0	See description of '32E2h'.
72h (32E5h)	REG32E5	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	GCR_PE_EN_CH[25:24]	1:0	See description of '32E2h'.
73h (32E6h)	REG32E6	7:0	Default : 0x00 Access : R/W
	GCR_DS_POL_CH[7:0]	7:0	Differential output polarity swap for channel [25:0].
73h (32E7h)	REG32E7	7:0	Default : 0x00 Access : R/W
	GCR_DS_POL_CH[15:8]	7:0	See description of '32E6h'.
74h (32E8h)	REG32E8	7:0	Default : 0x00 Access : R/W
	GCR_DS_POL_CH[23:16]	7:0	See description of '32E6h'.
74h (32E9h)	REG32E9	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	GCR_DS_POL_CH[25:24]	1:0	See description of '32E6h'.
75h	REG32EA	7:0	Default : 0x00 Access : R/W

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
(32EAh)	GCR_DTG_RETIRE_CH[7:0]	7:0	Enable channel [25:0] DTG input retimed by RSDS clock in MOD for GPO in RSDS mode.
75h (32EBh)	REG32EB	7:0	Default : 0x00 Access : R/W
	GCR_DTG_RETIRE_CH[15:8]	7:0	See description of '32EAh'.
76h (32ECh)	REG32EC	7:0	Default : 0x00 Access : R/W
	GCR_DTG_RETIRE_CH[23:16]	7:0	See description of '32EAh'.
76h (32EDh)	REG32ED	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	GCR_DTG_RETIRE_CH[25:24]	1:0	See description of '32EAh'.
77h (32EEh)	REG32EE	7:0	Default : 0x00 Access : R/W
	GCR_CH2_7_RSCK_SKEW[0]	7	RSDS clock output skew adjust for ch6_11 when enabled. 00: 0.09ns. 01: 0.27ns. 10: 0.45ns. 11: 0.63ns.
	GCR_CH8_13_RSCK_SKEWEN	6	Enable RSDS clock output skew adjust for ch12_13.
	GCR_CH8_13_RSCK_SKEW[1:0]	5:4	RSDS clock output skew adjust for ch12_13 when enabled. 00: 0.09ns. 01: 0.27ns. 10: 0.45ns. 11: 0.63ns.
	-	3	Reserved.
	EN_PORTB_IB	2	Enable MOD differential output current for LVDS/RSDS/mini-LVDS mode for ch12~17.
	EN_PORTA_IB	1	Enable MOD differential output current for LVDS/RSDS/mini-LVDS mode for ch0~11.
	EN_CK	0	Enable MOD high speed clock toggling in LVDS/RSDS/mini-LVDS mode.
77h (32EFh)	REG32EF	7:0	Default : 0x00 Access : R/W
	GCR_VCOM	7	Differential output common mode voltage adjust. 0: 1.25V. 1: 0.94V.
	GCR_PE_ADJ[1:0]	6:5	Pre-emphasis level adjust. 00: Off. 01: 26mV.

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description	
			10: 52mV. 11: 76mV.	
	GCR_CH0_1_RSCK_SKEWEN	4	Enable RSDS clock output skew adjust for ch0_5.	
	GCR_CH0_1_RSCK_SKEW[1:0]	3:2	RSDS clock output skew adjust for ch0_5 when enabled. 00: 0.09ns. 01: 0.27ns. 10: 0.45ns. 11: 0.63ns.	
	GCR_CH2_7_RSCK_SKEWEN	1	Enable RSDS clock output skew adjust for ch6_11.	
	GCR_CH2_7_RSCK_SKEW[1]	0	See description of '32EEh'.	
	78h (32F0h)	REG32F0	7:0	Default : 0x47
	PDN_REGU	7	MOD regulator power down.	
	GCR_OUTSWING2X	6	Register to double differential output swing for LVDS/RSDS/mini-LVDS mode.	
	-	5:1	Reserved.	
	PD_MOD	0	Power down mod.	
	78h (32F1h)	-	7:0	Default : -
	-	-	Reserved.	
79h (32F2h)	REG32F2	7:0	Default : 0x00	Access : R/W
	HALFLINE[7:0]	7:0	Half line for MFT line buffer.	
79h (32F3h)	REG32F3	7:0	Default : 0x00	Access : R/W
	MFT_LB_EN	7	Enable MFT line buffer.	
	LTD	6	LTD mode.	
	REVERSE	5	REVERSE mode.	
	-	4	Reserved.	
	HALFLINE[11:8]	3:0	See description of '32F2h'.	
7Ah (32F4h)	REG32F4	7:0	Default : 0x00	Access : R/W
	SYNC_OUT_DLY_VA[7:0]	7:0	Line end sync output delay value.	
7Ah (32F5h)	REG32F5	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	SYNC_OUT_DLY_VA[11:8]	3:0	See description of '32F4h'.	
7Bh (32F6h)	REG32F6	7:0	Default : 0x00	Access : R/W
	RSDS_TCON_ST_DLY_VA[7:0]	7:0	RSDS TCON signal start delay value.	
7Bh	REG32F7	7:0	Default : 0x00	Access : R/W

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
(32F7h)	-	7:4	Reserved.
	RSDS_TCON_ST_DLY_VA[11:8]	3:0	See description of '32F6h'.
7Ch (32F8h)	REG32F8	7:0	Default : 0x00 Access : R/W
	MINI_CH_SWAP[1:0]	7:6	Mini-LVDS channel swap bit.
	LVDS_CH_SWAP[2:0]	5:3	LVDS channel swap bit.
	G_CLK_SWAP	2	RSDS CLK and green group swap bit.
	RSDS_BIT_SWAP	1	RSDS MSB LSB swap bit.
	HLOAD_SEL	0	Hload select to LPLL bit.
7Ch (32F9h)	REG32F9	7:0	Default : 0x00 Access : R/W
	FLIP_ENABLE	7	Flip enable.
	MSB_P	6	MSB_P.
	MSB_S	5	MSB_S.
	R_B_SWAP	4	R_B_SWAP.
	DATA_SWAP	3	DATA_SWAP.
	L_R_SWAP	2	L_R_SWAP.
	-	1	Reserved.
	MINI_CH_SWAP[2]	0	See description of '32F8h'.
7Dh (32FAh)	REG32FA	7:0	Default : 0x00 Access : R/W
	MOD_DUMMY[7]	7	Calibration enable.
	MOD_DUMMY[6]	6	Selfibg enable.
	MOD_DUMMY[5:0]	5:0	Ibcal.
7Dh (32FBh)	REG32FB	7:0	Default : 0x00 Access : R/W
	MOD_DUMMY[15]	7	inv_real_ltd.
	-	6:1	Reserved.
	MOD_DUMMY[8]	0	0x327f[0] data select 0: mod_gpi[32] 1: c_dda_out
7Eh (32FCh)	REG32FC	7:0	Default : 0x00 Access : R/W
	GPO_DATAIN_35_32[3:0]	7:4	REG_GPO_DATAIN[35:32].
	GPO_OEZ_35_32[3:0]	3:0	REG_GPO_OEZ[35:32].
7Eh (32FDh)	REG32FD	7:0	Default : 0x00 Access : R/W
	EXT_DATA_EN_35_32[3:0]	7:4	EXT_DATA_EN[35:32].
	GPO_SEL_35_32[3:0]	3:0	REG_GPO_SEL[35:32].

MOD Register (Bank = 32, Sub-Bank =00)

Index (Absolute)	Mnemonic	Bit	Description
7Fh (32FEh)	REG32FE	7:0	Default : 0x00 Access : RO
	-	7:4	Reserved.
	MOD_GPI_35_32[3:0]	3:0	General purpose input.

PWM Register (Bank = 32, Sub-Bank =01)

PWM Register (Bank = 32, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
01h (3202h)	REG3202	7:0	Default : 0x00	Access : R/W
	-	7:3	Reserved.	
	PWM_GRP2_CLK_GATE_EN	2	Gating clk of pwm grp2.	
	PWM_GRP1_CLK_GATE_EN	1	Gating clk of pwm grp1.	
	PWM_GRP0_CLK_GATE_EN	0	Gating clk of pwm grp0.	
02h (3204h)	REG3204	7:0	Default : 0x00	Access : R/W
	PWM0_PERIOD[7:0]	7:0	PWM0 period.	
02h (3205h)	REG3205	7:0	Default : 0x00	Access : R/W
	PWM0_PERIOD[15:8]	7:0	See description of '3204h'.	
03h (3206h)	REG3206	7:0	Default : 0x00	Access : R/W
	PWM0_DUTY[7:0]	7:0	PWM0 duty.	
03h (3207h)	REG3207	7:0	Default : 0x00	Access : R/W
	PWM0_DUTY[15:8]	7:0	See description of '3206h'.	
04h (3208h)	REG3208	7:0	Default : 0x00	Access : R/W
	PWM0_DIV[7:0]	7:0	PWM0 divider.	
04h (3209h)	REG3209	7:0	Default : 0x00	Access : R/W
	PWM0_OEN	7	PWM0 output enable.	
	-	6:4	Reserved.	
	PWM0_DBEN	3	PWM0 double buffer enable.	
	PWM0_RESET_EN	2	PWM0 Vsync reset0.	
	PWM0_VDBEN	1	PWM0 Vsync double buffer enable.	
	PWM0_POLARITY	0	PWM0 polarity.	
05h (320Ah)	REG320A	7:0	Default : 0x00	Access : R/W
	PWM1_PERIOD[7:0]	7:0	PWM1 period.	
05h (320Bh)	REG320B	7:0	Default : 0x00	Access : R/W
	PWM1_PERIOD[15:8]	7:0	See description of '320Ah'.	
06h (320Ch)	REG320C	7:0	Default : 0x00	Access : R/W
	PWM1_DUTY[7:0]	7:0	PWM1 duty.	
06h (320Dh)	REG320D	7:0	Default : 0x00	Access : R/W
	PWM1_DUTY[15:8]	7:0	See description of '320Ch'.	
07h (320Eh)	REG320E	7:0	Default : 0x00	Access : R/W
	PWM1_DIV[7:0]	7:0	PWM1 divider.	

PWM Register (Bank = 32, Sub-Bank =01)

Index (Absolute)	Mnemonic	Bit	Description
07h (320Fh)	REG320F	7:0	Default : 0x80
	PWM1_OEN	7	PWM1 output enable.
	-	6:4	Reserved.
	PWM1_DBEN	3	PWM1 double buffer enable.
	PWM1_RESET_EN	2	PWM1 Vsync reset1.
	PWM1_VDBEN	1	PWM1 Vsync double buffer enable.
	PWM1_POLARITY	0	PWM1 polarity.
0Ah (3215h)	REG3215	7:0	Default : 0x80
	PWM2_OEN	7	PWM2 output enable.
	-	6:0	Reserved.
0Dh (321Bh)	REG321B	7:0	Default : 0x80
	PWM3_OEN	7	PWM3 output enable.
	-	6:0	Reserved.
0Eh (321Ch)	REG321C	7:0	Default : 0x00
	PWM4_PERIOD[7:0]	7:0	PWM4 period.
0Eh (321Dh)	REG321D	7:0	Default : 0x00
	PWM4_PERIOD[15:8]	7:0	See description of '321Ch'.
0Fh (321Eh)	REG321E	7:0	Default : 0x00
	PWM4_DUTY[7:0]	7:0	PWM4 duty.
0Fh (321Fh)	REG321F	7:0	Default : 0x00
	PWM4_DUTY[15:8]	7:0	See description of '321Eh'.
10h (3220h)	REG3220	7:0	Default : 0x00
	PWM4_DIV[7:0]	7:0	PWM4 divider.
10h (3221h)	REG3221	7:0	Default : 0x80
	PWM4_OEN	7	PWM4 output enable.
	-	6:4	Reserved.
	PWM4_DBEN	3	PWM4 double buffer enable.
	PWM4_RESET_EN	2	PWM4 Vsync reset4.
	PWM4_VDBEN	1	PWM4 Vsync double buffer enable.
	PWM4_POLARITY	0	PWM4 polarity.
11h (3222h)	REG3222	7:0	Default : 0x00
	PWM5_PERIOD[7:0]	7:0	PWM5 period.
11h	REG3223	7:0	Default : 0x00

PWM Register (Bank = 32, Sub-Bank =01)

Index (Absolute)	Mnemonic	Bit	Description
(3223h)	PWM5_PERIOD[15:8]	7:0	See description of '3222h'.
12h (3224h)	REG3224	7:0	Default : 0x00
	PWM5_DUTY[7:0]	7:0	PWM5 duty.
12h (3225h)	REG3225	7:0	Default : 0x00
	PWM5_DUTY[15:8]	7:0	See description of '3224h'.
13h (3226h)	REG3226	7:0	Default : 0x00
	PWM5_DIV[7:0]	7:0	PWM5 divider.
13h (3227h)	REG3227	7:0	Default : 0x80
	PWM5_OEN	7	PWM5 output enable.
	-	6:4	Reserved.
	PWM5_DBEN	3	PWM5 double buffer enable.
	PWM5_RESET_EN	2	PWM5 Vsync reset5.
	PWM5_VDBEN	1	PWM5 Vsync double buffer enable.
	PWM5_POLARITY	0	PWM5 polarity.
14h (3228h)	REG3228	7:0	Default : 0x00
	RST_MUX1	7	PWM1 reset mux.
	-	6:4	Reserved.
	HS_RST_CNT1[3:0]	3:0	PWM1 Hsync reset counter.
14h (3229h)	REG3229	7:0	Default : 0x00
	RST_MUX0	7	PWM0 reset mux.
	-	6:4	Reserved.
	HS_RST_CNT0[3:0]	3:0	PWM0 Hsync reset counter.
15h (322Ah)	REG322A	7:0	Default : 0x00
	RST_MUX3	7	PWM3 reset mux.
	-	6:4	Reserved.
	HS_RST_CNT3[3:0]	3:0	PWM3 Hsync reset counter.
15h (322Bh)	REG322B	7:0	Default : 0x00
	RST_MUX2	7	PWM2 reset mux.
	-	6:4	Reserved.
	HS_RST_CNT2[3:0]	3:0	PWM2 Hsync reset counter.
16h (322Ch)	REG322C	7:0	Default : 0x00
	RST_MUX5	7	PWM5 reset mux.
	-	6:4	Reserved.

PWM Register (Bank = 32, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
	HS_RST_CNT5[3:0]	3:0	PWM5 Hsync reset counter.	
16h (322Dh)	REG322D	7:0	Default : 0x00	Access : R/W
	RST_MUX4	7	PWM4 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT4[3:0]	3:0	PWM4 Hsync reset counter.	
17h ~ 1Fh (322Eh ~ 323Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
20h (3240h)	REG3240	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PWM1_PERIOD_EXT[1:0]	3:2	PWM1 extra 2 bit period setting.	
	PWM0_PERIOD_EXT[1:0]	1:0	PWM0 extra 2 bit period setting.	
20h (3241h)	REG3241	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PWM5_PERIOD_EXT[1:0]	3:2	PWM5 extra 2 bit period setting.	
	PWM4_PERIOD_EXT[1:0]	1:0	PWM4 extra 2 bit period setting.	
21h (3242h)	REG3242	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PWM1_DUTY_EXT[1:0]	3:2	PWM1 extra 2 bit duty setting.	
	PWM0_DUTY_EXT[1:0]	1:0	PWM0 extra 2 bit duty setting.	
21h (3243h)	REG3243	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PWM5_DUTY_EXT[1:0]	3:2	PWM5 extra 2 bit duty setting.	
	PWM4_DUTY_EXT[1:0]	1:0	PWM4 extra 2 bit duty setting.	
22h (3244h)	REG3244	7:0	Default : 0x00	Access : R/W
	PWM0_DIV_EXT[7:0]	7:0	PWM0 extra 8 bit divider setting.	
22h (3245h)	REG3245	7:0	Default : 0x00	Access : R/W
	PWM1_DIV_EXT[7:0]	7:0	PWM1 extra 8 bit divider setting.	
24h (3248h)	REG3248	7:0	Default : 0x00	Access : R/W
	PWM4_DIV_EXT[7:0]	7:0	PWM4 extra 8 bit divider setting.	
24h (3249h)	REG3249	7:0	Default : 0x00	Access : R/W
	PWM5_DIV_EXT[7:0]	7:0	PWM5 extra 8 bit divider setting.	
28h	REG3250	7:0	Default : 0x00	Access : R/W

PWM Register (Bank = 32, Sub-Bank =01)

Index (Absolute)	Mnemonic	Bit	Description
(3250h)	PWM0_SHIFT[7:0]	7:0	PWM0 rising point shift counter.
28h	REG3251	7:0	Default : 0x00
(3251h)	PWM0_SHIFT[15:8]	7:0	See description of '3250h'.
29h	REG3252	7:0	Default : 0x00
(3252h)	-	7:2	Reserved.
	PWM0_SHIFT[17:16]	1:0	See description of '3250h'.
2Ah	REG3254	7:0	Default : 0x00
(3254h)	PWM1_SHIFT[7:0]	7:0	PWM1 rising point shift counter.
2Ah	REG3255	7:0	Default : 0x00
(3255h)	PWM1_SHIFT[15:8]	7:0	See description of '3254h'.
2Bh	REG3256	7:0	Default : 0x00
(3256h)	-	7:2	Reserved.
	PWM1_SHIFT[17:16]	1:0	See description of '3254h'.
30h	REG3260	7:0	Default : 0x00
(3260h)	PWM4_SHIFT[7:0]	7:0	PWM4 rising point shift counter.
30h	REG3261	7:0	Default : 0x00
(3261h)	PWM4_SHIFT[15:8]	7:0	See description of '3260h'.
31h	REG3262	7:0	Default : 0x00
(3262h)	-	7:2	Reserved.
	PWM4_SHIFT[17:16]	1:0	See description of '3260h'.
32h	REG3264	7:0	Default : 0x00
(3264h)	PWM5_SHIFT[7:0]	7:0	PWM5 rising point shift counter.
32h	REG3265	7:0	Default : 0x00
(3265h)	PWM5_SHIFT[15:8]	7:0	See description of '3264h'.
33h	REG3266	7:0	Default : 0x00
(3266h)	-	7:2	Reserved.
	PWM5_SHIFT[17:16]	1:0	See description of '3264h'.
34h ~ 37h	-	7:0	Default : -
(3268h ~ 326Fh)	-	-	Reserved.
40h	REG3280	7:0	Default : 0x00
(3280h)	PWM6_PERIOD[7:0]	7:0	Pwm6 period.
40h	REG3281	7:0	Default : 0x00
			Access : R/W

PWM Register (Bank = 32, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
(3281h)	PWM6_PERIOD[15:8]	7:0	See description of '3280h'.	
41h	REG3282	7:0	Default : 0x00	Access : R/W
(3282h)	PWM6_DUTY[7:0]	7:0	Pwm6 duty.	
41h	REG3283	7:0	Default : 0x00	Access : R/W
(3283h)	PWM6_DUTY[15:8]	7:0	See description of '3282h'.	
42h	REG3284	7:0	Default : 0x00	Access : R/W
(3284h)	PWM6_DIV[7:0]	7:0	Pwm6 divider.	
42h	REG3285	7:0	Default : 0x80	Access : R/W
(3285h)	PWM6_OEN	7	PWM6 output enable.	
	-	6:4	Reserved.	
	PWM6_DBEN	3	Pwm6 double buffer enable.	
	PWM6_RESET_EN	2	Pwm6 Vsync reset0.	
	PWM6_VDBEN	1	Pwm6 Vsync double buffer enable.	
	PWM6_POLARITY	0	Pwm6 polarity.	
43h	REG3286	7:0	Default : 0x00	Access : R/W
(3286h)	PWM7_PERIOD[7:0]	7:0	Pwm7 period.	
43h	REG3287	7:0	Default : 0x00	Access : R/W
(3287h)	PWM7_PERIOD[15:8]	7:0	See description of '3286h'.	
44h	REG3288	7:0	Default : 0x00	Access : R/W
(3288h)	PWM7_DUTY[7:0]	7:0	Pwm7 duty.	
44h	REG3289	7:0	Default : 0x00	Access : R/W
(3289h)	PWM7_DUTY[15:8]	7:0	See description of '3288h'.	
45h	REG328A	7:0	Default : 0x00	Access : R/W
(328Ah)	PWM7_DIV[7:0]	7:0	Pwm7 divider.	
45h	REG328B	7:0	Default : 0x80	Access : R/W
(328Bh)	PWM7_OEN	7	PWM7 output enable.	
	-	6:4	Reserved.	
	PWM7_DBEN	3	Pwm7 double buffer enable.	
	PWM7_RESET_EN	2	Pwm7 Vsync reset1.	
	PWM7_VDBEN	1	Pwm7 Vsync double buffer enable.	
	PWM7_POLARITY	0	Pwm7 polarity.	
46h	REG328C	7:0	Default : 0x00	Access : R/W
(328Ch)	PWM8_PERIOD[7:0]	7:0	Pwm8 period.	

PWM Register (Bank = 32, Sub-Bank =01)

Index (Absolute)	Mnemonic	Bit	Description
46h (328Dh)	REG328D	7:0	Default : 0x00
	PWM8_PERIOD[15:8]	7:0	See description of '328Ch'.
47h (328Eh)	REG328E	7:0	Default : 0x00
	PWM8_DUTY[7:0]	7:0	Pwm8 duty.
47h (328Fh)	REG328F	7:0	Default : 0x00
	PWM8_DUTY[15:8]	7:0	See description of '328Eh'.
48h (3290h)	REG3290	7:0	Default : 0x00
	PWM8_DIV[7:0]	7:0	Pwm8 divider.
48h (3291h)	REG3291	7:0	Default : 0x80
	PWM8_OEN	7	PWM8 output enable.
	-	6:4	Reserved.
	PWM8_DBEN	3	Pwm8 double buffer enable.
	PWM8_RESET_EN	2	Pwm8 Vsync reset2.
	PWM8_VDBEN	1	Pwm8 Vsync double buffer enable.
	PWM8_POLARITY	0	Pwm8 polarity.
49h (3292h)	REG3292	7:0	Default : 0x00
	RST_MUX7	7	PWM7 reset mux.
	-	6:4	Reserved.
	HS_RST_CNT7[3:0]	3:0	PWM7 Hsync reset counter.
49h (3293h)	REG3293	7:0	Default : 0x00
	RST_MUX6	7	PWM6 reset mux.
	-	6:4	Reserved.
	HS_RST_CNT6[3:0]	3:0	PWM6 Hsync reset counter.
4Ah (3295h)	REG3295	7:0	Default : 0x00
	RST_MUX8	7	PWM8 reset mux.
	-	6:4	Reserved.
	HS_RST_CNT8[3:0]	3:0	PWM8 Hsync reset counter.
4Bh (3296h)	REG3296	7:0	Default : 0x00
	-	7:6	Reserved.
	PWM8_PERIOD_EXT[1:0]	5:4	PWM8 extra 2 bit period setting.
	PWM7_PERIOD_EXT[1:0]	3:2	PWM7 extra 2 bit period setting.
	PWM6_PERIOD_EXT[1:0]	1:0	PWM6 extra 2 bit period setting.
4Bh	REG3297	7:0	Default : 0x00

PWM Register (Bank = 32, Sub-Bank =01)				
Index (Absolute)	Mnemonic	Bit	Description	
(3297h)	-	7:6	Reserved.	
	PWM8_DUTY_EXT[1:0]	5:4	PWM8 extra 2 bit duty setting.	
	PWM7_DUTY_EXT[1:0]	3:2	PWM7 extra 2 bit duty setting.	
	PWM6_DUTY_EXT[1:0]	1:0	PWM6 extra 2 bit duty setting.	
4Ch (3298h)	REG3298	7:0	Default : 0x00	Access : R/W
	PWM6_DIV_EXT[7:0]	7:0	PWM6 extra 8 bit divider setting.	
4Ch (3299h)	REG3299	7:0	Default : 0x00	Access : R/W
	PWM7_DIV_EXT[7:0]	7:0	PWM7 extra 8 bit divider setting.	
4Dh (329Ah)	REG329A	7:0	Default : 0x00	Access : R/W
	PWM8_DIV_EXT[7:0]	7:0	PWM8 extra 8 bit divider setting.	
4Eh (329Ch)	REG329C	7:0	Default : 0x00	Access : R/W
	PWM6_SHIFT[7:0]	7:0	PWM6 rising point shift counter.	
4Eh (329Dh)	REG329D	7:0	Default : 0x00	Access : R/W
	PWM6_SHIFT[15:8]	7:0	See description of '329Ch'.	
4Fh (329Eh)	REG329E	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM6_SHIFT[17:16]	1:0	See description of '329Ch'.	
50h (32A0h)	REG32A0	7:0	Default : 0x00	Access : R/W
	PWM7_SHIFT[7:0]	7:0	PWM7 rising point shift counter.	
50h (32A1h)	REG32A1	7:0	Default : 0x00	Access : R/W
	PWM7_SHIFT[15:8]	7:0	See description of '32A0h'.	
51h (32A2h)	REG32A2	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM7_SHIFT[17:16]	1:0	See description of '32A0h'.	
52h (32A4h)	REG32A4	7:0	Default : 0x00	Access : R/W
	PWM8_SHIFT[7:0]	7:0	PWM8 rising point shift counter.	
52h (32A5h)	REG32A5	7:0	Default : 0x00	Access : R/W
	PWM8_SHIFT[15:8]	7:0	See description of '32A4h'.	
53h (32A6h)	REG32A6	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	PWM8_SHIFT[17:16]	1:0	See description of '32A4h'.	

MAILBOX_0 Register (Bank = 33)

MAILBOX_0 Register (Bank = 33)				
Index (Absolute)	Mnemonic	Bit	Description	
40h (3380h)	REG3380	7:0	Default : 0x00	Access : R/W
	MB0_0[7:0]	7:0	Mailbox 0_0.	
40h (3381h)	REG3381	7:0	Default : 0x00	Access : R/W
	MB0_0[15:8]	7:0	See description of '3380h'.	
41h (3382h)	REG3382	7:0	Default : 0x00	Access : R/W
	MB0_1[7:0]	7:0	Mailbox 0_1.	
41h (3383h)	REG3383	7:0	Default : 0x00	Access : R/W
	MB0_1[15:8]	7:0	See description of '3382h'.	
42h (3384h)	REG3384	7:0	Default : 0x00	Access : R/W
	MB0_2[7:0]	7:0	Mailbox 0_2.	
42h (3385h)	REG3385	7:0	Default : 0x00	Access : R/W
	MB0_2[15:8]	7:0	See description of '3384h'.	
43h (3386h)	REG3386	7:0	Default : 0x00	Access : R/W
	MB0_3[7:0]	7:0	Mailbox 0_3.	
43h (3387h)	REG3387	7:0	Default : 0x00	Access : R/W
	MB0_3[15:8]	7:0	See description of '3386h'.	
44h (3388h)	REG3388	7:0	Default : 0x00	Access : R/W
	MB0_4[7:0]	7:0	Mailbox 0_4.	
44h (3389h)	REG3389	7:0	Default : 0x00	Access : R/W
	MB0_4[15:8]	7:0	See description of '3388h'.	
45h (338Ah)	REG338A	7:0	Default : 0x00	Access : R/W
	MB0_5[7:0]	7:0	Mailbox 0_5.	
45h (338Bh)	REG338B	7:0	Default : 0x00	Access : R/W
	MB0_5[15:8]	7:0	See description of '338Ah'.	
46h (338Ch)	REG338C	7:0	Default : 0x00	Access : R/W
	MB0_6[7:0]	7:0	Mailbox 0_6.	
46h (338Dh)	REG338D	7:0	Default : 0x00	Access : R/W
	MB0_6[15:8]	7:0	See description of '338Ch'.	
47h (338Eh)	REG338E	7:0	Default : 0x00	Access : R/W
	MB0_7[7:0]	7:0	Mailbox 0_7.	
47h (338Fh)	REG338F	7:0	Default : 0x00	Access : R/W
	MB0_7[15:8]	7:0	See description of '338Eh'.	

48h (3390h)	REG3390	7:0	Default : 0x00	Access : R/W
	MB0_8[7:0]	7:0	Mailbox 0_8.	
48h (3391h)	REG3391	7:0	Default : 0x00	Access : R/W
	MB0_8[15:8]	7:0	See description of '3390h'.	
49h (3392h)	REG3392	7:0	Default : 0x00	Access : R/W
	MB0_9[7:0]	7:0	Mailbox 0_9.	
49h (3393h)	REG3393	7:0	Default : 0x00	Access : R/W
	MB0_9[15:8]	7:0	See description of '3392h'.	
4Ah (3394h)	REG3394	7:0	Default : 0x00	Access : R/W
	MB0_A[7:0]	7:0	Mailbox 0_A.	
4Ah (3395h)	REG3395	7:0	Default : 0x00	Access : R/W
	MB0_A[15:8]	7:0	See description of '3394h'.	
4Bh (3396h)	REG3396	7:0	Default : 0x00	Access : R/W
	MB0_B[7:0]	7:0	Mailbox 0_B.	
4Bh (3397h)	REG3397	7:0	Default : 0x00	Access : R/W
	MB0_B[15:8]	7:0	See description of '3396h'.	
4Ch (3398h)	REG3398	7:0	Default : 0x00	Access : R/W
	MB0_C[7:0]	7:0	Mailbox 0_C.	
4Ch (3399h)	REG3399	7:0	Default : 0x00	Access : R/W
	MB0_C[15:8]	7:0	See description of '3398h'.	
4Dh (339Ah)	REG339A	7:0	Default : 0x00	Access : R/W
	MB0_D[7:0]	7:0	Mailbox 0_D.	
4Dh (339Bh)	REG339B	7:0	Default : 0x00	Access : R/W
	MB0_D[15:8]	7:0	See description of '339Ah'.	
4Eh (339Ch)	REG339C	7:0	Default : 0x00	Access : R/W
	MB0_E[7:0]	7:0	Mailbox 0_E.	
4Eh (339Dh)	REG339D	7:0	Default : 0x00	Access : R/W
	MB0_E[15:8]	7:0	See description of '339Ch'.	
4Fh (339Eh)	REG339E	7:0	Default : 0x00	Access : R/W
	MB0_F[7:0]	7:0	Mailbox 0_F.	
4Fh (339Fh)	REG339F	7:0	Default : 0x00	Access : R/W
	MB0_F[15:8]	7:0	See description of '339Eh'.	

PMC Register (Bank = 34)

PMC Register (Bank = 34)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3400h)	REG3400	7:0	Default : 0x00	Access : R/W
	SAR5_GPIO_EN	7	SAR5 gpio enable.	
	SAR4_GPIO_EN	6	SAR4 gpio enable.	
	SAR3_GPIO_EN	5	SAR3 gpio enable.	
	SAR2_GPIO_EN	4	SAR2 gpio enable.	
	SAR1_GPIO_EN	3	SAR1 gpio enable.	
	SAR0_GPIO_EN	2	SAR0 gpio enable.	
	-	1	Reserved.	
	IR_GPIO_EN	0	IR PAD gpio enable.	
00h (3401h)	REG3401	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CHSEL[2:0]	5:3	SAR channel selection.	
	SAR_PD	2	SAR power down.	
	INT_GPIO_EN	1	INT PAD gpio enable.	
	-	0	Reserved.	
01h (3402h)	REG3402	7:0	Default : 0x00	Access : R/W
	GPIO_I[7:0]	7:0	GPIO PAD I pin.	
02h (3404h)	REG3404	7:0	Default : 0x00	Access : R/W
	GPIO_OEN[7:0]	7:0	GPIO PAD OEN pin.	
03h (3406h)	REG3406	7:0	Default : 0x00	Access : RO
	GPIO_C[7:0]	7:0	GPIO PAD C pin.	
04h (3408h)	REG3408	7:0	Default : 0x00	Access : R/W
	BOND_OV_KEY[7:0]	7:0	BOND_XTALDIS over write key.	
04h (3409h)	REG3409	7:0	Default : 0x00	Access : R/W
	BOND_OV_KEY[15:8]	7:0	See description of '3408h'.	
05h (340Ah)	REG340A	7:0	Default : 0x00	Access : RO, R/W
	-	7:3	Reserved.	
	BOND_STAT	2	BOND_XTALDIS value.	
	BOND_OV	1	BOND_XTALDIS over write value.	
	BOND_OV_EN	0	BOND_XTALDIS over write enable.	
05h	REG340B	7:0	Default : 0x80	Access : R/W

PMC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description
(340Bh)	FREQ_TUNE[4:0]	7:3	Pm_core frequency tune value.
	DEGLITCH[2:0]	2:0	Pm_core DEGLITCH value.
06h (340Ch)	REG340C	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	PMGPIO_GPIO_SEL	6	1: PAD_PMGPIO_OEN_NODIE; 0:PMGPIO_I.
	PAD_IRIN_OEN_SEL	5	1: Pad_irin_oen = 1; gpio_wakeup.
	PAD_PMCEC_OEN_SEL	4	1: Pad_pmcec_oen = 1; gpio_wakeup.
	PAD_PMGPIO_OEN_SEL	3	1: Pad_pmgpio_oen = 1; gpio_wakeup.
	PAD_INT_OEN_SEL	2	1: Pad_int_oen = 1; gpio_wakeup.
	GPIO_SEL[1:0]	1:0	00: PAD_INT, 01: PAD_PMGPIO, 10: PAD_PMCEC, 11: PAD_IRIN.
06h (340Dh)	-	7:0	Default : - Access : -
	-	-	Reserved.
07h (340Eh)	REG340E	7:0	Default : 0x00 Access : R/W
	DVIRAW_CLK_SEL[1:0]	7:6	DVIRAW_CLK_SEL.
	DVIRAW_CLK_INV	5	DVIRAW_CLK_INV.
	GATE_DVIRAW_CLK	4	GATE_DVIRAW_CLK.
	DVICLK_INV	3	DVICLK_INV.
	GATE_DVICLK	2	GATE_DVICLK.
	DVICLK_CLK_SEL[1:0]	1:0	DVICLK_CLK_SEL.
07h (340Fh)	REG340F	7:0	Default : 0x1E Access : R/W
	-	7:5	Reserved.
	PDN_DVICLKIN_A_FM_PM	4	PDN_DVICLKIN_A_FM_PM.
	PDN_DVIRCK_A_FM_PM[2:0]	3:1	PDN_DVIRCK_A_FM_PM.
	EN_DVI_CLK_DET	0	EN_DVI_CLK_DET.
08h (3410h)	REG3410	7:0	Default : 0x00 Access : R/W
	REG_RCKEY_MISC[4:0]	7:3	REG_RCKEY_MISC.
	BOND_XTALDIS	2	BOND_XTALDIS.
	CHIP_CONFIG[1:0]	1:0	CHIP_CONFIG.
08h (3411h)	REG3411	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	DVICNT[5:0]	5:0	DVICNT.
09h	REG3412	7:0	Default : 0x00 Access : R/W

PMC Register (Bank = 34)				
Index (Absolute)	Mnemonic	Bit	Description	
(3412h)	RCKEY_COMMAND[7:0]	7:0	RCKEY_COMMAND.	
09h	REG3413	7:0	Default : 0x00	Access : R/W
(3413h)	RCKEY_ADDRESS[7:0]	7:0	RCKEY_ADDRESS.	
0Ah	REG3414	7:0	Default : 0x00	Access : R/W
(3414h)	MCCS_WKUP_EN	7	MCCS_WKUP_EN.	
	MCCS_PWR05_EN	6	MCCS_PWR05_EN.	
	MCCS_PWR04_EN	5	MCCS_PWR04_EN.	
	-	4	Reserved.	
	D2B_EN_A0	3	D2B_EN_A0.	
	D2B_EN_A1	2	D2B_EN_A1.	
	D2B_EN_D0	1	D2B_EN_D0.	
	D2B_EN_D1	0	D2B_EN_D1.	
0Ah	REG3415	7:0	Default : 0x00	Access : R/W
(3415h)	EDIDCLK_INV	7	Edidclk gating.	
	EDIDCLK_GATE	6	Edidclk inversion.	
	EDIDCLK_CLK_SEL[1:0]	5:4	Edidclk selection.	
	-	3:0	Reserved.	
0Bh	REG3416	7:0	Default : 0x00	Access : R/W
(3416h)	PMDDC_FORCE_SEL	7	PMDDC_FORCE_SEL.	
	-	6:4	Reserved.	
	DDC_EN_A0	3	Reg_d2b_en_a0.	
	DDC_EN_A1	2	Reg_d2b_en_a1.	
	DDC_EN_D0	1	Reg_d2b_en_d0.	
	DDC_EN_D1	0	Reg_d2b_en_d1.	
0Bh	REG3417	7:0	Default : 0x00	Access : R/W
(3417h)	D2B_WAKEUP_CLR	7	D2B_WAKEUP_CLR.	
	-	6:0	Reserved.	
0Ch	REG3418	7:0	Default : 0x00	Access : R/W
(3418h)	-	7:4	Reserved.	
	FILTER_MSB	3	FILTER_MSB.	
	FILTER_ON	2	FILTER_ON.	
	SLEW_SEL[1:0]	1:0	SLEW_SEL.	
0Ch	REG3419	7:0	Default : 0x00	Access : R/W

PMC Register (Bank = 34)				
Index (Absolute)	Mnemonic	Bit	Description	
(3419h)	-	7	Reserved.	
	IR_WAIT_DDC_IDLE_EN	6	IR_WAIT_DDC_IDLE_EN.	
	CEC_WAIT_DDC_IDLE_EN	5	CEC_WAIT_DDC_IDLE_EN.	
	GPIO_WAIT_DDC_IDLE_EN	4	GPIO_WAIT_DDC_IDLE_EN.	
	RTC_WAIT_DDC_IDLE_EN	3	RTC_WAIT_DDC_IDLE_EN.	
	SAR_WAIT_DDC_IDLE_EN	2	SAR_WAIT_DDC_IDLE_EN.	
	DDC_WAIT_DDC_IDLE_EN	1	DDC_WAIT_DDC_IDLE_EN.	
	DDC_WAKEUP_EN	0	Ddc wakeup enable.	
0Dh (341Ah)	REG341A	7:0	Default : 0x01	Access : R/W
	MCCS_PWR05_FLAG_CLR	7	MCCS_PWR05_FLAG_CLR.	
	-	6	Reserved.	
	MCCS_PWR04_FLAG_CLR	5	MCCS_PWR04_FLAG_CLR.	
	-	4:1	Reserved.	
	RSTZ_SW_DDC	0	RSTZ_SW_DDC.	
0Dh (341Bh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Eh (341Ch)	REG341C	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	DDC_IDLE_LSH	3	DDC_IDLE_LSH.	
	PM_DDC_IDLE	2	PM_DDC_IDLE.	
	MCCS_PWR04_FLAG	1	MCCS_PWR04_FLAG.	
	MCCS_PWR05_FLAG	0	MCCS_PWR05_FLAG.	
0Eh (341Dh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
0Fh (341Eh)	REG341E	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	GPIO_IN_LATCH[4:0]	4:0	Gpio_in latch.	
0Fh (341Fh)	-	7:0	Default : -	
	-	-	Reserved.	

MIIC Register (Bank = 34)

MIIC Register (Bank = 34)				
Index (Absolute)	Mnemonic	Bit	Description	
10h (3420h)	REG3420	7:0	Default : 0x00	Access : R/W
	MENABLE	7	Master IIC enable.	
	SBIT	6	Start bit assert.	
	PBIT	5	Stop bit assert.	
	MACKO	4	Ack output.	
	MACKI	3	Ack input.	
	-	2	Reserved.	
	CLR_NEW_DATA	1	Clear new data flag. 1: Clear. 0: No use.	
	-	0	Reserved.	
11h (3422h)	REG3422	7:0	Default : 0x00	Access : R/W
	MCLK_SEL[7:0]	7:0	Master IIC 0 clock select. 1: CLK/4. 2: CLK/8. 3: CLK/16. 4: CLK/32. 5: CLK/64. 6: CLK/128. 7: CLK/256. 8: CLK/512. 9: CLK/1024. Others: CLK/2.	
12h (3424h)	REG3424	7:0	Default : 0x00	Access : R/W
	WMBUF[7:0]	7:0	Write data.	
13h (3426h)	REG3426	7:0	Default : 0x00	Access : RO
	RMBUF[7:0]	7:0	Read data.	
14h (3428h)	REG3428	7:0	Default : 0x00	Access : RO, R/W, WO
	-	7:4	Reserved.	
	MIIC_RST	3	Set 1 to reset Master IIC circuit.	
	RD_START	2	Set 1 to start byte reading.	
	INT_CLR	1	Set 1 to clear IIC 0 interrupt status.	
	INT_STATUS	0	Write/read/stop finish. Used for software polling, the bit is set if byte write, byte	

MIIC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description
			read or stop is finished. The interrupt status can be cleared by writing INT_CLR bit.
15h (342Ah)	REG342A	7:0	Default : 0x00 Access : R/W
	MIIC_RES[6:0]	7:1	Master IIC reset.
	EN_STOP_INT	0	Enable stop interrupt.
15h (342Bh)	REG342B	7:0	Default : 0x00 Access : R/W
	MIIC_RES[14:7]	7:0	See description of '342Ah'.
18h (3430h)	REG3430	7:0	Default : 0x00 Access : R/W
	MSTART[7:0]	7:0	Master IIC DMA target start address.
18h (3431h)	REG3431	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	MSTART[14:8]	6:0	See description of '3430h'.
19h (3432h)	REG3432	7:0	Default : 0x00 Access : R/W
	MCOUNT[7:0]	7:0	Master IIC DMA byte count. 0: 1 byte. 1: 2 bytes. n: N+1 bytes.
19h (3433h)	REG3433	7:0	Default : 0x00 Access : R/W
	MIIC_DMA_EN	7	Master IIC DMA enable.
	MCOUNT[14:8]	6:0	See description of '3432h'.
1Ah (3434h)	REG3434	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	EELOAD_DEV1_EN	1	EEPROM load to VD enable.
	EELOAD_DEV0_EN	0	EEPROM load to HK enable.
1Ah (3435h)	REG3435	7:0	Default : 0x00 Access : RO
	DMA_END	7	DMA finish flag.
	-	6:0	Reserved.

RTC Register (Bank = 34)

RTC Register (Bank = 34)				
Index (Absolute)	Mnemonic	Bit	Description	
40h (3480h)	REG3480	7:0	Default : 0x21	Access : R/W
	C_INT_CLEAR	7	Clear RTC interrupt.	
	C_INT_FORCE	6	Force RTC interrupt to be 1.	
	C_INT_MASK	5	Mask RTC interrupt.	
	C_READ_EN	4	Read enable for reading value from RTC counter (write and generate one-shot signal for latching rtc_cnt).	
	C_LOAD_EN	3	Load enable for loading value into RTC counter (write and generate one-shot enable signal).	
	C_WRAP_EN	2	Wrap RTC counter when c_match_val is reached.	
	C_CNT_EN	1	Enable RTC counter.	
	C_SOFT_RSTZ	0	RTC software reset (low active).	
41h (3482h)	REG3482	7:0	Default : 0xFF	Access : R/W
	C_FREQ_CW[7:0]	7:0	Frequency control word of RTC counter. Clock frequency of RTC counter = XTAL_frequency/control_word.	
41h (3483h)	REG3483	7:0	Default : 0x7F	Access : R/W
	C_FREQ_CW[15:8]	7:0	See description of '3482h'.	
42h (3484h)	REG3484	7:0	Default : 0x00	Access : R/W
	C_FREQ_CW[23:16]	7:0	See description of '3482h'.	
42h (3485h)	REG3485	7:0	Default : 0x00	Access : R/W
	C_FREQ_CW[31:24]	7:0	See description of '3482h'.	
43h (3486h)	REG3486	7:0	Default : 0x00	Access : R/W
	C_LOAD_VAL[7:0]	7:0	Value to load into RTC counter.	
43h (3487h)	REG3487	7:0	Default : 0x00	Access : R/W
	C_LOAD_VAL[15:8]	7:0	See description of '3486h'.	
44h (3488h)	REG3488	7:0	Default : 0x00	Access : R/W
	C_LOAD_VAL[23:16]	7:0	See description of '3486h'.	
44h (3489h)	REG3489	7:0	Default : 0x00	Access : R/W
	C_LOAD_VAL[31:24]	7:0	See description of '3486h'.	
45h (348Ah)	REG348A	7:0	Default : 0xFF	Access : R/W
	C_MATCH_VAL[7:0]	7:0	Counter match value.	
45h	REG348B	7:0	Default : 0xFF	Access : R/W

RTC Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description
(348Bh)	C_MATCH_VAL[15:8]	7:0	See description of '348Ah'.
46h (348Ch)	REG348C	7:0	Default : 0xFF
	C_MATCH_VAL[23:16]	7:0	See description of '348Ah'.
46h (348Dh)	REG348D	7:0	Default : 0xFF
	C_MATCH_VAL[31:24]	7:0	See description of '348Ah'.
47h (348Eh)	REG348E	7:0	Default : 0x00
	-	7:2	Reserved.
	RTC_INT	1	RTC interrupt status.
	RTC_RAW_INT	0	Raw interrupt status.
48h (3490h)	REG3490	7:0	Default : 0x00
	RTC_CNT[7:0]	7:0	RTC counter value.
48h (3491h)	REG3491	7:0	Default : 0x00
	RTC_CNT[15:8]	7:0	See description of '3490h'.
49h (3492h)	REG3492	7:0	Default : 0x00
	RTC_CNT[23:16]	7:0	See description of '3490h'.
49h (3493h)	REG3493	7:0	Default : 0x00
	RTC_CNT[31:24]	7:0	See description of '3490h'.

PM Register (Bank = 34)

PM Register (Bank = 34)				
Index (Absolute)	Mnemonic	Bit	Description	
50h (34A0h)	REG34A0	7:0	Default : 0x00	Access : R/W
	TEST_MODE	7	Enable PM 5V. 1: High byte debug test bus output. 0: Low byte debug test bus output.	
	CLR_INT	6	Clear interrupt.	
	INT_EN	5	PAD_INT enable.	
	INT_ACT_LEVEL	4	PAD_INT active level.	
	GPIO_WK_TH[3:0]	3:0	The wait threshold to turn on BIUCLK when wakened up by GPIO.	
50h (34A1h)	REG34A1	7:0	Default : 0x03	Access : R/W
	-	7:2	Reserved.	
	PM_SWRST	1	PM soft reset.	
	BULK_OFF	0	Turn off bulk voltage enable.	
51h (34A2h)	REG34A2	7:0	Default : 0x3F	Access : R/W
	RTC_ACT_LEVEL	7	RTC active level.	
	RTC_EN	6	RTC wakeup enable.	
	WAKEUP_EN	5	PAD_WAKEUP wakeup enable.	
	WAKEUP_ACT_LEVEL	4	PAD_WAKEUP wakeup active level.	
	KP_EN	3	Key pad wakeup enable.	
	KP_ACT_LEVEL	2	Key pad wakeup active level.	
	TP_EN	1	Touch panel wakeup enable.	
52h (34A4h)	REG34A4	7:0	Default : 0x81	Access : R/W
	IR_EN	7	IR wakeup enable.	
	IR_ACT_LEVEL	6	IR wakeup active level.	
	IR_WK_TH[3:0]	5:2	The wait threshold to turn on BIUCLK when wakened up by IR.	
	HALT_ON	1	Sleep mode enable.	
	FORCE_GPIO_WK_INT	0	The wait threshold to turn on BIUCLK when wakened up by GPIO (force).	
52h (34A5h)	REG34A5	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	HALT_TH[3:0]	3:0	The wait threshold to turn off standby signal when	

PM Register (Bank = 34)				
Index (Absolute)	Mnemonic	Bit	Description	
			wakened up by sleep mode.	
53h (34A6h)	REG34A6	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SYS_PD	6	Set 1 to start power down sequence, self-cleared.	
	CHECK_NOISE	5	Set 1 to enable IR noise check after being wakened up by IR.	
	DIS_PM_CLK_EN	4	DIS_PM_CLK_EN.	
	STANDBY_TH[3:0]	3:0	The wait threshold to turn off standby signal when wakened up by IR or GPIO.	
53h (34A7h)	REG34A7	7:0	Default : 0x00	Access : R/W
	DIV_SAMPLE[7:0]	7:0	Sleep mode sample enable divider value.	
54h (34A8h)	REG34A8	7:0	Default : 0x00	Access : R/W
	STANDBY_PW[7:0]	7:0	Write 0xA5E4 to enable power management to turn on standby signal.	
54h (34A9h)	REG34A9	7:0	Default : 0x00	Access : R/W
	STANDBY_PW[15:8]	7:0	See description of '34A8h'.	
55h (34AAh)	REG34AA	7:0	Default : 0x00	Access : R/W
	HALT_PW[7:0]	7:0	Write 0xA5B5 to enable power management to turn on standby signal.	
55h (34ABh)	REG34AB	7:0	Default : 0x00	Access : R/W
	HALT_PW[15:8]	7:0	See description of '34AAh'.	
56h (34ACh)	REG34AC	7:0	Default : 0x00	Access : R/W
	XTL_OFF_PW[7:0]	7:0	Write 0x9F8E to enable power management to turn off system crystal.	
56h (34ADh)	REG34AD	7:0	Default : 0x00	Access : R/W
	XTL_OFF_PW[15:8]	7:0	See description of '34ACh'.	
57h (34AEh)	REG34AE	7:0	Default : 0xFF	Access : R/W
	IR_CODE_0[7:0]	7:0	MSB byte IR decoder code.	
57h (34AFh)	REG34AF	7:0	Default : 0xFF	Access : R/W
	IR_CODE_0[15:8]	7:0	See description of '34AEh'.	
58h (34B0h)	REG34B0	7:0	Default : 0xFF	Access : R/W
	IR_CODE_1[7:0]	7:0	LSB byte IR decoder code.	
58h (34B1h)	REG34B1	7:0	Default : 0xFF	Access : R/W
	IR_CODE_1[15:8]	7:0	See description of '34B0h'.	

PM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description
59h (34B2h)	REG34B2	7:0	Default : 0x00 Access : RO
	IR_SAM32_0[7:0]	7:0	MSB byte PM IR decoder code.
59h (34B3h)	REG34B3	7:0	Default : 0x00 Access : RO
	IR_SAM32_0[15:8]	7:0	See description of '34B2h'.
5Ah (34B4h)	REG34B4	7:0	Default : 0x00 Access : RO
	IR_SAM32_1[7:0]	7:0	LSB byte PM IR decoder code.
5Ah (34B5h)	REG34B5	7:0	Default : 0x00 Access : RO
	IR_SAM32_1[15:8]	7:0	See description of '34B4h'.
5Bh (34B6h)	REG34B6	7:0	Default : 0x00 Access : RO
	IR_PTR_DEBUG[1:0]	7:6	IR_PTR value.
	IR_SAM_DEBUG[5:0]	5:0	IR_SAM value.
5Bh (34B7h)	REG34B7	7:0	Default : 0x00 Access : RO
	RDUMMY_0[3:0]	7:4	Read dummy 0.
	EXT_INT_IN	3	EXT_INT_IN.
	IR_PTR_DEBUG[4:2]	2:0	See description of '34B6h'.
5Ch (34B8h)	REG34B8	7:0	Default : 0x00 Access : RO
	PM5V_RST	7	PM5V_RST.
	KP_INT_IN	6	KP_INT_IN.
	RO_POWERGOOD_ORI	5	RO_POWERGOOD_ORI.
	RO_POR_RESET_ORI	4	RO_POR_RESET_ORI.
	VCORE_PWRGD_ORI	3	VCORE_PWRGD_ORI.
	XTL_EN_NEW	2	XTL_EN_NEW.
	RESETZ_NEW	1	RESETZ_NEW.
	BULK_ON	0	BULK_ON.
5Ch (34B9h)	REG34B9	7:0	Default : 0x00 Access : RO
	IR_CHECK_SUM_FAULT	7	IR check sum fault flag.
	IR_MATCH	6	IR_MATCH signal.
	BULK_ON_CHECK_FAULT	5	PO_MATCH check fault flag.
	RDUMMY_1[4:0]	4:0	Read dummy 1.
5Dh (34BAh)	REG34BA	7:0	Default : 0x00 Access : R/W
	IR_CLK_SEL[2:0]	7:5	0: RP_CLK4. 1: RP_CLK5. 2: RP_CLK6.

PM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description
			3: RP_CLK7. 4: RP_CLK0. 5: RP_CLK1. 6: RP_CLK2. 7: RP_CLK3.
	IR_MATCH_LSH_EN	4	IR_MATCH latch for debug.
	IR_CHECK_SUM_EN	3	IR check sum enable.
	IR_MATCH_SEL[1:0]	2:1	00/11: Match simple (!= 00, only read IR). 01: 32-bit IR match. 10: 8-bit IR match.
	GPIO_IN_SEL	0	0: GPIO_IN. 1: GPIO_IN & power down.
5Dh (34BBh)	REG34BB	7:0	Default : 0x00Access : R/W
	IR_SAM_SEL	7	IR SAM selection. 0: Auto. 1: IR_SAM.
	IR_CODE_SEL	6	IR code selection. 0: > 2. 1: >= 2.
	IR_SAM[5:0]	5:0	IR SAM value.
5Eh (34BCh)	REG34BC	7:0	Default : 0x00Access : R/W
	IR_REPEAT_IGNORE	7	IR repeat code ignore.
	WDUMMY_1[5:0]	6:1	Write dummy 1.
	RDUMMY_0_15_8_SEL	0	0: RDUMMY_0[15:8] = HALT_PW_5V[15:8]. 1: RDUMMY_0[15:8] = RDUMMY_0[15:8].
5Eh (34BDh)	REG34BD	7:0	Default : 0x00Access : R/W
	INTEGRATOR_THR[7:0]	7:0	Integrator threshold.
5Fh (34BEh)	REG34BE	7:0	Default : 0x00Access : R/W
	RC_WKUP_EN	7	RC wakeup enable.
	RC_IN_INV	6	RC input inversion.
	IR_MATCH_VCORE_PWRGD_SEL	5	0: IR_MATCH. 1: IR_MATCH & ~VORE_PWRGD.
	RC_ANY_KEY	4	RC any key wakeup.
	RC_AUTODETECT	3	RC auto detect function.
	RC_WKUP_CLR	2	RC wakeup flag clear.

PM Register (Bank = 34)

Index (Absolute)	Mnemonic	Bit	Description
	RC6_EN	1	RC6 enable.
	RC5EXT_EN	0	RC5 extension enable.
5Fh (34BFh)	REG34BF	7:0	Default : 0x16 Access : R/W
	RC_WDOG_COUNT[7:0]	7:0	RC watch dog counter.

A FEC Register (Bank = 35)

A FEC Register (Bank = 35)				
Index	Mnemonic	Bit	Description	
01h ~ 19h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
1Ah	REG1A	7:0	Default : 0x40	Access : R/W
	SVIDEO_EN	7	0: Chroma source from CVBS-channel input. 1: Chroma source from C-channel input.	
	ADC_C_ALWAYS_ON	6	Chroma ADC 16fsc-to-4fsc down-sampling is enabled.	
	-	5:0	Reserved.	
1Bh ~ 6Eh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
6Fh	REG6F	7:0	Default : 0x00	Access : R/W
	LINE_START_VF_SEL[1:0]	7:6	Line start V half line.	
	LINE_MIDDLE_VF_SEL[1:0]	5:4	Line middle V half line.	
	DPL_DPLDB	3	DPL_DE double mode enable.	
	DPL_DBDE	2	Double DE enable.	
	DPL_HSEN	1	DPL_HS mode enable.	
	DPL_DEEN	0	DPL _DE bypass mode enable.	
70h ~ 75h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
76h	REG76	7:0	Default : 0x02	Access : R/W
	-	7:3	Reserved.	
	656_BLANK_MD	2	656 blank mode.	
	656_EN	1	656 enable. 0: Disable. 1: Enable.	
	-	0	Reserved.	
77h	REG77	7:0	Default : 0x02	Access : R/W
	656_BLANK_MAX[7:0]	7:0	Maximum of 656 blank region.	
78h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
79h	REG79	7:0	Default : 0x18	Access : R/W
	656_HDES_O_9_2[7:0]	7:0	BT.656 SAV position. For VCR, 656_HDES = 656_HDES_O - 656_HDES_VCR_OFST * 4. Otherwise, 656_HDES = 656_HDES_O.	

AFEC Register (Bank = 35)				
Index	Mnemonic	Bit	Description	
7Ah	REG7A	7:0	Default : 0x20	Access : R/W
	656_HDES_O_1_0[1:0]	7:6	656 H DE start.	
	-	5:2	Reserved.	
	656_INV_F	1	656 field inverse.	
	SELMIX	0	Mixed data out select.	
7Bh	REG7B	7:0	Default : 0xB3	Access : R/W
	656_HDEW[7:0]	7:0	BT.656 active data width (*4+4).	
7Ch ~ 7Fh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
8Ch	REG8C	7:0	Default : 0x4A	Access : R/W
	TEST_Y[7:0]	7:0	Pattern generation Y.	
8Dh	REG8D	7:0	Default : 0xAD	Access : R/W
	TEST_CB[7:0]	7:0	Pattern generation Cb.	
8Eh	REG8E	7:0	Default : 0x27	Access : R/W
	TEST_CR[7:0]	7:0	Pattern generation Cr.	
8Fh	REG8F	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	FSC_TABLE_3_2[1:0]	3:2	Frequency synthesizer base. 0: 160MHz. 1: 15*14.31818MHz. 2: 216Mhz. 3: 15*14.31818MHz; only valid for REG_FSC_TABLE[4] = 1.	
	FSC_TABLE_1_0[1:0]	1:0	Frequency synthesizer output. 0: 4*fsc. 1: 8*fsc. 2: 16*fsc. 3: 16*fsc.	
92h ~ 95h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
96h	REG96	7:0	Default : 0xA0	Access : R/W
	NOISE_DC_SEL[1:0]	7:6	Noise magnitude estimation DC level selection. 0: IIR_8. 1: IIR_8. 2: CCTRAP_13. 3: CCTRAP.	

AFEC Register (Bank = 35)				
Index	Mnemonic	Bit	Description	
	EDGES_NOISY[5:0]	5:0	Threshold of the average number of sliced edges per line to determine noisy mode (/ 4).	
97h	REG97	7:0	Default : 0x05	Access : R/W
	SYNC_INMUX_3_2[1:0]	7:6	Slicer input pre-filter selection. Enable when SYNC_INMUX[0] = 0. 0: CCTRAP. 1: CCTRAP_13. 2: IIR_8. 3: IIR_16.	
	SYNC_INMUX_1	5	Slicer auxiliary pre-filter selection. 0: IIR_8. 1: IIR_16.	
	SYNC_INMUX_0	4	Slicer input pre-filter selection extend bit. 0: See SYNC_INMUX[3:2]. 1: IIR_4.	
	-	3:0	Reserved.	
98h ~ 9Ch	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
9Dh	REG9D	7:0	Default : 0x6C	Access : R/W
	DPL_NSPL_10_3[7:0]	7:0	PI-type display PLL number of samples per line (MSB). Typically 864.	
9Eh	REG9E	7:0	Default : 0x00	Access : R/W
	DPL_NSPL_2_0[2:0]	7:5	PI-type display PLL number of samples per line (LSB). Typically 864.	
	-	4:0	Reserved.	
9Fh ~ BDh	-	7:0	Default : -	Access : -
	-	7:6	Reserved.	
BEh	REGBE	7:0	Default : 0x6C	Access : R/W
	DPL_NSPL_656_10_3[7:0]	7:0	PI-type display PLL number of samples per line for BT.656 output (MSB). Typically 864.	
BFh	REGBF	7:0	Default : 0x00	Access : R/W
	DPL_NSPL_656_2_0[2:0]	7:5	PI-type display PLL number of samples per line for BT.656 output (LSB). Typically 864.	
	-	4:1	Reserved.	
	STD_656_EN	0	Enable standard 656 output.	
E3h ~	-	7:0	Default : -	Access : -

AFEC Register (Bank = 35)

Index	Mnemonic	Bit	Description
FFh	-	7:0	Reserved.

COMB Register (Bank = 36)

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
3610h	REG3610	7:0	Default : 0x17	Access : R/W
	SVDOIN	7	S-video input.	
	SVDOCBP	6	Band pass filter for S-video C channel.	
	DIRADCIN	5	Direct use ADC input(bypass AFEC).	
	NEW_COMB_EN	4	New Comb enable.	
	MANUCOMB	3	0/1 -> auto/manu select working mode.	
	WORKMD[2:0]	2:0	Working mode: 0/1: 1D, 2: 2D, 3: 3D, other: Enhanced 3D.	
3611h	REG3611	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	CRMAOFF	1	Chroma off.	
	BSTOFF	0	Burst off.	
3612h	REG3612	7:0	Default : 0x18	Access : R/W
	FREESYNC	7	H/V sync free run.	
	FREECNTMD	6	Free run counter mode, 0/1 -> NTSC/PAL.	
	SNOWTYPE[1:0]	5:4	Snow Type, 0: never, 1: auto, 2: force.	
	VWINPOS[3:0]	3:0	Vertical window position.	
3613h	-	7:0	Default : -	Access : -
~	-	-	Reserved.	
3614h	-	-	Reserved.	
3615h	REG3615	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	ETPXVEN	3	Extra vertical entropy enable.	
	SEPETPV	2	Separate vertical entropy.	
	LP2DYMD[1:0]	1:0	Low pass mode of 2D - Y. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
3616h	-	7:0	Default : -	Access : -
	-	-	Reserved.	
3617h	REG3617	7:0	Default : 0xC0	Access : R/W
	HORSTPOS[7:0]	7:0	3D window horizontal starting position, 0..255 -> -128..127.	
3618h	-	7:0	Default : -	Access : -

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
	-	-	Reserved.
3619h	REG3619	7:0	Default : 0x8D
	FREEHTOT_LOW[7:0]	7:0	Free run HSync total (L).
361Ah	REG361A	7:0	Default : 0x03
	-	7:4	Reserved.
	FREEHTOT_HIGH[3:0]	3:0	Free run HSync total (H).
361Bh	REG361B	7:0	Default : 0x83
	PHSDeten	7	Line-lock phase detection enable.
	PHSDetInv	6	Output inverse.
	NEWLLEN	5	New line lock enable(for no burst).
	SCLR_DO_DEM	4	New comb do dem disable.
	PAL_CMP_INV	3	New_comb pal cmp up inverse bit.
	PHSDetsft[2:0]	2:0	Shift-right bit number.
361Ch	REG361C	7:0	Default : 0xEC
	HSFRAFEC	7	H sync from AFEC.
	VSFRAFEC	6	V sync from AFEC.
	BLKFRAFEC	5	Black level from AFEC(MCU).
	-	4	Reserved.
	LNFRMCU	3	525/625 line information from MCU.
	FREQFRMCU	2	3.58/4.43 MHz information from MCU.
	STDSEL[1:0]	1:0	NTSC/PAL decision. 00: From MCU. 01: Force NTSC. 10: Force PAL. 11: From AFEC.
361Dh	-	7:0	Default : -
~	-	-	Reserved.
361Fh	-	-	Reserved.
3620h	REG3620	7:0	Default : 0x67
	-	7	Reserved.
	YNCHMD[2:0]	6:4	Notch mode of Y.
	-	3	Reserved.
	CNCHMD[2:0]	2:0	Notch mode of C.
3621h	REG3621	7:0	Default : 0x81
	-	7:4	Reserved.

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	CRMAFLTMD[1:0]	3:2	Chroma filter mode. 00: Off. 01: Band pass. 10: Median type A. 11: Median type B.	
	CDEMCHK[1:0]	1:0	Chroma vertical check(dem). 00: Off. 01: PAL only. 1x: Always do.	
3622h	-	7:0	Default : -	Access : -
~ 362Dh	-	-	Reserved.	
362Eh	REG362E	7:0	Default : 0x0C	Access : R/W
	THDEM[7:0]	7:0	Threshold for 2D comb filter,Check separated. Chroma complement with up/down line or not.	
362Fh	REG362F	7:0	Default : 0xF8	Access : R/W
	-	7:4	Reserved.	
	DEMOFFSET[3:0]	3:0	Threshold for 2D comb filter,Check separated. Chroma complement with up/down line or not.	
3630h	-	7:0	Default : -	Access : -
~ 363Fh	-	-	Reserved.	
3640h	REG3640	7:0	Default : 0x9C	Access : R/W
	-	7:3	Reserved.	
	BLNKDETMD	2	Blank level detect mode, 0: Either 240 or 252, 1: 230~262 is possible.	
	VDETMD[1:0]	1:0	Vertical timing detect mode. 0x: Auto. 10: Force 525 line. 11: Force 625 line.	
3641h	REG3641	7:0	Default : 0x08	Access : R/W
	SENSSIGDET[7:0]	7:0	Sensitivity of signal detect.	
3642h	REG3642	7:0	Default : 0xFF	Access : R/W
	SYNCLVLTLRN[7:0]	7:0	Sync level tolerance.	
3643h	REG3643	7:0	Default : 0x60	Access : R/W
	VRCOASTLEN[7:0]	7:0	VCR coast length.	
3644h	REG3644	7:0	Default : 0x80	Access : R/W

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	HBIDLY[7:0]	7:0	Horizontal blanking region position.	
3645h	-	7:0	Default : -	Access : -
~ 3646h	-	-	Reserved.	
3647h	REG3647	7:0	Default : 0x00	Access : R/W
	CTIFIR_GPATCH_COR[3:0]	7:4	CTI FIR Gray Patch Coring (val*2).	
	CTIFIR_GPATCH_GAIN[1:0]	3:2	CTI FIR Gray Patch Gain (0.25/0.5/1/2).	
	CTIFIR_GPATCH_MD[1:0]	1:0	CTI FIR Gray Patch Mode ([0]: Off [1]:30% [2]: 60% [3]:100%).	
3648h	REG3648	7:0	Default : 0x20	Access : R/W
	YCIPIPE[1:0]	7:6	Y/C pipe delay.	
	DEGPIPE[1:0]	5:4	Degree pipe delay.	
	-	3:0	Reserved.	
3649h	REG3649	7:0	Default : 0x01	Access : R/W
	IAN_MAXEV2_GAIN[1:0]	7:6	T-CrossH: V2 entropy gain selection.	
	IAN_MAXEV1_GAIN[1:0]	5:4	T-CrossH: V1 entropy gain selection.	
	-	3:1	Reserved.	
	IAN_EH_EN	0	H-direction T cross patch enable.	
364Ah	REG364A	7:0	Default : 0x56	Access : R/W
	CTIFIR_GAIN[3:0]	7:4	CTI FIR Gain (1/2/3/4/6/8/12/16/24/32/48/64/96/128).	
	-	3	Reserved.	
	CTIFIR_MD[1:0]	2:1	CTI FIR Mode for Max/Min Windows([0]: wide [1]: med [2] small [3] little).	
	CTIFIR_EN	0	CTI FIR Enable.	
364Bh	-	7:0	Default : -	Access : -
~ 364Dh	-	-	Reserved.	
364Eh	REG364E	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	PIPDGBHST[1:0]	5:4	Motion factor pipeline control.	
	PIPCHKHST[3:0]	3:0	Motion history pipeline control.	
364Fh	REG364F	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	3DBLUR_GAIN[4:0]	4:0	3D blur gain (1~1/16).	
3650h	REG3650	7:0	Default : 0x07	Access : R/W

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	DBG_2DCOMB_YCETP_SEL[1:0]	7:6	Selection of (entropyh/eh4/eh2) /. (entropyv/ev2/ev1) /. (entropyv-h/sw_gain/cdet_swgain). With d[5:4] = 2'd1/2'd2/2'd3.	
	DBG_2DCOMB_ENTROPY[1:0]	5:4	00: Normal. 01: EntropyH. 10: EntropyV. 11: EntropyV-entropyH.	
	AUTOSTOPSYNC	3	Automatic stop H/V sync when no input.	
	LNFREEMD[2:0]	2:0	Line buffer free run mode. 0: Off(always synchronize). 1: 909 return. 2: 910 return. 3: 917 return. 4: 1127 return. 5: 1135 return. 6: Decided by register. 7: Automatic.	
3651h	-	7:0	Default : -	Access : -
~ 365Fh	-	-	Reserved.	
3660h	REG3660	7:0	Default : 0x00	Access : R/W
	IFMODE[1:0]	7:6	IF compensation mode.	
	IFCOEF[5:0]	5:0	IF compensation coefficient, 2-bit integer, 4-bit frac.	
3661h	-	7:0	Default : -	Access : -
~ 366Bh	-	-	Reserved.	
366Ch	REG366C	7:0	Default : 0x00	Access : R/W
	ACC_MODE	7	ACC mode selection.	
	-	6:4	Reserved.	
	CBINV	3	Cb inverse for s-video.	
	CRINV	2	Cr inverse for s-video.	
	-	1:0	Reserved.	
366Dh	-	7:0	Default : -	Access : -
	-	-	Reserved.	
366Eh	REG366E	7:0	Default : 0x00	Access : R/W
	YDETV_SCL_THLO[3:0]	7:4	New EV1 scale threshold LOW.	

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	YDETV_SCL_BLD RG[1:0]	3:2	New EV1 scale blending region.	
	-	1	Reserved.	
	NEW_EV1_EN	0	New EV1 entropy enable.	
366Fh	-	7:0	Default : -	Access : -
	-	-	Reserved.	
3670h	REG3670	7:0	Default : 0xF0	Access : R/W
	-	7:6	Reserved.	
	CGMODE[1:0]	5:4	Auto chroma gain mode. 00: Off. 01: Auto. 10: Manu. 11: MCU control.	
	BRSTFRA FEC	3	Burst height from AFEC.	
	-	2	Reserved.	
	DBG_GAIN_SEL[1:0]	1:0	Debug gain selection.	
3671h	-	7:0	Default : -	Access : -
	-	-	Reserved.	
3672h	REG3672	7:0	Default : 0x00	Access : R/W
	BSTHGHT[7:0]	7:0	Burst height for auto chroma gain, 0: auto, 112 for NTSC and 117 for PAL; other: use RegBSTHGHT/DetBSTHGHT as C gain.	
3673h	REG3673	7:0	Default : 0x80	Access : R/W
	CTST[7:0]	7:0	Contrast adjustment coefficient.	
3674h	REG3674	7:0	Default : 0x80	Access : R/W
	BRHT[7:0]	7:0	Brightness adjustment coefficient.	
3675h	REG3675	7:0	Default : 0x80	Access : R/W
	SAT[7:0]	7:0	Saturation adjustment coefficient.	
3676h ~ 3677h	-	7:0	Default : -	Access : -
	-	-	Reserved.	
3678h	REG3678	7:0	Default : 0x80	Access : R/W
	CRMAGAIN_LOW[7:0]	7:0	Chroma gain value for manual chroma gain(7:0).	
3679h	REG3679	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	CRMAGAIN_HIGH[5:0]	5:0	Chroma gain value for manual chroma gain(13:8).	

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
367Ah	-	7:0	Default : -	Access : -
~	-	-	Reserved.	
367Ch	-	-	Reserved.	
367Dh	REG367D	7:0	Default : 0x80	Access : R/W
	SNOWDELAY[7:0]	7:0	Latency of snow output after signal missing.	
367Eh	REG367E	7:0	Default : 0x00	Access : R/W
	ACC_CRMAGAIN_INC[2:0]	7:5	Chroma gain step of ACC.	
	ACCUPONLY	4	ACC up only.	
	ACCDELAY[3:0]	3:0	ACC latency.	
367Fh	REG367F	7:0	Default : 0xFF	Access : R/W
	ACCMAXGAIN[7:0]	7:0	ACC maximum gain.	
3680h	REG3680	7:0	Default : 0xC8	Access : R/W
	YGAIN[7:0]	7:0	Luma gain for U/V demodulation.	
3681h	REG3681	7:0	Default : 0x96	Access : R/W
	CBGAIN[7:0]	7:0	Cb gain for U/V demodulation.	
3682h	REG3682	7:0	Default : 0x6A	Access : R/W
	CRGAIN[7:0]	7:0	Cr gain for U/V demodulation.	
3683h	REG3683	7:0	Default : 0x04	Access : R/W
	-	7:6	Reserved.	
	CTIMODE[1:0]	5:4	CTI mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
	-	3:2	Reserved.	
	CBCRLPMD[1:0]	1:0	Cb/Cr low pass mode. 00: Off. 01: Weak. 10: Normal. 11: Strong.	
3684h	REG3684	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	CTSTDITHEN	6	Dithering when contrast adjustment.	
	CTSTDITHPOS[1:0]	5:4	Dithering position(offset) of contrast.	
	-	3	Reserved.	

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	SATDITHEN	2	Dithering when saturation adjustment.	
	SATDITHPOS[1:0]	1:0	Dithering position(offset) of saturation.	
3685h	REG3685	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	YDEMDITHEN	6	Dithering when demodulation Y-gain.	
	YDEMDITHPOS[1:0]	5:4	Dithering position(offset) of Y gain.	
	-	3	Reserved.	
	CDEMDITHEN	2	Dithering when demodulation C-gain.	
	CDEMDITHPOS[1:0]	1:0	Dithering position(offset) of C gain.	
3686h	REG3686	7:0	Default : 0x00	Access : R/W
	MOT_ADP_STIL_TH[7:0]	7:0	Motion adaptive still image threshold.	
3687h	REG3687	7:0	Default : 0x00	Access : R/W
	-	7:1	Reserved.	
	MOT_DIFF_MIN_SEL	0	Motion Difference or minimum selection.	
3688h	REG3688	7:0	Default : 0x00	Access : R/W
	ETPV_COR[3:0]	7:4	Entropy V coring.	
	ETPH_COR[3:0]	3:0	Entropy H coring.	
3689h	REG3689	7:0	Default : 0x00	Access : R/W
	ETPV1_COR[3:0]	7:4	Entropy V1 coring.	
	ETPH2_COR[3:0]	3:0	Entropy H2 coring.	
368Bh	-	7:0	Default : -	Access : -
~	-	-	Reserved.	
368Ch	-	-	Reserved.	
368Dh	REG368D	7:0	Default : 0x00	Access : R/W
	COMBCTRL[7:0]	7:0	Some control signals for FPGA.	
368Eh	REG368E	7:0	Default : 0xE0	Access : R/W
	FPGACTRL[7:0]	7:0	Some control signals for FPGA.	
368Fh	-	7:0	Default : -	Access : -
	-	-	Reserved.	
3690h	REG3690	7:0	Default : 0x13	Access : R/W
	-	7:4	Reserved.	
	YDETV_PATCH_EN	3	YDET Patch V Enable.	
	MBS_V_HDIFF_EN	2	Jeff H MBS-C Enable([0]: {1,0,2,0,1} [1]: {2,0,0,0,-2}).	
	MIN_YDETH_EN	1	Minimum YDETH Mode Enable ([0]: Normal [1]:	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
			min(2tap,3tap)).
	NEW_YDET_EN	0	CVBS Lowpass YDET Enable.
3691h	REG3691	7:0	Default : 0x12 Access : R/W
	YDIFFV1_LUMA_ENG_GAIN[1:0]	7:6	YDET V Luma Gain(div 1/2/4/8).
	YDIFFV1_CRMA_ENG_GAIN[1:0]	5:4	YDET V Chroma Gain(div 1/2/4/8).
	YDIFFH2_LUMA_ENG_GAIN[1:0]	3:2	YDET H Luma Gain(div 1/2/4/8).
	YDIFFH2_CRMA_ENG_GAIN[1:0]	1:0	YDET H Chroma Gain(div 1/2/4/8).
3692h	REG3692	7:0	Default : 0x51 Access : R/W
	DET_FILTER_MD_H_B[1:0]	7:6	PAL H DET Filter Mode B([00]:lpf[1,2,-1] [11]:bpf[1,-1]).
	-	5	Reserved.
	PAL_MBS_TAP_MD_H_B	4	PAL H Multiburst Tap B([0]:2tap [1]:3tap) Note: If we set [0], det_filter_md MUST set [11]).
	-	3	Reserved.
	DET_FILTER_MD_H_A[1:0]	2:1	PAL H DET Filter Mode A([00]:lpf[1,2,-1] [11]:bpf[1,-1]).
	PAL_MBS_TAP_MD_H_A	0	PAL H Multiburst Tap A([0]:2tap [1]:3tap) Note: If we set [0], det_filter_md MUST set [11]).
3693h	REG3693	7:0	Default : 0x00 Access : R/W
	-	7:3	Reserved.
	DET_FILTER_MD_V[1:0]	2:1	PAL V DET Filter Mode([0]: 2tap mode: {2,0,-2}/{0,2,-2} [1]: 3tap mode: {1,1,-2}/{0,2,-2}).
	PAL_MBS_TAP_MD_V	0	PAL V Multiburst Tap([0]:2tap [1]:3tap).
3694h	REG3694	7:0	Default : 0x00 Access : R/W
	MB_GAIN_H[3:0]	7:4	YDET Patch H Multiburst Gain (multiply 1~16).
	C_GAIN_H[1:0]	3:2	YDET Patch H Chroma Gain (divide 2,4,8,16).
	ENG_SCALE[1:0]	1:0	YDET Patch Multiburst-Chroma Energy Scale(multiply 4/8/16/32).
3695h	REG3695	7:0	Default : 0xCC Access : R/W
	CDET_V_LUMA_ENG_GAIN[1:0]	7:6	CDET V Luma Gain(multiply 1/2/4/8).
	CDET_V_CRMA_ENG_GAIN[1:0]	5:4	CDET V Chroma Gain(multiply 1/2/4/8).
	CDET_H_LUMA_ENG_GAIN[1:0]	3:2	CDET H Luma Gain(multiply 1/2/4/8).
	CDET_H_CRMA_ENG_GAIN[1:0]	1:0	CDET H Chroma Gain(multiply 1/2/4/8).
3696h	REG3696	7:0	Default : 0x00 Access : R/W
	CDET_SWITCH_THR[7:0]	7:0	CDET Switch threshold.
3697h	REG3697	7:0	Default : 0x00 Access : R/W

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
	CDET_SWITCH_STEP[1:0]	7:6	CDET Switch Step (multiply 1/2/4/8).
	-	5:0	Reserved.
3698h	REG3698	7:0	Default : 0x2A Access : R/W
	PAL_2DCNCH_MD[1:0]	7:6	PAL Chroma 2D 9x5 Mode ([00]:V{12221} [01]:{14641} [1x] 01210).
	PAL_DIFFV2_SEL	5	CVDiff V2 Select for PAL([0]: Blend(max2, DiffUD) [1]: max(max2, DiffUD)).
	LPF_FACTOR[4:0]	4:0	CVBS Lowpass Blending Factor.
3699h	REG3699	7:0	Default : 0x01 Access : R/W
	CVH2PATCH_EN	7	SC's Diagonal Patch Enable(NTSC443 Only).
	CVDIFF_H2_GAIN[2:0]	6:4	SC's Diagonal Patch Gain (multiply 1/0.5/0.25/0.125//0.0625/0.03125/2/4).
	PAL_DIFFV1_SEL	3	PAL cvdiff v1 select [0]: Ian v1 [1]: Jeff v1.
	PAL_CVDIFF_V2_GAIN[2:0]	2:0	CVDiff V2 Gain for PAL (multiply 0/1/2/4/8/0.5/0.25/0.125).
369Ah	REG369A	7:0	Default : 0x03 Access : R/W
	AMPV1_GAIN[3:0]	7:4	AMP_YDIFF_V1 Gain (divide 8/16/24/32/40/48/56/64/80/96/112/128/160/192/224/256).
	AMPH2_GAIN[3:0]	3:0	AMP_YDIFF_H2 Gain (divide 8/16/24/32/40/48/56/64/80/96/112/128/160/192/224/256).
369Bh	REG369B	7:0	Default : 0x00 Access : R/W
	-	7:5	Reserved.
	CHROMA_ADPLD_SEL	4	Chroma Fix Select for AdaptiveCrma Blending ([0]: Original [1]: 12221Fix).
	YDETHBND_TH[2:0]	3:1	YDET H Bound TH by Reg.
	YDETHBND_EN	0	YDET H Bound Enable by Reg.
369Ch	REG369C	7:0	Default : 0x01 Access : R/W
	-	7	Reserved.
	V5DBG_EN	6	Entropy V5 Debug Mode Enable (Use V2).
	V5FLT_SEL	5	Entropy V5 Filter Select ([0]: Max [1]: LP12221).
	PALETPV_SEL	4	PAL Entropy V Select ([0]: Original [1]: Entropy V5).
	ETP_H2GAIN[1:0]	3:2	Entropy H2 Gain (mul 1/2/4/8).
	PALV1_EN	1	Disable PAL V1 Calculation in PAL(for pal use only).
	H2V1_EN	0	H2 v1 Enable ([0]: set y21_gain 0 [1]: default).
369Dh	REG369D	7:0	Default : 0x08 Access : R/W
	EV2_PROCFLT_SEL[1:0]	7:6	Entropy V2 Proc Filter Select([00]: Original [01]:

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
			lp121(NTSOnly) [10]: m_MaxMin [11]: lp12221 m_cvdifv2).
	-	5	Reserved.
	EH4_PROCFLT_SEL	4	Entropy H4 Proc Filter Select ([0]: Original [1]: LP{12221}).
	EV1_POSTFLT_SEL	3	Entropy V1 Post Filter Select ([0]: Original [1]: lp121).
	EV1_PROCFLT_SEL	2	Entropy V1 Proc Filter Select ([0]: Original [1]: minmax).
	EH2_POSTFLT_SEL	1	Entropy H2 Post Filter Select ([0]: Max [1]: Lp12221).
	EH2_PROCFLT_SEL	0	Entropy H2 Proc Filter Select ([0]: Original [1]: minmax).
369Eh	REG369E	7:0	Default : 0xC1 Access : R/W
	IAN_MAXEH4_GAIN[1:0]	7:6	T-Cross Patch H4 gain (1/2/4/8).
	IAN_MAXEH2_GAIN[1:0]	5:4	T-Cross Patch H2 gain (1/2/4/8).
	-	3:1	Reserved.
	IAN_EV_EN	0	T-Cross Patch V Enable.
369Fh	REG369F	7:0	Default : 0x01 Access : R/W
	-	7:5	Reserved.
	SAWBLENDIV[4:0]	4:0	SAW blend division.
36A0h	REG36A0	7:0	Default : 0x48 Access : R/W
	ADP9X5_CSWEN	7	Adaptive 9X5 use CDET switch gain enable.
	ADPGAIN_SCUP_EN	6	Adaptive 9x5 Scale Up Enable.
	REFER_3X3LRDIFF_EN	5	Adaptive 9x5 Reference Adaptive 3x3 Difference Enable(for LR Diff).
	REFER_H4_EN	4	Adaptive 3x3 Reference Adaptive 9x5 Difference Enable(for LR Diff).
	ADPCRMA_SEL	3	Adaptive Chroma Select ([0]: 14641 [1]: 12221).
	ADPLUMA_SEL	2	Adaptive Luma Select ([0]: 14641 [1]: 12221).
	ADP2DSEL[1:0]	1:0	Adaptive Mode (9x5 / 9x3 / 3x5 / 3x3).
36A1h	REG36A1	7:0	Default : 0x00 Access : R/W
	ADPGAINLR1P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.
	ADPGAINLR0P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.
36A2h	REG36A2	7:0	Default : 0x21 Access : R/W
	ADPGAINLR3P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.
	ADPGAINLR2P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.
36A3h	REG36A3	7:0	Default : 0x84 Access : R/W
	ADPGAINLR5P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	ADPGAINLR4P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
36A4h	REG36A4	7:0	Default : 0xEC	Access : R/W
	ADPGAINLR7P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.	
	ADPGAINLR6P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
36A5h	REG36A5	7:0	Default : 0x0F	Access : R/W
	ADPGAINLR9P[3:0]	7:4	Adp3x3 Lookup Gain LR Table.	
	ADPGAINLR8P[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
36A6h	REG36A6	7:0	Default : 0x60	Access : R/W
	-	7	Reserved.	
	ADPGAINLR8TOAP[2:0]	6:4	Adp3x3 Lookup Gain LR Table (Sign Bit), 8~Ap[4].	
	ADPGAINLRAP[3:0]	3:0	Adp3x3 Lookup Gain LR Table.	
36A7h	REG36A7	7:0	Default : 0x00	Access : R/W
	ADPGAINLR0TO7P[7:0]	7:0	Adp3x3 Lookup Gain LR Table (Sign Bit), 0~7p[4].	
36A8h	REG36A8	7:0	Default : 0x00	Access : R/W
	ADPGAINUD1P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD0P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
36A9h	REG36A9	7:0	Default : 0x21	Access : R/W
	ADPGAINUD3P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD2P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
36AAh	REG36AA	7:0	Default : 0x84	Access : R/W
	ADPGAINUD5P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD4P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
36ABh	REG36AB	7:0	Default : 0xEC	Access : R/W
	ADPGAINUD7P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD6P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
36ACh	REG36AC	7:0	Default : 0x0F	Access : R/W
	ADPGAINUD9P[3:0]	7:4	Adp3x3 Lookup Gain UD Table.	
	ADPGAINUD8P[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
36ADh	REG36AD	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	ADPGAINUD8TOAP[2:0]	6:4	Adp3x3 Lookup Gain UD Table (Sign Bit), 8~Ap[4].	
	ADPGAINUDAP[3:0]	3:0	Adp3x3 Lookup Gain UD Table.	
36AEh	REG36AE	7:0	Default : 0x00	Access : R/W
	ADPGAINUD0TO7P[7:0]	7:0	Adp3x3 Lookup Gain UD Table (Sign Bit), 0~7p[4].	

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
36AFh	REG36AF	7:0	Default : 0x20	Access : R/W
	LP2DYREF[7:0]	7:0	Reference for adaptive luma low pass filter.	
36B0h	REG36B0	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ADP9X5_CREGION_SEL[1:0]	5:4	Adaptive9x5 chroma region select.	
	-	3	Reserved.	
	ADP9X5_DBGSEL[2:0]	2:0	Adaptive 9x5 Debug Output Select.	
36B1h	REG36B1	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN0[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
36B2h	REG36B2	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN1[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
36B3h	REG36B3	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN2[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
36B4h	REG36B4	7:0	Default : 0x0C	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN3[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
36B5h	REG36B5	7:0	Default : 0x0F	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN4[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
36B6h	REG36B6	7:0	Default : 0x10	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN5[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
36B7h	REG36B7	7:0	Default : 0x11	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN6[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
36B8h	REG36B8	7:0	Default : 0x14	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN7[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	
36B9h	REG36B9	7:0	Default : 0x20	Access : R/W
	-	7:6	Reserved.	
	ADP9X5GAIN8[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
36BAh	REG36BA	7:0	Default : 0x20
	-	7:6	Reserved.
	ADP9X5GAIN9[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).
36BBh	REG36BB	7:0	Default : 0x20
	-	7:6	Reserved.
	ADP9X5GAINA[5:0]	5:0	Adp9x5 Lookup Gain Table (0~32)<=> (-16~16).
36BCh	REG36BC	7:0	Default : 0x01
	-	7:6	Reserved.
	FP_HOR_PIPE[1:0]	5:4	Final Patch Horizontal version pipe selection.
	-	3:1	Reserved.
	FP_HOR_EN	0	Enable Final Patch Horizontal version.
36BDh	REG36BD	7:0	Default : 0x50
	IAN_TH_HOR[7:0]	7:0	Ian PureLuma TH_Ver (25): U/D Diff Threshold for Detection.
36BEh	REG36BE	7:0	Default : 0x50
	IAN_DIFF_SHIFTR[1:0]	7:6	Ian PureLuma R Diff Shift(div 1/2/4/8) before TH.
	IAN_DIFF_SHIFTL[1:0]	5:4	Ian PureLuma L Diff Shift(div 1/2/4/8) before TH.
	IAN_DIFF_MSHTR[1:0]	3:2	Ian PureLuma R Diff Shift(div 4/8/16/32) after TH (8~=32 inC).
	IAN_DIFF_MSHTL[1:0]	1:0	Ian PureLuma L Diff Shift(div 4/8/16/32) after TH (8~=32 inC).
36BFh	REG36BF	7:0	Default : 0x04
	LP2DYTH[7:0]	7:0	Threshold for adaptive luma low pass filter.
36C0h	REG36C0	7:0	Default : 0xA0
	CRMA2D_SEL[1:0]	7:6	Chroma 2D Select (5x5/5x5/adaptive/DEMBld).
	LUMA2D_SEL[1:0]	5:4	Luma 2D Select (5x5/5x5/adaptive/adaptive).
	CRMAOUT_MODE[1:0]	3:2	Chroma Output Mode ([00]: Normal [01]: 1DH [10]: 1DV [11]: 2D).
	LUMAOUT_MODE[1:0]	1:0	Luma Output Mode ([00]: Normal [01]: 1DH [10]: 1DV [11]: 2D).
36C1h	REG36C1	7:0	Default : 0x33
	YETPV_GAIN[3:0]	7:4	Luma Entropy Gain V for Lookup Table (mul (1~16)/4).
	YETPH_GAIN[3:0]	3:0	Luma Entropy Gain H for Lookup Table (mul (1~16)/4).
36C2h	REG36C2	7:0	Default : 0x33

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	CETPV_GAIN[3:0]	7:4	Chroma Entropy Gain V for Lookup Table (mul (1~16)/4).	
	CETPH_GAIN[3:0]	3:0	Chroma Entropy Gain H for Lookup Table (mul (1~16)/4).	
36C3h	REG36C3	7:0	Default : 0x1F	Access : R/W
	-	7:5	Reserved.	
	AUTO2D_EN	4	When it is unknown TV System, force 2D Output Enable.	
	CETP_SCDN_EN	3	Chroma Entropy Scaled Down Enable.	
	CETP_SCUP_EN	2	Chroma Entropy Scaled Up Enable.	
	YETP_SCDN_EN	1	Luma Entropy Scaled Down Enable.	
	YETP_SCUP_EN	0	Luma Entropy Scaled Up Enable.	
36C4h	REG36C4	7:0	Default : 0x00	Access : R/W
	YBLD_FORCE_SW_GAIN[3:0]	7:4	Luma Blending Forced Switch Gain(0~128).	
	-	3:1	Reserved.	
	YBLD_FORCE_SW	0	Luma Blending Forced Switch Enable.	
36C5h	REG36C5	7:0	Default : 0x00	Access : R/W
	CROSSPT_EN	7	Cross point patch enable.	
	-	6:0	Reserved.	
36C6h	REG36C6	7:0	Default : 0x20	Access : R/W
	YGAIN_YH1P[3:0]	7:4	Luma Lookup Gain Table YH.	
	YGAIN_YH0P[3:0]	3:0	Luma Lookup Gain Table YH.	
36C7h	REG36C7	7:0	Default : 0x85	Access : R/W
	YGAIN_YH3P[3:0]	7:4	Luma Lookup Gain Table YH.	
	YGAIN_YH2P[3:0]	3:0	Luma Lookup Gain Table YH.	
36C8h	REG36C8	7:0	Default : 0x88	Access : R/W
	YGAIN_YH5P[3:0]	7:4	Luma Lookup Gain Table YH.	
	YGAIN_YH4P[3:0]	3:0	Luma Lookup Gain Table YH.	
36C9h	REG36C9	7:0	Default : 0x88	Access : R/W
	YGAIN_YH7P[3:0]	7:4	Luma Lookup Gain Table YH.	
	YGAIN_YH6P[3:0]	3:0	Luma Lookup Gain Table YH.	
36CAh	REG36CA	7:0	Default : 0x20	Access : R/W
	YGAIN_YV1P[3:0]	7:4	Luma Lookup Gain Table YV.	
	YGAIN_YV0P[3:0]	3:0	Luma Lookup Gain Table YV.	
36CBh	REG36CB	7:0	Default : 0x85	Access : R/W
	YGAIN_YV3P[3:0]	7:4	Luma Lookup Gain Table YV.	
	YGAIN_YV2P[3:0]	3:0	Luma Lookup Gain Table YV.	

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
36CCh	REG36CC	7:0	Default : 0x88	Access : R/W
	YGAINV5P[3:0]	7:4	Luma Lookup Gain Table YV.	
	YGAINV4P[3:0]	3:0	Luma Lookup Gain Table YV.	
36CDh	REG36CD	7:0	Default : 0x88	Access : R/W
	YGAINV7P[3:0]	7:4	Luma Lookup Gain Table YV.	
	YGAINV6P[3:0]	3:0	Luma Lookup Gain Table YV.	
36CEh	-	7:0	Default : -	Access : -
~	-	-	Reserved.	
36CFh	-	-	Reserved.	
36D0h	REG36D0	7:0	Default : 0xB9	Access : R/W
	PEAKING_PALCMP_INV	7	Peaking palcmp inverse.	
	IAN_ENH_CLIP[2:0]	6:4	Clipping TH (0/16/32/64/96/128/160/192).	
	IAN_ENH_CORING[1:0]	3:2	Coring TH (0/4/8/16).	
	NTSC_PEAKING_SEL	1	Ntsc peaking method select ([0]: Ian Mode [1]: X Mode).	
	IAN_ENH_PEAKING_EN	0	Ian Enhanced Peaking Enable.	
36D1h	REG36D1	7:0	Default : 0x40	Access : R/W
	IAN_ENH_Y1GAIN[7:0]	7:0	Y1 gain (div(16~128) >>3).	
36D2h	REG36D2	7:0	Default : 0x40	Access : R/W
	IAN_ENH_Y2GAIN[7:0]	7:0	Y2 gain (div(16~128) >>3).	
36D3h	REG36D3	7:0	Default : 0x60	Access : R/W
	IAN_ENH_Y3GAIN[7:0]	7:0	Y3 gain (div(16~128) >>3).	
36D4h	REG36D4	7:0	Default : 0x20	Access : R/W
	IAN_MIN_CDIFFH[7:0]	7:0	Peaking minimum C Difference Horizontal.	
36D5h	REG36D5	7:0	Default : 0x08	Access : R/W
	IAN_MIN_CDIFFV[7:0]	7:0	Peaking minimum C Difference Vertical.	
36D6h	REG36D6	7:0	Default : 0x0A	Access : R/W
	-	7:4	Reserved.	
	IAN_CDIFFV_RANGE[1:0]	3:2	Peaking C Difference Vertical Range (16/32/64/128).	
	IAN_CDIFFH_RANGE[1:0]	1:0	Peaking C Difference Horizontal Range (16/32/64/128).	
36D7h	REG36D7	7:0	Default : 0x00	Access : R/W
	YETP2D_VGAIN[3:0]	7:4	Y ETP2D VGain (V->2D).	
	YETP2D_HGAIN[3:0]	3:0	Y ETP2D HGain (H->2D).	
36D8h	REG36D8	7:0	Default : 0x00	Access : R/W
	CETP2D_VGAIN[3:0]	7:4	C ETP2D VGain (V->2D).	

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	CETP2D_HGAIN[3:0]	3:0	C ETP2D HGain (H->2D).	
36DAh	REG36DA	7:0	Default : 0x01	Access : R/W
	DBG_FP_MD[3:0]	7:4	Final Patch Debug Mode([3]: Debug Enable(1) [2:1]: VDiff(0)/HDiff(1)/Gain(2) [0]: Up(0)/Down(1)).	
	-	3:1	Reserved.	
	FINALPATCH_EN	0	Ian Final Patch Enable.	
36DBh	REG36DB	7:0	Default : 0x42	Access : R/W
	-	7	Reserved.	
	IAN_PLHDIFF_SC[2:0]	6:4	Ian PureLuma H-Diff Scale Select (mul 0/0.125/0.25/0.5/1/2/4/8).	
	-	3	Reserved.	
	IAN_PLHDIFF_TH[2:0]	2:0	Ian PureLuma H-Diff Threshold Select(32/64/128/256).	
36DCh	REG36DC	7:0	Default : 0x00	Access : R/W
	IAN_DIFF_SHIFTD[1:0]	7:6	Ian PureLuma D Diff Shift(div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_SHIFTU[1:0]	5:4	Ian PureLuma U Diff Shift(div 4/8/16/32) after TH (8~=32 inC).	
	IAN_DIFF_MSHTD[1:0]	3:2	Ian PureLuma D Diff Shift(div 1/2/4/8) before TH.	
	IAN_DIFF_MSHTU[1:0]	1:0	Ian PureLuma U Diff Shift(div 1/2/4/8) before TH.	
36DDh	REG36DD	7:0	Default : 0x00	Access : R/W
	IAN_TH_VER[7:0]	7:0	Ian PureLuma TH_Ver (25): U/D Diff Threshold for Detection.	
36DEh	REG36DE	7:0	Default : 0x05	Access : R/W
	PLHDIFF_TH[7:0]	7:0	Pure Luma H difference threshold.	
36E0h	REG36E0	7:0	Default : 0x00	Access : RO
	HSLOCK	7	HSync lock happen.	
	LOCK3D	6	Good timing happen.	
	MEMRDBWEVN	5	Memory Rd Bandwidth Evn.	
	MEMWRBWEVN	4	Memory Wr Bandwidth Evn.	
	NOTHSLOCK	3	HSync unlock happen.	
	NOTLOCK3D	2	Good timing disappear.	
	HSCHG	1	H-Sync counter change.	
	MEMBWEVN	0	DRAM bandwidth not enough.	
36E1h	REG36E1	7:0	Default : 0x00	Access : RO

COMB Register (Bank = 36)				
Index	Mnemonic	Bit	Description	
	STLIMG	7	Still image happen.	
	NOTSTLIMG	6	Still image disappear.	
	CCHNLACT	5	C-channel active(maybe S-video input).	
	NOTCCHNLACT	4	C-channel quiet(maybe CVBS input).	
	-	3	Reserved.	
	FLDCNTCHG	2	Field counter change.	
	-	1:0	Reserved.	
36E2h	REG36E2	7:0	Default : 0x00	Access : RO
	LN525	7	525 line system.	
	LN625	6	625 line system.	
	F358	5	3.58 MHz system.	
	F443	4	4.43 MHz system.	
	NOINPUT	3	No input.	
	VDOMD[2:0]	2:0	Video mode. 0: NTSC_M. 1: NTSC_443. 2: PAL_M. 3: PAL_BDGHIN. 4: PAL_Nc. 5: PAL_60. 6: Input without burst. 7: Unknown.	
36E3h	REG36E3	7:0	Default : 0x00	Access : RO
	-	7:1	Reserved.	
	INTERLACE	0	INTERLACE input.	
36E4h	REG36E4	7:0	Default : 0x00	Access : RO
	DETBANK[7:0]	7:0	Detected blank level.	
36E5h	REG36E5	7:0	Default : 0x00	Access : RO
	CURBLANK[7:0]	7:0	Current used blank level.	
36E6h	REG36E6	7:0	Default : 0x00	Access : RO
	SYNCLVL[7:0]	7:0	Detected sync level.	
36E7h	REG36E7	7:0	Default : 0x00	Access : RO
	SYNCHGHT[7:0]	7:0	Detected sync height.	
36E8h	REG36E8	7:0	Default : 0x00	Access : RO
	BURSTHGHT[7:0]	7:0	Detected burst height.	

COMB Register (Bank = 36)

Index	Mnemonic	Bit	Description
36E9h	REG36E9	7:0	Default : 0x00 Access : RO
	DETHORTOTAL_LOW[7:0]	7:0	Detected horizontal total(7:0).
36EAh	REG36EA	7:0	Default : 0x00 Access : RO
	DETHORTOTAL_HIGH[7:0]	7:0	Detected horizontal total(15:8).
36EBh	REG36EB	7:0	Default : 0x00 Access : RO
	RPTCOVFH[7:0]	7:0	Reported chroma overflow count per line.
36ECh	REG36EC	7:0	Default : 0x00 Access : RO
	RPTCOFV[7:0]	7:0	Reported chroma overflow count per field.
36F0h	-	7:0	Default : - Access : -
~ 36F4h	-	-	Reserved.

VBI Register (Bank = 37)

VBI Register (Bank = 37)				
Index	Mnemonic	Bit	Description	
01h ~ 0Fh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
10h	REG10	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	TTDECRST	1	Teletext decoder software reset.	
	TTEN	0	Teletext enable. 0: Disable. 1: Enable.	
11h	REG11	7:0	Default : 0xFF	Access : R/W
	DMASRC_ADR_7_0	7:0	DMA source linear address (lower 8 bits).	
12h	REG12	7:0	Default : 0xFF	Access : R/W
	DMASRC_ADR_15_8	7:0	DMA source linear address (middle 8 bits).	
13h	REG13	7:0	Default : 0xFF	Access : R/W
	DMASRC_ADR_23_16	7:0	DMA source linear address (upper 8 bits).	
14h	REG14	7:0	Default : 0xFF	Access : R/W
	DMADES_ADR_7_0	7:0	DMA destination linear address (lower 8 bits).	
15h	REG15	7:0	Default : 0xFF	Access : R/W
	DMADES_ADR_15_8	7:0	DMA destination linear address (middle 8 bits).	
16h	REG16	7:0	Default : 0xFF	Access : R/W
	DMADES_ADR_23_16	7:0	DMA destination linear address (upper 8 bits).	
17h	REG17	7:0	Default : 0x00	Access : R/W
	DMAQW_CNT_7_0	7:0	DMA block move count (unit: 8 bytes; lower 8 bits).	
18h	REG18	7:0	Default : 0x00	Access : R/W
	DMAQW_CNT_15_8	7:0	DMA block move count (unit: 8 bytes; upper 8 bits).	
19h	REG19	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	DMA_FUNC	4:0	DMA function.	
1Ah	REG1A	7:0	Default : 0x00	Access : RO, WO
	-	7:2	Reserved.	
	DMA_RDY	1	DMA ready status.	
	DMA_FIRE	0	DMA engine fire signal.	
1Bh	REG1B	7:0	Default : 0x20	Access : R/W
	DMAERASE_DAT	7:0	DMA erase data.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
1Ch	REG1C	7:0	Default : 0x00
	-	7:3	Reserved.
	TAG_INT_EN	2	Tag interrupt enable.
	DMA_INT_EN	1	DMA interrupt enable.
	VBI_INT_EN	0	VBI interrupt enable.
1Eh	REG1E	7:0	Default : 0xFF
	DMA_WBE_PRE	7:4	DMA previous write byte enable.
	DMA_WBE_POST	3:0	DMA post write byte enable.
1Fh	REG1F	7:0	Default : 0x00
	-	7:4	Reserved.
	DC_RAW	3	Designation code raw data mode.
	VBI_HEADER_RAW	2	VBI header raw data mode.
	VBI_ALL_RAW	1	VBI data raw data mode.
	SRH_ENG_CLEAR	0	Tag search engine clear.
20h	REG20	7:0	Default : -
	VBIREADY	7	VBI line end and teletext slicer ready indication.
	-	6:5	Reserved.
	VBI_LN_CNT	4:0	VBI line counter.
21h	REG21	7:0	Default : -
	TTSLICERRDY	7	Teletext slicer ready indication.
	VBI_FIELD_CNT_6_0	6:0	VBI field counter.
22h	REG22	7:0	Default : 0x00
	BURST_RE_MD	7	Burst read mode enable.
	BURST_WE_MD	6	Burst write mode enable.
	MCU_ADR_PORT	5:0	MCU memory access address port.
23h	REG23	7:0	Default : 0x00
	MCU_DATA_PORT	7:0	MCU memory access data port.
24h	REG24	7:0	Default : 0x00
	TAGRW_POS_7_0	7:0	Tag read/write position (lower 8 bits).
25h	REG25	7:0	Default : 0x00
	TAG_PT_DELTA32	7:4	Tag length 32 delta.
	TAGRW_POS_11_8	3:0	Tag read/write position (upper 4 bits).
26h	REG26	7:0	Default : -
	PAGEBUF_ADDR_7_0	7:0	Page buffer linear address (lower 8 bits).

VBI Register (Bank = 37)				
Index	Mnemonic	Bit	Description	
27h	REG27	7:0	Default : -	Access : RO
	PAGEBUF_ADDR_15_8	7:0	Page buffer linear address (middle 8 bits).	
28h	REG28	7:0	Default : -	Access : RO
	PAGEBUF_ADDR_23_16	7:0	Page buffer linear address (upper 8 bits).	
29h	REG29	7:0	Default : 0x00	Access : R/W
	PAGEBUF_CNT_7_0	7:0	Pager buffer counter (lower 8 bits).	
2Ah	REG2A	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	PAGEBUF_CNT_11_8	3:0	Pager buffer counter (upper 4 bits).	
2Bh	REG2B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	FW_SEARCH_SEL	3	MCU memory access data switch to FW search result data.	
	CYC_DISABLE	2	Disable cyclic search when touch physical size.	
	SEARCH_NOSUB	1	Search without sub-code.	
	REQ_64	0	The length of search request. 0->32; 1->64.	
2Ch	REG2C	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	MAGAZINE	3:0	Magazine.	
2Dh	REG2D	7:0	Default : 0x00	Access : R/W
	PAGE_TENS	7:4	Page number tens.	
	PAGE_UNITS	3:0	Page number units.	
2Eh	REG2E	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SUB_CODE4	5:4	Sub-code S4.	
	SUB_CODE3	3:0	Sub-code S3.	
2Fh	REG2F	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	SUB_CODE2	6:4	Sub-code S2.	
	SUB_CODE1	3:0	Sub-code S1.	
30h	REG30	7:0	Default : 0xFF	Access : R/W
	TAG_BASE_15_8	7:0	Tag base address.	
31h	REG31	7:0	Default : 0xFF	Access : R/W
	TAG_BASE_23_16	7:0	Tag base address.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
32h	REG32	7:0	Default : 0xFF Access : R/W
	PAGE_BASE_15_8	7:0	Page base address.
33h	REG33	7:0	Default : 0xFF Access : R/W
	PAGE_BASE_23_16	7:0	Page base address.
34h	REG34	7:0	Default : 0xFF Access : R/W
	PAGE_SIZE	7:0	One page size.
35h	REG35	7:0	Default : 0xFF Access : R/W
	TAG_PHY_SIZE	7:0	Tag physical size (lower 8 bits).
36h	REG36	7:0	Default : 0x0F Access : R/W
	-	7:4	Reserved.
	TAG_PHY_SIZE_11_8	3:0	Tag physical size (upper 4 bits).
37h	REG37	7:0	Default : 0x00 Access : RO, WO
	-	7:4	Reserved.
	BUF_ADDR_RDY	3	Page buffer linear address ready.
	HIT_STS	2	Search hit status.
	TAG_RDY	1	Tag ready status.
	TAG_FIRE	0	Tag engine fire signal.
38h	REG38	7:0	Default : 0x00 Access : R/W
	TTBASEADDR2_7_0	7:0	Teletext base address 2 (lower 8 bits).
39h	REG39	7:0	Default : 0xFF Access : R/W
	TTBASEADDR2_15_8	7:0	Teletext base address 2 (middle 8 bits).
3Ah	REG3A	7:0	Default : 0xFF Access : R/W
	TTBASEADDR2_23_16	7:0	Teletext base address 2 (upper 8 bits).
3Bh	REG3B	7:0	Default : 0x12 Access : R/W
	TTVBIBUFLEN_7_0	7:0	Teletext VBI buffer length (lower 8 bits).
3Ch	REG3C	7:0	Default : 0x00 Access : R/W
	TTVBIBUFLEN_15_8	7:0	Teletext VBI buffer length (upper 8 bits).
3Dh	REG3D	7:0	Default : - Access : RO
	TTPKTCNT_7_0	7:0	Teletext packet counter (lower 8 bits).
3Eh	REG3E	7:0	Default : - Access : RO
	TTPKTCNT_15_8	7:0	Teletext packet counter (upper 8 bits).
40h	REG40	7:0	Default : 0x21 Access : R/W
	CRIAMPTHDL_9_8	7:6	Closed caption clock run-in amplitude L (upper 2 bits).
	CCLNSTR1_4_3	5:4	Closed caption line start 1 (upper 2 bits).

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
	CRIDETENNUM_10_8	3:1	Closed caption clock run-in detection enable number (upper 3 bits).
	SLCTHDMD	0	Closed caption slicer threshold mode.
41h	REG41	7:0	Default : 0x52 Access : R/W
	CCLNSTR1_2_0	7:5	Closed caption line start 1 (lower 3 bits).
	CCLNEND1	4:0	Closed caption line end 1.
42h	REG42	7:0	Default : 0x1C Access : R/W
	CCINTTYPE	7	Closed caption interrupt type. 0: Assert 8T after CC line in even field if CC is found. 1: According to CCREQ.
	-	6:0	Reserved.
43h	REG43	7:0	Default : 0xA8 Access : R/W
	CRIDETENNUM_7_0	7:0	Closed caption clock run-un detection enable number (lower 8 bits).
44h	-	7:0	Default : - Access : -
	-	7:0	Reserved.
45h	REG45	7:0	Default : 0xA0 Access : R/W
	CRIAMPTHDL_7_0	7:0	Closed caption clock run-in amplitude L (lower 8 bits).
46h	REG46	7:0	Default : 0x00 Access : R/W
	-	7:6	Reserved.
	CCFRAMTRIGNUM_4_0	5:1	Closed caption frame trigger number. This controls CCFRAMTRIG (VBI_IRQ_STS[3]). When CCFRAMCNT == CCFRAMTRIGNUM, CCFRAMTRIG would be asserted.
	CCEN	0	Closed caption enable.
47h ~ 4Eh	-	7:0	Default : - Access : -
	-	7:0	Reserved.
4Fh	REG4F	7:0	Default : 0xF8 Access : R/W
	CRIAMPTHDH_7_0	7:0	Closed caption clock run-in amplitude upper threshold (lower 8 bits).
50h	REG50	7:0	Default : 0x72 Access : R/W
	CRIAMPTHDH_9_8	7:6	Closed caption clock run-in amplitude upper threshold (upper 2 bits).
	CCCRIZCTYPE	5	Closed caption CRI zero crossing type. 1: positive edge ; 0: negative edge.

VBI Register (Bank = 37)				
Index	Mnemonic	Bit	Description	
	CCLNSTR2	4:0	Closed caption line start 2.	
51h	REG51	7:0	Default : 0xB2	Access : R/W
	-	7:5	Reserved.	
	CCLNEND2	4:0	Closed caption line end 2.	
52h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
53h	REG53	7:0	Default : 0x90	Access : R/W
	CCSCWINLEN	7:0	Closed caption start code checking window length.	
54h	REG54	7:0	Default : 0x04	Access : R/W
	-	7:6	Reserved.	
	CCSTRCODEMSK	5:3	Closed caption start code mask. 1: mask(ignore) ; 0: normal.	
	CCSTRCODE	2:0	Closed caption start code.	
55h	REG55	7:0	Default : -	Access : RO
	-	7:2	Reserved.	
	CCBYTEERRH	1	Closed caption byte error (upper part).	
	CCBYTEERRL	0	Closed caption byte error (lower part).	
56h	REG56	7:0	Default : -	Access : RO
	CCODDFFOUND	7	Closed caption odd byte found indication.	
	CCEVEFOUND	6	Closed caption even byte found indication.	
	-	5	Reserved.	
	CCFRAMCNT	4:0	Closed caption frame counter.	
57h	REG57	7:0	Default : -	Access : RO
	CCBYTES_7_0	7:0	Closed caption bytes (lower 8 bits).	
58h	REG58	7:0	Default : -	Access : RO
	CCBYTES_15_8	7:0	Closed caption bytes (upper 8 bits).	
5Bh	REG5B	7:0	Default : -	Access : RO
	CC_PACKET_COUNTER	7:0	Closed caption packet counter.	
5Ch	REG5C	7:0	Default : 0x0F	Access : R/W
	-	7	Reserved.	
	CCBUFLEN	6:0	Closed caption buffer length.	
5Dh	REG5D	7:0	Default : 0xFF	Access : R/W
	CCBASEADDR_23_16	7:0	Closed caption base address (upper 8 bits).	
5Eh	REG5E	7:0	Default : 0xFF	Access : R/W

VBI Register (Bank = 37)				
Index	Mnemonic	Bit	Description	
	CCBASEADDR_15_8	7:0	Closed caption base address (middle 8 bits).	
5Fh	REG5F	7:0	Default : 0xFF	Access : R/W
	CCBASEADDR_7_0	7:0	Closed caption base address (lower 8 bits).	
68h ~ 69h	-	7:0	Default : -	Access : -
	-	7:0	-	
6Ah	REG6A	7:0	Default : 0x05	Access : R/W
	-	7:5	Reserved.	
	TT2KPM	4:3	Teletext two KP mode. 00, 01: Disable. 10: Using 2nd KP value when the difference of TTINTP zero crossing value is smaller than TTINPTZXTH each line. 11: Using 2nd KP value when the difference of TTINTP zero crossing value is smaller than TTINPTZXTH each field.	
	TTKPSL2ND	2:0	Teletext DPLL phase error gain selection 2nd parameter. 000: 2 ⁻⁹ . 001: 2 ⁻¹⁰ . 010: 2 ⁻¹¹ . 011: 2 ⁻¹² . 100: 2 ⁻¹³ . 101: 2 ⁻¹⁴ . 110: 2 ⁻¹⁵ . 111: 2 ⁻¹⁶ .	
6Bh	REG6B	7:0	Default : 0x00	Access : R/W
	VBI_IRQ_FORCE	7:0	VBI interrupt request force bits.	
6Ch	REG6C	7:0	Default : 0xFF	Access : R/W
	VBI_IRQ_MSK	7:0	VBI interrupt request mask bits.	
6Dh	REG6D	7:0	Default : 0x00	Access : R/W
	VBI_IRQ_CLR	7:0	VBI interrupt request clear bits.	
6Eh	REG6E	7:0	Default : -	Access : RO
	VBI_IRQ_STS	7:0	VBI interrupt request status report.	
6Fh	-	7:0	Default : -	Access : -
	-	7:0	-	
70h	REG70	7:0	Default : 0x00	Access : R/W
	VPS_WSS_EN	7	VPS/WSS enable.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
			0: Disable. 1: Enable.
	VPS_EACHFLD	6	VPS each field option. 0: Only detect in odd field. 1: Detect in odd and even field.
	WSS_EACHFLD	5	WSS each field option. 0: Only detect in odd field. 1: Detect in odd and even field.
	-	4	Reserved.
	VBI_RST	3	VBI software reset.
	TTINTTYPE	2:1	Teletext interrupt type. [1]: 0: Assert 8T cycle. 1: Wait TTX_INTACK to clear the assertion. [0]: 0: Interrupt is issued when Teletext slicer is ready after Teletext available lines. 1: Interrupt is issued after Teletext available lines no matter whether there is Teletext data.
	TTEN2	0	Teletext forced enable bit. Teletext function could be enabled by two ways. The formal way is enabled from internal MCU and stable VD state is necessary. The other way is enabled by this bit directly.
71h	REG71	7:0	Default : 0xA0Access : R/W
	TT_INI_CRIWIN_STRPT	7:0	Teletext initial state clock run-in window start point (lower 7 bits).
72h	REG72	7:0	Default : 0x3CAccess : R/W
	-	7:6	Reserved.
	TT_LN_UPD_DEF	5	Teletext line default update enable.
	TT_LN_UPD_REG335	4	Teletext line 335 update enable.
	TT_LNUPD_REG318	3	Teletext line 318 update enable.
	TT_LNUPD_REG22	2	Teletext line 22 update enable.
	TT_CRIWIN_MD	1	Teletext clock run-in window mode. 0: Teletext clock run-in start-point and end-point are using TT_INI_CRIWIN_STRPT and TT_INI_CRIWIN_ENDPT in initial state and TT_SDY_CRIWIN_STRPT and TT_SDY_CRIWIN_ENDPT in steady state.

VBI Register (Bank = 37)				
Index	Mnemonic	Bit	Description	
			1: Teletext clock run-in start-point and end-point are always using TT_INI_CRIWIN_STRPT and TT_INI_CRIWIN_ENDPT.	
	TT_INI_CRIWIN_STRPT	0	Teletext initial clock run-in window start point (MSB).	
73h	REG73	7:0	Default : 0xFF	Access : R/W
	TT_LN_UPDREG06_13	7:0	Teletext line 6 to 13 (bit 7 to 0) update enable.	
74h	REG74	7:0	Default : 0xFF	Access : R/W
	TT_LN_UPDREG14_21	7:0	Teletext line 14 to 21 (bit 7 to 0) update enable.	
75h	REG75	7:0	Default : 0xFF	Access : R/W
	TT_LN_UPDREG319_326	7:0	Teletext line 319 to 326 (bit 7 to 0) update enable.	
76h	REG76	7:0	Default : 0xFF	Access : R/W
	TT_LN_UPDREG327_334	7:0	Teletext line 327 to 334 (bit 7 to 0) update enable.	
77h	REG77	7:0	Default : 0x26	Access : R/W
	TT_CRI_AMP_ACC_PT	7:0	Teletext clock run-in amplitude accumulation start point.	
78h	REG78	7:0	Default : 0x01	Access : R/W
	TT_DPLL_PT	7:0	Teletext DPLL start point.	
79h	REG79	7:0	Default : 0x7D	Access : R/W
	TT_BLK_LVL_PT	7:0	Teletext blank level accumulation start point.	
7Ah	REG7A	7:0	Default : 0xCF	Access : R/W
	TT_VBI_LNEND_4_3	7:6	Teletext VBI line end (upper 2 bits). It is used to generate a notice signal to TTDEC_TOP to indicate Teletext data is received in this field.	
	TT_DPLL_EN_LEN	5:0	Teletext DPLL enable length.	
7Bh	REG7B	7:0	Default : 0x27	Access : R/W
	TT_FRAM_CODE	7:0	Teletext framing code value.	
7Ch	REG7C	7:0	Default : 0x06	Access : R/W
	TT_VBI_LNEND_2_0	7:5	Teletext VBI line end (lower 3 bits).	
	TT_DAT_LN_STR1	4:0	Teletext data line start 1 (odd field).	
7Dh	REG7D	7:0	Default : 0x16	Access : R/W
	TT_FC_WIN_MD	7	Teletext framing code window mode. This is valid when TT_CRIWIN_MD = 1.	
	TT_FC_ERR_BOND	6	Teletext framing code error bond value. 0: Fully match framing code. 1: Allow 1 error in framing code.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
	TT_SLICER_RDY_MD	5	Teletext slicer ready mode. 0: Teletext slicer is ready when TT_FCC_NT >= TT_FCC_NT_THD at TT_CHK_PT. 1: Teletext slicer is ready when TT_FCC_NT >= TT_FCC_NT_THD.
	TT_DAT_LNEND1	4:0	Teletext data line end 1 (odd field).
7Eh	REG7E	7:0	Default : 0x85 Access : R/W
	TT_INIT_PKT_EN	7	Teletext initial packet counter enable. 0: Packet counter increases when Teletext packet is detected with upper-bound (TT_VBI_BUF_LEN). 1: Packet counter increases when Teletext packet is detected without upper-bound.
	-	6:5	Reserved.
	TT_DAT_LN_STR2	4:0	Teletext data line start 2 (even field).
7Fh	REG7F	7:0	Default : 0xF6 Access : R/W
	TT_BASE_ADDR_SEL	7	Teletext base address source selection.
	TT_SL_PT_MD	6:5	Teletext single line point mode. [1]: 0: Start from TT_DAT_LINE_STRL. 1: Start from the line when previous line is no Teletext. [0]: 0: Disable TT_SL_PT_MD. 1: Enable TT_SL_PT_MD.
	TT_DAT_LN_END2	4:0	Teletext data line end 2 (even field).
80h	REG80	7:0	Default : 0x54 Access : R/W
	TT_KP_SELMAN	7:5	Teletext DPLL phase error gain parameter selection. 000: 2 ⁻⁹ . 001: 2 ⁻¹⁰ . 010: 2 ⁻¹¹ . 011: 2 ⁻¹² . 100: 2 ⁻¹³ . 101: 2 ⁻¹⁴ . 110: 2 ⁻¹⁵ . 111: 2 ⁻¹⁶ .
	TT_BLK_LVL_MD	4	Teletext blank level mode. 0: Calculate blank level from TT_BLK_LVL_PT in the line set by TT_BLK_LVL_LN. 1: Calculate blank level in every line from TTBLKLVLPT.

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
	TT_BLK_LVL_LN	3:0	Teletext blank level line.
81h	REG81	7:0	Default : 0x37 Access : R/W
	TT_CRI_AMP_THD	7:0	Teletext clock run-in amplitude threshold.
82h	REG82	7:0	Default : 0x8E Access : R/W
	TT_PH_ACC_INC_NORM1_15_8	7:0	Teletext phase accumulated incremental normalized parameter 1, used in PAL.
83h	REG83	7:0	Default : 0x6B Access : R/W
	TT_PH_ACC_INC_NORM1_7_0	7:0	Teletext phase accumulated incremental normalized parameter 1, used in PAL.
84h	REG84	7:0	Default : 0x36 Access : R/W
	TT_INI_CRI_WIN_ENDPT_7_0	7:0	Teletext initial clock run-in window end point (lower 8 bits).
85h	REG85	7:0	Default : 0x80 Access : R/W
	TT_INI_CRI_WIN_ENDPT_8	7	Teletext initial clock run-in window end point (MSB).
	-	6:4	Reserved.
	TT_TESTBUS_SEL	3:0	VBI test bus data selection.
86h	REG86	7:0	Default : 0x8C Access : R/W
	TT_MU_CRIAMP	7:6	Teletext blending parameter for clock run-in amplitude. 00: 1/4. 01: 1/8. 10: 1/16. 11: 1/32.
	TT_CRI_WIN_LEN	5:0	Teletext clock run-in window length.
87h	REG87	7:0	Default : 0x19 Access : R/W
	TT_SLC_THD_TRKPT	7:0	Teletext slicer threshold track point. If TT_SLC_THD_ADPON = 1, slice threshold automatic tracking would be started after TT_SLC_THD_TRKPT.
88h	REG88	7:0	Default : 0xD5 Access : R/W
	-	7:5	Reserved.
	TT_SDY_FCMON_CNTTHD	4:0	Teletext line monitor counter threshold in steady state. TT_CHK_PT is at TT_DAT_LN_END when TT_MON_CNT = TT_SDY_FC_MON_CNT_THD.
89h	REG89	7:0	Default : 0xC1 Access : R/W
	TT_INI_TPKTSEL	7	Teletext packet receiving mode selection. 0: Refresh when the field changes. 1: Refresh when reaching TTVBIBUFLEN.

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	TT_PH_ACC_MD	6	Teletext phase accumulation parameter mode. 0: Depend on SCM_FSC. 1: Depend on TTPHACCTYPE.	
	TT_PH_ACC_TYPE	5	0: TT_PH_ACC_INC_NORM1 1: TT_PH_ACC_INC_NORM2.	
	TT_SRCH_FCCNT_THD	4:0	Teletext framing code counter threshold in search-FC state. If TTFCCNT were not over threshold, re-training would be ignited.	
8Ah	REG8A	7:0	Default : 0x31	Access : R/W
	-	7	Reserved.	
	TT_CRI_AMP_HALF_HLMT_9_8	6:5	Teletext CRI half amplitude high limit (upper 2 bits).	
	TT_SDY_FCCNT_THD	4:0	Teletext framing code counter threshold in steady state. If TTFCCNT were not over threshold, re-training would be ignited.	
8Bh	REG8B	7:0	Default : 0x04	Access : R/W
	-	7:5	Reserved.	
	TT_SRCH_FCMON_CNTTHD	4:0	Teletext line monitor counter threshold in search-FC state. TT_CHK_PT is at TT_DAT_LN_END when TT_MON_CNT = TT_SRCH_FC_MON_CNT_THD.	
8Ch	REG8C	7:0	Default : 0x9A	Access : R/W
	TT_MUCRI_FOUND_PT	7:6	Teletext blending parameter for clock run-in found point. 00: 1/2. 01: 1/4. 10: 1/8. 11: 1/16.	
	-	5:4	Reserved.	
	TT_FAST_DPLL_ACQ_ON	3	Teletext fast DPLL acquisition on.	
	TT_SYMB_INTP_BASE	2:0	Teletext symbol interpolation base.	
8Dh	REG8D	7:0	Default : 0xE5	Access : R/W
	TT_SLC_THD_ADPON	7	Teletext slicer threshold adaptation on.	
	TT_SIG_DET_SEL	6	Teletext signal detection type selection. 0: TT_SLC_THD is based on TT_BLK_LVL + TT_CRI_AMP_VAL_HALF, which are average values after accumulation. TT_CRI_FOUND is base on mode0. 1: TT_SLC_THD is based on CC_DIN1_2FSC with error adjustment. TT_CRI_FOUND is based on mode1.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description	
	TT_MU_SLC_THD_ERR	5:4	Teletext slicer threshold error parameter selection, useful when TT_SIG_DET_SEL = 1. 00: ¼. 01: 1/8. 10: 1/16. 11: 1/32.	
	TT_SLC_THD_LAT_SEL	3:2	Teletext slicer threshold latch selection. Select delay point of CC_DIN1_2FSC for slice threshold. 00: 0. 01: 1. 10: 2. 11: 3.	
	TT_BLK_LVL_LAT_SEL	1:0	Teletext blank level latch selection. Select delay point of CCDIN1_2FSC for blank level. 00: 12. 01: 11. 10: 10. 11: 9.	
8Eh	REG8E	7:0	Default : 0x78	Access : R/W
	TT_PH_ACC_INC_NORM2_15_8	7:0	Teletext phase accumulated incremental normalized parameter 2, used in SECAM.	
8Fh	REG8F	7:0	Default : 0x81	Access : R/W
	TT_PH_ACC_INC_NORM2_7_0	7:0	Teletext phase accumulated incremental normalized parameter 2, used in SECAM.	
90h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
91h	REG91	7:0	Default : 0x50	Access : R/W
	TTLN_CNTRFLD_THD_9_8	7:6	Teletext line counter folded threshold (upper 2 bits).	
	TT_CRI_DET_SEL	5	0: The same as TT_SIG_DET_SEL setting. 1: Inversion of TT_SIG_DET_SEL setting.	
	VPS_DAT_LN_STR	4:0	VPS data line start definition.	
92h	REG92	7:0	Default : 0x30	Access : R/W
	-	7	Reserved.	
	VPS_CRI_WIN_ENDPT_9_8	6:5	VPS clock run-in window end point (upper 2 bits).	
	VPS_DAT_LN_END	4:0	VPS data line end definition.	
93h	REG93	7:0	Default : 0xA3	Access : R/W
	VPS_CRI_WIN_STRPT	7:0	VPS clock run-in window start point.	

VBI Register (Bank = 37)				
Index	Mnemonic	Bit	Description	
94h	REG94	7:0	Default : 0x86	Access : R/W
	VPS_CRI_WIN_ENDPT_7_0	7:0	VPS clock run-in window end point (lower 7 bits).	
95h	REG95	7:0	Default : 0x36	Access : R/W
	VPS_SLC_THDPT	7:0	VPS start point for slicer threshold calculation.	
96h	REG96	7:0	Default : 0x14	Access : R/W
	VPS_DPLLPT	7:0	VPS DPLL start point.	
97h	REG97	7:0	Default : 0x0F	Access : R/W
	TT_FC_WIN_ENDPT_9_8	7:6	Teletext framing code window end point (upper 2 bits).	
	VPS_DPLL_ENLEN	5:0	VPS DPLL enable length.	
98h	REG98	7:0	Default : 0x37	Access : R/W
	VPS_CRI_AMP_THD	7:0	VPS clock run-in amplitude threshold.	
99h	REG99	7:0	Default : 0x8C	Access : R/W
	VPS_PH_ACC_INC_NORM_15_8	7:0	VPS phase accumulation incremental normalized parameter.	
9Ah	REG9A	7:0	Default : 0x01	Access : R/W
	VPS_PH_ACC_INC_NORM_7_0	7:0	VPS phase accumulation incremental normalized parameter.	
9Bh ~ 9Ch	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
9Dh	REG9D	7:0	Default : 0x00	Access : R/W
	TT_BASE_ADDR1_7_0	7:0	Teletext base address 1 (lower 8 bits).	
9Eh	REG9E	7:0	Default : 0xFF	Access : R/W
	TT_BASE_ADDR1_15_8	7:0	Teletext base address 1 (middle 8 bits).	
9Fh	REG9F	7:0	Default : 0xFF	Access : R/W
	TT_BASE_ADDR1_23_16	7:0	Teletext base address 1 (upper 8 bits).	
A0h	REGA0	7:0	Default : 0xAF	Access : R/W
	TT_FC_WIN_ENDPT_7_0	7:0	Teletext framing code window end point (lower 8 bits).	
A1h	REGA1	7:0	Default : 0x39	Access : R/W
	TTLN_CNTRFLD_THD_7_0	7:0	Teletext line counter folded threshold (lower 8 bits).	
A2h	REGA2	7:0	Default : 0x24	Access : R/W
	TT_CRIAMPHALFLMT	7:0	Teletext CRI half amplitude low limit.	
A3h	REGA3	7:0	Default : 0x2C	Access : R/W
	TT_CRI_AMP_HALF_HLMT_7_0	7:0	Teletext CRI half amplitude high limit (lower 8 bits).	
A5h	REGA5	7:0	Default : -	Access : RO

VBI Register (Bank = 37)				
Index	Mnemonic	Bit	Description	
	VPS_SC_CNT	7:4	VPS start code counter.	
	WSS_SC_CNT	3:0	WSS start code counter.	
A6h	REGA6	7:0	Default : -	Access : RO
	VPS_BYTE3	7:0	VPS byte 3, which is the received byte set by VPS_BYTE_IDX3.	
A7h	REGA7	7:0	Default : -	Access : RO
	VPS_BYTE4	7:0	VPS byte 4, which is the received byte set by VPS_BYTE_IDX4.	
A8h	-	7:0	Default : -	Access : *
	*	7:0	Reserved.	
A9h	REGA9	7:0	Default : -	Access : RO
	TT_PKT_CNT2_7_0	7:0	Teletext packet counter (lower 8 bits).	
AAh	REGAA	7:0	Default : -	Access : RO
	TT_PKT_CNT2_15_8	7:0	Teletext packet counter (upper 8 bits).	
ABh	REGAB	7:0	Default : -	Access : RO
	-	7:4	Reserved.	
	TT_FLD_CNT	3:0	Teletext field counter.	
ACh	REGAC	7:0	Default : -	Access : RO
	VPS_BIT_BIPH_ERR_CNT1	7:4	VPS bit bi-phase error counter 1 (index 1 byte).	
	VPS_BIT_BIPH_ERRCNT2	3:0	VPS bit bi-phase error counter 2 (Index 2 byte).	
ADh	REGAD	7:0	Default : -	Access : RO
	VPS_BYTE1	7:0	VPS byte 1, which is the received byte set by VPS_BYTE_IDX1.	
AEh	REGAE	7:0	Default : -	Access : RO
	VPS_BYTE2	7:0	VPS byte 2, which is the received byte set by VPS_BYTE_IDX2.	
AFh	REGAF	7:0	Default : -	Access : RO
	WSS_SC_STS	7	WSS start code status. 1 when WSS_SC_CNT >= WSS_SC_REAL_CNT_THD, set by WSS_SDY_SC_REAL_CNT_THD or WSS_PULL_SC_REAL_CNT_THD.	
	WSS_SLICER_RDY	6	WSS slicer ready indication.	
	-	5	Reserved.	
	VPS_SLICER_RDY	4	VPS slicer ready indication. 1 when VPS_SC_CNT >= VPS_SC_CNT_THD, set by VPS_SRCH_SC_CNT_THD	

VBI Register (Bank = 37)				
Index	Mnemonic	Bit	Description	
			or VPS_SDY_SC_CNT_THD, and VPS_ state is steady.	
	-	3:2	Reserved.	
	TT_SLICER_RDY2	1	Teletext slicer ready indication. 1 when TT_FC_CNT >= TT_FC_CNT_THD at TT_CHK_PT and TT_STATE is steady.	
	-	0	Reserved.	
B0h	REGB0	7:0	Default : -	Access : RO
	TT_BLK_LVL_9_2	7:0	Teletext blank level.	
B1h	REGB1	7:0	Default : -	Access : RO
	TT_SLC_THD_9_2	7:0	Teletext slicer threshold.	
B2h	REGB2	7:0	Default : 0x8A	Access : R/W
	VPS_STR_CODE_15_8	7:0	VPS start code (upper 8 bits).	
B3h	REGB3	7:0	Default : 0x99	Access : R/W
	VPS_STRCODE_7_0	7:0	VPS start code (lower 8 bits).	
B4h	REGB4	7:0	Default : 0x45	Access : R/W
	VPS_KPSEL_MAN	7:5	VPS DPLL gain parameter selection. 000: 2 ⁻⁹ . 001: 2 ⁻¹⁰ . 010: 2 ⁻¹¹ . 011: 2 ⁻¹² . 100: 2 ⁻¹³ . 101: 2 ⁻¹⁴ . 110: 2 ⁻¹⁵ . 111: 2 ⁻¹⁶ .	
	VPS_SRCH_SC_CNT_THD	4:0	VPS search start code counter threshold. Refer to VPS_SLICER_RDY.	
B5h	REGB5	7:0	Default : 0x65	Access : R/W
	VPS_SYMB_INTP_BASE	7:5	VPS symbol interpolation base.	
	VPS_SDY_SC_CNT_THD	4:0	VPS steady state start code counter threshold. Refer to VPS_SLICER_RDY.	
B6h	REGB6	7:0	Default : 0xB5	Access : R/W
	VPS_BYTE_IDX4	7:4	VPS byte index 4.	
	VPS_BYTE_IDX3	3:0	VPS byte index 3.	
B7h	REGB7	7:0	Default : 0xED	Access : R/W
	VPS_BYTE_IDX2	7:4	VPS byte index 2.	
	VPS_BYTE_IDX1	3:0	VPS byte index 1.	

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
B8h	REGB8	7:0	Default : 0x4F Access : R/W
	VPS_SC_WIN_ENDPT_9_8	7:6	VPS start code window end point (upper 2 bits).
	VPS_INT_TYPE	5	VPS interrupt type. 0: Issue after VPS detection line if VPS slicer is ready. 1: Always issue after VPS detection line.
	WSS_INT_TYPE	4	WSS interrupt type. 0: Issue after WSS detection line if WSS slicer is ready. 1: Always issue after WSS detection line.
	VPS_BYTENUM	3:0	VPS byte number.
B9h	REGB9	7:0	Default : 0x7D Access : R/W
	VW_BLK_LVL_PT	7:0	VPS / WSS start point for blank level calculation.
BAh	REGBA	7:0	Default : 0x63 Access : R/W
	VPS_SC_WIN_ENDPT_7_0	7:0	VPS / WSS start code window end point (lower 8 bits).
BBh	REGBB	7:0	Default : 0x0A Access : R/W
	-	7:6	Reserved.
	WSS_DATA_CHK_OP	5	WSS data check option. 0: No checking data difference. 1: Checking data difference.
	VPS_SDY_SC_MON_CNT_THD	4:0	VPS steady state start code monitor counter threshold.
BCh	REGBC	7:0	Default : 0x60 Access : R/W
	WSS525_SYMB_INTP_BASE	7:0	WSS symbol interpolation base for NTSC 525-line system.
BDh	REGBD	7:0	Default : 0x00 Access : R/W
	WSS525_PH_ACCINC	7:0	WSS phase accumulation incremental parameter for NTSC 525-line system.
BEh	REGBE	7:0	Default : 0x78 Access : R/W
	WSS_CRI_AMPTHD_N	7:0	WSS clock run-in amplitude threshold for NTSC 525-line system.
BFh	REGBF	7:0	Default : 0x58 Access : R/W
	NP_MD[1:0]	7:6	NTSC/PAL mode selection for debugging.
	WSS_BIT_ID_THRSD	5:0	WSS bit identification threshold for 525-line system. 1 bit equals 32 cycles at 4*Fsc.
C0h	REGCO	7:0	Default : 0x57 Access : R/W
	WSS_KPSELMAN	7:5	WSS DPLL gain parameter selection. 000: 2 ⁻⁹ . 001: 2 ⁻¹⁰ .

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
			010: 2 ⁻¹¹ . 011: 2 ⁻¹² . 100: 2 ⁻¹³ . 101: 2 ⁻¹⁴ . 110: 2 ⁻¹⁵ . 111: 2 ⁻¹⁶ .
	WSS_DATLNSTR_P	4:0	WSS data start line for PAL 625-line system.
C1h	REGC1	7:0	Default : 0xA3 Access : R/W
	WSS_CRI_WIN_STRPT	7:0	WSS clock run-in window start point.
C2h	REGC2	7:0	Default : 0x9C Access : R/W
	WSS_CRI_WIN_ENDPT_7_0	7:0	WSS clock run-in window end point (lower 8 bits).
C3h	REGC3	7:0	Default : 0x4B Access : R/W
	WSS_CRI_WIN_ENDPT_9_8	7:6	WSS clock run-in window end point (upper 2 bits).
	WSS_DPLL_ENLEN[5:0]	5:0	WSS DPLL enable length.
C4h	REGC4	7:0	Default : 0x32 Access : R/W
	WSS_SLC_THD_EN_ENDPT	7:0	WSS slicer threshold enable end point.
C5h	REGC5	7:0	Default : 0x78 Access : R/W
	WSS_CRI_AMP_THD_P	7:0	WSS clock run-in amplitude threshold for PAL 625-line system.
C6h	REGC6	7:0	Default : 0xB8 Access : R/W
	WSS_SC_WIN_ENDPT_7_0	7:0	WSS start code window end point (lower 8 bits).
C7h	REGC7	7:0	Default : 0x1E Access : R/W
	WSS_STR_CODE_23_16	7:0	WSS start code (upper 8 elements).
C8h	REGC8	7:0	Default : 0x3C Access : R/W
	WSS_STR_CODE_15_8	7:0	WSS start code (middle 8 elements).
C9h	REGC9	7:0	Default : 0x1F Access : R/W
	WSS_STR_CODE_7_0	7:0	WSS start code (lower 8 elements).
CAh	REGCA	7:0	Default : 0x42 Access : R/W
	WSS_PULL_SC_MON_CNT_THD	7:4	WSS pull-in state start code monitor counter threshold.
	WSS_PULL_SC_REAL_CNT_THD	3:0	WSS pull-in state start code real counter threshold.
CBh	REGCB	7:0	Default : 0xC8 Access : R/W
	WSS_SDY_SC_MON_CNT_THD	7:4	WSS steady state start code monitor counter threshold.
	WSS_SDY_SC_REAL_CNT_THD	3:0	WSS steady state start code real counter threshold.
CCh	REGCC	7:0	Default : 0xBD Access : R/W

VBI Register (Bank = 37)

Index	Mnemonic	Bit	Description
	WSS_DAT_LNEND_P	7:3	WSS data end line for PAL 625-line system.
	WSS_STUS_CHK_OP	2	WSS status check option. 0: Original method. 1: Depend on WSS_SC_CHKPT.
	WSS_SC_WIN_ENDPT_9_8	1:0	WSS start code window end point (upper 2 bits).
CDh	REGCD	7:0	Default : - Access : RO
	WSS_WORD_7_0	7:0	WSS word (lower 8 bits).
CEh	REGCE	7:0	Default : - Access : RO
	WSS_WORD_15_8	7:0	WSS word (middle 8 bits).
CFh	REGCF	7:0	Default : - Access : RO
	-	7:4	Reserved.
	WSS_WORD_19_16	3:0	WSS word (upper 4 bits).

SECAM Register (Bank = 38)

SECAM Register (Bank = 38)				
Index	Mnemonic	Bit	Description	
01h	REG01	7:0	Default : 0x00	Access : R/W
	SCM_RST	7	SECAM software reset. 0: Normal operation. 1: Reset.	
	MIXC_EN	6	Chroma mixing enable. 0: Disable. 1: Enable according to settings of WFUNC_ISO and YDEV_THRSD.	
	WFUNC_ISO	5	Chroma weighting function isolation. 0: Normal. 1: Isolate asymmetric weighting.	
	SCM_RES_OP	4	SCM_RESULT report option. 0: Immediate. 1: During VBI.	
	-	3	Reserved.	
	ID_MD	2	Identification mode selection. Set to 1 only if using frame ID for SECAM detection in line 7~15 and line 320~328.	
	SCMID_OP	1	SECAM identification option. 0: Identification is on when VD state is stable. 1: Ignore VD state stable condition.	
	SCMID_EN	0	SECAM identification forced enable.	
02h	REG02	7:0	Default : 0x98	Access : R/W
	SAMPLE_STO_7_0	7:0	Start of sample point (lower 8 bits) for 4.43 MHz.	
03h	REG03	7:0	Default : 0xA4	Access : R/W
	SAMPLE_END0_7_0	7:0	End of sample point (lower 8 bits) for 4.43 MHz.	
04h	REG04	7:0	Default : 0x1B	Access : R/W
	LINE_STA	7:0	Start of line number of odd field.	
05h	REG05	7:0	Default : 0x54	Access : R/W
	LINE_STB_7_0	7:0	Start of line number of even field.	
06h	REG06	7:0	Default : 0x01	Access : R/W
	SAMPLE_STO_10_8	7:5	Start of sample point (upper 3 bits) for 4.43MHz.	
	SAMPLE_END0_10_8	4:2	End of sample point (upper 3 bits) for 4.43MHz.	
	LINE_STB_9_8	1:0	Start of line number of even field (upper 2 bits).	
07h	REG07	7:0	Default : 0xF0	Access : R/W

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description
	LINE_LEN0	7:0	Length of observation line for 4.43MHz.
08h	REG08	7:0	Default : 0x01 Access : R/W
	SCM_Y2Y601_BP	7	SECAM Y (Luma) to BT601 operation bypassing option.
	MAG_MD	6:5	00: Original value. 01: MAG_INT/2. 10: MAG_INT/8. 11: MAG/32.
	ID_CTR_MD	4:3	SECAM identification criterion mode. 00: Depend on magnitude difference. 01: Depend on magnitude and sign difference. 10: Depend on magnitude difference and sign flipping. 11: Depend on magnitude difference, sign difference, and sign flipping.
	ID_ACT_FIELD	2:0	Active field number of SECAM identification.
09h	REG09	7:0	Default : 0x60 Access : R/W
	MAG_THRSD44_7_0	7:0	Magnitude threshold for Fsc 4.43MHz (lower 8 bits).
0Ah	REG0A	7:0	Default : 0x21 Access : R/W
	MAG_THRSD44_15_8	7:0	Magnitude threshold for Fsc 4.43MHz (middle 8 bits).
0Bh	REG0B	7:0	Default : 0x40 Access : R/W
	-	7	Reserved.
	LINE_PIXNUM_10_8	6:4	Pixel number of line buffer (upper 3 bits).
	MAG_THRSD44_19_16	3:0	Magnitude threshold for Fsc 4.43MHz (upper 4 bits).
0Ch	REG0C	7:0	Default : 0x48 Access : R/W
	LINE_PIXNUM_7_0	7:0	Pixel number of line buffer (if the number is 1097, program 11'h448).
0Dh	REG0D	7:0	Default : 0x06 Access : R/W
	ID_THRSD	7:0	Threshold for SECAM identification.
0Eh	REG0E	7:0	Default : 0x88 Access : R/W
	NONSCM_THRSD	7:4	Non-SECAM decision threshold.
	SCM_THRSD	3:0	SECAM decision threshold.
0Fh	-	7:0	Default : - Access : -
	-	7:0	Reserved.
10h	REG10	7:0	Default : 0x00 Access : R/W
	MAG_THRSD42_7_0	7:0	Magnitude threshold for Fsc 4.285MHz (lower 8 bits).
11h	REG11	7:0	Default : 0x20 Access : R/W

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description
	MAG_THRSD42_15_8	7:0	Magnitude threshold for Fsc 4.285MHz (middle 8 bits).
12h	REG12	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	MAG_THRSD42_19_16	3:0	Magnitude threshold for Fsc 4.285MHz (upper 4 bits).
13h	REG13	7:0	Default : 0x08 Access : R/W
	MAG_DEV_THRSD_7_0	7:0	Magnitude deviation threshold for SECAM color-off detection (unsigned lower 8 bits).
14h	REG14	7:0	Default : 0x00 Access : R/W
	MAG_DEV_THRSD_15_8	7:0	Magnitude deviation threshold for SECAM color-off detection (unsigned upper 8 bits).
15h	REG15	7:0	Default : 0xFF Access : R/W
	HW_SCM_COFF_EN	7	Hardware SECAM color-off enable. 0: Disable ; 1: Enable.
	SCM_COFF_THRSD	6:0	Hardware SECAM color-off threshold (2 lines / unit).
16h ~ 18h	-	7:0	Default : - Access : -
	-	7:0	Reserved.
19h	REG19	7:0	Default : 0x03 Access : R/W
	SCM_BPYN	7	Bypass Y (Luma) notch filter option. 0: Normal mode. 1: Bypass mode.
	OBV_MD	6	Observation mode. 0: Field base. 1: Within one field.
	-	5:4	Reserved.
	SCMGCLK_OP	3	SECAM clock gating option. 0: Gate SECAM clock when operating at 3.58MHz(or not stable VD state). 1: No clock gating.
	CMBGCLK_OP	2	Comb clock gating option. 0: No clock gating. 1: Gate comb filter clock when SECAM decoder is operating.
	CLPMD[1:0]	1:0	Chroma LPF mode. 00: Bypass. 01: 1.5 MHz. 10: 1.25 MHz. 11: 1 MHz.

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description
1Ah ~ 1Dh	-	7:0	Default : - Access : -
	-	7:0	Reserved.
1Eh	REG1E	7:0	Default : 0x04 Access : R/W
	SCM_YSEP_FLTMD	7:6	Y separation filter selection. 00: Normal. 01: Medium. 10: Strong. 11: Reserved.
	-	5	Reserved.
	SCM_CBCRLPON	4	SECAM Cb/Cr LPF switch. 0: Off. 1: On.
	LUMAFIXMD	3	Luma Fix Mode. 0: Normal. 1: Luma is controlled by SDBK level.
	SCM_YDLYMD	2:0	SECAN Luma(Y) delay mode. 0: advance 4 ; 1: advance 3 ; 2: advance 2 ; 3: advance 1 ; 4: normal ; 5: delay 1 ; 6: delay 2 ; 7: delay 3.
1Fh	REG1F	7:0	Default : 0x30 Access : RO, R/W
	SCM_IRQ_FORCE	7:6	SECAM Interrupt force bits.
	SCM_IRQ_MSK	5:4	SECAM Interrupt mask bits.
	SCM_IRQ_CLR	3:2	SECAM Interrupt clear bits.
	SCM_IRQ_STS	1:0	SECAM Interrupt status bits.
20h	REG20	7:0	Default : 0x00 Access : R/W
	-	7:4	Reserved.
	SCMINTTYPE	3	SECAM interrupt type. 0: Issue when SECAM ID result changes. 1: Issue when detection related data updates.
	-	2:0	Reserved.
21h ~ 24h	-	7:0	Default : - Access : -
	-	7:0	Reserved.
25h	REG25	7:0	Default : 0x00 Access : R/W
	-	7	Reserved.
	SCM_IFMD	6:4	SECAM IF Compensation Filter Mode.
	-	3:0	Reserved.
26h	REG26	7:0	Default : 0xFC Access : R/W

SECAM Register (Bank = 38)

Index	Mnemonic	Bit	Description
	SDBKLEVEL_7_0	7:0	Static de-blanking level (lower 8 bits).
27h	REG27	7:0	Default : 0x04 Access : R/W
	SCMBLANKSTR	7:0	Start point of blank period.
28h	REG28	7:0	Default : 0x6C Access : R/W
	SCMBLANKEND	7:0	End point of blank period.
29h	REG29	7:0	Default : 0x0F Access : R/W
	-	7:4	Reserved.
	SIGN_FLIP_THRSD_11_8	3:0	Frequency deviation sign flipping threshold for detection (upper 4 bits).
2Ah	REG2A	7:0	Default : 0xFF Access : R/W
	SIGN_FLIP_THRSD_7_0	7:0	Frequency deviation sign flipping threshold for detection (lower 8 bits).
2Bh	REG2B	7:0	Default : 0x5F Access : R/W
	VDE_SCTL_11_8	7:4	Saturation bound value control after de-emphasis filter (upper 4 bits).
	DCAL_SCTL_11_8	3:0	Saturation bound value control before de-emphasis filter (upper 4 bits).
2Ch	REG2C	7:0	Default : 0x3A Access : R/W
	DCAL_SCTL_7_0	7:0	Saturation bound value control before de-emphasis filter (lower 8 bits).
2Dh	REG2D	7:0	Default : 0x54 Access : R/W
	VDE_SCTL_7_0	7:0	Saturation bound value control after de-emphasis filter (lower 8 bits).
2Eh	REG2E	7:0	Default : 0x06 Access : R/W
	TRIG_LINE_NUM_7_0	7:0	Trigger line number for generating interrupt (lower 8 bits).
2Fh	REG2F	7:0	Default : 0x80 Access : R/W
	SCM_CGAINMD	7	SECAM chroma gain register mode. 0: Controlled by DSP. 1: Controlled by 2Fh[6:5].
	SCM_CGAINREG	6:5	SECAM chroma gain. 01: x2. 10: x4. Others: x1.
	-	4:2	Reserved.
	TRIG_LINE_NUM_9_8	1:0	Trigger line number for generating interrupt (upper 2

SECAM Register (Bank = 38)				
Index	Mnemonic	Bit	Description	
			bits).	
30h	REG30	7:0	Default : -	Access : RO
	SCMID_DONE	7	SECAM identification done indication.	
	SCMID_YES	6	SECAM signal found bit.	
	DR_LINE	5	Dr line indication.	
	DB_LINE	4	Db line indication.	
	INTB	3	Line type indication.	
	SCMID_STS	2:0	SECAM ID status. 000: Idle. 001/010/011: ID progress. 110: SECAM. 111: No SECAM signal discovery.	
31h ~ 35h	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	
36h	REG36	7:0	Default : -	Access : RO
	-	7:5	Reserved.	
	HW_SCM_COFF	4	Hardware SECAM color-off indication.	
	-	3:2	Reserved.	
	SCM_FSC	1:0	Fsc status from AFEC_TOP. 00: NTSC 3.58MHz. 01: PAL 4.43MHz. 10: SECAM 4.285156MHz. 11: Reserved.	
38h ~ 3Bh	-	7:0	Default : -	Access : -
	-	7:0	Reserved.	

BIST Register (Bank = 39)

BIST Register (Bank = 39)				
Index (Absolute)	Mnemonic	Bit	Description	
40h (3980h)	REG3980	7:0	Default : 0x98	Access : R/W
	MICROCODE_0_H[7:0]	7:0	Microcode_0[15:8].	
41h (3982h)	REG3982	7:0	Default : 0x00	Access : R/W
	MICROCODE_0_L[7:0]	7:0	Microcode_0[7:0].	
42h (3984h)	REG3984	7:0	Default : 0xA4	Access : R/W
	MICROCODE_1_H[7:0]	7:0	Microcode_1[15:8].	
43h (3986h)	REG3986	7:0	Default : 0x40	Access : R/W
	MICROCODE_1_L[7:0]	7:0	Microcode_1[7:0].	
44h (3988h)	REG3988	7:0	Default : 0xF5	Access : R/W
	MICROCODE_2_H[7:0]	7:0	Microcode_2[15:8].	
45h (398Ah)	REG398A	7:0	Default : 0x90	Access : R/W
	MICROCODE_2_L[7:0]	7:0	Microcode_2[7:0].	
46h (398Ch)	REG398C	7:0	Default : 0x00	Access : R/W
	MICROCODE_3_H[7:0]	7:0	Microcode_3[15:8].	
47h (398Eh)	REG398E	7:0	Default : 0x80	Access : R/W
	MICROCODE_3_L[7:0]	7:0	Microcode_3[7:0].	
48h (3990h)	REG3990	7:0	Default : 0xF5	Access : R/W
	MICROCODE_4_H[7:0]	7:0	Microcode_4[15:8].	
49h (3992h)	REG3992	7:0	Default : 0x60	Access : R/W
	MICROCODE_4_L[7:0]	7:0	Microcode_4[7:0].	
4Ah (3994h)	REG3994	7:0	Default : 0x90	Access : R/W
	MICROCODE_5_H[7:0]	7:0	Microcode_5[15:8].	
4Bh (3996h)	REG3996	7:0	Default : 0x00	Access : R/W
	MICROCODE_5_L[7:0]	7:0	Microcode_5[7:0].	
4Ch (3998h)	REG3998	7:0	Default : 0x98	Access : R/W
	MICROCODE_6_H[7:0]	7:0	Microcode_6[15:8].	
4Dh (399Ah)	REG399A	7:0	Default : 0x08	Access : R/W
	MICROCODE_6_L[7:0]	7:0	Microcode_6[7:0].	
4Eh (399Ch)	REG399C	7:0	Default : 0xA4	Access : R/W
	MICROCODE_7_H[7:0]	7:0	Microcode_7[15:8].	
4Fh (399Eh)	REG399E	7:0	Default : 0x48	Access : R/W
	MICROCODE_7_L[7:0]	7:0	Microcode_7[7:0].	

BIST Register (Bank = 39)				
Index (Absolute)	Mnemonic	Bit	Description	
50h (39A0h)	REG39A0	7:0	Default : 0xF5	Access : R/W
	MICROCODE_8_H[7:0]	7:0	Microcode_8[15:8].	
51h (39A2h)	REG39A2	7:0	Default : 0x98	Access : R/W
	MICROCODE_8_L[7:0]	7:0	Microcode_8[7:0].	
52h (39A4h)	REG39A4	7:0	Default : 0x00	Access : R/W
	MICROCODE_9_H[7:0]	7:0	Microcode_9[15:8].	
53h (39A6h)	REG39A6	7:0	Default : 0x88	Access : R/W
	MICROCODE_9_L[7:0]	7:0	Microcode_9[7:0].	
54h (39A8h)	REG39A8	7:0	Default : 0xF5	Access : R/W
	MICROCODE_A_H[7:0]	7:0	Microcode_a[15:8].	
55h (39AAh)	REG39AA	7:0	Default : 0x68	Access : R/W
	MICROCODE_A_L[7:0]	7:0	Microcode_a[7:0].	
56h (39ACh)	REG39AC	7:0	Default : 0x90	Access : R/W
	MICROCODE_B_H[7:0]	7:0	Microcode_b[15:8].	
57h (39AEh)	REG39AE	7:0	Default : 0x08	Access : R/W
	MICROCODE_B_L[7:0]	7:0	Microcode_b[7:0].	
58h (39B0h)	REG39B0	7:0	Default : 0x00	Access : R/W
	MICROCODE_C_H[7:0]	7:0	Microcode_c[15:8].	
59h (39B2h)	REG39B2	7:0	Default : 0x00	Access : R/W
	MICROCODE_C_L[7:0]	7:0	Microcode_c[7:0].	
5Ah (39B4h)	REG39B4	7:0	Default : 0x00	Access : R/W
	MICROCODE_D_H[7:0]	7:0	Microcode_d[15:8].	
5Bh (39B6h)	REG39B6	7:0	Default : 0x00	Access : R/W
	MICROCODE_D_L[7:0]	7:0	Microcode_d[7:0].	
5Ch (39B8h)	REG39B8	7:0	Default : 0x00	Access : R/W
	MICROCODE_E_H[7:0]	7:0	Microcode_e[15:8].	
5Dh (39BAh)	REG39BA	7:0	Default : 0x00	Access : R/W
	MICROCODE_E_L[7:0]	7:0	Microcode_e[7:0].	
5Eh (39BCh)	REG39BC	7:0	Default : 0x00	Access : RO
	MICROCODE_F_H[7:0]	7:0	Microcode_f[15:8].	
5Fh (39BEh)	REG39BE	7:0	Default : 0x00	Access : RO
	MICROCODE_F_L[7:0]	7:0	Microcode_f[7:0].	
60h	REG39C0	7:0	Default : 0x00	Access : RO, R/W

BIST Register (Bank = 39)				
Index (Absolute)	Mnemonic	Bit	Description	
(39C0h)	-	7:3	Reserved.	
	RST_PAT_GEN	2	Reset bist pattern gen.	
	ANY_BIST_FAIL	1	ANY_BIST_FAIL.	
	BISTDONE	0	BISTDONE.	
61h (39C2h)	REG39C2	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	BIST_EN	1	BIST_EN.	
	BISTMODE	0	BISTMODE.	
62h (39C4h)	REG39C4	7:0	Default : 0x55	Access : R/W
	PATTERN_H[7:0]	7:0	Pattern[15:8].	
63h (39C6h)	REG39C6	7:0	Default : 0x00	Access : R/W
	PATTERN_L[7:0]	7:0	Pattern[7:0].	
64h (39C8h)	REG39C8	7:0	Default : 0x00	Access : R/W
	MIN_ADDR_H[7:0]	7:0	MIN_ADDR[15:8].	
65h (39CAh)	REG39CA	7:0	Default : 0x00	Access : R/W
	MIN_ADDR_L[7:0]	7:0	MIN_ADDR[7:0].	
66h (39CCh)	REG39CC	7:0	Default : 0xFF	Access : R/W
	MAX_ADDR_H[7:0]	7:0	MAX_ADDR[15:8].	
67h (39CEh)	REG39CE	7:0	Default : 0xFF	Access : R/W
	MAX_ADDR_L[7:0]	7:0	MAX_ADDR[7:0].	
68h (39D0h)	REG39D0	7:0	Default : 0x00	Access : R/W
	RETENTION_COUNTER_HH[7:0]	7:0	Retention_Counter[31:24].	
69h (39D2h)	REG39D2	7:0	Default : 0x00	Access : R/W
	RETENTION_COUNTER_HL[7:0]	7:0	Retention_Counter[23:16].	
6Ah (39D4h)	REG39D4	7:0	Default : 0x00	Access : R/W
	RETENTION_COUNTER_LH[7:0]	7:0	Retention_Counter[15:8].	
6Bh (39D6h)	REG39D6	7:0	Default : 0x00	Access : R/W
	RETENTION_COUNTER_LL[7:0]	7:0	Retention_Counter[7:0].	
6Ch (39D8h)	REG39D8	7:0	Default : 0x00	Access : RO
	BIST_FAIL_BUS_HH[7:0]	7:0	8'b0.	
6Dh (39DAh)	REG39DA	7:0	Default : 0x00	Access : RO
	BIST_FAIL_BUS_HL[7:0]	7:0	8'b0.	
6Eh	REG39DC	7:0	Default : 0x00	Access : RO

BIST Register (Bank = 39)

Index (Absolute)	Mnemonic	Bit	Description
(39DCh)	BIST_FAIL_BUS_LH[7:0]	7:0	8'b0.
6Fh	REG39DE	7:0	Default : 0x00
(39DEh)	BIST_FAIL_BUS_LL[7:0]	7:0	8'b0.

SAR Register (Bank = 3A)

SAR Register (Bank = 3A)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3A00h)	REG3A00	7:0	Default : 0x00	Access : R/W
	SAR_START	7	SAR start.	
	SAR_PD	6	SAR power down. 0: Enable. 1: Power down.	
	SAR_MODE	5	Select SAR ADC operation mode. 0: One-shot. 1: Freerun.	
	SINGLE	4	1: Enable SINGLE channel mode.	
	KEYPAD_LEVEL	3	Keypad level. 0: Active high. 1: Active low.	
	SAR_SINGLE_CH[2:0]	2:0	Select channel for single channel mode.	
01h (3A02h)	REG3A02	7:0	Default : 0x00	Access : R/W
	CKSAMP_PRD[7:0]	7:0	CKSAMP_PRD.	
05h (3A0Ah)	REG3A0A	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CH1_LOB[5:0]	5:0	SAR channel 1 lower bound.	
06h (3A0Ch)	REG3A0C	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CH2_UPB[5:0]	5:0	SAR channel 2 upper bound.	
07h (3A0Eh)	REG3A0E	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CH2_LOB[5:0]	5:0	SAR channel 2 lower bound.	
08h (3A10h)	REG3A10	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CH3_UPB[5:0]	5:0	SAR channel 3 upper bound.	
09h (3A12h)	REG3A12	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CH3_LOB[5:0]	5:0	SAR channel 3 lower bound.	
0Ah (3A14h)	REG3A14	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CH4_UPB[5:0]	5:0	SAR channel 4 upper bound.	

SAR Register (Bank = 3A)				
Index (Absolute)	Mnemonic	Bit	Description	
0Bh (3A16h)	REG3A16	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	SAR_CH4_LOB[5:0]	5:0	SAR channel 4 lower bound.	
0Ch (3A18h)	REG3A18	7:0	Default : 0x00	Access : RO
	SAR_RDY	7	SAR ready.	
	-	6	Reserved.	
	SAR_ADC_CH1_DATA[5:0]	5:0	SAR ADC channel 1 output data.	
0Dh (3A1Ah)	REG3A1A	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	SAR_ADC_CH2_DATA[5:0]	5:0	SAR ADC channel 2 output data.	
0Eh (3A1Ch)	REG3A1C	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	SAR_ADC_CH3_DATA[5:0]	5:0	SAR ADC channel 3 output data.	
0Fh (3A1Eh)	REG3A1E	7:0	Default : 0x00	Access : RO
	-	7:6	Reserved.	
	SAR_ADC_CH4_DATA[5:0]	5:0	SAR ADC channel 4 output data.	
10h (3A20h)	REG3A20	7:0	Default : 0xFF	Access : R/W
	OEN_SAR_GPIO[3:0]	7:4	Output enable for GPIO pad. 0: Enable. 1: Disable.	
	SAR_AISEL[3:0]	3:0	Pad GPIO/Ain switch. 1: Analog input. 0: GPIO.	
10h (3A21h)	REG3A21	7:0	Default : 0x00	Access : R/W
	SAR_FREERUN	7	Set up SAR ADC for freerun. 0: Controlled by digital (default). 1: Freerun.	
	SARADC_PD	6	SAR ADC power down. 1: Power down. 0: Enable SAR ADC.	
	SAR_CHSEL[1:0]	5:4	SAR ADC channel select. 00: Channel 0. 01: Channel 1. 10: Channel 2. 11: Channel 3.	

SAR Register (Bank = 3A)

Index (Absolute)	Mnemonic	Bit	Description
	I_SAR_GPIO[3:0]	3:0	Output data for GPIO pad.
12h (3A24h)	REG3A24	7:0	Default : 0x00
	-	7:6	Reserved.
	C_SAR_GPIO[5:0]	5:0	Input data for GPIO pad.
13h (3A26h)	REG3A26	7:0	Default : 0x01
	-	7:4	Reserved.
	SAR_INT_STATUS	3	Status of SAR_INT.
	SAR_INT_FORCE	2	Force interrupt for SAR_INT.
	SAR_INT_CLR	1	Interrupt clear for SAR_INT.
	SAR_INT_MASK	0	Interrupt mask for SAR_INT. 0: Enable. 1: Disable.
15h (3A2Ah)	REG3A2A	7:0	Default : 0x00
	-	7:6	Reserved.
	SAR_CH5_UPB[5:0]	5:0	SAR channel 5 upper bound.
16h (3A2Ch)	REG3A2C	7:0	Default : 0x00
	-	7:6	Reserved.
	SAR_CH5_LOB[5:0]	5:0	SAR channel 5 lower bound.
17h (3A2Eh)	REG3A2E	7:0	Default : 0x00
	-	7:6	Reserved.
	SAR_CH6_UPB[5:0]	5:0	SAR channel 6 upper bound.
18h (3A30h)	REG3A30	7:0	Default : 0x00
	-	7:6	Reserved.
	SAR_CH6_LOB[5:0]	5:0	SAR channel 6 lower bound.
19h (3A32h)	REG3A32	7:0	Default : 0x00
	-	7:6	Reserved.
	SAR_ADC_CH5_DATA[5:0]	5:0	SAR ADC for channel 5 data read back.
1Ah (3A34h)	REG3A34	7:0	Default : 0x00
	-	7:6	Reserved.
	SAR_ADC_CH6_DATA[5:0]	5:0	SAR ADC for channel 6 data read back.
1Bh (3A36h)	REG3A36	7:0	Default : 0x0F
	-	7:6	Reserved.
	I_SAR_GPIO_EXT_2CH[1:0]	5:4	SAR[5:4] Output data for GPIO pad.

SAR Register (Bank = 3A)				
Index (Absolute)	Mnemonic	Bit	Description	
	OEN_SAR_GPIO_EXT_2CH[1:0]	3:2	SAR[5:4] Output enable for GPIO pad. 0: Enable. 1: Disable.	
	SAR_AISEL_EXT_2CH[1:0]	1:0	SAR[5:4] Pad GPIO/Ain switch. 1: Analog input. 0: GPIO.	
20h ~ 22h	-	7:0	Default : -	Access : -
(3A40h ~ 3A45h)	-	-	Reserved.	

PIU_MISC_0 Register (Bank = 3C)

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	Mnemonic	Bit	Description	
00h ~ 0Fh (3C00h ~ 3C1Fh)	-	7:0	Default : -	Access : -
	-	-	Reserved.	
10h (3C20h)	REG3C20	7:0	Default : 0x00	Access : RO, R/W
	CRC_DUM_10[4:0]	7:3	Bit 0 is used as DST_SEL_VDMCU.	
	DMA_BUSY	2	DMA busy.	
	DMA_DONE	1	DMA idle.	
	-	0	Reserved.	
10h (3C21h)	REG3C21	7:0	Default : 0x00	Access : RO
	DMA_STATE[7:0]	7:0	DMA status.	
20h (3C40h)	REG3C40	7:0	Default : 0x11	Access : R/W
	CSZ_SETUP[3:0]	7:4	Number of cycles between SPI_CSZ falling and first SPI_SCK.	
	CSZ_HOLD[3:0]	3:0	Number of cycles between last SPI_SCK and SPI_CSZ rising.	
20h (3C41h)	REG3C41	7:0	Default : 0x01	Access : R/W
	FAST	7	FAST mode.	
	-	6:4	Reserved.	
	CSZ_HIGH[3:0]	3:0	Number of cycles when SPI_CSZ = high.	
26h (3C4Ch)	REG3C4C	7:0	Default : 0x00	Access : R/W
	RESERVED0[7:0]	7:0	[5:0]: SPI clock selection. [8]: SPI new cycle.	
26h (3C4Dh)	REG3C4D	7:0	Default : 0x00	Access : R/W
	RESERVED0[15:8]	7:0	See description of '3C4Ch'.	
27h (3C4Eh)	REG3C4E	7:0	Default : 0x00	Access : R/W
	RESERVED0[23:16]	7:0	See description of '3C4Ch'.	
27h (3C4Fh)	REG3C4F	7:0	Default : 0x00	Access : R/W
	RESERVED0[31:24]	7:0	See description of '3C4Ch'.	
2Ah (3C54h)	REG3C54	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	SPI_NEW_CYCLE	0	Force SPI to issue a new cycle.	
30h (3C60h)	REG3C60	7:0	Default : 0xAA	Access : R/W
	WDT_KEY[7:0]	7:0	enable: WDT_KEY != 0xaa55.	

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	Mnemonic	Bit	Description	
30h (3C61h)	REG3C61	7:0	Default : 0x55	Access : R/W
	WDT_KEY[15:8]	7:0	See description of '3C60h'.	
31h (3C62h)	REG3C62	7:0	Default : 0x00	Access : R/W
	WDT_SEL[7:0]	7:0	WDT interval, 65536 * (65536 - WDT_SEL) cycles.	
31h (3C63h)	REG3C63	7:0	Default : 0xFC	Access : R/W
	WDT_SEL[15:8]	7:0	See description of '3C62h'.	
32h (3C64h)	REG3C64	7:0	Default : 0x00	Access : R/W
	WDT_INT_SEL[7:0]	7:0	When WDT_CNT[31:16] > WDT_INT_SEL, watchdog interrupt occurs.	
32h (3C65h)	REG3C65	7:0	Default : 0xFF	Access : R/W
	WDT_INT_SEL[15:8]	7:0	See description of '3C64h'.	
33h (3C66h)	REG3C66	7:0	Default : 0x00	Access : RO, WO
	-	7:3	Reserved.	
	WDT_CLR_RESET_FLAG	2	Clear watchdog reset flag.	
	WDT_CLR_MCU	1	Clear watchdog.	
	WDT_RST	0	Watchdog reset occurs.	
38h (3C70h)	REG3C70	7:0	Default : 0x00	Access : R/W
	POWER_STATUS0[7:0]	7:0	Power status 0.	
38h (3C71h)	REG3C71	7:0	Default : 0x00	Access : R/W
	POWER_STATUS0[15:8]	7:0	See description of '3C70h'.	
39h (3C72h)	REG3C72	7:0	Default : 0x00	Access : R/W
	POWER_STATUS1[7:0]	7:0	Power status 1.	
39h (3C73h)	REG3C73	7:0	Default : 0x00	Access : R/W
	POWER_STATUS1[15:8]	7:0	See description of '3C72h'.	
3Ah (3C74h)	REG3C74	7:0	Default : 0x00	Access : R/W
	POWER_STATUS2[7:0]	7:0	Power status 2.	
3Ah (3C75h)	REG3C75	7:0	Default : 0x00	Access : R/W
	POWER_STATUS2[15:8]	7:0	See description of '3C74h'.	
3Bh (3C76h)	REG3C76	7:0	Default : 0x00	Access : R/W
	POWER_STATUS3[7:0]	7:0	Power status 3.	
3Bh (3C77h)	REG3C77	7:0	Default : 0x00	Access : R/W
	POWER_STATUS3[15:8]	7:0	See description of '3C76h'.	
3Ch	REG3C78	7:0	Default : 0x00	Access : R/W

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	Mnemonic	Bit	Description	
(3C78h)	POWER_STATUS4[7:0]	7:0	Power status 4.	
3Ch (3C79h)	REG3C79 POWER_STATUS4[15:8]	7:0	Default : 0x00	Access : R/W
3Dh (3C7Ah)	REG3C7A POWER_STATUS5[7:0]	7:0	Default : 0x00	Access : R/W
3Dh (3C7Bh)	REG3C7B POWER_STATUS5[15:8]	7:0	Default : 0x00	Access : R/W
3Eh (3C7Ch)	REG3C7C POWER_STATUS6[7:0]	7:0	Default : 0x00	Access : R/W
3Eh (3C7Dh)	REG3C7D POWER_STATUS6[15:8]	7:0	Default : 0x00	Access : R/W
3Fh (3C7Eh)	REG3C7E POWER_STATUS7[7:0]	7:0	Default : 0x00	Access : R/W
3Fh (3C7Fh)	REG3C7F POWER_STATUS7[15:8]	7:0	Default : 0x00	Access : R/W
40h (3C80h)	REG3C80 TIMER_MAX_0[7:0]	7:0	Default : 0x00	Access : R/W
40h (3C81h)	REG3C81 TIMER_MAX_0[15:8]	7:0	Default : 0x00	Access : R/W
41h (3C82h)	REG3C82 TIMER_MAX_0[23:16]	7:0	Default : 0x00	Access : R/W
41h (3C83h)	REG3C83 TIMER_MAX_0[31:24]	7:0	Default : 0x00	Access : R/W
42h (3C84h)	REG3C84 TIMER_CNT_CAP_0[7:0]	7:0	Default : 0x00	Access : RO
42h (3C85h)	REG3C85 TIMER_CNT_CAP_0[15:8]	7:0	Default : 0x00	Access : RO
43h (3C86h)	REG3C86 TIMER_CNT_CAP_0[23:16]	7:0	Default : 0x00	Access : RO
43h (3C87h)	REG3C87 TIMER_CNT_CAP_0[31:24]	7:0	Default : 0x00	Access : RO
44h (3C88h)	REG3C88 -	7:2	Default : 0x00	Access : WO
			Reserved.	

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	Mnemonic	Bit	Description	
	CLR_0	1	Clear internal counter.	
	CAPTURE_0	0	Capture internal counter.	
44h (3C89h)	REG3C89	7:0	Default : 0x00	Access : R/W
	TIMER_CTRL_0[7:0]	7:0	0: Disable. 3: Enable.	
50h (3CA0h)	REG3CA0	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_1[7:0]	7:0	When internal counter == TIMER_MAX, interrupt occurs.	
50h (3CA1h)	REG3CA1	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_1[15:8]	7:0	See description of '3CA0h'.	
51h (3CA2h)	REG3CA2	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_1[23:16]	7:0	See description of '3CA0h'.	
51h (3CA3h)	REG3CA3	7:0	Default : 0x00	Access : R/W
	TIMER_MAX_1[31:24]	7:0	See description of '3CA0h'.	
52h (3CA4h)	REG3CA4	7:0	Default : 0x00	Access : RO
	TIMER_CNT_CAP_1[7:0]	7:0	Captured counter.	
52h (3CA5h)	REG3CA5	7:0	Default : 0x00	Access : RO
	TIMER_CNT_CAP_1[15:8]	7:0	See description of '3CA4h'.	
53h (3CA6h)	REG3CA6	7:0	Default : 0x00	Access : RO
	TIMER_CNT_CAP_1[23:16]	7:0	See description of '3CA4h'.	
53h (3CA7h)	REG3CA7	7:0	Default : 0x00	Access : RO
	TIMER_CNT_CAP_1[31:24]	7:0	See description of '3CA4h'.	
54h (3CA8h)	REG3CA8	7:0	Default : 0x00	Access : WO
	-	7:2	Reserved.	
	CLR_1	1	Clear internal counter.	
	CAPTURE_1	0	Capture internal counter.	
54h (3CA9h)	REG3CA9	7:0	Default : 0x00	Access : R/W
	TIMER_CTRL_1[7:0]	7:0	0: Disable. 3: Enable.	
60h (3CC0h)	REG3CC0	7:0	Default : 0x92	Access : R/W
	ISP_ID[7:0]	7:0	ID of ISP.	
60h (3CC1h)	REG3CC1	7:0	Default : 0x4D	Access : R/W
	ISP_PWD1[7:0]	7:0	ISP password 1.	
61h	REG3CC2	7:0	Default : 0x53	Access : R/W

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	Mnemonic	Bit	Description	
(3CC2h)	ISP_PWD2[7:0]	7:0	ISP password 2.	
61h	REG3CC3	7:0	Default : 0x54	Access : R/W
(3CC3h)	ISP_PWD3[7:0]	7:0	ISP password 3.	
62h	REG3CC4	7:0	Default : 0x41	Access : R/W
(3CC4h)	ISP_PWD4[7:0]	7:0	ISP password 4.	
62h	REG3CC5	7:0	Default : 0x52	Access : R/W
(3CC5h)	ISP_PWD5[7:0]	7:0	ISP password 5.	
63h	REG3CC6	7:0	Default : 0x00	Access : R/W
(3CC6h)	ISP_CTRL0[7:0]	7:0	ISP password 6.	
70h	REG3CE0	7:0	Default : 0x00	Access : R/W
(3CE0h)	DMA_SRC_ADR_0[7:0]	7:0	Source address lower word.	
70h	REG3CE1	7:0	Default : 0x00	Access : R/W
(3CE1h)	DMA_SRC_ADR_0[15:8]	7:0	See description of '3CE0h'.	
71h	REG3CE2	7:0	Default : 0x00	Access : R/W
(3CE2h)	DMA_SRC_ADR_1[7:0]	7:0	Source address higher word.	
71h	REG3CE3	7:0	Default : 0x00	Access : R/W
(3CE3h)	DMA_SRC_ADR_1[15:8]	7:0	See description of '3CE2h'.	
72h	REG3CE4	7:0	Default : 0x00	Access : R/W
(3CE4h)	DMA_DST_ADR_0[7:0]	7:0	Destination address lower word, must align to 8-byte when destination is DRAM.	
72h	REG3CE5	7:0	Default : 0x00	Access : R/W
(3CE5h)	DMA_DST_ADR_0[15:8]	7:0	See description of '3CE4h'.	
73h	REG3CE6	7:0	Default : 0x00	Access : R/W
(3CE6h)	DMA_DST_ADR_1[7:0]	7:0	Destination address higher word, must align to 8-byte when destination is DRAM.	
73h	REG3CE7	7:0	Default : 0x00	Access : R/W
(3CE7h)	DMA_DST_ADR_1[15:8]	7:0	See description of '3CE6h'.	
74h	REG3CE8	7:0	Default : 0x00	Access : R/W
(3CE8h)	DMA_SIZE_0[7:0]	7:0	DMA size lower word, must align to 8-byte when destination is DRAM.	
74h	REG3CE9	7:0	Default : 0x00	Access : R/W
(3CE9h)	DMA_SIZE_0[15:8]	7:0	See description of '3CE8h'.	
75h	REG3CEA	7:0	Default : 0x00	Access : R/W

PIU_MISC_0 Register (Bank = 3C)				
Index (Absolute)	Mnemonic	Bit	Description	
(3CEAh)	DMA_SIZE_1[7:0]	7:0	DMA size higher word, must align to 8-byte when destination is DRAM.	
75h	REG3CEB	7:0	Default : 0x00	Access : R/W
(3CEBh)	DMA_SIZE_1[15:8]	7:0	See description of '3CEAh'.	
76h	REG3CEC	7:0	Default : 0x00	Access : R/W, WO
(3CECh)	DMA_ADDR_INC	7	Set to 1 when destination is not increasing, for VDMCU.	
	DMA_RIU_MODE	6	Same as DMA_DST_SEL.	
	DMA_BIG_ENDIAN	5	Swap byte order in 4-byte word.	
	-	4	Reserved.	
	DMA_DST_SEL	3	0: DRAM. 1: DSP when CRC_DUM_10[0] is 0, VDMCU when CRC_DUM_10[0] is 1.	
	-	2:1	Reserved.	
	DMA_TRIG	0	DMA trigger bit, write only.	
7Dh ~ 7Fh	-	7:0	Default : -	Access : -
(3CFAh ~ 3CFEh)	-	-	Reserved.	

IR Register (Bank = 3D)

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3D00h)	REG3D00	7:0	Default : 0x1F	Access : R/W
	RC_FIFO_WFIRST	7	RC FIFO write first. 0: Read first; 1: write first.	
	RC_FIFO_CLEAR	6	RC FIFO clear. 0: Disable; 1: enable.	
	RC_AUTOCONFIG	5	Auto config RC5 and RC6 setting.	
	RC6_LS_THR_L[4:0]	4:0	RC6 leading pulse threshold * 32.	
00h (3D01h)	REG3D01	7:0	Default : 0x00	Access : R/W
	RCIN_INV	7	RC input invert. 0=disabe;1=enable.	
	RC_DEBUG_SEL[2:0]	6:4	RC debug output select.	
	RC_WKUP_EN	3	RC wake up enable. 0=disable; 1=enable.	
	RC5EXT_EN	2	Extended RC-5 enable. 0=disable; 1=enable.	
	RC6_EN	1	0= RC5;1= RC6.	
	RC_EN	0	RC receiver enable. 0=disable; 1=enable.	
01h (3D02h)	REG3D02	7:0	Default : 0xA0	Access : R/W
	RC_LONGPULSE_THR[7:0]	7:0	RC long pulse threshold. To judge long pulse or not.	
01h (3D03h)	REG3D03	7:0	Default : 0x04	Access : R/W
	-	7:5	Reserved.	
	RC_LONGPULSE_THR[12:8]	4:0	See description of '3D02h'.	
02h (3D04h)	REG3D04	7:0	Default : 0xC0	Access : R/W
	RC_LONGPULSE_MAR[7:0]	7:0	RC6 long pulse margin, only for RC6.	
02h (3D05h)	REG3D05	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	RC6_LS_THR_H[2:0]	4:2	RC6 leading pulse threshold * 1024.	
	RC_LONGPULSE_MAR[9:8]	1:0	See description of '3D04h'.	
03h (3D06h)	REG3D06	7:0	Default : 0x41	Access : R/W
	RC_INT_THR[6:0]	7:1	RC Integrator threshold * 8. To judge 0 or 1.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	RC6_ECO_EN	0	RC6 ECO function enable.	
03h (3D07h)	REG3D07	7:0	Default : 0x00	Access : R/W
	-	7:5	Reserved.	
	RC_CLKDIV[4:0]	4:0	RC operating clock divisor ratio.	
04h (3D08h)	REG3D08	7:0	Default : 0x3C	Access : R/W
	RC_WDOG_COUNT[7:0]	7:0	RC watch dog counter (based on 2kHz for 1MHz clock input).	
04h (3D09h)	REG3D09	7:0	Default : 0x10	Access : R/W
	RC_TIMEOUT_COUNT[7:0]	7:0	RC timeout counter (based on 0.5kHz for 1MHz clock input).	
05h (3D0Ah)	REG3D0A	7:0	Default : 0xFF	Access : R/W
	COMP_RKEY1[7:0]	7:0	RC power wakeup key1.	
05h (3D0Bh)	REG3D0B	7:0	Default : 0xFF	Access : R/W
	COMP_RKEY2[7:0]	7:0	RC power wakeup key2.	
06h (3D0Ch)	REG3D0C	7:0	Default : 0x00	Access : RO
	RKEY_ADDRESS[7:0]	7:0	RC decode address. RC5: {2'b0,toggle,address[4:0]}. RC6: Address[7:0].	
06h (3D0Dh)	REG3D0D	7:0	Default : 0x00	Access : RO
	RKEY_COMMAND[7:0]	7:0	RC decode command. RC5: {repeat,1'b0,command[5:0]}. RC5EXT: {repeat,command[6:0]}. RC6: Command[7:0].	
07h (3D0Eh)	REG3D0E	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	RKEY_MISC[4:0]	4:0	RC6 decode MISC data. [2:0]: MODE[2:0]. [3]: Toggle. [4]: Repeat.	
08h (3D10h)	REG3D10	7:0	Default : 0x00	Access : RO
	-	7	Reserved.	
	RC_FIFO_WPTR[2:0]	6:4	RC FIFO write pointer.	
	-	3	Reserved.	
	RC_FIFO_FULL	2	RC FIFO full.	
	RC_TIMEOUT_FLAG	1	RC time-out flag. 1: Time-out.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	RC_FIFO_EMPTY	0	RC FIFO empty.	
08h (3D11h)	REG3D11	7:0	Default : 0x00	Access : RO
	-	7:3	Reserved.	
	RC_FIFO_RPTR[2:0]	2:0	RC FIFO read pointer.	
09h (3D12h)	REG3D12	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	RC_FIFO_RD_PULSE	0	RC FIFO read pulse gen.	
09h (3D13h)	REG3D13	7:0	Default : 0x00	Access : WO
	-	7:1	Reserved.	
	RC_WKUP_CLR	0	RC wake up clear pulse generator.	
0Ah (3D14h)	REG3D14	7:0	Default : 0xFF	Access : R/W
	RC_ADDRESS[7:0]	7:0	RC power wakeup address.	
0Ah (3D15h)	REG3D15	7:0	Default : 0x01	Access : R/W
	-	7:2	Reserved.	
	RC_ANYKEY_EN	1	RC anykey wakeup enable.	
	RCADR_CMP_EN	0	RC power wakeup address enable.	
40h (3D80h)	REG3D80	7:0	Default : 0xBE	Access : R/W
	IR_INV	7	Invert the polarity for input IR signal.	
	IR_INT_MASK	6	IR Interrupt request Mask for mcu.	
	IR_RPCODE_EN	5	IR Repeat Code check enable.	
	IR_LG01H_CHK_EN	4	IR Logic 0/1 High level edge Check Enable.	
	IR_DCODE_PCHK_EN	3	IR Data Code Parity Check Enable.	
	IR_CCODE_CHK_EN	2	IR Customer Code Check Enable.	
	IR_LDCCHK_EN	1	IR Leader Code (header + off code) Check Enable.	
	IR_EN	0	IR NEC-like (PPM format) decode Enable for Full/Raw mode.	
40h (3D81h)	REG3D81	7:0	Default : 0xC1	Access : R/W
	IR_INT_CRC_MASK	7	Interrupt Mask for IR CRC check.	
	RAW_RPT_INT_MASK	6	Interrupt Mask for Repeat code in RAW mode.	
	-	5:4	Reserved.	
	IR_BIT_INV_EN	3	Enable for IR decode logic bit inverse. 0: Disable. 1: Enable.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	IR_KEY_MSB_FIRST	2	Enable for IR key MSB first. 0: The key data format is LSB first. (ie, key[0:7]). 1: The key data format is MSB first (ie, key[7:0]).	
	IR_SEPR_EN	1	IR Separator Code check Enable (This bit is for Mitsubishi only).	
	IR_TIMEOUT_CHK_EN	0	IR Time-Out Check Enable.	
41h (3D82h)	REG3D82	7:0	Default : 0xF2	Access : R/W
	IR_HDC_UPB[7:0]	7:0	The counter Upper Bound for Header Code.	
41h (3D83h)	REG3D83	7:0	Default : 0x2B	Access : R/W
	-	7:6	Reserved.	
	IR_HDC_UPB[13:8]	5:0	See description of '3D82h'.	
42h (3D84h)	REG3D84	7:0	Default : 0x5E	Access : R/W
	IR_HDC_LOB[7:0]	7:0	The counter Lower Bound for Header Code.	
42h (3D85h)	REG3D85	7:0	Default : 0x1A	Access : R/W
	-	7:6	Reserved.	
	IR_HDC_LOB[13:8]	5:0	See description of '3D84h'.	
43h (3D86h)	REG3D86	7:0	Default : 0xF9	Access : R/W
	IR_OFC_UPB[7:0]	7:0	The counter Upper Bound for Off Code.	
43h (3D87h)	REG3D87	7:0	Default : 0x15	Access : R/W
	-	7:5	Reserved.	
	IR_OFC_UPB[12:8]	4:0	See description of '3D86h'.	
44h (3D88h)	REG3D88	7:0	Default : 0x2F	Access : R/W
	IR_OFC_LOB[7:0]	7:0	The counter Lower Bound for Off Code.	
44h (3D89h)	REG3D89	7:0	Default : 0x0D	Access : R/W
	-	7:5	Reserved.	
	IR_OFC_LOB[12:8]	4:0	See description of '3D88h'.	
45h (3D8Ah)	REG3D8A	7:0	Default : 0x35	Access : R/W
	IR_OFC_RP_UPB[7:0]	7:0	The counter Upper Bound for Repeat Off Code.	
45h (3D8Bh)	REG3D8B	7:0	Default : 0x0C	Access : R/W
	-	7:4	Reserved.	
	IR_OFC_RP_UPB[11:8]	3:0	See description of '3D8Ah'.	
46h (3D8Ch)	REG3D8C	7:0	Default : 0x53	Access : R/W
	IR_OFC_RP_LOB[7:0]	7:0	The counter Lower Bound for Repeat Off Code.	
46h	REG3D8D	7:0	Default : 0x07	Access : R/W

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
(3D8Dh)	-	7:4	Reserved.	
	IR_OFC_RP_LOB[11:8]	3:0	See description of '3D8Ch'.	
47h (3D8Eh)	REG3D8E	7:0	Default : 0xBC	Access : R/W
	IR_LG01H_UPB[7:0]	7:0	The counter Upper Bound for Logic 0/1 High level width.	
47h (3D8Fh)	REG3D8F	7:0	Default : 0x02	Access : R/W
	-	7:2	Reserved.	
	IR_LG01H_UPB[9:8]	1:0	See description of '3D8Eh'.	
48h (3D90h)	REG3D90	7:0	Default : 0xA4	Access : R/W
	IR_LG01H_LOB[7:0]	7:0	The counter Lower Bound for Logic 0/1 High level width.	
48h (3D91h)	REG3D91	7:0	Default : 0x01	Access : R/W
	-	7:2	Reserved.	
	IR_LG01H_LOB[9:8]	1:0	See description of '3D90h'.	
49h (3D92h)	REG3D92	7:0	Default : 0x78	Access : R/W
	IR_LG0_UPB[7:0]	7:0	The counter Upper Bound for Logic 0 width.	
49h (3D93h)	REG3D93	7:0	Default : 0x05	Access : R/W
	-	7:3	Reserved.	
	IR_LG0_UPB[10:8]	2:0	See description of '3D92h'.	
4Ah (3D94h)	REG3D94	7:0	Default : 0x48	Access : R/W
	IR_LG0_LOB[7:0]	7:0	The counter Lower Bound for Logic 0 width.	
4Ah (3D95h)	REG3D95	7:0	Default : 0x03	Access : R/W
	-	7:3	Reserved.	
	IR_LG0_LOB[10:8]	2:0	See description of '3D94h'.	
4Bh (3D96h)	REG3D96	7:0	Default : 0xF0	Access : R/W
	IR_LG1_UPB[7:0]	7:0	The counter Upper Bound for Logic 1 width.	
4Bh (3D97h)	REG3D97	7:0	Default : 0x0A	Access : R/W
	-	7:4	Reserved.	
	IR_LG1_UPB[11:8]	3:0	See description of '3D96h'.	
4Ch (3D98h)	REG3D98	7:0	Default : 0x90	Access : R/W
	IR_LG1_LOB[7:0]	7:0	The counter Lower Bound for Logic 1 width.	
4Ch (3D99h)	REG3D99	7:0	Default : 0x06	Access : R/W
	-	7:4	Reserved.	
	IR_LG1_LOB[11:8]	3:0	See description of '3D98h'.	
4Dh	REG3D9A	7:0	Default : 0x00	Access : R/W

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
(3D9Ah)	IR_SEPR_UPB[7:0]	7:0	The counter Upper Bound for Separator Code width.	
4Dh (3D9Bh)	REG3D9B	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_SEPR_UPB[11:8]	3:0	See description of '3D9Ah'.	
4Eh (3D9Ch)	REG3D9C	7:0	Default : 0x00	Access : R/W
	IR_SEPR_LOB[7:0]	7:0	The counter Lower Bound for Separator Code width.	
4Eh (3D9Dh)	REG3D9D	7:0	Default : 0x00	Access : R/W
	-	7:4	Reserved.	
	IR_SEPR_LOB[11:8]	3:0	See description of '3D9Ch'.	
4Fh (3D9Eh)	REG3D9E	7:0	Default : 0x8C	Access : R/W
	IR_TIMEOUT_CYC[7:0]	7:0	The counter value for IR Timeout Cycles. Timeout check will start when under below conditions. 1. IR_TIMEOUT_CHK_EN=1. 2. Counter value > IR_TIMEOUT_CYC.	
4Fh (3D9Fh)	REG3D9F	7:0	Default : 0x00	Access : R/W
	IR_TIMEOUT_CYC[15:8]	7:0	See description of '3D9Eh'.	
50h (3DA0h)	REG3DA0	7:0	Default : 0x30	Access : R/W
	IR_TIMEOUT_CLR_SW	7	IR Timeout Clear by SoftWare. 1: Enable. 0: Disable.	
	IR_TIMEOUT_CLR_SET[2:0]	6:4	IR Timeout Clear method Set. 000: Timeout be clear at HDC check pass. 001: Timeout be clear at OFC check pass & Decode 0 state. 010: Timeout be clear at Customer Code check pass. 011: Timeout be clear at Key Data Code check pass. 100: S/W clear, need also to set IR_TIMEOUT_CLR_SW=1. Recommend: Set 011 for NEC-like format.	
	-	3	Reserved.	
	IR_TIMEOUT_CYC[18:16]	2:0	See description of '3D9Eh'.	
50h (3DA1h)	REG3DA1	7:0	Default : 0x1F	Access : R/W
	IR_CCODE_BYTE	7	IR Customer Code Byte setting (full mode use only). 0: 1 byte customer code. 1: 2 bytes customer code. Recommend: 1 for NEC format.. Please also see 0x3DA4h and 0x3DA5h for customer code setting.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	IR_CODE_BIT_NUM[6:0]	6:0	IR data code total bits. 00: 1 bit. 01: 2 bits. 10: 3 bits. ... 7f: 128 bits. Recommend: 1f for NEC format.	
51h (3DA2h)	REG3DA2	7:0	Default : 0x00	Access : R/W, WO
	RPT_FLAG_CLR_RAW	7	Interrupt Flag Clear for IR repeat code flag in RAW mode. 1: Clear interrupt flag. 0: Not clear interrupt flag.	
	-	6	Reserved.	
	IR_SEPR_BIT[5:0]	5:0	IR Separator Bits setting (Only used for Mitsubishi format in full/raw mode). The code data bit decode after this bit will into separator state when REG_IR_SEPR_EN=1 (3D81h[1]).	
51h (3DA3h)	REG3DA3	7:0	Default : 0x0F	Access : R/W, WO
	IR_FIFO_CLR	7	IR FIFO Clear Pulse Generation. 1: Generate 1T fifo clear pulse. 0: Normal operation. It is recommended to clear IR fifo when leaving power down mode.	
	-	6	Reserved.	
	IR_SHOT_SEL[1:0]	5:4	The pshot/nshot selection for internal counter (Only used in S/W mode). 2_b01 : only pshot edge detect for counter. 2_b10 : only nshot edge detect for counter. 2_b00/11 : both pshot and nshot edge detect for counter.	
	IR_FIFO_FULL_EN	3	IR FIFO Full Enable (Used in Full/Raw mode). 0: Disable FIOF Full (data can be written over when FIFO is full). 1: Enable FIFO Full (data will be discarded when FIFO is full).	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	IR_FIFO_DEPTH[2:0]	2:0	FIFO Depth (for decoded IR code data or IR raw data, not for S/W mode counter data), totally support 16 bytes depth. 000: 9 bytes. 001: 10 bytes. 010: 11 bytes. 011: 12 bytes. 100: 13 bytes. 101: 14 bytes. 110: 15 bytes. 111: 16 bytes. Recommend: 16bytes (111).	
52h (3DA4h)	REG3DA4	7:0	Default : 0x00	Access : R/W
	IR_CC CODE[7:0]	7:0	IR Customer Code. If the customer code only have 1 byte, we can set IR_CC CODE[7:0] instead of set IR_CC CODE[15:0]. The number of bytes for customer code compare depends on the setting of IR_CC CODE_BYTE (0x3DA1h[7]).	
52h (3DA5h)	REG3DA5	7:0	Default : 0x00	Access : R/W
	IR_CC CODE[15:8]	7:0	See description of '3DA4h'.	
53h (3DA6h)	REG3DA6	7:0	Default : 0x00	Access : R/W
	IR_GLHRM_NUM[7:0]	7:0	Glitch Removal Number for crystal based counter. The glitches will be removed whenever their cycle width below the GLHRM_NUM cycle.	
53h (3DA7h)	REG3DA7	7:0	Default : 0x00	Access : R/W
	-	7:6	Reserved.	
	IR_DECOMODE[1:0]	5:4	IR Decode Mode selection. 00/11 : Full decode mode (NEC and NEC-like format). 01: S/W mode (shot mode, output edge count value). 10: Raw mode (header decode only and output raw data, for NEC-like formats).	
	IR_GLHRM_EN	3	Glitch Removal Enable.	
	IR_GLHRM_NUM[10:8]	2:0	See description of '3DA6h'.	
54h	REG3DA8	7:0	Default : 0x00	Access : R/W

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
(3DA8h)	IR_CKDIV_NUM[7:0]	7:0	The Divided Number of IR decoder input clock, the divided clock is for internal counter use. The input clock source of IR decoder is (XTAL/4) MHz. 8_h00 : Divided by 1. 8_h01 : Divided by 2. ... 8_hFF : Divided by 256. Recommend: 8_h02 for Xtal clock=14.318MHz. 8_h05 for Xtal clock=25.00MHz.	
54h (3DA9h)	REG3DA9	7:0	Default : 0x00	Access : RO
	IR_KEY_DATA[7:0]	7:0	IR Key Data output for Full/Raw mode data. After reading IR_KEY_DATA (3DA9h), you must set IR_FIFO_RD_PULSE=1 (3DB0h[0]) for internal fifo read pointer go to the next one.	
55h (3DAAh)	REG3DAA	7:0	Default : 0x00	Access : RO
	IR_SHOT_CNT[7:0]	7:0	IR Shot Count value output in s/w mode, the type of shot is select from IR_SHOT_SEL (3DA3h[5:4]).	
55h (3DABh)	REG3DAB	7:0	Default : 0x00	Access : RO
	IR_SHOT_CNT[15:8]	7:0	See description of '3DAAh'.	
56h (3DACH)	REG3DAC	7:0	Default : 0x00	Access : RO
	-	7:5	Reserved.	
	IR_SHOT_P	4	IR shot type (pshot/nshot) in s/w mode. 0: Nshot occurs. 1: Pshot occurs.	
	-	3	Reserved.	
	IR_SHOT_CNT[18:16]	2:0	See description of '3DAAh'.	
56h (3DADh)	REG3DAD	7:0	Default : 0x00	Access : RO
	IR_RC_WKUP_FLAG	7	IR RC wakeup function flag.	
	IR_NEC_WKUP_FLAG	6	IR NEC (or NEC-like) wakeup function flag.	
	IR_INT_CRC_FLAG	5	IR CRC function interrupt flag.	
	IR_INT_FLAG	4	IR normal function interrupt flag.	
	IR_FIFO_FULL	3	IR FIFO Full Flag for NEC-like (PPM modulation) format decoder. 1: FIFO is full. 0: FIFO is not full yet.	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
	IR_TIMEOUT_FLAG	2	IR Timeout Flag. 1: Timeout occurs. 0: Not timeout yet.	
	IR_FIFO_EMPTY	1	IR FIFO Empty flag for Full/Raw mode.	
	IR_RPT_FLAG	0	IR FIFO data Repeat Flag for Full mode.	
57h (3DAEh)	REG3DAE	7:0	Default : 0x00	Access : RO
	IR_CRC_GOLDEN[7:0]	7:0	IR CRC Golden value, calculated by hardware while entering into power down mode. This value can be read just for reference, software don't need to fill any value. (Read-Only).	
57h (3DAFh)	REG3DAF	7:0	Default : 0x00	Access : RO
	IR_CRC_GOLDEN[15:8]	7:0	See description of '3DAEh'.	
58h (3DB0h)	REG3DB0	7:0	Default : 0x20	Access : R/W, WO
	IR_WKUP_KEY_SEL[3:0]	7:4	IR key byte select for wakeup key compare. 0: Select byte 0 of IR signal as IR key (1st byte of IR data bytes). 1: Select byte 1 of IR signal as IR key (2nd byte of IR data bytes). 2: Select byte 2 of IR signal as IR key (3rd byte of IR data bytes). 15: Select byte 15 of IR signal as IR key (7th byte of IR data bytes).	
	IR_NEC_WKUP_FLAG_CLR	3	IR wakeup flag clear of NEC (or NEC-like) format. 1: Clear pulse generate. 0: No operation.	
	IR_FLAG_CLR	2	IR interrupt flag clear. 1: Clear pulse generate. 0: No operation.	
	IR_CRC_FLAG_CLR	1	IR crc interrupt flag clear. 1: Clear pulse generate. 0: No operation.	
	IR_FIFO_RD_PULSE	0	IR FIFO Read Pulse. 1: Read. 0: Not read. Note: Need to set this bit to 1 after s/w read "IR_KEY_DATA" (3DA9h) (to let FIFO read pointer go to the next one).	

IR Register (Bank = 3D)				
Index (Absolute)	Mnemonic	Bit	Description	
59h (3DB2h)	REG3DB2	7:0	Default : 0xFF	Access : R/W
	IR_NEC_COMP_KEY1[7:0]	7:0	IR compare key1 for wakeup function of NEC (or NEC-like) format.	
59h (3DB3h)	REG3DB3	7:0	Default : 0xFF	Access : R/W
	IR_NEC_COMP_KEY2[7:0]	7:0	IR compare key2 for wakeup function of NEC (or NEC-like) format.	
5Ah (3DB4h)	REG3DB4	7:0	Default : 0x00	Access : R/W
	IR_ANYKEY_WKUP_EN	7	Enable for IR wakeup by any key (Customer code must matched) matched function. 0: Disable. 1: Enable.	
	IR_NEC_WKUP_EN	6	Enable for IR wakeup function of NEC (or NEC-like) format. 0: Disable. 1: Enable.	
	-	5	Reserved.	

IR Register (Bank = 3D)

Index (Absolute)	Mnemonic	Bit	Description
	IR_4MAT_SEL[4:0]	4:0	<p>IR data sequence format select for NEC-like (PPM modulation) formats.</p> <p>0: Format not define, decided by code_bit assignment (ir_ccode_byte (reg_3D50h[15], ir_code_bit_num (reg_3D50h[14:8])).</p> <p>1: C16D8D8P format (ex: NEC, Toshiba format).</p> <p>2: C8D8 format (ex: Mitsubishi, Konka format).</p> <p>3: C4D8C4D8P format (ex: RCA format).</p> <p>4: C26D8D8P format.</p> <p>5: C32D8D8P format.</p> <p>6: C5D6C5D6P format.</p> <p>7: C6D6C6D6P format.</p> <p>8: D7C6 format (ex: Sony-D7C6).</p> <p>9: D7C8 format (ex: Sony-D7C8).</p> <p>10: D8C6 format (ex: Sony-D8C6).</p> <p>11: D5_only format (ex: MV500).</p> <p>12: S1C4D6 format (ex: IRT1250).</p> <p>13: C5D6D4 format (ex: LR3715M).</p> <p>14: R1T1C3D6 format (ex: M3004 LAB1-Carrier).</p> <p>15~31: Reserved.</p> <p>Note:</p> <p>S = System Code.</p> <p>C = Customer Code Bits, (ex: C8= customer code 8bits).</p> <p>D = Data (Key) Code Bits, (ex: D8= data code 8bits).</p> <p>P = Format with Parity Check (ex: 3th byte and 4th byte of NEC format).</p>

DDC Register (Bank = 3E)

DDC Register (Bank = 3E)				
Index (Absolute)	Mnemonic	Bit	Description	
00h (3E00h)	REG3E00	7:0	Default : 0x00	Access : RO
	D2B_WBUF_RPORT_A0[7:0]	7:0	DDC2Bi master write buffer, MCU read point of A0.	
00h (3E01h)	REG3E01	7:0	Default : 0x00	Access : R/W
	D2B_RBUF_WPORT_A0[7:0]	7:0	DDC2Bi master read buffer, MCU write point of A0.	
02h (3E04h)	REG3E04	7:0	Default : 0x00	Access : RO
	D2B_WBUF_RPORT_D0[7:0]	7:0	DDC2Bi master write buffer, MCU read point of D0.	
02h (3E05h)	REG3E05	7:0	Default : 0x00	Access : R/W
	D2B_RBUF_WPORT_D0[7:0]	7:0	DDC2Bi master read buffer, MCU write point of D0.	
04h (3E08h)	REG3E08	7:0	Default : 0x00	Access : WO
	D2B_RBUF_WPORT_PULSE_A0	7	MCU write pulse generate for D2B RBUF_A0.	
	-	6	Reserved.	
	D2B_RBUF_WPORT_PULSE_D0	5	MCU write pulse generate for D2B RBUF_D0.	
	-	4:0	Reserved.	
04h (3E09h)	REG3E09	7:0	Default : 0x00	Access : R/W
	-	7:2	Reserved.	
	EN_NO_ACK	1	DDC2Bi does not send ack if data buffer has not been read by cpu. 0: Disable. 1: Enable.	
	-	0	Reserved.	
05h (3E0Ah)	REG3E0A	7:0	Default : 0x00	Access : R/W
	D2B_ID_A0[7:0]	7:0	[7] DDC2Bi Enable for A0. [6:0] DDCBi ID[7:1] for A0.	
06h (3E0Ch)	REG3E0C	7:0	Default : 0x00	Access : R/W
	D2B_ID_D0[7:0]	7:0	[7] DDC2Bi Enable for D0. [6:0] DDCBi ID[7:1] for D0.	
07h (3E0Eh)	REG3E0E	7:0	Default : 0x00	Access : RO
	C_LAT_SRAM_DATA_A0[7:0]	7:0	DDC Data Read Port for ADC Sram. Cpu read ADC sram data.	
07h (3E0Fh)	REG3E0F	7:0	Default : 0x00	Access : RO
	C_LAT_SRAM_DATA_D0[7:0]	7:0	DDC Data Read Port for DVI Sram. Cpu read DVI sram data.	

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description
08h (3E10h)	REG3E10	7:0	Default : 0x00 Access : RO
	-	7	Reserved.
	D2B_INT_FINAL_STATUS_A0[6:0]	6:0	[6] DDC2Bi Start interrupt flag. [5] DDC2Bi Stop interrupt flag. [4] DDC2Bi Data Read interrupt flag. (write data into rbuf to clear). [3] DDC2Bi Data Write interrupt flag. (read data from wbuf to clear). [2] The 8th bit of the ID, interrupt flag. 0: Write. 1: Read.(RO, update automatically). [1] WADR interrupt flag. 1: The data in wbuf is the 2nd byte.(WADR). 0: The data in wbuf is not the 2nd byte(Not WADR). [0] DDC2Bi ID interrupt flag.
09h (3E12h)	REG3E12	7:0	Default : 0x00 Access : RO
	-	7	Reserved.
	D2B_INT_FINAL_STATUS_D0[6:0]	6:0	[6] DDC2Bi Start interrupt flag. [5] DDC2Bi Stop interrupt flag. [4] DDC2Bi Data Read interrupt flag. (write data into rbuf to clear). [3] DDC2Bi Data Write interrupt flag. (read data from wbuf to clear). [2] The 8th bit of the ID, interrupt flag. 0: Write. 1: Read.(RO, update automatically). [1] WADR interrupt flag. 1: The data in wbuf is the 2nd byte.(WADR). 0: The data in wbuf is not the 2nd byte(Not WADR). [0] DDC2Bi ID interrupt flag.
0Ah (3E14h)	REG3E14	7:0	Default : 0x06 Access : R/W
	-	7	Reserved.
	D2B_INT_MASK_A0[6:0]	6:0	[6] DDC2Bi Start interrupt mask. [5] DDC2Bi Stop interrupt mask. [4] DDC2Bi Data Read interrupt mask. (write data into rbuf to clear). [3] DDC2Bi Data Write interrupt mask. (read data from wbuf to clear).

DDC Register (Bank = 3E)				
Index (Absolute)	Mnemonic	Bit	Description	
			[2] The 8th bit of the ID, interrupt mask. 0: Write. 1: Read.(RO, update automatically). [1] WADR interrupt mask. 1: The data in wbuf is the 2nd byte.(WADR). 0: The data in wbuf is not the 2nd byte(Not WADR). [0] DDC2Bi ID interrupt flag.	
0Bh (3E16h)	REG3E16	7:0	Default : 0x06	Access : R/W
	-	7	Reserved.	
	D2B_INT_MASK_D0[6:0]	6:0	[6] DDC2Bi Start interrupt flag. [5] DDC2Bi Stop interrupt flag. [4] DDC2Bi Data Read interrupt flag. (write data into rbuf to clear). [3] DDC2Bi Data Write interrupt flag. (read data from wbuf to clear). [2] The 8th bit of the ID, interrupt mask. 0: Write. 1: Read.(RO, update automatically). [1] WADR interrupt mask. 1: The data in wbuf is the 2nd byte.(WADR). 0: The data in wbuf is not the 2nd byte(Not WADR). [0] DDC2Bi ID interrupt flag.	
0Ch (3E18h)	REG3E18	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	D2B_INT_FORCE_A0[6:0]	6:0	Force the d2b_int_final_status_a0 to 1. By setting each of the related bit to 1.	
0Dh (3E1Ah)	REG3E1A	7:0	Default : 0x00	Access : R/W
	-	7	Reserved.	
	D2B_INT_FORCE_D0[6:0]	6:0	Force the d2b_int_final_status_d0 to 1. By setting each of the related bit to 1.	
0Eh (3E1Ch)	REG3E1C	7:0	Default : 0x00	Access : WO
	-	7	Reserved.	
	D2B_INT_CLR_A0[6:0]	6:0	Clear the d2b_int_final_status_a0 to 0. By setting each of the related bit to 1.	
0Fh (3E1Eh)	REG3E1E	7:0	Default : 0x00	Access : WO
	-	7	Reserved.	

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description
	D2B_INT_CLR_D0[6:0]	6:0	Clear the d2b_int_final_status_d0 to 0. By setting each of the related bit to 1.
21h (3E42h)	REG3E42	7:0	Default : 0x00 Access : WO
	D0_CLR_DIRTY	7	Clear dirty bit for DVI_0 (clear pulse generate). 0: Not clear. 1: Clear.
	A0_CLR_DIRTY	6	Clear dirty bit for ADC_0 (clear pulse generate). 0: Not clear. 1: Clear.
	-	5:0	Reserved.
21h (3E43h)	REG3E43	7:0	Default : 0x00 Access : R/W, WO
	EN_WDATA_CLK_D0	7	DVI sram write data pulse gen when cpu write. 0: Not gen pulse. 1: Gen pulse.
	CPURRO_ST_0_D0	6	DVI sram read pulse gen when cpu read. 0: Not gen pulse. 1: Gen pulse.
	EN_WDATA_CLK_A0	5	ADC sram write data pulse gen when cpu write. 0: Not gen pulse. 1: Gen pulse.
	CPURRO_ST_0_A0	4	ADC sram read pulse gen when cpu read. 0: Not gen pulse. 1: Gen pulse.
	-	3:2	Reserved.
	D0_EN_READ	1	DDC SRAM Read/Write enable for DVI SRAM. 0: Write. 1: Read.
	-	0	Reserved.
22h (3E44h)	REG3E44	7:0	Default : 0x00 Access : RO, R/W, WO
	CHK_SUM_OK	7	DDC Check Sum.(256Bytes), (R.O). 0: Not OK. 1: OK.
	CHK1ST_SUM_OK	6	DDC Check Sum1.(128Bytes), (R.O). 0: Not OK. 1: OK.
	MASTER_FINISH	5	DDC Master function Finish.

DDC Register (Bank = 3E)				
Index (Absolute)	Mnemonic	Bit	Description	
			(R.O). 0: Not finish. 1: Finish.	
	MASTER_OK	4	Master OK. (write 128 bytes with acknowledgement received), (R.O). 0: Not OK. 1: OK.	
	F128_DVI	3	First 128 bytes send to DVI (second 128 send to ADC). 0: Is DVI. 1: Is ADC.	
	SEL_256	2	Master moves from EEPROM. 0: 128 bytes. 1: 256 bytes.	
	MASTER_ENABLE	1	Master disable/Enable. 0: Disable. 1: Enable.	
	MASTER_START	0	Soft Master stop/Start. Trigger. 0: Stop. 1: Start.	
22h (3E45h)	REG3E45	7:0	Default : 0x00	Access : RO, R/W
	D0_DDC_EN	7	DDC function Enable for DVI_0. 0: Disable. 1: Enable.	
	FILTER_ON	6	DDC Filter. 0: Disable. 1: Enable.	
	D0_DDCW_PROTECT	5	DDC I2C bus Write Protect for DVI_0 port. 0: Not protected. 1: Protected.	
	BYPASS_DDC	4	Bypass DDC. 0: Disable. 1: Enable.	
	BYPASS_SEL_DVI	3	Bypass Select DVI. 0: ADC. 1: DVI.	

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description
	D0_DDC_BUSY	2	DDC Busy for DVI_0 (read only). 0: Not busy. 1: Busy.
	D0_LAST_RW	1	DDC last Read/Write status for DVI_0 (read only). 0: Write. 1: Read.
	D0_DIRTY_BIT	0	DDC SRAM Dirty status for DVI_0 (read only). 0: Not dirty. 1: Dirty.
23h (3E46h)	REG3E46	7:0	Default : 0x00 Access : RO, R/W
	FILTER_MSB	7	DDC Filter Msb.
	D0_LAST_ADR[6:0]	6:0	DDC Last R/W address for DVI_0.
23h (3E47h)	REG3E47	7:0	Default : 0x00 Access : R/W
	D0_CPU_ADR[7:0]	7:0	DDC Address Port for CPU read/write for DVI_0.
24h (3E48h)	REG3E48	7:0	Default : 0x00 Access : R/W
	D0_CPU_WDATA[7:0]	7:0	DDC Data Port for CPU write for DVI_0.
24h (3E49h)	REG3E49	7:0	Default : 0x00 Access : RO, R/W
	A0_DDC_EN	7	DDC function Enable for ADC_0. 0: Disable. 1: Enable.
	-	6	Reserved.
	A0_DDCW_PROTECT	5	DDC I2C bus Write Protect for ADC_0 port. 0: Not protected. 1: Protected.
	SLEW_SEL[1:0]	4:3	Slew Rate Control. 00: Bypass. 01: Drive 1 cycle. 10: Drive 2 cycles. 11: Drive 3 cycles.
	A0_DDC_BUSY	2	DDC Busy for ADC_0 (read only). 0: Not busy. 1: Busy.
	A0_LAST_RW	1	DDC last Read/Write status for ADC_0 (read only). 0: Write. 1: Read.
	A0_DIRTY_BIT	0	DDC SRAM Dirty status for ADC_0 (read only).

DDC Register (Bank = 3E)				
Index (Absolute)	Mnemonic	Bit	Description	
			0: Not dirty. 1: Dirty.	
25h (3E4Ah)	REG3E4A	7:0	Default : 0x80	Access : RO, R/W
	-	7	Reserved.	
	A0_LAST_ADR[6:0]	6:0	DDC Last R/W address for ADC_0. (read only).	
25h (3E4Bh)	REG3E4B	7:0	Default : 0x00	Access : R/W
	A0_EN_READ	7	DDC SRAM Read/Write enable for ADC SRAM. 0: Write. 1: Read.	
	A0_CPU_ADR[6:0]	6:0	DDC address port for CPU read/write for ADC_0.	
26h (3E4Ch)	REG3E4C	7:0	Default : 0x00	Access : R/W
	A0_CPU_WDATA[7:0]	7:0	DDC Data Port for cpu write for ADC_0.	
30h (3E60h)	REG3E60	7:0	Default : 0x80	Access : R/W
	HDMI_256_EN	7	HDMI sram 256 enable. (allow DVI SRAM256x8 instead of SRAM128x8).	
	BYPASS_SEL_0	6	DDC bypass source port selection. If BYP_SEL_DVI==1. 0: Choose D1. 1: Choose D0.	
	-	5:0	Reserved.	
3Ah (3E74h)	REG3E74	7:0	Default : 0x22	Access : RO, R/W
	-	7:6	Reserved.	
	HDCP_EN	5	HDCP Enable for ddc. 0: Not enable. 1: Enable.	
	-	4:3	Reserved.	
	HDCP_MA_FINISH	2	HDCP master finish (Read Only).	
	ENWRITE_HDCP	1	Enable cpu write (for hdcp sram/74reg). 0: Not enable. 1: Enable.	
	HDCP_SRAM_ACCESS	0	HDCP sram access enable (1 for cpu; 0 for 74reg access). 0: Access HDCP 74reg. 1: Access HDCP sram.	

DDC Register (Bank = 3E)

Index (Absolute)	Mnemonic	Bit	Description
3Bh (3E76h)	REG3E76	7:0	Default : 0x00 Access : R/W
	CPU_ADR_REG[7:0]	7:0	CPU r/w address (for hdcp_key_sram/74reg).
3Bh (3E77h)	REG3E77	7:0	Default : 0x00 Access : R/W
	-	7:2	Reserved.
	CPU_ADR_REG[9:8]	1:0	See description of '3E76h'.
3Ch (3E78h)	REG3E78	7:0	Default : 0x00 Access : R/W
	CPU_WDATA_REG[7:0]	7:0	CPU write data port (for hdcp_key_sram/74reg).
3Ch (3E79h)	REG3E79	7:0	Default : 0x00 Access : RO
	HDCP_DATA_PORT_RD[7:0]	7:0	HDCP read data port (for hdcp_key_sram/74reg).
3Dh (3E7Ah)	REG3E7A	7:0	Default : 0x00 Access : WO
	-	7:3	Reserved.
	LOAD_ADR_P	2	HDCP address load pulse generate. 0: Not gen pulse. 1: Gen pulse.
	HDCP_DATA_WR_P	1	HDCP data write port pulse generate. 0: Not gen pulse. 1: Gen pulse.
	HDCP_DATA_RD_P	0	HDCP data read port pulse generate. 0: Not gen pulse. 1: Gen pulse.
3Dh (3E7Bh)	-	7:0	Default : - Access : -
	-	-	Reserved.
3Eh (3E7Ch)	REG3E7C	7:0	Default : 0x80 Access : R/W
	RSTZ_SW_DDC	7	Software reset for DDC (low active).
	-	6:0	Reserved.

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
2009/04/25		Y Create first version.

This page is intended to be left blank.