MSD3393LU
Single Chip Digital TV Solution Compliant with ATSC Standard

Preliminary Data Sheet

Version 0.1

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REVISION HISTORY

Revision No.	Description	Date
0.1	Ÿ Initial release	10/22/2012

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FEATURES

MSD3393LU is a highly integrated single chip solution for digital ATSC TV system. Key features include:

1. *Digital and Analog TV Front-End Demodulator*
2. *Multi-Standard A/V Format Decoder*
3. *The MStarACE6^{UC} Video Processor*
4. *Home Theater Sound Processor*
5. *Embedded Memory for optimized BOM cost*
6. *Multiple HDMI 1.4 Compliant Ports with ARC Support*
7. *One MHL 2.0 Compliant Port*

- High Performance Micro-processor
  - High speed/performance 32-bit RISC CPU
  - One full duplex UARTs
  - Supports USB and ISP programming
  - DMA Engine
- MPEG-2 Video Decoder
  - ISO/IEC 13818-2 MPEG-2 video MP@HL
  - Automatic frame rate conversion
  - Supports resolution up to HDTV (1080i, 720p) and SDTV
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding
  - Supports resolutions up to HDTV (1080p@30fps)
  - Supports DivX[1] Home Theater & HD profiles[Optional]
  - Supports VC-1, FLV video format decoding
- H.264 Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.1) video decoding
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports resolution up to 1080p@30fps
  - Supports CABAC and CAVLC stream types
  - Processing of ES and PES streams, extraction and provision of time stamps
  - Supports Bitrate up to 40 Mbits (Blu-ray spec.)
- RealMedia Decoder[Optional]
  - Supports maximum resolution up to 1080p@30fps
  - Supports RV8, RV9, RV10, and RA8-LBR decoders
  - Supports file formats with RM and RMVB
  - Supports Picture Re-sampling
  - Supports in-loop de-block for B-frame
- AVS Video Decoder[Optional]
  - Jizhun profile, level 6.0
  - Max. resolutions up to 1920x1080@30fps
  - Supports bit rate up to 20Mbps
- Hardware JPEG
  - Supports sequential mode, single scan
  - Supports both color and grayscale pictures
  - Following the file header scan the hardware decoder fully handles the decode process
  - Supports programmable Region of Interest (ROI)
  - Supported formats: 422/411/420/444/422T
  - Supported scaling down ratios: 1/2, 1/4, 1/8
  - Supports picture rotation
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Two configurable CVBS & Y/C S-video inputs
  - Supports Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE

[1] **Trademark of DivX, Inc.**

Optional **Please contact MStar sales for the correct suffix.**

- **Multi-Standard TV Sound Processor**
  - SIF audio decoding
  - Supports BTSC/A2/EIA-J demodulation
  - Supports FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC/ EIA-J mode
  - Supports Mono/Stereo/Dual in A2 mode
  - Built-in audio sampling rate conversion (SRC)
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
  - Advanced sound processing options available, for example: Dolby[1], SRS[2], BBE[3], QSound[4]
  - Supports digital audio format decoding:
    - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3) Optional, AAC-LC, WMA
    - Dolby Digital Plus Optional
- **Audio Interface**
  - Three L/R audio line-inputs
  - Two L/R outputs for main speakers and additional line-outputs
  - HDMI audio channel processing
  - Programmable delay for audio/video synchronization
- **Analog RGB Compliant Input Ports**
  - Two analog ports support up to 1080P
  - Supports PC RGB input up to SXGA@75Hz
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG Sync-on-Green
  - Automatic color calibration
  - AV-link support
- **Analogue RGB Auto-Configuration & Detection**
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
  - Sync Detection for H/V Sync
- **DVI/HDCP/HDMI Compliant Input Ports**
  - Three HDMI/MHL/DVI Input ports
  - HDMI 1.3/1.4 Compliant
  - HDCP 1.2 Compliant
  - 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
  - Supports CEC
  - Supports HDMI 4Kx2K input
  - Supports HDMI ARC
  - Single link DVI 1.0 compliant
  - Robust receiver with excellent long-cable support
- **HDMI/MHL Dual-Purpose Port**
  - MHL 2.0 Compliant
  - MHL/HDMI Auto-detection
  - Supports MHL charging in normal/standby mode
- **MStar Advanced Color Engine (MStarACE-6^{UC})**
  - 10-bit Data Processing Path
  - Fully programmable multi-function scaling engine
    - Nonlinear video scaling supports various modes including Panorama
    - Supports dynamic scaling for RM, VC-1
  - Advanced video processing engine
    - MStar Ultra-Clear video deinterlacer with edge and artifact smoother
    - MStar Ultra-Clear Noise Reduction Engine
    - Edge-oriented deinterlacer with edge and artifact smoother
    - Automatic 3:2/2:2/M:N pull-down detection and recovery
    - 3D noise reduction for lousy air/cable input
    - Automatic de-blocking
    - MStar Cross-Color Compression Technology
    - Arbitrary frame rate conversion
  - MStar Professional Picture Enhancement:
    - Dynamic brilliant and fresh color
    - Dynamic *Blue Stretch*
    - Intensified contrast and details
    - Dynamic *Vivid Skin*
    - Dynamic sharpened Luma/Chroma edges
    - Global and local dynamic depth of field perception
    - Accurate and independent color control
    - Supports sRGB and xvYCC color processing
    - Supports HDMI 1.3 deep color format
  - Programmable 12-bit RGB gamma CLUT

[1] **Trademark of Dolby Laboratories**
[2] **Trademark of SRS Labs, Inc.**
[3] **Registered trademark of BBE Sound, Inc.**
[4] **Registered trademark of QSound Labs, Inc.**
Optional **Please see Ordering Guide for details.**

- Output Interface
  - Single/dual link 8-bit LVDS output
  - Supports panel resolution up to Full-HD (1920x1080) @ 60Hz
  - Supports TH/TI format
  - Supports dithering options to 6/8-bit output
  - Spread spectrum output for EMI suppression
  - Supports 60Hz 3D passive panel (Line alternative mode)
- CVBS Video Outputs
  - Supports CVBS bypass output
- 2D Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill, text draw and trapezoid draw
  - BitBlt, stretch BitBlt, trapezoid BitBlt, mirror BitBlt and rotate BitBlt
  - Supports alpha and destination alpha compare
  - Raster Operation (ROP)
- Porter-Duff VIF Demodulator
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
  - Digital low IF architecture
  - Audio/Video dual-path processor
  - Stepped-gain PGA with 25 dB tuning range and 1 dB tuning resolution
  - Maximum IF gain of 37 dB
  - Programmable TOP to accommodate different tuner gain and SAW filter insertion loss to optimize noise and linearity performance
  - Multi-standard processing with dual SAW or sawless
  - Supports silicon tuner low IF output architecture
- ATSC/QAM Demodulator
  - ATSC A/53 compliant 8VSB
  - ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
  - Integrated 11-bit A/D converter (for optional external A/D converter support)
  - All digital demodulation
  - Integrated deinterleaver RAM for all modes (No need of external memory for deinterleaver)
  - Supports 44MHz IF input
  - Supports no SAW for any application
- Connectivity
  - Two USB 2.0 host ports
  - USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Miscellaneous
  - Bootable SPI interface with serial flash support
  - Lower power standby mode
  - 128-pin EPLQFP package
  - Operating Voltages: 1.15V (core), 1.8V and 3.3V (I/O and analog)

GENERAL DESCRIPTION

MSD3393LU is a highly integrated TV SoC solution for ATSC digital television platform. Integrating latest advanced technologies from MStar Semiconductor, the world leading TV SoC provider in TV industry, MSD3393LU provides the most cost-efficient solution for multimedia TV application with creative and attractive features exclusively presented.

In order to achieve the lowest BOM cost in a multi-media TV platform, MSD3393LU integrates DTV, ATSC/QAM demodulator, TV/multi-media all-purpose AV decoder, VIF demodulator, and advanced Sound/Video processors into a single device. This not only reduces the overall BOM significantly, but also facilitates the design of originally-complicated TV systems for developers. In addition, the memory-embedded solution provided by MSD3393LU can reduce the excessive work of memory interface routing on board and the risk of memory performance degradation while powering cost-down in the total system.

The powerful multimedia A/V decoder inside MSD3393LU is hosted with a dedicated hardware video codec engine to secure fast and stable video streaming playback. Moreover, MSD3393LU is equipped with a DSP specifically designated for audio application, including digital audio format decoding and advanced sound effects, and a high performance RISC CPU to manipulate all possible routines and house-keeping activities. With extendable USB 2.0 interface, an MSD3393LU based system can turn into a high quality media-center in a simple manner.

MSD3393LU supports the latest MHL technology, which allows user to stream audio and full HD video from mobile devices to televisions. Power management and low-power design of MSD3393LU makes it possible to charge MHL devices even in standby mode. The MHL/HDMI dual-purpose port on MSD3393LU will enable charging if MHL devices are automatically detected.

For standard users, the MSD3393LU provides multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. The built-in audio decoder is capable of decoding FM, AM, A2, BTSC and EIA-J sound standards. MSD3393LU also supplies all the necessary A/V inputs and outputs to complete a receiver design including HDMI receivers and component video ADCs. All input selection multiplexers for video and audio are integrated, including full SCART support with CVBS output. The equipped MStar MStarACE-6 color engine is the latest masterpiece of MStar technologies, providing excellent video and picture quality in Full-HD and large-scale display system. MSD3393LU also supports an ultra low power standby mode to meet the latest energy legislative requirements without any additional hardware.

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		TBD		LSB
Integral Nonlinearity		TBD		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum		0.5		V p-p
Maximum		TBD		V p-p
Input Bias Current			1	uA
SWITCHING PERFORMANCE				
Maximum Conversion Rate	170			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		170	MHz
PLL Jitter		TBD		ps p-p
Sampling Phase Tempco		TBD		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		0.3		V
Output High		1.3		V
AUDIO				
ADC Input		2.8		V p-p
DAC Output		2.8		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p
SAR ADC Input	0		3.3	V
FB ADC Input*	0		1.2	V

Specifications subject to change without notice.
Note: Input full scale is 1.2V, but input range is 0 ~ 3.3V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
1.8V Supply Voltages	$V_{VDD\ 18}$	1.70		1.90	V
1.15V Supply Voltages	V_{VDD_115}	1.12	1.15	1.18	V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
3.3V Supply Voltages	V_{VDD_33}		3.6	V
1.8V Supply Voltages	V_{VDD_18}		1.99	V
1.15V Supply Voltages	V_{VDD_115}		1.2	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C

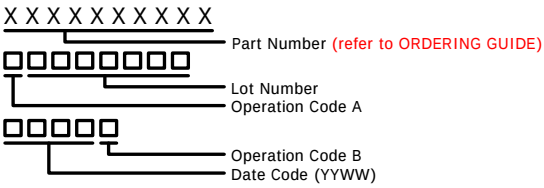
Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MSD3393LB	0°C to +70°C	EPLQFP	156-pin
MSD3393LB-XX	0°C to +70°C	EPLQFP	156-pin

Note:
XX suffix represents advanced features. Please contact MStar sales for details.

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MSD3393LB comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REGISTER DESCRIPTION

MIU1 Register (Bank = 1006)

MIU1 Register (Bank = 1006)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (100600h)	**REG100600**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	AUTO_REF_OFF	5	Turn off auto refresh.	
	ODT	4	Turn on ODT (only for DDR2/DDR3).	
	RSTZ	3	DRAM reset.	
	CS	2	DRAM chip select.	
	CKE	1	Enable CKE.	
	INIT_MIU	0	Auto initial DRAM cycle.	
00h (100601h)	**REG100601**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_INIT_DONE	7	Auto initial DRAM cycle done flag.	
	R_SINGLE_CMD_DONE	6	Single command done flag.	
	SELF_REFRESH	5	Enter self refresh mode.	
	-	4	Reserved.	
	SINGLE_CMD[2:0]	3:1	Single command = {rasz, casz, wez}.	
	SINGLE_CMD_EN	0	Issue single command.	
01h (100602h)	**REG100602**	**7:0**	**Default : 0x00**	**Access : R/W**
	CA_SIZE[1:0]	7:6	00: 8col. 01: 9col. 10: 10col. 11: Reserved.	
	BA_SIZE[1:0]	5:4	00: 2ba. 01: 4ba. 10: 8ba. 11: Reserved.	
	DRAM _BUS[1:0]	3:2	00: 16-bit. 01: 32-bit. 10: 64-bit. 11: Reserved.	
	DRAM _TYPE[1:0]	1:0	00: SDR. 01: DDR. 10: DDR2. 11: DDR3.	
01h	**REG100603**	**7:0**	**Default : 0xF0**	**Access : R/W**

MIU1 Register (Bank = 1006)

Index (Absolute)	Mnemonic	Bit	Description	
	CKO_OENZ	7	Ck output enable.	
	ADR_OENZ	6	Address output enable.	
	DQ_OENZ	5	Data output enable.	
	CKE_OENZ	4	CKE output enable.	
	DATA_SWAP[1:0]	3:2	01: [15:0]. 10: [31:16].	
	DATA_RATIO[1:0]	1:0	00: 1x. 01: 2x. 10: 4x. 11: 8x.	
02h (100604h)	**REG100604**	**7:0**	**Default : 0x09**	**Access : R/W**
	I64_MODE	7	0: All 128 internal bus. 1: Support 64 internal bus (only 4x mode).	
	-	6:5	Reserved.	
	RD_TIMING[4:0]	4:0	Read back data delay timing.	
03h (100606h)	**REG100606**	**7:0**	**Default : 0x08**	**Access : R/W**
	TREFPERIOD[7:0]	7:0	Refresh cycle period, unit = 16 mclk.	
03h (100607h)	**REG100607**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	ODT_ALWAYS_ON	5	ODT always on.	
	CKE_ALWAYS_ON	4	CKE always on.	
	-	3	Reserved.	
	TCKE[2:0]	2:0	DRAM TCKE timing.	
04h (100608h)	**REG100608**	**7:0**	**Default : 0x33**	**Access : R/W**
	TRP[3:0]	7:4	DRAM TRP timing.	
	TRCD[3:0]	3:0	DRAM TRCD timing.	
04h (100609h)	**REG100609**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	TRAS[4:0]	4:0	DRAM TRAS timing.	
05h (10060Ah)	**REG10060A**	**7:0**	**Default : 0x12**	**Access : R/W**
	TRTP[3:0]	7:4	DRAM TRTP timing.	
	TRRD[3:0]	3:0	DRAM TRRD timing.	
05h (10060Bh)	**REG10060B**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:6	Reserved.	

MIU1 Register (Bank = 1006)

Index (Absolute)	Mnemonic	Bit	Description	
	TRC[5:0]	5:0	DRAM TRC timing.	
06h (10060Ch)	**REG10060C**	**7:0**	**Default : 0x61**	**Access : R/W**
	TWR[3:0]	7:4	DRAM TWR timing: write recovery time.	
	TWL[3:0]	3:0	DRAM TWL timing: write latency.	
06h (10060Dh)	**REG10060D**	**7:0**	**Default : 0x63**	**Access : R/W**
	TRTW[3:0]	7:4	Read to write delay.	
	TWTR[3:0]	3:0	DRAM TWTR timing: write to read delay.	
07h (10060Eh)	**REG10060E**	**7:0**	**Default : 0x0E**	**Access : R/W**
	TRFC[7:0]	7:0	DRAM TRFC timing.	
07h (10060Fh)	**REG10060F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	TCCD[2:0]	6:4	DRAM TCCD timing.	
	-	3:0	Reserved.	
08h (100610h)	**REG100610**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[7:0]	7:0	Mode register 0.	
08h (100611h)	**REG100611**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[15:8]	7:0	See description of '101210h'.	
09h (100612h)	**REG100612**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR1[7:0]	7:0	Mode register 1.	
09h (100613h)	**REG100613**	**7:0**	**Default : 0x40**	**Access : R/W**
	MR1[15:8]	7:0	See description of '101212h'.	
0Ah (100614h)	**REG100614**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR2[7:0]	7:0	Mode register 2.	
0Ah (100615h)	**REG100615**	**7:0**	**Default : 0x80**	**Access : R/W**
	MR2[15:8]	7:0	See description of '101214h'.	
0Bh (100616h)	**REG100616**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR3[7:0]	7:0	Mode register 3.	
0Bh (100617h)	**REG100617**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MR3[15:8]	7:0	See description of '101216h'.	

MIU0 Register (Bank = 1012)

MIU0 Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (101200h)	**REG101200**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	AUTO_REF_OFF	5	Turn off auto refresh.	
	ODT	4	Turn on ODT (only for DDR2/DDR3).	
	RSTZ	3	DRAM reset.	
	CS	2	DRAM chip select.	
	CKE	1	Enable CKE.	
	INIT_MIU	0	Auto initial DRAM cycle.	
00h (101201h)	**REG101201**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_INIT_DONE	7	Auto initial DRAM cycle done flag.	
	R_SINGLE_CMD_DONE	6	Single command done flag.	
	SELF_REFRESH	5	Enter self refresh mode.	
	-	4	Reserved.	
	SINGLE_CMD[2:0]	3:1	Single command = {rasz, casz, wez}.	
	SINGLE_CMD_EN	0	Issue single command.	
01h (101202h)	**REG101202**	**7:0**	**Default : 0x00**	**Access : R/W**
	CA_SIZE[1:0]	7:6	00: 8col. 01: 9col. 10: 10col. 11: Reserved.	
	BA_SIZE[1:0]	5:4	00: 2ba. 01: 4ba. 10: 8ba. 11: Reserved.	
	DRAM _BUS[1:0]	3:2	00: 16-bit. 01: 32-bit. 10: 64-bit. 11: Reserved.	
	DRAM _TYPE[1:0]	1:0	00: SDR. 01: DDR. 10: DDR2. 11: DDR3.	
01h (101203h)	**REG101203**	**7:0**	**Default : 0xF0**	**Access : R/W**
	CKO_OENZ	7	Ck output enable.	

MIU0 Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADR_OENZ	6	Address output enable.	
	DQ_OENZ	5	Data output enable.	
	CKE_OENZ	4	CKE output enable.	
	DATA_SWAP[1:0]	3:2	01: [15:0]. 10: [31:16].	
	DATA_RATIO[1:0]	1:0	00: 1x. 01: 2x. 10: 4x. 11: 8x.	
02h (101204h)	**REG101204**	**7:0**	**Default : 0x09**	**Access : R/W**
	I64_MODE	7	0: All 128 internal bus. 1: Support 64 internal bus (only 4x mode).	
	-	6:5	Reserved.	
	RD_TIMING[4:0]	4:0	Read back data delay timing.	
03h (101206h)	**REG101206**	**7:0**	**Default : 0x08**	**Access : R/W**
	TREFPERIOD[7:0]	7:0	Refresh cycle period, unit = 16 mclk.	
03h (101207h)	**REG101207**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	ODT_ALWAYS_ON	5	ODT always on.	
	CKE_ALWAYS_ON	4	CKE always on.	
	-	3	Reserved.	
	TCKE[2:0]	2:0	DRAM TCKE timing.	
04h (101208h)	**REG101208**	**7:0**	**Default : 0x33**	**Access : R/W**
	TRP[3:0]	7:4	DRAM TRP timing.	
	TRCD[3:0]	3:0	DRAM TRCD timing.	
04h (101209h)	**REG101209**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	TRAS[4:0]	4:0	DRAM TRAS timing.	
05h (10120Ah)	**REG10120A**	**7:0**	**Default : 0x12**	**Access : R/W**
	TRTP[3:0]	7:4	DRAM TRTP timing.	
	TRRD[3:0]	3:0	DRAM TRRD timing.	
05h (10120Bh)	**REG10120B**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:6	Reserved.	
	TRC[5:0]	5:0	DRAM TRC timing.	

MIU0 Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
06h (10120Ch)	**REG10120C**	**7:0**	**Default : 0x61**	**Access : R/W**
	TWR[3:0]	7:4	DRAM TWR timing: write recovery time.	
	TWL[3:0]	3:0	DRAM TWL timing: write latency.	
06h (10120Dh)	**REG10120D**	**7:0**	**Default : 0x63**	**Access : R/W**
	TRTW[3:0]	7:4	Read to write delay.	
	TWTR[3:0]	3:0	DRAM TWTR timing: write to read delay.	
07h (10120Eh)	**REG10120E**	**7:0**	**Default : 0x0E**	**Access : R/W**
	TRFC[7:0]	7:0	DRAM TRFC timing.	
07h (10120Fh)	**REG10120F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	TCCD[2:0]	6:4	DRAM TCCD timing.	
	-	3:0	Reserved.	
08h (101210h)	**REG101210**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[7:0]	7:0	Mode register 0.	
08h (101211h)	**REG101211**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[15:8]	7:0	See description of '101210h'.	
09h (101212h)	**REG101212**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR1[7:0]	7:0	Mode register 1.	
09h (101213h)	**REG101213**	**7:0**	**Default : 0x40**	**Access : R/W**
	MR1[15:8]	7:0	See description of '101212h'.	
0Ah (101214h)	**REG101214**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR2[7:0]	7:0	Mode register 2.	
0Ah (101215h)	**REG101215**	**7:0**	**Default : 0x80**	**Access : R/W**
	MR2[15:8]	7:0	See description of '101214h'.	
0Bh (101216h)	**REG101216**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR3[7:0]	7:0	Mode register 3.	
0Bh (101217h)	**REG101217**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MR3[15:8]	7:0	See description of '101216h'.	

SC0 IPMUX Register (Bank = 102E)

SC0 IPMUX Register (Bank = 102E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102E02h)	**REG102E02**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPMUX_SEL2[3:0]	7:4	Input source select. 0: ADC A. 1: DVI_1. 2: VD. 3: MPEG2 VOP (DC0). 4: Reversed. 5: Ext VD. 6: ADC B. 7: Capture. 8: Mlink. D: MHL. Others: Debug mode.	
	IPMUX_SEL1[3:0]	3:0	Input source select. 0: ADC A. 1: DVI_1. 2: VD. 3: MPEG2 VOP (DC0). 4: Reversed. 5: Ext VD. 6: ADC B. 7: Capture. 8: Mlink. D: MHL. Others: Debug mode.	
01h (102E03h)	**REG102E03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IPMUX_SEL0[3:0]	3:0	Input source select. 0: ADC A. 1: DVI_1. 2: VD. 3: MPEG2 VOP (DC0). 4: Reversed. 5: Ext VD. 6: ADC B. 7: Capture. 8: Mlink. Others: Debug mode.	
46h	**-**	**7:0**	**Default : -**	**Access : -**

SC0 IPMUX Register (Bank = 102E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	-	-	Reserved.

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102F00h)	**REG102F00**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler.	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]: SWRST1[4]: IP, including F1 and F2. SWRST1[3]: OP, including OP1, VIP and VOP. SWRST1[2]: IP_F2. SWRST1[1]: IP_F1. SWRST1[0]: All engines.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PDMD[1:0]	1:0	PowerDown mode: 01: IDCLK. Others: IDCLK and ODCLK.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 VS INT Edge. 1: Tailing. 0: Leading.	
	IPVSINT_EDGE	0	IP VS INT Edge. 1: Tailing. 0: Leading.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CHG_HMD	0	CHG_HMD: H Change Mode for INT. 0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.	

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)

Index (Absolute)	Mnemonic	Bit	Description	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_SYNC_TO_GOP_SEL[1:0]	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.	
	GOP2IP_EN	5	GOP blending to IP enable.	
	-	4:0	Reserved.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GOP2IP_DATA_SEL[1:0]	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	COP_EN	7	Enable cop for VOP2.	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_7_0[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2.	

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_31_24[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2.	

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ.	

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
16h	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_7_0[7:0]	7:0	The raw status of interrupt source. D[7]: Vtt_CHG_INT_F1. D[6]: Vtt_LOSE_INT_F2. D[5]: VSINT. D[4]: Tune_fail_p. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)

Index (Absolute)	Mnemonic	Bit	Description	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_15_8[7:0]	7:0	The raw status of interrupt source. D[7]: IPHCs_DET_INT_F1. D[6]: IPHCs_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: Jitter_INT_F1. D[2]: Jitter_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_23_16[7:0]	7:0	The raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: Htt_CHG_INT_F1. D[2]: Htt_CHG_INT_F2. D[1]: IPHCs1_DET_INT_F1. D[0]: IPHCs1_DET_INT_F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_31_24[7:0]	7:0	The raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	

SC1 GOP_INT Register (Bank = 102F, Sub-Bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	See description of '102F48h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0xE1**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	WDT_EN	0	H/V sync lose watch dog timer count enable.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. #0: Enable. #1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. #00: Auto detected. #01: Input is separated HSYNC and VSYNC. #10: Input is Composite sync. #11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). #0: CSYNC. #1: SOG.	
	CSC_EN	3	Input CSC function. #0: Disable (RGB -> RGB, default). #1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. #000: Analog 1. #001: Analog 2. #010: Analog 3. #011: DVI. #100: Video. #101: Reserved. #111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. #0: Disable (Auto selected by h/W, used when input is video, default). #1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. #0: Sync is Generated from Data Internally. #1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Format.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. #00: External 8/10 bits video port. #01: Internal video decoder mode A.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			#10: External 16/20 bits video port. #11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. #0: Use DE as sample range, only V position can be adjusted. #1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. #0: Disable. #1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. #0: Delay 1/4 input HSYNC. #1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. #0: From HSYNC leading edge. #1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. #0: From VSYNC leading edge. #1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. #0: 8 lines. #1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. #0: Disable. #1: Enable.	
	HWRAP	0	Input image Horizontal wrap. #0: Disable. #1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. #1 : Display will adaptively follow the Source. If Display Select this source. #0 : Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change,	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. #0: Disable. #1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. #00: Normal. #01: 1. #10: 2. #11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. #0: Mask. #1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). #0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. #1: Use Hsync only. When ISEL = 011:(DVI). #0: Normal. #1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). #0: Normal. #1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). #0: Normal. #1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. #0: Normal. #1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. #0 : Use Separate Hs for Coast Period. #1 : Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. #0: Leading edge. #1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. #0: Auto Switch VST(04), VDC (06). #1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. #0000 : 8 Line Ahead from SPRange_Vst. #0001 : 1 Line Ahead from SPRange_Vst. #0010: 2 Line Ahead from SPRange_Vst. #0011: 3 Line Ahead from SPRange_Vst. .. #1111: 15 Line Ahead from SPRange_Vst.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0		
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0		
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	[0]: Htt change mask on. [1]: Vtt change mask on. [2]: Vtt change INT mask on. [4]: No_signal function off. [5]: No_signal with auto freeze.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetition.	
	-	6	Reserved.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DUMMY0C_2_5[3:0]	5:2		
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. #0 : HW Auto Decide. #1 : SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap support. #1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. #0: no down, 5 tap. #1: 2 to 1 down, 11 tap. Others: Reserved. For ExtVD = CCIR656, set to 0 and OverSap_En = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0		
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). #0: Normal. #1: Max value (255) value when ATG_Data_MD = 0. Output over max value (255) when ATG_Data_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0. Output over max value (255) when. ATG_Data_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). #0: Normal. #1: Max value (255) value when. ATG_Data_MD = 0.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description
			Output over max value (255) when. ATG_Data_MD = 1.
	ATG_CALMD	4	ADC Calibration Enable. #0: Disable. #1: Reserved.
	ATG_DATA_MD	3	Auto Gain Result selection. #0: Output has max/min value. #1: Output is overflow/underflow.
	ATG_HISMD	2	Auto Gain Mode. #0: Normal mode (result will be cleared every frame). #1: History mode (result remains not cleared till ATG_En = 0).
	ATG_READY	1	Auto Gain Result Ready. #0: Result not ready. #1: Result ready.
	ATG_EN	0	Auto Gain Function Enable. #0: Disable. #1: Enable.
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	-	7	Reserved.
	AV_DET	6	AV Detect for Cb Cr. #0 : CbCr Range is define by 03[2]. YCbCr_En. #1 : Cb Cr Min is defined in 89 ATP_GTH, Cb Cr Max is defined in 8A ATP_TH.
	-	5:3	Reserved.
	ATG_UPR	2	Min value flag for R channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.
	ATG_UPG	1	Min value flag for G channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATG_UPB	0	Min value flag for B channel. #0: Normal. #1: Min value present when ATG_CalMD = 0, ATG_Data_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. #0: Disable. #1: Enable.	
	OP2_COAST	6	. Coast Status (Read only). #0: Coast is inactive. #1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). #00: R/G/B total value. #01: Only R value. #10: Only G value. #11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. #1. VD. #2. Ext VD 656 Format. #3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. #000: Minimum R value. #001: Minimum G value. #010: Minimum G value. #011: Maximum R value. #100: Maximum G value. #101: Maximum B value. #11x: Reserved.	
0Fh	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DUMMY0F_8_15[7:0]	7:0		
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. #0: Left result. #1: right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. #0: Not clear. #1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. #0: Update every frame. #1: Keep the history value.	
	JITTER	3	JITTER function Result. #0: No JITTER. #1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. #0: Update every frame. #1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. #0: Result not ready. #1: Result ready.	
	ATS_EN	0	Auto position function Enable. #0: Disable. #1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	THOLD[3:0]	7:4	Auto position Valid Data Value. #0000: Valid if data >= 0000 0000. #0001: Valid if data >= 0001 0000. #0010: Valid if data >= 0010 0000. .. #1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Position Force Pixel Mode. #0 : DE or Pixel decide by the Source. #1 : Force Pixel Mode.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Auto Gain Value. (selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VSTDBUF[12:8]	4:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HSTDBUF[12:8]	4:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VEDDBUF[12:8]	4:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HEDDBUF[12:8]	4:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on Reg_10h[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	REG_JLST[12:8]	4:0	See description of '102F2Ch'.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. #111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	HTT change mask period.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. #000: Mask 0 bit, default value. #001: Mask 1 bit. #010: Mask 2 bit. #011: Mask 3 bit. #100: Mask 4 bit. #101: Mask 5 bit. #110: Mask 6 bit. #111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. #0: Result not ready. #1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. #0: Disable. #1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	VTT change mask period.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. #0: In display. #1: In blanking.	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Position Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Separator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. #0: Disable. #1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. #1: Default value.	
1Eh	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. #0: Not active. #1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. #0: Not active. #1: Active.	
	CS_DET	5	Composite Sync Detected status. #0: Input is not composite sync. #1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. #0: Input is not SOG. #1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. #0: Non-interlace. #1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. #0: Even. #1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. #0: Active low. #1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulse Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. #0: 1 line. #1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Separator Htt. #0 : Htt Report by Mode Detector. #1 : Htt Report by Sync Separator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. #0: Old method. #1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. #0: HSOUT (recommended). #1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. #0: Active low. #1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_VsPol).	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. #0: Active low. #1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_HsPol).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. #0: Non-interlace. #1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. #0: Use result of internal circuit detection. #1: Defined by user (Usr_IntLac).	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. #00 : Sample V End. #01 : Sample V Start. #10 : Sample V Start Ahead by Current Bank 09[3:0]. #11 : Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. #0 : Mode Change Provide in data clock Domain. #1 : Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. #0 : Form Input DE. #1 : From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_Video = 1 for Data Align. #0: Normal. #1: Invert.	
	EXT_FIELDMD	2	Video External Field. #0: Use result of internal circuit detection. #1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. #0: Use the HSYNC numbers of a field to judge. #1: Use the relationship of VSYNC and HSYNC to judge.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FIELD_INV	0	Interlace Field Invert. #0: Normal. #1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Separator VSYNC for Mode Detect. #0 : RAW VSYNC (H / V Relationship is Keep for Interlace Detect). #1 : HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + Video_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. #0: PC Source. #1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (Video_D1L_H + VIDEO_D1L_L) = #00: Delay 1 Line for Another Field. #01: Delay 2 Line for Another Field. #10: Delay 3 Line for Another Field. #11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). #0: Disable. #1: Enable.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when Coast_SrcS is 1). #0: Normal. #1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. #0: Internal Separated VSYNC.(Default). #1: External VSYNC.(Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. #00: Coast start from 1 HSYNC leading edge. #01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. #00: Coast end at 1 HSYNC leading edge. #01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. #0: Disable. #1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: #000: 0 XTAL clock. #001: 1 XTAL clock. #010: 2 XTAL clock. #111: 7 XTAL clock. DVI: #000: 0x8 input clock. #001: 1x8 input clock. #010: 2x8 input clock. #111: 7x8 input clock.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: #0: Filter off. #1: Filter on. When input source is DVI: #0: Normal. #1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. #0: Normal. #1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. #0: By counter overflow. #1: By counter overflow + Active Detect IPVs_Act, IPHs_Act (E1[7:6]). (recommended).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. #0: Normal. #1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1		
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). #0: Disable. #1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. #0: Disable. #1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). #0: Disable. #1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). #0: Disable. #1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. #0: Disable.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			#1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1		
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. #00: off. #01: Only for line total number is even. #10: all case. #11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. #0 : Define Automatically. #1 : Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. #0: Can gate the GOP clock. #1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. #0: Don't gate the idclk. #1: Can gate the idclk.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATS_B_SKIP	2	Auto search ignore B data.	
	ATS_G_SKIP	1	Auto search ignore G data.	
	ATS_R_SKIP	0	Auto search ignore R data.	
2Fh	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_BYPASS_MODE	7	Use input DE to replace SPRange_H as output DE.	
	-	6:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMber_offset.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync insert_number_offset enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMber_offset.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync lock_number_offset enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. #0x : reference 21[15:14]. #10 : Sample V end delay 1 line. #11 : Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MACROVISION_FILTER_RANGE[7:0]	7:0	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. #0: not valid. #1: valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. #0: 60 lines. #1: 120 lines.	
	MACROVISION_FILTER_SEL[1:0]	5:4	When MACROVISION_FILTER_EN is enable and input Hsync period is less than MACROVISION_FILTER_RANGE, this Hsync signal will be recognized as Macrovison or glitch and be filtered out in the coast region.	
	MACROVISION_FILTER_RANGE[11:8]	3:0	See description of '102F6Ah'.	
36h	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE_Q[7:0]	7:0	Auto Gain value latch by Vsync pulse.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE_Q[9:8]	1:0	See description of '102F7Eh'.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FDET_CHECK_EN	6	H/V sync status check enable.	
	FDET_H_INV	5	H sync invert.	
	FDET_V_INV	4	V sync invert.	
	FDET_VTOTAL_PIX_CNT_EN	3	V total count by pixel clock enable.	
	FDET_SYNC_SRC_SEL[1:0]	2:1	H/V sync source select for mode detection.	
	FDET_EN	0	New mode interlaced detect enable.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VWIDTH_TOR[7:0]	7:0	V sync pulse width tolerance.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VTOTAL_TOR[7:0]	7:0	V total tolerance.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FDET_STATUS_INTLAC_DET2	2	Mode detect result 2.	
	FDET_STATUS_INTLAC_DET1	1	Mode detect result 1.	
	FDET_STATUS_INTLAC_DET0	0	Mode detect result 0.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH0[7:0]	7:0	V sync pulse width 0.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH0[13:8]	5:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH1[7:0]	7:0	V sync pulse width 1.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH1[13:8]	5:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[7:0]	7:0	V total report 0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[23:16]	7:0	See description of '102F9Ah'.	

SC1 IP1_M Register (Bank = 102F, Sub-Bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL0[24]	0	See description of '102F9Ah'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[7:0]	7:0	V total report 1.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[23:16]	7:0	See description of '102F9Eh'.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL1[24]	0	See description of '102F9Eh'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[7:0]	7:0	V total report 2.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[23:16]	7:0	See description of '102FA2h'.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL2[24]	0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[7:0]	7:0	V total report 3.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[23:16]	7:0	See description of '102FA6h'.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL3[24]	0	See description of '102FA6h'.	
71h (102FE3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VOUT_PROC	5	VOUT_PROC.	
	HOUT_PROC	4	HOUT_PROC.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bits to 8-bits.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '102F08h'.	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode. 0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	PREV_DOWN_3D	4	PREV_DOWN_3D.	
	-	3:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x08**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP[1:0]	6:5	Cb/Cr swap for 444 to 422.	
	YDELAY_EN	4	Y delay enable.	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_DLY_WITH_Y	3	DE_DLY_WITH_Y.	
	YCDELAY_STEP[2:0]	2:0	Y/C delay pipe step.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	44TO42_DITH_EN	0	444 to 422 filter dith enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FILL_BLACK_NUM[5:0]	5:0	Fill black number.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILL_BLACK_ACT	7	FILL_BLACK_ACT.	
	FILL_BLACK_CLR	6	Clear fill_black register manually.	
	-	5:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_OSD_HSK	4	Force ip2 to OSD in handshaking mode.	
	-	3	Reserved.	
	IP2_VS_SEL	2	1: Use mvop_vs to generate vs to opvs. 0: Use ip1_vs to generate vs to opvs.	
	FORCE_PRE2LAST	1	1: Use vsd last valid as pre align. 0: Use original pre align.	
	MVOP_DIN_EN	0	1: Data is form mvop. 0: Form yc delay.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0xD0**	**Access : R/W**
	H_TOTAL[7:0]	7:0	Patgen h total.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	H_TOTAL[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0xE0**	**Access : R/W**
	V_TOTAL[7:0]	7:0	Patgen v total.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	V_TOTAL[11:8]	3:0	See description of '102F24h'.	
13h	**REG102F26**	**7:0**	**Default : 0x40**	**Access : R/W**

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	H_BLOCK[7:0]	7:0	Patgen h block.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_BLOCK[9:8]	1:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x20**	**Access : R/W**
	V_BLOCK[7:0]	7:0	Patgen v block.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	V_BLOCK[9:8]	1:0	See description of '102F28h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xF2**	**Access : R/W**
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x1F**	**Access : R/W**
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x5E**	**Access : R/W**
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xF4**	**Access : R/W**
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x0C**	**Access : R/W**
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x5A**	**Access : R/W**
	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x37**	**Access : R/W**
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0xF5**	**Access : R/W**
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
1Eh	**REG102F3C**	**7:0**	**Default : 0xFA**	**Access : R/W**

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y0. Format: S7 of 2's complement (-15 <= Y0 <= 15).	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 127).	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x17**	**Access : R/W**
	HSD_CT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_CT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x0B**	**Access : R/W**
	HSD_CT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_CT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x29**	**Access : R/W**
	HSD_CT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C3. Format: Fix 8 (0 <= C3 <= 255).	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x01**	**Access : R/W**
	HSD_CT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C4. Format: S7 of 2's complement (-63 <= C4 <= + 63).	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x04**	**Access : R/W**
	HSD_CT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x3C**	**Access : R/W**
	HSD_CT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C2. Format: Fix 8 (0 <= C2 <= 127).	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:0	Reserved.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIN_CTRL_EN	7	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	6	IP2 VSD input line count number setting enable.	
	-	5	Reserved.	
	VSD_IN_NUM_USR[12:8]	4:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VOUT_CTRL_EN	7	IP2 VSD output line count control enable.	
	-	6:5	Reserved.	
	VSD_OUT_NUMBER[12:8]	4:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_USR_VACT_VIDEO[7:0]	7:0	VSD user mode v_active region.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_USR_VACT_VIDEO_EN	7	VSD user mode v_active region enable.	
	-	6:5	Reserved.	
	VSD_USR_VACT_VIDEO[12:8]	4:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	VSD_VACT_VIDEO_READ[7:0]	7:0	VSD user mode v_active region.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	VSD_VACT_VIDEO_READ[12:8]	4:0	See description of '102F72h'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_HSD_OUT_CNT[12:8]	4:0	See description of '102F7Ch'.	
3Fh	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_VSD_OUT_CNT[12:8]	4:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PREFLT_ALPHA_EN	7	IP2 Pre-Filter alpha blending enable.	
	-	6:5	Reserved.	
	PREFLT_ALPHA[4:0]	4:0	IP2 Pre-Filter alpha blending for original and filter.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_Y_TAP0[3:0]	3:0	IP2 Pre-Filter coefficient 0 [s.3] (T8).	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_FILTER_EN	7	IP2 Pre-Filter enable.	
	FIR_DITH_EN	6	IP2 Pre-Filter dith enable.	
	-	5:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7	Reserved.	
	PRE_Y_TAP1[6:0]	6:0	IP2 Pre-Filter coefficient 1 [s.6] (T8).	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x6A**	**Access : R/W**
	-	7	Reserved.	
	PRE_Y_TAP2[6:0]	6:0	IP2 Pre-Filter coefficient 2 [s.6] (T8).	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x2F**	**Access : R/W**
	PRE_Y_TAP3[7:0]	7:0	IP2 Pre-Filter coefficient 3 [s.7] (T8).	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP4[7:0]	7:0	IP2 Pre-Filter coefficient 4 [s.8] (T8).	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PRE_Y_TAP4[8]	0	See description of '102F98h'.	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)

Index (Absolute)	Mnemonic	Bit	Description	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x6A**	**Access : R/W**
	PRE_Y_TAP5[7:0]	7:0	IP2 Pre-Filter coefficient 5 [s.9] (T8).	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP5[9:8]	1:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x8C**	**Access : R/W**
	PRE_Y_TAP6[7:0]	7:0	IP2 Pre-Filter coefficient 6 [0.10] (T8).	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP6[9:8]	1:0	See description of '102F9Ch'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FLT_MODE	0	In advance mode 0:use 4 phase blending 1: use 8 phase blending.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT3_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x0D**	**Access : R/W**
	HSD_YT3_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x5C**	**Access : R/W**
	HSD_YT3_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x23**	**Access : R/W**
	HSD_YT3_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT3_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x03**	**Access : R/W**
	HSD_YT3_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT4_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0.	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Format: S7 of 2's complement (-31 <= Y0 <= 31).	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT4_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_YT4_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x3B**	**Access : R/W**
	HSD_YT4_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT4_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSD_YT4_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GOP_REQ_CNT[4:0]	4:0	In mvop handshake mode, gen GOP needs timing.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2GOP_SRC_SEL	7	For GOPD src of ip2 0: IP2IN 1:IP2OUT.	
	-	6:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADJ_HI_PRI[7:0]	7:0	Adjust memory priority.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PSEUDO_STOP	0	Enable pseudo blanking.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x08**	**Access : R/W**
	LB_SPLIT_BLANK[7:0]	7:0	LB pseudo blank cycle.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x18**	**Access : R/W**
	PRE_ADJ_SPLIT_BLANK[7:0]	7:0	Adjust pseudo blank cycle.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EXT_LR_EN	4	Enable external lr signal.	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:1	Reserved.	
	INIT_3D_STAT	0	Initialize 3d stat.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	WAIT_LEFT_FRM_INV	5	Reg_wait_right_frm.	
	WAIT_LEFT_FRM	4	WAIT_LEFT_FRM.	
	-	3:1	Reserved.	
	EXT_LR_INV	0	Inverse external lr signal.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	INI_LR_IDX	4	0: L is the first frame 1: R is the first frame.	
	-	3	Reserved.	
	ADJ_FORCE_EN	2	Adj bypass enable.	
	LR_CHG_MODE[1:0]	1:0	0: Line. 1: Block. 2: Frame.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAX_LOOP[2:0]	6:4	3d mode setting.	
	-	3:1	Reserved.	
	SPLIT_HALF	0	Split 1 frame into 2 frames.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VACT_SPC_EN[1:0]	5:4	3d mode setting.	
	-	3	Reserved.	
	MASK_EN[2:0]	2:0	3d mode setting.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GEN_VS_ACT[3:0]	7:4	Enable gen pseudo vsync in 3d.	
	GEN_VS_EN[3:0]	3:0	Enable gen pseudo vsync in 3d.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_VIDEO[7:0]	7:0	V_active region.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VACT_VIDEO[12:8]	4:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_SPC_0[7:0]	7:0	V blanking between field1&field2 or field3&field4.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_SPC_0[12:8]	4:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_SPC_1[7:0]	7:0	V blanking between field2&field3.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_SPC_1[12:8]	4:0	See description of '102FCEh'.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0xC0**	**Access : R/W**
	LB_AUTO	7	LB_AUTO.	
	VSD_FAC_AUTO_RST_EN	6	VSD 3d auto factor reset mode enable.	
	AUTO_VACT_VIDEO_RST	5	AUTO vact_video mode reset.	
	-	4:0	Reserved.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_OUTACK	1	Enable dat_adj to src force ready.	
	ADJ_AUTO	0	ADJ_AUTO.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : RO**
	FIFO_DIFF[7:0]	7:0	Number of FIFO.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FIFO_DIFF[8]	0	See description of '102FD4h'.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LR_ALT_LINE	2	RSP line initialization.	
	LR_FST_PIX	1	RSP LR initialization.	
	PIX_SEP_EN	0	PIX_SEP_EN.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HALF_PIX[7:0]	7:0	IP2 3D separation half number for user mode.	
6Ch	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HALF_PIX_USR_EN	7	IP2 3D separation user mode.	
	-	6:3	Reserved.	
	HALF_PIX[10:8]	2:0	See description of '102FD8h'.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSP_PH0_COEF0[7:0]	7:0	RSP phase 0 coefficient 0.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x80**	**Access : R/W**
	RSP_PH0_COEF1[7:0]	7:0	RSP phase 0 coefficient 1.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSP_PH1_COEF0[7:0]	7:0	RSP phase 1 coefficient 0.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x40**	**Access : R/W**
	RSP_PH1_COEF1[7:0]	7:0	RSP phase 1 coefficient 1.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RSP_LINE7_PH	7	RSP line phase 7.	
	RSP_LINE6_PH	6	RSP line phase 6.	
	RSP_LINE5_PH	5	RSP line phase 5.	
	RSP_LINE4_PH	4	RSP line phase 4.	
	RSP_LINE3_PH	3	RSP line phase 3.	
	RSP_LINE2_PH	2	RSP line phase 2.	
	RSP_LINE1_PH	1	RSP line phase 1.	
	RSP_LINE0_PH	0	RSP line phase 0.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RSP_FIELD_USR_EN	6	Re-sample local toggle field flag.	
	RSP_FIELD_INV	5	Re-sample field polarity invert.	
	RSP_FIELD_EN	4	Re-sample field mode.	
	-	3:1	Reserved.	
	RESAMP_EN	0	RSP enable.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DUMMY_CLR[7:0]	7:0	DUMMY_CLR.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_CLR[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[7:0]	7:0	DUMMY_SET.	

SC1 IP2_M Register (Bank = 102F, Sub-Bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[15:8]	7:0	See description of '102FFEh'.	

SC1 PNR Register (Bank = 102F, Sub-Bank = 05)

SC1 PNR Register (Bank = 102F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PNR_ENY_F1	3	Sub Window Post Noise Reduction for Y.	
	PNR_ENC_F1	2	Sub Window Post Noise Reduction for C.	
	RATIOYC_F1[1:0]	1:0	Sub Window Motion Ratio.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	PNR_BYPASS_F1	2	Sub Window PNR function bypass enable.	
	NR_EN_F1	1	Sub Window Post NR enable.	
	PCCS_EN_F1	0	Sub Window Post CCS enable.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FILM_DETECT_NXT_EN_F1	3	PNR pack next_y 5-bit to opm_itf for sub window.	
	DITHER_FRAME_RST_CNT[1:0]	2:1	Dither frame reset count.	
	DITHER_FRAME_RST_EN	0	Dither frame reset enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_F2[1:0]	1:0	Main Window Motion Ratio.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_MODE_SEL_F2	7	Main Window C average mode selection when dotline cycle.	
	FIELD_AVG_Y_MODE_SEL_F2	6	Main Window Y average mode selection when dotline cycle.	
	-	5:1	Reserved.	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for noc_sel.	

SC1 PNR Register (Bank = 102F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F2	7	Main Window DHD 3f mode enable.	
	PCCS_3F_EN_F2	6	Main Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F2	4	Main Window PCCS dither enable.	
	DHD_DITHER_EN_F2	3	Main Window DHD dither enable.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PAL_EN_F2	6	Main Window PAL enable.	
	-	5:0	Reserved.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for c.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window c motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window y motion divide mode.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FILM_DETECT_NXT_EN_F2	3	PNR pack next_y 5-bit to opm_itf for main window.	
	-	2:0	Reserved.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F2	5	Main Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F2	4	Main Window DHD Interleaved History MR enable.	

SC1 PNR Register (Bank = 102F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DHD_CMR_IIR_EN_F2	3	Main Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F2	2	Main Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F2	1	Main Window DHD YMR02 enable.	
	DHD_EN_F2	0	Main Window DHD enable.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F1	5	Sub Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F1	4	Sub Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F1	3	Sub Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F1	2	Sub Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F1	1	Sub Window DHD YMR02 enable.	
	DHD_EN_F1	0	Sub Window DHD enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR02_TH[5:0]	5:0	DHD YMR02 threshold.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR02_GAIN[2:0]	2:0	DHD YMR02 gain.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR04_TH[5:0]	5:0	DHD YMR04 threshold.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR04_GAIN[2:0]	2:0	DHD YMR04 gain.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_CVAL_GAIN[7:0]	7:0	DHD C value gain.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_DIFFPIX_GAIN[3:0]	3:0	DHD pixel diff gain.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_CMR02_TH[5:0]	5:0	DHD C motion02 threshold.	
24h	**REG102F49**	**7:0**	**Default : 0x01**	**Access : R/W**

SC1 PNR Register (Bank = 102F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:3	Reserved.	
	DHD_CMR02_GAIN[2:0]	2:0	DHD C motion02 gain.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_CMR04_TH[5:0]	5:0	DHD C motion04 threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR04_GAIN[2:0]	2:0	DHD C motion04 gain.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x30**	**Access : R/W**
	DHD_CEDGE_GAIN[7:0]	7:0	DHD C edge gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_YEDGE_GAIN[7:0]	7:0	DHD Y edge gain.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_YMR_IIR_ALPHA[2:0]	6:4	DHD YMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_YMR_IIR_STEP[1:0]	1:0	DHD YMR IIR step.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_CMR_IIR_ALPHA[2:0]	6:4	DHD CMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_CMR_IIR_STEP[1:0]	1:0	DHD CMR IIR step.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_CEDGE_TH[7:0]	7:0	DHD C edge threshold.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_YEDGE_TH[7:0]	7:0	DHD Y edge threshold.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_CVAL_TH[7:0]	7:0	DHD C value threshold.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_USER_W[3:0]	3:0	DHD user weight of final result.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	

SC1 PNR Register (Bank = 102F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CCS_YMR04_GAIN[4:0]	4:0	CCS Y motion gain of diff of cur and ext.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_YMR04_TH[4:0]	4:0	CCS Y motion threshold of diff of cur and ext.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_YMR02_24_GAIN[4:0]	4:0	CCS Y motion 02 24 gain.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_YMR02_24_TH[4:0]	4:0	CCS Y motion 02 24 threshold.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	CCS_CMR04_GAIN[3:0]	3:0	CCS C motion 04 gain.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CMR04_TH[4:0]	4:0	CCS C motion 04 threshold.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	CCS_CMR02_24_GAIN[3:0]	3:0	CCS C motion 02 24 gain.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CMR02_24_TH[4:0]	4:0	CCS C motion 02 24 threshold.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CRCE_GAIN[4:0]	4:0	CCS C real edge gain.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CRCE_TH[4:0]	4:0	CCS C real edge threshold.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:6	Reserved.	
	CCS_YEDGE_GAIN[5:0]	5:0	CCS Y edge gain.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCS_YEDGE_TH[7:0]	7:0	CCS Y edge threshold.	

SC1 PNR Register (Bank = 102F, Sub-Bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CSAT_GAIN[4:0]	4:0	CCS C saturation gain.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CSAT_TH[4:0]	4:0	CCS C saturation gain.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	CCS_USER_W[3:0]	3:0	CCS user weight of final result.	
78h ~ 78h (102FF0h ~ 102FF1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 DNR Register (Bank = 102F, Sub-Bank = 06)

SC1 DNR Register (Bank = 102F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION EN.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_NR_TABLE_SEL_C	1	F2 DNR Table C Mapping Select. #0: non-linear. #1: linear.	
	F2_NR_TABLE_SEL_Y	0	F2 DNR Table Y Mapping Select. #0: non-linear. #1: linear.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SNR_MD_MODE_EN	1	F2 SNR Motion Mode EN.	
	SNR_EN	0	F2 SNR FUNCTION EN.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_ROUND_MODE_C[1:0]	3:2	F2 DNR C blend rounding select. #00: add 0. #01: add dither. #10: add dither. #11: add dither.	
	F2_ROUND_MODE_Y[1:0]	1:0	F2 DNR Y blend rounding select. #00: add 0. #01: add dither. #10: add dither. #11: add dither.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_MAX_MOT_ENABLE_C	3	F2_MAX_MOT_ENABLE_C.	
	F2_MAX_MOT_ENABLE_Y	2	F2_MAX_MOT_ENABLE_Y.	
	F2_DNR_FILTER_EN_C	1	F2_DNR_FILTER_EN_C.	
	F2_DNR_FILTER_EN_Y	0	F2_DNR_FILTER_EN_Y.	

SC1 DNR Register (Bank = 102F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_DIV0_C[2:0]	7:5	F2_DNR_FILTER_DIV0_C.	
	F2_DNR_FILTER_DIV0_Y[2:0]	4:2	F2_DNR_FILTER_DIV0_Y.	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_MODE_C[1:0]	7:6	F2_DNR_FILTER_MODE_C.	
	F2_DNR_FILTER_MODE_Y[1:0]	5:4	F2_DNR_FILTER_MODE_Y.	
	F2_DNR_FILTER_DIV1_C[1:0]	3:2	F2_DNR_FILTER_DIV1_C.	
	F2_DNR_FILTER_DIV1_Y[1:0]	1:0	F2_DNR_FILTER_DIV1_Y.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SNR_SHARP_LEVEL[3:0]	3:0	SNR sharpness level.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '102F88h'.	
45h	**REG102F8A**	**7:0**	**Default : 0x56**	**Access : R/W**

SC1 DNR Register (Bank = 102F, Sub-Bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEC_1[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '102F8Eh'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	F2_WIN_EN	0	F2 DNR/SNR active window enable.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_XSTART[7:0]	7:0	F2 DNR/SNR active window start X.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XSTART[10:8]	2:0	See description of '102FE8h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_YSTART[7:0]	7:0	F2 DNR/SNR active window start Y.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_YSTART[10:8]	2:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x68**	**Access : R/W**
	F2_WIN_XEND[7:0]	7:0	F2 DNR/SNR active window end X.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XEND[10:8]	2:0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0xF0**	**Access : R/W**
	F2_WIN_YEND[7:0]	7:0	F2 DNR/SNR active window end Y.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

SC1 DNR Register (Bank = 102F, Sub-Bank = 06)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	F2_WIN_YEND[10:8]	2:0	See description of '102FEEh'.

SC1 FILM Register (Bank = 102F, Sub-Bank = 0A)

SC1 FILM Register (Bank = 102F, Sub-Bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7	Reserved.	
	DET_FIELD_SEL_LC	6	DET_FIELD_SEL_LC.	
	-	5	Reserved.	
	DIFF_TH[12:8]	4:0	Difference threshold.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_CUR_ERROR_TH_F2[7:0]	7:0	32 current error threshold.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_PRE_ERROR_TH_F2[15:8]	7:0	32 previous error threshold.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_CUR_ERROR_TH_F2[7:0]	7:0	22 current error threshold.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_PRE_ERROR_TH_F2[15:8]	7:0	22 previous error threshold.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	32_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	32 total error max th.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x7F**	**Access : R/W**
	32_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	32 total error sum th.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x08**	**Access : R/W**
	22_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	22 total error max th.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x7F**	**Access : R/W**
	22_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	22 total error sum th.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	FIX_DIFF_TH[12:8]	4:0	Cur error sum th.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_1_TH_F2[7:0]	7:0	F2 counter 1 threshold.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_1_TH_F2[15:8]	7:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_3_TH_F2[7:0]	7:0	F2 counter 3 threshold.	

SC1 FILM Register (Bank = 102F, Sub-Bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_3_TH_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_FIX_TH_F2[7:0]	7:0	F2 counter fix threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	POINT_UNMATCH_FIX_TH_F2[15:8]	7:0	See description of '102F1Ch'.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x30**	**Access : R/W**
	FILM32_EN_F2	7	F2 32 film mode enable.	
	FILM22_EN_F2	6	F2 22 film mode enable.	
	-	5:4	Reserved.	
	PRE32_F2	3	F2 pre32.	
	-	2:0	Reserved.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xEE**	**Access : R/W**
	MOT_TH_PATCH_F2[7:4]	7:4	F2 patch motion threshold.	
	FM_MOT_PIXTH_F2[3:0]	3:0	F2 motion ratio threshold.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x14**	**Access : R/W**
	FM_MOT_CNTTH_F2[15:8]	7:0	F2 unmatch threshold.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FILM32_N1_EN_F2	7	F2 N1 film32 enable.	
	FILM22_N1_EN_F2	6	F2 N1 film22 enable.	
	-	5:0	Reserved.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_STATUS_F2[7:0]	7:0	F2 read status.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_STATUS_F2[15:8]	7:0	See description of '102F30h'.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[7:0]	7:0	F2 patch read status.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[15:8]	7:0	See description of '102F34h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x50**	**Access : R/W**
	MULT_COEF_F2[7:4]	7:4	F2 multiplicand ratio.	

SC1 FILM Register (Bank = 102F, Sub-Bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:1	Reserved.	
	RELATIVE_FM_EN_F2	0	F2 relative film mode frame diff enable.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x05**	**Access : R/W**
	LOWER_BOUND_FM_32_F2[15:8]	7:0	F2 frame diff lower bound.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	UPPER_BOUND_FM_32_F2[7:0]	7:0	F2 frame diff upper bound.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x03**	**Access : R/W**
	UPPER_BOUND_FM_32_F2[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x0F**	**Access : R/W**
	CHECK_SEQ_F2[7:0]	7:0	F2 lock threshold to enter 22.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x44**	**Access : R/W**
	SPEEDUP_STEP_F2[7:4]	7:4	F2 speedup step.	
	SPEEDUP_SHIFT_F2[3:0]	3:0	F2 speedup shift value.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x80**	**Access : R/W**
	SPEEDUP_EN_F2	7	F2 speedup enable.	
	-	6:0	Reserved.	
55h ~ 57h (102FAAh ~ 102FAFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Dh ~ 0Fh (102F1Ah ~ 102F1Fh)	-	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x66**	**Access : R/W**
	DBK_TEST_EN	7	De-blocking test mode.	
	DBK_EN_V_F1	6	Vertical de-blocking enable F1.	
	DBK_EN_H_F1	5	Horizontal de-blocking enable F1.	
	DBK_EN_F1	4	De-blocking enable F1.	
	-	3	Reserved.	
	DBK_EN_V_F2	2	Vertical de-blocking enable F2.	
	DBK_EN_H_F2	1	Horizontal de-blocking enable F2.	
	DBK_EN_F2	0	De-blocking enable F2.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x30**	**Access : R/W**
	DBK_STD_LOW_THRD[7:0]	7:0	De-blocking active threshold.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x0F**	**Access : R/W**
	DBK_ALPHA_STEP[2:0]	7:5	De-blocking alpha step.	
	-	4	Reserved.	
	DBK_STRENGTH_GAIN_F2[3:0]	3:0	De-blocking strength F2 (.xxxx).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:6	Reserved.	
	DBK_MOTION_RATIO_EN_F1	5	De-blocking motion ratio enable F1.	
	DBK_MOTION_RATIO_EN_F2	4	De-blocking motion ratio enable F2.	
	DBK_STRENGTH_GAIN_F1[3:0]	3:0	De-blocking strength F1 (.xxxx).	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0xEF**	**Access : R/W**
	DBK_TABLE_01[7:0]	7:0	De-blocking LUT_01.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0xCD**	**Access : R/W**
	DBK_TABLE_23[7:0]	7:0	De-blocking LUT_23.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xAB**	**Access : R/W**
	DBK_TABLE_45[7:0]	7:0	De-blocking LUT_45.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x89**	**Access : R/W**
	DBK_TABLE_67[7:0]	7:0	De-blocking LUT_67.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x67**	**Access : R/W**
	DBK_TABLE_89[7:0]	7:0	De-blocking LUT_89.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x45**	**Access : R/W**
	DBK_TABLE_AB[7:0]	7:0	De-blocking LUT_AB.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x23**	**Access : R/W**
	DBK_TABLE_CD[7:0]	7:0	De-blocking LUT_CD.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x01**	**Access : R/W**
	DBK_TABLE_EF[7:0]	7:0	De-blocking LUT_EF.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_INIT_1_F2[7:0]	7:0	De-blocking H counter initial value[7:0] F2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_INIT_2_F2[7:0]	7:0	De-blocking H counter initial value[15:8] F2.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_H_INIT_3_F2[3:0]	3:0	De-blocking H counter initial value[19:16] F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_INIT_4_F2[4:0]	4:0	De-blocking H counter initial value[24:20] F2.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_INIT_1_F2[7:0]	7:0	De-blocking V counter initial value[7:0] F2.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_INIT_2_F2[7:0]	7:0	De-blocking V counter initial value[15:8] F2.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_V_INIT_3_F2[3:0]	3:0	De-blocking V counter initial value[19:16] F2.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_INIT_4_F2[4:0]	4:0	De-blocking V counter initial value[24:20] F2.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_RATIO_1_F2[7:0]	7:0	De-blocking H counter ratio[7:0] F2.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_RATIO_2_F2[7:0]	7:0	De-blocking H counter ratio[15:8] F2.	
1Dh	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	DBK_H_RATIO_3_F2[3:0]	3:0	De-blocking H counter ratio[19:16] F2.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_RATIO_4_F2[4:0]	4:0	De-blocking H counter ratio[24:20] F2.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_RATIO_1_F2[7:0]	7:0	De-blocking V counter ratio[7:0] F2.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_RATIO_2_F2[7:0]	7:0	De-blocking V counter ratio[15:8] F2.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_V_RATIO_3_F2[3:0]	3:0	De-blocking V counter ratio[19:16] F2.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_RATIO_4_F2[4:0]	4:0	De-blocking V counter ratio[24:20] F2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_INIT_1_F1[7:0]	7:0	De-blocking H counter initial value[7:0] F1.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_INIT_2_F1[7:0]	7:0	De-blocking H counter initial value[15:8] F1.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_H_INIT_3_F1[3:0]	3:0	De-blocking H counter initial value[19:16] F1.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_INIT_4_F1[4:0]	4:0	De-blocking H counter initial value[24:20] F1.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_INIT_1_F1[7:0]	7:0	De-blocking V counter initial value[7:0] F1.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_INIT_2_F1[7:0]	7:0	De-blocking V counter initial value[15:8] F1.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_V_INIT_3_F1[3:0]	3:0	De-blocking V counter initial value[19:16] F1.	
23h	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	DBK_V_INIT_4_F1[4:0]	4:0	De-blocking V counter initial value[24:20] F1.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_RATIO_1_F1[7:0]	7:0	De-blocking H counter ratio[7:0] F1.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_RATIO_2_F1[7:0]	7:0	De-blocking H counter ratio[15:8] F1.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_H_RATIO_3_F1[3:0]	3:0	De-blocking H counter ratio[19:16] F1.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_RATIO_4_F1[4:0]	4:0	De-blocking H counter ratio[24:20] F1.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_RATIO_1_F1[7:0]	7:0	De-blocking V counter ratio[7:0] F1.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_RATIO_2_F1[7:0]	7:0	De-blocking V counter ratio[15:8] F1.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_V_RATIO_3_F1[3:0]	3:0	De-blocking V counter ratio[19:16] F1.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_RATIO_4_F1[4:0]	4:0	De-blocking V counter ratio[24:20] F1.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_BLOCK_WIDTH_F2[4:0]	4:0	H block width F2.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BLOCK_WIDTH_F2[4:0]	4:0	V block width F2.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_BOUNDARY_LEFT_F2[4:0]	4:0	H block left boundary F2.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DBK_H_BOUNDARY_RIGHT_F2[4:0]	4:0	H block right boundary F2.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BOUNDARY_UP_F2[4:0]	4:0	V block up boundary F2.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BOUNDARY_DOWN_F2[4:0]	4:0	V block down boundary F2.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_BLOCK_WIDTH_F1[4:0]	4:0	H block width F1.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BLOCK_WIDTH_F1[4:0]	4:0	V block width F1.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_BOUNDARY_LEFT_F1[4:0]	4:0	H block left boundary F1.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_BOUNDARY_RIGHT_F1[4:0]	4:0	H block right boundary F1.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BOUNDARY_UP_F1[4:0]	4:0	V block up boundary F1.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BOUNDARY_DOWN_F1[4:0]	4:0	V block down boundary F1.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SNR_MOTION_RATIO_EN_F1	5	SNR motion ratio enable F1.	
	SNR_EN_F1	4	SNR enable F1.	
	-	3:2	Reserved.	
	SNR_MOTION_RATIO_EN_F2	1	SNR motion ratio enable F2.	
	SNR_EN_F2	0	SNR enable F2.	
30h	**REG102F61**	**7:0**	**Default : 0x0A**	**Access : R/W**

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SNR_STD_LOW_THRD[7:0]	7:0	SNR active threshold.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x48**	**Access : R/W**
	SNR_ALPHA_STEP[2:0]	7:5	SNR alpha step.	
	-	4	Reserved.	
	SNR_STRENGTH_GAIN_F2[3:0]	3:0	SNR strength F2.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	SNR_STRENGTH_GAIN_F1[3:0]	3:0	SNR strength F1.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0xCF**	**Access : R/W**
	SNR_TABLE_01[7:0]	7:0	SNR LUT_01.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x69**	**Access : R/W**
	SNR_TABLE_23[7:0]	7:0	SNR LUT_23.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x24**	**Access : R/W**
	SNR_TABLE_45[7:0]	7:0	SNR LUT_45.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x01**	**Access : R/W**
	SNR_TABLE_67[7:0]	7:0	SNR LUT_67.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_89[7:0]	7:0	SNR LUT_89.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_AB[7:0]	7:0	SNR LUT_AB.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_CD[7:0]	7:0	SNR LUT_CD.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_EF[7:0]	7:0	SNR LUT_EF.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x66**	**Access : R/W**
	DBK_CORING_STEP_F2[1:0]	7:6	De-blocking blockiness coring step F2.	
	DBK_DEC_STEP_F2[1:0]	5:4	De-blocking decrease step in new mode F2.	
	-	3	Reserved.	
	DBK_BLOCKINESS_IIR_VER_EN_F2	2	De-blocking blockiness IIR vertical enable F2.	
	DBK_CORING_EN_F2	1	De-blocking blockiness coring enable F2.	
	DBK_DEC_MODE_EN_F2	0	De-blocking new mode enable F2.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x66**	**Access : R/W**
	DBK_CORING_STEP_F1[1:0]	7:6	De-blocking blockiness coring step F1.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DBK_DEC_STEP_F1[1:0]	5:4	De-blocking decrease step in new mode F1.	
	-	3	Reserved.	
	DBK_BLOCKINESS_IIR_VER_EN_F1	2	De-blocking blockiness IIR vertical enable F1.	
	DBK_CORING_EN_F1	1	De-blocking blockiness coring enable F1.	
	DBK_DEC_MODE_EN_F1	0	De-blocking new mode enable F1.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x09**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_BKN_INTERVAL_LEFT_F2[4:0]	4:0	De-blocking blockiness left interval F2. // location from 2 to 30.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_BKN_INTERVAL_RIGHT_F2[4:0]	4:0	De-blocking blockiness right interval F2. // location from 2 to 30.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x47**	**Access : R/W**
	-	7	Reserved.	
	DBK_BKN_IIR_ALPHA_VER_F2[2:0]	6:4	De-blocking blockiness interval iir alpha vertical strength F2.	
	-	3	Reserved.	
	DBK_BKN_INTERVAL_IIR_ALPHA_F2[2:0]	2:0	De-blocking blockiness interval iir alpha strength F2.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:3	Reserved.	
	DBK_BKN_INTERVAL_IIR_ALPHA_INI_F2[2:0]	2:0	De-blocking blockiness interval iir alpha initial boundary strength F2.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x09**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_BKN_INTERVAL_LEFT_F1[4:0]	4:0	De-blocking blockiness left interval F1. // location from 2 to 30.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_BKN_INTERVAL_RIGHT_F1[4:0]	4:0	De-blocking blockiness right interval F1. // location from 2 to 30.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x47**	**Access : R/W**
	-	7	Reserved.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DBK_BKN_IIR_ALPHA_VER_F1[2:0]	6:4	De-blocking blockiness interval iir alpha vertical strength F1.	
	-	3	Reserved.	
	DBK_BKN_INTERVAL_IIR_ALPHA_F1[2:0]	2:0	De-blocking blockiness interval iir alpha strength F1.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:3	Reserved.	
	DBK_BKN_INTERVAL_IIR_ALPHA_INI_F1[2:0]	2:0	De-blocking blockiness interval iir alpha initial strength boundary F1.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x0A**	**Access : R/W**
	DBK_CORING_THRD_F2[7:0]	7:0	De-blocking blockiness coring low threshold F2.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x0A**	**Access : R/W**
	DBK_CORING_THRD_F1[7:0]	7:0	De-blocking blockiness coring low threshold F1.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x67**	**Access : R/W**
	-	7	Reserved.	
	DBK_BLOCKINESS_INTERVAL_IIR_EN_F2	6	De-blocking blockiness interval iir enable F2.	
	DBK_BLOCKINESS_PIXEL_EN_F2	5	De-blocking blockiness pixel active enable F2.	
	-	4	Reserved.	
	DBK_COARSE_STEP_F2[1:0]	3:2	De-blocking coarse detect step F2.	
	DBK_BK_PULSE_FILTER_EN_F2	1	De-blocking blockiness pulse filter enable F2.	
	DBK_BLOCKINESS_EN_F2	0	De-blocking blockiness detect enable F2.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x03**	**Access : R/W**
	DBK_COARSE_LOW_THRD_F2[7:0]	7:0	De-blocking coarse active threshold F2.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x42**	**Access : R/W**
	-	7:3	Reserved.	
	DBK_SIDE_STEP_F2[1:0]	2:1	De-blocking side detect step F2.	
	-	0	Reserved.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_SIDE_LOW_THRD_F2[7:0]	7:0	De-blocking side active threshold F2.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:6	Reserved.	
	DBK_BLOCKINESS_STEP_F2[1:0]	5:4	De-blocking blockiness strength step F2.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3	Reserved.	
	DBK_BK_PULSE_FILTER_F2[2:0]	2:0	De-blocking blockiness pulse filter F2. // 0 : [-1 -1 4 -1 -1]/2. // 1 : [-2 -2 4 -2 -2]/2. // 2 : [-2 0 4 0 -2]/2. // 3 : [-1 0 4 0 -1]/2. // 4 : [-2 0 0 4 0 0 -2]/2. // 5 : [-2 0 0 4 0 0 -2].	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_BK_REF_STEP_RIGHT_F2[1:0]	3:2	De-blocking blockiness right reference step F2. // 0: no reference. // 1: one more right pixel reference. // 2: two more right pixel reference.	
	DBK_BK_REF_STEP_LEFT_F2[1:0]	1:0	De-blocking blockiness left reference step F2. // 0: no reference. // 1: one more left pixel reference. // 2: two more left pixel reference.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x67**	**Access : R/W**
	-	7	Reserved.	
	DBK_BLOCKINESS_INTERVAL_IIR_EN_F1	6	De-blocking blockiness interval iir enable F1.	
	DBK_BLOCKINESS_PIXEL_EN_F1	5	De-blocking blockiness pixel active enable F1.	
	-	4	Reserved.	
	DBK_COARSE_STEP_F1[1:0]	3:2	De-blocking coarse detect step F1.	
	DBK_BK_PULSE_FILTER_EN_F1	1	De-blocking blockiness pulse filter enable F1.	
	DBK_BLOCKINESS_EN_F1	0	De-blocking blockiness detect enable F1.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x03**	**Access : R/W**
	DBK_COARSE_LOW_THRD_F1[7:0]	7:0	De-blocking coarse active threshold F1.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x42**	**Access : R/W**
	-	7:3	Reserved.	
	DBK_SIDE_STEP_F1[1:0]	2:1	De-blocking side detect step F1.	
	-	0	Reserved.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_SIDE_LOW_THRD_F1[7:0]	7:0	De-blocking side active threshold F1.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_ALPHA_MAX[4:0]	4:0	De-blocking alpha maximum value.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:6	Reserved.	
	DBK_BLOCKINESS_STEP_F1[1:0]	5:4	De-blocking blockiness strength step F1.	
	-	3	Reserved.	
	DBK_BK_PULSE_FILTER_F1[2:0]	2:0	De-blocking blockiness pulse filter F1. // 0 : [-1 -1 4 -1 -1]/2. // 1 : [-2 -2 4 -2 -2]/2. // 2 : [-2 0 4 0 -2]/2. // 3 : [-1 0 4 0 -1]/2. // 4 : [-2 0 0 4 0 0 -2]/2. // 5 : [-2 0 0 4 0 0 -2].	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_BK_REF_STEP_RIGHT_F1[1:0]	3:2	De-blocking blockiness right reference step F1. // 0: no reference. // 1: one more right pixel reference. // 2: two more right pixel reference.	
	DBK_BK_REF_STEP_LEFT_F1[1:0]	1:0	De-blocking blockiness left reference step F1. // 0: no reference. // 1: one more right pixel reference. // 2: two more right pixel reference.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_14	7	Reserved.	
	-	6	Reserved.	
	SNR_NM_MOTION_RATIO_EN_F1	5	Noise masking motion ratio enable F1.	
	SNR_NM_FILTER_EN_F1	4	Noise masking enable F1.	
	-	3:2	Reserved.	
	SNR_NM_MOTION_RATIO_EN_F2	1	Noise masking motion ratio enable F2.	
	SNR_NM_FILTER_EN_F2	0	Noise masking enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RESERVED_SNR_5[1:0]	3:2	Reserved.	
	-	1:0	Reserved.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SNR_MR_LPF_EN_F1	4	De-blocking and SNR motion ratio low pass filter enable F1 (lpf is 3x3 mask).	
	-	3:1	Reserved.	
	SNR_MR_LPF_EN_F2	0	De-blocking and SNR motion ratio low pass filter enable F2 (lpf is 3x3 mask).	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_9[1:0]	7:6	Reserved.	
	SNR_NM_GAIN_F2[5:0]	5:0	Noise masking gain F2.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_10[1:0]	7:6	Reserved.	
	SNR_NM_GAIN_F1[5:0]	5:0	Noise masking gain F1.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SNR_NM_MIN_THRD[3:0]	7:4	Noise masking min threshold bound.	
	SNR_NM_MAX_THRD[3:0]	3:0	Noise masking max threshold bound.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_MOTION_TABLE_01[7:0]	7:0	SNR motion ratio LUT_01.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_MOTION_TABLE_23[7:0]	7:0	SNR motion ratio LUT_23.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_MOTION_TABLE_45[7:0]	7:0	SNR motion ratio LUT_45.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_MOTION_TABLE_67[7:0]	7:0	SNR motion ratio LUT_67.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_MOTION_TABLE_89[7:0]	7:0	SNR motion ratio LUT_89.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_MOTION_TABLE_AB[7:0]	7:0	SNR motion ratio LUT_AB.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_MOTION_TABLE_CD[7:0]	7:0	SNR motion ratio LUT_CD.	
5Fh	**REG102FBF**	**7:0**	**Default : 0xFE**	**Access : R/W**

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SNR_MOTION_TABLE_EF[7:0]	7:0	SNR motion ratio LUT_EF.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x35**	**Access : R/W**
	DBK_BKN_PRE_CORING_F2[3:0]	7:4	De-blocking blockiness pre coring F2.	
	DBK_BKN_POST_CORING_F2[3:0]	3:0	De-blocking blockiness post coring F2.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x35**	**Access : R/W**
	DBK_BKN_PRE_CORING_F1[3:0]	7:4	De-blocking blockiness pre coring F1.	
	DBK_BKN_POST_CORING_F1[3:0]	3:0	De-blocking blockiness post coring F1.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_NM_MOTION_TABLE_01[7:0]	7:0	Noise masking motion ratio LUT_01.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_NM_MOTION_TABLE_23[7:0]	7:0	Noise masking motion ratio LUT_23.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_NM_MOTION_TABLE_45[7:0]	7:0	Noise masking motion ratio LUT_45.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_NM_MOTION_TABLE_67[7:0]	7:0	Noise masking motion ratio LUT_67.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_NM_MOTION_TABLE_89[7:0]	7:0	Noise masking motion ratio LUT_89.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_NM_MOTION_TABLE_AB[7:0]	7:0	Noise masking motion ratio LUT_AB.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_NM_MOTION_TABLE_CD[7:0]	7:0	Noise masking motion ratio LUT_CD.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_NM_MOTION_TABLE_EF[7:0]	7:0	Noise masking motion ratio LUT_EF.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x10**	**Access : R/W**
	DBK_MOTION_TABLE_01[7:0]	7:0	De-blocking motion ratio LUT_01.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x32**	**Access : R/W**
	DBK_MOTION_TABLE_23[7:0]	7:0	De-blocking motion ratio LUT_23.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x54**	**Access : R/W**
	DBK_MOTION_TABLE_45[7:0]	7:0	De-blocking motion ratio LUT_45.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x76**	**Access : R/W**
	DBK_MOTION_TABLE_67[7:0]	7:0	De-blocking motion ratio LUT_67.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x98**	**Access : R/W**
	DBK_MOTION_TABLE_89[7:0]	7:0	De-blocking motion ratio LUT_89.	

SC1 SNR Register (Bank = 102F, Sub-Bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0xBA**	**Access : R/W**
	DBK_MOTION_TABLE_AB[7:0]	7:0	De-blocking motion ratio LUT_AB.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0xDC**	**Access : R/W**
	DBK_MOTION_TABLE_CD[7:0]	7:0	De-blocking motion ratio LUT_CD.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0xFE**	**Access : R/W**
	DBK_MOTION_TABLE_EF[7:0]	7:0	De-blocking motion ratio LUT_EF.	
7Ch ~ 7Fh (102FF8h ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO_BO[3:0]	7:4	Main window border outside height of Left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.	
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.	
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.	
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.	
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.	
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.	
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.	
	-	3:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST[7:0]	7:0	Sub window Horizontal Start.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST[7:0]	7:0	Sub window Vertical Star.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND[7:0]	7:0	Sub window Vertical End.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_3RD[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	See description of '102F24h'.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_4TH[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_4TH[11:8]	3:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_4TH[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWBCOL[7:0]	7:0	Sub Window Border Color.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
20h	**REG102F41**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SMEN	7	SVM Main window Enable.	
	SMTE	6	SVM Main window Tap Enable.	
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
	SSWEN	3	SVM Sub window Enable.	
	SSWETE	2	SVM Sub window Tap Enable.	
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.	
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.	
	SVMBYS[1:0]	5:4	SVM Bypass Y Select. 0x: SMV data. 10: Original Y data.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: Y with tap filter.	
	SCORING[3:0]	3:0	SVM Coring.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SVMLMT[7:0]	7:0	SVM Limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM Main window Step.	
	SMGAIN[3:0]	3:0	SVM Main window Gain.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM Sub window Step.	
	SWGAIN[3:0]	3:0	SVM Sub window Gain.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM Pipe Adjust.	
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SVM_SEP_DLY	7	SVM Separate Delay Enable.	
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.	
	IPFI	5	To Pad Field Invert enable.	
	-	4:2	Reserved.	
	IOFI	1	Interlace Output Field Invert.	
	IOEN	0	Interlace Output Enable.	
2Bh	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.	
	-	3:0	Reserved.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_FINV	7	IP Field Inverse.	
	IP_ITLC	6	IP Interlace.	
	-	5:4	Reserved.	
	BES[1:0]	3:2	Border Extend for SVM.	
	OES[1:0]	1:0	OSD Extend for SVM.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.	
	RESERVED[1:0]	6:5	RESERVED.	
	-	4:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_BRI_OFFSET[7:0]	7:0	Offset for R data.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_EN	7	Brightness enable (after gamma).	
	CON_EN	6	Contrast enable (after gamma).	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	G_BRI_OFFSET[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	See description of '102F64h'.	
33h	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_R[7:0]	7:0	Brightness offset (bri_function) for main window R.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_G[7:0]	7:0	Brightness offset (bri_function) for main window G.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_G[10:8]	2:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_B[7:0]	7:0	Brightness offset (bri_function) for main window B.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	See description of '102F70h'.	
39h	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	S_BRI_R[7:0]	7:0	Brightness offset (bri_function) for sub window R.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_G[7:0]	7:0	Brightness offset (bri_function) for sub window G.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_B[7:0]	7:0	Brightness offset (bri_function) for sub window B.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE0[7:0]	7:0	Check value for auto mload base0 R channel.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE0[11:8]	3:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE1[7:0]	7:0	Check value for auto mload base1 R channel.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE1[11:8]	3:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE0[7:0]	7:0	Check value for auto mload base0 G channel.	
3Eh	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE0[11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE1[7:0]	7:0	Check value for auto mload base1 G channel.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_1	7	Base1 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE1[11:8]	3:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE0[7:0]	7:0	Check value for auto mload base0 B channel.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE0[11:8]	3:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE1[7:0]	7:0	Check value for auto mload base1 B channel.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE1[11:8]	3:0	See description of '102F82h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CAP_STAGE	4	Capture stage selection. 0: Before OSD. 1: After OSD.	
	-	3:0	Reserved.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_CON_GAIN[11:8]	3:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_CON_GAIN[11:8]	3:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_CON_GAIN[11:8]	3:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.	
4Dh	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:3	Reserved.	
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.	
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma CON_BRI.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.	
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.	
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FREEZ_VCNT_VALUE[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when REG_NEW_LOCK_POINT is set high.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LOCK_VCNT_VALUE[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PSEUDO_VS_EN	6	Enable pseudo vsync for freeze region.	
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.	
	OTUPUT_FIELD_INV	4	Invert field for output reference signal.	
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.	
	IVS_SEL	2	Select insert_end point as input reference for frame PLL.	
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.	
	INPUT_FREEZ	0	V-counter freeze enable.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VCNT_FREEZ_REGION	7	In V-counter freeze status.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6:2	Reserved.	
	IVS_CNT[9:8]	1:0	Frame number for input reference generation.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for CCIR656 format.	
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for CCIR656 format.	
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.	
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.	
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.	
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.	
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.	
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.	
	NOISE_DITH_EN	5	Noise dither enable.	
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.	
	CAP_EN	3	Capture image to IP enable.	
	-	2:0	Reserved.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. REG_MAIN_R_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_R_MIN_LIMIT. REG_MAIN_R_MIN_SIGN = 0: MAIN_R_MIN = MAIN_R_MIN_LIMIT.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_MAIN_G_MIN_SIGN = 1: MAIN_G_MIN = -MAIN_G_MIN_LIMIT. REG_MAIN_G_MIN_SIGN = 0: MAIN_G_MIN = MAIN_G_MIN_LIMIT.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_MAIN_B_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_B_MIN_LIMIT. REG_MAIN_B_MIN_SIGN = 0: MAIN_R_MIN = MAIN_B_MIN_LIMIT.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. REG_SUB_R_MIN_SIGN = 1: MAIN_R_MIN = -SUB_R_MIN_LIMIT. REG_SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_SUB_G_MIN_SIGN = 1: MAIN_G_MIN = -SUB_G_MIN_LIMIT. REG_SUB_G_MIN_SIGN = 0: MAIN_G_MIN = SUB_G_MIN_LIMIT.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_SUB_B_MIN_SIGN = 1: MAIN_R_MIN = -SUB_B_MIN_LIMIT. REG_SUB_B_MIN_SIGN = 0: MAIN_R_MIN = SUB_B_MIN_LIMIT.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
63h	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '102FC6h'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FWC_SAT_FROM_YUV	5	Saturation Calculation from YUV domain.	
	FWC_SUB_EN	4		
	FWC_DELTAX2X4[1:0]	3:2	0x0: No change. 0x1: R5_offset to R16_offset, B5_offset to B16_offset x2 (-256 to +254). 0x2: R5_offset to R16_offset, B5_offset to B16_offset x4 (-512 to +508).	
	FWC_DITHER_EN	1		
	FWC_MAIN_EN	0	Main window Fresh White Correction Function on/off.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FWC_STRENGTH[3:0]	3:0		
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FWC_SLOPE[5:0]	5:0	Fresh white strength decreasing slope between gray color and non-gray color area.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	FWC_CTH[7:0]	7:0	Fresh white Function Saturation threshold.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[7:0]	7:0	R adjust offset.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[23:16]	7:0	See description of '102FE4h'.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[31:24]	7:0	See description of '102FE4h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[39:32]	7:0	See description of '102FE4h'.	
74h	**REG102FE9**	**7:0**	**Default : 0x80**	**Access : R/W**

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FWC_DELTA_R[47:40]	7:0	See description of '102FE4h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[55:48]	7:0	See description of '102FE4h'.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[63:56]	7:0	See description of '102FE4h'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[71:64]	7:0	See description of '102FE4h'.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[79:72]	7:0	See description of '102FE4h'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[87:80]	7:0	See description of '102FE4h'.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[95:88]	7:0	See description of '102FE4h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[7:0]	7:0	B adjust offset.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[15:8]	7:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[23:16]	7:0	See description of '102FF4h'.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[31:24]	7:0	See description of '102FF4h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[39:32]	7:0	See description of '102FF4h'.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[47:40]	7:0	See description of '102FF4h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[55:48]	7:0	See description of '102FF4h'.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[63:56]	7:0	See description of '102FF4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[71:64]	7:0	See description of '102FF4h'.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[79:72]	7:0	See description of '102FF4h'.	

SC1 S_VOP Register (Bank = 102F, Sub-Bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[87:80]	7:0	See description of '102FF4h'.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[95:88]	7:0	See description of '102FF4h'.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND0[7:0]	7:0	20h: Recommended value (power on default value is 0).	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_NO_SIGNAL_SEL	7	Select main window mute source. 1: From main window mute source. 0: From sub window mute source.	
	SUB_NO_SIGNAL_SEL	6	Select sub window mute source. 1: From sub window mute source. 0: From main window mute source.	
	MAIN_NO_SIGNAL_EN	5	Enable main window mute by no signal or AV mute.	
	SUB_NO_SIGNAL_EN	4	Enable sub window mute by no signal or AV mute.	
	-	3:1	Reserved.	
	DB_MASK	0	Double buffer register mask signal. The double buffer register is updated when DB_MASK and DB_LOAD.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSST[7:0]	7:0	Output VSYNC start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VSST_D11	4	Output VSYNC D[11]start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h - 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No Signal VSYNC. Registers 22h and 23h are used to define minimum H total.	
	VSST[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOVS=1).	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSEND[11:8]	3:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHST[7:0]	7:0	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEHST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHEND[7:0]	7:0	Output DE Horizontal END. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEHEND[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVST[7:0]	7:0	Output DE Vertical Start. 00: Default value.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTSEL	7	Vertical Start Select. 0: DEVST[10:0] is Output DE vertical start. 1: DEVST[10:0] is Scaling Image Window vertical start.	
	-	6:4	Reserved.	
	DEVST[11:8]	3:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVEND[7:0]	7:0	Output DE Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEVEND[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start. 48h: Recommended value (power on default is 0).	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SIHST[12:8]	4:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SIHEND[12:8]	4:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVST[7:0]	7:0	Scaling Image window Vertical Start.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVST[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVEND[7:0]	7:0	Scaling Image window Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVEND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDTOT[7:0]	7:0	Output Horizontal Total. 53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HDTOT[12:8]	4:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDTOT[7:0]	7:0	Output Vertical Total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VDTOT[11:8]	3:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND[7:0]	7:0	20h: Recommended value (power on default value is 0).	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x4C**	**Access : R/W**
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 - 0x23).	
	OUTM	6	Output Mode. 0: Mode 0. 1: Mode 1.	
	-	5:4	Reserved.	
	EHTT	3	Even H Total. 0: Enable, Output H Total is always even pixels. 1: Disable, Output H Total is always odd pixels.	
	MOD2	2	Mode 2. 0: Disable. 1: Enable.	
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLLMD0	7	Frame PLL Mode 0.	
	SL_TUNE_EN	6	Short line tune enable.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_H_TOTAL_UPDATE_EN	5	Enable update AUTO_H_TOTAL value to H_TOTAL.	
	-	4:2	Reserved.	
	SSC_SHIFT	1	0: Enable. 1: Disable.	
	CLKDIV2_POINT_SELECT	0	0: Original. 1: New.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x20**	**Access : R/W**
	LCK_TH[7:0]	7:0	Frame PLL Lock Threshold.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x08**	**Access : R/W**
	LCK_TH[15:8]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	FTNS[3:0]	7:4	Tune Frame Number of Short-line tune.	
	-	3	Reserved.	
	PIP_REG_EN	2	PIP Register Enable.	
	-	1	Reserved.	
	NOISY_GEN	0	Noise Generator.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT1[7:0]	7:0	Frame PLL Limit.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT0[7:0]	7:0	Frame PLL Limit.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT[7:0]	7:0	Frame PLL Limit.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : RO**
	INTLX_VS_OFFSET[7:0]	7:0	The interlace vsync offset.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLX_VS_EN	5	Interlace vsync enable.	
	INTLX_VS_OFFSET[12:8]	4:0	See description of '102F2Eh'.	
18h	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BY_STAGE_VIP[3:0]	7:4	Vip report point stage.	
	BY_STAGE_OP2[3:0]	3:0	Report point stage.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	REP_RD_TRID	0	Report SW read trigger.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SWBLBK	6	Sub window Blue screen color. 0: Black color. 1: Blue color.	
	SWBLUE	5	Sub window Blue screen control. 0: Off. 1: On.	
	-	4:3	Reserved.	
	MBD_EN	2	Main window Border Enable.	
	MBLK	1	Main window Black screen control. 0: Off. 1: On.	
	NOSC_EN	0	No Signal Color Enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_G[7:0]	7:0	Frame Color - Green.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_B[7:0]	7:0	Frame Color - Blue.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_E_4_FRAME	7	Reset noise generator by frames enable.	
	NDMD	6	Noise Dithering Method.	
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.	
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.	
	DT3	3	Dither Type 2 control. 0: Disable dither type 2. 1: Enable dither type 2.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.	
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.	
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SHORT_1LINE_DISABLE	6	1: Disable. 0: Enable.	
	-	5	Reserved.	
	EGWT	4	Encode Gamma Write.	
	-	3:1	Reserved.	
	OUTFRR_EN0	0	Output Free-run Enable.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x07**	**Access : R/W**
	TUNE_FIELD_IP	7	Select insert point of one field for VOP_DISP inset signal.	
	-	6:0	Reserved.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LMT_ADD_NMB[7:0]	7:0	Limit adjust Number in ACC_FPLL mode.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_MD1	7	FPLL Mode 1.	
	FPLL_DIS	6	FPLL Stop.	
	-	5:3	Reserved.	
	ADD_LINE_SEL	2	Select Add Line into frame or pixel into line.	
	-	1:0	Reserved.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DOT	6	Differential Output Type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/Increased-swing RSDS.	
	WHTS	5	White Screen (including Main window and Sub window).	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	BLSK	4	Black Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	REVERSE	3	REVERSE luminosity. 0: Off. 1: On.	
	-	2:0	Reserved.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBLALL_SET	7	Frame buffer less all set.	
	-	6:0	Reserved.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCHBLEND	7	OSD Character Blending mode.	
	-	6	Reserved.	
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).	
	-	4	Reserved.	
	GATP	3	Gamma Automatically On/Off based on Auto Phase value. 0: Disable. 1: Enable.	
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0%% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x8F**	**Access : R/W**
	OSD_PATH4_SEL	7	Select DWIN capture source. 1: For OSD output. 0: For others.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6:4	Reserved.	
	MAIN_NO_SIGNAL_SOURCE_EN	3	Main window no signal source enable.	
	SUB_NO_SIGNAL_SOURCE_EN	2	Sub window no signal source enable.	
	MAIN_AV_MUTE_SOURCE_EN	1	Main window av mute source enable.	
	SUB_AV_MUTE_SOURCE_EN	0	Sub window av mute source enable.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	MNS_COL[7:0]	7:0	Main Window No Signal Color.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	MBCOL[7:0]	7:0	Main Window Border Color.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	-	6:0	Reserved.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLOCK_DL_LN[2:0]	5:3	Delay line number in Flock mode.	
	FLOCK_AH_LN[2:0]	2:0	Ahead line in Flock mode.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: -128~127.	
	GRAN	1	Green Range. 0: 0~255.1: -128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: -128~127.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSFD	7	Sub window Shift Field. 0: Shift even field. 0: Shift odd field.	
	SSLN[1:0]	6:5	Sub window Shift Line Numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.	
	ILIM	4	Insert Line when Interlace Mode. 0: Do not insert. 1: Insert.	
	MSFD	3	Main window Shift Field. 0: Shift even field. 1: Shift odd field.	
	MSLN[2:0]	2:0	Main window Shift Line Numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 lines between odd and even field. 010: Shift 2 lines between odd and even field. 011: Shift 3 lines between odd and even field. 1xx: Shift 4 lines between odd and even field.	
30h	**REG102F60**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IFVP[7:0]	7:0	Insert Fraction Vertical Position.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[7:0]	7:0	Insert Fraction Width. PD Down value.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : RO**
	OVSSTAT[7:0]	7:0	Output Vertical Total Status. Lock status. Equal to 1 when phase error less than 29h/2Ah.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	OVERDESTAT	6	Output Vertical DE Status.	
	-	5:3	Reserved.	
	OVSSTAT[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	OHTSTAT0[7:0]	7:0	OHSTAT initial value.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : RO**
	OHTSTAT1[7:0]	7:0	Output H Total Status.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRACST0[7:0]	7:0	Fraction initial value.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	FRACST1[7:0]	7:0	Fraction Status.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FRACST2[2:0]	2:0	Fraction Status.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FRACST3[2:0]	2:0	Fraction Status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	HTTMGN[7:0]	7:0	H Total Margin.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSCMGN[7:0]	7:0	SSC Margin.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSTVALUE0[7:0]	7:0	Read Start initial value.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	RSTVALUE1[7:0]	7:0	Read Start Value.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RSTVALUE2[4:0]	4:0	Read Start initial value.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	RSTVALUE3[4:0]	4:0	Read Start Value.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRONT_BACK	5	Set front back mode.	
	-	4:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	INP8	7	This bit with REG_INE_DRV3 to enable G replace R and B for gamma mapping.	
	ONE_DRV3	6	Gamma use G replace R and B for gamma mapping.	
	GABYP	5	By pass gamma function.	
	-	4:3	Reserved.	
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTDATA[7:0]	7:0	Reserved.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	LFCOEF1[2:0]	7:5	Loop filter coefficient 1.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LFCOEF2[4:0]	4:0	Loop filter coefficient 2.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	TFRACN[7:0]	7:0	Target Fraction Number. / Frame PLL limit RK[7:0].	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	PDP_MASK_EN	6	Reserved.	
	-	5	Reserved.	
	FX_PROT	4	Frame Change Protect.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x40**	**Access : R/W**
	TSTMD_REG_EN	7	Test Mode Register Enable. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	SEE_DEBUG_SEL[2:0]	5:3	See Debug bus output byte enable, bit0=DI[7:0], bit1=DI[15:8], bit2=DI[23:16].	
	-	2:0	Reserved.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CLK_MODE	7	0: Disable. 1: Enable.	
	-	6	Reserved.	
	DDR_TEST	5	1: Select DDR 29est bus.	
	TEST_MD_D	4	1: Enable 24-bit test bus output.	
	TEST_MD[3:0]	3:0	Reserved.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	BOND_STS[7:0]	7:0	Reserved.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x44**	**Access : R/W**
	LP_SET0[7:0]	7:0	Output PLL Set.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x55**	**Access : R/W**
	LP_SET0[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	LP_SET1[7:0]	7:0	Output PLL Set.	
50h	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	OBN10	7	10-bit Bus enable.	
	DITHER_MINUS	6	1: Enable.	
	-	5	Reserved.	
	M_GRG	4	Main window Gamma Rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_ST[7:0]	7:0	OSD new reference h start.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_NEW_REF	7	OSD new reference enable.	
	-	6:4	Reserved.	
	OSD_HS_ST[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_END[7:0]	7:0	OSD new reference h end.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_HS_END[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_ST[7:0]	7:0	OSD new reference v start.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OSD_VFDE_ST[10:8]	2:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_END[7:0]	7:0	OSD new reference v end.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OSD_VFDE_END[10:8]	2:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIM_HS	7	Limit Htotal by PWM counter enable.	
	NEW_FIELD_SEL	6	Select field created method. 0: Created by Vsync and Hsync. 1: Created by VFDE.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end. 1: Vsync end.	
	-	4:0	Reserved.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	REM[7:0]	7:0	Htotal REMainder value.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	REM[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DIV[7:0]	7:0	PWM5 CLK div factor.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PWM5DIV[8]	0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DUTY[7:0]	7:0	PWM5 period.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	TRACE_PHASE_HTOTAL[7:0]	7:0	New Htotal for fast phase offset reduce, only active when REG_TRACE_PHASE_EN is set to 1.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TRACE_PHASE_EN	4	Enable modify Htotal for fast phase offset reduce.	
	TRACE_PHASE_HTOTAL[11:8]	3:0	See description of '102FB4h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x07**	**Access : R/W**
	BIUCLK_DIV[7:0]	7:0	Calculate VDE ratio BIUCLK divider.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RPT_VRATIO_EN	0	Report VDE Vtotal ratio enable.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_0_REG[7:0]	7:0		
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_1_REG[7:0]	7:0		
66h	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	PIP_OP2_2_REG[7:0]	7:0		
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_3_REG[7:0]	7:0		
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_4_REG[7:0]	7:0		
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_5_REG[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[7:0]	7:0	Input VDE PRD value.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[15:8]	7:0	See description of '102FD0h'.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[7:0]	7:0	Input Vtt PRD value.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HIFRC_SROT	7	Enable HIFRC spatial rotation.	
	RAN[1:0]	6:5	Enable HIFRC RANdom noise latch for rotation.	
	F2_EN	4	Enable noise repeats 2 frames.	
	NEW_DITH_M	3	New dither method select.	
	-	2	Reserved.	
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.	
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.	
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.	
	H_RAN_EN	3	H direction using random noise enable for HIFRC.	
	NEW_ACBD	2	Swap HIFRC probability sequence.	
	OLD_HIFRC	1	Select old HIFRC dither method.	
	RAN_DIR_EN	0	Enable noise as rotate direction.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table r/w address.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_W_FLAG2	7	LUT table blue write command.	
	LUT_W_FLAG1	6	LUT table green write command.	
	LUT_W_FLAG0	5	LUT table red write command.	
	-	4	Reserved.	
	LUT_BW_CH_SEL[1:0]	3:2	Lut table burst write channel selection: 2'b00: Select R channel. 2'b01: Select G channel. 2'b10: Select B channel. 2'b11: Select All R/G/B channel.	
	-	1	Reserved.	
	LUT_BW_MAIN_EN	0	Lut table burst write enable.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_R_FLAG2	7	LUT table blue read command.	
	LUT_R_FLAG1	6	LUT table green read command.	
	LUT_R_FLAG0	5	LUT table red read command.	
	-	4:1	Reserved.	
	LUT_BW_FLAG	0	Lut table burst write status when burst write enable.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_R[7:0]	7:0	Data write to R LUT SRAM.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_R[11:8]	3:0	See description of '102FDCh'.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_G[7:0]	7:0	Data write to G LUT SRAM.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_G[11:8]	3:0	See description of '102FDEh'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_B[7:0]	7:0	Data write to B LUT SRAM.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	WR_B[11:8]	3:0	See description of '102FE0h'.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_R[7:0]	7:0	Data read from R LUT SRAM.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_R[11:8]	3:0	See description of '102FE2h'.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_G[7:0]	7:0	Data read from G LUT SRAM.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_G[11:8]	3:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_B[7:0]	7:0	Data read from B LUT SRAM.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_B[11:8]	3:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:4	Reserved.	
	CLR_MLOAD_TOO_SLOW	3	Clear auto mload gamma too slow flag.	
	MLOAD_TOO_SLOW	2	Auto mload gamma too slow flag.	
	AUTO_MLOAD_SWITCH	1	Enable auto mload gamma switch gamma table by frame.	
	AUTO_MLOAD_GAMMA	0	Enable auto mload gamma function.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[15:8]	7:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[23:16]	7:0	See description of '102FEAh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[15:8]	7:0	See description of '102FEEh'.	
78h	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 VOP Register (Bank = 102F, Sub-Bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MLOAD_GAMMA_BASE1[23:16]	7:0	See description of '102FEEh'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE0[11:8]	3:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE1[11:8]	3:0	See description of '102FF6h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE0[11:8]	3:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE1[11:8]	3:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE0[11:8]	3:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE1[11:8]	3:0	See description of '102FFEh'.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data config from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data config from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data config from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data config from mode 5 change to mode 4.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_F1_EN	7	Enable OPM F1 register.	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	
	STILL_MODE_F2	3	F2 image freeze enable.	
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.	
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAPTURE_START_F2	7	F2 image capture start.	
	IPM_READ_OFF_F2	6	F2 force IP read request disable.	
	MADI_FORCE_OFF_F2	5	F2 force MADi off.	
	MADI_FORCE_ON_F2	4	F2 force MADi on.	
	FBL_25D	3	F2 frame buffer less de-interlace mode.	
	-	2	Reserved.	
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.	
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.	
	OPM_LINEAR_BASE_SEL_F2	6	F2 linear mode base address selection.	
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.	
	IPM_LINEAR_EN_F2	4	F2 IP linear address enable.	
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.	
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.	
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.	
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.	
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.	
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.	
	DOT_LN_PON_SEL_F2	1	F2 OP MADi dot line data select.	
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.	
	-	6:4	Reserved.	
	Y8_M4_ONLY_MODE_F2	3	F2 FB store Y8/M4 only mode.	
	Y8_ONLY_MODE_F2	2	F2 FB store Y-8bits only.	
	BOB_YMR_10_EN_F2	1	F2 10-bits Bob mode with Y motion.	
	BOB_YMR_8_EN_F2	0	F2 8-bits Bob mode with Y motion.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	BYPASS_DUAL_CH	6	Enable dual channel bypass.	
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.	
	IP_BYPASS_INTERLACE_FILM_F2	4	Film-supported bypass interlace mode.	
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.	
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.	
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.	
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F2	7	F2 memysnc write bank reset.	
	IPM_WREQ_HPRI_SEL_F2	6	F2 IPM wreq high priority selection: 1'b0: IPM local priority. 1'b1: ip2_adj priority.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FRC_FREEMD_F2	5	F2 Force output odd/even toggle when 2DDi for interlace input.	
	MIU_SELECT_F2	4	F2 access MIU0 or MIU1 select.	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY05_9_15[6:0]	7:1		
	BK_FIELD_SEL_F2	0	F2 memysnc fd selection.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RW_BANK_MAP_MSB_F2	7	F2 MSB bit of read/write bank mapping mode.	
	OPM_RBANK_SEL_MSB_F2	6	F2 OP force read bank select MSB.	
	-	5:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x88**	**Access : R/W**
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.	
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.	
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.	
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.	
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.	
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x40**	**Access : R/W**
	RW_BANK_MAP_F2[2:0]	7:5	F2 read/write bank mapping mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_BASE_ADDR0_F2[24]	0	See description of '102F10h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_PITCH_F2[7:0]	7:0	F2 IP frame buffer ring mode pitch.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_PITCH_F2[15:8]	7:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_PITCH_F2[23:16]	7:0	See description of '102F14h'.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_EN_F2	7	F2 IP frame buffer ring mode enable.	
	IPM_RING_INIT_F2	6	F2 IP frame buffer ring mode enable.	
	-	5:1	Reserved.	
	IPM_RING_PITCH_F2[24]	0	See description of '102F14h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_RBK_VCNT_F2[7:0]	7:0	F2 IP frame buffer ring mode rbank update point.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_RING_RBK_VCNT_F2[12:8]	4:0	See description of '102F18h'.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IPM_RING_OPM_BASE_USR_EN	3	F2 IP frame buffer ring OPM user mode.	
	-	2	Reserved.	
	IPM_RING_OPM_BASE_USR[1:0]	1:0	F2 IP frame buffer ring OPM user mode base selection.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_OFFSET_F2[12:8]	4:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_FETCH_NUM_F2[12:8]	4:0	See description of '102F1Eh'.	
10h	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F20h'.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR0_F2[24]	0	See description of '102F20h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR1_F2[24]	0	See description of '102F24h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F2[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_EN_F2	7	F2 IP line count limit enable.	
	-	6:5	Reserved.	
	IPM_VCNT_LIMIT_NUM_F2[12:8]	4:0	See description of '102F30h'.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FORCE_MUTE_IPW_ENABLE_F2	5	Force IPM enable at av-mute case.	
	FIELD_NUM_F2[4:0]	4:0	F2 field number.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_FIELD_NUM_DEFINE_F2	7	Enable OPM F2 field number define.	
	OPM_FIELD_NUM_F2[4:0]	6:2	OPM F2 field number.	
	OPM_8READ_EN_F2	1	F2 OPM 8read mode enable.	
	OPM_6READ_EN_F2	0	F2 OPM 6read mode enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_EN_F2	7	F2 IP write limit enable.	
	IPM_W_LIMIT_MIN_F2	6	F2 IP write limit flag 0: maximum 1: minimum.	
	-	5:1	Reserved.	
	IPM_W_LIMIT_ADR_F2[24]	0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_EN_F2	7	F2 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F2[14:8]	6:0	See description of '102F38h'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.	
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x28**	**Access : R/W**
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x28**	**Access : R/W**
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_FLOW_CTRL_CNT[7:0]	7:0	OPW request flow control count.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x88**	**Access : R/W**
	OPW_VP_CNT_CLR	7	OPW write mask field count clear.	
	OPW_MASK_MODE[2:0]	6:4	OPW write mask number by field.	
	OPW_STATUS_CLR	3	OPW status clear enable.	
	OPW_REQ_RST	2	OPW write request reset.	
	-	1	Reserved.	
	OPW_WREQ_OFF_F2	0	OPW write request disable.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OPW_WBE_MASK_DUP_EN	6	OPW mask write byte enable for dup-frame.	
	-	5:4	Reserved.	
	OPW_DUP_INIT_INV	3	OPW duplicate frame offset init invert.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPW_DUP_FRAME_LN_INV	2	OPW duplicate frame line mask invert.	
	OPW_DUP_FRAME_INV	1	OPW duplicate frame command mask invert.	
	OPW_DUP_FRAME_MD	0	OPW duplicate frame mode.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_THRD[7:0]	7:0	OPW FIFO threshold for read request.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_HPRI[7:0]	7:0	OPW high priority threshold for read request.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPW_WREQ_MAX[7:0]	7:0	OPW read request max number.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x22**	**Access : R/W**
	OPW_WFIFO_DEPTH[7:0]	7:0	OPW line buffer length for memory data write.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at real line case.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at real line case.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F2[4:0]	4:0	F2 OP extend data rbank difference between current	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			data rbank at dot line and NOC1 case.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IPM_3D_SBS_FORCE_EN_F2	1	F2 IPM 3D side by side input enable.	
	IPM_3D_EN_F2	0	F2 IPM 3D input enable.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OPM_DUP_FRAME_LN_INV	2	OPM duplicate frame line mask invert.	
	OPM_DUP_FRAME_MD	1	OPM duplicate frame mode.	
	-	0	Reserved.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY34_7_7	7	HDMI 3D OPM side by side read using PIP.	
	-	6:0	Reserved.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_LA_DELTA_1[3:0]	7:4	Delta for 3d LA at dot line.	
	OPM_LA_DELTA_0[3:0]	3:0	Delta for 3d LA at real line.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x08**	**Access : R/W**
	DUMMY40_4_15[3:0]	7:4		
	UPDATE_MEM_CONFIG_EN	3	Update memory format enable.	
	-	2	Reserved.	
	IPM_REG_DBF_EN_F2	1	F2 Register latch with input V sync enable.	
	OPM_REG_DBF_EN	0	Register latch with output V sync enable.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY40_4_15[11:4]	7:0	See description of '102F80h'.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MADI_FORCE_OFF_F1	5	F1 force MADi off.	
	MADI_FORCE_ON_F1	4	F1 force MADi on.	
	-	3:0	Reserved.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_LINEAR_EN_F1	4	F1 IP linear address enable.	
	OPM_4READ_EN_F1	3	F1 OP read 4 fields enable.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	OPM_3READ_EN_F1	2	F1 OP read 3 fields enable.	
	OPM_2READ_EN_F1	1	F1 OP read 2 fields enable.	
	OPM_1READ_EN_F1	0	F1 OP read 1 field enable.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	FILM_HIGH_PRI_F1	3	F1 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F1	2	F1 OP film dot line data select.	
	DOT_LN_PON_SEL_F1	1	F1 OP MADi dot line data select.	
	-	0	Reserved.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DUMMY44_2_3[1:0]	3:2		
	-	1:0	Reserved.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F1	7	F1 memysnc write bank reset.	
	IPM_WREQ_HPRI_SEL_F1	6	F1 IPM wreq high priority selection: 1'b0: IPM local priority. 1'b1: ip2_adj priority.	
	-	5:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY45_9_15[6:0]	7:1		
	BK_FIELD_SEL_F1	0	F2 memysnc fd selection.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY46_0_7[7:0]	7:0		
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_PITCH_F1[7:0]	7:0	F1 IP frame buffer ring mode pitch.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_PITCH_F1[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_PITCH_F1[23:16]	7:0	See description of '102F94h'.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_EN_F1	7	F1 IP frame buffer ring mode enable.	
	IPM_RING_INIT_F1	6	F1 IP frame buffer ring mode enable.	

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:1	Reserved.	
	IPM_RING_PITCH_F1[24]	0	See description of '102F94h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_RING_RBK_VCNT_F1[7:0]	7:0	F1 IP frame buffer ring mode rbank update point.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_RING_RBK_VCNT_F1[12:8]	4:0	See description of '102F98h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[7:0]	7:0	F1 OP frame buffer base address 0.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[23:16]	7:0	See description of '102FA0h'.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR0_F1[24]	0	See description of '102FA0h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[7:0]	7:0	F1 OP frame buffer base address 1.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[23:16]	7:0	See description of '102FA4h'.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR1_F1[24]	0	See description of '102FA4h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MWE_OFFSET_F1[7:0]	7:0	F1 OP demo mode pixel offset (pixel unit).	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_MWE_OFFSET_F1[11:8]	3:0	See description of '102FA8h'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F1[7:0]	7:0	F1 OP frame buffer line offset (pixel unit).	
56h	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	OPM_OFFSET_F1[12:8]	4:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F1[7:0]	7:0	F1 OP fetch pixel number of one line.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F1[11:8]	3:0	See description of '102FAEh'.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:2	Reserved.	
	OPM_8READ_EN_F1	1	F1 OPM 8read mode enable.	
	OPM_6READ_EN_F1	0	F1 OPM 6read mode enable.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[7:0]	7:0	OPW write limit address.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[23:16]	7:0	See description of '102FBCh'.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_EN	7	OPW write limit enable.	
	OPW_W_LIMIT_MIN	6	OPW write limit flag 0: maximum 1: minimum.	
	-	5:1	Reserved.	
	OPW_W_LIMIT_ADR[24]	0	See description of '102FBCh'.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY66_13_15[2:0]	7:5		
	-	4:0	Reserved.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x01**	**Access : R/W**
	DUMMY67_4_15[3:0]	7:4		
	-	3:2	Reserved.	
	OPW_WREQ_OFF_ALL	1	All OPW write request disable.	
	OPW_WREQ_OFF_F1	0	F1 OPW write request disable.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY67_4_15[11:4]	7:0	See description of '102FCEh'.	
6Ch	**REG102FD8**	**7:0**	**Default : 0x12**	**Access : R/W**

SC1 SCMI Register (Bank = 102F, Sub-Bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at real line case.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at real line case.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	

SC1 ACE Register (Bank = 102F, Sub-Bank = 18)

SC1 ACE Register (Bank = 102F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_FCC_8T_EN	7	Main window FCC region 8 enable.	
	MAIN_FCC_7T_EN	6	Main window FCC region 7 enable.	
	MAIN_FCC_6T_EN	5	Main window FCC region 6 enable.	
	MAIN_FCC_5T_EN	4	Main window FCC region 5 enable.	
	MAIN_FCC_4T_EN	3	Main window FCC region 4 enable.	
	MAIN_FCC_3T_EN	2	Main window FCC region 3 enable.	
	MAIN_FCC_2T_EN	1	Main window FCC region 2 enable.	
	MAIN_FCC_1T_EN	0	Main window FCC region 1 enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FCC_DITHER_EN	6	FCC dither bit enable.	
	-	5:2	Reserved.	
	MAIN_FCC_9T_FIRST_EN	1	Main window FCC window 9 priority one enable.	
	MAIN_FCC_9T_EN	0	Main window FCC window 9 enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_FCC_8T_EN	7	Sub window FCC region 8 enable.	
	SUB_FCC_7T_EN	6	Sub window FCC region 7 enable.	
	SUB_FCC_6T_EN	5	Sub window FCC region 6 enable.	
	SUB_FCC_5T_EN	4	Sub window FCC region 5 enable.	
	SUB_FCC_4T_EN	3	Sub window FCC region 4 enable.	
	SUB_FCC_3T_EN	2	Sub window FCC region 3 enable.	
	SUB_FCC_2T_EN	1	Sub window FCC region 2 enable.	
	SUB_FCC_1T_EN	0	Sub window FCC region 1 enable.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_FCC_9T_FIRST_EN	1	Sub window FCC window 9 priority one enable.	
	SUB_FCC_9T_EN	0	Sub window FCC region 9 enable.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_FCC_BDRY_DIST[1:0]	5:4	Sub window FCC boundary limit distance. #0: disable.	

SC1 ACE Register (Bank = 102F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			#1: x4. #2: x2. #3: x1.	
	-	3:2	Reserved.	
	MAIN_FCC_BDRY_DIST[1:0]	1:0	Main window FCC boundary limit distance. #0: disable. #1: x4. #2: x2. #3: x1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T1[7:0]	7:0	FCC region 1 cb target.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T1[7:0]	7:0	FCC region 1 cr target.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T2[7:0]	7:0	FCC region 2 cb target.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T2[7:0]	7:0	FCC region 2 cr target.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T3[7:0]	7:0	FCC region 3 cb target.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T3[7:0]	7:0	FCC region 3 cr target.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T4[7:0]	7:0	FCC region 4 cb target.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T4[7:0]	7:0	FCC region 4 cr target.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T5[7:0]	7:0	FCC region 5 cb target.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T5[7:0]	7:0	FCC region 5 cr target.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T6[7:0]	7:0	FCC region 6 cb target.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T6[7:0]	7:0	FCC region 6 cr target.	
1Eh	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 ACE Register (Bank = 102F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FCC_CB_T7[7:0]	7:0	FCC region 7 cb target.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T7[7:0]	7:0	FCC region 7 cr target.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T8[7:0]	7:0	FCC region 8 cb target.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T8[7:0]	7:0	FCC region 8 cr target.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_2T[3:0]	7:4	FCC region 2 strength.	
	FCC_K_1T[3:0]	3:0	FCC region 1 strength.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_4T[3:0]	7:4	FCC region 4 strength.	
	FCC_K_3T[3:0]	3:0	FCC region 3 strength.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_6T[3:0]	7:4	FCC region 6 strength.	
	FCC_K_5T[3:0]	3:0	FCC region 5 strength.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_8T[3:0]	7:4	FCC region 8 strength.	
	FCC_K_7T[3:0]	3:0	FCC region 7 strength.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	FCC_K_9T[3:0]	3:0	FCC region 9 strength.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN1_CB_UP[1:0]	7:6	FCC region 1 target cb up distance.	
	FCC_WIN1_CB_DOWN[1:0]	5:4	FCC region 1 target cb down distance.	
	FCC_WIN1_CR_UP[1:0]	3:2	FCC region 1 target cr up distance.	
	FCC_WIN1_CR_DOWN[1:0]	1:0	FCC region 1 target cr down distance.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN2_CB_UP[1:0]	7:6	FCC region 2 target cb up distance.	
	FCC_WIN2_CB_DOWN[1:0]	5:4	FCC region 2 target cb down distance.	
	FCC_WIN2_CR_UP[1:0]	3:2	FCC region 2 target cr up distance.	
	FCC_WIN2_CR_DOWN[1:0]	1:0	FCC region 2 target cr down distance.	
25h	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 ACE Register (Bank = 102F, Sub-Bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
	FCC_WIN3_CB_UP[1:0]	7:6	FCC region 3 target cb up distance.	
	FCC_WIN3_CB_DOWN[1:0]	5:4	FCC region 3 target cb down distance.	
	FCC_WIN3_CR_UP[1:0]	3:2	FCC region 3 target cr up distance.	
	FCC_WIN3_CR_DOWN[1:0]	1:0	FCC region 3 target cr down distance.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN4_CB_UP[1:0]	7:6	FCC region 4 target cb up distance.	
	FCC_WIN4_CB_DOWN[1:0]	5:4	FCC region 4 target cb down distance.	
	FCC_WIN4_CR_UP[1:0]	3:2	FCC region 4 target cr up distance.	
	FCC_WIN4_CR_DOWN[1:0]	1:0	FCC region 4 target cr down distance.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN5_CB_UP[1:0]	7:6	FCC region 5 target cb up distance.	
	FCC_WIN5_CB_DOWN[1:0]	5:4	FCC region 5 target cb down distance.	
	FCC_WIN5_CR_UP[1:0]	3:2	FCC region 5 target cr up distance.	
	FCC_WIN5_CR_DOWN[1:0]	1:0	FCC region 5 target cr down distance.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN6_CB_UP[1:0]	7:6	FCC region 6 target cb up distance.	
	FCC_WIN6_CB_DOWN[1:0]	5:4	FCC region 6 target cb down distance.	
	FCC_WIN6_CR_UP[1:0]	3:2	FCC region 6 target cr up distance.	
	FCC_WIN6_CR_DOWN[1:0]	1:0	FCC region 6 target cr down distance.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN7_CB_UP[1:0]	7:6	FCC region 7 target cb up distance.	
	FCC_WIN7_CB_DOWN[1:0]	5:4	FCC region 7 target cb down distance.	
	FCC_WIN7_CR_UP[1:0]	3:2	FCC region 7 target cr up distance.	
	FCC_WIN7_CR_DOWN[1:0]	1:0	FCC region 7 target cr down distance.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN8_CB_UP[1:0]	7:6	FCC region 8 target cb up distance.	
	FCC_WIN8_CB_DOWN[1:0]	5:4	FCC region 8 target cb down distance.	
	FCC_WIN8_CR_UP[1:0]	3:2	FCC region 8 target cr up distance.	
	FCC_WIN8_CR_DOWN[1:0]	1:0	FCC region 8 target cr down distance.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FCC_WIN9_CB[2:0]	5:3	FCC region 9 target cb distance.	
	FCC_WIN9_CR[2:0]	2:0	FCC region 9 target cr distance.	

SC1 ACE Register (Bank = 102F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WPL_WHITE_PEAK_LIMIT_THRD[7:0]	7:0	White peak limit threshold.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_HIGH_PASS_EN	7	Main window Y H_coring as high pass filter.	
	MAIN_Y_TABLE_STEP[2:0]	6:4	Main window Y H_coring LUT step.	
	MAIN_PC_MODE	3	Main window PC mode.	
	-	2	Reserved.	
	MAIN_Y_BAND2_H_CORING_EN	1	Main window Y band2 H_coring enable.	
	MAIN_Y_BAND1_H_CORING_EN	0	Main window Y band1 H_coring enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_HIGH_PASS_EN	7	Main window C H_coring as high pass filter.	
	MAIN_C_TABLE_STEP[2:0]	6:4	Main window C H_coring LUT step.	
	MAIN_WHITE_PEAK_LIMIT_EN	3	Main window white peak limit enable.	
	-	2	Reserved.	
	MAIN_C_BAND2_H_CORING_EN	1	Main window C band2 H_coring enable.	
	MAIN_C_BAND1_H_CORING_EN	0	Main window C band1 H_coring enable.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE1[7:0]	7:0	Main window Y gain table 1.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE2[7:0]	7:0	Main window Y gain table 2.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE3[7:0]	7:0	Main window Y gain table 3.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE4[7:0]	7:0	Main window Y gain table 4.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE1[7:0]	7:0	Main window C gain table 1.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE2[7:0]	7:0	Main window C gain table 2.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE3[7:0]	7:0	Main window C gain table 3.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE4[7:0]	7:0	Main window C gain table 4.	
55h	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 ACE Register (Bank = 102F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_Y_NOISE_MASKING_EN	7	Main window horizontal Y NMR enable.	
	MAIN_Y_COLOR_NOISE_MASKING_EN	6	Main window horizontal Y NMR color adaptive enable.	
	MAIN_Y_NOISE_MASK_GAIN[5:0]	5:0	Main window horizontal Y NMR gain (xxxx.xx).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_Y_NM_MIN_THRD[3:0]	7:4	Main window Y mosquito noise remove min value threshold.	
	MAIN_Y_NM_MAX_THRD[3:0]	3:0	Main window Y mosquito noise remove max value threshold.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_HIGH_PASS_EN	7	Sub window Y H_coring as high pass filter.	
	SUB_Y_TABLE_STEP[2:0]	6:4	Sub window Y H_coring LUT step.	
	SUB_PC_MODE	3	Sub window PC mode.	
	-	2	Reserved.	
	SUB_Y_BAND2_H_CORING_EN	1	Sub window Y band2 H_coring enable.	
	SUB_Y_BAND1_H_CORING_EN	0	Sub window Y band1 H_coring enable.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_HIGH_PASS_EN	7	Sub window C H_coring as high pass filter.	
	SUB_C_TABLE_STEP[2:0]	6:4	Sub window C H_coring LUT step.	
	SUB_WHITE_PEAK_LIMIT_EN	3	Sub window white peak limit enable.	
	-	2	Reserved.	
	SUB_C_BAND2_H_CORING_EN	1	Sub window C band2 H_coring enable.	
	SUB_C_BAND1_H_CORING_EN	0	Sub window C band1 H_coring enable.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_NOISE_MASKING_EN	7	Sub window horizontal Y noise-masking enable.	
	SUB_Y_COLOR_NOISE_MASKING_EN	6	Sub window horizontal Y noise-masking color adaptive enable.	
	-	5:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Pseudo return to initial value frame numbers. #2'b00: 1 frame initial. #2'b01: 2 frame initial. #2'b10: 4 frame initial. #2'b11: 8 frame initial.	

SC1 ACE Register (Bank = 102F, Sub-Bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PSEUDO_VCLR_EN	0	Pseudo return to initial value by vclear enable.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R2Y_EN	4	Sub window RGB to YCbCr enable.	
	-	3:2	Reserved.	
	R2Y_DITHER_EN	1	RGB to YCbCr dither enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr enable.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_R2Y_EQ_SEL[2:0]	6:4	Sub window RGB to YCbCr equation selection. 3'b000: SDTV with R' G' B' 16-235 range. 3'b001: SDTV with R' G' B' 0-255 range. 3'b010: HDTV with R' G' B' 16-235 range. 3'b011: HDTV with R' G' B' 0-255 range. 3'b100: 709 to 601.	
	-	3	Reserved.	
	MAIN_R2Y_EQ_SEL[2:0]	2:0	Main window RGB to YCbCr equation selection. 3'b000: SDTV with R' G' B' 16-235 range. 3'b001: SDTV with R' G' B' 0-255 range. 3'b010: HDTV with R' G' B' 16-235 range. 3'b011: HDTV with R' G' B' 0-255 range. 3'b100: 709 to 601.	
74h (102FE9h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	VPS_SRAM_ACT	7	2D peaking line-buffer SRAM active.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2:1	Reserved.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_PEAKING_EN	7	Main window band8 peaking enable.	
	MAIN_BAND7_PEAKING_EN	6	Main window band7 peaking enable.	
	MAIN_BAND6_PEAKING_EN	5	Main window band6 peaking enable.	
	MAIN_BAND5_PEAKING_EN	4	Main window band5 peaking enable.	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.	
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.	
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.	
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_COEF_STEP[1:0]	7:6	Main window band8 coefficient step.	
	MAIN_BAND7_COEF_STEP[1:0]	5:4	Main window band7 coefficient step.	
	MAIN_BAND6_COEF_STEP[1:0]	3:2	Main window band6 coefficient step.	
	MAIN_BAND5_COEF_STEP[1:0]	1:0	Main window band5 coefficient step.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_V_NOISE_MASKING_EN	7	Main window vertical Y noise-masking enable.	
	MAIN_V_COLOR_NOISE_MASKING_EN	6	Main window vertical Y noise-masking color adaptive enable.	
	MAIN_V_NOISE_MASK_GAIN[5:0]	5:0	Main window vertical Y noise-masking gain.	
12h	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7	Reserved.	
	MAIN_V_LPF_COEF_2[2:0]	6:4	Main window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	
	MAIN_V_LPF_COEF_1[2:0]	2:0	Main window vertical up-down pixel Y LPF coefficient.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_OSD_SHARPNESS_CTRL[5:0]	5:0	Main window user sharpness adjust.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_LPF_COEF[2:0]	6:4	Sub window horizontal Y LPF coefficient.	
	MAIN_SUB_EXCHANGE_EN	3	Main/Sub window swap enable.	
	-	2:1	Reserved.	
	SUB_POST_PEAKING_EN	0	Sub window 2D peaking enable.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND8_PEAKING_EN	7	Sub window band8 peaking enable.	
	SUB_BAND7_PEAKING_EN	6	Sub window band7 peaking enable.	
	SUB_BAND6_PEAKING_EN	5	Sub window band6 peaking enable.	
	SUB_BAND5_PEAKING_EN	4	Sub window band5 peaking enable.	
	SUB_BAND4_PEAKING_EN	3	Sub window band4 peaking enable.	
	SUB_BAND3_PEAKING_EN	2	Sub window band3 peaking enable.	
	SUB_BAND2_PEAKING_EN	1	Sub window band2 peaking enable.	
	SUB_BAND1_PEAKING_EN	0	Sub window band1 peaking enable.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND4_COEF_STEP[1:0]	7:6	Sub window band4 coefficient step.	
	SUB_BAND3_COEF_STEP[1:0]	5:4	Sub window band3 coefficient step.	
	SUB_BAND2_COEF_STEP[1:0]	3:2	Sub window band2 coefficient step.	
	SUB_BAND1_COEF_STEP[1:0]	1:0	Sub window band1 coefficient step.	
15h	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BAND8_COEF_STEP[1:0]	7:6	Sub window band8 coefficient step.	
	SUB_BAND7_COEF_STEP[1:0]	5:4	Sub window band7 coefficient step.	
	SUB_BAND6_COEF_STEP[1:0]	3:2	Sub window band6 coefficient step.	
	SUB_BAND5_COEF_STEP[1:0]	1:0	Sub window band5 coefficient step.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_V_NOISE_MASKING_EN	7	Sub window vertical Y noise-masking enable.	
	SUB_V_COLOR_NOISE_MASKING_EN	6	Sub window vertical Y noise-masking color adaptive enable.	
	SUB_V_NOISE_MASK_GAIN[5:0]	5:0	Sub window vertical Y noise-masking gain.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_V_LPF_COEF_2[2:0]	6:4	Sub window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	
	SUB_V_LPF_COEF_1[2:0]	2:0	Sub window vertical up-down pixel Y LPF coefficient.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CORING_THRD_2[3:0]	7:4	Sub window coring threshold 2.	
	SUB_CORING_THRD_1[3:0]	3:0	Sub window coring threshold 1.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_OSD_SHARPNESS_CTRL[5:0]	5:0	Sub window user sharpness adjust.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND5_COEF[5:0]	5:0	Main window band5 coefficient.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND6_COEF[5:0]	5:0	Main window band6 coefficient.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND7_COEF[5:0]	5:0	Main window band7 coefficient.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_BAND8_COEF[5:0]	5:0	Main window band8 coefficient.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM2_SELECT[2:0]	6:4	Main window peaking term2 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM1_SELECT[2:0]	2:0	Main window peaking term1 select.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM4_SELECT[2:0]	6:4	Main window peaking term4 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM3_SELECT[2:0]	2:0	Main window peaking term3 select.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM6_SELECT[2:0]	6:4	Main window peaking term6 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM5_SELECT[2:0]	2:0	Main window peaking term5 select.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM8_SELECT[2:0]	6:4	Main window peaking term8 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM7_SELECT[2:0]	2:0	Main window peaking term7 select.	

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM10_SELECT[2:0]	6:4	Main window peaking term10 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM9_SELECT[2:0]	2:0	Main window peaking term9 select.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM12_SELECT[2:0]	6:4	Main window peaking term12 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM11_SELECT[2:0]	2:0	Main window peaking term11 select.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM14_SELECT[2:0]	6:4	Main window peaking term14 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM13_SELECT[2:0]	2:0	Main window peaking term13 select.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PEAKING_TERM16_SELECT[2:0]	6:4	Main window peaking term16 select.	
	-	3	Reserved.	
	MAIN_PEAKING_TERM15_SELECT[2:0]	2:0	Main window peaking term15 select.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND1_OVERSHOOT_LIMIT[7:0]	7:0	Main window band1 overshoot limit.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND2_OVERSHOOT_LIMIT[7:0]	7:0	Main window band2 overshoot limit.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND3_OVERSHOOT_LIMIT[7:0]	7:0	Main window band3 overshoot limit.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND4_OVERSHOOT_LIMIT[7:0]	7:0	Main window band4 overshoot limit.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND5_OVERSHOOT_LIMIT[7:0]	7:0	Main window band5 overshoot limit.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND6_OVERSHOOT_LIMIT[7:0]	7:0	Main window band6 overshoot limit.	
23h	**REG102F46**	**7:0**	**Default : 0xFF**	**Access : R/W**

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BAND7_OVERSHOOT_LIMIT[7:0]	7:0	Main window band7 overshoot limit.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND8_OVERSHOOT_LIMIT[7:0]	7:0	Main window band8 overshoot limit.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND1_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band1 undershoot limit.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND2_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band2 undershoot limit.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND3_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band3 undershoot limit.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND4_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band4 undershoot limit.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND5_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band5 undershoot limit.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND6_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band6 undershoot limit.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND7_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band7 undershoot limit.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND8_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band8 undershoot limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND1_COEF[5:0]	5:0	Sub window band1 coefficient.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND2_COEF[5:0]	5:0	Sub window band2 coefficient.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND3_COEF[5:0]	5:0	Sub window band3 coefficient.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND4_COEF[5:0]	5:0	Sub window band4 coefficient.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BAND5_COEF[5:0]	5:0	Sub window band5 coefficient.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND6_COEF[5:0]	5:0	Sub window band6 coefficient.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND7_COEF[5:0]	5:0	Sub window band7 coefficient.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_BAND8_COEF[5:0]	5:0	Sub window band8 coefficient.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM2_SELECT[2:0]	6:4	Sub window peaking term2 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM1_SELECT[2:0]	2:0	Sub window peaking term1 select.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM4_SELECT[2:0]	6:4	Sub window peaking term4 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM3_SELECT[2:0]	2:0	Sub window peaking term3 select.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM6_SELECT[2:0]	6:4	Sub window peaking term6 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM5_SELECT[2:0]	2:0	Sub window peaking term5 select.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM8_SELECT[2:0]	6:4	Sub window peaking term8 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM7_SELECT[2:0]	2:0	Sub window peaking term7 select.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM10_SELECT[2:0]	6:4	Sub window peaking term10 select.	

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3	Reserved.	
	SUB_PEAKING_TERM9_SELECT[2:0]	2:0	Sub window peaking term9 select.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM12_SELECT[2:0]	6:4	Sub window peaking term12 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM11_SELECT[2:0]	2:0	Sub window peaking term11 select.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM14_SELECT[2:0]	6:4	Sub window peaking term14 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM13_SELECT[2:0]	2:0	Sub window peaking term13 select.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_PEAKING_TERM16_SELECT[2:0]	6:4	Sub window peaking term16 select.	
	-	3	Reserved.	
	SUB_PEAKING_TERM15_SELECT[2:0]	2:0	Sub window peaking term15 select.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_PEAKING_EN	7	Main window color adaptive peaking enable.	
	MAIN_COLOR_FACTOR_LPF_EN	6	Main window color factor LPF enable.	
	-	5:4	Reserved.	
	SUB_COLOR_PEAKING_EN	3	Sub window color adaptive peaking enable.	
	-	2:0	Reserved.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x33**	**Access : R/W**
	MAIN_COLOR_CORING_EN	7	Main window color adaptive coring enable.	
	-	6	Reserved.	
	MAIN_CORING_THRD_STEP[1:0]	5:4	Main window coring step.	
	SUB_COLOR_CORING_EN	3	Sub window color adaptive coring enable.	
	-	2	Reserved.	
	SUB_CORING_THRD_STEP[1:0]	1:0	Sub window coring step.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND2_CORING_THRD[3:0]	7:4	Main window band2 coring threshold.	
	MAIN_BAND1_CORING_THRD[3:0]	3:0	Main window band1 coring threshold.	

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND4_CORING_THRD[3:0]	7:4	Main window band4 coring threshold.	
	MAIN_BAND3_CORING_THRD[3:0]	3:0	Main window band3 coring threshold.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND6_CORING_THRD[3:0]	7:4	Main window band6 coring threshold.	
	MAIN_BAND5_CORING_THRD[3:0]	3:0	Main window band5 coring threshold.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_CORING_THRD[3:0]	7:4	Main window band8 coring threshold.	
	MAIN_BAND7_CORING_THRD[3:0]	3:0	Main window band7 coring threshold.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND2_CORING_THRD[3:0]	7:4	Sub window band2 coring threshold.	
	SUB_BAND1_CORING_THRD[3:0]	3:0	Sub window band1 coring threshold.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND4_CORING_THRD[3:0]	7:4	Sub window band4 coring threshold.	
	SUB_BAND3_CORING_THRD[3:0]	3:0	Sub window band3 coring threshold.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND6_CORING_THRD[3:0]	7:4	Sub window band6 coring threshold.	
	SUB_BAND5_CORING_THRD[3:0]	3:0	Sub window band5 coring threshold.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND8_CORING_THRD[3:0]	7:4	Sub window band8 coring threshold.	
	SUB_BAND7_CORING_THRD[3:0]	3:0	Sub window band7 coring threshold.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CORING_THRD_SEC[5:0]	5:0	Main window color coring limit.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CORING_THRD_SEC[5:0]	5:0	Sub window color coring limit.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_Y_V_NM_MIN_THRD[3:0]	7:4	Main window vertical Y mosquito noise remove min value threshold.	
	MAIN_Y_V_NM_MAX_THRD[3:0]	3:0	Main window vertical Y mosquito noise remove max value threshold.	
3Ah	**REG102F74**	**7:0**	**Default : 0xFF**	**Access : R/W**

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_Y_V_NM_MIN_THRD[3:0]	7:4	Sub window vertical Y mosquito noise remove min value threshold.	
	SUB_Y_V_NM_MAX_THRD[3:0]	3:0	Sub window vertical Y mosquito noise remove max value threshold.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_CR_DELAY_NUM	6	Sub window cr delay number. #0: no delay. #1: delay 1T.	
	-	5	Reserved.	
	MAIN_CR_DELAY_NUM	4	Main window cr delay number. #0: no delay. #1: delay 1T.	
	-	3:2	Reserved.	
	SUB_YC_DELAY_EN	1	Sub window yc delay enable.	
	MAIN_YC_DELAY_EN	0	Main window yc delay enable.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_CB_DELAY_NUM	6	Sub window cb delay number. #0: no delay. #1: delay 1T.	
	-	5	Reserved.	
	SUB_Y_DELAY_NUM	4	Sub window y delay number. #0: no delay. #1: delay 1T.	
	-	3	Reserved.	
	MAIN_CB_DELAY_NUM	2	Main window cb delay number. #0: no delay. #1: delay 1T.	
	-	1	Reserved.	
	MAIN_Y_DELAY_NUM	0	Main window y delay number. #0: no delay. #1: delay 1T.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_COLOR_PK_WIN1_EN	4	Sub window color adaptive win1 enable.	
	-	3:1	Reserved.	
	MAIN_COLOR_PK_WIN1_EN	0	Main window color adaptive win1 enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	COLOR_PK_WIN1_TRANSITION_STEP[1:0]	1:0	Color adaptive win1 transition step.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	COLOR_PK_WIN1_ENTRY_VALUE[3:0]	3:0	Color adaptive win1 strength.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	COLOR_PK_TEST_EN[3:0]	3:0	Color adaptive test mode enable.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CB_UP[7:0]	7:0	Color adaptive win1 cb up.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CR_UP[7:0]	7:0	Color adaptive win1 cr up.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CB_DOWN[7:0]	7:0	Color adaptive win1 cb down.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CR_DOWN[7:0]	7:0	Color adaptive win1 cr down.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_GAUSS_LUT_STEP[1:0]	5:4	Main window Gaussian SNR LUT step.	
	-	3:1	Reserved.	
	MAIN_GAUSS_NR_EN	0	Main window Gaussian SNR enable.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_GAUSS_THRD[4:0]	4:0	Main window Gaussian SNR threshold.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_GAUSS_LUT_STEP[1:0]	5:4	Sub window Gaussian SNR LUT step.	
	-	3:1	Reserved.	
	SUB_GAUSS_NR_EN	0	Sub window green Gaussian SNR bypass	

SC1 PEAKING Register (Bank = 102F, Sub-Bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			enable.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_GAUSS_THRD[4:0]	4:0	Sub window Gaussian SNR threshold.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_0[7:0]	7:0	Gaussian SNR Table 0.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_1[7:0]	7:0	Gaussian SNR Table 1.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_2[7:0]	7:0	Gaussian SNR Table 2.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_3[7:0]	7:0	Gaussian SNR Table 3.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_4[7:0]	7:0	Gaussian SNR Table 4.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_5[7:0]	7:0	Gaussian SNR Table 5.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_6[7:0]	7:0	Gaussian SNR Table 6.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_7[7:0]	7:0	Gaussian SNR Table 7.	

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 01h (102F02h ~ 102F03h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PRE_Y_GAIN_LSB[3:0]	7:4	Main window pre Y gain LSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
	MAIN_Y_GAIN_LSB[3:0]	3:0	Main window Y gain LSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PRE_Y_GAIN_LSB[3:0]	7:4	Sub window pre Y gain LSB. Pre_y_gain_new(1.10) = {pre_y_gain,pre_y_gain_lsb}.	
	SUB_Y_GAIN_LSB[3:0]	3:0	Sub window Y gain LSB. Y_gain_new(1.10) = {y_gain,y_gain_lsb}.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	UVC_DITHER_EN	7	UV compensate dither enable.	
	-	6	Reserved.	
	SUB_UVC_LOCATE	5	Sub window UV compensate reference location. //0: after ble/wle. //1: after curve fit.	
	SUB_UVC_EN	4	Sub window UV compensate enable.	
	-	3:2	Reserved.	
	MAIN_UVC_LOCATE	1	Main window UV compensate reference location. //0: after ble/wle. //1: after curve fit0.	
	MAIN_UVC_EN	0	Main window UV compensate enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximum pixel.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MAX_PIXEL[7:0]	7:0	Sub window maximum pixel.	
0Ch	**REG102F19**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_MIN_PIXEL[7:0]	7:0	Sub window minimum pixel.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_BRI_ADJUST_LSB[1:0]	1:0	Sub window Y adjust low bit.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BRI_ADJUST[7:0]	7:0	Sub window Y adjust.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_Y_GAIN[6:0]	6:0	Main window Y gain (x.xxxxxx).	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x40**	**Access : R/W**
	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_GAIN[6:0]	6:0	Sub window Y gain (x.xxxxxx).	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x40**	**Access : R/W**
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	MAIN_PRE_Y_GAIN[6:0]	6:0	Main window pre- Y gain (x.xxxxxx).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	SUB_PRE_Y_GAIN[6:0]	6:0	Sub window pre- Y gain (x.xxxxxx).	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_POST_BRI_ADJUST_LSB[1:0]	1:0	Main window post Y adjust low bit (2's complement).	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_POST_BRI_ADJUST_LSB[1:0]	1:0	Sub window post Y adjust low bit (2's complement).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_POST_BRI_ADJUST[7:0]	7:0	Main window post Y adjust.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_POST_BRI_ADJUST[7:0]	7:0	Sub window post Y adjust.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x18**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x28**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x38**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h	**REG102F64**	**7:0**	**Default : 0x48**	**Access : R/W**

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x58**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x68**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x78**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x98**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0xA8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0xC8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0xE8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_0[7:0]	7:0	Histogram report section 32_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_1[7:0]	7:0	Histogram report section 32_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.	

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[15:8]	7:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[15:8]	7:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.	
4Ah	**REG102F95**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TOTAL_32_10[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[15:8]	7:0	See description of '102FA4h'.	

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[15:8]	7:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[15:8]	7:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[15:8]	7:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[15:8]	7:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[15:8]	7:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[15:8]	7:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[15:8]	7:0	See description of '102FB4h'.	
5Bh	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TOTAL_32_27[7:0]	7:0	Histogram report section 32_27.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[15:8]	7:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[7:0]	7:0	Histogram report section 32_28.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[15:8]	7:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[7:0]	7:0	Histogram report section 32_29.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[15:8]	7:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[7:0]	7:0	Histogram report section 32_30.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[7:0]	7:0	Histogram report section 32_31.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[15:8]	7:0	See description of '102FBEh'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x60**	**Access : R/W**
	MAIN_UVC_GAIN_HIGH_LIMIT[7:0]	7:0	Main window UV compensate gain up limit (format is 4.8).	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_HIGH_LIMIT[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAIN_UVC_GAIN_LOW_LIMIT[7:0]	7:0	Main window UV compensate gain down limit (format is 4.8).	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_LOW_LIMIT[11:8]	3:0	See description of '102FCAh'.	
76h	**REG102FEC**	**7:0**	**Default : 0x08**	**Access : R/W**

SC1 DLC Register (Bank = 102F, Sub-Bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_CURVE_FIT_TABLE_N0[7:0]	7:0	Main window curve table left point.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_N0[8]	0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_16[7:0]	7:0	Main window curve table 16.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_16[8]	0	See description of '102FEEh'.	

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_FCC_FR_EN	1	Sub window FCC region 1 enable for full range.	
	MAIN_FCC_FR_EN	0	Main window FCC region 1 enable for full range.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T2_LSB[1:0]	7:6	FCC region 2 cr target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CB_T2_LSB[1:0]	5:4	FCC region 2 cb target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CR_T1_LSB[1:0]	3:2	FCC region 1 cr target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CB_T1_LSB[1:0]	1:0	FCC region 1 cb target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, FCC_FR_CB_T1_LSB}.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T4_LSB[1:0]	7:6	FCC region 4 cr target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CB_T4_LSB[1:0]	5:4	FCC region 4 cb target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CR_T3_LSB[1:0]	3:2	FCC region 3 cr target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CB_T3_LSB[1:0]	1:0	FCC region 3 cb target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T6_LSB[1:0]	7:6	FCC region 6 cr target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CB_T6_LSB[1:0]	5:4	FCC region 6 cb target for full range, LSB.	

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CR_T5_LSB[1:0]	3:2	FCC region 5 cr target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CB_T5_LSB[1:0]	1:0	FCC region 5 cb target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T8_LSB[1:0]	7:6	FCC region 8 cr target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CB_T8_LSB[1:0]	5:4	FCC region 8 cb target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CR_T7_LSB[1:0]	3:2	FCC region 7 cr target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
	FCC_FR_CB_T7_LSB[1:0]	1:0	FCC region 7 cb target for full range, LSB. Reg_fcc_fr_cb_t1 = {reg_fcc_cb_t1, reg_fcc_fr_cb_t1_lsb}.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CB_T9[7:0]	7:0	FCC region 9 cb target for full range.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_CB_T9[9:8]	1:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T9[7:0]	7:0	FCC region 9 cr target for full range.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_CR_T9[9:8]	1:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN1_CR_DOWN[7:0]	7:0	FCC region 1 target cr down distance for full range,	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
	FCC_FR_WIN1_CR_DOWN[9:8]	1:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN1_CR_UP[7:0]	7:0	FCC region 1 target cr up distance for full range.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN1_CR_UP[9:8]	1:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN1_CB_DOWN[7:0]	7:0	FCC region 1 target cb down distance for full range.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN1_CB_DOWN[9:8]	1:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN1_CB_UP[7:0]	7:0	FCC region 1 target cb up distance for full range.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN1_CB_UP[9:8]	1:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN2_CR_DOWN[7:0]	7:0	FCC region 2 target cr down distance for full range.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN2_CR_DOWN[9:8]	1:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN2_CR_UP[7:0]	7:0	FCC region 2 target cr up distance for full range.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN2_CR_UP[9:8]	1:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN2_CB_DOWN[7:0]	7:0	FCC region 2 target cb down distance for full range.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN2_CB_DOWN[9:8]	1:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN2_CB_UP[7:0]	7:0	FCC region 2 target cb up distance for full range.	

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN2_CB_UP[9:8]	1:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN3_CR_DOWN[7:0]	7:0	FCC region 3 target cr down distance for full range.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN3_CR_DOWN[9:8]	1:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN3_CR_UP[7:0]	7:0	FCC region 3 target cr up distance for full range.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN3_CR_UP[9:8]	1:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN3_CB_DOWN[7:0]	7:0	FCC region 3 target cb down distance for full range.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN3_CB_DOWN[9:8]	1:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN3_CB_UP[7:0]	7:0	FCC region 3 target cb up distance for full range.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN3_CB_UP[9:8]	1:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN4_CR_DOWN[7:0]	7:0	FCC region 4 target cr down distance for full range.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN4_CR_DOWN[9:8]	1:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN4_CR_UP[7:0]	7:0	FCC region 4 target cr up distance for full range.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN4_CR_UP[9:8]	1:0	See description of '102F84h'.	

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN4_CB_DOWN[7:0]	7:0	FCC region 4 target cb down distance for full range.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN4_CB_DOWN[9:8]	1:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN4_CB_UP[7:0]	7:0	FCC region 4 target cb up distance for full range.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN4_CB_UP[9:8]	1:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN5_CR_DOWN[7:0]	7:0	FCC region 5 target cr down distance for full range.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN5_CR_DOWN[9:8]	1:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN5_CR_UP[7:0]	7:0	FCC region 5 target cr up distance for full range.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN5_CR_UP[9:8]	1:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN5_CB_DOWN[7:0]	7:0	FCC region 5 target cb down distance for full range.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN5_CB_DOWN[9:8]	1:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN5_CB_UP[7:0]	7:0	FCC region 5 target cb up distance for full range.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN5_CB_UP[9:8]	1:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN6_CR_DOWN[7:0]	7:0	FCC region 6 target cr down distance for full range.	
49h	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:2	Reserved.	
	FCC_FR_WIN6_CR_DOWN[9:8]	1:0	See description of '102F92h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN6_CR_UP[7:0]	7:0	FCC region 6 target cr up distance for full range.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN6_CR_UP[9:8]	1:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN6_CB_DOWN[7:0]	7:0	FCC region 6 target cb down distance for full range.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN6_CB_DOWN[9:8]	1:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN6_CB_UP[7:0]	7:0	FCC region 6target cb up distance for full range.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN6_CB_UP[9:8]	1:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN7_CR_DOWN[7:0]	7:0	FCC region 7 target cr down distance for full range.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN7_CR_DOWN[9:8]	1:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN7_CR_UP[7:0]	7:0	FCC region 7 target cr up distance for full range.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN7_CR_UP[9:8]	1:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN7_CB_DOWN[7:0]	7:0	FCC region 7 target cb down distance for full range.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN7_CB_DOWN[9:8]	1:0	See description of '102FAAh'.	
56h	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
	FCC_FR_WIN7_CB_UP[7:0]	7:0	FCC region 7 target cb up distance for full range.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN7_CB_UP[9:8]	1:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN8_CR_DOWN[7:0]	7:0	FCC region 8 target cr down distance for full range.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN8_CR_DOWN[9:8]	1:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN8_CR_UP[7:0]	7:0	FCC region 8 target cr up distance for full range.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN8_CR_UP[9:8]	1:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN8_CB_DOWN[7:0]	7:0	FCC region 8 target cb down distance for full range.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN8_CB_DOWN[9:8]	1:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN8_CB_UP[7:0]	7:0	FCC region 8 target cb up distance for full range.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN8_CB_UP[9:8]	1:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN9_CR_DOWN[7:0]	7:0	FCC region 9 target cr down distance for full range.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN9_CR_DOWN[9:8]	1:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN9_CR_UP[7:0]	7:0	FCC region 9 target cr up distance for full range.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

SC1 DLC2 Register (Bank = 102F, Sub-Bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FCC_FR_WIN9_CR_UP[9:8]	1:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN9_CB_DOWN[7:0]	7:0	FCC region 9 target cb down distance for full range.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN9_CB_DOWN[9:8]	1:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN9_CB_UP[7:0]	7:0	FCC region 9 target cb up distance for full range.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN9_CB_UP[9:8]	1:0	See description of '102FBCh'.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IBC_EN	7	Main window IBC enable.	
	SUB_IBC_EN	6	Sub window IBC enable.	
	-	5:0	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR0_ADJ[5:0]	5:0	Main window IBC Y adjustment of color0.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR1_ADJ[5:0]	5:0	Main window IBC Y adjustment of color1.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR2_ADJ[5:0]	5:0	Main window IBC Y adjustment of color2.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR3_ADJ[5:0]	5:0	Main window IBC Y adjustment of color3.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR4_ADJ[5:0]	5:0	Main window IBC Y adjustment of color4.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR5_ADJ[5:0]	5:0	Main window IBC Y adjustment of color5.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR6_ADJ[5:0]	5:0	Main window IBC Y adjustment of color6.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR7_ADJ[5:0]	5:0	Main window IBC Y adjustment of color7.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR8_ADJ[5:0]	5:0	Main window IBC Y adjustment of color8.	
15h	**REG102F2B**	**7:0**	**Default : 0x20**	**Access : R/W**

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:6	Reserved.	
	MAIN_YCOLOR9_ADJ[5:0]	5:0	Main window IBC Y adjustment of color9.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR10_ADJ[5:0]	5:0	Main window IBC Y adjustment of color10.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR11_ADJ[5:0]	5:0	Main window IBC Y adjustment of color11.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR12_ADJ[5:0]	5:0	Main window IBC Y adjustment of color12.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR13_ADJ[5:0]	5:0	Main window IBC Y adjustment of color13.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR14_ADJ[5:0]	5:0	Main window IBC Y adjustment of color14.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YCOLOR15_ADJ[5:0]	5:0	Main window IBC Y adjustment of color15.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_EN	7	Main window IHC enable.	
	SUB_IHC_EN	6	Sub window IHC enable.	
	-	5:0	Reserved.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR0[6:0]	6:0	Main window IHC hue adjustment of color0.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR1[6:0]	6:0	Main window IHC hue adjustment of color1.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR2[6:0]	6:0	Main window IHC hue adjustment of color2.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR3[6:0]	6:0	Main window IHC hue adjustment of color3.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR4[6:0]	6:0	Main window IHC hue adjustment of color4.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR5[6:0]	6:0	Main window IHC hue adjustment of color5.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR6[6:0]	6:0	Main window IHC hue adjustment of color6.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR7[6:0]	6:0	Main window IHC hue adjustment of color7.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR8[6:0]	6:0	Main window IHC hue adjustment of color8.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR9[6:0]	6:0	Main window IHC hue adjustment of color9.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR10[6:0]	6:0	Main window IHC hue adjustment of color10.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR11[6:0]	6:0	Main window IHC hue adjustment of color11.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR12[6:0]	6:0	Main window IHC hue adjustment of color12.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR13[6:0]	6:0	Main window IHC hue adjustment of color13.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)

Index (Absolute)	Mnemonic	Bit	Description	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR14[6:0]	6:0	Main window IHC hue adjustment of color14.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR15[6:0]	6:0	Main window IHC hue adjustment of color15.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR0_0[6:0]	6:0	Main window IHC hue adjustment of color0 in section 0.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR1_0[6:0]	6:0	Main window IHC hue adjustment of color1 in section 0.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR2_0[6:0]	6:0	Main window IHC hue adjustment of color2 in section 0.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR3_0[6:0]	6:0	Main window IHC hue adjustment of color3 in section 0.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR4_0[6:0]	6:0	Main window IHC hue adjustment of color4 in section 0.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR5_0[6:0]	6:0	Main window IHC hue adjustment of color5 in section 0.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR6_0[6:0]	6:0	Main window IHC hue adjustment of color6 in section 0.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR7_0[6:0]	6:0	Main window IHC hue adjustment of color7 in section 0.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR8_0[6:0]	6:0	Main window IHC hue adjustment of color8 in section 0.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR9_0[6:0]	6:0	Main window IHC hue adjustment of color9 in section 0.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR10_0[6:0]	6:0	Main window IHC hue adjustment of color10 in section 0.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR11_0[6:0]	6:0	Main window IHC hue adjustment of color11 in section 0.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR12_0[6:0]	6:0	Main window IHC hue adjustment of color12 in section 0.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_HUE_USER_COLOR13_0[6:0]	6:0	Main window IHC hue adjustment of color13 in section 0.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR14_0[6:0]	6:0	Main window IHC hue adjustment of color14 in section 0.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR15_0[6:0]	6:0	Main window IHC hue adjustment of color15 in section 0.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR0_1[6:0]	6:0	Main window IHC hue adjustment of color0 in section 1.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR1_1[6:0]	6:0	Main window IHC hue adjustment of color1 in section 1.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR2_1[6:0]	6:0	Main window IHC hue adjustment of color2 in section 1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR3_1[6:0]	6:0	Main window IHC hue adjustment of color3 in section 1.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR4_1[6:0]	6:0	Main window IHC hue adjustment of color4 in section 1.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR5_1[6:0]	6:0	Main window IHC hue adjustment of color5 in section 1.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR6_1[6:0]	6:0	Main window IHC hue adjustment of color6 in section 1.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR7_1[6:0]	6:0	Main window IHC hue adjustment of color7 in section 1.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR8_1[6:0]	6:0	Main window IHC hue adjustment of color8 in section 1.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR9_1[6:0]	6:0	Main window IHC hue adjustment of color9 in section 1.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR10_1[6:0]	6:0	Main window IHC hue adjustment of color10 in section 1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR11_1[6:0]	6:0	Main window IHC hue adjustment of color11 in section 1.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR12_1[6:0]	6:0	Main window IHC hue adjustment of color12 in section 1.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR13_1[6:0]	6:0	Main window IHC hue adjustment of color13 in section 1.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_HUE_USER_COLOR14_1[6:0]	6:0	Main window IHC hue adjustment of color14 in section 1.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR15_1[6:0]	6:0	Main window IHC hue adjustment of color15 in section 1.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR0_2[6:0]	6:0	Main window IHC hue adjustment of color0 in section 2.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR1_2[6:0]	6:0	Main window IHC hue adjustment of color1 in section 2.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR2_2[6:0]	6:0	Main window IHC hue adjustment of color2 in section 2.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR3_2[6:0]	6:0	Main window IHC hue adjustment of color3 in section 2.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR4_2[6:0]	6:0	Main window IHC hue adjustment of color4 in section 2.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR5_2[6:0]	6:0	Main window IHC hue adjustment of color5 in section 2.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7	Reserved.	
	MAIN_HUE_USER_COLOR6_2[6:0]	6:0	Main window IHC hue adjustment of color6 in section 2.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR7_2[6:0]	6:0	Main window IHC hue adjustment of color7 in section 2.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR8_2[6:0]	6:0	Main window IHC hue adjustment of color8 in section 2.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR9_2[6:0]	6:0	Main window IHC hue adjustment of color9 in section 2.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR10_2[6:0]	6:0	Main window IHC hue adjustment of color10 in section 2.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR11_2[6:0]	6:0	Main window IHC hue adjustment of color11 in section 2.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR12_2[6:0]	6:0	Main window IHC hue adjustment of color12 in section 2.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR13_2[6:0]	6:0	Main window IHC hue adjustment of color13 in section 2.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_COLOR14_2[6:0]	6:0	Main window IHC hue adjustment of color14 in section 2.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_HUE_USER_COLOR15_2[6:0]	6:0	Main window IHC hue adjustment of color15 in section 2.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_Y_MODE_EN	7	Main window IHC adaptive Y mode enable.	
	SUB_IHC_Y_MODE_EN	6	Sub window IHC adaptive Y mode enable.	
	-	5:2	Reserved.	
	MAIN_IHC_Y_MODE_DIFF_COLOR_EN	1	Main window IHC adaptive Y mode in different color enable.	
	SUB_IHC_Y_MODE_DIFF_COLOR_EN	0	Sub window IHC adaptive Y mode in different color enable.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ICC_SRAM_IO_EN	0	ICC SRAM IO enable.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICC_IOADDR[7:0]	7:0	ICC io address.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	ICC_IORE	7	ICC io read enable.	
	-	6:2	Reserved.	
	ICC_IOADDR[9:8]	1:0	See description of '102FF2h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICC_IOWDATA[7:0]	7:0	ICC io write data.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICC_IOWE	7	ICC io write enable.	
	-	6:1	Reserved.	
	ICC_IOWDATA[8]	0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : RO**
	ICC_IORDATA[7:0]	7:0	ICC io read data.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	ICC_IORDATA[8]	0	See description of '102FF6h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IHC_SRAM_IO_SELECT[1:0]	2:1	IHC SRAM IO select.	

SC1 ACE3 Register (Bank = 102F, Sub-Bank = 1C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IHC_SRAM_IO_EN	0	IHC SRAM IO enable.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	IHC_IOADDR[7:0]	7:0	IHC io address.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W, WO**
	IHC_IORE	7	IHC io read enable.	
	-	6:1	Reserved.	
	IHC_IOADDR[8]	0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	IHC_IOWDATA[7:0]	7:0	IHC io write data.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	IHC_IOWE	7	IHC io write enable.	
	-	6:2	Reserved.	
	IHC_IOWDATA[9:8]	1:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : RO**
	IHC_IORDATA[7:0]	7:0	IHC io read data.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	IHC_IORDATA[9:8]	1:0	See description of '102FFEh'.	

SC1 DYN_SCL Register (Bank = 102F, Sub-Bank = 1F)

SC1 DYN_SCL Register (Bank = 102F, Sub-Bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_IDX_DEPTH[7:0]	7:0	The number of menuload data (0: disable menuload).	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_IDX_DEPTH[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_REQ_LEN[7:0]	7:0	Length of menuload DMA's request (0: disable menuload).	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_EN	7	Menuload enable.	
	-	6:3	Reserved.	
	MLOAD_REQ_LEN[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[7:0]	7:0	Base address of allocated memory for menuload.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[23:16]	7:0	See description of '102F06h'.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MLOAD_BASE_ADR[24]	0	See description of '102F06h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x01**	**Access : R/W**
	MLOAD_TRIG_DLY[7:0]	7:0	Generate MLAOD_TRIG_P from delayed line of Vsync.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0xC0**	**Access : R/W**
	SEL_MLOAD[1:0]	7:6	Select the source to trigger menuload. 0: Falling edge of VFDE. 1: Rising edge of VSync. 2: Falling edge of Vsync. 3: Delay line set by REG_MLOAD_TRIG_DLY.	
	-	5:4	Reserved.	
	MLOAD_TRIG_DLY[11:8]	3:0	See description of '102F18h'.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DS_RIU_WE	4	Enable write register through RIU.	

SC1 DYN_SCL Register (Bank = 102F, Sub-Bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:0	Reserved.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x03**	**Access : R/W, WO**
	-	7	Reserved.	
	DS_ACTIVE_CNT_CLR	6	Ds_activating xarb cnt clear pulse.	
	DS_IPS_ACTIVE_CLR	5	Ds_activating_ips clear pulse.	
	DS_IPM_ACTIVE_CLR	4	Ds_activating_ipm clear pulse.	
	DS_ACTIVE_SW_CLR_EN	3	Set ds_activating cleared by SW.	
	-	2	Reserved.	
	DS_RIU_BE[1:0]	1:0	Byte enable for DS RIU interface.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SEL_OPM_LOCK[1:0]	1:0	Select init reference signal to lock the memory read bank. 0: From initial state machine. 1: Falling edge of Vsync. 2: From TRAIN_TRIG_P. 3: From DS_LOAD_P (for dynamic scaling enabled).	

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x01**	**Access : R/W**
	PIP_DISABLE	7	Disable PIP Function.	
	-	6	Reserved.	
	SC2LB_EN	5	Enable HD side by side line buffer mode.	
	-	4:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	SW_SUB_EN	1	Enable sub window shown on the screen.	
	MAIN_EN	0	Enable main window shown on the screen.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	
	FBL_MASK_OVERLAP	5	Do not write overlapped portion of FBL channel to line buffer.	
	FBL_SEL	4	Select FBL source. #b0: Source F2 is FBL. #b1: Source F1 is FBL.	
	VBLANK_SUB	3	Fill the sub windows line buffer in vertical blanking.	
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.	
	F2_IS_SUB	1	Set main window display on the foreground.	
	MAIN_IS_TOP	0	Set second channel display in sub-window.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x70**	**Access : R/W**
	-	7	Reserved.	
	EXTRA_POS[2:0]	6:4	Enable extra request at specified region. [0] Enable at bottom B session. [1] Enable at bottom A session. [2] Enable at top session.	
	EXTRA_TH_LN[3:0]	3:0	Enable extra request for overlapping when the jumping line less than this threshold.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x07**	**Access : R/W**
	EXTRA_EN	7	Enable extra request engine.	
	VBLANK_OVL	6	Doing the extra request in vertical blanking.	
	EXTRA_Y_HALF	5	Reduce the extra_y to half.	
	-	4:3	Reserved.	

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BO_LENGTH[2:0]	2:0	Select the length of extra request. #h0: 16 pixel. #h1: 32 pixel. #h2: 64 pixel. #h3: 128 pixel. #h4: (overlap length) / 8. #h5: (overlap length) / 4. #h6: (overlap length) / 2. #h7: (overlap length).	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F2[7:0]	7:0	The starting address of f2 stored at line buffer.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F2[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F1[7:0]	7:0	The starting address of f1 stored at line buffer.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F1[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BA_RIGHT[7:0]	7:0	Extend the pixel of bottom A session at the right side.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BB_LEFT[7:0]	7:0	Extend the pixel of bottom B session at the left side.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F2[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F1[7:0]	7:0	Set the maximum request lines for first channel.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F1[11:8]	3:0	See description of '102F2Ch'.	
17h	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EXT_SUB_BORDER[3:0]	7:4	Extend the specified line in sub window to insert additional border.	
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional border.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x02**	**Access : R/W**
	EXTRA_ADV_LINE[3:0]	7:4	Advance the specified lines of extra end line (2's complement).	
	EXTRA_FETCH_LINE[3:0]	3:0	Indicate how many lines will be fetched by extra request. Minimum is 1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_F2_EN	1	Force F1 use F2's register setting.	
	ATP_EN	0	Manual tune parameter.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x38**	**Access : R/W**
	-	7	Reserved.	
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter. #0: vsync of SC_TOP. #1: delay one line of vfde.	
	SEL_DISP[1:0]	5:4	Select the trig point to start op1 engine. #h0: down_eq7. #h1: down_eq8. #h2: down_eq9. #h3: delay lines set by reg_disp_trig_dly.	
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. #h0: Falling edge of vsync. #h1: Nearly raising edge of vsync. #h2: delay line set by reg_atp_trig_dly. #h3: Manual trig by set reg_atp_en.	
	SEL_SYNC[1:0]	1:0	Select the trig point for sync to initial engine. #h0: Falling edge of vfde. #h1: Raising edge of vsync. #h2: Reserved. #h3: Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x03**	**Access : R/W**
	ATP_TRIG_DLY[7:0]	7:0	Generate train_trig_p from delayed line of vsync.	
1Ah	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	-	7:4	Reserved.	
	ATP_TRIG_DLY[11:8]	3:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x05**	**Access : R/W**
	DISP_TRIG_DLY[7:0]	7:0	Generate disp_trig_p from delayed line of vsync.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F1[7:0]	7:0	Offset line buffer position of F1 in right direction.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIN_OVERLAP_TH[7:0]	7:0	Threshold of overlapped length. Extra_eq will be disabled when overlapped length less then this threshold.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIN_OVERLAP_CNT[7:0]	7:0	Stop count between two extra requests.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xC2**	**Access : R/W**
	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. #h0: 2 pixel. #h1: 4 pixel. #h2: 8 pixel. #h3: 16 pixel.	
	DISP_START_MODE	5	Select the display line buffer start mode. #0: start at advance 1 display line. #1: start at falling edge of vsync_init.	
	DISP_LB_MODE	4	Select the trig mode. #0: Line base. #1: Fill line buffer.	
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. #h0: before 8 pixel.	

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			#h1: before 16 pixel. #h2: before 32 pixel. #h3: before 64 pixel.	
	DISP_RLN_MODE[1:0]	1:0	Select the under_run value of display level. #h0: update by hsync (not optimum performance). #h1: update when session done (may error). #h2: update when line done (reg_disp_trig_mode = 1'b0). #h3: Reserved.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_UNDER_MODE	3	Select the under_run value of display level. #0: 16'h0000. #1: 16'hffff.	
	DISP_PAT_EN	2	Enable internal pattern of op1_disp.	
	DISP_LB_WEZ	1	Disable wen of display line buffer.	
	DISP_TRIG_MODE	0	Select the trig mode. #0: Trigged by self_counter. #1: Trigged by op2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x07**	**Access : R/W**
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '102F40h'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FLAG_BB_ADR_INI	2	Status of cnt_bb_adr_ini, write 1 to switch back to hardware. #h0: Calculated by hardware. #h1: Written by software.	
	FLAG_BO_END_LN	1	Status of line_base_bot, write 1 to switch back to hardware. #h0: Calculated by hardware. #h1: Written by software.	
	-	0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BO_END_LN[7:0]	7:0	Software mode to set the line_base_bot for extra request.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SW_BO_END_LN[11:8]	3:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BB_ADR_INI[7:0]	7:0	Software mode to set the cnt_bb_adr_ini.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_BB_ADR_INI[11:8]	3:0	See description of '102F64h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	DISPLAY_UNDERRUN	0	Indicate that the display line buffer is underrun in previous frame.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line cnt of first display position.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line cnt of minimum display level occurred.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	MIN_DISP_LINE[11:8]	3:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[15:8]	7:0	See description of '102F88h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_ADR_INI[7:0]	7:0	Read SCLB_TF_ADR_INI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	SCLB_TF_ADR_INI[11:8]	3:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_ADR_INI[7:0]	7:0	Read SCLB_BB_ADR_INI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_ADR_INI[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BO_ADR_INI[7:0]	7:0	Read SCLB_BO_ADR_INI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BO_ADR_INI[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_LEN[7:0]	7:0	Read SCLB_TF_LEN.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_LEN[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BF_LEN[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_LEN[7:0]	7:0	Read SCLB_BA_LEN.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_LEN[11:8]	3:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_LEN[7:0]	7:0	Read SCLB_BB_LEN.	

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_LEN[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1A[7:0]	7:0	Read FETCH_NUM_F1A.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1A[11:8]	3:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1B[7:0]	7:0	Read FETCH_NUM_F1B.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1B[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2A[7:0]	7:0	Read FETCH_NUM_F2A.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2A[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2B[7:0]	7:0	Read FETCH_NUM_F2B.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2B[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_OFFSET_B[7:0]	7:0	Read FETCH_OFFSET_B.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_OFFSET_B[11:8]	3:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_LENGTH_RD[7:0]	7:0	Read bo_length.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_LENGTH_RD[11:8]	3:0	See description of '102FBAh'.	

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_START_LN[7:0]	7:0	Read BO_START_LN.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_START_LN[11:8]	3:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_END_LN[7:0]	7:0	Read BO_END_LN.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_END_LN[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_ADR_INI[7:0]	7:0	Read DISP_TF_ADR_INI.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_ADR_INI[11:8]	3:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_ADR_INI[7:0]	7:0	Read DISP_BB_ADR_INI.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_ADR_INI[11:8]	3:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_LEN[7:0]	7:0	Read DISP_TF_LEN.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_LEN[11:8]	3:0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 OP1_TOP Register (Bank = 102F, Sub-Bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_LEN[7:0]	7:0	Read DISP_BA_LEN.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_LEN[11:8]	3:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_LEN[7:0]	7:0	Read DISP_BB_LEN.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_LEN[11:8]	3:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPR_BB_ADR_INI[7:0]	7:0	Read HSPR_BB_ADR_INI.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	HSPR_BB_ADR_INI[11:8]	3:0	See description of '102FCEh'.	

SC1 ELA Register (Bank = 102F, Sub-Bank = 21)

SC1 ELA Register (Bank = 102F, Sub-Bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 02h (102F02h ~ 102F04h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. #1: Enable. #0: Disable.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F1	0	F1 window EODi enable. #1: Enable. #0: Disable.	
7Fh ~ 7Fh (102FFEh ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 TDDI Register (Bank = 102F, Sub-Bank = 22)

SC1 TDDI Register (Bank = 102F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x04**	**Access : R/W**
	RATIO_DIV_YCSEP_F2	7	Main window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F2[2:0]	2:0	Main window ratio divide mode when Y/C separate.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F2[2:0]	5:3	Main window ratio divide mode.	
	RATIO_MD_F2[2:0]	2:0	Main window ratio filter mode.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x80**	**Access : R/W**
	RATIO_C_INDEP_F2	7	Main window C ratio independent mode. #0: disable C ratio filter. #1: enable C ratio filter.	
	RSV_02_2_F2[2:0]	6:4	Reserved.	
	RATIO_C_MIN_F2[3:0]	3:0	Main window C minimum ratio in independent mode.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x02**	**Access : R/W**
	RSV_02_0_F2[2:0]	7:5	Reserved.	
	-	4	Reserved.	
	RSV_02_1_F2[1:0]	3:2	Reserved.	
	RATIO_C_YMAX_SEL_F2	1	Main window C ratio takes Y ratio mode. #0: Select Y ratio before SST. #1: Select Y ratio after SST.	
	RATIO_C_YMAX_DIS_F2	0	Main window C ratio takes Y ratio mode disable. #0: Enable. #1: Disable.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILM_EODIW_EN_F2	7	Main window EODi weight compensation enable in film mode.	
	-	6:0	Reserved.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PRE_MOT_OFFSET_F2[5:0]	5:0	Main Window pre-memory motion offset for motion calculation.	
08h	**REG102F11**	**7:0**	**Default : 0x08**	**Access : R/W**

SC1 TDDI Register (Bank = 102F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	PRE_MOT_GAIN_F2[3:0]	3:0	Main Window pre-memory motion gain for motion calculation.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F2[5:0]	5:0	Main Window post-memory motion offset for motion calculation.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x88**	**Access : R/W**
	POST_MOT_CGAIN_F2[3:0]	7:4	Main Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F2[3:0]	3:0	Main Window post-memory motion gain for C motion calculation.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x86**	**Access : R/W**
	POST_MOT_YMAX_EN_F2	7	Main Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F2[2:0]	2:0	Main Window history weighting.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x07**	**Access : R/W**
	RSV_STAT_0_F2[1:0]	7:6	Reserved.	
	STAT_INC_MODE_F2	5	Main window ratio statistics: ratio incremental mode.	
	STAT_SEL_C_F2	4	Main window ratio statistics: ratio selection.	
	STAT_CORE_F2[3:0]	3:0	Main window ratio statistics: coring threshold.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[7:0]	7:0	Main window ratio statistics: motion status.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[23:16]	7:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ADAPT_MED_EN_F2	7	Main window adaptive DFK enable.	
	WEGT_MED_EN_F2	6	Main window weighted DFK enable.	
	RSV_MED_0_F2	5	Reserved.	
	MED_MANUAL_EN_F2	4	Main window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F2[3:0]	3:0	Main window DFK manual weighting.	

SC1 TDDI Register (Bank = 102F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F2[4:0]	4:0	Main window weighted DFK low-frequency begin.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F2[3:0]	3:0	Main window weighted DFK low-frequency slope adjustment.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	MED_HF_BEGIN_F2[4:0]	4:0	Main window weighted DFK high-frequency begin.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F2[3:0]	3:0	Main window weighted DFK high-frequency slope adjustment.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F2[5:0]	5:0	Main window adaptive DFK motion threshold.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x13**	**Access : R/W**
	SST_EN_F2	7	Main window SST enable.	
	-	6	Reserved.	
	RSV_SST_0_F2	5	Reserved.	
	SST_MOTION_LPF_EN_F2	4	Main window SST low-pass on motion enable.	
	SST_MOTION_TH_F2[3:0]	3:0	Main window SST motion threshold.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x27**	**Access : R/W**
	RSV_SST_1_F2[1:0]	7:6	Reserved.	
	SST_ERODE_MODE_F2[1:0]	5:4	Main window SST motion area erosion mode.	
	RSV_SST_2_F2	3	Reserved.	
	SST_DILATE_MODE_F2[2:0]	2:0	Main window SST motion area dilation mode.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xDF**	**Access : R/W**
	SST_POSTLPF_EN_F2	7	Main window SST post-LPF enable.	
	SST_POSTLPF_MAX_F2	6	Main window SST post-LPF maximum function enable.	
	SST_DYNAMIC_CORE_TH_F2[5:0]	5:0	Main window SST dynamic motion coring threshold.	
19h	**REG102F33**	**7:0**	**Default : 0x85**	**Access : R/W**

SC1 TDDI Register (Bank = 102F, Sub-Bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SST_DYNAMIC_SGAIN_F2[3:0]	7:4	Main window SST dynamic motion spatial difference gain.	
	SST_DYNAMIC_TGAIN_F2[3:0]	3:0	Main window SST dynamic motion temporal difference gain.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSV_SST_3_F2[1:0]	7:6	Reserved.	
	SST_STATIC_CORE_TH_F2[5:0]	5:0	Main window SST static motion coring threshold.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x22**	**Access : R/W**
	SST_STATIC_SGAIN_F2[3:0]	7:4	Main window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F2[3:0]	3:0	Main window SST static motion temporal difference gain.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADAPT_MED_EN_F1	7	Sub window adaptive DFK enable.	
	-	6:0	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	SST_EN_F1	7	Sub window SST enable.	
	-	6:0	Reserved.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	FBASE_LVL_STATUS[1:0]	1:0	Frame-based level status.	
7Ch ~ 7Fh (102FF8h ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '102F02h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '102F06h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '102F0Ah'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '102F0Eh'.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '102F12h'.	

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '102F12h'.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode.	

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F2	7	Main window data format is 422.	
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F2	5	Main Cr_load initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.	
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.	
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.	
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F2[7:0]	7:0	Main window horizontal Y coring threshold.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x38**	**Access : R/W**
	HSP_DE_RING_G_ON_F2	7	Main window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F2[2:0]	6:4	Main window horizontal de-ringing threshold1.	
	HSP_DE_RING_TH0_F2[3:0]	3:0	Main window horizontal de-ringing threshold0.	

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x58**	**Access : R/W**
	HSP_DE_RING_RB_ON_F2	7	Main window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F2[2:0]	6:4	Main window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F2[3:0]	3:0	Main window horizontal de-ringing threshold2.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET_F2[7:0]	7:0	Main window horizontal de-ringing offset.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_OFFSET2_F2[7:0]	7:0	Main window horizontal de-ringing offset2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x38**	**Access : R/W**
	VSP_DE_RING_G_ON_F2	7	Main window vertical Y de-ringing enable.	
	VSP_DE_RING_TH1_F2[2:0]	6:4	Main window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F2[3:0]	3:0	Main window vertical de-ringing threshold0.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x58**	**Access : R/W**
	VSP_DE_RING_RB_ON_F2	7	Main window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F2[2:0]	6:4	Main window vertical de-ringing threshold3.	
	VSP_DE_RING_TH2_F2[3:0]	3:0	Main window vertical de-ringing threshold2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET_F2[7:0]	7:0	Main window vertical de-ringing offset.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_OFFSET2_F2[7:0]	7:0	Main window vertical de-ringing offset2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.	
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F2	1	Main window field polarity switch.	
	2_INIFAC_MD_F2	0	Main window two initial factors mode.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F2	7	Main window vertical 3tap scaling enable.	
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width2 LSB.	

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width0 LSB.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width0.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width1.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width0.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.	
1Ch	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DY_FACTOR_HO[7:0]	7:0	Dynamic horizontal scaling factor.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_HO[23:16]	7:0	See description of '102F38h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE[7:0]	7:0	Dynamic vertical scaling factor.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_VE[23:16]	7:0	See description of '102F3Ch'.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_SELECT	7	Dynamic scaling factor usage. 0: For main window. 1: For sub window.	
	-	6:0	Reserved.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F1	0	Sub window horizontal scaling enable.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SCALE_VE_EN_F1	0	Sub window vertical scaling enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F1	7	Sub window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F1	6	Sub window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F1	5	Sub window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F1	4	Sub window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F1[2:0]	3:1	Sub window horizontal C scaling filter mode.	

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F1	0	Sub window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F1	7	Sub window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F1	6	Sub window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F1	5	Sub window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F1	4	Sub window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F1[2:0]	3:1	Sub window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F1	0	Sub window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x80**	**Access : R/W**
	FORMAT_422_F1	7	Sub window data format is 422.	
	-	6:2	Reserved.	
	VSP_DITH_EN_F1	1	Sub window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F1	0	Sub window dithering enable for horizontal scaling process.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F1	3	Sub window vertical Y coring enable.	
	VSP_CORING_EN_C_F1	2	Sub window vertical C coring enable.	

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
	HSP_CORING_EN_Y_F1	1	Sub window horizontal Y coring enable.	
	HSP_CORING_EN_C_F1	0	Sub window horizontal C coring enable.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CRAM_RW_EN	1	C SRAM read/write enable.	
	YRAM_RW_EN	0	Y SRAM read/write enable.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RAM_R_PULSE	1	SRAM read data pulse.	
	RAM_W_PULSE	0	SRAM write data pulse.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_ADDR[7:0]	7:0	SRAM read/write address. 0: Address 0~127. 1: Address 128~255.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[7:0]	7:0	SRAM write data.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[23:16]	7:0	See description of '102F86h'.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[31:24]	7:0	See description of '102F86h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA[39:32]	7:0	See description of '102F86h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[7:0]	7:0	SRAM read data.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[23:16]	7:0	See description of '102F8Ch'.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA[31:24]	7:0	See description of '102F8Ch'.	
48h	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
	RAM_RDATA[39:32]	7:0	See description of '102F8Ch'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x41**	**Access : R/W**
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.	
	FACTOR_MANUAL	6	Vertical factor manual mode.	
	VDOWN_SEL	5	Vertical scaling down selection. 0: Bottom. 1: Top.	
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.	
	-	3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.	
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish. 1: DE end.	
	-	6:0	Reserved.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x08**	**Access : R/W**
	3DLR_SIDE2LINE_EN	7	3D LR side-by-side to line-to-line enable.	
	-	6:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x40**	**Access : R/W**
	CTI_STEP_F2[2:0]	7:5	Main window CTI step.	
	-	4:3	Reserved.	
	CTI_LPF_COEF_F2[2:0]	2:0	Main window CTI LPF coefficients.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F2	7	Main window CTI enable.	
	-	6:0	Reserved.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F2[3:0]	3:0	Main window CTI mutual threshold.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F2[2:0]	2:0	Main window CTI mutual step.	

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F2[1:0]	1:0	Main window CTI patch mode. 0: None. 1: Trans. 2: Clfp/wts. 3: Both.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F2[4:0]	4:0	Main window CTI mutual level patch threshold.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x28**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F2[5:0]	5:0	Main window CTI mutual trans level slope gain.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F2[4:0]	4:0	Main window CTI mutual C low freq threshold.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F2[5:0]	5:0	Main window CTI mutual C low freq slope gain.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_CLFP_STEP_F2[1:0]	1:0	Main window CTI mutual C low freq step.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_LPF_COEF_F1[2:0]	2:0	Sub window CTI LPF coefficients.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F1	7	Sub window CTI enable.	
	-	6:0	Reserved.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EXTRA_FACTOR_EN	0	Extra horizontal initial factor enable.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_1[7:0]	7:0	Extra horizontal initial factor 1.	
78h	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 HVSP Register (Bank = 102F, Sub-Bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EXTRA_INI_FACTOR_HO_2[7:0]	7:0	Extra horizontal initial factor 2.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_3[7:0]	7:0	Extra horizontal initial factor 3.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_4[7:0]	7:0	Extra horizontal initial factor 4.	

SC1 PAFRC Register (Bank = 102F, Sub-Bank = 24)

SC1 PAFRC Register (Bank = 102F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x0A**	**Access : R/W**
	-	7:6	Reserved.	
	POL_TYPE	5	Pol type setting.	
	PAFRC_TAIL_CUT	4	Pafrc tail cut function. 0: Lsb use ori lsb. 1: Lsb use 0tailcut enable.	
	NOISE_DITH_DISABLE	3	PAFRC mixed with noise dither disable. 0: Enable. 1: Disable.	
	DITH_BITS	2	Dithering bits. 0: 2-bits. 1: 4-bits.	
	TCON_OFF_EN	1	Tcon frc_gamma function off signal enable. 1: Gamma/dither function turn off by tcon frc_gamma_offTCON FRC_GAMMA function off signal enable.	
	FRC_ON	0	PAFRC enable.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x23**	**Access : R/W**
	BOX_ROTATE_EN	7	Box A/B/C/D relation rotation enable.	
	TOP_BOX_UNIT_FLAG[1:0]	6:5	Top box A/B/C/D swap flag. 00: Per 2x2 box. 01: Per 4x4 box. 1x: Per 8x8 box.	
	TOP_BOX_FREEZE	4	Top box freeze.	
	TOP_BOX_SHRINK	3	Top box shrink to 2x2 from 4x4.	
	FR_C2_BIT	2	Top box frame rotation step bit location for codexx10. 0: Bit[0]. 1: Bit[1].	
	C2X2_ROT_B_DIR_S	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_B_DIR_S	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
40h	**REG102F81**	**7:0**	**Default : 0x20**	**Access : R/W**

SC1 PAFRC Register (Bank = 102F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7	Reserved.	
	G_V_SWAP	6	Green channel vertical swap, avoid polarity not consistent.	
	G_H_SWAP	5	Green channel horizontal swap, avoid polarity not consistent.	
	B_D_SWAP	4	Blue channel diagonal swap.	
	BOX_FR_SW	3	FRAME_CNT bit [1:0] swap for box rotate.	
	BOX4X4_FR_SW	2	FRAME_CNT bit [1:0] swap for box4x4 rotate.	
	BOX8X8_ROT_UNIT	1	0: Rotate step under per A, B, C or D. 1: Rotate step between A/B/C/D.	
	BOX_FREEZE	0	Box local rotation freeze.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0xF3**	**Access : R/W**
	C2X2_ROT_G_DIR	7	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_G_DIR	6	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_G_DIR_S	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_G_DIR_S	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	A2X2_ROT_B_DIR	3	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_B_DIR	2	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_B_DIR	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_B_DIR	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
41h	**REG102F83**	**7:0**	**Default : 0x3C**	**Access : R/W**

SC1 PAFRC Register (Bank = 102F, Sub-Bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
	A2X2_ROT_R_DIR	7	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_R_DIR	6	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_R_DIR	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_R_DIR	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_R_DIR_S	3	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_R_DIR_S	2	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	A2X2_ROT_G_DIR	1	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_G_DIR	0	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0xC9**	**Access : R/W**
	TOP_BOX_FR_SEQ2[7:0]	7:0	Top box frame 2nd 4 frame rotation step.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x9C**	**Access : R/W**
	TOP_BOX_FR_SEQ1[7:0]	7:0	Top box frame 1st 4 frame rotation step.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0xC9**	**Access : R/W**
	TOP_BOX_FR_SEQ4[7:0]	7:0	Top box frame 4th 4 frame rotation step.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x9C**	**Access : R/W**
	TOP_BOX_FR_SEQ3[7:0]	7:0	Top box frame 3rd 4 frame rotation step.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0xAA**	**Access : R/W**
	TOP_BOX_FR_C2_SEQ34[7:0]	7:0	Top box frame 3rd/4th 4 frame rotation step for codexx10.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0xAA**	**Access : R/W**
	TOP_BOX_FR_C2_SEQ12[7:0]	7:0	Top box frame 1st/2nd 4 frame rotation step for codexx10.	

SC1 PAFRC Register (Bank = 102F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x50**	**Access : R/W**
	BOX_A_ROT_DIR	7	Location A frame counter direction. 0: Counterwise. 1: Back.	
	BOX_B_ROT_DIR	6	Location B frame counter direction. 0: Counterwise. 1: Back.	
	BOX_C_ROT_DIR	5	Location C frame counter direction. 0: Counterwise. 1: Back.	
	BOX_D_ROT_DIR	4	Location D frame counter direction. 0: Counterwise. 1: Back.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x22**	**Access : R/W**
	BOX8X8_ROT_00[1:0]	7:6	Box8x8 entity 00 rotation step by reference.	
	BOX8X8_ROT_01[1:0]	5:4	Box8x8 entity 01 rotation step by reference.	
	BOX8X8_ROT_11[1:0]	3:2	Box8x8 entity 11 rotation step by reference.	
	BOX8X8_ROT_10[1:0]	1:0	Box8x8 entity 10 rotation step by reference.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0xD8**	**Access : R/W**
	B_LU_00[1:0]	7:6	B 2x2 block left up entity.	
	B_RU_01[1:0]	5:4	B 2x2 block right up entity.	
	B_RD_11[1:0]	3:2	B 2x2 block right down entity.	
	B_LD_10[1:0]	1:0	B 2x2 block left down entity.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	A_LU_00[1:0]	7:6	A 2x2 block left up entity.	
	A_RU_01[1:0]	5:4	A 2x2 block right up entity.	
	A_RD_11[1:0]	3:2	A 2x2 block right down entity.	
	A_LD_10[1:0]	1:0	A 2x2 block left down entity.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x72**	**Access : R/W**
	D_LU_00[1:0]	7:6	D 2x2 block left up entity.	
	D_RU_01[1:0]	5:4	D 2x2 block right up entity.	
	D_RD_11[1:0]	3:2	D 2x2 block right down entity.	
	D_LD_10[1:0]	1:0	D 2x2 block left down entity.	

SC1 PAFRC Register (Bank = 102F, Sub-Bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x72**	**Access : R/W**
	C_LU_00[1:0]	7:6	C 2x2 block left up entity.	
	C_RU_01[1:0]	5:4	C 2x2 block right up entity.	
	C_RD_11[1:0]	3:2	C 2x2 block right down entity.	
	C_LD_10[1:0]	1:0	C 2x2 block left down entity.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x8D**	**Access : R/W**
	D_LU_00_S[1:0]	7:6	D 2x2 block left up entity, 2nd.	
	D_RU_01_S[1:0]	5:4	D 2x2 block right up entity, 2nd.	
	D_RD_11_S[1:0]	3:2	D 2x2 block right down entity, 2nd.	
	D_LD_10_S[1:0]	1:0	D 2x2 block left down entity, 2nd.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x8D**	**Access : R/W**
	C_LU_00_S[1:0]	7:6	C 2x2 block left up entity, 2nd.	
	C_RU_01_S[1:0]	5:4	C 2x2 block right up entity, 2nd.	
	C_RD_11_S[1:0]	3:2	C 2x2 block right down entity, 2nd.	
	C_LD_10_S[1:0]	1:0	C 2x2 block left down entity, 2nd.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x27**	**Access : R/W**
	BOX_B_LU_00[1:0]	7:6	Location B block A LSB 2 bits plus value.	
	BOX_B_RU_01[1:0]	5:4	Location B block B LSB 2 bits plus value.	
	BOX_B_RD_11[1:0]	3:2	Location B block C LSB 2 bits plus value.	
	BOX_B_LD_10[1:0]	1:0	Location B block D LSB 2 bits plus value.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0xD8**	**Access : R/W**
	BOX_A_LU_00[1:0]	7:6	Location A block A LSB 2 bits plus value.	
	BOX_A_RU_01[1:0]	5:4	Location A block B LSB 2 bits plus value.	
	BOX_A_RD_11[1:0]	3:2	Location A block C LSB 2 bits plus value.	
	BOX_A_LD_10[1:0]	1:0	Location A block D LSB 2 bits plus value.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x72**	**Access : R/W**
	BOX_D_LU_00[1:0]	7:6	Location D block A LSB 2 bits plus value.	
	BOX_D_RU_01[1:0]	5:4	Location D block B LSB 2 bits plus value.	
	BOX_D_RD_11[1:0]	3:2	Location D block C LSB 2 bits plus value.	
	BOX_D_LD_10[1:0]	1:0	Location D block D LSB 2 bits plus value.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x8D**	**Access : R/W**
	BOX_C_LU_00[1:0]	7:6	Location C block A LSB 2 bits plus value.	
	BOX_C_RU_01[1:0]	5:4	Location C block B LSB 2 bits plus value.	

SC1 PAFRC Register (Bank = 102F, Sub-Bank = 24)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	BOX_C_RD_11[1:0]	3:2	Location C block C LSB 2 bits plus value.
	BOX_C_LD_10[1:0]	1:0	Location C block D LSB 2 bits plus value.

SC1 XV_YCC Register (Bank = 102F, Sub-Bank = 25)

SC1 XV_YCC Register (Bank = 102F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	-	3:0	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	
	POST_SUB_BRI_EN	4	Sub window post brightness enable.	
	-	3:0	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post r channel offset.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post g channel offset.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post b channel offset.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post r channel gain.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F48h'.	

SC1 XV_YCC Register (Bank = 102F, Sub-Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post g channel gain.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_CON_GAIN[7:0]	7:0	Main window post b channel gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_BRI_OFFSET[7:0]	7:0	Sub window post r channel offset.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_BRI_OFFSET[7:0]	7:0	Sub window post g channel offset.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_BRI_OFFSET[7:0]	7:0	Sub window post b channel offset.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post r channel gain.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[11:8]	3:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post g channel gain.	
2Bh	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 XV_YCC Register (Bank = 102F, Sub-Bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_CON_GAIN[7:0]	7:0	Sub window post b channel gain.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[11:8]	3:0	See description of '102F58h'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PG_OSD_SEL	5	OSD mux with pattern gen output. 1: Select OSD output. 0: Select pattern gen output.	
	-	4:0	Reserved.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	BIST_FAIL_XV_YCC_FIX_GAMMA_SRAM [5:0]	5:0	Xvycc fix gamma SRAM BIST fail report.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	BIST_FAIL_XV_YCC_DE_GAMMA_SRAM[2:0]	2:0	Xvycc de gamma SRAM BIST fail report.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BT601_YC422_OP_CH_SEL	0		
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_GAT_BW_EN	7	Xvycc programmable gamma table burst write enable.	
	XVYCC_GATCS[1:0]	6:5	Xvycc programmable gamma table channel select: 00: Select R Channel. 01: Select G Channel. 10: Select B Channel. 11: Select All Channel when write; reserved for read.	
	XVYCC_GAT_RD_EN	4	Xvycc programmable gamma table read	

SC1 XV_YCC Register (Bank = 102F, Sub-Bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
			enable: will hardware clear to 0 after read back.	
	XVYCC_GAT_WR_EN	3	Xvycc programmable gamma table write enable: will hardware clear to 0 after write.	
	-	2:0	Reserved.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:3	Reserved.	
	XVYCC_GAT_MAX_EN	2	Xvycc programmable gamma table max data enable.	
	XVYCC_GAT_BW_FLAG	1	Xvycc programmable gamma table burst write status when burst write enable.	
	-	0	Reserved.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_GAT_ADR[7:0]	7:0	Xvycc programmable gamma table address port.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_GAT_DATA[7:0]	7:0	Xvycc programmable gamma table write data port.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XVYCC_GAT_DATA[11:8]	3:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_GAT_MAX_DATA[7:0]	7:0	Xvycc programmable gamma table max data.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	XVYCC_GAT_MAX_DATA[11:8]	3:0	See description of '102FF6h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : RO**
	XVYCC_GAT_RD_DATA[7:0]	7:0	Xvycc programmable gamma table read data port.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	XVYCC_GAT_RD_DATA[11:8]	3:0	See description of '102FFAh'.	

SC1 DMS Register (Bank = 102F, Sub-Bank = 26)

SC1 DMS Register (Bank = 102F, Sub-Bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DMS_ALPHA_LPF_EN_F2	1	Alpha low pass filter enable F2.	
	DMS_EN_F2	0	Mosquito noise reduction enable F2.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMS_STRENGTH_F2[4:0]	4:0	Mosquito noise reduction strength F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_LOW_THRD_HOR_F2[7:0]	7:0	Horizontal std low threshold F2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_LOW_THRD_CEN_F2[7:0]	7:0	Center std low threshold F2.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DMS_ALPHA_LPF_EN_F1	1	Alpha low pass filter enable F1.	
	DMS_EN_F1	0	Mosquito noise reduction enable F1.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DMS_STRENGTH_F1[4:0]	4:0	Mosquito noise reduction strength F1.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_LOW_THRD_HOR_F1[7:0]	7:0	Horizontal std low threshold F1.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	LUT_STEP_HOR_F1[1:0]	1:0	Horizontal look-up-table step F1.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_LOW_THRD_CEN_F1[7:0]	7:0	Horizontal Center std low threshold F1.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	LUT_STEP_CEN_F1[2:0]	2:0	Horizontal Center look-up-table step F1.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x44**	**Access : R/W**
	-	7:6	Reserved.	
	V_C_LPF_EN_F1	5	Vertical C Low Pass Filter Enable F1.	
	SPIKE_NR_EN_F1	4	Spike NR Enable F1.	

SC1 DMS Register (Bank = 102F, Sub-Bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SPIKE_NR_MR_EN	3	Spike NR motion ratio enable.	
	-	2	Reserved.	
	V_C_LPF_EN_F2	1	Vertical C Low Pass Filter Enable F2.	
	SPIKE_NR_EN_F2	0	Spike NR Enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SPIKE_NR_COEF[3:0]	3:0	Spike NR Coefficient.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	P_THRD_1[4:0]	4:0	Spike NR P threshold 1.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_THRD_2[7:0]	7:0	Spike NR P threshold 2.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_THRD_3[7:0]	7:0	Spike NR P threshold 3.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	D_31_STEP[2:0]	6:4	Spike NR D31 Step.	
	-	3	Reserved.	
	D_11_21_STEP[2:0]	2:0	Spike NR D11_21 Step.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	YP_22_STEP[2:0]	2:0	Spike NR YP22 Step.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPK_MR_LPF_EN_F1	4	Spike NR motion ratio low pass filter enable F1 (lpf is 3x3 mask).	
	-	3:1	Reserved.	
	SPK_MR_LPF_EN_F2	0	Spike NR motion ratio low pass filter enable F2 (lpf is 3x3 mask).	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_0[7:0]	7:0	Spike NR motion ratio look-up-table 0.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x32**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_1[7:0]	7:0	Spike NR motion ratio look-up-table 1.	

SC1 DMS Register (Bank = 102F, Sub-Bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x54**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_2[7:0]	7:0	Spike NR motion ratio look-up-table 2.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x76**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_3[7:0]	7:0	Spike NR motion ratio look-up-table 3.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x98**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_4[7:0]	7:0	Spike NR motion ratio look-up-table 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_5[7:0]	7:0	Spike NR motion ratio look-up-table 5.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_6[7:0]	7:0	Spike NR motion ratio look-up-table 6.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_7[7:0]	7:0	Spike NR motion ratio look-up-table 7.	

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CURVE_FIT_CF_LPF_EN	5	Sub window color factor low pass filter enable for luma curve [1 2 1].	
	SUB_COLOR_CURVE_FIT_EN	4	Sub window color adaptive enable for luma curve.	
	-	3:2	Reserved.	
	MAIN_CURVE_FIT_CF_LPF_EN	1	Main window color factor low pass filter enable for luma curve [1 2 1].	
	MAIN_COLOR_CURVE_FIT_EN	0	Main window color adaptive enable for luma curve.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G0_SELECT_CF[7:0]	7:0	Main window color selection for luma curve of Color Group 0.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G0_SELECT_CF[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G1_SELECT_CF[7:0]	7:0	Main window color selection for luma curve of Color Group 1.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G1_SELECT_CF[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G2_SELECT_CF[7:0]	7:0	Main window color selection for luma curve of Color Group 2.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G2_SELECT_CF[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G3_SELECT_CF[7:0]	7:0	Main window color selection for luma curve of Color Group 3.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G3_SELECT_CF[15:8]	7:0	See description of '102F10h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_COLOR_G1_STRENGTH_CF[3:0]	7:4	Main window color adaptive for luma curve of Color Group 1.	
	MAIN_COLOR_G0_STRENGTH_CF[3:0]	3:0	Main window color adaptive for luma curve of Color	

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Group 0.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_COLOR_G3_STRENGTH_CF[3:0]	7:4	Main window color adaptive for luma curve of Color Group 3.	
	MAIN_COLOR_G2_STRENGTH_CF[3:0]	3:0	Main window color adaptive for luma curve of Color Group 2.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G0_SELECT_PK[7:0]	7:0	Main window color selection for peaking of Color Group 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G0_SELECT_PK[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G1_SELECT_PK[7:0]	7:0	Main window color selection for peaking of Color Group 1.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G1_SELECT_PK[15:8]	7:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G2_SELECT_PK[7:0]	7:0	Main window color selection for peaking of Color Group 2.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G2_SELECT_PK[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G3_SELECT_PK[7:0]	7:0	Main window color selection for peaking of Color Group 3.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_G3_SELECT_PK[15:8]	7:0	See description of '102F26h'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_COLOR_G1_STRENGTH_PK[3:0]	7:4	Main window color adaptive for peaking of Color Group 1.	
	MAIN_COLOR_G0_STRENGTH_PK[3:0]	3:0	Main window color adaptive for peaking of Color Group 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_COLOR_G3_STRENGTH_PK[3:0]	7:4	Main window color adaptive for peaking of Color Group 3.	

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_COLOR_G2_STRENGTH_PK[3:0]	3:0	Main window color adaptive for peaking of Color Group 2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_CTI_EN	4	Sub window CTI enable.	
	-	3:1	Reserved.	
	MAIN_CTI_EN	0	Main window CTI enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CTI_STEP[1:0]	5:4	Main window CTI step.	
	-	3:0	Reserved.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CTI_CORING_THRD[3:0]	3:0	Main window CTI coring threshold.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CTI_BAND_COEF[5:0]	5:0	Main window CTI band pass filter coefficient.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CTI_STEP[1:0]	5:4	Sub window CTI step.	
	-	3:0	Reserved.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_CTI_CORING_THRD[3:0]	3:0	Sub window CTI coring threshold.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CTI_BAND_COEF[5:0]	5:0	Sub window CTI band pass filter coefficient.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CTI_GRAY_THRD[3:0]	3:0	Main window CTI grap patch threshold.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_CTI_GRAY_THRD[3:0]	3:0	Sub window CTI grap patch threshold.	

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR0_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color0.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR0_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color0.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR0_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color0.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR0_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color0.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR1_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color1.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR1_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color1.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR1_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color1.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR1_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color1.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR2_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color2.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR2_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color2.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR2_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color2.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR2_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for	

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			color2.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR3_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color3.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR3_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color3.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR3_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color3.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR3_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color3.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR4_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color4.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR4_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color4.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR4_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color4.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR4_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color4.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR5_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color5.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR5_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color5.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR5_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color5.	
33h	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_IHC_ICC_COLOR5_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color5.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR6_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color6.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR6_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color6.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR6_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color6.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR6_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color6.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR7_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color7.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR7_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color7.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR7_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color7.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR7_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color7.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR8_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color8.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR8_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color8.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR8_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color8.	

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR8_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color8.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR9_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color9.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR9_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color9.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR9_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color9.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR9_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color9.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR10_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color10.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR10_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color10.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR10_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color10.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR10_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color10.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR11_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color11.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR11_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color11.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR11_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for	

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			color11.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR11_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color11.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR12_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color12.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR12_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color12.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR12_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color12.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR12_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color12.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR13_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color13.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR13_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color13.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR13_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color13.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR13_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color13.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR14_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color14.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR14_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color14.	
55h	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 ACE2 Register (Bank = 102F, Sub-Bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_IHC_ICC_COLOR14_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color14.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR14_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color14.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR15_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for color15.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR15_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for color15.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR15_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for color15.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_COLOR15_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for color15.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VIP_FUN_BYPASS_EN	0	Vip all function bypass enable.	
7Dh ~ 7Dh (102FFAh ~ 102FFBh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 MCNR Register (Bank = 102F, Sub-Bank = 2A)

SC1 MCNR Register (Bank = 102F, Sub-Bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h ~ 02h (102F04h ~ 102F05h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MED_AUTO	7	Median auto.	
	MED_EN	6	Median enable.	
	SNR_EN_F2	5	SNR enable.	
	PATCH_W4_EN	4	Patch w4 enable.	
	PATCH_W3_EN	3	Patch w3 enable.	
	PATCH_W2_EN	2	Patch w2 enable.	
	MCDI_FILM_EN	1	Film act use MCDi data.	
	MCNR_EN_F2	0	Mcnr enable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	NR_EN_F2	7	Nr enable.	
	PDNR_EN_F2	6	Pdnr enable.	
	RANDOM_MOTION_CHECK_DIFF	5	Random motion check diff enable.	
	RANDOM_MOTION_EN	4	Random motion enable.	
	DITHER_EN	3	Dither enable.	
	KEEP_DETAIL_EN	2	Keep detail enable.	
	FAVOR_MV0_EN	1	Favor mv0 enable.	
	C_PDNR_EN_F2	0	Pdnr c enable.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0xEE**	**Access : R/W**
	NR_LUT_2[7:4]	7:4	Nr look up table 2.	
	NR_LUT_3[3:0]	3:0	Nr look up table 3.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0xFF**	**Access : R/W**
	NR_LUT_0[15:12]	7:4	Nr look up table 0.	
	NR_LUT_1[11:8]	3:0	Nr look up table 1.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0xCC**	**Access : R/W**
	NR_LUT_6[7:4]	7:4	Nr look up table 6.	
	NR_LUT_7[3:0]	3:0	Nr look up table 7.	
09h	**REG102F13**	**7:0**	**Default : 0xDD**	**Access : R/W**

SC1 MCNR Register (Bank = 102F, Sub-Bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NR_LUT_4[15:12]	7:4	Nr look up table 4.	
	NR_LUT_5[11:8]	3:0	Nr look up table 5.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0xAA**	**Access : R/W**
	NR_LUT_10[7:4]	7:4	Nr look up table 10.	
	NR_LUT_11[3:0]	3:0	Nr look up table 11.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0xBB**	**Access : R/W**
	NR_LUT_8[15:12]	7:4	Nr look up table 8.	
	NR_LUT_9[11:8]	3:0	Nr look up table 9.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x88**	**Access : R/W**
	NR_LUT_14[7:4]	7:4	Nr look up table 14.	
	NR_LUT_15[3:0]	3:0	Nr look up table 15.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x99**	**Access : R/W**
	NR_LUT_12[15:12]	7:4	Nr look up table 12.	
	NR_LUT_13[11:8]	3:0	Nr look up table 13.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x66**	**Access : R/W**
	NR_LUT_18[7:4]	7:4	Nr look up table 18.	
	NR_LUT_19[3:0]	3:0	Nr look up table 19.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x77**	**Access : R/W**
	NR_LUT_16[15:12]	7:4	Nr look up table 16.	
	NR_LUT_17[11:8]	3:0	Nr look up table 17.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x44**	**Access : R/W**
	NR_LUT_22[7:4]	7:4	Nr look up table 22.	
	NR_LUT_23[3:0]	3:0	Nr look up table 23.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x55**	**Access : R/W**
	NR_LUT_20[15:12]	7:4	Nr look up table 20.	
	NR_LUT_21[11:8]	3:0	Nr look up table 21.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x22**	**Access : R/W**
	NR_LUT_26[7:4]	7:4	Nr look up table 26.	
	NR_LUT_27[3:0]	3:0	Nr look up table 27.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x33**	**Access : R/W**
	NR_LUT_24[15:12]	7:4	Nr look up table 24.	
	NR_LUT_25[11:8]	3:0	Nr look up table 25.	
0Fh	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 MCNR Register (Bank = 102F, Sub-Bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NR_LUT_30[7:4]	7:4	Nr look up table 30.	
	NR_LUT_31[3:0]	3:0	Nr look up table 31.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x11**	**Access : R/W**
	NR_LUT_28[15:12]	7:4	Nr look up table 28.	
	NR_LUT_29[11:8]	3:0	Nr look up table 29.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x88**	**Access : R/W**
	PDNR_LOW_LUT_2[7:4]	7:4	Pdnr low look up table 2.	
	PDNR_LOW_LUT_3[3:0]	3:0	Pdnr low look up table 3.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x88**	**Access : R/W**
	PDNR_LOW_LUT_0[15:12]	7:4	Pdnr low look up table 0.	
	PDNR_LOW_LUT_1[11:8]	3:0	Pdnr low look up table 1.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_6[7:4]	7:4	Pdnr low look up table 6.	
	PDNR_LOW_LUT_7[3:0]	3:0	Pdnr low look up table 7.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x51**	**Access : R/W**
	PDNR_LOW_LUT_4[15:12]	7:4	Pdnr low look up table 4.	
	PDNR_LOW_LUT_5[11:8]	3:0	Pdnr low look up table 5.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_10[7:4]	7:4	Pdnr low look up table 10.	
	PDNR_LOW_LUT_11[3:0]	3:0	Pdnr low look up table 11.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_8[15:12]	7:4	Pdnr low look up table 8.	
	PDNR_LOW_LUT_9[11:8]	3:0	Pdnr low look up table 9.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_14[7:4]	7:4	Pdnr low look up table 14.	
	PDNR_LOW_LUT_15[3:0]	3:0	Pdnr low look up table 15.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_12[15:12]	7:4	Pdnr low look up table 12.	
	PDNR_LOW_LUT_13[11:8]	3:0	Pdnr low look up table 13.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0xDC**	**Access : R/W**
	PDNR_HIGH_LUT_2[7:4]	7:4	Pdnr high look up table 2.	
	PDNR_HIGH_LUT_3[3:0]	3:0	Pdnr high look up table 3.	
24h	**REG102F49**	**7:0**	**Default : 0xFE**	**Access : R/W**

SC1 MCNR Register (Bank = 102F, Sub-Bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PDNR_HIGH_LUT_0[15:12]	7:4	Pdnr high look up table 0.	
	PDNR_HIGH_LUT_1[11:8]	3:0	Pdnr high look up table 1.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x98**	**Access : R/W**
	PDNR_HIGH_LUT_6[7:4]	7:4	Pdnr high look up table 6.	
	PDNR_HIGH_LUT_7[3:0]	3:0	Pdnr high look up table 7.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0xBA**	**Access : R/W**
	PDNR_HIGH_LUT_4[15:12]	7:4	Pdnr high look up table 4.	
	PDNR_HIGH_LUT_5[11:8]	3:0	Pdnr high look up table 5.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x54**	**Access : R/W**
	PDNR_HIGH_LUT_10[7:4]	7:4	Pdnr high look up table 10.	
	PDNR_HIGH_LUT_11[3:0]	3:0	Pdnr high look up table 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x76**	**Access : R/W**
	PDNR_HIGH_LUT_8[15:12]	7:4	Pdnr high look up table 8.	
	PDNR_HIGH_LUT_9[11:8]	3:0	Pdnr high look up table 9.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x10**	**Access : R/W**
	PDNR_HIGH_LUT_14[7:4]	7:4	Pdnr high look up table 14.	
	PDNR_HIGH_LUT_15[3:0]	3:0	Pdnr high look up table 15.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x32**	**Access : R/W**
	PDNR_HIGH_LUT_12[15:12]	7:4	Pdnr high look up table 12.	
	PDNR_HIGH_LUT_13[11:8]	3:0	Pdnr high look up table 13.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x88**	**Access : R/W**
	PDNR_C_LUT_2[7:4]	7:4	Pdnr c look up table 2.	
	PDNR_C_LUT_3[3:0]	3:0	Pdnr c look up table 3.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x88**	**Access : R/W**
	PDNR_C_LUT_0[15:12]	7:4	Pdnr c look up table 0.	
	PDNR_C_LUT_1[11:8]	3:0	Pdnr c look up table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_6[7:4]	7:4	Pdnr c look up table 6.	
	PDNR_C_LUT_7[3:0]	3:0	Pdnr c look up table 7.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x51**	**Access : R/W**
	PDNR_C_LUT_4[15:12]	7:4	Pdnr c look up table 4.	
	PDNR_C_LUT_5[11:8]	3:0	Pdnr c look up table 5.	
32h	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 MCNR Register (Bank = 102F, Sub-Bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PDNR_C_LUT_10[7:4]	7:4	Pdnr c look up table 10.	
	PDNR_C_LUT_11[3:0]	3:0	Pdnr c look up table 11.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_8[15:12]	7:4	Pdnr c look up table 8.	
	PDNR_C_LUT_9[11:8]	3:0	Pdnr c look up table 9.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_14[7:4]	7:4	Pdnr c look up table 14.	
	PDNR_C_LUT_15[3:0]	3:0	Pdnr c look up table 15.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_12[15:12]	7:4	Pdnr c look up table 12.	
	PDNR_C_LUT_13[11:8]	3:0	Pdnr c look up table 13.	
77h ~ 7Fh (102FEEh ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_SA_USER_COLOR0_0[3:0]	3:0	Main window ICC saturation adjustment of color0 in section 0.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_SA_USER_COLOR1_0[3:0]	3:0	Main window ICC saturation adjustment of color1 in section 0.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_SA_USER_COLOR2_0[3:0]	3:0	Main window ICC saturation adjustment of color2 in section 0.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_SA_USER_COLOR3_0[3:0]	3:0	Main window ICC saturation adjustment of color3 in section 0.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_SA_USER_COLOR4_0[3:0]	3:0	Main window ICC saturation adjustment of color4 in section 0.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_SA_USER_COLOR5_0[3:0]	3:0	Main window ICC saturation adjustment of color5 in section 0.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_SA_USER_COLOR6_0[3:0]	3:0	Main window ICC saturation adjustment of color6 in section 0.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x08**	**Access : R/W**
	_	7:4	Reserved.	
	MAIN_SA_USER_COLOR7_0[3:0]	3:0	Main window ICC saturation adjustment of color7 in section 0.	
3Ch	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR8_0[3:0]	3:0	Main window ICC saturation adjustment of color8 in section 0.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR9_0[3:0]	3:0	Main window ICC saturation adjustment of color9 in section 0.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR10_0[3:0]	3:0	Main window ICC saturation adjustment of color10 in section 0.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR11_0[3:0]	3:0	Main window ICC saturation adjustment of color11 in section 0.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR12_0[3:0]	3:0	Main window ICC saturation adjustment of color12 in section 0.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR13_0[3:0]	3:0	Main window ICC saturation adjustment of color13 in section 0.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR14_0[3:0]	3:0	Main window ICC saturation adjustment of color14 in section 0.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR15_0[3:0]	3:0	Main window ICC saturation adjustment of color15 in section 0.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR0_1[3:0]	3:0	Main window ICC saturation adjustment of color0 in	

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			section 1.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR1_1[3:0]	3:0	Main window ICC saturation adjustment of color1 in section 1.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR2_1[3:0]	3:0	Main window ICC saturation adjustment of color2 in section 1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR3_1[3:0]	3:0	Main window ICC saturation adjustment of color3 in section 1.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR4_1[3:0]	3:0	Main window ICC saturation adjustment of color4 in section 1.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR5_1[3:0]	3:0	Main window ICC saturation adjustment of color5 in section 1.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR6_1[3:0]	3:0	Main window ICC saturation adjustment of color6 in section 1.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR7_1[3:0]	3:0	Main window ICC saturation adjustment of color7 in section 1.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR8_1[3:0]	3:0	Main window ICC saturation adjustment of color8 in section 1.	
44h	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR9_1[3:0]	3:0	Main window ICC saturation adjustment of color9 in section 1.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR10_1[3:0]	3:0	Main window ICC saturation adjustment of color10 in section 1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR11_1[3:0]	3:0	Main window ICC saturation adjustment of color11 in section 1.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR12_1[3:0]	3:0	Main window ICC saturation adjustment of color12 in section 1.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR13_1[3:0]	3:0	Main window ICC saturation adjustment of color13 in section 1.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR14_1[3:0]	3:0	Main window ICC saturation adjustment of color14 in section 1.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR15_1[3:0]	3:0	Main window ICC saturation adjustment of color15 in section 1.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR0_2[3:0]	3:0	Main window ICC saturation adjustment of color0 in section 2.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR1_2[3:0]	3:0	Main window ICC saturation adjustment of color1 in	

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			section 2.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR2_2[3:0]	3:0	Main window ICC saturation adjustment of color2 in section 2.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR3_2[3:0]	3:0	Main window ICC saturation adjustment of color3 in section 2.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR4_2[3:0]	3:0	Main window ICC saturation adjustment of color4 in section 2.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR5_2[3:0]	3:0	Main window ICC saturation adjustment of color5 in section 2.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR6_2[3:0]	3:0	Main window ICC saturation adjustment of color6 in section 2.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR7_2[3:0]	3:0	Main window ICC saturation adjustment of color7 in section 2.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR8_2[3:0]	3:0	Main window ICC saturation adjustment of color8 in section 2.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR9_2[3:0]	3:0	Main window ICC saturation adjustment of color9 in section 2.	
4Dh	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR10_2[3:0]	3:0	Main window ICC saturation adjustment of color10 in section 2.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR11_2[3:0]	3:0	Main window ICC saturation adjustment of color11 in section 2.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR12_2[3:0]	3:0	Main window ICC saturation adjustment of color12 in section 2.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR13_2[3:0]	3:0	Main window ICC saturation adjustment of color13 in section 2.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR14_2[3:0]	3:0	Main window ICC saturation adjustment of color14 in section 2.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR15_2[3:0]	3:0	Main window ICC saturation adjustment of color15 in section 2.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_ICC_Y_MODE_EN	7	Main window ICC adaptive Y mode enable.	
	SUB_ICC_Y_MODE_EN	6	Sub window ICC adaptive Y mode enable.	
	-	5:2	Reserved.	
	MAIN_ICC_Y_MODE_DIFF_COLOR_EN	1	Main window ICC adaptive Y mode in different color enable.	
	SUB_ICC_Y_MODE_DIFF_COLOR_EN	0	Sub window ICC adaptive Y mode in different color enable.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER_0[7:0]	7:0	Main window ICC decrease saturation in section 0,	
51h	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_SIGN_SA_USER_0[15:8]	7:0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER_1[7:0]	7:0	Main window ICC decrease saturation in section 1 ,	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER_1[15:8]	7:0	See description of '102FA6h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER_2[7:0]	7:0	Main window ICC decrease saturation in section 2,	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER_2[15:8]	7:0	See description of '102FAAh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	IHC_COLOR_TEST[7:0]	7:0	IHC color test mode, 16 colors [15:0].	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	IHC_COLOR_TEST[15:8]	7:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICC_COLOR_TEST[7:0]	7:0	ICC color test mode, 16 colors [15:0].	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICC_COLOR_TEST[15:8]	7:0	See description of '102FB2h'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CBCR_TO_UV	7	Main window cbcr to uv enable.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:4	Reserved.	
	SUB_CBCR_TO_UV	3	Sub window cbcr to uv enable.	
	SUB_ICC_EN	2	Sub window ICC enable.	
	ICC_LOW_RESERVE1	1	Reserved.	
	-	0	Reserved.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR0[3:0]	3:0	Main window ICC saturation adjustment of color 0.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR1[3:0]	3:0	Main window ICC saturation adjustment of color 1.	

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR2[3:0]	3:0	Main window ICC saturation adjustment of color 2.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR3[3:0]	3:0	Main window ICC saturation adjustment of color 3.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR4[3:0]	3:0	Main window ICC saturation adjustment of color 4.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR5[3:0]	3:0	Main window ICC saturation adjustment of color 5.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR6[3:0]	3:0	Main window ICC saturation adjustment of color 6.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR7[3:0]	3:0	Main window ICC saturation adjustment of color 7.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR8[3:0]	3:0	Main window ICC saturation adjustment of color 8.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR9[3:0]	3:0	Main window ICC saturation adjustment of color 9.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR10[3:0]	3:0	Main window ICC saturation adjustment of color 10.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR11[3:0]	3:0	Main window ICC saturation adjustment of color 11.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR12[3:0]	3:0	Main window ICC saturation adjustment of color 12.	

SC1 PEAKING2 Register (Bank = 102F, Sub-Bank = 2B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR13[3:0]	3:0	Main window ICC saturation adjustment of color 13.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR14[3:0]	3:0	Main window ICC saturation adjustment of color 14.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_COLOR15[3:0]	3:0	Main window ICC saturation adjustment of color 15.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation,	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER[15:8]	7:0	See description of '102FD2h'.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain, .XXXXX.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold, .XXXXXXX.	
6Eh ~ 6Eh (102FDCh ~ 102FDDh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SC1 VOP2_RP Register (Bank = 102F, Sub-Bank = 2D)

SC1 VOP2_RP Register (Bank = 102F, Sub-Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 02h (102F02h ~ 102F04h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_BW_EN	7	Xvycc programmable degamma table burst write enable.	
	XVYCC_DGTCS[1:0]	6:5	Xvycc programmable degamma table channel select: 00: Select R Channel. 01: Select G Channel. 10: Select B Channel. 11: Select All Channel when write; reserved for read.	
	XVYCC_DGT_RD_EN	4	Xvycc programmable degamma table read enable: will hardware clear to 0 after read back.	
	XVYCC_DGT_WR_EN	3	Xvycc programmable degamma table write enable: will hardware clear to 0 after write.	
	-	2:0	Reserved.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	XVYCC_DGT_BW_FLAG	1	Xvycc programmable degamma table burst write status when burst write enable.	
	-	0	Reserved.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_ADR[7:0]	7:0	Xvycc programmable degamma table address port.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_ADR[9:8]	1:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_DATA[7:0]	7:0	Xvycc programmable degamma table write data port[15:0].	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_DATA[15:8]	7:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_DATA_EX1[7:0]	7:0	Xvycc programmable degamma table write data port[24:16].	

SC1 VOP2_RP Register (Bank = 102F, Sub-Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	XVYCC_DGT_DATA_EX1[8]	0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : RO**
	XVYCC_DGT_RD_DATA[7:0]	7:0	Xvycc programmable degamma table read data port[15:0].	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : RO**
	XVYCC_DGT_RD_DATA[15:8]	7:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : RO**
	XVYCC_DGT_RD_DATA_EX1[7:0]	7:0	Xvycc programmable degamma table read data port[24:16].	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	XVYCC_DGT_RD_DATA_EX1[8]	0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP1_ADR_R[7:0]	7:0	Xvycc programmable degamma table R channel offset value separate point1.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP1_ADR_R[9:8]	1:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP2_ADR_R[7:0]	7:0	Xvycc programmable degamma table R channel offset value separate point2.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP2_ADR_R[9:8]	1:0	See description of '102FCEh'.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP3_ADR_R[7:0]	7:0	Xvycc programmable degamma table R channel offset value separate point3.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP3_ADR_R[9:8]	1:0	See description of '102FD0h'.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP1_ADR_G[7:0]	7:0	Xvycc programmable degamma table G channel offset	

SC1 VOP2_RP Register (Bank = 102F, Sub-Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			value separate point1.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP1_ADR_G[9:8]	1:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP2_ADR_G[7:0]	7:0	Xvycc programmable degamma table G channel offset value separate point2.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP2_ADR_G[9:8]	1:0	See description of '102FD4h'.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP3_ADR_G[7:0]	7:0	Xvycc programmable degamma table G channel offset value separate point3.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP3_ADR_G[9:8]	1:0	See description of '102FD6h'.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP1_ADR_B[7:0]	7:0	Xvycc programmable degamma table B channel offset value separate point1.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP1_ADR_B[9:8]	1:0	See description of '102FD8h'.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP2_ADR_B[7:0]	7:0	Xvycc programmable degamma table B channel offset value separate point2.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP2_ADR_B[9:8]	1:0	See description of '102FDAh'.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_SP3_ADR_B[7:0]	7:0	Xvycc programmable degamma table B channel offset value separate point3.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	XVYCC_DGT_SP3_ADR_B[9:8]	1:0	See description of '102FDCh'.	

SC1 VOP2_RP Register (Bank = 102F, Sub-Bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_OFFSET3_R[1:0]	7:6	Xvycc programmable degamma table R channel offset value for segment3.	
	XVYCC_DGT_OFFSET2_R[1:0]	5:4	Xvycc programmable degamma table R channel offset value for segment2.	
	XVYCC_DGT_OFFSET1_R[1:0]	3:2	Xvycc programmable degamma table R channel offset value for segment1.	
	XVYCC_DGT_OFFSET0_R[1:0]	1:0	Xvycc programmable degamma table R channel offset value for segment0.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_OFFSET3_G[1:0]	7:6	Xvycc programmable degamma table G channel offset value for segment3.	
	XVYCC_DGT_OFFSET2_G[1:0]	5:4	Xvycc programmable degamma table G channel offset value for segment2.	
	XVYCC_DGT_OFFSET1_G[1:0]	3:2	Xvycc programmable degamma table G channel offset value for segment1.	
	XVYCC_DGT_OFFSET0_G[1:0]	1:0	Xvycc programmable degamma table G channel offset value for segment0.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	XVYCC_DGT_OFFSET3_B[1:0]	7:6	Xvycc programmable degamma table B channel offset value for segment3.	
	XVYCC_DGT_OFFSET2_B[1:0]	5:4	Xvycc programmable degamma table B channel offset value for segment2.	
	XVYCC_DGT_OFFSET1_B[1:0]	3:2	Xvycc programmable degamma table B channel offset value for segment1.	
	XVYCC_DGT_OFFSET0_B[1:0]	1:0	Xvycc programmable degamma table B channel offset value for segment0.	

SC3 LPLL Register (Bank = 1031)

SC3 LPLL Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (103102h)	**REG103102**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control: 00: /1; 01: /2; 10: /4; 11: /8.	
01h (103103h)	**REG103103**	**7:0**	**Default : 0x02**	**Access : R/W**
	LPLL1_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio=(1/N); Default ratio=8; 0: Divide 1 ; 1: Divide 1; 2: Divide 2; 3: Divide 3; 4: Divide 4...	
02h (103104h)	**REG103104**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
02h (103105h)	**REG103105**	**7:0**	**Default : 0x07**	**Access : R/W**
	LPLL1_OUTPUT_DIV_SECOND[7:0]	7:0	Output divider.	
03h (103106h)	**REG103106**	**7:0**	**Default : 0x33**	**Access : R/W**
	LPLL1_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL1_2CHIP_SYN_EN	6		
	LPLL1_PD	5	Power down control to PLL (active high).	
	LPLL1_IBIAS_ICTRL[2:0]	4:2		
	LPLL1_ICP_ICTRL[1:0]	1:0	Lpll current control.	
03h (103107h)	**REG103107**	**7:0**	**Default : 0x10**	**Access : RO, R/W**
	LPLL1_HIGH_FLAG	7		
	LPLL1_LOCK	6		
	-	5	Reserved.	
	LPLL1_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL1_EN_SKEW_DIVIDER	1		
	LPLL1_ENFRUN	0		
04h	**REG103108**	**7:0**	**Default : 0x00**	**Access : R/W**

SC3 LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	-	7:5	Reserved.	
	LPLL1_SKEW_CLKP_PHASE_SEL[4:0]	4:0		
04h (103109h)	**REG103109**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL1_SKEW_CLKM_PHASE_SEL[4:0]	4:0		
05h (10310Ah)	**REG10310A**	**7:0**	**Default : 0x22**	**Access : R/W**
	PRD_LOCK_THRESH[3:0]	7:4	Prd lock threshold.	
	PRD_STABLE_THRESH[3:0]	3:0	Clock stable threshold.	
05h (10310Bh)	**REG10310B**	**7:0**	**Default : 0x02**	**Access : R/W**
	PHASE_LOCK_THRESH[7:0]	7:0	Phase lock threshold.	
06h (10310Ch)	**REG10310C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[7:0]	7:0	Limit for clock freq correction modification.	
06h (10310Dh)	**REG10310D**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[15:8]	7:0	See description of '10310Ch'.	
07h (10310Eh)	**REG10310E**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[23:16]	7:0	See description of '10310Ch'.	
08h (103110h)	**REG103110**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[7:0]	7:0	Limit for phase correction modification.	
08h (103111h)	**REG103111**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[15:8]	7:0	See description of '103110h'.	
09h (103112h)	**REG103112**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[23:16]	7:0	See description of '103110h'.	
0Ah (103114h)	**REG103114**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_LPLL_OFFSET[7:0]	7:0	Limit for lpll phase offset.	
0Ah (103115h)	**REG103115**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_LPLL_OFFSET[15:8]	7:0	See description of '103114h'.	
0Bh (103116h)	**REG103116**	**7:0**	**Default : 0x10**	**Access : R/W**
	P_GAIN_PRD[3:0]	7:4	P_gain for prd_lock, gain setting is same as i_gain_prd.	
	I_GAIN_PRD[3:0]	3:0	I_gain for prd lock. 0: >> 5. 1: >> 4. 2: >> 3. 3: >> 2.	

SC3 LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
			4: >> 1. 5: Same. 6: << 1. 7: << 2. 8: << 3. 9: << 4. 10: << 5. 11: << 6. 12: << 7. 13: << 8. 14: << 9. 15: << 10.	
0Bh (103117h)	**REG103117**	**7:0**	**Default : 0x10**	**Access : R/W**
	P_GAIN_PHASE[3:0]	7:4	P_gain for phase lock, gain setting is same as i_gain_prd.	
	I_GAIN_PHASE[3:0]	3:0	I_gain for phase lock, game setting is same as i_gain_prd.	
0Ch (103118h)	**REG103118**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_GAIN_PHASE_ZERO	7	Disable p_gain for lock phase.	
	I_GAIN_PHASE_ZERO	6	Disable i_gain for lock phase.	
	P_GAIN_PRD_ZERO	5	Disable p_gain for lock prd.	
	I_GAIN_PRD_ZERO	4	Disable i_gain for lock prd.	
	FRAME_LPLL_EN	3	Frame lpll enable.	
	-	2	Reserved.	
	FPLL_MODE[1:0]	1:0	FPLL Mode. 00: Lock phase mode. 01: Full mode. 10: Lock_prd_phase_mode. 11: Reduce_phase_mode.	
0Ch (103119h)	**REG103119**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVS_FRAME_DIV[3:0]	7:4	Output fame div for frame sync (bit3 ~ bit0).	
	IVS_FRAME_DIV[3:0]	3:0	Input frame div for frame sync (bit3 ~ bit0).	
0Dh (10311Ah)	**REG10311A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_2_LIMIT	4	Enable 2 limit.	
	FORCE_PHASE_CLOSE_DONE	3	S.W.	

SC3 LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
			Force phase close done.	
	FORCE_PHASE_REDUCE_DONE	2	S.W. Force phase reduce done.	
	FORCE_PRD_LOCK_DONE	1	S.W. Force prd lock done.	
	FORCE_PRD_STABLE	0	S.W. Force prd stable check ok.	
0Dh (10311Bh)	**REG10311B**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	SSC_EN	3	SSC mode enable.	
	-	2	Reserved.	
	NON_STABLE_EN	1	Frame pll disable when non_stable flag high.	
	NO_SIGNAL_EN	0	Frame pll disable when no_signal flag high.	
0Eh (10311Ch)	**REG10311C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	EXT_OVS_FRAME_DIV	1	Output frame div for frame sync, high bit (bit4).	
	EXT_IVS_FRAME_DIV	0	Input frame div for frame sync, high bit (bit4).	
0Fh (10311Eh)	**REG10311E**	**7:0**	**Default : 0x44**	**Access : R/W**
	PLL_SET[7:0]	7:0	PLL initial setting value.	
0Fh (10311Fh)	**REG10311F**	**7:0**	**Default : 0x55**	**Access : R/W**
	PLL_SET[15:8]	7:0	See description of '10311Eh'.	
10h (103120h)	**REG103120**	**7:0**	**Default : 0x24**	**Access : R/W**
	PLL_SET[23:16]	7:0	See description of '10311Eh'.	
11h (103122h)	**REG103122**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_DIF[7:0]	7:0	Phase dif value.	
11h (103123h)	**REG103123**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_DIF[15:8]	7:0	See description of '103122h'.	
12h (103124h)	**REG103124**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PHASE_UP	0	Ovs leading or lagging related to ivs. 0: Leading. 1: Lagging.	
13h (103126h)	**REG103126**	**7:0**	**Default : 0x00**	**Access : RO**
	PRD_DIF[7:0]	7:0	Reference signal prd difference value.	

SC3 LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
13h (103127h)	**REG103127**	**7:0**	**Default : 0x00**	**Access : RO**
	PRD_DIF[15:8]	7:0	See description of '103126h'.	
14h (103128h)	**REG103128**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PRD_UP	0	Ovs prd related to ivs prd. 0: Faster. 1: Slower.	
15h (10312Ah)	**REG10312A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control: 00: /1; 01: /2; 10: /4; 11: /8.	
15h (10312Bh)	**REG10312B**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N); 0: Divide 1 ; 1: Divide 1; 2: Divide 2; 3: Divide 3; 4: Divide 4...	
17h (10312Eh)	**REG10312E**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL_STEP[7:0]	7:0	Output PLL spread spectrum step.	
17h (10312Fh)	**REG10312F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_STEP[9:8]	1:0	See description of '10312Eh'.	
18h (103130h)	**REG103130**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_SPAN[7:0]	7:0	Output PLL spread spectrum span.	
18h (103131h)	**REG103131**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_SPAN[13:8]	5:0	See description of '103130h'.	
19h (103132h)	**REG103132**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDCLK_DIV[7:0]	7:0	Input clock divider for prd sync.	
19h (103133h)	**REG103133**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDCLK_DIV[15:8]	7:0	See description of '103132h'.	

SC3 LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
1Ah (103134h)	**REG103134**	**7:0**	**Default : 0x00**	**Access : R/W**
	IDCLK_DIV[23:16]	7:0	See description of '103132h'.	
1Bh (103136h)	**REG103136**	**7:0**	**Default : 0x00**	**Access : R/W**
	ODCLK_DIV[7:0]	7:0	Output dlock divider for prd sync.	
1Bh (103137h)	**REG103137**	**7:0**	**Default : 0x00**	**Access : R/W**
	ODCLK_DIV[15:8]	7:0	See description of '103136h'.	
1Ch (103138h)	**REG103138**	**7:0**	**Default : 0x00**	**Access : R/W**
	ODCLK_DIV[23:16]	7:0	See description of '103136h'.	
1Fh (10313Eh)	**REG10313E**	**7:0**	**Default : 0x80**	**Access : R/W**
	PHASE_CLOSE_THRESH[7:0]	7:0	Phase close done threshold.	
1Fh (10313Fh)	**REG10313F**	**7:0**	**Default : 0x30**	**Access : R/W**
	REDUCE_DONE_THRESH[3:0]	7:4	Phase reduce done threshold.	
	PHASE_CLOSE_THRESH[11:8]	3:0	See description of '10313Eh'.	
20h (103140h)	**REG103140**	**7:0**	**Default : 0x52**	**Access : R/W**
	-	7	Reserved.	
	HIS_CNT_HIGH_THRESH[2:0]	6:4	History counter high threshold.	
	-	3	Reserved.	
	HIS_CNT_LOW_THRESH[2:0]	2:0	History counter low threshold.	
21h (103142h)	**REG103142**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[7:0]	7:0	Ivs prd value.	
21h (103143h)	**REG103143**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[15:8]	7:0	See description of '103142h'.	
22h (103144h)	**REG103144**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[23:16]	7:0	See description of '103142h'.	
23h (103146h)	**REG103146**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[7:0]	7:0	Ovs prd value.	
23h (103147h)	**REG103147**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[15:8]	7:0	See description of '103146h'.	
24h (103148h)	**REG103148**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[23:16]	7:0	See description of '103146h'.	
26h (10314Ch)	**REG10314C**	**7:0**	**Default : 0x00**	**Access : RO**
	FIX_V_TOTAL[7:0]	7:0	Reduce phase modify v_total value.	
26h	**REG10314D**	**7:0**	**Default : 0x00**	**Access : RO**

SC3 LPLL Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	FIX_V_TOTAL[11:8]	3:0	See description of '10314Ch'.	
28h (103150h)	**REG103150**	**7:0**	**Default : 0x00**	**Access : RO**
	PLL_SET_USING[7:0]	7:0	Pll_set value for using.	
28h (103151h)	**REG103151**	**7:0**	**Default : 0x00**	**Access : RO**
	PLL_SET_USING[15:8]	7:0	See description of '103150h'.	
29h (103152h)	**REG103152**	**7:0**	**Default : 0x00**	**Access : RO**
	PLL_SET_USING[23:16]	7:0	See description of '103150h'.	
2Ah (103154h)	**REG103154**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_REDUCE_DONE	7	Phase reduce done flag.	
	PRD_LOCK_DONE	6	Prd lock done flag.	
	IVS_PRD_STABLE	5	Idclk stable flag.	
	OVS_PRD_STABLE	4	Odclk stable flag.	
	-	3	Reserved.	
	CS_STATE[2:0]	2:0	Frame pll FSM state. 3'h0 : free run. 3'h1 : lock_freq. 3'h2 : reduce_phase. 3'h3 : wait phase_close. 3'h4 : lock_phase. Others: Reserved.	
2Ah (103155h)	**REG103155**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PHASE_LOCK_DONE	0	Phase lock done flag.	
30h (103160h)	**REG103160**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control: 00: /1; 01: /2; 10: /4; 11: /8.	
30h (103161h)	**REG103161**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N); 0: Divide 1 ; 1: Divide 1;	

SC3 LPLL Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2: Divide 2; 3: Divide 3; 4: Divide 4...	
31h (103162h)	**REG103162**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control: 00: /1; 01: /2; 10: /4; 11: /8.	
31h (103163h)	**REG103163**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio=(1/N); Default ratio=8; 0: Divide 1 ; 1: Divide 1; 2: Divide 2; 3: Divide 3; 4: Divide 4...	
32h (103164h)	**REG103164**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
32h (103165h)	**REG103165**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_OUTPUT_DIV_SECOND[7:0]	7:0	Output divider.	
33h (103166h)	**REG103166**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL2_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL2_2CHIP_SYN_EN	6		
	LPLL2_PD	5	Power down control to PLL (active high).	
	LPLL2_IBIAS_ICTRL[2:0]	4:2		
	LPLL2_ICP_ICTRL[1:0]	1:0	Lpll current control.	
33h (103167h)	**REG103167**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LPLL2_HIGH_FLAG	7		
	LPLL2_LOCK	6		
	-	5	Reserved.	
	LPLL2_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL2_EN_SKEW_DIVIDER	1		

SC3 LPLL Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LPLL2_ENFRUN	0		
34h (103168h)	**REG103168**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL2_SKEW_CLKP_PHASE_SEL[5:0]	5:0		
34h (103169h)	**REG103169**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL2_SKEW_CLKM_PHASE_SEL[5:0]	5:0		
35h (10316Ah)	**REG10316A**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_2NDPLL_CLK_SEL	5		
	LPLL_POSTDIV_RESET	4		
	-	3	Reserved.	
	LPLL_2CHIP_REFIN_SEL	2		
	LPLL_2CHIP_FBIN_SEL	1		
	LPLL_2CHIP_CLKOUT_SEL	0		
35h (10316Bh)	**REG10316B**	**7:0**	**Default : 0x1F**	**Access : R/W**
	LPLL_RESERVED_DIV_I[3:0]	7:4	Reserved div sel.	
	LPLL_RESERVED_PD[3:0]	3:0	Reserved power down control (active high).	
36h (10316Ch)	**REG10316C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[7:0]	7:0	LPLL1_TEST.	
36h (10316Dh)	**REG10316D**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[15:8]	7:0	See description of '10316Ch'.	
37h (10316Eh)	**REG10316E**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[23:16]	7:0	See description of '10316Ch'.	
37h (10316Fh)	**REG10316F**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[31:24]	7:0	See description of '10316Ch'.	
38h (103170h)	**REG103170**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_SCALAR_FB_DIV2_EN	1		
	LPLL_NCO_RETIME_SEL	0	Retime NCO clock, 1'b0:enable, 1'b1:disable.	
39h (103172h)	**REG103172**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_TEST[7:0]	7:0	LPLL2_TEST.	
39h	**REG103173**	**7:0**	**Default : 0x00**	**Access : R/W**

SC3 LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	LPLL2_TEST[15:8]	7:0	See description of '103172h'.	
3Ah (103174h)	**REG103174**	**7:0**	**Default : 0x0C**	**Access : R/W**
	LPLL_RESERVED_DIV_J[3:0]	7:4	Reserved div sel.	
	OEN_FBIN	3		
	OEN_REFIN	2		
	LPLL1_RX_CLKFB_SEL	1		
	LPLL1_CLKIN_SEL	0		
3Ah (103175h)	**REG103175**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_RESERVED_DIV_M[3:0]	7:4	Reserved div sel.	
	LPLL_RESERVED_DIV_N[3:0]	3:0	Reserved div sel.	
40h (103180h)	**REG103180**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_SYN_CLK_SEL	7		
	-	6:2	Reserved.	
	LPLL_EXT_INPUT_DIV_FIRST[1:0]	1:0		
40h (103181h)	**REG103181**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_INPUT_DIV_SECOND[7:0]	7:0		
41h (103182h)	**REG103182**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_EXT_LOOP_DIV_FIRST[1:0]	1:0		
41h (103183h)	**REG103183**	**7:0**	**Default : 0x03**	**Access : R/W**
	LPLL_EXT_LOOP_DIV_SECOND[7:0]	7:0		
42h (103184h)	**REG103184**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_EXT_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
43h (103186h)	**REG103186**	**7:0**	**Default : 0x2A**	**Access : R/W**
	-	7	Reserved.	
	LPLL_EXT_NCO_RETIME_SEL	6	1: Disable retime.	
	LPLL_EXT_PD	5	Power down control to PLL (active high).	
	LPLL_EXT_IBIAS_ICTRL[2:0]	4:2		
	LPLL_EXT_ICP_ICTRL[1:0]	1:0	Lpll current control.	
43h (103187h)	**REG103187**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LPLL_EXT_HIGH_FLAG	7		
	LPLL_EXT_LOCK	6		

SC3 LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	-	5:1	Reserved.	
	LPLL_EXT_SSC_EN	0	SSC mode enable (extra).	
44h (103188h)	**REG103188**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LPLL_EXT_PHSEL[3:0]	3:0		
44h (103189h)	**REG103189**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL_EXT_COARSE_PHSEL[4:0]	4:0		
45h (10318Ah)	**REG10318A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_EXT_SCALAR_DIV_FIRST[1:0]	1:0		
45h (10318Bh)	**REG10318B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LPLL_EXT_SCALAR_DIV_SECOND[3:0]	3:0		
46h (10318Dh)	**REG10318D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LPLL_EXT_SKEW_DIV[2:0]	2:0		
48h (103190h)	**REG103190**	**7:0**	**Default : 0x44**	**Access : R/W**
	LPLL_EXT_SET[7:0]	7:0	Ext PLLSET.	
48h (103191h)	**REG103191**	**7:0**	**Default : 0x55**	**Access : R/W**
	LPLL_EXT_SET[15:8]	7:0	See description of '103190h'.	
49h (103192h)	**REG103192**	**7:0**	**Default : 0x24**	**Access : R/W**
	LPLL_EXT_SET[23:16]	7:0	See description of '103190h'.	
4Ah (103194h)	**REG103194**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_TEST[7:0]	7:0	LPLL_EXT_TEST.	
4Ah (103195h)	**REG103195**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_TEST[15:8]	7:0	See description of '103194h'.	
4Bh (103196h)	**REG103196**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_TEST[23:16]	7:0	See description of '103194h'.	
4Eh (10319Ch)	**REG10319C**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL_EXT_STEP[7:0]	7:0	Output PLL spread spectrum step (extra).	
4Eh (10319Dh)	**REG10319D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

SC3 LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	LPLL_EXT_STEP[9:8]	1:0	See description of '10319Ch'.	
4Fh (10319Eh)	**REG10319E**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_EXT_SPAN[7:0]	7:0	Output PLL spread spectrum span (extra).	
4Fh (10319Fh)	**REG10319F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_EXT_SPAN[13:8]	5:0	See description of '10319Eh'.	
60h (1031C0h)	**REG1031C0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LPLL1_VBYONE_DIV[2:0]	2:0	Lpll1 v-by-one divider.	
60h (1031C1h)	**REG1031C1**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_EN_VBYONE	7	Enable lpll1 v-by-one mode.	
	-	6:0	Reserved.	
70h (1031E0h)	**REG1031E0**	**7:0**	**Default : 0x80**	**Access : R/W**
	FSYNC_RESET_THRESH[7:0]	7:0	Fsync phase offset threshold.	
70h (1031E1h)	**REG1031E1**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	EN_CLK_DIV	7	Enable lock freq mode.	
	-	6:4	Reserved.	
	EN_PLL_FSYNC_RESET	3	Enable fsync reset signal generate.	
	-	2	Reserved.	
	CLR_FSYNC_RESET_2T_FLAG	1	Clear fsync reset multi-time flag.	
	FSYNC_RESET_2T_FLAG	0	Fsync reset multi-times flag.	
72h (1031E4h)	**REG1031E4**	**7:0**	**Default : 0x00**	**Access : RO**
	IDCLK_DIV_PRD[7:0]	7:0	Input clock divider period in mclk.	
72h (1031E5h)	**REG1031E5**	**7:0**	**Default : 0x00**	**Access : RO**
	IDCLK_DIV_PRD[15:8]	7:0	See description of '1031E4h'.	
73h (1031E6h)	**REG1031E6**	**7:0**	**Default : 0x00**	**Access : RO**
	IDCLK_DIV_PRD[23:16]	7:0	See description of '1031E4h'.	
74h (1031E8h)	**REG1031E8**	**7:0**	**Default : 0x00**	**Access : RO**
	ODCLK_DIV_PRD[7:0]	7:0	Output clock divider period in mclk.	
74h (1031E9h)	**REG1031E9**	**7:0**	**Default : 0x00**	**Access : RO**
	ODCLK_DIV_PRD[15:8]	7:0	See description of '1031E8h'.	
75h (1031EAh)	**REG1031EA**	**7:0**	**Default : 0x00**	**Access : RO**
	ODCLK_DIV_PRD[23:16]	7:0	See description of '1031E8h'.	

SC3 LPLL Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Fh (1031FEh)	**REG1031FE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SW_TRIG_DB_LOAD	1	Trig to load double buffer register.	
	DB_EN	0	Enable lpll register double.	
7Fh (1031FFh)	**REG1031FF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	TGEN_SRC_SEL	0	Tgen source selection.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 07h (103203h ~ 10320Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Dh (10321Ah)	**REG10321A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	FRC_DVI340_SW_RST	0	Software reset of dvi340 domain.	
0Dh (10321Bh)	**REG10321B**	**7:0**	**Default : 0x08**	**Access : R/W**
	HDMI_BYPASS	7	Enable HDMI bypass mode.	
	HDMI_VS_INV	6	HDMI vsync invert.	
	HDMI_HS_INV	5	HDMI hsync invert.	
	HDMI_DE_INV	4	HDMI de invert.	
	HDMI_HW_FULL_CLR_EN	3	HDMI FIFO full clear enable.	
	-	2:0	Reserved.	
0Eh (10321Ch)	**REG10321C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HALFLINE[7:0]	7:0	Set HDE/2-1 for LR output.	
0Eh (10321Dh)	**REG10321D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	MFT_LB_EN	7	Enable mft LB for LR output.	
	DE2TO1_ENABLE	6	De2to1 for 3D PDP mode.	
	-	5:4	Reserved.	
	HALFLINE[11:8]	3:0	See description of '10321Ch'.	
0Fh (10321Eh)	**REG10321E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	HALFLINE2[7:0]	7:0	Set HDE/2-1 for LR output.	
0Fh (10321Fh)	**REG10321F**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	HALFLINE2[11:8]	3:0	See description of '10321Eh'.	
10h (103220h)	**REG103220**	**7:0**	**Default : 0xFF**	**Access : R/W**
	V_BLK_ST1_VPOS[7:0]	7:0	Bt656 v blanking 1st start v position.	
10h (103221h)	**REG103221**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	V_BLK_ST1_VPOS[11:8]	3:0	See description of '103220h'.	
11h	**REG103222**	**7:0**	**Default : 0xFF**	**Access : R/W**

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	V_BLK_ST1_HPOS[7:0]	7:0	Bt656 v blanking 1st start h position.	
11h (103223h)	**REG103223**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	V_BLK_ST1_HPOS[11:8]	3:0	See description of '103222h'.	
12h (103224h)	**REG103224**	**7:0**	**Default : 0xFF**	**Access : R/W**
	V_BLK_END1_VPOS[7:0]	7:0	Bt656 v blanking 1st end v position.	
12h (103225h)	**REG103225**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	V_BLK_END1_VPOS[11:8]	3:0	See description of '103224h'.	
13h (103226h)	**REG103226**	**7:0**	**Default : 0xFF**	**Access : R/W**
	V_BLK_END1_HPOS[7:0]	7:0	Bt656 v blanking 1st end h position.	
13h (103227h)	**REG103227**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	V_BLK_END1_HPOS[11:8]	3:0	See description of '103226h'.	
14h (103228h)	**REG103228**	**7:0**	**Default : 0xFF**	**Access : R/W**
	V_BLK_ST2_VPOS[7:0]	7:0	Bt656 v blanking 2nd start v position.	
14h (103229h)	**REG103229**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	V_BLK_ST2_VPOS[11:8]	3:0	See description of '103228h'.	
15h (10322Ah)	**REG10322A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	V_BLK_ST2_HPOS[7:0]	7:0	Bt656 v blanking 2nd start h position.	
15h (10322Bh)	**REG10322B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	V_BLK_ST2_HPOS[11:8]	3:0	See description of '10322Ah'.	
16h (10322Ch)	**REG10322C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	V_BLK_END2_VPOS[7:0]	7:0	Bt656 v blanking 2nd end v position.	
16h (10322Dh)	**REG10322D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	V_BLK_END2_VPOS[11:8]	3:0	See description of '10322Ch'.	
17h (10322Eh)	**REG10322E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	V_BLK_END2_HPOS[7:0]	7:0	Bt656 v blanking 2nd end h position.	
17h (10322Fh)	**REG10322F**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	V_BLK_END2_HPOS[11:8]	3:0	See description of '10322Eh'.	
18h (103230h)	**REG103230**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FLD_ST1_VPOS[7:0]	7:0	Bt656 field1 start v position.	
18h (103231h)	**REG103231**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	FLD_ST1_VPOS[11:8]	3:0	See description of '103230h'.	
19h (103232h)	**REG103232**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FLD_ST1_HPOS[7:0]	7:0	Bt656 field1 start h position.	
19h (103233h)	**REG103233**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	FLD_ST1_HPOS[11:8]	3:0	See description of '103232h'.	
1Ah (103234h)	**REG103234**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FLD_ST2_VPOS[7:0]	7:0	Bt656 field2 start v position.	
1Ah (103235h)	**REG103235**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	FLD_ST2_VPOS[11:8]	3:0	See description of '103234h'.	
1Bh (103236h)	**REG103236**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FLD_ST2_HPOS[7:0]	7:0	Bt656 field2 start h position.	
1Bh (103237h)	**REG103237**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	FLD_ST2_HPOS[11:8]	3:0	See description of '103236h'.	
1Ch (103238h)	**REG103238**	**7:0**	**Default : 0x00**	**Access : R/W**
	MASK_Y_BLK_VA[7:0]	7:0	Bt656 mask y blk value.	
1Ch (103239h)	**REG103239**	**7:0**	**Default : 0x08**	**Access : R/W**
	BT656_EN	7	Bt656 enable.	
	BT656_8BIT	6	Bt656 8bit mode.	
	DDR_HL_SWAP	5	Bt656 DDR high low swap.	
	CRCB_SWAP	4	Swap crcb position in 422.	
	444_BYPASS	3	Enable 444 to 422 conversion.	
	MASK_Y_BLK_EN	2	Bt656 mask y blk enable.	
	MASK_Y_BLK_VA[9:8]	1:0	See description of '103238h'.	
1Dh (10323Ah)	**REG10323A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MASK_C_BLK_VA[7:0]	7:0	Bt656 mask c blk value.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (10323Bh)	**REG10323B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MASK_C_BLK_EN	2	Bt656 mask c blk enable.	
	MASK_C_BLK_VA[9:8]	1:0	See description of '10323Ah'.	
1Eh (10323Ch)	**REG10323C**	**7:0**	**Default : 0x00**	**Access : R/W**
	TCON_OUT_MUX[7:0]	7:0	Enable TCON gpo output mux.	
1Eh (10323Dh)	**REG10323D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	TCON_OUT_MUX[13:8]	5:0	See description of '10323Ch'.	
20h (103240h)	**REG103240**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_DOT_MINI_PRE_OSD[3:0]	7:4	Clock gen register of clk_dot_mini_pre_OSD. Bit[0]: gating. Bit[1]: invert. Bit[3:2] = 00:normal, 01:OSD.	
	CKG_DOT_MINI_OSD[3:0]	3:0	Clock gen register of clk_dot_mini_OSD. Bit[0]: gating. Bit[1]: invert. Bit[3:2] = 00:normal, 01:OSD.	
20h (103241h)	**REG103241**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_DOT_MINI_PRE[3:0]	7:4	Clock gen register of clk_dot_mini_pre. Bit[0]: gating. Bit[1]: invert. Bit[3:2] = 00, enable.	
	CKG_DOT_MINI[3:0]	3:0	Clock gen register of clk_dot_mini. Bit[0]: gating. Bit[1]: invert. Bit[3:2] = 00, enable.	
23h (103246h)	**REG103246**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_PE_ADJ_CH2[1:0]	7:6	Differential output data/clock pre-emphasis level adjust of ch2.	
	GCR_PE_ADJ_CH1[2:0]	5:3	Differential output data/clock pre-emphasis level adjust of ch1.	
	GCR_PE_ADJ_CH0[2:0]	2:0	Differential output data/clock pre-emphasis level adjust of ch0. Pre-emphasis level adj. 3'b000: 0mV +/- 15%.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			3'b001: 20mV +/- 15 %. 3'b010: 40mV +/- 15%. .. 3'b111: 140mV +/- 15%. Pre-emphasis Voltage Formula: Vpem = 20* ADJ[2:0] mV +/- 15%.	
23h (103247h)	**REG103247**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GCR_PE_ADJ_CH4[2:0]	6:4	Differential output data/clock pre-emphasis level adjust of ch4.	
	GCR_PE_ADJ_CH3[2:0]	3:1	Differential output data/clock pre-emphasis level adjust of ch3.	
	GCR_PE_ADJ_CH2[2]	0	See description of '103246h'.	
24h (103248h)	**REG103248**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_PE_ADJ_CH7[1:0]	7:6	Differential output data/clock pre-emphasis level adjust of ch7.	
	GCR_PE_ADJ_CH6[2:0]	5:3	Differential output data/clock pre-emphasis level adjust of ch6.	
	GCR_PE_ADJ_CH5[2:0]	2:0	Differential output data/clock pre-emphasis level adjust of ch5.	
24h (103249h)	**REG103249**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GCR_PE_ADJ_CH9[2:0]	6:4	Differential output data/clock pre-emphasis level adjust of ch9.	
	GCR_PE_ADJ_CH8[2:0]	3:1	Differential output data/clock pre-emphasis level adjust of ch8.	
	GCR_PE_ADJ_CH7[2]	0	See description of '103248h'.	
25h (10324Ah)	**REG10324A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_PE_ADJ_CH12[1:0]	7:6	Differential output data/clock pre-emphasis level adjust of ch12.	
	GCR_PE_ADJ_CH11[2:0]	5:3	Differential output data/clock pre-emphasis level adjust of ch11.	
	GCR_PE_ADJ_CH10[2:0]	2:0	Differential output data/clock pre-emphasis level adjust of ch10.	
25h (10324Bh)	**REG10324B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GCR_PE_ADJ_CH13[2:0]	3:1	Differential output data/clock pre-emphasis level adjust of ch13.	
	GCR_PE_ADJ_CH12[2]	0	See description of '10324Ah'.	
29h (103252h)	**REG103252**	**7:0**	**Default : 0x50**	**Access : R/W**
	GCR_ICON_CH0[3:0]	7:4	Control swing of ch0. Control swing of each pair. 6'h0: 40mV +/- 15%. 6'h1: 50mV +/- 15%. 6'h2: 60mV +/- 15%. .. 6'h3f: 670mV +/- 15%. Output Swing Formula: Vout_swing= 40 + 10 * ICON[5:0] mV +/- 15%.	
	-	3:0	Reserved.	
29h (103253h)	**REG103253**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH1[5:0]	7:2	Control swing of ch1.	
	GCR_ICON_CH0[5:4]	1:0	See description of '103252h'.	
2Ah (103254h)	**REG103254**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH3[1:0]	7:6	Control swing of ch3.	
	GCR_ICON_CH2[5:0]	5:0	Control swing of ch2.	
2Ah (103255h)	**REG103255**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH4[3:0]	7:4	Control swing of ch4.	
	GCR_ICON_CH3[5:2]	3:0	See description of '103254h'.	
2Bh (103256h)	**REG103256**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH5[5:0]	7:2	Control swing of ch5.	
	GCR_ICON_CH4[5:4]	1:0	See description of '103255h'.	
2Bh (103257h)	**REG103257**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH7[1:0]	7:6	Control swing of ch7.	
	GCR_ICON_CH6[5:0]	5:0	Control swing of ch6.	
2Ch (103258h)	**REG103258**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH8[3:0]	7:4	Control swing of ch8.	
	GCR_ICON_CH7[5:2]	3:0	See description of '103257h'.	
2Ch (103259h)	**REG103259**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH9[5:0]	7:2	Control swing of ch9.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GCR_ICON_CH8[5:4]	1:0	See description of '103258h'.	
2Dh (10325Ah)	**REG10325A**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH11[1:0]	7:6	Control swing of ch11.	
	GCR_ICON_CH10[5:0]	5:0	Control swing of ch10.	
2Dh (10325Bh)	**REG10325B**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH12[3:0]	7:4	Control swing of ch12.	
	GCR_ICON_CH11[5:2]	3:0	See description of '10325Ah'.	
2Eh (10325Ch)	**REG10325C**	**7:0**	**Default : 0x55**	**Access : R/W**
	GCR_ICON_CH13[5:0]	7:2	Control swing of ch13.	
	GCR_ICON_CH12[5:4]	1:0	See description of '10325Bh'.	
32h (103264h)	**REG103264**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MINI_CLK_GATE_EN	1	Gate mini FIFO clk enable.	
	MOD_CLK_GATE_EN	0	Gate mod clk enable.	
32h (103265h)	**REG103265**	**7:0**	**Default : 0x00**	**Access : R/W**
	DIGI_SERI_TEST_EN	7	Test enable of digi seri.	
	-	6:0	Reserved.	
33h (103266h)	**REG103266**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWUPLIMIT[0]	7	Mod_seri_top software up limit.	
	SWLOWLIMIT[2:0]	6:4	Mod_seri_top software low limit.	
	SWCHECK_POINT[3:0]	3:0	Mod_seri_top software check point.	
33h (103267h)	**REG103267**	**7:0**	**Default : 0x80**	**Access : R/W**
	CHECKENABLE	7	Mod_seri_top CHECKENABLE.	
	DATA_FORMAT	6	{DATA_FORMAT3,DATA_FORMAT2,reg_data format}. 000: LVDS. 001: MiniLVDS. 010: New LVDS format. 100: Reserved. 101: Reserved. 110: Reserved.	
	SWRST_POINT[2:0]	5:3	Mod_seri_top software reset point.	
	SWMODE_EN	2	Mod_seri_top software mode enable.	
	SWUPLIMIT[2:1]	1:0	See description of '103266h'.	
34h	**REG103268**	**7:0**	**Default : 0x00**	**Access : R/W**

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SWLOWLIMIT_BIT4_3[1:0]	7:6	Mod_seri_top software low limit.	
	SWCHECK_POINT_BIT4_3[1:0]	5:4	Mod_seri_top software check point.	
	-	3:0	Reserved.	
34h (103269h)	**REG103269**	**7:0**	**Default : 0x00**	**Access : R/W**
	DATAX_SEL[1:0]	7:6	Digital serializer source mux. 00: LVDS. 01: MiniLVDS. 1x: Reserved.	
	DATA_FORMAT3	5	{DATA_FORMAT3,reg_data_format2,reg_data format}. 000: LVDS. 001: MiniLVDS. 010: New LVDS format. 100: Reserved. 101: Reserved. 110: Reserved.	
	DATA_FORMAT2	4	{reg_data_format3,DATA_FORMAT2,reg_data format}. 000: LVDS. 001: MiniLVDS. 010: New LVDS format. 100: Reserved. 101: Reserved. 110: Reserved.	
	SWRST_POINT_BIT4_3[1:0]	3:2	Mod_seri_top software reset point.	
	SWUPLIMIT_BIT4_3[1:0]	1:0	Mod_seri_top software up limit.	
37h (10326Eh)	**REG10326E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GCR_PVDD_2P5	6	MOD PVDD power. 0: 3.3V. 1: 2.5V.	
	GCR_VCM_0P9	5	Differential output common mode voltage adjust. 0: 1.25V. 1: 0.94V.	
	-	4:0	Reserved.	
3Eh (10327Ch)	**REG10327C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MINICLK_SEL[7:0]	7:0	Select pair number as miniLVDS clk.	
3Eh	**REG10327D**	**7:0**	**Default : 0x40**	**Access : R/W**

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MINICLK_PHASE[1:0]	7:6	MiniLVDS clock phase sel. 01 or 10.	
	MINICLK_SEL[13:8]	5:0	See description of '10327Ch'.	
40h (103280h)	**REG103280**	**7:0**	**Default : 0x08**	**Access : R/W**
	LVDS_OSD_A	7	LVDS OSD enable for Channel A.	
	CH_SWAP	6	For pair swapping with reg_pdp_10bit.	
	CH_POLARITY	5	Channel polarity p/n swap for LVDS pair.	
	LVDS_PLASMA_A	4	LVDS_PLASMA for Channel A.	
	PDP_10BIT	3	PDP_10BIT for pair swap with reg_ch_swap.	
	LVDS_TI	2	LVDS_TI. 0: JEIDA mode. 1: VESA mode with reg_ti_bitmode.	
	-	1:0	Reserved.	
40h (103281h)	**REG103281**	**7:0**	**Default : 0x00**	**Access : R/W**
	ECLKDLYSEL[3:0]	7:4	De delay for TTL output.	
	CLKDLYSEL[3:0]	3:0	Clock delay for TTL output.	
41h (103283h)	**REG103283**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDP_MASK_EN_A	7	PDP_MASK_EN DE channel A.	
	PDP_MASK_SET_A	6	PDP_MASK_SET DE channel A.	
	PDP_CH3_EN_A	5	PDP_CH3_EN channel A.	
	PDP_CH3_SET_A	4	PDP_CH3_SET channel A.	
	PDP_CH4_EN_A	3	PDP_CH4_EN channel A.	
	PDP_CH4_SET_A	2	PDP_CH4_SET for channel A.	
	SKEW[1:0]	1:0	ODD Red TTL data SKEW.	
42h (103284h)	**REG103284**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PDP_10BIT_MOR[1:0]	5:4	More pair swap mode.	
	EN_OSD_LVDS	3	Enable OSD LVDS path.	
	EN_VS_ON_OSD	2	Vsync on OSD enable.	
	PAIR_SWAP_MOR[1:0]	1:0	More pair swap mode.	
42h (103285h)	**REG103285**	**7:0**	**Default : 0x10**	**Access : R/W**
	OSD_DE_INV	7	Invert OSD DE.	
	OSD_ON_DE_B	6	PDP OSD de on DE channel B.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OSD_ON_DE_A	5	PDP OSD de on DE channel A.	
	SW_RST	4	Software reset.	
	LVDS_OSD_B	3	LVDS OSD enable for Channel B.	
	LVDS_PLASMA_B	2	LVDS_PLASMA for Channel B.	
	-	1	Reserved.	
	EN_MORE_PAIR_SWAP	0	Enable more pair swap.	
43h (103286h)	**REG103286**	**7:0**	**Default : 0xC6**	**Access : R/W**
	LVDS_CLOCK_PHASE[6:0]	7:1	Clock phase could be set by register.	
	CLK_PAIR_SWAP	0	More LVDS clock pair swap.	
43h (103287h)	**REG103287**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDP_MASK_EN_B	7	PDP_MASK_EN DE channel B.	
	PDP_MASK_SET_B	6	PDP_MASK_SET DE channel B.	
	PDP_CH3_EN_B	5	PDP_CH3_EN channel B.	
	PDP_CH3_SET_B	4	PDP_CH3_SET channel B.	
	PDP_CH4_EN_B	3	PDP_CH4_EN channel B.	
	PDP_CH4_SET_B	2	PDP_CH4_SET for channel B.	
	-	1:0	Reserved.	
44h (103288h)	**REG103288**	**7:0**	**Default : 0x00**	**Access : R/W**
	SKEW_OTHER[7:0]	7:0	TTL skew for others. [1:0]: ODD Green. [3:2]: ODD Blue. [5:4]: EVEN Red. [7:6]: EVEN Green. [9:8]: EVEN Blue.	
44h (103289h)	**REG103289**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LCK_PHASE_SEL	3	Phase select of TTL clkx2, 1:phase ahead 90 degree.	
	-	2	Reserved.	
	SKEW_OTHER[9:8]	1:0	See description of '103288h'.	
45h (10328Ah)	**REG10328A**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	LVDS_LA_OEZ	5	LVDS_LA_OEZ.	
	LVDS_LB_OEZ	4	LVDS_LB_OEZ.	
	CK_OEZ	3	TTL-CK_OEZ.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_OEZ	2	TTL-DE_OEZ.	
	HS_OEZ	1	TTL-HS_OEZ.	
	VS_OEZ	0	TTL-VS_OEZ.	
46h (10328Ch)	**REG10328C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXT_DATA_EN[7:0]	7:0	External test bus enable mode for pair0~13.	
46h (10328Dh)	**REG10328D**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXT_DATA_EN[15:8]	7:0	See description of '10328Ch'.	
47h (10328Eh)	**REG10328E**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXT_DATA_EN[23:16]	7:0	See description of '10328Ch'.	
47h (10328Fh)	**REG10328F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	EXT_DATA_EN[27:24]	3:0	See description of '10328Ch'.	
48h (103290h)	**REG103290**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	INV_CHECKBOARD_LINE_CNT	2	Invert line select for L/R pixel in chalkboard mode.	
	EN_3D_CHECKBOARD	1	Enable checkboard mode.	
	LR_INTERLEAVE_LVDS_EN	0	Enable LR output.	
49h (103292h)	**REG103292**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLX_METHOD[1:0]	7:6	Output format selection for TTL output. 10: 8-bit. 01: 6-bit. Other: 10-bit.	
	ERGX	5	Even channel red and green swap.	
	EGBX	4	Even channel green and blue swap.	
	ORGX	3	Odd channel red and green swap.	
	OGBX	2	Odd channel green and blue swap.	
	-	1:0	Reserved.	
49h (103293h)	**REG103293**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATE_DE	7	Output de gating.	
	EMLX	6	Even LSB and MSB swapping.	
	ERBX	5	Even channel red and blue swap.	
	OMLX	4	Odd LSB and MSB swapping.	
	ORBX	3	Odd channel red and blue swap.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	2	Reserved.	
	WDG	1	Blanking time data become all 1.	
	REVL	0	Reverse output pix.	
4Ah (103294h)	**REG103294**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	TTL_LVDS	6	TTL dual clock output.	
	-	5	Reserved.	
	CLK_INVERT	4	Output clock invert.	
	VS_INVERT	3	Output Vsync invert.	
	DE_INVERT	2	Output DE invert.	
	DUALMODE	1	Dual LVDS channel selection.	
	ABSWITCH	0	Odd -even LVDS channel switch.	
4Ah (103295h)	**REG103295**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTOVS_EARLY	7	Auto Vsync early DE.	
	-	6:5	Reserved.	
	HS_INVERT	4	Hsync invert.	
	HS_REMO	3	GPO or original Hsync selection.	
	-	2:1	Reserved.	
	PUA	0	VSYNC and CLOCK for TTL gating.	
4Bh (103296h)	**REG103296**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MASK_TTL_DUAL	2	Mask dual channel de output.	
	TI_BITMODE[1:0]	1:0	TI bitmode. 0x: 10-bit. 10: 8-bit. 11: 6-bit.	
4Ch (103298h)	**REG103298**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CRC_EN	3	CRC testing enable.	
	CHANNEL_SEL[2:0]	2:0	CRC testing channel selection.	
4Dh (10329Ah)	**REG10329A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_SEL[7:0]	7:0	General purpose output for pair0~13.	
4Dh	**REG10329B**	**7:0**	**Default : 0x00**	**Access : R/W**

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPO_SEL[15:8]	7:0	See description of '10329Ah'.	
4Eh (10329Ch)	**REG10329C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_SEL[23:16]	7:0	See description of '10329Ah'.	
4Eh (10329Dh)	**REG10329D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPO_SEL[27:24]	3:0	See description of '10329Ah'.	
4Fh (10329Eh)	**REG10329E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[7:0]	7:0	General purpose datain for pair0~13.	
4Fh (10329Fh)	**REG10329F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[15:8]	7:0	See description of '10329Eh'.	
50h (1032A0h)	**REG1032A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[23:16]	7:0	See description of '10329Eh'.	
50h (1032A1h)	**REG1032A1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPO_DATAIN[27:24]	3:0	See description of '10329Eh'.	
51h (1032A2h)	**REG1032A2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_OEZ[7:0]	7:0	General purpose pad direction for pair0~13. 0: Output. 1: Input.	
51h (1032A3h)	**REG1032A3**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_OEZ[15:8]	7:0	See description of '1032A2h'.	
52h (1032A4h)	**REG1032A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_OEZ[23:16]	7:0	See description of '1032A2h'.	
52h (1032A5h)	**REG1032A5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPO_OEZ[27:24]	3:0	See description of '1032A2h'.	
53h (1032A7h)	**REG1032A7**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBI_EN	7	VBI information on LVDS enable.	
	-	6:0	Reserved.	
54h (1032A8h)	**REG1032A8**	**7:0**	**Default : 0x00**	**Access : RO**
	CRC_OUT[7:0]	7:0	CRC testing result.	
54h (1032A9h)	**REG1032A9**	**7:0**	**Default : 0x00**	**Access : RO**
	CRC_OUT[15:8]	7:0	See description of '1032A8h'.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (1032AAh)	**REG1032AA**	**7:0**	**Default : 0x00**	**Access : RO**
	MOD_GPI[7:0]	7:0	General purpose input for pair0~13.	
55h (1032ABh)	**REG1032AB**	**7:0**	**Default : 0x00**	**Access : RO**
	MOD_GPI[15:8]	7:0	See description of '1032AAh'.	
56h (1032ACh)	**REG1032AC**	**7:0**	**Default : 0x00**	**Access : RO**
	MOD_GPI[23:16]	7:0	See description of '1032AAh'.	
56h (1032ADh)	**REG1032AD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	MOD_GPI[27:24]	3:0	See description of '1032AAh'.	
5Ah (1032B5h)	**REG1032B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	3D_CH3_EN_A	7	Enable 3d flag on LVDS channel A pair 3.	
	3D_CH4_EN_A	6	Enable 3d flag on LVDS channel A pair 4.	
	3D_CH3_EN_B	5	Enable 3d flag on LVDS channel B pair 3.	
	3D_CH4_EN_B	4	Enable 3d flag on LVDS channel B pair 4.	
	-	3:0	Reserved.	
6Dh (1032DAh)	**REG1032DA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_OUTCONF_CH3[1:0]	7:6	Output mode configuration for channel 3.	
	GCR_OUTCONF_CH2[1:0]	5:4	Output mode configuration for channel 2.	
	GCR_OUTCONF_CH1[1:0]	3:2	Output mode configuration for channel 1.	
	GCR_OUTCONF_CH0[1:0]	1:0	Output mode configuration for channel 0. 2'b00: TTL mode/Standby mode. 2'b01: LVDS data output mode. 2'b10: skew clock output mode. 2'b11: Test clock output mode.	
6Dh (1032DBh)	**REG1032DB**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_OUTCONF_CH7[1:0]	7:6	Output mode configuration for channel 7.	
	GCR_OUTCONF_CH6[1:0]	5:4	Output mode configuration for channel 6.	
	GCR_OUTCONF_CH5[1:0]	3:2	Output mode configuration for channel 5.	
	GCR_OUTCONF_CH4[1:0]	1:0	Output mode configuration for channel 4.	
6Eh (1032DCh)	**REG1032DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_OUTCONF_CH11[1:0]	7:6	Output mode configuration for channel 11.	
	GCR_OUTCONF_CH10[1:0]	5:4	Output mode configuration for channel 10.	
	GCR_OUTCONF_CH9[1:0]	3:2	Output mode configuration for channel 9.	
	GCR_OUTCONF_CH8[1:0]	1:0	Output mode configuration for channel 8.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Eh (1032DDh)	**REG1032DD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GCR_OUTCONF_CH13[1:0]	3:2	Output mode configuration for channel 13.	
	GCR_OUTCONF_CH12[1:0]	1:0	Output mode configuration for channel 12.	
71h (1032E2h)	**REG1032E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_PE_EN_CH[7:0]	7:0	Differential output pre-emphasis enable for channel [13:0].	
71h (1032E3h)	**REG1032E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GCR_PE_EN_CH[13:8]	5:0	See description of '1032E2h'.	
73h (1032E6h)	**REG1032E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_DS_POL_CH[7:0]	7:0	Differential output polarity swap for channel [13:0].	
73h (1032E7h)	**REG1032E7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GCR_DS_POL_CH[13:8]	5:0	See description of '1032E6h'.	
75h (1032EAh)	**REG1032EA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_EN_RINT_CH[7:0]	7:0	Internal resistor enable.	
75h (1032EBh)	**REG1032EB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GCR_EN_RINT_CH[13:8]	5:0	See description of '1032EAh'.	
77h (1032EEh)	**REG1032EE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_CK_PD	4	Part C differential clock enable. This pin is used for CH14~CH21.	
	EN_CK_PC	3	Part C differential clock enable. This pin is used for CH8~CH13.	
	EN_CK_PB	2	Part B differential clock enable. This pin is used for CH2~CH7.	
	EN_CK_PA	1	Part A differential clock enable. This pin is used for CH0~CH1.	
	GCR_CKEN	0	Part A,B,C differential clock enable. This pin is used for CH0~CH13.	
77h (1032EFh)	**REG1032EF**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_SKEWCLK_PATH2	7	Enable skew clock of path2.	

SC4 MOD Register (Bank = 1032, Sub-Bank = 0)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GCR_CKEN_PATH2	6	Enable clock of path2.	
	-	5:2	Reserved.	
	EN_SKEWCLK_PA	1	Part A skew clock enable. This pin is used for CH.	
	EN_SKEWCLK_PB	0	Part B skew clock enable. This pin is used for CH.	
78h (1032F0h)	**REG1032F0**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	PD_IB_MOD	0	Power down mod bias current source.	
78h (1032F1h)	**REG1032F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GCR_REG_REF_SEL	1	Internal regulator reference. 0: AVDD_MOD. 1: DVDD.	
	GCR_EN_REG	0	Enable internal regulator.	
7Dh (1032FAh)	**REG1032FA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_CAL_EN	7	Enable calibration function.	
	-	6:4	Reserved.	
	GCR_CAL_SRC[1:0]	3:2	Select calibration source pair. 0: CH2, 1: CH6, 2: CH8, 3: CH12.	
	GCR_CAL_LEVEL[1:0]	1:0	Select calibration target voltage. 00: 250mV, 01:350mV, 10: 300mV, 11: 200mV.	
7Dh (1032FBh)	**REG1032FB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	C_CAL_OUT	0	Calibration result output. 1: Higher than target. 0: Lower than target.	

PM_SLEEP Register (Bank = 0E)

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (0E10h)	**REG0E10**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WK_IRQ_MASK[7:0]	7:0	IRQ mask for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
08h (0E11h)	**REG0E11**	**7:0**	**Default : 0x00**	**Access : R/W**
	WK_IRQ_FORCE[7:0]	7:0	IRQ force for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
09h (0E12h)	**REG0E12**	**7:0**	**Default : 0x00**	**Access : R/W**
	WK_IRQ_POL[7:0]	7:0	IRQ polarity for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
09h (0E13h)	**REG0E13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEEP_SLEEP	7	1: Deep sleep (using internal crystal). 0: Sleep (using external crystal).	
	WAKEUP_RST_51_EN	6	1: Wake up 8051 from address 0x0. 0: Wake up 8051 from last address.	
	WAKEUP_RST_CHIP_TOP_EN	5	Reset CHIP_TOP w/s 512 cycles of CLK_PM_SLEEP when waking up.	

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HK51_UART0_EN	4	Select UART source via PAD_DDCA. 1: HK MCU51 UART0. 0: DIG_MUX (REG_UART_SEL0).	
	UART_RX_ENABLE	3	1: Enable UART RX via PAD_DDCA for DIG_MUX (REG_UART_SEL0).	
	-	2:0	Reserved.	
0Eh (0E1Ch)	**REG0E1C**	**7:0**	**Default : 0x00**	**Access : RO**
	WK_IRQ_FINAL_STATUS[7:0]	7:0	IRQ final status for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
0Eh (0E1Dh)	**REG0E1D**	**7:0**	**Default : 0x00**	**Access : RO**
	WK_IRQ_RAW_STATUS[7:0]	7:0	IRQ raw status for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
12h (0E24h)	**REG0E24**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_LOCK[7:0]	7:0	The password to control the GPIO that is used for controlling external LDO (16'hbabe). The password to enter sleep mode (16'hbabe).	
12h (0E25h)	**REG0E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_LOCK[15:8]	7:0	See description of '0E24h'.	
13h (0E26h)	**REG0E26**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_LOCK2[7:0]	7:0	The password to control isolation & reset die-domain (16'hbabe).	
13h (0E27h)	**REG0E27**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_LOCK2[15:8]	7:0	See description of '0E26h'.	

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ch (0E38h)	**REG0E38**	**7:0**	**Default : 0x00**	**Access : R/W**
	AV_LNK_IS_GPIO	7	'd0: Normal use. 'd1: PAD_AV_LNK is used as GPIO.	
	CEC_IS_GPIO	6	'd0: Normal use. 'd1: PAD_CEC is used as GPIO.	
	-	5	Reserved.	
	IR_IS_GPIO	4	'd0: Normal use. 'd1: PAD_IRIN is used as GPIO.	
	-	3:0	Reserved.	
20h (0E40h)	**REG0E40**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_MCU_CLK	7	Switch CLK MCU by glitch-free clock switch (between CLK_MCU_P and CLK_EXT_XTALI_BUF).	
	-	6	Reserved.	
	CKG_MCU[5:0]	5:0	Clock selection for CLK MCU. [0]: Gate. [1]: Invert. [5:2]: See the following: 'd0: 170 MHz. 'd1: 160MHz. 'd2: 144MHz. 'd3: 123MHz. 'd4: 108MHz. 'd5: MEMPLL_CLK_BUF. 'd6: MEMPLL_CLK_BUF /2. 'd7: CLK_INT_XTALI_BUF. 'd8: CLK_EXT_XTALI_BUF /8. 'd9: 24MHz. 'd10: CLK_INT_XTALI_BUF divided to 1MHz. 'd11: CLK_EXT_XTALI_BUF /16. 'd12: CLK_EXT_XTALI_BUF /2. 'd13: CLK_EXT_XTALI_BUF /4. 'd14: 216MHz. 'd15: 192MHz.	
21h (0E42h)	**REG0E42**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_IR[2:0]	7:5	Clock selection for CLK_IR. [0]: Gate. [1]: Invert. [4:2]: See the following:	

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
	CKG_DDC[4:0]	4:0	Clock selection for CLK_DDC. [0]: Gate. [1]: Invert. [4:2]: See the following: 'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
21h (0E43h)	**REG0E43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_IR[4:3]	1:0	See description of '0E42h'.	
22h (0E44h)	**REG0E44**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_SAR[2:0]	7:5	Clock selection for CLK_SAR. [0]: Gate. [1]: Invert. [4:2]: See the following: 'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
	CKG_RTC[4:0]	4:0	Clock selection for CLK_RTC. [0]: Gate. [1]: Invert.	

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[4:2]: See the following: 'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
22h (0E45h)	**REG0E45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKG_PM_SLEEP[4:0]	6:2	Clock selection for CLK_PM_SLEEP (cannot be either inversed or gated). [4:2]: See the following: 'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
	CKG_SAR[4:3]	1:0	See description of '0E44h'.	
23h (0E46h)	**REG0E46**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_CEC[3:0]	3:0	Clock selection for CLK_CEC. [0]: Gate. [1]: Invert. [3:2]: See the following: 'd0: CLK_EXT_XTALI_BUF divided to 1MHz. 'd1: CLK_INT_XTALI_BUF /4. 'd2: CLK_INT_XTALI_BUF. 'd3: 0.	
27h (0E4Eh)	**REG0E4E**	**7:0**	**Default : 0x0F**	**Access : R/W**
	HOTPLUG_OUT[3:0]	7:4	Hot plug out. [0]: Hot plug A. [1]: Hot plug B. [2]: Hot plug C.	

PM_SLEEP Register (Bank = 0E)

Index (Absolute)	Mnemonic	Bit	Description	
			[3]: Hot plug D.	
	HOTPLUG_OEN[3:0]	3:0	Hot plug OEN. [0]: Hot plug A. [1]: Hot plug B. [2]: Hot plug C. [3]: Hot plug D.	
27h (0E4Fh)	**REG0E4F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	HOTPLUG_IN[3:0]	3:0	Hot plug in. [0]: Hot plug A. [1]: Hot plug B. [2]: Hot plug C. [3]: Hot plug D.	
30h (0E60h)	**REG0E60**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	EXT_XTALI_SEL[1:0]	5:4	External crystal settings (driving strength).	
	-	3	Reserved.	
	INT_XTALI_DEGLITCH[2:0]	2:0	Test bits for internal crystal clock.	
30h (0E61h)	**REG0E61**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7	Reserved.	
	EXT_XTALI_AMP_GAIN[1:0]	6:5	External crystal amplitude gain.	
	EXT_XTALI_FRSEL	4	External crystal frequency selection.	
	INT_XTALI_FREQ_TUNE[3:0]	3:0	Frequency tune for internal clock.	
31h (0E63h)	**REG0E63**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC1_SW_RST	7	Software reset (active high) for RTC1.	
	RTC0_SW_RST	6	Software reset (active high) for RTC0.	
	-	5	Reserved.	
	CEC_SW_RST	4	Software reset (active high) for CEC.	
	AV_LNK_SW_RST	3	Software reset (active high) for AV_LNK_TOP.	
	SAR_SW_RST	2	Software reset (active high) for SAR_TOP.	
	-	1:0	Reserved.	
32h (0E64h)	**REG0E64**	**7:0**	**Default : 0x00**	**Access : R/W**
	XTAL_OFF_KEY[7:0]	7:0	Key to turn off external crystal (32'h9f8e9f8e).	
32h	**REG0E65**	**7:0**	**Default : 0x00**	**Access : R/W**

PM_SLEEP Register (Bank = 0E)

Index (Absolute)	Mnemonic	Bit	Description	
	XTAL_OFF_KEY[15:8]	7:0	See description of '0E64h'.	
33h (0E66h)	**REG0E66**	**7:0**	**Default : 0x00**	**Access : R/W**
	XTAL_OFF_KEY[23:16]	7:0	See description of '0E64h'.	
33h (0E67h)	**REG0E67**	**7:0**	**Default : 0x00**	**Access : R/W**
	XTAL_OFF_KEY[31:24]	7:0	See description of '0E64h'.	
35h (0E6Bh)	**REG0E6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TESTBUS_SW[1:0]	7:6	Testbus switch.	
	ISO_CONTROL[1:0]	5:4	[0]: Isolation control selection. 0: By PM_ATOP. 1: By software. [1]: Isolation control. 0: Not isolate. 1: Isolate.	
	UART_IS_GPIO[3:0]	3:0	[0]: Switch GPIO_PM[5] to HK51's UART_RX1 and GPIO_PM[8] to HK51's UART_TX1. [1]: Switch GPIO_PM[5] to HK51's UART_RX1 and GPIO_PM[1] to HK51's UART_TX1. [3:2]: Reserved.	
50h (0EA0h)	**REG0EA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[7:0]	7:0	Key to off RIU_CKSUM_PROT (h51685168).	
50h (0EA1h)	**REG0EA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[15:8]	7:0	See description of '0EA0h'.	
51h (0EA2h)	**REG0EA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[23:16]	7:0	See description of '0EA0h'.	
51h (0EA3h)	**REG0EA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[31:24]	7:0	See description of '0EA0h'.	
60h (0EC0h)	**REG0EC0**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	BOND_STAT[1:0]	1:0	Bonding status. [0]: Clock selection. [1]: Security.	
61h (0EC2h)	**REG0EC2**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	CHIP_TOP_POWERGOOD_DEGLITCH	3	DVDD_CORE_PWRGD after de-glitch and ISO_CONTROL.	

PM_SLEEP Register (Bank = 0E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	CHIP_TOP_POWERGOOD[2:0]	2:0	CHIP_TOP'S powergood from PM_ATOP. [0]: NODIE_PWRGD. [1]: DVDD_CORE_PWRGD. [2]: VD33_SHUTDN_PWRGD.

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
09/03/2012		Created first version.