项目名称：P60-X9 V6.0　　开案日期：2012.8.14

开案规格：

全功能版本：　名称　　料号

规格

公板版本：　名称　　料号

规格

版本更新记录

版本	更新记录	修订	审核	日期
P60-X9 V6.1 20130117				

Power Config:

Date	Modify Number	Modify By

深圳市鼎科实业有限公司

SheetName: 01.Page Cover

Size: A3　Document Number: P82-69ZR V6.0　Rev: A

Modify Date: Wednesday, March 18, 2015　Designed By: chuizi　Sheet 1 of 10

GPIO CONFIG

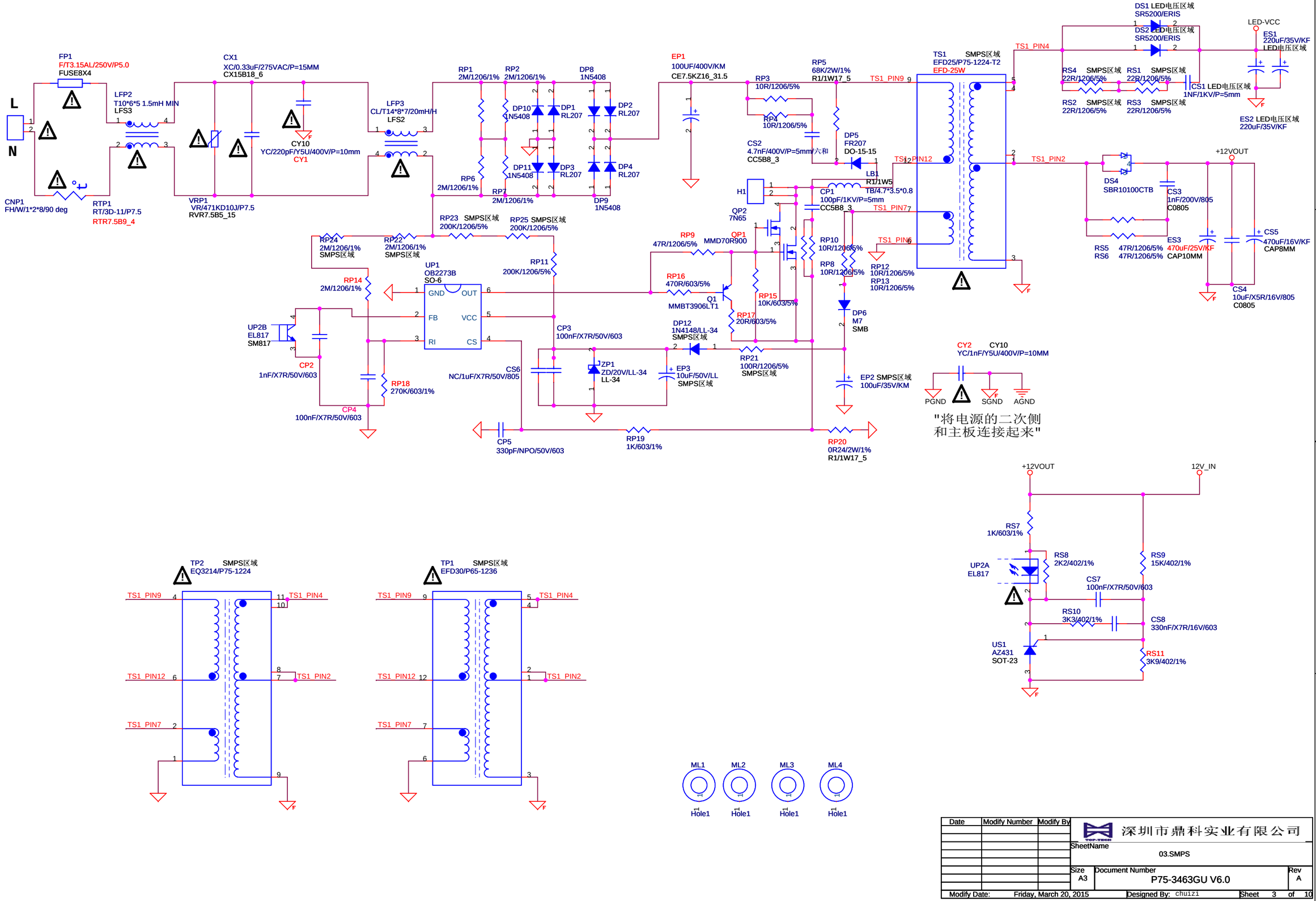
Date	Modify Number	Modify By

深圳市鼎科实业有限公司

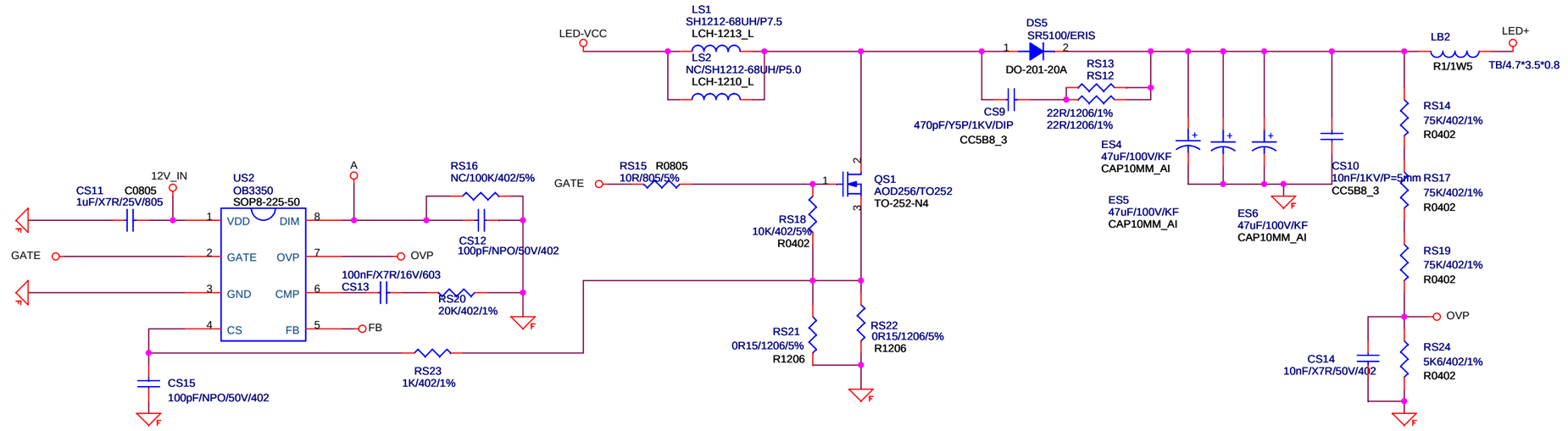
SheetName: 02.GPIO CONFIG

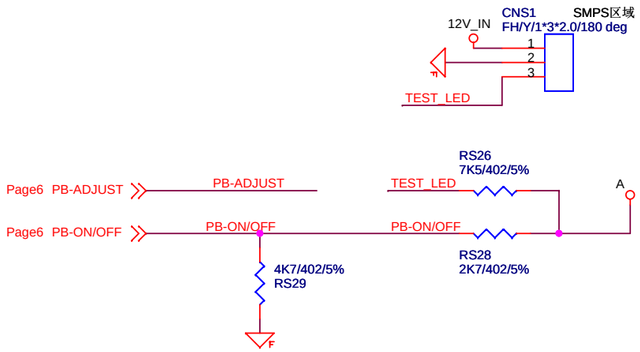
Size	Document Number	Rev
A3	P82-69ZR V6.0	A

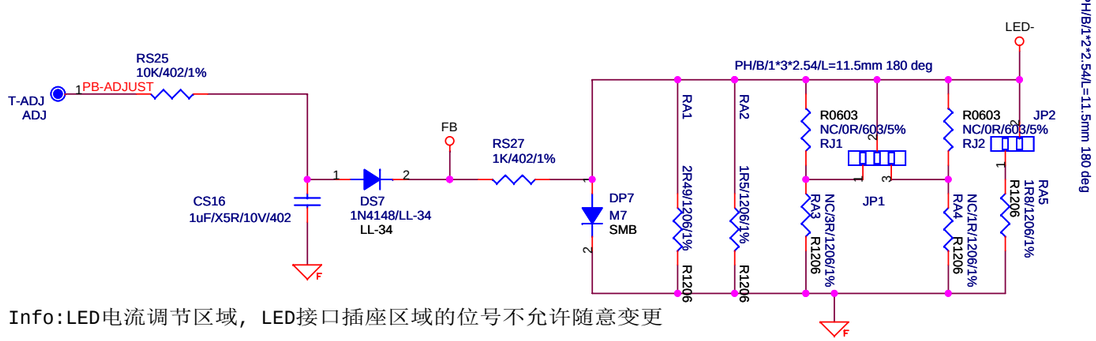
Modify Date: Friday, February 06, 2015 | Designed By: chuizi | Sheet 2 of 10



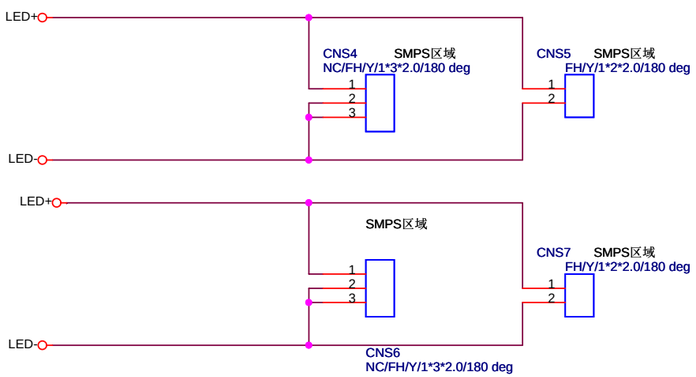
Date	Modify Number	Modify By	
			深圳市鼎科实业有限公司
			SheetName: 03.SMPS
			Size: A3 / Document Number: P75-3463GU V6.0 / Rev: A
Modify Date: Friday, March 20, 2015			Designed By: chuizi / Sheet 3 of 10

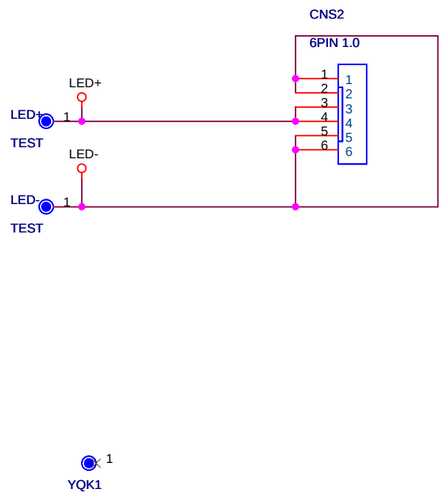


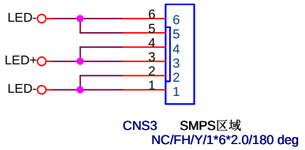




Info:LED电流调节区域，LED接口插座区域的位号不允许随意变更







Date	Modify Number	Modify By

深圳市鼎科实业有限公司

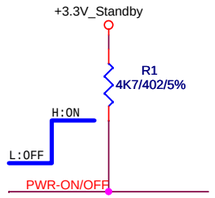
SheetName: 04.LED Power

Size: A3 | Document Number: P75-3463GU V6.0 | Rev: A

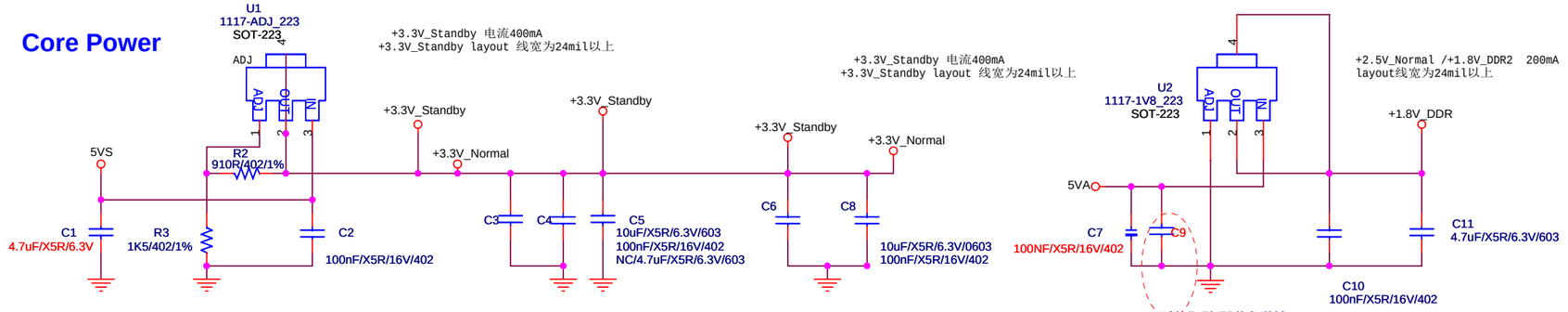
Modify Date: Friday, March 20, 2015 | Designed By: | Sheet 4 of 10

Power Input

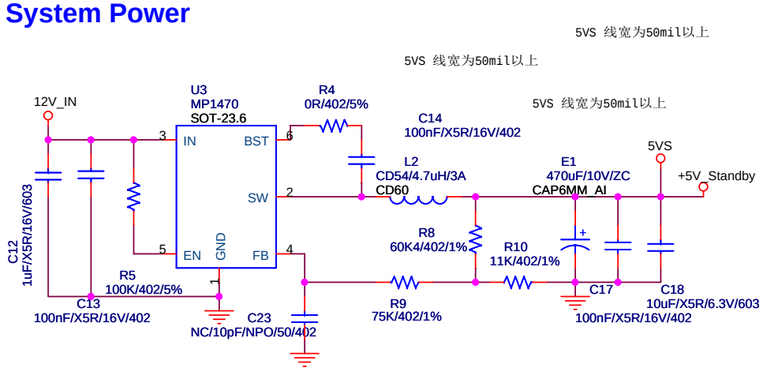
Standby controler



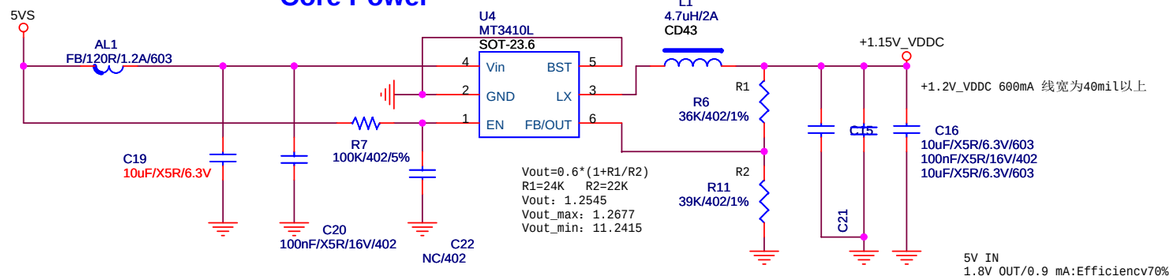
Core Power



System Power

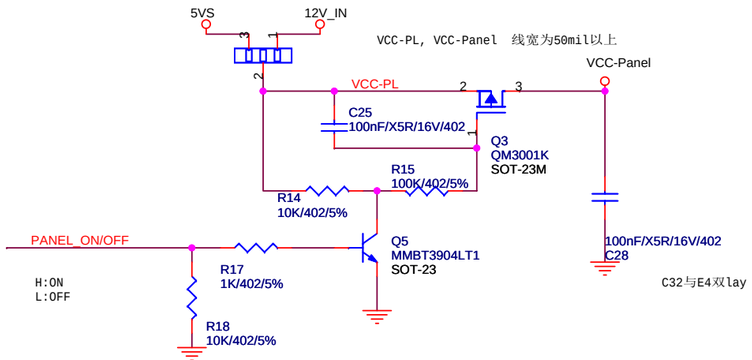


Core Power



PANEL POWER

JP3
PH/B/1*3*2.54/L=11.5mm 180 deg
JP3/2.54

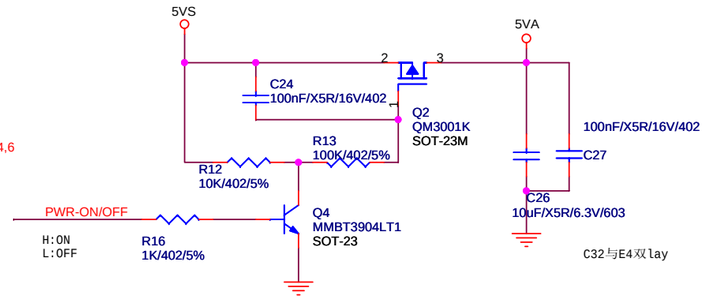


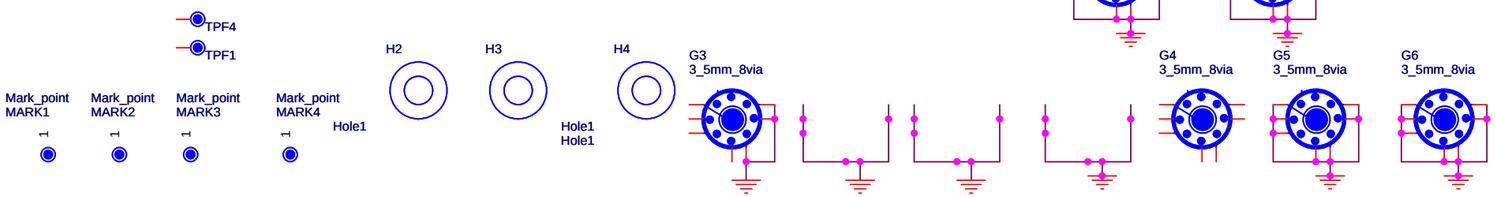
Inverter controler

VBL_CTRL	Panel Backlight
H	OFF
L	ON

VBL_CTRL — PB-ON/OFF — PB-ON/OFF Page4,6

BRI_ADJ-PWM0 — PB-ADJUST
BRI_ADJ-PWM0,PB-ADJUST 网络要包地，线宽8mil





VBL_CTRL — VBL_CTRL Page4,6
BRI_ADJ-PWM0 — BRI_ADJ-PWM0 Page4,6
PANEL_ON/OFF — PANEL_ON/OFF Page6
PWR-ON/OFF — PWR-ON/OFF Page6
PB-ADJUST — PB-ADJUST Page4,6

Date	Modify Number	Modify By

深圳市鼎科实业有限公司

SheetName: 05.System Power

Size: A3 | Document Number: P75-3463GU V6.0 | Rev: A

Modify Date: Wednesday, March 18, 2015 | Designed By: suncheng | Sheet 5 of 10

MHL Port

Page8 HDMI1_RX2P → HDMI1_RX2P
Page8 HDMI1_RX2N → HDMI1_RX2N
Page8 HDMI1_RX1P → HDMI1_RX1P
Page8 HDMI1_RX1N → HDMI1_RX1N
Page8 HDMI1_RX0P → HDMI1_RX0P
Page8 HDMI1_RX0N → HDMI1_RX0N
Page8 HDMI1_CLKP → HDMI1_CLKP
Page8 HDMI1_CLKN → HDMI1_CLKN
Page8 HDMI1_SDA → HDMI1_SDA
Page8 HDMI1_SCL → HDMI1_SCL
Page8 HDMI1_HPDIN → HDMI1_HPDIN

HDMI0-RX2P → HDMI0_RX2P
HDMI0-RX2N → HDMI0_RX2N
HDMI0-RX1P → HDMI0_RX1P
HDMI0-RX1N → HDMI0_RX1N
HDMI0-RX0P → HDMI0_RX0P
HDMI0-RX0N → HDMI0_RX0N
HDMI0-CLKP → HDMI0_CLKP
HDMI0-CLKN → HDMI0_CLKN
HDMI0-SDA → HDMI0_SDA
HDMI0-SCL → HDMI0_SCL
HDMI0_HPDIN → HDMI0_HPDIN

Page8 HDMI2_RX2P → HDMI2_RX2P
Page8 HDMI2_RX2N → HDMI2_RX2N
Page8 HDMI2_RX1P → HDMI2_RX1P
Page8 HDMI2_RX1N → HDMI2_RX1N
Page8 HDMI2_RX0P → HDMI2_RX0P
Page8 HDMI2_RX0N → HDMI2_RX0N
Page8 HDMI2_CLKP → HDMI2_CLKP
Page8 HDMI2_CLKN → HDMI2_CLKN
Page8 HDMI2_SDA → HDMI2_SDA
Page8 HDMI2_SCL → HDMI2_SCL
Page8 HDMI2_HPDIN → HDMI2_HPDIN

Page8 MHL_CABLE_DET → MHL_CABLE_DET
Page8 HDMI_CEC → HDMI_CEC
Page8 HDMI1_DEC → HDMI1_DEC
Page7,8 ARC → ARC
C32 33PF/NPO/50V/402

VGA

Page7 VGA_HS → HSYNC0
Page7 RGB0_Pb+ → RGB0_Pb+ → C33 47nF/X5R/16V/402 → BIN0
Page7 RGB0_Y+ → RGB0_Y+ → C34 47nF/X5R/16V/402 → GIN0P
R29 68R/402/5% C35 47nF/X5R/16V/402 GIN0M
Page7 RGB0_Pr+ → RGB0_Pr+ → C37 47nF/X5R/16V/402 → RIN0
Page7 VGA_VS → VSYNC0
Page7 PC-Lin → PC-Lin → C38 1uF/X5R/10V/402 → AUL3
PC-Rin → PC-Rin → C36 1uF/X5R/10V/402 → AUR3

YPbPr Input

Page7 RGB2-HDTV_BIN → RGB2-HDTV_BIN → C39 47nF/X5R/16V/402 → BIN2
Page7 RGB2-HDTV_GIN → RGB2-HDTV_GIN → C40 47nF/X5R/16V/402 → GIN2P
R31 68R/402/5% C41 47nF/X5R/16V/402 GIN2M
Page7 RGB2-HDTV_RIN → RGB2-HDTV_RIN → C42 47nF/X5R/16V/402 → RIN2

CVBS VCOM

R32 180R/402/5% C43 47nF/X5R/16V/402 VCOM0

AV Input

Page7 CVBSIN → CVBSIN → C44 47nF/X5R/16V/402 → CVBS0
Page7 AV1-Lin → AV1-Lin → C45 1uF/X5R/10V/402 → AUL4
Page7 AV1-Rin → AV1-Rin → C46 1uF/X5R/10V/402 → AUR4

Page7 CVBSOUT → CVBS_OUT0

CVBS & SPDIF &IR OUT

Page7 AV-AUOUTL → AV-AUOUTL
Page7 AV-AUOUTR → AV-AUOUTR

AMP INPUT

Page10 AMP_AUOUTR0 → AMP_AUOUTR0 → R33 200K/402/5% → AMP-AUOUTR
C47 10nF/NPO/50V/402
Page10 AMP-MUTE → AMP-MUTE
Page10 AMP_AUOUTL0 → AMP_AUOUTL0 → R37 200K/402/5% → AMP-AUOUTL
C50
C51 10nF/NPO/50V/402
10nF/NPO/50V/402

Debug port

5VS
R46 4K7/402/5%
R47 4K7/402/5%
Page7 UART-RX → DDCA_CK R49 68R/402/5% → UART_RX
Page7 UART-TX → DDCA_DA R51 68R/402/5% → UART_TX

USB Interface

Page8 USB0_DP → USB0_DP
Page8 USB0_DM → USB0_DM
Page8 USB1_DP → USB1_DP
Page8 USB1_DM → USB1_DM

Audio REF

AUVRM
AUVAG
C48 100nF/X5R/16V/402
C49 10uF/X5R/6.3V/603
L3 FB/120R/0.2A/402
靠近主改片放置，并且走线尽量宽

Tuner Interface

+3.3V_TU
10K/402/5% R52 Tuner区域
Page9 TAGC → TAGC
0R/402/5% R53 → IFAGC
Page9 VIFP → VIFP → IFM
Page9 VIFM → VIFM → IFP
Tuner区域
靠近主芯片放置
C64 Tuner区域
22nF/X7R/25V/402

VIF IN

GPIO

Page9 SYS_SCL → SYS_SCL → M-SCL
Page9 SYS_SDA → SYS_SDA → M-SDA
Page9 AIR-CABLE → AIR-CABLE
Page4 BRI_ADJ-PWM0 → BRI_ADJ PWM0
Page5 PWR-ON/OFF → PWR_ON/OFF
Page4 VBL_CTRL → VBL_CTRL
Page5 PANEL_ON/OFF → PANEL_ON/OFF

System

X2
33pF/NPO/50V/402
Y1
24MHz/CL=20pF/20PPM
C30 33pF/NPO/50V/402
XTALI
R20
1M/402/5%
R21
0R/402/5%
XTALO
NOTE:晶体频偏需要小于30PPM
Page9 24MH_IN → R24 200R/402/5%

System RESET

+3.3V_Standby
U6
810 SOT-23
VCC
RESET
GND
R22
System_RST
R23 47K/402/5%
1K/402/5%

+3.3V_Standby
R109 10K/402/5%
R19 10K/402/5%
U6
VDD CE#
HOLD# SO
SCK WP#
SI VSS
SPI_CLK
SPI_DI
SPI_CSN
SPI_DO
SPI_WP
C31
CD/MX25L3206E
100nF/X5R/16V/402

软件必须要做写保护

CHIP_CONFIG

2b 00/01/10:Boot from SPI
+3.3V_Normal
R25 4K7/402/5%
R26 NC/4K7/402/5%
PWM1
PWM0
R27 NC/4K7/402/5%
R28 4.7K/402/5%
C95 10nF/NPO/50V/402

{PAD_PWM1, PAD_PWM0}

HDMI Interface

MHL Port

MSD3463GU

U7

AVDD5V_MHL
AVDDL_DVI
AVDD_DDR_CMD
AVDD_DDR_DATA
AVDD_MOD1
DVDD_DDR

E-PAD GND RXCP_B RXCN_B RXP2_D RXN2_D RX1P_D RX1N_D RX0P_D RX0N_D RXCP_D RXCN_D AVDDL_DVI_VDDC ARC AVDD_5V HOTPLUG_A HOTPLUG_B HOTPLUG_D CEC GND_EFUSE VDDIO_DRAM VDDIO_DATA AVDD_MOD DVDD_DDR_DATA SAR1 SAR0 MHL_DET DDCA_CK DDCA_DA SPI_DO SPI_CLK SPI_DI SPI_CZ PWM1

HDMI1_CLKP HDMI1_CLKN HDMI0_RX2P HDMI0_RX2N HDMI0_RX1P HDMI0_RX1N HDMI0_RX0P HDMI0_RX0N HDMI0_CLKP HDMI0_CLKN ARC HDMI2_HPDIN HDMI1_HPDIN HDMI0_HPDIN HDMI_CEC VBL_CTRL KEY0_IN MHL_CABLE_DET UART_RX UART_TX SPI_CSN PANEL_ON/OFF PWM1

HDMI1_RX0N 1 → RX0N_B
HDMI1_RX0P 2 → RX0P_B
HDMI1_RX1N 3 → RX1N_B
HDMI1_RX1P 4 → RX1P_B
HDMI1_RX2N 5 → RX2N_B
HDMI1_RX2P 6 → RX2P_B
AVDD_MOD → 7 AVDD_MOD
HDMI2_CLKN 8 → RXCN_A
HDMI2_CLKP 9 → RXCP_A
HDMI2_RX0N 10 → RX0N_A
HDMI2_RX0P 11 → RX0P_A
HDMI2_RX1N 12 → RX1N_A
HDMI2_RX1P 13 → RX1P_A
HDMI2_RX2N 14 → RX2N_A
HDMI2_RX2P 15 → RX2P_A
VGA_HS 16 → HSYNC0
BIN0 17 → BIN0P
GIN0P 18 → GIN0P
GIN0M 19 → GIN0M
RIN0 20 → RIN0P
VGA_VS 21 → VSYNC0
AVDD3P3_ADC → 22 AVDD3P3_ADC
BIN2 23 → BIN2P
GIN2P 24 → GIN2P
GIN2M 25 → GIN2M
RIN2 26 → RIN2P
CVBS0 27 → CVBS0
VCOM0 28 → VCOM
CVBS_OUT0 29 → CVBS_OUT1
VDDC 30 → VDDC
AVDD_AU33 31 → AVDD_AU33
AUVRM 32 → AUVRM

PWM0 96 → BRI_ADJ PWM0
RESET 95 → System_RST
IRIN 94 → IRIN
GPIO0 93 → PWR_ON/OFF
GPIO2/MHL_VBUS 92 → MHL-EN
VDDC 91 → VDDC
AVDD_MOD 90 → AVDD_MOD
R_ODD[1]/LVB0- 89 → RXO0-
R_ODD[0]/LVB0+ 88 → RXO0+
G_ODD[7]/LVB1- 87 → RXO1-
G_ODD[6]/LVB1+ 86 → RXO1+
G_ODD[5]/LVB2- 85 → RXO2-
G_ODD[4]/LVB2+ 84 → RXO2+
G_ODD[3]/LVB3- 83 → RXO3-
G_ODD[2]/LVB3+ 82 → RXO3+
G_ODD[1]/LVA0- 81 → RXE0-
G_ODD[0]/LVA0+ 80 → RXE0+
B_ODD[7]/LVA1- 79 → RXE1-
B_ODD[6]/LVA1+ 78 → RXE1+
B_ODD[5]/LVA2- 77 → RXE2-
B_ODD[4]/LVA2+ 76 → RXE2+
B_ODD[3]/LVACLK- 75 → RXEC-
B_ODD[2]/LVACLK+ 74 → RXEC+
B_ODD[1]/LVA3- 73 → RXE3-
B_ODD[0]/LVA3+ 72 → RXE3+
DP_P0 71 → USB0_DP
DM_P0 70 → USB0_DM
DP_P1 69 → USB1_DP
DM_P1 68 → USB1_DM
TS0_D0/DDCDD_CLK 67 → HDMI0_SCL
TS0_D1/DDCDD_DAT 66 → HDMI0_SDA
I2S_OUT_SD/GPIO104 65 → HDMI1_DEC

AUVAG AUR3 AUL3 AUR4 AUL4 AUL5 LINEOUTR3 LINEOUTL3 LINEOUTR2 LINEOUTL2 AVDD3P3_DADC IFAGC VIFP VIFM AVDD3P3_DMPLL XIN XOUT VDDC GPIO44/TX1 GPIO45/RX1 VDDIO_CMD VDDC AVDD_MOD DDCDA_CK/(PCM_D4)/EJ_TCK DDCDA_DA/(PCM_D5)/EJ_TDO DDCDB_CLK/(PCM_D6)/EJ_TDI DDCDB_DAT/(PCM_D7)/EJ_TRST_N GPIO118/EJ_TMS GPIO111/I2S OUT MCK GPIO110/I2S OUT BCK GPIO109/I2S_OUT_WS

AUVAG AUR3 AUL3 AUR4 AUL4 AMP-AUOUTR AMP-AUOUTL AV-AUOUTR AV-AUOUTL IFAGC VIFP VIFM XTALI XTALO M-SDA M-SCL HDMI2_SCL HDMI2_SDA HDMI1_SCL HDMI1_SDA AMP-MUTE

AIR-CABLE
I2S_OUT_MCK
AVDD_DADC
AVDD_DMPLL
VDDC
AVDD_MOD
VDDC
AVDD_DDR_CMD

R48 200R/402/5% LED_G
R108 10K/402/5%
C53 C54 C55 100nF/X5R/16V/402 ×3

LED

+3.3V_Standby
R117 NC/1K5/402/5%
R38 2K7/402/5%
R118 NC/10K/402/5%
NC/MMBT3906LT1
Q8
I2S_OUT_MCK
LED_R
R34 1K5/402/5%
R39 2K7/402/1%
R44 1K/402/5%
KEY0_IN

+3.3V_Standby
R35 430R/402/1% SOURCE
R36 3K9/402/1% CH+
R40 2K/402/1% MENU
R41 0R/402/1% ON/OFF
R42 18K/402/1% VOL-
R43 1K/402/1% VOL+
R45 7K5/402/1% CH-
ESD1 NC/ESD
C52 10nF/X7R/50V/402

IR&KEYB

CN2
FH/Y/1*13*2.0/180 deg
GPIO
ON/OFF
MENU
VOL-
VOL+
CH-
CH+
SOURCE
IR_IN
LED_G
LED_R
IR_VCC
R50 NC/100R/402/5%
MHL-EN

LVDS CONNECTOR

VCC-Panel
R30 47K/402/5%
GND
CN1
TPF2
TPF3
RXO0- RXO1- RXO2- RXEC- RXO3- RXE0- RXE1- RXE2- RXEC- RXE3-
RXO0+ RXO1+ RXO2+ RXO3+ RXE0+ RXE1+ RXE2+ RXEC+ RXE3+
GND GND
PH/B/2*17*2.0/180 deg
CON30A/2.0

GND
33pF/NPO/50V/402 C56
R54 100R/402/5% IRIN
5VS
R55 4K7/402/5%
ESD2 NC/ESD
C65 1uF/X5R/10V/402
GND

DDR power

+1.8V_DDR
AVDD_DDR_CMD
AVDD_DDR_DATA
C58 C60
L4 FB/120R/0.2A/402
100nF/X5R/16V/402 ×2
C57 4.7uF/X5R/6.3V/603
100nF/X5R/16V/402
C59

+3.3V_Standby AVDD_DMPLL
L5 FB/120R/0.2A/402
Pin51
C61 100nF/X5R/16V/402

+3.3V_Standby AVDD_DADC
L6 FB/120R/0.2A/402
C62 100nF/X5R/16V/402

+3.3V_Standby AVDD_AU33
L7 FB/120R/0.2A/402
C63 100nF/X5R/16V/402
Pin34

Normal Power 1.2V

+1.15V_VDDC VDDC AVDDL_DVI DVDD_DDR
L8
C66 4.7uF/X5R/6.3V/603
C67 C68 C69 C70 C71 C72
0R/402/5%
100nF/X5R/16V/402 ×6

Normal Power 3.3V

+3.3V_Standby
AVDD_MOD
AVDD3P3_ADC
AVDD_MOD1
C75 C77
C73 NC/4.7uF/X5R/6.3V/603
C74 C76 C78
100nF/X5R/16V/402 ×4

Date	Modify Number	Modify By

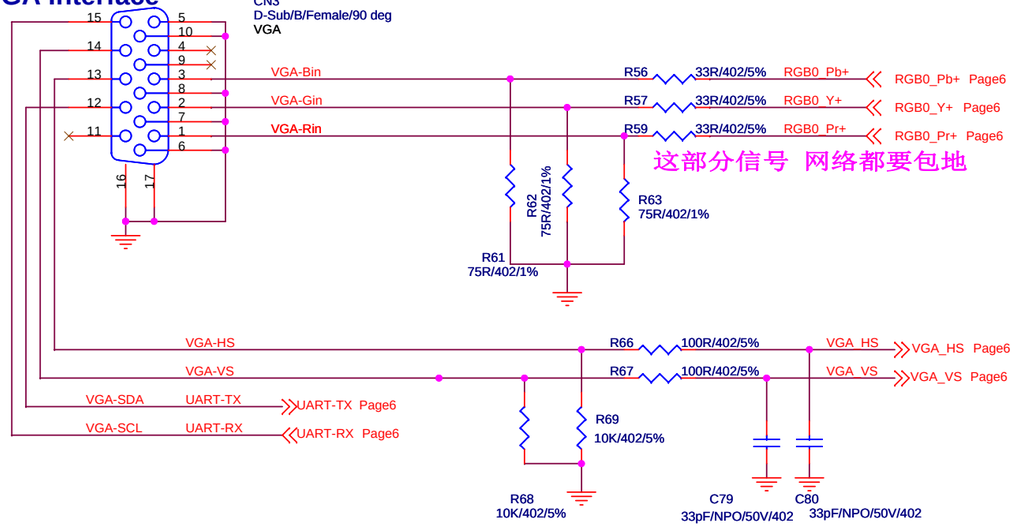
深圳市鼎科实业有限公司

SheetName: 06.MSD3463GU System

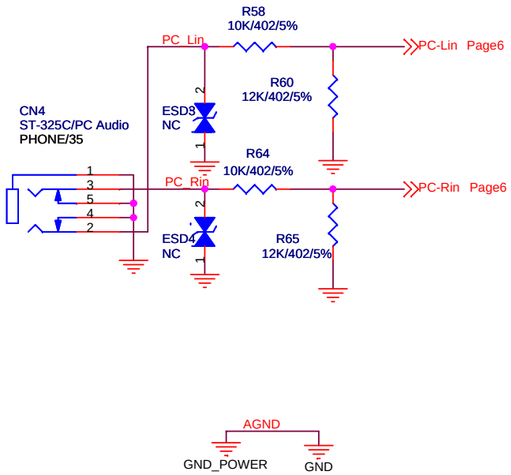
Size: Custom | Document Number: P75-3463GU V6.0 | Rev: A

Modify Date: Monday, March 23, 2015 | Designed By: chuizi | Sheet 6 of 10

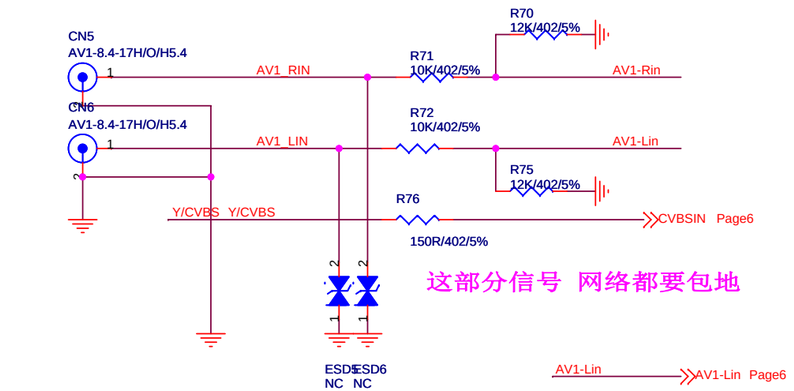
VGA Interface



PC Audio In

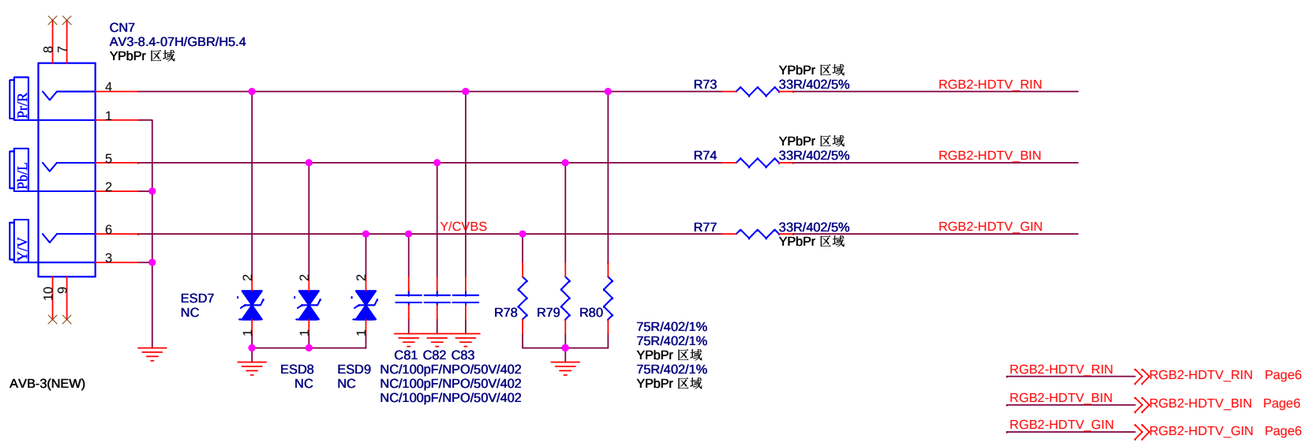


AV1 Interface



YPBPR_IN Interface

这部分信号 网络都要包地



CVBS & SPDIF OUT

Date	Modify Number	Modify By

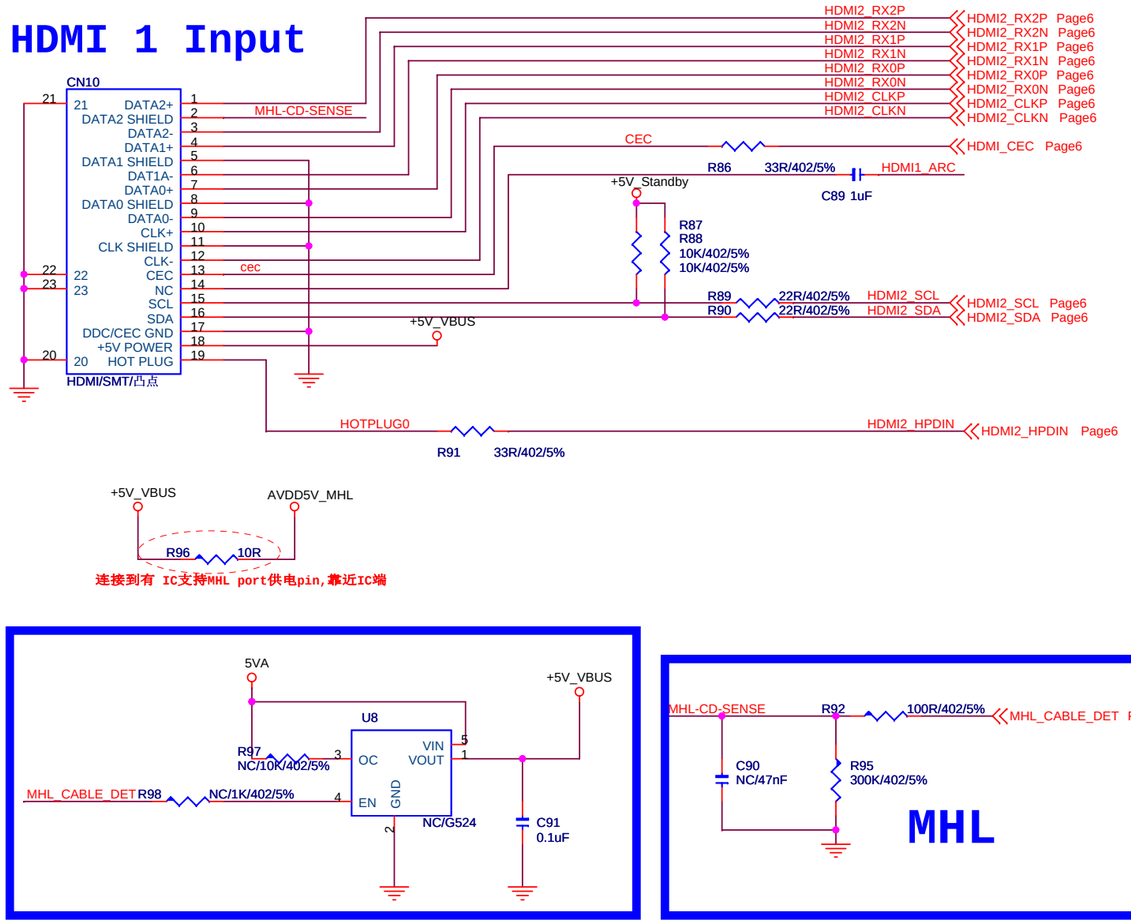
深圳市鼎科实业有限公司

SheetName: 07.Singnal Interface

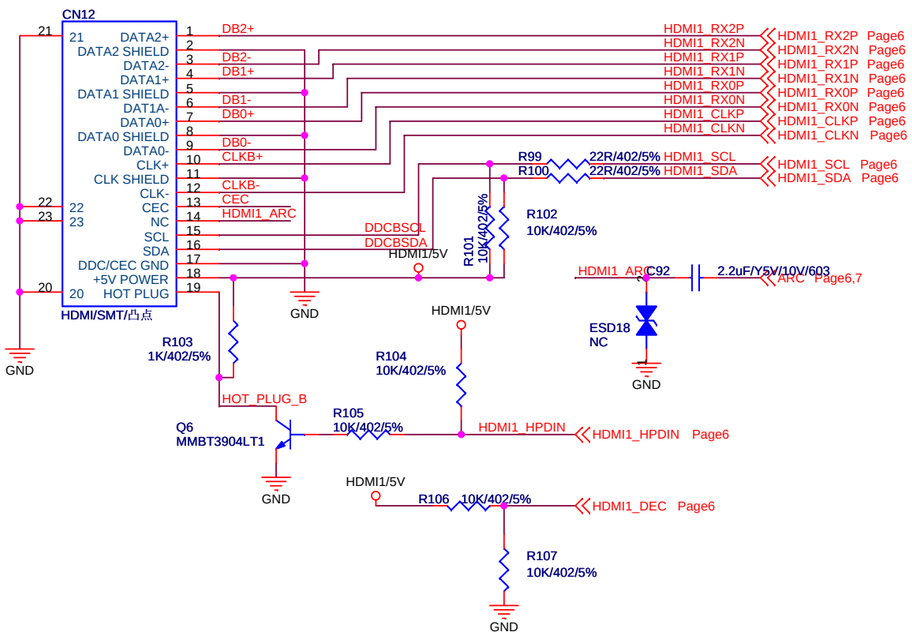
Size	Document Number	Rev
A3	P75-3463GU V6.0	A

Modify Date: Monday, March 23, 2015 | Designed By: suncheng | Sheet 7 of 10

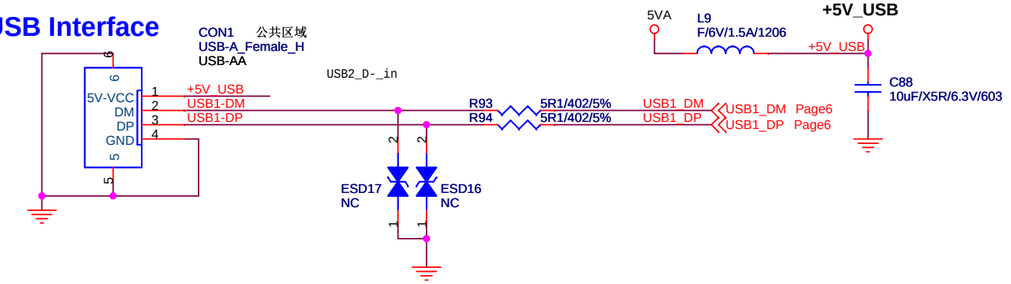
HDMI 1 Input

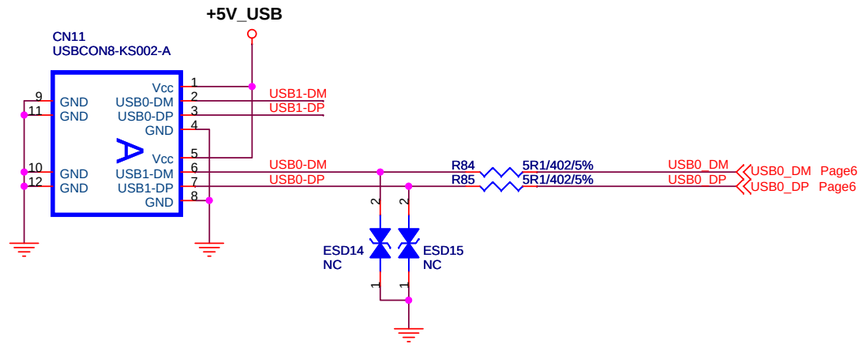


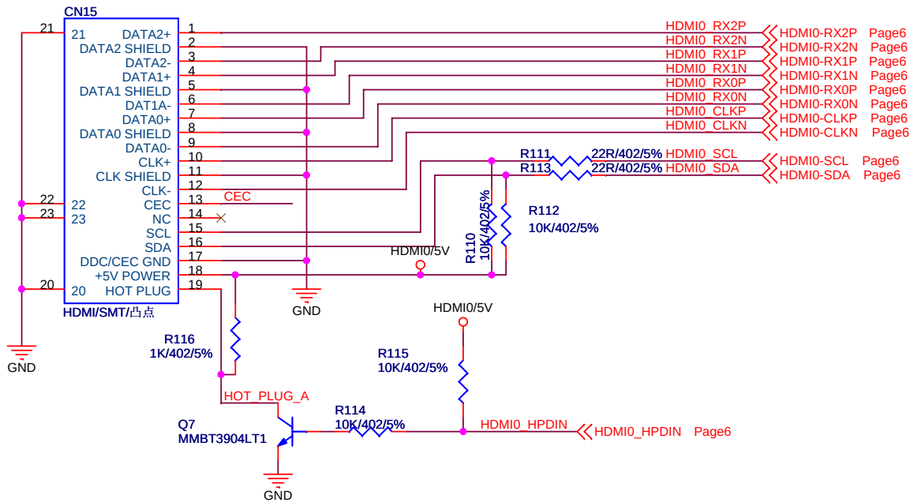
连接到有 IC支持MHL port供电pin,靠近IC端



USB Interface







Date	Modify Number	Modify By	
			深圳市鼎科实业有限公司
			SheetName: 08.HDMI & USB
			Size: A3 / Document Number: P75-3463GU V6.0 / Rev: A
Modify Date: Tuesday, March 24, 2015			Designed By: suncheng / Sheet 8 of 10

硅tuner DVB-T/C

Silicon Tuner:R840

optional component of WIFI filter,
if no need this option, pls short it

for GPIO purpose. R22=10kR for GPIO
R22=NC if no need this option.

for GPIO purpose. R22=10kR for GPIO.
R22=NC if no need this option.

5V_FB
TJ1 DVBT区域
TUNER_CON/IEC/HL=14/B22-064
CON\IEC\CTP-124J-7A
RF
CT3 1nF/X7R/50V/402
CT1 1p5F/NPO/50V/402
C6 C10
L22 L26
LT1 2.2nH/150mA/402
LT3 NC/TBD/220nH
L25
180P/NPO/50V/402
CT2 C3
L27
LT2 150NH/402
CT4 0R/402/1% C8
DT1
BAV99
C4
CT7 220PF/NPO/50V.402
L20
LT4 180NH/402
TBD/1000R/100MHZ
LT7 L18
close to D403(BAV99)
75 ohm line

VDD3V
68nH/180mA/402
FB_CTR
270nH/100mA/402
100nF/X7R/16V/402
CT8 L15 L16 L17 CT9 CT10
22nF/X7R/25V/402

UT1 R840

25	GND	AVDD	24
1	RFIN	TFH	23
2	RFIN2	TFL	22
3	TF1	GPIO	21
4	TF2	VBG	20
5	DECT1	DET2	19
6	SCL	AVDD	18
7	SDA	VOP	17
8	AVDD	VON	16
9	CP	VAGC	15
10	DVSS	VAGC2	14
11	DVDD	XTAL_O	13
12	XTAL_I		

L24 LT8
FB/1000R/100mA/402
180nH/100mA/402
LT9
CT12 100nF/X7R/16V/402
CT11 100nF/X7R/16V/402
CT19 1nF/X5R/50V/402 24MH_IN Page6
T-SCL T-SDA
CT22 100nF/X7R/16V/402
RT5 1K8/402/1%
CT23 330pF/NPO/50V/402
CT24 6.8NF/X7R/25V/402
CT25 100nF/X7R/16V/402
GND

5V_FB LT23 NC/680nH FT1 NC/F/6V/1.5A/1206
CT59 NC/100nF/X5R/16V/402
TQ1 QM3001K SOT-23M
CT58 100nF/X5R/16V/402
RT17 100K/402/1%
5VA
RT16 10K/402/5%
TQ2 MMBT3904LT1 SOT-23 DVBT区域
RT18 4K7/402/5%
+3.3V_TU
RT19 10K/402/5%
FB_CTR
DVBT区域

T-SCL RT1 4K7/402/5% Tuner_VCC RT2 4K7/402/5%
T-SDA TR1 Tuner区域 NC/33R/402/5% SYS_SCL SYS_SCL Page6
TR2 Tuner区域 NC/33R/402/5% SYS_SDA SYS_SDA Page6
CT5 39pF/NPO/50V/402
CT6 39pF/NPO/50V/402

UT2
TUNER POWER
2.2uF/X7R/16V/603
1117-3V3_223 100nF/X5R/16V/402
10uF/X5R/6.3V/603
100nF/X5R/16V/402
+3.3V_TU Tuner_VCC
5VA
CT15 CT16 CT17 CT18

close to tuner
VAGC RT3 10K/402/5% T-AGC RT4 NC/0R/402/5% TAGC TAGC Page6
CT21 100nF/X5R/16V/402
Tuner区域

Bead (L21):
1k@100M &
400ohm@400M,300mA

VDD3V
VDD3V
CT30 100nF/X5R/16V/402
DVBT区域
FB/600R/1.2A/603
LT11
+3.3V_TU
CT31 10uF/X5R/6.3V/603
0805C_ST

if no need VAGC2, pls R111=C111=NC
IF Interface Filter
VON RT6 220R/402/5%
Tuner区域 IF-IN- CT26 100nF/X5R/16V/402
CABLE-IF- TL1 FB/560R/0.2A/0402
CT27 100nF/X5R/16V/402 VIFM VIFM Page6
CT28
RT7 470R/402/5%
CT29
VOP RT8 220R/402/5% Tuner区域 IF-IN+ CT32 100nF/X5R/16V/402
CABLE-IF+ LT12 FB/560R/0.2A/0402
CT33 100nF/X5R/16V/402 VIFP VIFP Page6
100PF/NPO/50V0402
100PF/NPO/50V0402

Application
DTMB_bypass
L17=L18=GZ1005D102CTF, C3=C4=C10=L20=L25=NC, C8=L26=L27=0R
Other standard_bypass
L17=270nH, L18=GZ1005D102CTF, C3=C4=C10=L20=L25=NC, C8=L26=L27=0R
Hybrid (with S1 filter for EN55020)
L17=L18=L20=L25=270nH, C8=82pF, C3=C10=270pF, C4=100pF, L26=L27=150nH

optional component of WIFI filter,
if no need this option, pls short it

for GPIO purpose. R22=10kR for GPIO
R22=NC if no need this option.

硅tuner DVB-T2/C

Silicon Tuner:R840

TJ2 DVBT区域
TUNER_CON/IEC/HL=14/B22-064
CON\IEC\CTP-124J-7A
RF1
CT36 1nF/X7R/50V/402
1p5F/NPO/50V/402
C6 CT34
L22 L26
LT13 2.2nH/150mA/402
LT15 NC/TBD/220nH
L25
180PF/NPO/50V/402
CT35 C3
L27
LT14 150NH/402
CT37 0R/402/1% C8
DT2
BAV99
C4
CT38 220PF/NPO/50V.402
L20
LT16 180NH/402
TBD/1000R/100MHZ
LT19 L18
close to D403(BAV99)
75 ohm line

VDD3V_CABLE
68nH/180mA/402
270nH/100mA/402
100nF/X7R/16V/402
CT38 L17 L18 L19 CT40 CT41
22nF/X7R/25V/402

UT3 R840

25	GND	AVDD	24
1	RFIN	TFH	23
2	RFIN2	TFL	22
3	TF1	GPIO	21
4	TF2	VBG	20
5	DECT1	DET2	19
6	SCL	AVDD	18
7	SDA	VOP	17
8	AVDD	VON	16
9	CP	VAGC	15
10	DVSS	VAGC2	14
11	DVDD	XTAL_O	13
12	XTAL_I		

L24 LT20
FB/1000R/100mA/402
180nH/100mA/402
LT21
CT44 100nF/X7R/16V/402
CT43 100nF/X7R/16V/402
CT45 NC/16p
YT1 24MHz,CL=16pF
CT47 NC/16p
CT-SCL CT-SDA
CT48 39pF/NPO/50V/402
CT49 39pF/NPO/50V/402
CT50 100nF/X7R/16V/402
RT12 1K8/402/1%
CT52 330pF/NPO/50V/402
CT53 6.8NF/X7R/25V/402
CT54 100nF/X7R/16V/402
GND

TU4 SGM330A
QSOP16
T-SDA T-SCL T-AGC
CT-SDA CT-SCL C-AGC
S1A S1B S1C S1D S2A S2B S2C S2D VCC GND EN IN DA DB DC DD
SYS_SDA SYS_SCL TUAGC
Tuner_VCC
CT42 100nF/X5R/16V/402
RT9 Tuner区域 100R/402/5%
AIR-CABLE Page6

L----> AIR
H----> CABLE

close to tuner
VAGC_C RT11 10K/402/5% C-AGC
CT46 100nF/X5R/16V/402

Bead (L21):
1k@100M &
400ohm@400M,300mA

VDD3V_CABLE
VDD3V_CABLE
CT55 100nF/X5R/16V/402
DVBT区域
FB/600R/1.2A/603
LT22
+3.3V_TU
CT56 10uF/X5R/6.3V/603
0805C_ST

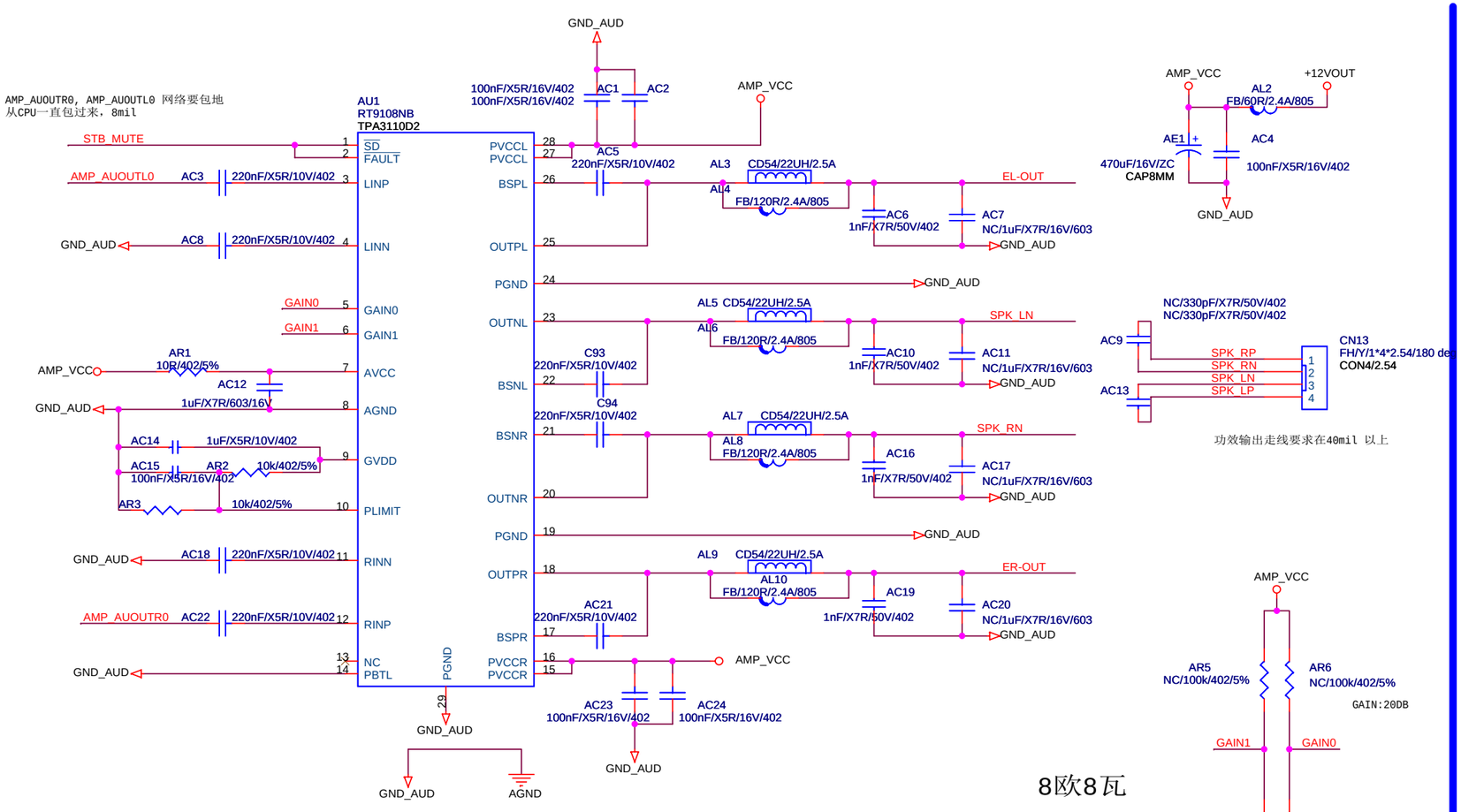
if no need VAGC2, pls R111=C111=NC
IF Interface Filter
VON_C RT13 220R/402/5%
Tuner区域 CT51 100nF/X5R/16V/402
CABLE-IF-
470R/402/5%
RT15 220R/402/5% Tuner区域 RT14
VOP_C CT57 100nF/X5R/16V/402
CABLE-IF+

GND

Date	Modify Number	Modify By

深圳市鼎科实业有限公司
SheetName 9.Front End
Size Custom | Document Number P75-3463GU V6.0 | Rev A
Modify Date: Monday, March 23, 2015 | Designed By: suncheng | Sheet 9 of 10

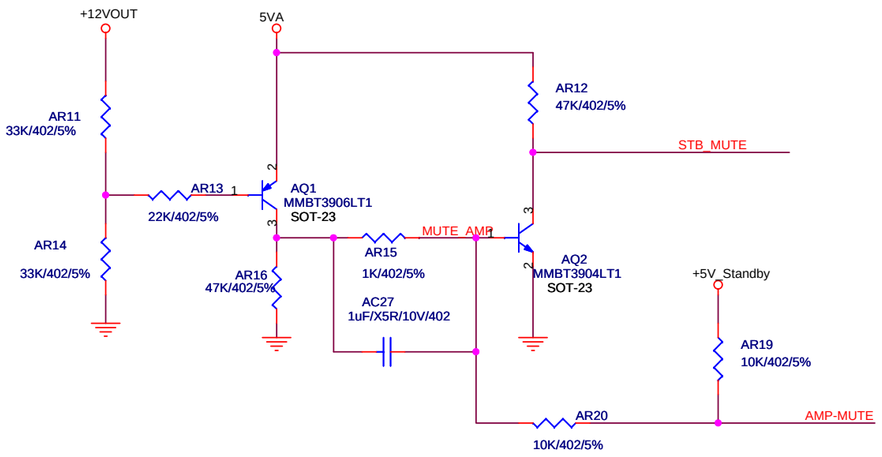
EARPHONE OUT

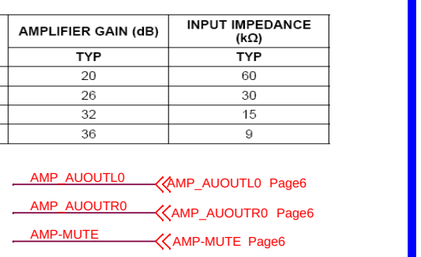


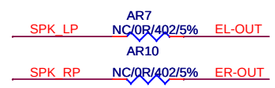
功效输出走线要求在40mil 以上

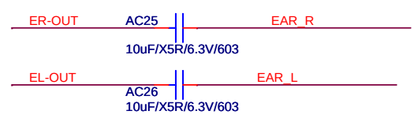
8欧8瓦

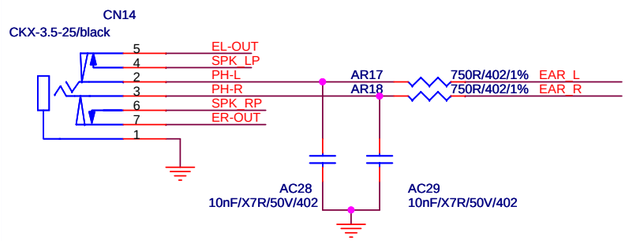
GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9











PIN NAME	Pin #	I/O/P	DESCRIPTION
SD	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
FAULT	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULT pin to SD pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
GAIN0	5	I	Gain select least significant bit. TTL logic levels with compliance to AVCC.
GAIN1	6	I	Gain select most significant bit. TTL logic levels with compliance to AVCC.

Date	Modify Number	Modify By

深圳市鼎科实业有限公司

SheetName: 10..Amplify

Size: A3 | Document Number: P75-3463GU V6.0 | Rev: A

Modify Date: Monday, March 23, 2015 | Designed By: suncheng | Sheet 10 of 10