Attention Please: Under the technology license agreement between MStar and Dolby/SRS/BBE/DivX/Microsoft/QSound/Audyssey, MStar is obliged not to provide samples that incorporate Dolby/SRS/BBE/DivX/Microsoft/QSound/Audyssey technology to any third party who is not a qualified licensee of Dolby/SRS/BBE/DivX/Microsoft/QSound/Audyssey respectively.

FEATURES

MSD3391DS, an SOC solution that supports channel decoding and MPEG decoding

Key features includes,

1. *Digital and Analog Front-End Demodulator*
2. *A Multi-Standard A/V Format Decoder*
3. *The MACE-5 Video Processor*
4. *Home Theater Sound Processor*
5. *Peripheral and Power Management*

- High Performance Micro-processor
  - Ultra high speed/performance 32-bit RISC CPU
  - One full duplex UARTs
  - DMA Engine
- Transport Stream De-multiplexer
  - Supports serial TS interface, with or without sync signal
  - Maximum TS data rate is 104 Mb/sec
  - 32 general purpose PID filters and section filters for each transport stream de-multiplexer
- MPEG-2 Video Decoder
  - ISO/IEC 13818-2 MPEG-2 video MP@HL
  - Automatic frame rate conversion
  - Supports resolution up to HDTV (1080i, 720p) and SDTV
- Hardware JPEG
  - Supports sequential mode, single scan
  - Supports both color and grayscale pictures
  - Following the file header scan the hardware decoder fully handles the decode process
  - Supports programmable Region of Interest (ROI)
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2, 1/4, 1/8
  - Supports picture rotation
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Four configurable CVBS & Y/C S-video inputs
  - Supports Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE
- Multi-Standard TV Sound Processor
  - SIF audio decoding
  - Supports BTSC/EIA-J demodulation
  - Supports FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC/ EIA-J mode
  - Built-in audio sampling rate conversion (SRC)
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
  - Advanced sound processing options available, for example: Dolby[1], SRS[2], BBE[3], QSound[4], Audyssey[5]
  - Supports digital audio format decoding:
    - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3)[Optional], AAC-LC
- Audio Interface
  - One SIF audio input interface without any external SAW filter
  - Four L/R audio line-inputs
  - One TV line-output
  - One embedded stereo headphone driver
  - I2S digital audio input & output
  - S/PDIF digital audio input & output
  - HDMI[6] audio channel processing
  - Programmable delay for audio/video synchronization

[1] **Trademark of Dolby Laboratories**
[2] **Trademark of SRS Labs, Inc.**
[3] **Registered trademark of BBE Sound, Inc.**
[4] **Registered trademark of QSound Labs, Inc.**
[5] **Registered trademark of Audyssey Laboratories, Inc.**
[Optional] **Please see Ordering Guide for details.**
[6] **Registered trademark of HDMI Licensing LLC**

- Analog RGB Compliant Input Ports
  - Two analog ports support up to 1080P
  - Supports PC RGB input up to SXGA@75Hz
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG Sync-on-Green
  - Automatic color calibration
- Analogue RGB Auto-Configuration & Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
  - Sync Detection for H/V Sync
- DVI/HDCP/HDMI Compliant Input Ports
  - Three HDMI/DVI Input ports
  - HDMI 1.3/1.4 Compliant
  - MStar iSwitch for fast HDMI switching
  - HDCP 1.3 Compliant
  - 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
  - Supports HDMI CEC
  - Supports HDMI 1.4a 3D format input
  - Supports HDMI 4Kx2K input
  - Supports HDMI ARC
  - Single link DVI 1.0 compliant
  - Robust receiver with excellent long-cable support
- MStar Advanced Color Engine (MACE-5)
  - 10/12-bit internal data processing
  - Dual-engine architecture supporting PIP/PBP with same quality
  - High taps and fully programmable multi-function scaling engine
    - Nonlinear video scaling supports various modes including Panorama
  - High-Quality DTV video processor
    - 3D motion video deinterlacer with motion object stabilizer
    - Edge-oriented deinterlacer with edge and artifact smoother
    - Automatic 3:2/2:2/M:N pull-down detection and recovery
    - 3D multi-purpose noise reduction for DTV or lousy air/cable input
    - MPEG artifact removal including de-blocking and mosquito noise reduction
    - Arbitrary frame rate conversion
  - Automatic picture enhancement:
    - Includes all features in MACE-3/4 engine
    - 3D adaptive color control enabling vivid visual reception in the true world from most dark to most bright scenes
    - 3D adaptive sharpening control enabling crystal clear visual reception without distorting scene reality
    - Supports sRGB and xvYCC color processing
    - Supports HDMI 1.3 deep color format
    - Supports enhanced and seamless color mapping for wider gamut panels
  - Programmable 12-bit RGB gamma CLUT
- Output Interface
  - Single/dual link 8/10-bit LVDS output
  - Supports panel resolution up to Full-HD (1920x1080) @ 60Hz
  - Supports dithering options
  - Spread spectrum output frequency for EMI suppression
- CVBS Video Outputs
  - Supports CVBS bypass output
- 3D-like Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill, text draw and trapezoid draw
  - BitBlt, stretch BitBlt, trapezoid BitBlt, mirror BitBlt and rotate BitBlt
  - Supports alpha and destination alpha compare
  - Raster Operation (ROP)
  - Support Porter-Duff
- VIF Demodulator
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
  - Digital low IF architecture
  - Audio/Video dual-path processor
  - Stepped-gain PGA with 25 dB tuning range and 1 dB tuning resolution
  - Maximum IF gain of 37 dB
  - Programmable TOP to accommodate different tuner gain and SAW filter insertion loss to optimize noise and linearity performance
  - Multi-standard processing without any external SAW filter

- Ÿ Supports silicon tuner low IF output architecture

n ATSC/QAM Demodulator

- Ÿ ATSC A/53 compliant 8VSB
- Ÿ ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
- Ÿ Integrated 11-bit A/D converter (for optional external A/D converter support)
- Ÿ All digital demodulation
- Ÿ Integrated deinterleaver RAM for all modes (No need of external memory for deinterleaver)
- Ÿ Supports 44MHz IF input
- Ÿ Supports no SAW for any application

n Connectivity

- Ÿ Two USB 2.0 host ports
- Ÿ USB architecture designed for efficient support of external storage devices

n Miscellaneous

- Ÿ DRAM interface supporting one 16-bit DDR2 @ 1066MHz
- Ÿ Bootable SPI interface with serial flash support
- Ÿ Power control module with ultra low power MCU available in standby mode
- Ÿ 216-pin EPLQFP package
- Ÿ Operating Voltages: 1.2V (core), 1.8V (DDR2), 2.5V and 3.3V (I/O and analog)

GENERAL DESCRIPTION

The MSD3391DS is MStar's most up-to-date system-on-chip flagship for flat panel integrated digital television products. The MSD3391DS integrates DTV, ATSC/QAM demodulator, VIF demodulator, and Sound/Video processor into a single device. This allows the overall BOM to be reduced significantly making the MSD3391DS a very cost effective multi-media DTV solution.

For standard users, the MSD3391DS provides multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. The build-in audio decoder is capable of decoding FM, AM, BTSC and EIA-J sound standards. The MSD3391DS supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selection multiplexed for video and audio are integrated, including full SCART support with CVBS output.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MSD3391DS has an ultra low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		TBD		LSB
Integral Nonlinearity		TBD		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum		0.5		V p-p
Maximum		TBD		V p-p
Input Bias Current			1	uA
SWITCHING PERFORMANCE				
Maximum Conversion Rate	170			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		170	MHz
PLL Jitter		TBD		ps p-p
Sampling Phase Tempco		TBD		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		0.3		V
Output High		1.3		V
AUDIO				
ADC Input		2.8		V p-p
DAC Output		2.8		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p

Parameter	Min	Typ	Max	Unit
SAR ADC Input	0		3.3	V
FB ADC Input*	0		1.2	V

Specifications subject to change without notice.
Note: Input full scale is 1.2V, but input range is 0 ~ 3.3V.

Recommended Operating Power Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
2.5V Supply Voltages	$V_{VDD\ 25}$	2.38		2.62	V
1.8V Supply Voltage	$V_{VDD\ 18}$	1.71		1.89	V
1.2V Supply Voltage	V_{VDD_12}	1.20		1.32	V
Junction Temperature	T_J			125	°C
Case Temperature	T_C			100	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		3.6	V
2.5V Supply Voltages	V_{VDD_25}		2.75	V
1.8V Supply Voltages	V_{VDD_18}		1.98	V
1.2V Supply Voltages	V_{VDD_12}		1.32	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{STG}	-40	150	°C
Junction Temperature	T_J		150	°C

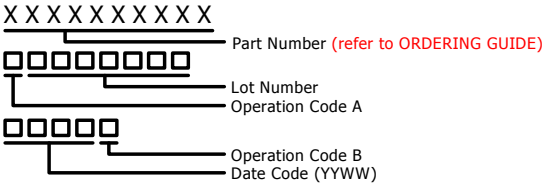
Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MSD3391DS	0°C to +70°C	EPLQFP	216-pin
MSD3391DS-XX	0°C to +70°C	EPLQFP	216-pin

Note:
XX suffix represents advanced features. Please contact MStar sales for details.

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MSD3391DS comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MSD3391DS_ds_v01	Ÿ Initial release	May 2011

REGISTER DESCRIPTION

MIU1 Register (Bank = 1006)

MIU1 Register (Bank = 1006)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (100600h)	**REG100600**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	AUTO_REF_OFF	5	Turn off auto refresh.	
	ODT	4	Turn on ODT (only for DDR2/DDR3).	
	RSTZ	3	DRAM reset.	
	CS	2	DRAM chip select.	
	CKE	1	Enable CKE.	
	INIT_MIU	0	Auto initial DRAM cycle.	
00h (100601h)	**REG100601**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_INIT_DONE	7	Auto initial DRAM cycle done flag.	
	R_SINGLE_CMD_DONE	6	Single command done flag.	
	SELF_REFRESH	5	Enter self refresh mode.	
	-	4	Reserved.	
	SINGLE_CMD[2:0]	3:1	Single command = {rasz, casz, wez}.	
	SINGLE_CMD_EN	0	Issue single command.	
01h (100602h)	**REG100602**	**7:0**	**Default : 0x00**	**Access : R/W**
	CA_SIZE[1:0]	7:6	00: 8col. 01: 9col. 10: 10col. 11: Reserved.	
	BA_SIZE[1:0]	5:4	00: 2ba. 01: 4ba. 10: 8ba. 11: Reserved.	
	DRAM _BUS[1:0]	3:2	00: 16-bit. 01: 32-bit. 10: 64-bit. 11: Reserved.	
	DRAM _TYPE[1:0]	1:0	00: SDR. 01: DDR. 10: DDR2. 11: DDR3.	
01h	**REG100603**	**7:0**	**Default : 0xF0**	**Access : R/W**

MIU1 Register (Bank = 1006)

Index (Absolute)	Mnemonic	Bit	Description	
	CKO_OENZ	7	Ck output enable.	
	ADR_OENZ	6	Address output enable.	
	DQ_OENZ	5	Data output enable.	
	CKE_OENZ	4	CKE output enable.	
	DATA_SWAP[1:0]	3:2	01: [15:0]. 10: [31:16].	
	DATA_RATIO[1:0]	1:0	00: 1x. 01: 2x. 10: 4x. 11: 8x.	
02h (100604h)	**REG100604**	**7:0**	**Default : 0x09**	**Access : R/W**
	I64_MODE	7	0: All 128 internal bus. 1: Support 64 internal bus (only 4x mode).	
	-	6:5	Reserved.	
	RD_TIMING[4:0]	4:0	Read back data delay timing.	
03h (100606h)	**REG100606**	**7:0**	**Default : 0x08**	**Access : R/W**
	TREFPERIOD[7:0]	7:0	Refresh cycle period, unit = 16 mclk.	
03h (100607h)	**REG100607**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	ODT_ALWAYS_ON	5	ODT always on.	
	CKE_ALWAYS_ON	4	CKE always on.	
	-	3	Reserved.	
	TCKE[2:0]	2:0	DRAM TCKE timing.	
04h (100608h)	**REG100608**	**7:0**	**Default : 0x33**	**Access : R/W**
	TRP[3:0]	7:4	DRAM TRP timing.	
	TRCD[3:0]	3:0	DRAM TRCD timing.	
04h (100609h)	**REG100609**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	TRAS[4:0]	4:0	DRAM TRAS timing.	
05h (10060Ah)	**REG10060A**	**7:0**	**Default : 0x12**	**Access : R/W**
	TRTP[3:0]	7:4	DRAM TRTP timing.	
	TRRD[3:0]	3:0	DRAM TRRD timing.	
05h (10060Bh)	**REG10060B**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:6	Reserved.	

MIU1 Register (Bank = 1006)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TRC[5:0]	5:0	DRAM TRC timing.	
06h (10060Ch)	**REG10060C**	**7:0**	**Default : 0x61**	**Access : R/W**
	TWR[3:0]	7:4	DRAM TWR timing: write recovery time.	
	TWL[3:0]	3:0	DRAM TWL timing: write latency.	
06h (10060Dh)	**REG10060D**	**7:0**	**Default : 0x63**	**Access : R/W**
	TRTW[3:0]	7:4	Read to write delay.	
	TWTR[3:0]	3:0	DRAM TWTR timing: write to read delay.	
07h (10060Eh)	**REG10060E**	**7:0**	**Default : 0x0E**	**Access : R/W**
	TRFC[7:0]	7:0	DRAM TRFC timing.	
07h (10060Fh)	**REG10060F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	TCCD[2:0]	6:4	DRAM TCCD timing.	
	-	3:0	Reserved.	
08h (100610h)	**REG100610**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[7:0]	7:0	Mode register 0.	
08h (100611h)	**REG100611**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[15:8]	7:0	See description of '101210h'.	
09h (100612h)	**REG100612**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR1[7:0]	7:0	Mode register 1.	
09h (100613h)	**REG100613**	**7:0**	**Default : 0x40**	**Access : R/W**
	MR1[15:8]	7:0	See description of '101212h'.	
0Ah (100614h)	**REG100614**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR2[7:0]	7:0	Mode register 2.	
0Ah (100615h)	**REG100615**	**7:0**	**Default : 0x80**	**Access : R/W**
	MR2[15:8]	7:0	See description of '101214h'.	
0Bh (100616h)	**REG100616**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR3[7:0]	7:0	Mode register 3.	
0Bh (100617h)	**REG100617**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MR3[15:8]	7:0	See description of '101216h'.	

MIU0 Register (Bank = 1012)

MIU0 Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (101200h)	**REG101200**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	AUTO_REF_OFF	5	Turn off auto refresh.	
	ODT	4	Turn on ODT (only for DDR2/DDR3).	
	RSTZ	3	DRAM reset.	
	CS	2	DRAM chip select.	
	CKE	1	Enable CKE.	
	INIT_MIU	0	Auto initial DRAM cycle.	
00h (101201h)	**REG101201**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	R_INIT_DONE	7	Auto initial DRAM cycle done flag.	
	R_SINGLE_CMD_DONE	6	Single command done flag.	
	SELF_REFRESH	5	Enter self refresh mode.	
	-	4	Reserved.	
	SINGLE_CMD[2:0]	3:1	Single command = {rasz, casz, wez}.	
	SINGLE_CMD_EN	0	Issue single command.	
01h (101202h)	**REG101202**	**7:0**	**Default : 0x00**	**Access : R/W**
	CA_SIZE[1:0]	7:6	00: 8col. 01: 9col. 10: 10col. 11: Reserved.	
	BA_SIZE[1:0]	5:4	00: 2ba. 01: 4ba. 10: 8ba. 11: Reserved.	
	DRAM _BUS[1:0]	3:2	00: 16-bit. 01: 32-bit. 10: 64-bit. 11: Reserved.	
	DRAM _TYPE[1:0]	1:0	00: SDR. 01: DDR. 10: DDR2. 11: DDR3.	
01h (101203h)	**REG101203**	**7:0**	**Default : 0xF0**	**Access : R/W**
	CKO_OENZ	7	Ck output enable.	

MIU0 Register (Bank = 1012)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ADR_OENZ	6	Address output enable.	
	DQ_OENZ	5	Data output enable.	
	CKE_OENZ	4	CKE output enable.	
	DATA_SWAP[1:0]	3:2	01: [15:0]. 10: [31:16].	
	DATA_RATIO[1:0]	1:0	00: 1x. 01: 2x. 10: 4x. 11: 8x.	
02h (101204h)	**REG101204**	**7:0**	**Default : 0x09**	**Access : R/W**
	I64_MODE	7	0: All 128 internal bus. 1: Support 64 internal bus (only 4x mode).	
	-	6:5	Reserved.	
	RD_TIMING[4:0]	4:0	Read back data delay timing.	
03h (101206h)	**REG101206**	**7:0**	**Default : 0x08**	**Access : R/W**
	TREFPERIOD[7:0]	7:0	Refresh cycle period, unit = 16 mclk.	
03h (101207h)	**REG101207**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	ODT_ALWAYS_ON	5	ODT always on.	
	CKE_ALWAYS_ON	4	CKE always on.	
	-	3	Reserved.	
	TCKE[2:0]	2:0	DRAM TCKE timing.	
04h (101208h)	**REG101208**	**7:0**	**Default : 0x33**	**Access : R/W**
	TRP[3:0]	7:4	DRAM TRP timing.	
	TRCD[3:0]	3:0	DRAM TRCD timing.	
04h (101209h)	**REG101209**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	TRAS[4:0]	4:0	DRAM TRAS timing.	
05h (10120Ah)	**REG10120A**	**7:0**	**Default : 0x12**	**Access : R/W**
	TRTP[3:0]	7:4	DRAM TRTP timing.	
	TRRD[3:0]	3:0	DRAM TRRD timing.	
05h (10120Bh)	**REG10120B**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:6	Reserved.	
	TRC[5:0]	5:0	DRAM TRC timing.	

MIU0 Register (Bank = 1012)

Index (Absolute)	Mnemonic	Bit	Description	
06h (10120Ch)	**REG10120C**	**7:0**	**Default : 0x61**	**Access : R/W**
	TWR[3:0]	7:4	DRAM TWR timing: write recovery time.	
	TWL[3:0]	3:0	DRAM TWL timing: write latency.	
06h (10120Dh)	**REG10120D**	**7:0**	**Default : 0x63**	**Access : R/W**
	TRTW[3:0]	7:4	Read to write delay.	
	TWTR[3:0]	3:0	DRAM TWTR timing: write to read delay.	
07h (10120Eh)	**REG10120E**	**7:0**	**Default : 0x0E**	**Access : R/W**
	TRFC[7:0]	7:0	DRAM TRFC timing.	
07h (10120Fh)	**REG10120F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	TCCD[2:0]	6:4	DRAM TCCD timing.	
	-	3:0	Reserved.	
08h (101210h)	**REG101210**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[7:0]	7:0	Mode register 0.	
08h (101211h)	**REG101211**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR0[15:8]	7:0	See description of '101210h'.	
09h (101212h)	**REG101212**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR1[7:0]	7:0	Mode register 1.	
09h (101213h)	**REG101213**	**7:0**	**Default : 0x40**	**Access : R/W**
	MR1[15:8]	7:0	See description of '101212h'.	
0Ah (101214h)	**REG101214**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR2[7:0]	7:0	Mode register 2.	
0Ah (101215h)	**REG101215**	**7:0**	**Default : 0x80**	**Access : R/W**
	MR2[15:8]	7:0	See description of '101214h'.	
0Bh (101216h)	**REG101216**	**7:0**	**Default : 0x00**	**Access : R/W**
	MR3[7:0]	7:0	Mode register 3.	
0Bh (101217h)	**REG101217**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MR3[15:8]	7:0	See description of '101216h'.	

Scaler1 Register (Bank = 102F)

GOP_INT Register (Bank = 102F, Sub-bank = 00)

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102F00h)	**REG102F00**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler.	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]: SWRST1[4]: IP, include F1 and F2. SWRST1[3]: OP include OP1, VIP and VOP. SWRST1[2]: IP_F2. SWRST1[1]: IP_F1. SWRST1[0]: All engines.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PDMD[1:0]	1:0	Power Down mode. 01: IDCLK. Others: IDCLK and ODCLK.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 VS INT Edge. 0: Leading. 1: Tailing.	
	IPVSINT_EDGE	0	IP VS INT Edge. 0: Leading. 1: Tailing.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	CHG_HMD	0	CHG_HMD: H Change Mode for INT.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_SYNC_TO_GOP_SEL[1:0]	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.	
	GOP2IP_EN	5	GOP blending to IP enable.	
	-	4:0	Reserved.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GOP2IP_DATA_SEL[1:0]	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	COP_EN	7	Enable cop for VOP2.	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_7_0[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: IPHCS_DET_INT_F1.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_FINAL_STATUS_31_24[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[1]: N/A. D[0]: N/A.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_7_0[7:0]	7:0	The raw status of interrupt source. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_15_8[7:0]	7:0	The raw status of interrupt source. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_23_16[7:0]	7:0	The raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : RO**
	IRQ_RAW_STATUS_31_24[7:0]	7:0	The raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BIST_FAIL_0[10:8]	2:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : RO**
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	See description of '102F48h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0xE1**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	WDT_EN	0	H/V sync lose watch dog timer count enable.	

IP1_M Register (Bank = 102F, Sub-bank = 01)

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.	
	CSC_EN	3	Input CSC function. 0: Disable (RGB -> RGB, default). 1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: Reserved. 111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. 0: Disable (Auto selected by h/W, used when input is video, default). 1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
	YCBCR_EN	2	Input Source is YPbPr Format.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. 00: External 8/10 bits video port. 01: Internal video decoder mode A.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: External 16/20 bits video port. 11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. 0: Delay 1/4 input HSYNC. 1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. 0: Disable. 1: Enable.	
	HWRAP	0	Input image Horizontal wrap. 0: Disable. 1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. 1: Display will adaptive follow the Source. If Display Select this source. 0: Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change,	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	
	VD16_C_AHEAD	1	Video 16 bit mode fine tune Y/C order.	
	-	0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HST[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. 0: Disable.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. 0: Mask. 1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). 0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. 1: Use Hsync only. When ISEL = 011:(DVI). 0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). 0: Normal. 1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. 0: Normal. 1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. 0: Use Separate Hs for Coast Period. 1: Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**

IP1_M Register (Bank = 102F, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. 0: Leading edge. 1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. 0: Auto Switch VST(04), VDC (06). 1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. 0000: 8 Lines Ahead from SPRANGE_VST. 0001: 1 Line Ahead from SPRANGE_VST. 0010: 2 Lines Ahead from SPRANGE_VST. 0011: 3 Lines Ahead from SPRANGE_VST. .. 1111: 15 Lines Ahead from SPRANGE_VST.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0	Reserved.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	Reserved.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetition.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2	Reserved.	
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: HW Auto Decide. 1: SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. 0: no down, 5 tap support. 1: down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. 0: no down, 5 tap. 1: 2 to 1 down, 11 tap. Else: Reserved. For ExtVD is CCIR656, set to 0 and OVERSAP_EN = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_DATA_MD = 0. Output over max value (255) when. ATG_DATA_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_DATA_MD = 0. Output over max value (255) when. ATG_DATA_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). 0: Normal. 1: Max value (255) value when. ATG_DATA_MD = 0. Output over max value (255) when. ATG_DATA_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable.	

IP1_M Register (Bank = 102F, Sub-bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			0: Disable. 1: Reserved.
	ATG_DATA_MD	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.
	ATG_HISMD	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATG_EN = 0).
	ATG_READY	1	Auto Gain Result Ready. 0: Result not ready. 1: Result ready.
	ATG_EN	0	Auto Gain Function Enable. 0: Disable. 1: Enable.
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00** **Access : RO, R/W**
	-	7	Reserved.
	AV_DET	6	AV Detect for Cb Cr. 0: CbCr Range is define by 03[2]. YCBCR_EN. 1: Cb Cr Min is define in 89 ATP_GTH, Cb Cr Max is define in 8A ATP_TH.
	-	5:3	Reserved.
	ATG_UPR	2	Min value flag for R channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.
	ATG_UPG	1	Min value flag for G channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.
	ATG_UPB	0	Min value flag for B channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. 0: Disable. 1: Enable.	
	OP2_COAST	6	Coast Status (Read only). 0: Coast is inactive. 1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for: 1. VD. 2. Ext VD 656 Format. 3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. 000: Minimum R value. 001: Minimum G value. 010: Minimum G value. 011: Maximum R value. 100: Maximum G value. 101: Maximum B value. 11x: Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0F_8_15[7:0]	7:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: Right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. 0: Not clear. 1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Update every frame. 1: Keep the history value.	
	JITTER	3	JITTER function Result. 0: No JITTER. 1: JITTER present.	
	ATS_HISMD	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. 0: Result not ready. 1: Result ready.	
	ATS_EN	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	THOLD[3:0]	7:4	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000. 0010: Valid if data >= 0010 0000. .. 1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Position Force Pixel Mode. 0: DE or Pixel decide by the Source. 1: Force Pixel Mode.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE[7:0]	7:0	Auto Gain Value. (selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h	**REG102F25**	**7:0**	**Default : 0x00**	**Access : RO**

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	ATS_VSTDBUF[12:8]	4:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HSTDBUF[12:8]	4:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_VEDDBUF[12:8]	4:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	ATS_HEDDBUF[12:8]	4:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : RO**
	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on REG_10H[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	REG_JLST[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. 111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	Reserved.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. 0: Disable. 1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. 0: In display. 1: In blanking.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Position Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. #5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Separator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. 0: Disable. 1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. 1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			(Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. 0: Not active. 1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. 0: Not active. 1: Active.	
	CS_DET	5	Composite Sync Detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. 0: Input is not SOG. 1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulse Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. 0: 1 line. 1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Separator Htt. 0: Htt Report by Mode Detector. 1: Htt Report by Sync Separator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. 0: Old method. 1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. 0: Active low. 1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_VSPOL).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. 0: Active low. 1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_HSPOL).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Defined by user (USR_INTLAC).	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. 00: Sample V End. 01: Sample V Start. 10: Sample V Start Ahead by Current Bank 09[3:0]. 11: Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. 0: Mode Change Provide in data clock Domain. 1: Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. 0: Form Input DE. 1: From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_VIDEO = 1 for Data Align. 0: Normal. 1: Invert.	
	EXT_FIELDMD	2	Video External Field. 0: Use result of internal circuit detection. 1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. 0: Normal. 1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Separator VSYNC for Mode Detect. 0: RAW VSYNC (H / V Relationship is Keep for Interlace Detect). 1: HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. 0: PC Source. 1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). 0: Disable. 1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when COAST_SRCS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. 0: Internal Separated VSYNC (Default). 1: External VSYNC (Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			#255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. 0: Disable. 1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI: 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPVS_ACT, IPHS_ACT (E1[7:6]) (recommend).	
	IDCLK_INV	0	Capture Port Sample CLK Invert.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Normal. 1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_9_15[6:0]	7:1	Reserved.	
	IP1_RDY_MASK_EN	0	Mask IP1 output DE enable.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). 0: Disable. 1: Enable.	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). 0: Disable. 1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). 0: Disable. 1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable. 1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_9_15[6:0]	7:1	Reserved.	
	LOCK_FIELD_EN	0	Lock field flag toggle sequence enable.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_ID_FOR_READ[7:0]	7:0	HTT by IDCLK.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. 00: off. 01: Only for line total number is even. 10: all case. 11: off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. 0: Define Automatically. 1: Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**

IP1_M Register (Bank = 102F, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. 0: Can gate the GOP clock. 1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. 0: Don't gate the IDCLK. 1: Can gate the IDCLK.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	ATS_B_SKIP	2	Auto search ignore B data.	
	ATS_G_SKIP	1	Auto search ignore G data.	
	ATS_R_SKIP	0	Auto search ignore R data.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DE_BYPASS_MODE	7	Use input DE to replace SPRANGE_H as output DE.	
	-	6:0	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMBER_OFFSET.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_SEL	7	Vsync INSERT_NUMBER_OFFSET enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMBER_OFFSET.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_SEL	7	Vsync LOCK_NUMBER_OFFSET enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. 0x: reference 21[15:14]. 10: Sample V end delay 1 line. 11: Sample V end delay 3 line.	
	-	5:0	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_CLAMP_EN	7	RGB value clamp enable, from 10'h3ff to 10'h3fc.	
	-	6:3	Reserved.	
	ATG_NEW_RANGE	2	Internal signal timing range for Auto Gain.	
	ATG_NEW_CLR	1	Auto Gain reset.	
	ATG_NEW_MODE	0	Use internal signal to do Auto Gain.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SOG_VALID	7	Input composite/SOG signal is valid or not. 0: Not valid. 1: Valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. 0: 60 lines. 1: 120 lines.	
	-	5:0	Reserved.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	ATGSEL_VALUE_Q[7:0]	7:0	Atuto Gain value latch by Vsync pulse.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE_Q[9:8]	1:0	See description of '102F7Eh'.	
40h ~ 43h (102F80h ~ 102F86h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FDET_CHECK_EN	6	H/V sync status check enable.	
	FDET_H_INV	5	H sync invert.	
	FDET_V_INV	4	V sync invert.	
	FDET_VTOTAL_PIX_CNT_EN	3	V total count by pixel clock enable.	
	FDET_SYNC_SRC_SEL[1:0]	2:1	H/V sync source select for mode detection.	
	FDET_EN	0	New mode interlaced detect enable.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VWIDTH_TOR[7:0]	7:0	V sync pulse width tolerance.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	FDET_VTOTAL_TOR[7:0]	7:0	V total tolerance.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FDET_STATUS_INTLAC_DET2	2	Mode detect result 2.	
	FDET_STATUS_INTLAC_DET1	1	Mode detect result 1.	
	FDET_STATUS_INTLAC_DE	0	Mode detect result 0.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	T0			
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH0[7:0]	7:0	V sync pulse width 0.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH0[13:8]	5:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VWIDTH1[7:0]	7:0	V sync pulse width 1.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FDET_STATUS_VWIDTH1[13:8]	5:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[7:0]	7:0	V total report 0.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL0[23:16]	7:0	See description of '102F9Ah'.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL0[24]	0	See description of '102F9Ah'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[7:0]	7:0	V total report 1.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[15:8]	7:0	See description of '102F9Eh'.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL1[23:16]	7:0	See description of '102F9Eh'.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL1[24]	0	See description of '102F9Eh'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[7:0]	7:0	V total report 2.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL2[23:16]	7:0	See description of '102FA2h'.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL2[24]	0	See description of '102FA2h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[7:0]	7:0	V total report 3.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	FDET_STATUS_VTOTAL3[23:16]	7:0	See description of '102FA6h'.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FDET_STATUS_VTOTAL3[24]	0	See description of '102FA6h'.	
60h ~ 60h	**-**	**7:0**	**Default : -**	**Access : -**

IP1_M Register (Bank = 102F, Sub-bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	-	-	Reserved.

IP2_M Register (Bank = 102F, Sub-bank = 02)

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	0: IP 444. 1: IP 422.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VOUT_PROC	5	VOUT_PROC.	
	HOUT_PROC	4	HOUT_PROC.	
	DITH_10TO8_SEL	3	Use random noise or rounding for 10-bit to 8-bit.	
	DITH_10TO8_EN	2	Dither enable for 10-bits to 8-bits.	
	DYNAMIC_SC_EN	1	Dynamic scaling enable.	
	-	0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HFACIN[22:16]	6:0	See description of '102F08h'.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode. 0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	VSD_DUP_BLACK	5	Duplicate black line for last line when VSD is enabled.	
	PREV_DOWN_3D	4	PREV_DOWN_3D.	
	-	3:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x08**	**Access : R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP[1:0]	6:5	Cb/Cr swap for 444 to 422.	

IP2_M Register (Bank = 102F, Sub-bank = 02)

Index (Absolute)	Mnemonic	Bit	Description	
	YDELAY_EN	4	Y delay enable.	
	DE_DLY_WITH_Y	3	DE_DLY_WITH_Y.	
	YCDELAY_STEP[2:0]	2:0	Y/C delay pipe step.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	44TO42_DITH_EN	0	444 to 422 filter dith enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	FILL_BLACK_NUM[5:0]	5:0	Fill black number.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILL_BLACK_ACT	7	FILL_BLACK_ACT.	
	FILL_BLACK_CLR	6	Clear FILL_BLACK register manually.	
	-	5:0	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FORCE_OSD_HSK	4	Force IP2 to OSD in handshaking mode.	
	-	3	Reserved.	
	IP2_VS_SEL	2	0: Use IP1_VS to generate VS to OPVS. 1: Use MVOP_VS to generate VS to OPVS.	
	FORCE_PRE2LAST	1	0: Use original pre align. 1: Use VSD last valid as pre align.	
	MVOP_DIN_EN	0	0: Form YC delay. 1: Data is form MVOP.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0xD0**	**Access : R/W**
	H_TOTAL[7:0]	7:0	Patgen h total.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	H_TOTAL[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0xE0**	**Access : R/W**
	V_TOTAL[7:0]	7:0	Patgen v total.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	V_TOTAL[11:8]	3:0	See description of '102F24h'.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x40**	**Access : R/W**
	H_BLOCK[7:0]	7:0	Patgen h block.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_BLOCK[9:8]	1:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x20**	**Access : R/W**
	V_BLOCK[7:0]	7:0	Patgen v block.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	V_BLOCK[9:8]	1:0	See description of '102F28h'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xF2**	**Access : R/W**
	HSD_YT0_C0[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x1F**	**Access : R/W**
	HSD_YT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x5E**	**Access : R/W**
	HSD_YT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xF4**	**Access : R/W**
	HSD_YT1_C0[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y0. Format: S7 of 2's complement (-31 <= Y0 <= 31).	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x0C**	**Access : R/W**
	HSD_YT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x5A**	**Access : R/W**
	HSD_YT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 255).	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x37**	**Access : R/W**
	HSD_YT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y3. Format: Fix 8 (0 <= Y3 <= 255).	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0xF5**	**Access : R/W**
	HSD_YT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y4. Format: S7 of 2's complement (-63 <= Y4 <= + 63).	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0xFA**	**Access : R/W**
	HSD_YT1_C5[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient Y5. Format: S7 of 2's complement (-31 < Y5 <= 31).	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xF7**	**Access : R/W**
	HSD_YT2_C0[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y0. Format: S7 of 2's complement (-15 <= Y0 <= 15).	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFE**	**Access : R/W**
	HSD_YT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y1. Format: S7 of 2's complement (-63 <= Y1 <= 63).	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_YT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient Y2. Format: Fix 8 (0 <= Y2 <= 127).	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x17**	**Access : R/W**
	HSD_CT0_C1[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x52**	**Access : R/W**
	HSD_CT0_C2[7:0]	7:0	Up-sample 1st pix (oxxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x0B**	**Access : R/W**
	HSD_CT1_C1[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x4B**	**Access : R/W**
	HSD_CT1_C2[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C2. Format: Fix 8 (0 <= C2 <= 255).	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x29**	**Access : R/W**
	HSD_CT1_C3[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C3. Format: Fix 8 (0 <= C3 <= 255).	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x01**	**Access : R/W**
	HSD_CT1_C4[7:0]	7:0	Up-sample 2nd pix (xoxx) coefficient C4. Format: S7 of 2's complement (-63 <= C4 <= + 63).	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x04**	**Access : R/W**
	HSD_CT2_C1[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C1. Format: S7 of 2's complement (-63 <= C1 <= 63).	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x3C**	**Access : R/W**
	HSD_CT2_C2[7:0]	7:0	Up-sample 3rd pix (xxox) coefficient C2.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Format: Fix 8 (0 <= C2 <= 127).	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:0	Reserved.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_IN_NUM_USR[7:0]	7:0	IP2 VSD input line count number.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VIN_CTRL_EN	7	IP2 VSD input line count control enable.	
	VSD_IN_USR_EN	6	IP2 VSD input line count number setting enable.	
	-	5	Reserved.	
	VSD_IN_NUM_USR[12:8]	4:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_OUT_NUMBER[7:0]	7:0	IP2 VSD output line count number.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VOUT_CTRL_EN	4	IP2 VSD output line count control enable.	
	-	3	Reserved.	
	VSD_OUT_NUMBER[10:8]	2:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_USR_VACT_VIDEO[7:0]	7:0	VSD user mode V_ACTIVE region.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSD_USR_VACT_VIDEO_EN	7	VSD user mode V_ACTIVE region enable.	
	-	6:5	Reserved.	
	VSD_USR_VACT_VIDEO[12:8]	4:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	VSD_VACT_VIDEO_READ[7:0]	7:0	VSD user mode V_ACTIVE region.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	VSD_VACT_VIDEO_READ[1	4:0	See description of '102F72h'.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	2:8]			
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	READ_HSD_OUT_CNT[11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	READ_VSD_OUT_CNT[12:8]	4:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PREFLT_ALPHA_EN	7	IP2 Pre-Filter alpha blending enable.	
	-	6:5	Reserved.	
	PREFLT_ALPHA[4:0]	4:0	IP2 Pre-Filter alpha blending for original and filter.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PRE_Y_TAP0[3:0]	3:0	IP2 Pre-Filter coefficient 0 [s.3].	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_FILTER_EN	7	IP2 Pre-Filter enable.	
	FIR_DITH_EN	6	IP2 Pre-Filter dith enable.	
	-	5:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PRE_Y_TAP1[6:0]	6:0	IP2 Pre-Filter coefficient 1 [s.6].	
4Ah	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7	Reserved.	
	PRE_Y_TAP2[6:0]	6:0	IP2 Pre-Filter coefficient 2 [s.6].	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP3[7:0]	7:0	IP2 Pre-Filter coefficient 3 [s.7].	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP4[7:0]	7:0	IP2 Pre-Filter coefficient 4 [s.8].	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PRE_Y_TAP4[8]	0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP5[7:0]	7:0	IP2 Pre-Filter coefficient 5 [s.9].	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP5[9:8]	1:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PRE_Y_TAP6[7:0]	7:0	IP2 Pre-Filter coefficient 6 [0.10].	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	PRE_Y_TAP6[9:8]	1:0	See description of '102F9Ch'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GOP_REQ_CNT[4:0]	4:0	In MVOP handshake mode, gen GOP needs timing.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP2GOP_SRC_SEL	7	For GOPD SRC of IP2. 0: IP2IN. 1: IP2OUT.	
	-	6:0	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADJ_HI_PRI[7:0]	7:0	Adjust memory priority.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PSEUDO_STOP	0	Enable b pseudo blanking.	
61h	**REG102FC2**	**7:0**	**Default : 0x08**	**Access : R/W**

IP2_M Register (Bank = 102F, Sub-bank = 02)

Index (Absolute)	Mnemonic	Bit	Description	
	LB_SPLIT_BLANK[7:0]	7:0	LB pseudo blank cycle.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x18**	**Access : R/W**
	PRE_ADJ_SPLIT_BLANK[7:0]	7:0	Adj pseudo blank cycle.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EXT_LR_EN	4	Enable external LR signal.	
	-	3:1	Reserved.	
	INIT_3D_STAT	0	Initialize 3D stat.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	WAIT_LEFT_FRM_INV	5	WAIT_RIGHT_FRM.	
	WAIT_LEFT_FRM	4	WAIT_LEFT_FRM.	
	-	3:1	Reserved.	
	EXT_LR_INV	0	Inverse external LR signal.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	INI_LR_IDX	4	0: L is the first frame. 1: R is the first frame.	
	-	3	Reserved.	
	ADJ_FORCE_EN	2	Adj bypass enable.	
	LR_CHG_MODE[1:0]	1:0	0: Line. 1: Block. 2: Frame.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAX_LOOP[2:0]	6:4	3D mode setting.	
	-	3:1	Reserved.	
	SPLIT_HALF	0	Split 1 frame into 2 frame.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	VACT_SPC_EN[1:0]	5:4	3D mode setting.	
	-	3	Reserved.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MASK_EN[2:0]	2:0	3D mode setting.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	GEN_VS_ACT[3:0]	7:4	Enable gen pseudo vsync in 3D.	
	GEN_VS_EN[3:0]	3:0	Enable gen pseudo vsync in 3D.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_VIDEO[7:0]	7:0	V_ACTIVE region.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_VIDEO[12:8]	4:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_SPC_0[7:0]	7:0	V blanking between field1&field2 or field3&field4.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_SPC_0[12:8]	4:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	VACT_SPC_1[7:0]	7:0	V blanking between field2&field3.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VACT_SPC_1[12:8]	4:0	See description of '102FCEh'.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0xC0**	**Access : R/W**
	LB_AUTO	7	LB_AUTO.	
	VSD_FAC_AUTO_RST_EN	6	VSD 3D auto factor reset mode enable.	
	AUTO_VACT_VIDEO_RST	5	AUTO VACT_VIDEO mode reset.	
	-	4:0	Reserved.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_OUTACK	1	Enable DAT_ADJ to src force ready.	
	ADJ_AUTO	0	ADJ_AUTO.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[7:0]	7:0	Debug.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	DATA_ADJ_DEBUG[15:8]	7:0	See description of '102FD2h'.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : RO**
	FIFO_DIFF[7:0]	7:0	Number of fifo.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	FIFO_DIFF[8]	0	See description of '102FD4h'.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LR_ALT_LINE	2	LR_ALT_LINE.	
	LR_FST_PIX	1	LR_FST_PIX.	
	PIX_SEP_EN	0	PIX_SEP_EN.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	HALF_PIX[7:0]	7:0	HALF_PIX.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	HALF_PIX[10:8]	2:0	See description of '102FD8h'.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSP_PH0_COEF0[7:0]	7:0	RSP_PH0_COEF0.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x80**	**Access : R/W**
	RSP_PH0_COEF1[7:0]	7:0	RSP_PH0_COEF1.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x40**	**Access : R/W**
	RSP_PH1_COEF0[7:0]	7:0	RSP_PH1_COEF0.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x40**	**Access : R/W**
	RSP_PH1_COEF1[7:0]	7:0	RSP_PH1_COEF1.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0xAA**	**Access : R/W**
	RSP_LINE7_PH	7	RSP_LINE7_PH.	
	RSP_LINE6_PH	6	RSP_LINE6_PH.	
	RSP_LINE5_PH	5	RSP_LINE5_PH.	
	RSP_LINE4_PH	4	RSP_LINE4_PH.	
	RSP_LINE3_PH	3	RSP_LINE3_PH.	
	RSP_LINE2_PH	2	RSP_LINE2_PH.	
	RSP_LINE1_PH	1	RSP_LINE1_PH.	
	RSP_LINE0_PH	0	RSP_LINE0_PH.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	RSP_FIELD_USR_EN	6	Re-sample local toggle field flag.	
	RSP_FIELD_INV	5	Re-sample field polarity invert.	
	RSP_FIELD_EN	4	Re-sample field mode.	
	-	3:1	Reserved.	
	RESAMP_EN	0	RESAMP_EN.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DUMMY_CLR[7:0]	7:0	DUMMY_CLR.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_CLR[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[7:0]	7:0	SBS half width.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY_SET[15:8]	7:0	See description of '102FFEh'.	

PNR Register (Bank = 102F, Sub-bank = 05)

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F1	7	Sub Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F1	6	Sub Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F1	5	Sub Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F1	4	Sub Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F1	3	Sub Window Post Noise Reduction for Y.	
	PNR_ENC_F1	2	Sub Window Post Noise Reduction for C.	
	RATIOYC_F1[1:0]	1:0	Sub Window Motion Ratio.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_MODE_SEL_F1	7	Sub Window C average mode selection when dotline cycle.	
	FIELD_AVG_Y_MODE_SEL_F1	6	Sub Window Y average mode selection when dotline cycle.	
	-	5:1	Reserved.	
	SEL_NEXT_FIELD_INV_F1	0	Sub Window select next field inverter for NOC_SEL.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F1	7	Sub Window DHD 3f mode enable.	
	PCCS_3F_EN_F1	6	Sub Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F1	4	Sub Window PCCS dither enable.	
	DHD_DITHER_EN_F1	3	Sub Window DHD dither enable.	
	PNR_BYPASS_F1	2	Sub Window PNR function bypass enable.	
	NR_EN_F1	1	Sub Window Post NR enable.	
	PCCS_EN_F1	0	Sub Window Post CCS enable.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PAL_EN_F1	6	Sub Window PAL enable.	
	-	5:0	Reserved.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F1[2:	7:5	Sub Window user-defined C motion threshold value.	

PNR Register (Bank = 102F, Sub-bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
	0]			
	POS_MOTIONY_TH1_F1[2:0]	4:2	Sub Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F1	1	Sub Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F1	0	Sub Window user-defined Y motion threshold enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F1	6	Sub Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F1	5	Sub Window enable select max motion for c.	
	YMOT_MAX_SEL_F1	4	Sub Window enable select max motion for y.	
	CMOT_DIV_MODE_F1[1:0]	3:2	Sub Window C motion divide mode.	
	YMOT_DIV_MODE_F1[1:0]	1:0	Sub Window Y motion divide mode.	
0Bh (102F16h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	DITHER_FRAME_RST_CNT[1:0]	2:1	Dither frame reset count.	
	DITHER_FRAME_RST_EN	0	Dither frame reset enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_F2[1:0]	1:0	Main Window Motion Ratio.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_AVG_C_MODE_SEL_F2	7	Main Window C average mode selection when dotline cycle.	
	FIELD_AVG_Y_MODE_SEL_F2	6	Main Window Y average mode selection when dotline cycle.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	5:1	Reserved.	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for NOC_SEL.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x18**	**Access : R/W**
	DHD_3F_EN_F2	7	Main Window DHD 3f mode enable.	
	PCCS_3F_EN_F2	6	Main Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F2	4	Main Window PCCS dither enable.	
	DHD_DITHER_EN_F2	3	Main Window DHD dither enable.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x80**	**Access : R/W**
	-	7	Reserved.	
	PAL_EN_F2	6	Main Window PAL enable.	
	-	5:0	Reserved.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for c.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window c motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window y motion divide mode.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F2	5	Main Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F2	4	Main Window DHD Interleaved History MR enable.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DHD_CMR_IIR_EN_F2	3	Main Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F2	2	Main Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F2	1	Main Window DHD YMR02 enable.	
	DHD_EN_F2	0	Main Window DHD enable.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F1	5	Sub Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F1	4	Sub Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F1	3	Sub Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F1	2	Sub Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F1	1	Sub Window DHD YMR02 enable.	
	DHD_EN_F1	0	Sub Window DHD enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x1C**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR02_TH[5:0]	5:0	DHD YMR02 threshold.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR02_GAIN[2:0]	2:0	DHD YMR02 gain.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_YMR04_TH[5:0]	5:0	DHD YMR04 threshold.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_YMR04_GAIN[2:0]	2:0	DHD YMR04 gain.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_CVAL_GAIN[7:0]	7:0	DHD C value gain.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_DIFFPIX_GAIN[3:0]	3:0	DHD pixel diff gain.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_CMR02_TH[5:0]	5:0	DHD C motion02 threshold.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR02_GAIN[2:0]	2:0	DHD C motion02 gain.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	DHD_CMR04_TH[5:0]	5:0	DHD C motion04 threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	DHD_CMR04_GAIN[2:0]	2:0	DHD C motion04 gain.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x30**	**Access : R/W**
	DHD_CEDGE_GAIN[7:0]	7:0	DHD C edge gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x40**	**Access : R/W**
	DHD_YEDGE_GAIN[7:0]	7:0	DHD Y edge gain.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_DEBUG0_EN	7	DHD debug0 enable.	
	DHD_DEBUG1_EN	6	DHD debug1 enable.	
	-	5:0	Reserved.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_YMR_IIR_ALPHA[2:0]	6:4	DHD YMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_YMR_IIR_STEP[1:0]	1:0	DHD YMR IIR step.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x63**	**Access : R/W**
	-	7	Reserved.	
	DHD_CMR_IIR_ALPHA[2:0]	6:4	DHD CMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_CMR_IIR_STEP[1:0]	1:0	DHD CMR IIR step.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_CEDGE_TH[7:0]	7:0	DHD C edge threshold.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	DHD_YEDGE_TH[7:0]	7:0	DHD Y edge threshold.	
2Bh	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**

PNR Register (Bank = 102F, Sub-bank = 05)

Index (Absolute)	Mnemonic	Bit	Description	
	DHD_CVAL_TH[7:0]	7:0	DHD C value threshold.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	DHD_USER_W[3:0]	3:0	DHD user weight of final result.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLEY[7:0]	7:0	PNR Table Y.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLEY[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x12**	**Access : R/W**
	PNR_TABLEY[23:16]	7:0	See description of '102F60h'.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY[31:24]	7:0	See description of '102F60h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY[39:32]	7:0	See description of '102F60h'.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY[47:40]	7:0	See description of '102F60h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY[55:48]	7:0	See description of '102F60h'.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEY[63:56]	7:0	See description of '102F60h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLEC[7:0]	7:0	PNR Table C.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x22**	**Access : R/W**
	PNR_TABLEC[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x12**	**Access : R/W**
	PNR_TABLEC[23:16]	7:0	See description of '102F80h'.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC[31:24]	7:0	See description of '102F80h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC[39:32]	7:0	See description of '102F80h'.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC[47:40]	7:0	See description of '102F80h'.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC[55:48]	7:0	See description of '102F80h'.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	PNR_TABLEC[63:56]	7:0	See description of '102F80h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_YMR04_GAIN[4:0]	4:0	CCS Y motion gain of diff of cur and ext.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_YMR04_TH[4:0]	4:0	CCS Y motion threshold of diff of cur and ext.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_YMR02_24_GAIN[4:0]	4:0	CCS Y motion 02 24 gain.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_YMR02_24_TH[4:0]	4:0	CCS Y motion 02 24 threshold.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	CCS_CMR04_GAIN[3:0]	3:0	CCS C motion 04 gain.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CMR04_TH[4:0]	4:0	CCS C motion 04 threshold.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	CCS_CMR02_24_GAIN[3:0]	3:0	CCS C motion 02 24 gain.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CMR02_24_TH[4:0]	4:0	CCS C motion 02 24 threshold.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CRCE_GAIN[4:0]	4:0	CCS C real edge gain.	
50h	**REG102FA1**	**7:0**	**Default : 0x11**	**Access : R/W**

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	CCS_CRCE_TH[4:0]	4:0	CCS C real edge threshold.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:6	Reserved.	
	CCS_YEDGE_GAIN[5:0]	5:0	CCS Y edge gain.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CCS_YEDGE_TH[7:0]	7:0	CCS Y edge threshold.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x05**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CSAT_GAIN[4:0]	4:0	CCS C saturation gain.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x11**	**Access : R/W**
	-	7:5	Reserved.	
	CCS_CSAT_TH[4:0]	4:0	CCS C saturation threshold.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	CCS_USER_W[3:0]	3:0	CCS user weight of final result.	
78h ~ 78h (102FF0h ~ 102FF1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

DNR Register (Bank = 102F, Sub-bank = 06)

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_DNR_CORE_EN	1	F2 DNR CORE FUNCTION EN.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) FUNCTION EN.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	F2_NR_TABLE_SEL_C	1	F2 DNR Table C Mapping Select. 0: Non-linear. 1: Linear.	
	F2_NR_TABLE_SEL_Y	0	F2 DNR Table Y Mapping Select. 0: Non-linear. 1: Linear.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SNR_MD_MODE_EN	1	F2 SNR Motion Mode EN.	
	SNR_EN	0	F2 SNR FUNCTION EN.	
24h (102F48h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_ROUND_MODE_C[1:0]	3:2	F2 DNR C blend rounding select. 00: Add 0. 01: Add dither. 10: Add dither. 11: Add dither.	
	F2_ROUND_MODE_Y[1:0]	1:0	F2 DNR Y blend rounding select. 00: Add 0. 01: Add dither. 10: Add dither. 11: Add dither.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	F2_MAX_MOT_ENABLE_C	3	F2_MAX_MOT_ENABLE_C.	
	F2_MAX_MOT_ENABLE_Y	2	F2_MAX_MOT_ENABLE_Y.	

DNR Register (Bank = 102F, Sub-bank = 06)

Index (Absolute)	Mnemonic	Bit	Description	
	F2_DNR_FILTER_EN_C	1	F2_DNR_FILTER_EN_C.	
	F2_DNR_FILTER_EN_Y	0	F2_DNR_FILTER_EN_Y.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_DIV0_C[2:0]	7:5	F2_DNR_FILTER_DIV0_C.	
	F2_DNR_FILTER_DIV0_Y[2:0]	4:2	F2_DNR_FILTER_DIV0_Y.	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_DNR_FILTER_MODE_C[1:0]	7:6	F2_DNR_FILTER_MODE_C.	
	F2_DNR_FILTER_MODE_Y[1:0]	5:4	F2_DNR_FILTER_MODE_Y.	
	F2_DNR_FILTER_DIV1_C[1:0]	3:2	F2_DNR_FILTER_DIV1_C.	
	F2_DNR_FILTER_DIV1_Y[1:0]	1:0	F2_DNR_FILTER_DIV1_Y.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SNR_SHARP_LEVEL[3:0]	3:0	SNR sharpness level.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0xBD**	**Access : R/W**
	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x79**	**Access : R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x56**	**Access : R/W**
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x34**	**Access : R/W**
	DNR_TABLEC_1[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x12**	**Access : R/W**
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '102F8Eh'.	
58h ~ 71h (102FB0h ~ 102FE2h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	F2_WIN_EN	0	F2 DNR/SNR active window enable.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_XSTART[7:0]	7:0	F2 DNR/SNR active window start X.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XSTART[10:8]	2:0	See description of '102FE8h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	F2_WIN_YSTART[7:0]	7:0	F2 DNR/SNR active window start Y.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	F2_WIN_YSTART[10:8]	2:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x68**	**Access : R/W**
	F2_WIN_XEND[7:0]	7:0	F2 DNR/SNR active window end X.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_XEND[10:8]	2:0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0xF0**	**Access : R/W**
	F2_WIN_YEND[7:0]	7:0	F2 DNR/SNR active window end Y.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	F2_WIN_YEND[10:8]	2:0	See description of '102FEEh'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_HCNT_F2[7:0]	7:0	F2 hcnt for debug.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	STATUS_HCNT_F2[10:8]	2:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_VCNT_F2[7:0]	7:0	F2 vcnt for debug.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	STATUS_CLR_F2	7	F2 DEBUG STATUS CLEAR.	
	-	6:3	Reserved.	
	STATUS_VCNT_F2[10:8]	2:0	See description of '102FF6h'.	

FILM Register (Bank = 102F, Sub-bank = 0A)

FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h ~ 02h (102F04h ~ 102F05h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_CUR_ERROR_TH_F2[7:0]	7:0	32 current error threshold.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	32_PRE_ERROR_TH_F2[15:8]	7:0	32 previous error threshold.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_CUR_ERROR_TH_F2[7:0]	7:0	22 current error threshold.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x04**	**Access : R/W**
	22_PRE_ERROR_TH_F2[15:8]	7:0	22 previous error threshold.	
05h ~ 05h (102F0Ah ~ 102F0Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	32_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	32 total error max th.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x7F**	**Access : R/W**
	32_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	32 total error sum th.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x08**	**Access : R/W**
	22_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	22 total error max th.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x7F**	**Access : R/W**
	22_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	22 total error sum th.	
08h ~ 10h (102F10h ~ 102F20h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h	**REG102F21**	**7:0**	**Default : 0x0C**	**Access : R/W**

FILM Register (Bank = 102F, Sub-bank = 0A)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	FILM32_EN_F2	7	F2 32 film mode enable.
	FILM22_EN_F2	6	F2 22 film mode enable.
	-	5:4	Reserved.
	PRE32_F2	3	F2 pre32.
	PRE32_F1	2	F1 pre32.
	-	1:0	Reserved.
50h ~ 5Ah (102FA0h ~ 102FB5h)	**-**	**7:0**	**Default : -** **Access : -**
	-	-	Reserved.
11h ~ 43h (102F22h ~ 102F87h)	**-**	**7:0**	**Default : -** **Access : -**
	-	-	Reserved.

SNR Register (Bank = 102F, Sub-bank = 0C)

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_TEST_EN	7	De-blocking test mode.	
	-	6:5	Reserved.	
	DBK_EN_F1	4	De-blocking enable F1.	
	-	3	Reserved.	
	DBK_EN_V_F2	2	Vertical de-blocking enable F2.	
	DBK_EN_H_F2	1	Horizontal de-blocking enable F2.	
	DBK_EN_F2	0	De-blocking enable F2.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x05**	**Access : R/W**
	DBK_STD_LOW_THRD[7:0]	7:0	De-blocking active threshold.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x08**	**Access : R/W**
	DBK_ALPHA_STEP[2:0]	7:5	De-blocking alpha step.	
	-	4	Reserved.	
	DBK_STRENGTH_GAIN_F2[3:0]	3:0	De-blocking strength F2 (.xxxx).	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_MOTION_RATIO_EN_F2	4	De-blocking motion ratio enable F2.	
	-	3:0	Reserved.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0xEF**	**Access : R/W**
	DBK_TABLE_01[7:0]	7:0	De-blocking LUT_01.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0xCD**	**Access : R/W**
	DBK_TABLE_23[7:0]	7:0	De-blocking LUT_23.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xAB**	**Access : R/W**
	DBK_TABLE_45[7:0]	7:0	De-blocking LUT_45.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x89**	**Access : R/W**
	DBK_TABLE_67[7:0]	7:0	De-blocking LUT_67.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x67**	**Access : R/W**
	DBK_TABLE_89[7:0]	7:0	De-blocking LUT_89.	
16h	**REG102F2D**	**7:0**	**Default : 0x45**	**Access : R/W**

SNR Register (Bank = 102F, Sub-bank = 0C)

Index (Absolute)	Mnemonic	Bit	Description	
	DBK_TABLE_AB[7:0]	7:0	De-blocking LUT_AB.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x23**	**Access : R/W**
	DBK_TABLE_CD[7:0]	7:0	De-blocking LUT_CD.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x01**	**Access : R/W**
	DBK_TABLE_EF[7:0]	7:0	De-blocking LUT_EF.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_INIT_1_F2[7:0]	7:0	De-blocking H counter initial value[7:0] F2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_INIT_2_F2[7:0]	7:0	De-blocking H counter initial value[15:8] F2.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_H_INIT_3_F2[3:0]	3:0	De-blocking H counter initial value[19:16] F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_INIT_4_F2[4:0]	4:0	De-blocking H counter initial value[24:20] F2.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_INIT_1_F2[7:0]	7:0	De-blocking V counter initial value[7:0] F2.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_INIT_2_F2[7:0]	7:0	De-blocking V counter initial value[15:8] F2.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_V_INIT_3_F2[3:0]	3:0	De-blocking V counter initial value[19:16] F2.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_INIT_4_F2[4:0]	4:0	De-blocking V counter initial value[24:20] F2.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_RATIO_1_F2[7:0]	7:0	De-blocking H counter ratio[7:0] F2.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_H_RATIO_2_F2[7:0]	7:0	De-blocking H counter ratio[15:8] F2.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_H_RATIO_3_F2[3:0]	3:0	De-blocking H counter ratio[19:16] F2.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_RATIO_4_F2[4:0]	4:0	De-blocking H counter ratio[24:20] F2.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_RATIO_1_F2[7:0]	7:0	De-blocking V counter ratio[7:0] F2.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_V_RATIO_2_F2[7:0]	7:0	De-blocking V counter ratio[15:8] F2.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DBK_V_RATIO_3_F2[3:0]	3:0	De-blocking V counter ratio[19:16] F2.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_RATIO_4_F2[4:0]	4:0	De-blocking V counter ratio[24:20] F2.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_BLOCK_WIDTH_F2 [4:0]	4:0	H block width F2.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BLOCK_WIDTH_F2 [4:0]	4:0	V block width F2.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_BOUNDARY_LEFT_ F2[4:0]	4:0	H block left boundary F2.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_H_BOUNDARY_RIGH T_F2[4:0]	4:0	H block right boundary F2.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x06**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BOUNDARY_UP_F2 [4:0]	4:0	V block up boundary F2.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DBK_V_BOUNDARY_DOWN_F2[4:0]	4:0	V block down boundary F2.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SNR_EN_F1	4	SNR enable F1.	
	-	3:2	Reserved.	
	SNR_MOTION_RATIO_EN_F2	1	SNR motion ratio enable F2.	
	SNR_EN_F2	0	SNR enable F2.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x0A**	**Access : R/W**
	SNR_STD_LOW_THRD[7:0]	7:0	SNR active threshold.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x48**	**Access : R/W**
	SNR_ALPHA_STEP[2:0]	7:5	SNR alpha step.	
	-	4	Reserved.	
	SNR_STRENGTH_GAIN_F2[3:0]	3:0	SNR strength F2.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0xCF**	**Access : R/W**
	SNR_TABLE_01[7:0]	7:0	SNR LUT_01.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x69**	**Access : R/W**
	SNR_TABLE_23[7:0]	7:0	SNR LUT_23.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x24**	**Access : R/W**
	SNR_TABLE_45[7:0]	7:0	SNR LUT_45.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x01**	**Access : R/W**
	SNR_TABLE_67[7:0]	7:0	SNR LUT_67.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_89[7:0]	7:0	SNR LUT_89.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_AB[7:0]	7:0	SNR LUT_AB.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_CD[7:0]	7:0	SNR LUT_CD.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_TABLE_EF[7:0]	7:0	SNR LUT_EF.	
38h ~ 38h (102F70h ~ 102F71h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x07**	**Access : R/W**
	-	7:3	Reserved.	
	DBK_BKN_INTERVAL_IIR_ALPHA_F2[2:0]	2:0	De-blocking blockiness interval IIR alpha strength F2.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7	Reserved.	
	DBK_BLOCKINESS_INTERVAL_IIR_EN_F2	6	De-blocking blockiness interval IIR enable F2.	
	DBK_BLOCKINESS_PIXEL_EN_F2	5	De-blocking blockiness pixel active enable F2.	
	-	4	Reserved.	
	DBK_COARSE_STEP_F2[1:0]	3:2	De-blocking coarse detect step F2.	
	DBK_BK_PULSE_FILTER_EN_F2	1	De-blocking blockiness pulse filter enable F2.	
	DBK_BLOCKINESS_EN_F2	0	De-blocking blockiness detect enable F2.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x03**	**Access : R/W**
	DBK_COARSE_LOW_THRD_F2[7:0]	7:0	De-blocking coarse active threshold F2.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x42**	**Access : R/W**
	-	7	Reserved.	
	DBK_BLOCKINESS_IIR_GAIN_F2[2:0]	6:4	De-blocking blockiness IIR gain F2.	
	-	3	Reserved.	
	DBK_SIDE_STEP_F2[1:0]	2:1	De-blocking side detect step F2.	
	-	0	Reserved.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	DBK_SIDE_LOW_THRD_F2[7:0]	7:0	De-blocking side active threshold F2.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x22**	**Access : R/W**
	-	7:6	Reserved.	
	DBK_BLOCKINESS_STEP_F2[1:0]	5:4	De-blocking blockiness strength step F2.	
	-	3:0	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_14	7	Reserved.	
	SNR_NM_C_FILTER_EN_F1	6	Noise masking chroma enable F1.	
	-	5	Reserved.	
	SNR_NM_FILTER_EN_F1	4	Noise masking enable F1.	
	-	3	Reserved.	
	SNR_NM_C_FILTER_EN_F2	2	Noise masking chroma enable F2.	
	SNR_NM_MOTION_RATIO_EN_F2	1	Noise masking motion ratio enable F2.	
	SNR_NM_FILTER_EN_F2	0	Noise masking enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_15[1:0]	7:6	Reserved.	
	-	5:4	Reserved.	
	RESERVED_SNR_5[1:0]	3:2	Reserved.	
	-	1:0	Reserved.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SNR_MR_LPF_EN_F2	0	De-blocking and SNR motion ratio low pass filter enable F2 (LPF is 3x3 mask).	
51h ~ 53h (102FA3h ~ 102FA6h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_9[1:0]	7:6	Reserved.	
	SNR_NM_GAIN_F2[5:0]	5:0	Noise masking gain F2.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_SNR_10[1:0]	7:6	Reserved.	
	-	5:0	Reserved.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SNR_NM_MIN_THRD[3:0]	7:4	Noise masking min threshold bound.	
	SNR_NM_MAX_THRD[3:0]	3:0	Noise masking max threshold bound.	
55h (102FABh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x10**	**Access : R/W**
	SNR_MOTION_TABLE_01[7:0]	7:0	De-blocking and SNR motion ratio LUT_01.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x32**	**Access : R/W**
	SNR_MOTION_TABLE_23[7:0]	7:0	De-blocking and SNR motion ratio LUT_23.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x54**	**Access : R/W**
	SNR_MOTION_TABLE_45[7:0]	7:0	De-blocking and SNR motion ratio LUT_45.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x76**	**Access : R/W**
	SNR_MOTION_TABLE_67[7:0]	7:0	De-blocking and SNR motion ratio LUT_67.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x98**	**Access : R/W**
	SNR_MOTION_TABLE_89[7:0]	7:0	De-blocking and SNR motion ratio LUT_89.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SNR_MOTION_TABLE_AB[7:0]	7:0	De-blocking and SNR motion ratio LUT_AB.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SNR_MOTION_TABLE_CD[7:0]	7:0	De-blocking and SNR motion ratio LUT_CD.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SNR_MOTION_TABLE_EF[7:0]	7:0	De-blocking and SNR motion ratio LUT_EF.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SNR_FUN_BYPASS_EN	0	SNR function bypass enable.	
70h ~ 7Bh (102FE1h ~	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SNR Register (Bank = 102F, Sub-bank = 0C)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**

S_VOP Register (Bank = 102F, Sub-bank = 0F)

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:1	Reserved.	
	MW_BD_REG_EN	0	Main Window Border Register Enable. 0: Sub window Border register enable. 1: Main window Border register Enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDLO_BO[3:0]	7:4	Main window border outside height of Left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.	
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.	
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.	
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.	
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.	
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.	
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.	
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.	
	-	3:2	Reserved.	
	181FWINSEL[1:0]	1:0	18h~1Fh Display Window Select. 00: 1st window. 01: 2nd window. 10: 3rd window. 11: 4th window.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST[7:0]	7:0	Sub window Horizontal Start.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST[7:0]	7:0	Sub window Vertical Star.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND[7:0]	7:0	Sub window Vertical End.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	S_VDEEND[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	See description of '102F20h'.	
11h	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_3RD[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEST_4TH[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_HDEEND_4TH[11:8]	3:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	S_VDEEND_4TH[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWBCOL[7:0]	7:0	Sub Window Border Color.	
17h	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_HBC_GAIN[3:0]	7:4	HBC gain for sub window.	
	S_HBC_EN	3	HBC function enable for sub window.	
	S_HBC_ROUNDING	2	HBC rounding enable for sub window.	
	-	1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
19h ~ 1Ah (102F32h ~ 102F35h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	KSTPD[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	CM31[12:8]	4:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control. 0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SMEN	7	SVM Main window Enable.	
	SMTE	6	SVM Main window Tap Enable.	
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: 4 taps. 11: 5 taps.	
	SSWEN	3	SVM Sub window Enable.	
	SSWETE	2	SVM Sub window Tap Enable.	
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.	
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.	
	SVMBYS[1:0]	5:4	SVM Bypass Y Select. 0x: SMV data. 10: Original Y data. 11: Y with tap filter.	
	SCORING[3:0]	3:0	SVM Coring.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SVMLMT[7:0]	7:0	SVM Limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM Main window Step.	
	SMGAIN[3:0]	3:0	SVM Main window Gain.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM Sub window Step.	
	SWGAIN[3:0]	3:0	SVM Sub window Gain.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM Pipe Adjust.	
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SVM_SEP_DLY	7	SVM Separate Delay Enable.	
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	C1080I	7	1080i mode. 0: Follow DE. 1: Follow HSYNC.	
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.	
	IPFI	5	To Pad Field Invert enable.	
	I1440	4	Interlace 1440 mode. This bit works at frame SBPCM= 0. 0: Disable, horizontal valid pixel = 720; SVM support. 1: Enable, horizontal valid pixel = 1440; does not support SVM.	
	IRDEN	3	Random 10 bit DAC Enable.	
	IHSRE	2	HSYNC Shift control. 0: Shift left. 1: Shift right.	
	IOFI	1	Interlace Output Field Invert.	
	IOEN	0	Interlace Output Enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.	
	-	3:0	Reserved.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	IP_FINV	7	IP Field Inverse.	
	IP_ITLC	6	IP Interlace.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SIM	5	Single Interlace Mode. 0: Disable. 1: Enable.	
	LPM	4	LVDS 10-bit Mode. 0: Disable. 1: Enable.	
	BES[1:0]	3:2	Border Extend for SVM.	
	OES[1:0]	1:0	OSD Extend for SVM.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSOFFS[7:0]	7:0	HSYNC Shift Offset.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.	
	RESERVED[1:0]	6:5	RESERVED.	
	-	4	Reserved.	
	HSOFFS[11:8]	3:0	See description of '102F58h'.	
2Dh ~ 2Fh (102F5Ah ~ 102F5Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_BRI_OFFSET[7:0]	7:0	Offset for R data.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	BRI_EN	7	Brightness enable (after gamma).	
	CON_EN	6	Contrast enable (after gamma).	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	G_BRI_OFFSET[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.	
32h	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_R[7:0]	7:0	Brightness offset (BRI_FUNCTION) for main window R.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_G[7:0]	7:0	Brightness offset (BRI_FUNCTION) for main window G.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	M_BRI_G[10:8]	2:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	M_BRI_B[7:0]	7:0	Brightness offset (BRI_FUNCTION) for main window B.	
38h	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_R[7:0]	7:0	Brightness offset (BRI_FUNCTION) for sub window R.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_G[7:0]	7:0	Brightness offset (BRI_FUNCTION) for sub window G.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	S_BRI_B[7:0]	7:0	Brightness offset (BRI_FUNCTION) for sub window B.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE0[7:0]	7:0	Check value for auto mload base0 R channel.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE0[11:8]	3:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_R_BASE1[7:0]	7:0	Check value for auto mload base1 R channel.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.	
	-	6:4	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GAMMA_MLOAD_CHECK_R_BASE1[11:8]	3:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE0[7:0]	7:0	Check value for auto mload base0 G channel.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE0[11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_G_BASE1[7:0]	7:0	Check value for auto mload base1 G channel.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_1	7	Base1 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE1[11:8]	3:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE0[7:0]	7:0	Check value for auto mload base0 B channel.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE0[11:8]	3:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAMMA_MLOAD_CHECK_B_BASE1[7:0]	7:0	Check value for auto mload base1 B channel.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE1[11:8]	3:0	See description of '102F82h'.	
42h ~ 45h (102F84h ~ 102F8Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAP_STAGE[3:0]	7:4	Capture stage selection. 0: VOP2_DP input data. 1: BRI output. 2: HBC output. 3: CON_BRI output. 4: FWC output. 5: Gamma output. 6: Noise dither output.	
	-	3:0	Reserved.	
46h (102F8Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F92h'.	
4Ah	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_CON_GAIN[11:8]	3:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_CON_GAIN[11:8]	3:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_CON_GAIN[11:8]	3:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F9Eh'.	
50h	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.	
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma CON_BRI.	
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.	
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.	
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FREEZ_VCNT_VALUE[10:8]	2:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when NEW_LOCK_POINT is set high.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LOCK_VCNT_VALUE[10:8]	2:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.	
	OTUPUT_FIELD_INV	4	Invert field for output reference signal.	
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.	
	IVS_SEL	2	Select INSERT_END point as input reference for frame PLL.	
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.	
	INPUT_FREEZ	0	V-counter freeze enable.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VCNT_FREEZ_REGION	7	In V-counter freeze status.	
	-	6:2	Reserved.	
	IVS_CNT[9:8]	1:0	Frame number for input reference generate.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for CCIR656 format.	
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for CCIR656 format.	
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.	
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.	
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.	
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.	
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.	
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.	
	NOISE_DITH_EN	5	Noise dither enable.	
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.	
	CAP_EN	3	Capture image to IP enable.	
	-	2:0	Reserved.	
58h	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. MAIN_R_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_R_MIN_LIMIT. MAIN_R_MIN_SIGN = 0: MAIN_R_MIN = MAIN_R_MIN_LIMIT.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. MAIN_G_MIN_SIGN = 1: MAIN_G_MIN = -MAIN_G_MIN_LIMIT. MAIN_G_MIN_SIGN = 0: MAIN_G_MIN = MAIN_G_MIN_LIMIT.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. MAIN_B_MIN_SIGN = 1: MAIN_R_MIN = -MAIN_B_MIN_LIMIT. MAIN_B_MIN_SIGN = 0: MAIN_R_MIN = MAIN_B_MIN_LIMIT.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)

Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value. S.12 format sign bit is bit-12. SUB_R_MIN_SIGN = 1: MAIN_R_MIN = -SUB_R_MIN_LIMIT. SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. SUB_G_MIN_SIGN = 1: MAIN_G_MIN = -SUB_G_MIN_LIMIT. SUB_G_MIN_SIGN = 0: MAIN_G_MIN = SUB_G_MIN_LIMIT.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '102FC2h'.	
62h	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. SUB_B_MIN_SIGN = 1: MAIN_R_MIN = -SUB_B_MIN_LIMIT. SUB_B_MIN_SIGN = 0: MAIN_R_MIN = SUB_B_MIN_LIMIT.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '102FC6h'.	
64h ~ 69h (102FC8h ~ 102FD3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[7:0]	7:0	New add function for RGB_COMPRESSION.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	RGB_COMPRESSION_MODE[15:8]	7:0	See description of '102FD8h'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	FWC_SUB_EN	4		
	-	3:2	Reserved.	
	FWC_DITHER_EN	1		
	FWC_MAIN_EN	0		
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	FWC_STRENGTH[3:0]	3:0		
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FWC_SLOPE[5:0]	5:0		

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	FWC_CTH[7:0]	7:0		
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[7:0]	7:0		
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[23:16]	7:0	See description of '102FE4h'.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[31:24]	7:0	See description of '102FE4h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[39:32]	7:0	See description of '102FE4h'.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[47:40]	7:0	See description of '102FE4h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[55:48]	7:0	See description of '102FE4h'.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[63:56]	7:0	See description of '102FE4h'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[71:64]	7:0	See description of '102FE4h'.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[79:72]	7:0	See description of '102FE4h'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[87:80]	7:0	See description of '102FE4h'.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_R[95:88]	7:0	See description of '102FE4h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[7:0]	7:0		
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[15:8]	7:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[23:16]	7:0	See description of '102FF4h'.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[31:24]	7:0	See description of '102FF4h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[39:32]	7:0	See description of '102FF4h'.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[47:40]	7:0	See description of '102FF4h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[55:48]	7:0	See description of '102FF4h'.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[63:56]	7:0	See description of '102FF4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[71:64]	7:0	See description of '102FF4h'.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[79:72]	7:0	See description of '102FF4h'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[87:80]	7:0	See description of '102FF4h'.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x80**	**Access : R/W**
	FWC_DELTA_B[95:88]	7:0	See description of '102FF4h'.	

VOP Register (Bank = 102F, Sub-bank = 10)

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND0[7:0]	7:0	20h: Recommended value (power on default value is 0).	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DB_MASK	0	Double buffer register mask signal. The double buffer register is updated when DB_MASK and DB_LOAD.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSST[7:0]	7:0	Output VSYNC start (only useful when AOVS= 1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	VSST_11	4	Output VSYNC[11] start (only useful when AOVS= 1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h - 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No Signal VSYNC. Registers 22h and 23h are used to define minimum H total.	
	VSST[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOVS= 1). 304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSEND[11:8]	3:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHST[7:0]	7:0	External VD Using Sync. 0: Sync is Generated from Data Internally.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Sync from External Source.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEHST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEHEND[7:0]	7:0	Output DE Horizontal END. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	DEHEND[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVST[7:0]	7:0	Output DE Vertical Start. 00: Default value.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSTSEL	7	Vertical Start Select. 0: DEVST[10:0] is Output DE vertical start. 1: DEVST[10:0] is Scaling Image Window vertical start.	
	-	6:4	Reserved.	
	DEVST[11:8]	3:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEVEND[7:0]	7:0	Output DE Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DEVEND[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start. 48h: Recommended value (power on default is 0).	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SIHST[12:8]	4:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SIHEND[12:8]	4:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVST[7:0]	7:0	Scaling Image window Vertical Start.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVST[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	SIVEND[7:0]	7:0	Scaling Image window Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SIVEND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDTOT[7:0]	7:0	Output Horizontal Total. 53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HDTOT[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDTOT[7:0]	7:0	Output Vertical Total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output.	
0Dh	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	-	7:4	Reserved.	
	VDTOT[11:8]	3:0	See description of '102F1Ah'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_BP[6:0]	7:1	Vsync back-porch setting.	
	VS_AUTO_BP	0	Auto vsync back-porch.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SHORT_LINE_GATE	0	Short lint gatting.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSEND[7:0]	7:0	20h: Recommended value (power on default value is 0).	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x4C**	**Access : R/W**
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 - 0x23).	
	OUTM	6	Output Mode. 0: Mode 0. 1: Mode 1.	
	HRSM	5	HSYNC Remove Mode. 0: Normal. 1: Remove HSYNC when GPOA (Bank 2 register0x62 - 0x6A) is low.	
	VSGP	4	VSYNC use GPO9. 0: Disable. 1: Enable (using Bank 2 register 0x59 - 0x61 to define OVSYNC).	
	EHTT	3	Even H Total. 0: Enable, Output H Total is always even pixels. 1: Disable, Output H Total is always odd pixels.	
	MOD2	2	Mode 2. 0: Disable. 1: Enable.	
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	ATCTRL function enable. 0: Disable.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLLMD0	7	Frame PLL Mode 0.	
	SL_TUNE_EN	6	Short line tune enable.	
	AUTO_H_TOTAL_UPDATE_EN	5	Enable update AUTO_H_TOTAL value to H_TOTAL.	
	-	4:2	Reserved.	
	SSC_SHIFT	1	0: Enable. 1: Disable.	
	CLKDIV2_POINT_SELECT	0	0: Original. 1: New.	
11h (102F23h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x20**	**Access : R/W**
	LCK_TH[7:0]	7:0	Frame PLL Lock Threshold.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x08**	**Access : R/W**
	LCK_TH[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x10**	**Access : R/W**
	FTNF[7:0]	7:0	Frame Tune Number of Frame.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	FTNS[3:0]	7:4	Tune Frame Number of Short-line tune.	
	-	3	Reserved.	
	PIP_REG_EN	2	PIP Register Enable.	
	FPLL_REP_EN	1	Frame PLL Report Enable.	
	NOISY_GEN	0	Noise Generator.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT1[7:0]	7:0	Frame PLL Limit.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT0[7:0]	7:0	Frame PLL Limit.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PFLL_LMT[7:0]	7:0	Frame PLL Limit.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_LMT_OFST0[7:0]	7:0	Frame PLL Limit Offset low byte.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_LMT_OFST1[7:0]	7:0	Frame PLL Limit Offset high byte.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0xF0**	**Access : R/W**
	M_HBC_GAIN[3:0]	7:4	Main window High brightness gain.	
	M_HBC_EN	3	Main window High brightness enable.	
	M_HBC_ROUNDING	2	Main window High brightness enable.	
	-	1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : RO**
	INTLX_VS_OFFSET[7:0]	7:0	The interlace vsync offset.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLX_VS_EN	5	Interlace vsync enable.	
	INTLX_VS_OFFSET[12:8]	4:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	BY_STAGE_VIP[3:0]	7:4	Vip report point stage.	
	BY_STAGE_OP2[3:0]	3:0	Report point stage.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	REP_RD_TRID	0	Report SW read trigger.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADEAD_EN	7	Ahead mode enable.	
	SWBLBK	6	Sub window Blue screen color. 0: Black color. 1: Blue color.	
	SWBLUE	5	Sub window Blue screen control. 0: Off. 1: On.	
	S_FMCLR_EN	4	Sub window frame color enable.	
	-	3	Reserved.	
	MBD_EN	2	Main window Border Enable.	
	MBLK	1	Main window Black screen control.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			0: Off. 1: On.	
	NOSC_EN	0	No Signal Color Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_R[7:0]	7:0	Frame Color - Red.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_G[7:0]	7:0	Frame Color - Green.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCL_B[7:0]	7:0	Frame Color - Blue.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x02**	**Access : R/W**
	DITHG[1:0]	7:6	Dither coefficient for G channel.	
	DITHB[1:0]	5:4	Dither coefficient for B channel.	
	SROT	3	Spatial coefficient Rotate. 0: Disable. 1: Enable.	
	TROT	2	Temporal coefficient Rotate. 0: Disable. 1: Enable.	
	OBN	1	Output Bits Number (used for 8/10-bit gamma). 0: 8-bit output. 1: 6-bit output (power on default value).	
	DITH	0	DITHer function. 0: Off. 1: On.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x2D**	**Access : R/W**
	TL[1:0]	7:6	Top - Left dither coefficient.	
	TR[1:0]	5:4	Top - Right dither coefficient.	
	BL[1:0]	3:2	Bottom - Left dither coefficient.	
	BR[1:0]	1:0	Bottom - Right dither coefficient.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_E_4_FRAME	7	Reset noise generator by frames enable.	
	NDMD	6	Noise Dithering Method.	
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.
	DT3	3	Dither Type 2 control. 0: Disable dither type 2. 1: Enable dither type 2.
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7	Reserved.
	SHORT_1LINE_DISABLE	6	1: Disable. 0: Enable.
	-	5	Reserved.
	EGWT	4	Encode Gamma Write.
	HTOTAL	3	H Total End 11.
	HDE_END	2	HDE End 11.
	HFDE_END	1	HFDE END 11.
	OUTFRR_EN0	0	Output Free-run Enable.
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x03** **Access : R/W**
	IVS_DIFF_THR[7:0]	7:0	Input vs Different Thresholds.
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x07** **Access : R/W**
	TUNE_FIELD_IP	7	Select insert point of one field for VOP_DISP inset signal.
	IVS_STB_THR[6:0]	6:0	Input vs Stable Thresholds.
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00** **Access : R/W**
	LMT_ADD_NMB[7:0]	7:0	Limit adjust Number in ACC_FPLL mode.
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00** **Access : R/W**
	FPLL_MD1	7	FPLL Mode 1.
	FPLL_DIS	6	FPLL Stop.

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	ACC1_SEL[1:0]	5:4	Select modify numbers. 00: 3/4 diff numbers. 01: 1/2 diff numbers. Others: 1/4 diff numbers.	
	-	3	Reserved.	
	ADD_LINE_SEL	2	Select Add Line into frame or pixel into line.	
	CH_CH_MD1	1	ACC FPLL Mode 1.	
	CH_CH_MD0	0	ACC FPLL Mode 0.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IVS_PRD_NUM[7:0]	7:0	Count Number per Input v.s.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	IVS_PRD_NUM[11:8]	3:0	See description of '102F3Eh'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	LCPS	7	LVDS Channel Polarity Swap (P/N swap). 0: Disable. 1: Enable.	
	LCS	6	LVDS Channel Swap. 0: Disable. 1: Enable. When enabled in dual LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap, LVB0M/LVB3M swap, LVB0P/LVB3P swap, LVB1M/LVBCKM swap, LVB1P/LVBCKP swap. When enabled in single LVDS: LVA0M/LVA3M swap, LVA0P/LVA3P swap, LVA1M/LVACKM swap, LVA1P/LVACKP swap.	
	MLXT0	5	MSB/LSB Exchange Type for 6/8/10-bit.	
	LTIM	4	LVDS TI Mode. 0: Normal. 1: TI Mode.	
	OMLX	3	Odd channel MSB/LSB Exchange. 0: Normal. 1: Exchange.	
	EMLX	2	Even channel MSB/LSB Exchange. 0: Normal.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
			1: Exchange.
	ORBX	1	Odd channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.
	ERBX	0	Even channel Red/Blue bus Exchange. 0: Normal. 1: Exchange.
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00** **Access : R/W**
	MLXT1	7	MSB/LSB Exchange Type for 6/8/10-bit.
	DOT	6	Differential Output Type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/Increased-swing RSDS.
	WHTS	5	White Screen (including Main window and Sub window). 0: Disable. 1: Enable.
	BLSK	4	Black Screen (including Main window and Sub window). 0: Disable. 1: Enable.
	REVERSE	3	REVERSE luminosity. 0: Off. 1: On.
	STO	2	Stagger Output (only used when DPO= 1). 0: Disable. 1: Enable.
	DPX	1	A/B Port Swap (only used when DPO= 1). 0: Disable. 1: Enable.
	DUAL_PIXEL_OUTPUT	0	Dual Pixel Output. 0: Single pixel. 1: Dual pixel.
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:6	Reserved.
	AB_SWAP	5	LVDS AB Port Swap.
	CKSEL[4:0]	4:0	Enable clock of internal control. 00h: TTL output. 11H: Single LVDS output.

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			13h: Dual LVDS output.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBLALL_SET	7	Frame buffer less all set.	
	PUT_REG_PTT1	6	Register overwrite 0 bit 1.	
	PDP10BIT	5	PDP 10 bits mode, support single 10 bit LVDS PDP.	
	TTL_LVDS	4	TTL LVDS mode, let single TTL and LVDS use same board.	
	BRGS	3	B port pixel R/G Swap. 0: Disable. 1: Enable.	
	ARGS	2	A port pixel R/G Swap. 0: Disable. 1: Enable.	
	BGBS	1	B port pixel G/B Swap. 0: Disable. 1: Enable.	
	AGBS	0	A port pixel G/B Swap. 0: Disable. 1: Enable.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSDCHBLEND	7	OSD Character Blending mode.	
	-	6	Reserved.	
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).	
	-	4	Reserved.	
	GATP	3	Gamma Automatically On/Off based on Auto Phase value. 0: Disable. 1: Enable.	
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency. 011: 50.0%% transparency. 100: 62.5% transparency.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
			101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	MNS_COL[7:0]	7:0	Main Window No Signal Color.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	MBCOL[7:0]	7:0	Main Window Border Color.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	SLOW_RAW_LIM[3:0]	6:3	RAW_THRESHOLD in FPLL_TUNE_SLOW.	
	SLOW_CNT_LIM[2:0]	2:0	Count threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLOCK_DL_LN[2:0]	5:3	Delay line number in Flock mode.	
	FLOCK_AH_LN[2:0]	2:0	Ahead line in Flock mode.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
29h	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.	
	CMRND	5	Color Matrix Rounding control.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: -128~127.	
	GRAN	1	Green Range. 0: 0~255.1: -128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: -128~127.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSFD	7	Sub window Shift Field. 0: Shift even field. 0: Shift odd field.	
	SSLN[1:0]	6:5	Sub window Shift Line Numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.	
	ILIM	4	Insert Line when Interlace Mode. 0: Do not insert. 1: Insert.	
	MSFD	3	Main window Shift Field. 0: Shift even field. 1: Shift odd field.	
	MSLN[2:0]	2:0	Main window Shift Line Numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 lines between odd and even field. 010: Shift 2 lines between odd and even field. 011: Shift 3 lines between odd and even field. 1xx: Shift 4 lines between odd and even field.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[7:0]	7:0	Insert Fraction Vertical Position.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : RO**
	IFVP[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[7:0]	7:0	Insert Fraction Width. PD Down value.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : RO**
	IFRACTW[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : RO**
	OVSSTAT[7:0]	7:0	Output Vertical Total Status. Lock status. Equal to 1 when phase error less than 29h/2Ah.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7	Reserved.	
	OVERDESTAT	6	Output Vertical DE Status.	
	-	5:3	Reserved.	
	OVSSTAT[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	OHTSTAT0[7:0]	7:0	OHSTAT initial value.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : RO**
	OHTSTAT1[7:0]	7:0	Output H Total Status.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FRACST0[7:0]	7:0	Fraction initial value.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	FRACST1[7:0]	7:0	Fraction Status.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FRACST2[2:0]	2:0	Fraction Status.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:3	Reserved.	
	FRACST3[2:0]	2:0	Fraction Status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	HTTMGN[7:0]	7:0	H Total Margin.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	SSCMGN[7:0]	7:0	SSC Margin.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSTVALUE0[7:0]	7:0	Read Start initial value.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	RSTVALUE1[7:0]	7:0	Read Start Value.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	RSTVALUE2[4:0]	4:0	Read Start initial value.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	RSTVALUE3[4:0]	4:0	Read Start Value.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FRONT_BACK	5	Set front back mode.	
	-	4:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	INP8	7	This bit with INE_DRV3 to enable G replace R and B for gamma mapping.	
	ONE_DRV3	6	Gamma use G replace R and B for gamma mapping.	
	GABYP	5	By pass gamma function.	
	-	4:3	Reserved.	
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	TSTDATA[7:0]	7:0	Reserved.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	LFCOEF1[2:0]	7:5	Loop filter coefficient 1.	
	LFCOEF2[4:0]	4:0	Loop filter coefficient 2.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	TUNE_SLOW[7:0]	7:0	Tune number for OVDE lock value fine tune.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	TFRACN[7:0]	7:0	Target Fraction Number. / Frame PLL limit RK[7:0].	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	PDP_MASK_EN	6	Reserved.	
	-	5	Reserved.	
	FX_PROT	4	Frame Change Protect.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x40**	**Access : R/W**
	TSTMD_REG_EN	7	Test Mode Register Enable. 0: Disable. 1: Enable.	
	EOCK	6	Use External Clock (pin) as Output Dot Clock. 0: Disable (use internal dot clock). 1: Enable (use external dot clock).	
	-	5:3	Reserved.	
	BPM	2	Bypass clock Mode (IDCLK as ODCLK). 0: Disable. 1: Enable.	
	PTEN	1	PLL Test register protect bit. 0: Disable. 1: Enable.	
	LRTM	0	LVDS/RSDS Test Mode enable. 0: Disable. 1: Enable.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	CLKDLYSEL[3:0]	7:4	OCKDLY[3:0]: OCLK Delay adjustment (TCON feature only). 0: 16 step to adjust. 1: Typical 0.8ns delay/step.	
	OCLK	3	Output CLK control. 0: Normal. 1: Invert.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description
	ODE	2	Output DE control. 0: Active high. 1: Active low.
	OVS	1	Output VSYNC control. 0: Active high. 1: Active low.
	OHS	0	Output HSYNC control. 0: Active high. 1: Active low.
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:6	Reserved.
	OEDB	5	Output Even Data Bus pin control. 0: Normal. 1: Tri-state.
	OODB	4	Output Odd Data Bus pin control. 0: Normal. 1: Tri-state.
	OVS0	3	OVSYNC pin control. 0: Normal. 1: Tri-state.
	OHS0	2	OHSYNC pin control. 0: Normal. 1: Tri-state.
	ODE0	1	ODE pin control. 0: Normal. 1: Tri-state.
	OCLK0	0	OCLK pin control. 0: Normal. 1: Tri-state.
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00** **Access : R/W**
	DEDRV[1:0]	7:6	Output DE Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.
	CLKDRV[1:0]	5:4	Output Clock Driving current select. 00: 4mA.01: 6mA.

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: 8mA. 11: 12mA.	
	ODDDRV[1:0]	3:2	Output data Odd channel Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
	EVENDRV[1:0]	1:0	Output data Even channel Driving current select. 00: 4mA. 01: 6mA. 10: 8mA. 11: 12mA.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SKEW[1:0]	5:4	Output data SKEW.	
	ECLKDLY[3:0]	3:0	ECLK Delay adjustment (TCON feature only). 0: 16 steps to adjust. 1: Typical 0.8ns delay/step.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	TEST_CLK_MODE	7	0: Disable. 1: Enable.	
	PLL_DIV2	6	0: Normal. 1: Test clock output divided by 2.	
	DDR_TEST	5	1: Select DDR 29est bus.	
	TEST_MD_D	4	1: Enable 24-bit test bus output.	
	-	3:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	BIST_STS[7:0]	7:0	Reserved.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	CHIPID[7:0]	7:0	Chip ID.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	BOND_STS[7:0]	7:0	Reserved.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x44**	**Access : R/W**
	LP_SET0[7:0]	7:0	Output PLL Set.	
4Bh	**REG102F97**	**7:0**	**Default : 0x55**	**Access : R/W**

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	LP_SET0[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	LP_SET1[7:0]	7:0	Output PLL Set.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OBN10	7	10-bit Bus enable.	
	DITHER_MINUS	6	1: Enable.	
	GPODDC	5	GPO, GPO[3] use for DDC DAT/CLK.	
	M_GRG	4	Main window Gamma Rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIM_HS	7	Limit Htotal by PWM counter enable.	
	NEW_FIELD_SEL	6	Select field created method. 0: Created by Vsync and Hsync. 1: Created by VFDE.	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end. 1: Vsync end.	
	-	4:0	Reserved.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	REM[7:0]	7:0	Htotal REMainder value.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	REM[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DIV[7:0]	7:0	PWM5 CLK div factor.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	PWM5DIV[8]	0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5DUTY[7:0]	7:0	PWM5 period.	
5Ah	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TRACE_PHASE_HTOTAL[7:0]	7:0	New Htotal for fast phase offset reduce, only active when TRACE_PHASE_EN is set to 1.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	NEW_HBC_CLAMP	6	Clamp function for HBC gain.	
	NEW_HBC_GAIN	5	HBC gain mode. 0: 0.4. 1: 0.04.	
	TRACE_PHASE_EN	4	Enable modify Htotal for fast phase offset reduce.	
	TRACE_PHASE_HTOTAL[11:8]	3:0	See description of '102FB4h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x07**	**Access : R/W**
	BIUCLK_DIV[7:0]	7:0	Calculate VDE ratio BIUCLK divider.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	RPT_VRATIO_EN	0	Report VDE Vtotal ratio enable.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_0_REG[7:0]	7:0		
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_1_REG[7:0]	7:0		
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_2_REG[7:0]	7:0		
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_3_REG[7:0]	7:0		
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_4_REG[7:0]	7:0		
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	PIP_OP2_5_REG[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[7:0]	7:0	Input VDE PRD value.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : RO**
	VDE_PRD_VALUE[15:8]	7:0	See description of '102FD0h'.	
69h	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : RO**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VTT_PRD_VALUE[7:0]	7:0	Input Vtt PRD value.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_PRD_VALUE[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	HIFRC_SROT	7	Enable HIFRC spatial rotation.	
	RAN[1:0]	6:5	Enable HIFRC RANdom noise latch for rotation.	
	F2_EN	4	Enable noise repeats 2 frames.	
	NEW_DITH_M	3	New dither method select.	
	-	2	Reserved.	
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.	
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.	
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.	
	H_RAN_EN	3	H direction using random noise enable for HIFRC.	
	NEW_ACBD	2	Swap HIFRC probability sequence.	
	OLD_HIFRC	1	Select old HIFRC dither method.	
	RAN_DIR_EN	0	Enable noise as rotate direction.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table r/w address.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_W_FLAG2	7	LUT table blue write command.	
	LUT_W_FLAG1	6	LUT table green write command.	
	LUT_W_FLAG0	5	LUT table red write command.	
	-	4	Reserved.	
	LUT_BW_CH_SEL[1:0]	3:2	Lut table burst write channel selection: 2'b00: Select R channel. 2'b01: Select G channel. 2'b10: Select B channel. 2'b11: Select All R/G/B channel.	
	-	1	Reserved.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
	LUT_BW_MAIN_EN	0	Lut table burst write enable.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	LUT_R_FLAG2	7	LUT table blue read command.	
	LUT_R_FLAG1	6	LUT table green read command.	
	LUT_R_FLAG0	5	LUT table red read command.	
	-	4:1	Reserved.	
	LUT_BW_FLAG	0	Lut table burst write status when burst write enable.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_R[7:0]	7:0	Data write to R LUT SRAM and burst mode data write to selected channel.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_R[11:8]	3:0	See description of '102FDCh'.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_G[7:0]	7:0	Data write to G LUT SRAM.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_G[11:8]	3:0	See description of '102FDEh'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	WR_B[7:0]	7:0	Data write to B LUT SRAM.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	WR_B[11:8]	3:0	See description of '102FE0h'.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_R[7:0]	7:0	Data read from R LUT SRAM.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_R[11:8]	3:0	See description of '102FE2h'.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_G[7:0]	7:0	Data read from G LUT SRAM.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_G[11:8]	3:0	See description of '102FE4h'.	

VOP Register (Bank = 102F, Sub-bank = 10)

Index (Absolute)	Mnemonic	Bit	Description	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	RD_B[7:0]	7:0	Data read from B LUT SRAM.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RD_B[11:8]	3:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7:4	Reserved.	
	CLR_MLOAD_TOO_SLOW	3	Clear auto mload gamma too slow flag.	
	MLOAD_TOO_SLOW	2	Auto mload gamma too slow flag.	
	AUTO_MLOAD_SWITCH	1	Enable auto mload gamma switch gamma table by frame.	
	AUTO_MLOAD_GAMMA	0	Enable auto mload gamma function.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[15:8]	7:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE0[23:16]	7:0	See description of '102FEAh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[15:8]	7:0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_GAMMA_BASE1[23:16]	7:0	See description of '102FEEh'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.	
7Ah	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	R_MAX_BASE0[11:8]	3:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	R_MAX_BASE1[11:8]	3:0	See description of '102FF6h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE0[11:8]	3:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	G_MAX_BASE1[11:8]	3:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE0[11:8]	3:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	B_MAX_BASE1[11:8]	3:0	See description of '102FFEh'.	

SCMI Register (Bank = 102F, Sub-bank = 12)

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bits format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bits format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data config from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data config from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data config from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data config from mode 5 change to mode 4.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	
	STILL_MODE_F2	3	F2 image freeze enable.	
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.	
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	CAPTURE_START_F2	7	F2 image capture start.	
	IPM_READ_OFF_F2	6	F2 force IP read request disable.	
	MADI_FORCE_OFF_F2	5	F2 force MADi off.	
	MADI_FORCE_ON_F2	4	F2 force MADi on.	
	FBL_25D	3	F2 frame buffer less de-interlace mode.	
	-	2	Reserved.	
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.	
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.	
	OPM_LINEAR_BASE_SEL_F2	6	F2 linear mode base address selection.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.	
	-	4	Reserved.	
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.	
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.	
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.	
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.	
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.	
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.	
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.	
	DOT_LN_PON_SEL_F2	1	F2 OP MADi dot line data select.	
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.	
	-	6:4	Reserved.	
	Y8_M4_ONLY_MODE_F2	3	F2 FB store Y8/M4 only mode.	
	Y8_ONLY_MODE_F2	2	F2 FB store Y-8bits only.	
	BOB_YMR_10_EN_F2	1	F2 10-bits Bob mode with Y motion.	
	BOB_YMR_8_EN_F2	0	F2 8-bits Bob mode with Y motion.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY04_14_14	6	F2 FB store Y-8bits only.	
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.	
	IP_BYPASS_INTERLACE_FILM_F2	4	Film-supported bypass interlace mode.	
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.	
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.	
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.	
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.	
05h	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	W_BANK_RST_F2	7	F2 MEMYSNC write bank reset.	
	IPM_WREQ_HPRI_SEL_F2	6	F2 IPM wreq high priority selection: 1'b0: IPM local priority. 1'b1: IP2_ADJ priority.	
	FRC_FREEMD_F2	5	F2 Force output odd/even toggle when 2DDi for interlace input.	
	MIU_SELECT_F2	4	F2 access MIU0 or MIU1 select.	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x02**	**Access : R/W**
	DUMMY05_10_15[5:0]	7:2	Reserved.	
	OPM_F1_EN	1	Enable OPM F1 register.	
	BK_FIELD_SEL_F2	0	F2 MEMYSNC FD selection.	
06h (102F0Ch)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RW_BANK_MAP_MSB_F2	7	F2 MSB bit of read/write bank mapping mode.	
	OPM_RBANK_SEL_MSB_F2	6	F2 OP force read bank select MSB.	
	-	5:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x88**	**Access : R/W**
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.	
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.	
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.	
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.	
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.	
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x40**	**Access : R/W**
	RW_BANK_MAP_F2[2:0]	7:5	F2 read/write bank mapping mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	
08h	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IPM_BASE_ADDR0_F2[24]	0	See description of '102F10h'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_OFFSET_F2[12:8]	4:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	IPM_FETCH_NUM_F2[12:8]	4:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F20h'.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR0_F2[24]	0	See description of '102F20h'.	
12h	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR1_F2[24]	0	See description of '102F24h'.	
14h ~ 14h (102F28h ~ 102F29h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F2[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_VCNT_LIMIT_EN_F2	7	F2 IP line count limit enable.	
	-	6:5	Reserved.	
	IPM_VCNT_LIMIT_NUM_F2[12:8]	4:0	See description of '102F30h'.	
19h	**REG102F32**	**7:0**	**Default : 0x04**	**Access : R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	FIELD_NUM_F2[4:0]	4:0	F2 field number.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_FIELD_NUM_DEFINE_F2	7	Enable OPM F2 field number define.	
	OPM_FIELD_NUM_F2[4:0]	6:2	OPM F2 field number.	
	OPM_8READ_EN_F2	1	F2 OPM 8read mode enable.	
	OPM_6READ_EN_F2	0	F2 OPM 6read mode enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	IPM_W_LIMIT_EN_F2	7	F2 IP write limit enable.	
	IPM_W_LIMIT_MIN_F2	6	F2 IP write limit flag 0: maximum 1: minimum.	
	-	5:1	Reserved.	
	IPM_W_LIMIT_ADR_F2[24]	0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_HMIR_OFFSET_EN_F2	7	F2 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F2[14:8]	6:0	See description of '102F38h'.	
1Dh ~ 1Fh (102F3Ah ~ 102F3Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h	**REG102F40**	**7:0**	**Default : 0x10**	**Access : R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x10**	**Access : R/W**
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.	
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x14**	**Access : R/W**
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x14**	**Access : R/W**
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_FLOW_CTRL_CNT[7:0]	7:0	OPW request flow control count.	
27h	**REG102F4E**	**7:0**	**Default : 0x88**	**Access : R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPW_VP_CNT_CLR	7	OPW write mask field count clear.	
	OPW_MASK_MODE[2:0]	6:4	OPW write mask number by field.	
	OPW_STATUS_CLR	3	OPW status clear enable.	
	OPW_REQ_RST	2	OPW write request reset.	
	-	1	Reserved.	
	OPW_WREQ_OFF_F2	0	OPW write request disable.	
27h ~ 28h (102F4Fh ~ 102F51h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_THRD[7:0]	7:0	OPW FIFO threshold for read request.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x10**	**Access : R/W**
	OPW_WREQ_HPRI[7:0]	7:0	OPW high priority threshold for read request.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x20**	**Access : R/W**
	OPW_WREQ_MAX[7:0]	7:0	OPW read request max number.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x22**	**Access : R/W**
	OPW_WFIFO_DEPTH[7:0]	7:0	OPW line buffer length for memory data write.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F2[4:0]	4:0	F2 OP previous data Rbank difference between current data Rbank at real line case.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F2[4:0]	4:0	F2 OP previous data Rbank difference between current data Rbank at dot line and NOC0 case.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F2[4:0]	4:0	F2 OP previous data Rbank difference between current data Rbank at dot line and NOC1 case.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F2[4:0]	4:0	F2 OP extend data Rbank difference between current data Rbank at real line case.	
2Eh	**REG102F5D**	**7:0**	**Default : 0x14**	**Access : R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F2[4:0]	4:0	F2 OP extend data Rbank difference between current data Rbank at dot line and NOC0 case.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F2[4:0]	4:0	F2 OP extend data Rbank difference between current data Rbank at dot line and NOC1 case.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	IPM_3D_SBS_FORCE_EN_F2	1	F2 IPM 3D side by side input enable.	
	IPM_3D_EN_F2	0	F2 IPM 3D input enable.	
31h ~ 33h (102F62h ~ 102F67h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY34_7_7	7	HDMI 3D OPM side by side read using PIP.	
	-	6:0	Reserved.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[7:0]	7:0	F2 status read out for debug.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_35_F2[15:8]	7:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[7:0]	7:0	F2 status read out for debug.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_36_F2[15:8]	7:0	See description of '102F6Ch'.	
37h ~ 37h (102F6Eh ~ 102F6Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_38_F2[7:0]	7:0	F2 status read out for debug.	
38h	**REG102F71**	**7:0**	**Default : 0x00**	**Access : RO**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	STATUS_READ_38_F2[15:8]	7:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[7:0]	7:0	F2 status read out for debug.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_39_F2[15:8]	7:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[7:0]	7:0	F2 status read out for debug.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3A_F2[15:8]	7:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[7:0]	7:0	F2 status read out for debug.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3B_F2[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[7:0]	7:0	F2 status read out for debug.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3C_F2[15:8]	7:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[7:0]	7:0	F2 status read out for debug.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3D_F2[15:8]	7:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[7:0]	7:0	F2 status read out for debug.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_3E_F2[15:8]	7:0	See description of '102F7Ch'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x08**	**Access : R/W**
	DUMMY40_4_15[3:0]	7:4		

SCMI Register (Bank = 102F, Sub-bank = 12)

Index (Absolute)	Mnemonic	Bit	Description	
	UPDATE_MEM_CONFIG_EN	3	Update memory format enable.	
	-	2	Reserved.	
	IPM_REG_DBF_EN_F2	1	F2 Register latch with input V sync enable.	
	OPM_REG_DBF_EN	0	Register latch with output V sync enable.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY40_4_15[11:4]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY41_7_6[1:0]	7:6		
	-	5:0	Reserved.	
41h ~ 42h (102F83h ~ 102F84h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MADI_FORCE_OFF_F1	5	F1 force madi off.	
	MADI_FORCE_ON_F1	4	F1 force madi on.	
	-	3:0	Reserved.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_4READ_EN_F1	3	F1 OP read 4 fields enable.	
	OPM_3READ_EN_F1	2	F1 OP read 3 fields enable.	
	OPM_2READ_EN_F1	1	F1 OP read 2 fields enable.	
	OPM_1READ_EN_F1	0	F1 OP read 1 field enable.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	FILM_HIGH_PRI_F1	3	F1 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F1	2	F1 OP film dot line data select.	
	DOT_LN_PON_SEL_F1	1	F1 OP MADi dot line data select.	
	-	0	Reserved.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DUMMY44_2_3[1:0]	3:2	Reserved.	
	-	1:0	Reserved.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
44h (102F89h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	W_BANK_RST_F1	7	F1 MEMYSNC write bank reset.	
	IPM_WREQ_HPRI_SEL_F1	6	F1 IPM WREQ high priority selection. 1'b0: IPM local priority. 1'b1: IP2_ADJ priority.	
	-	5:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY45_9_15[6:0]	7:1		
	BK_FIELD_SEL_F1	0	F2 MEMYSNC FD selection.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY46_0_7[7:0]	7:0	Reserved.	
46h ~ 4Fh (102F8Dh ~ 102F9Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[7:0]	7:0	F1 OP frame buffer base address 0.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR0_F1[23:16]	7:0	See description of '102FA0h'.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR0_F1[24]	0	See description of '102FA0h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[7:0]	7:0	F1 OP frame buffer base address 1.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[15:8]	7:0	See description of '102FA4h'.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_BASE_ADDR1_F1[23:16]	7:0	See description of '102FA4h'.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR1_F1[24]	0	See description of '102FA4h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_MWE_OFFSET_F1[7:0]	7:0	F1 OP demo mode pixel offset (pixel unit).	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_MWE_OFFSET_F1[11:8]	3:0	See description of '102FA8h'.	
56h (102FAChh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_OFFSET_F1[7:0]	7:0	F1 OP frame buffer line offset (pixel unit).	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F1[12:8]	4:0	See description of '102FAChh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPM_FETCH_NUM_F1[7:0]	7:0	F1 OP fetch pixel number of one line.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F1[11:8]	3:0	See description of '102FAEh'.	
58h ~ 59h (102FB0h ~ 102FB2h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:2	Reserved.	
	OPM_8READ_EN_F1	1	F1 OPM 8read mode enable.	
	OPM_6READ_EN_F1	0	F1 OPM 6read mode enable.	
5Ah ~ 5Dh (102FB4h ~ 102FBBh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[7:0]	7:0	OPW write limit address.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_ADR[23:16]	7:0	See description of '102FBCh'.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	OPW_W_LIMIT_EN	7	OPW write limit enable.	
	OPW_W_LIMIT_MIN	6	OPW write limit flag. 0: Maximum. 1: Minimum.	
	-	5:1	Reserved.	
	OPW_W_LIMIT_ADR[24]	0	See description of '102FBCh'.	
60h ~ 65h (102FC0h ~ 102FCBh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY66_13_15[2:0]	7:5	Reserved.	
	-	4:0	Reserved.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x01**	**Access : RO, R/W**
	-	7:6	Reserved.	
	FD_MASK_READ_F1	5	F1 FD mask read back.	
	FD_MASK_READ_F2	4	F2 FD mask read back.	
	-	3:2	Reserved.	
	OPW_WREQ_OFF_ALL	1	All OPW write request disable.	
	OPW_WREQ_OFF_F1	0	F1 OPW write request disable.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY67_8_15[7:0]	7:0	Reserved.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F1[4:0]	4:0	F1 OP previous data Rbank difference between current data Rbank at real line case.	
6Ch	**REG102FD9**	**7:0**	**Default : 0x02**	**Access : R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F1[4:0]	4:0	F1 OP previous data Rbank difference between current data Rbank at dot line and NOC0 case.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F1[4:0]	4:0	F1 OP previous data Rbank difference between current data Rbank at dot line and NOC1 case.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F1[4:0]	4:0	F1 OP extend data Rbank difference between current data Rbank at real line case.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x12**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F1[4:0]	4:0	F1 OP extend data Rbank difference between current data Rbank at dot line and NOC0 case.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F1[4:0]	4:0	F1 OP extend data Rbank difference between current data Rbank at dot line and NOC1 case.	
70h ~ 7Ch (102FE4h ~ 102FF9h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7D_F1[7:0]	7:0	F1 status read out for debug.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7D_F1[15:8]	7:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7E_F1[7:0]	7:0	F1 status read out for debug.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7E_F1[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7F_F1[7:0]	7:0	F1 status read out for debug.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : RO**
	STATUS_READ_7F_F1[15:8]	7:0	See description of '102FFEh'.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x83**	**Access : R/W**
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.	
	-	3	Reserved.	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: Reserved. 111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x00**	**Access : R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. 0: Disable (Auto selected by h/W, used when input is video, default). 1: Enable (use 0Dh[3:0] as divider).	
	-	6:4	Reserved.	
	VDEXT_SYNMD	3	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	
	-	2	Reserved.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. 00: External 8/10 bits video port. 01: Internal video decoder mode A. 10: External 16/20 bits video port. 11: Internal video decoder mode B.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x18**	**Access : R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. 0: Delay 1/4 input HSYNC. 1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.	
	-	1:0	Reserved.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x08**	**Access : R/W**
	FRCV	7	Source Sync Enable. 1: Display will adaptive follow the Source. If Display Select this source. 0: Display Free Run. If Display Select this source.	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, The Sync Process for this window will be stop until. Set Source Sync Enable = 1 again. This is the. Backup solution for Coast.	
	-	5:4	Reserved.	
	DATA10BIT	3	Set 10 bit input mode.	
	DATA8_ROUND	2	Use rounding for 8 bits input mode.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	1:0	Reserved.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x01**	**Access : R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_VDC[12:8]	4:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPRANGE_HDC[12:8]	4:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x20**	**Access : R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode. 0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Mask. 1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010:(ADC). 0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. 1: Use Hsync only. When ISEL = 011:(DVI). 0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL = 100:(VD). 0: Normal. 1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. 0: Normal. 1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. 0: Use Separate Hs for Coast Period. 1: Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. 0: Leading edge. 1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Auto Switch VST(04), VDC (06). 1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. 0000: 8 Line Ahead from SPRANGE_VST. 0001: 1 Line Ahead from SPRANGE_VST. 0010: 2 Line Ahead from SPRANGE_VST. 0011: 3 Line Ahead from SPRANGE_VST. .. 1111: 15 Line Ahead from SPRANGE_VST.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY09_8_15[7:0]	7:0	Reserved.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0A_8_15[7:0]	7:0	Reserved.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0B_0_14[7:0]	7:0	Reserved.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	DUMMY0B_0_14[14:8]	6:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	HDMI_444_REP	7	HDMI 444 format repetition.	
	-	6	Reserved.	
	DUMMY0C_2_5[3:0]	5:2	Reserved.	
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. 0: HW Auto Decide. 1: SW Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5 tap support. 1: Down Enable, ratio / tap depend on 0D[3:0].	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			FIR Purpose. 0: No down, 5 tap. 1: 2 to 1 down, 11 tap. Else: Reserved. For ExtVD is CCIR656, set to 0 and OVERSAP_EN = 1 will do 2X oversample.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0D_8_15[7:0]	7:0	Reserved.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. 0: Disable. 1: Enable.	
	OP2_COAST	6	Coast Status (Read only). 0: Coast is inactive. 1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. 1. VD. 2. Ext VD 656 Format. 3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate. For FIR Down Sample, and give 11 TAP Filter.	
	-	2:0	Reserved.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0F_8_15[7:0]	7:0	Reserved.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. 111: Noise level = 16.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY17_8_15[7:0]	7:0	Reserved.	
18h	**REG102F30**	**7:0**	**Default : 0x01**	**Access : R/W**

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bit. 011: Mask 3 bit. 100: Mask 4 bit. 101: Mask 5 bit. 110: Mask 6 bit. 111: Mask 7 bit.	
	ATP_READY	1	Auto Phase Result ready. 0: Result not ready. 1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. 0: Disable. 1: Enable.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY19_8_15[7:0]	7:0	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : RO**
	ATPV[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : RO, R/W**
	DELAYLN_NUM[3:0]	7:4	Delay Line After Sample V Start for Input Trigger Point.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LB_TUNE_READY	3	Input VSYNC Blanking Status. 0: In display. 1: In blanking.	
	-	2:0	Reserved.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	DELAYLN_NUM[5:4]	1:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x05**	**Access : RO, R/W**
	VS2HS_2SMALL	7	Vs to Hs timing too small.	
	DE_LOCKH_MD	6	DE Lock H Position Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. 5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x01**	**Access : R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Separator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. 0: Disable. 1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. 1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	IPHCS_ACT	4	Analog HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	-	1:0	Reserved.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. 0: Not active.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. 0: Not active. 1: Active.	
	CS_DET	5	Composite Sync Detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. 0: Input is not SOG. 1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.	
	FIELD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : RO**
	VTT_FOR_READ[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulse Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	VTT_FOR_READ[12:8]	4:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: 1 line. 1: 8 lines.	
	HTT_REPORT_SEL	6	Report Sync Separator Htt. 0: Htt Report by Mode Detector. 1: Htt Report by Sync Separator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. 0: Old method. 1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. 0: HSOUT (recommended). 1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. 0: Active low. 1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_VSPOL).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. 0: Active low. 1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_HSPOL).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_INTLAC).	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Mode Change Provide in data clock Domain. 1: Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. 0: Form Input DE. 1: From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion When. ADC_VIDEO = 1 for Data Align. 0: Normal. 1: Invert.	
	EXT_FIELDMD	2	Video External Field. 0: Use result of internal circuit detection. 1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. 0: Normal. 1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPW[7:0]	7:0	HSYNC Pulse Width Report.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : RO**
	VSPW[7:0]	7:0	VSYNC Pulse Width Report.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	VS_SEP_SEL	7	SYNC Separator VSYNC for Mode Detect. 0: RAW VSYNC (H / V Relationship is Keep for Interlace Detect). 1: HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + VIDEO_D1L_L) =	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	ADC_VIDEO	5	ADC Input Select. 0: PC Source. 1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Line for Another Field. 10: Delay 3 Line for Another Field. 11: Delay 4 Line for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). 0: Disable. 1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when COAST_SRCS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. 0: Internal Separated VSYNC (Default). 1: External VSYNC (Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. .. #254: Coast start from 255 HSYNC leading edge. #255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. .. #254: Coast end at 255 HSYNC leading edge. #255: Coast end at 256 HSYNC leading edge.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x10**	**Access : R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable. 0: Disable. 1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI: 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPVS_ACT, IPHS_ACT (E1[7:6]) (recommend).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. 0: Normal. 1: Invert.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY26_8_15[7:0]	7:0	Reserved.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	ATP_FILTERMD	7	ATP Filter for Text (4 frames). 0: Disable. 1: Enable.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DE_ONLY_IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.	
	GR_VS_EN	5	VSYNC glitch removal with line less than 2 (DE Only). 0: Disable. 1: Enable.	
	VS_PROTECT	4	VSYNC Protect with V total (DE Only). 0: Disable. 1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable. 1: Enable.	
	TEST_BUS_SEL[1:0]	1:0	Test bus select for debug.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY27_8_15[7:0]	7:0	Reserved.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	HTT_ID_FOR_READ[7:0]	7:0	HTT by idclk.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	HTT_ID_FOR_READ[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. 00: Off. 01: Only for line total number is even. 10: All case. 11: Off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. 0: Define Automatically. 1: Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VST[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x01**	**Access : R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HST[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_VDC[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x10**	**Access : R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	ATRANGE_HDC[12:8]	4:0	See description of '102F5Ah'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	VLOCK_MD	7	Vlock mode.	
	-	6	Reserved.	
	VLOCK_VAL[5:0]	5:0	Vlock value.	
33h	**REG102F67**	**7:0**	**Default : 0x00**	**Access : RO, R/W**

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OP2_COAST_STATUS	7	Auto OP free run status.	
	AUTO_COAST_HV_LOSE	6	Auto OP free run set enable when H/V sync lose.	
	AUTO_COAST_V_LOSE	5	Auto OP free run set enable when V sync lose.	
	AUTO_COAST_H_LOSE	4	Auto OP free run set enable when H sync lose.	
	NO_SIGNAL_STATUS	3	Auto no signal status.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer V pulse select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer H pulse select.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HDMI_VMUTE_DET_EN	1	HDMI V-mute detect enable.	
	WDT_EN	0	H/Vsync lose watch dog enable.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	SOG_VALID	7	Input composite/SOG signal is valid or not. 0: Not valid. 1: Valid.	
	CNT_NUMBER_SEL	6	Select how many lines of valid input composite/SOG signals to make sure the input signal is stable. 0: 60 lines. 1: 120 lines.	
	-	5:0	Reserved.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_OVERCNT	7	Coast over count enable.	
	OVERCNT[6:0]	6:0	Coast over count.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_NEW_CSOURCE	7	Separate sync pulse select.	
	-	6:1	Reserved.	
	GENCSOG_RESET	0	Reset SOG separate control.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	

OFFLINE_DETECT Register (Bank = 102F, Sub-bank = 13)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INTLAC_DET_EN[5:0]	5:0	New interlace detect function enable.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	INTLAC_DET_ALL[5:0]	5:0	The result of interlace detection.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FIELD_DET_EN[5:0]	5:0	New interlace detect function field select.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	FIELD_DET_ALL[5:0]	5:0	The field status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[7:0]	7:0	Vsync to Vsync pixel count.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : RO**
	SPR_V_LOCK_P_IP_CNT[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:5	Reserved.	
	SPR_V_LOCK_P_IP_CNT[20:16]	4:0	See description of '102F76h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HTT_RPT_MD	0	H total report mode.	

ACE Register (Bank = 102F, Sub-bank = 18)

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_FCC_8T_EN	7	Main window FCC region 8 enable.	
	MAIN_FCC_7T_EN	6	Main window FCC region 7 enable.	
	MAIN_FCC_6T_EN	5	Main window FCC region 6 enable.	
	MAIN_FCC_5T_EN	4	Main window FCC region 5 enable.	
	MAIN_FCC_4T_EN	3	Main window FCC region 4 enable.	
	MAIN_FCC_3T_EN	2	Main window FCC region 3 enable.	
	MAIN_FCC_2T_EN	1	Main window FCC region 2 enable.	
	MAIN_FCC_1T_EN	0	Main window FCC region 1 enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	FCC_DITHER_EN	6	FCC dither bit enable.	
	-	5:2	Reserved.	
	MAIN_FCC_9T_FIRST_EN	1	Main window FCC window 9 priority one enable.	
	MAIN_FCC_9T_EN	0	Main window FCC window 9 enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_FCC_8T_EN	7	Sub window FCC region 8 enable.	
	SUB_FCC_7T_EN	6	Sub window FCC region 7 enable.	
	SUB_FCC_6T_EN	5	Sub window FCC region 6 enable.	
	SUB_FCC_5T_EN	4	Sub window FCC region 5 enable.	
	SUB_FCC_4T_EN	3	Sub window FCC region 4 enable.	
	SUB_FCC_3T_EN	2	Sub window FCC region 3 enable.	
	SUB_FCC_2T_EN	1	Sub window FCC region 2 enable.	
	SUB_FCC_1T_EN	0	Sub window FCC region 1 enable.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_FCC_9T_FIRST_EN	1	Sub window FCC window 9 priority one enable.	
	SUB_FCC_9T_EN	0	Sub window FCC region 9 enable.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_FCC_BDRY_DIST[1:0]	5:4	Sub window FCC boundary limit distance.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: x4. 2: x2. 3: x1.	
	-	3:2	Reserved.	
	MAIN_FCC_BDRY_DIST[1:0]	1:0	Main window FCC boundary limit distance. 0: Disable. 1: x4. 2: x2. 3: x1.	
13h ~ 17h (102F26h ~ 102F2Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T1[7:0]	7:0	FCC region 1 cb target.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T1[7:0]	7:0	FCC region 1 cr target.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T2[7:0]	7:0	FCC region 2 cb target.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T2[7:0]	7:0	FCC region 2 cr target.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T3[7:0]	7:0	FCC region 3 cb target.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T3[7:0]	7:0	FCC region 3 cr target.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T4[7:0]	7:0	FCC region 4 cb target.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T4[7:0]	7:0	FCC region 4 cr target.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T5[7:0]	7:0	FCC region 5 cb target.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T5[7:0]	7:0	FCC region 5 cr target.	
1Dh	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FCC_CB_T6[7:0]	7:0	FCC region 6 cb target.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T6[7:0]	7:0	FCC region 6 cr target.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T7[7:0]	7:0	FCC region 7 cb target.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T7[7:0]	7:0	FCC region 7 cr target.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CB_T8[7:0]	7:0	FCC region 8 cb target.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_CR_T8[7:0]	7:0	FCC region 8 cr target.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_2T[3:0]	7:4	FCC region 2 strength.	
	FCC_K_1T[3:0]	3:0	FCC region 1 strength.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_4T[3:0]	7:4	FCC region 4 strength.	
	FCC_K_3T[3:0]	3:0	FCC region 3 strength.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_6T[3:0]	7:4	FCC region 6 strength.	
	FCC_K_5T[3:0]	3:0	FCC region 5 strength.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0xFF**	**Access : R/W**
	FCC_K_8T[3:0]	7:4	FCC region 8 strength.	
	FCC_K_7T[3:0]	3:0	FCC region 7 strength.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	FCC_K_9T[3:0]	3:0	FCC region 9 strength.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN1_CB_UP[1:0]	7:6	FCC region 1 target cb up distance.	
	FCC_WIN1_CB_DOWN[1:0]	5:4	FCC region 1 target cb down distance.	
	FCC_WIN1_CR_UP[1:0]	3:2	FCC region 1 target cr up distance.	
	FCC_WIN1_CR_DOWN[1:0]	1:0	FCC region 1 target cr down distance.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN2_CB_UP[1:0]	7:6	FCC region 2 target cb up distance.	
	FCC_WIN2_CB_DOWN[1:0]	5:4	FCC region 2 target cb down distance.	
	FCC_WIN2_CR_UP[1:0]	3:2	FCC region 2 target cr up distance.	
	FCC_WIN2_CR_DOWN[1:0]	1:0	FCC region 2 target cr down distance.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN3_CB_UP[1:0]	7:6	FCC region 3 target cb up distance.	
	FCC_WIN3_CB_DOWN[1:0]	5:4	FCC region 3 target cb down distance.	
	FCC_WIN3_CR_UP[1:0]	3:2	FCC region 3 target cr up distance.	
	FCC_WIN3_CR_DOWN[1:0]	1:0	FCC region 3 target cr down distance.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN4_CB_UP[1:0]	7:6	FCC region 4 target cb up distance.	
	FCC_WIN4_CB_DOWN[1:0]	5:4	FCC region 4 target cb down distance.	
	FCC_WIN4_CR_UP[1:0]	3:2	FCC region 4 target cr up distance.	
	FCC_WIN4_CR_DOWN[1:0]	1:0	FCC region 4 target cr down distance.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN5_CB_UP[1:0]	7:6	FCC region 5 target cb up distance.	
	FCC_WIN5_CB_DOWN[1:0]	5:4	FCC region 5 target cb down distance.	
	FCC_WIN5_CR_UP[1:0]	3:2	FCC region 5 target cr up distance.	
	FCC_WIN5_CR_DOWN[1:0]	1:0	FCC region 5 target cr down distance.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN6_CB_UP[1:0]	7:6	FCC region 6 target cb up distance.	
	FCC_WIN6_CB_DOWN[1:0]	5:4	FCC region 6 target cb down distance.	
	FCC_WIN6_CR_UP[1:0]	3:2	FCC region 6 target cr up distance.	
	FCC_WIN6_CR_DOWN[1:0	1:0	FCC region 6 target cr down distance.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	]			
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN7_CB_UP[1:0]	7:6	FCC region 7 target cb up distance.	
	FCC_WIN7_CB_DOWN[1:0]	5:4	FCC region 7 target cb down distance.	
	FCC_WIN7_CR_UP[1:0]	3:2	FCC region 7 target cr up distance.	
	FCC_WIN7_CR_DOWN[1:0]	1:0	FCC region 7 target cr down distance.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_WIN8_CB_UP[1:0]	7:6	FCC region 8 target cb up distance.	
	FCC_WIN8_CB_DOWN[1:0]	5:4	FCC region 8 target cb down distance.	
	FCC_WIN8_CR_UP[1:0]	3:2	FCC region 8 target cr up distance.	
	FCC_WIN8_CR_DOWN[1:0]	1:0	FCC region 8 target cr down distance.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	FCC_WIN9_CB[2:0]	5:3	FCC region 9 target cb distance.	
	FCC_WIN9_CR[2:0]	2:0	FCC region 9 target cr distance.	
28h (102F51h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CBCR_TO_UV	7	Main window cbcr to UV enable.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:4	Reserved.	
	SUB_CBCR_TO_UV	3	Sub window cbcr to UV enable.	
	SUB_ICC_EN	2	Sub window ICC enable.	
	ICC_LOW_RESERVE1	1	Reserved.	
	-	0	Reserved.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ICC_LUT_SRAM_BASE_EN	0	ICC LUT SRAM base enable. 0: Fix table. 1: SRAM base.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_R[3:0]	7:4	Sub window ICC saturation adjustment of R.	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_G[3:0]	7:4	Sub window ICC saturation adjustment of G.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_B[3:0]	7:4	Sub window ICC saturation adjustment of B.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_C[3:0]	7:4	Sub window ICC saturation adjustment of C.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_M[3:0]	7:4	Sub window ICC saturation adjustment of M.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_Y[3:0]	7:4	Sub window ICC saturation adjustment of Y.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_F[3:0]	7:4	Sub window ICC saturation adjustment of F.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation, [0]: OTHER_COLOR. [1]: Red. [2]: Green. [3]: Blue. [4]: Cyan. [5]: Magenta. [6]: Yellow. [7]: Flesh.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SIGN_SA_USER[7:0]	7:0	Sub window ICC decrease saturation, [0]: OTHER_COLOR.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[1]: Red. [2]: Green. [3]: Blue. [4]: Cyan. [5]: Magenta. [6]: Yellow. [7]: Flesh.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain, XXXXX.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold, XXXXXXX.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_SA_USER_NC[3:0]	7:4	Sub window ICC saturation adjustment of No color.	
	MAIN_SA_USER_NC[3:0]	3:0	Main window ICC saturation adjustment of No color.	
38h ~ 3Bh (102F70h ~ 102F77h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WPL_WHITE_PEAK_LIMIT_THRD[7:0]	7:0	White peak limit threshold.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RESERVED_ICC_LOW_Y[7:0]	7:0	Reserved.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IBC_EN	7	Main window IBC enable.	
	SUB_IBC_EN	6	Sub window IBC enable.	
	-	5:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YR_ADJ[5:0]	5:0	Sub window IBC Y adjustment of R.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YG_ADJ[5:0]	5:0	Sub window IBC Y adjustment of G.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YB_ADJ[5:0]	5:0	Sub window IBC Y adjustment of B.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YC_ADJ[5:0]	5:0	Sub window IBC Y adjustment of C.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YM_ADJ[5:0]	5:0	Sub window IBC Y adjustment of M.	
47h	**REG102F8F**	**7:0**	**Default : 0x20**	**Access : R/W**

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:6	Reserved.	
	SUB_YY_ADJ[5:0]	5:0	Sub window IBC Y adjustment of Y.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_YF_ADJ[5:0]	5:0	Sub window IBC Y adjustment of F.	
48h (102F91h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_HIGH_PASS_EN	7	Main window Y H_CORING as high pass filter.	
	MAIN_Y_TABLE_STEP[2:0]	6:4	Main window Y H_CORING LUT step.	
	MAIN_PC_MODE	3	Main window PC mode.	
	-	2	Reserved.	
	MAIN_Y_BAND2_H_CORING_EN	1	Main window Y band2 H_CORING enable.	
	MAIN_Y_BAND1_H_CORING_EN	0	Main window Y band1 H_CORING enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_HIGH_PASS_EN	7	Main window C H_CORING as high pass filter.	
	MAIN_C_TABLE_STEP[2:0]	6:4	Main window C H_CORING LUT step.	
	MAIN_WHITE_PEAK_LIMIT_EN	3	Main window white peak limit enable.	
	-	2	Reserved.	
	MAIN_C_BAND2_H_CORING_EN	1	Main window C band2 H_CORING enable.	
	MAIN_C_BAND1_H_CORING_EN	0	Main window C band1 H_CORING enable.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE1[7:0]	7:0	Main window Y gain table 1.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE2[7:0]	7:0	Main window Y gain table 2.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE3[7:0	7:0	Main window Y gain table 3.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	]			
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_GAIN_TABLE4[7:0]	7:0	Main window Y gain table 4.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE1[7:0]	7:0	Main window C gain table 1.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE2[7:0]	7:0	Main window C gain table 2.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE3[7:0]	7:0	Main window C gain table 3.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_GAIN_TABLE4[7:0]	7:0	Main window C gain table 4.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_NOISE_MASKING_EN	7	Main window horizontal Y noise-masking enable.	
	MAIN_Y_COLOR_NOISE_MASKING_EN	6	Main window horizontal Y noise-masking color adaptive enable.	
	MAIN_Y_NOISE_MASK_GAIN[5:0]	5:0	Main window horizontal Y noise-masking gain (xxxx.xx).	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_C_NOISE_MASKING_EN	7	Main window horizontal C noise-masking enable.	
	MAIN_C_COLOR_NOISE_MASKING_EN	6	Main window horizontal C noise-masking color adaptive enable.	
	MAIN_C_NOISE_MASK_GAIN[5:0]	5:0	Main window horizontal C noise-masking gain (xxxx.xx).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_Y_NM_MIN_THRD[3:0]	7:4	Main window Y NOISE_MASKING min value threshold.	
	MAIN_Y_NM_MAX_THRD[3:0]	3:0	Main window Y NOISE_MASKING max value threshold.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_C_NM_MIN_THRD[3:0]	7:4	Main window C NOISE_MASKING min value threshold.	
	MAIN_C_NM_MAX_THRD[3:0]	3:0	Main window C NOISE_MASKING max value threshold.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x81**	**Access : R/W**
	COLOR_PK_WIN1_NM_ENTRY_VALUE[3:0]	7:4	Flesh color adaptive noise masking strength (x.xxx).	
	-	3:2	Reserved.	
	MAIN_COLOR_NM_STEP[1:0]	1:0	Main window color NOISE_MASKING step.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x81**	**Access : R/W**
	COLOR_PK_WIN2_NM_ENTRY_VALUE[3:0]	7:4	Blue color adaptive noise masking strength (x.xxx).	
	-	3:2	Reserved.	
	SUB_COLOR_NM_STEP[1:0]	1:0	Sub window color NOISE_MASKING step.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_HIGH_PASS_EN	7	Sub window Y H_CORING as high pass filter.	
	SUB_Y_TABLE_STEP[2:0]	6:4	Sub window Y H_CORING LUT step.	
	SUB_PC_MODE	3	Sub window PC mode.	
	-	2	Reserved.	
	SUB_Y_BAND2_H_CORING_EN	1	Sub window Y band2 H_CORING enable.	
	SUB_Y_BAND1_H_CORING_EN	0	Sub window Y band1 H_CORING enable.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_HIGH_PASS_EN	7	Sub window C H_CORING as high pass filter.	
	SUB_C_TABLE_STEP[2:0]	6:4	Sub window C H_CORING LUT step.	
	SUB_WHITE_PEAK_LIMIT_EN	3	Sub window white peak limit enable.	
	-	2	Reserved.	
	SUB_C_BAND2_H_CORING_EN	1	Sub window C band2 H_CORING enable.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_C_BAND1_H_CORING_EN	0	Sub window C band1 H_CORING enable.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_GAIN_TABLE1[7:0]	7:0	Sub window Y gain table 1.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_GAIN_TABLE2[7:0]	7:0	Sub window Y gain table 2.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_GAIN_TABLE3[7:0]	7:0	Sub window Y gain table 3.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_GAIN_TABLE4[7:0]	7:0	Sub window Y gain table 4.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_CORE_TABLE1[7:0]	7:0	Sub window C gain table 1.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_CORE_TABLE2[7:0]	7:0	Sub window C gain table 2.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_CORE_TABLE3[7:0]	7:0	Sub window C gain table 3.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_CORE_TABLE4[7:0]	7:0	Sub window C gain table 4.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_NOISE_MASKING_EN	7	Sub window horizontal Y noise-masking enable.	
	SUB_Y_COLOR_NOISE_MASKING_EN	6	Sub window horizontal Y noise-masking color adaptive enable.	
	SUB_Y_NOISE_MASK_GAIN[5:0]	5:0	Sub window horizontal Y noise-masking gain (xxxx.xx).	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_C_NOISE_MASKING_EN	7	Sub window horizontal C noise-masking enable.	
	SUB_C_COLOR_NOISE_MASKING_EN	6	Sub window horizontal C noise-masking color adaptive enable.	
	SUB_C_NOISE_MASK_GAIN[5:0]	5:0	Sub window horizontal C noise-masking gain (xxxx.xx).	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SUB_Y_NM_MIN_THRD[3:	7:4	Sub window Y NOISE_MASKING min value threshold.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	0]			
	SUB_Y_NM_MAX_THRD[3:0]	3:0	Sub window Y NOISE_MASKING max value threshold.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SUB_C_NM_MIN_THRD[3:0]	7:4	Sub window C NOISE_MASKING min value threshold.	
	SUB_C_NM_MAX_THRD[3:0]	3:0	Sub window C NOISE_MASKING max value threshold.	
5Fh ~ 5Fh (102FBEh ~ 102FBFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_EN	7	Main window IHC enable.	
	SUB_IHC_EN	6	Sub window IHC enable.	
	-	5:3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Pseudo return to initial value frame numbers. 2'b00: 1 frame initial. 2'b01: 2 frame initial. 2'b10: 4 frame initial. 2'b11: 8 frame initial.	
	PSEUDO_VCLR_EN	0	Pseudo return to initial value by vclear enable.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IHC_LUT_SRAM_BASE_EN	0	IHC LUT SRAM base enable. 0: Fix table. 1: SRAM base.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_R[6:0]	6:0	Sub window IHC hue adjustment of R.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_G[6:0]	6:0	Sub window IHC hue adjustment of G.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_B[6:0]	6:0	Sub window IHC hue adjustment of B.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_C[6:0]	6:0	Sub window IHC hue adjustment of C.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_M[6:0]	6:0	Sub window IHC hue adjustment of M.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_Y[6:0]	6:0	Sub window IHC hue adjustment of Y.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_HUE_USER_F[6:0]	6:0	Sub window IHC hue adjustment of F.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_TEST_EN[1:0]	7:6	Color adaptive test mode enable in horizontal noise masking.	
	SUB_COLOR_PK_WIN2_EN	5	Sub window color adaptive win2 enable in horizontal noise masking.	
	SUB_COLOR_PK_WIN1_EN	4	Sub window color adaptive win1 enable in horizontal noise masking.	
	-	3:2	Reserved.	
	MAIN_COLOR_PK_WIN2_EN	1	Main window color adaptive win2 enable in horizontal noise masking.	
	MAIN_COLOR_PK_WIN1_EN	0	Main window color adaptive win1 enable in horizontal noise masking.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	COLOR_PK_WIN2_TRANSITION_STEP[1:0]	3:2	Color adaptive win2 transition step in horizontal noise masking.	
	COLOR_PK_WIN1_TRANSITION_STEP[1:0]	1:0	Color adaptive win1 transition step in horizontal noise masking.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CB_UP[7:0]	7:0	Color adaptive win1 cb up in horizontal noise masking.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CR_UP[7:0]	7:0	Color adaptive win1 cr up in horizontal noise masking.	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CB_DOWN[7:0]	7:0	Color adaptive win1 cb down in horizontal noise masking.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN1_CR_DOWN[7:0]	7:0	Color adaptive win1 cr down in horizontal noise masking.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CB_UP[7:0]	7:0	Color adaptive win2 cb up in horizontal noise masking.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CR_UP[	7:0	Color adaptive win2 cr up in horizontal noise masking.	

ACE Register (Bank = 102F, Sub-bank = 18)

Index (Absolute)	Mnemonic	Bit	Description	
	7:0]			
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CB_DOWN[7:0]	7:0	Color adaptive win2 cb down in horizontal noise masking.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	COLOR_PK_WIN2_CR_DOWN[7:0]	7:0	Color adaptive win2 cr down in horizontal noise masking.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_R2Y_EN	4	Sub window RGB to YCbCr enable.	
	-	3:2	Reserved.	
	R2Y_DITHER_EN	1	RGB to YCbCr dither enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr enable.	
6Eh (102FDDh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_R2Y_EQ_SEL[2:0]	6:4	Sub window RGB to YCbCr equation selection. 3'b000: SDTV with R' G' B' 16-235 range. 3'b001: SDTV with R' G' B' 0-255 range. 3'b010: HDTV with R' G' B' 16-235 range. 3'b011: HDTV with R' G' B' 0-255 range. 3'b100: 709 to 601.	
	-	3	Reserved.	
	MAIN_R2Y_EQ_SEL[2:0]	2:0	Main window RGB to YCbCr equation selection. 3'b000: SDTV with R' G' B' 16-235 range. 3'b001: SDTV with R' G' B' 0-255 range. 3'b010: HDTV with R' G' B' 16-235 range. 3'b011: HDTV with R' G' B' 0-255 range. 3'b100: 709 to 601.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_NM_LOW_Y_EN	4	Sub window mosquito noise low y mode enable.	
	-	3:1	Reserved.	
	MAIN_NM_LOW_Y_EN	0	Main window mosquito noise low y mode enable.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (102FE1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0x10**	**Access : R/W**
	MAIN_NM_LOW_Y_TH[7:0]	7:0	Main window mosquito noise low y mode threshold.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_NM_LOW_Y_GAIN[5:0]	5:0	Main window mosquito noise low y mode gain.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_NM_LOW_Y_STEP[1:0]	1:0	Main window mosquito noise low y mode step.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x10**	**Access : R/W**
	SUB_NM_LOW_Y_TH[7:0]	7:0	Sub window mosquito noise low y mode threshold.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_NM_LOW_Y_GAIN[5:0]	5:0	Sub window mosquito noise low y mode gain.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_NM_LOW_Y_STEP[1:0]	1:0	Sub window mosquito noise low y mode step.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ICC_SRAM_IO_EN	0	ICC SRAM IO enable.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICC_IOADDR[7:0]	7:0	ICC IO address.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	ICC_IORE	0	ICC IO read enable.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	ICC_IOWDATA[7:0]	7:0	ICC IO write data.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	ICC_IOWE	0	ICC IO write enable.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : RO**
	ICC_IORDATA[7:0]	7:0	ICC IO read data.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	IHC_SRAM_IO_SELECT[1:0]	2:1	IHC SRAM IO select.	
	IHC_SRAM_IO_EN	0	IHC SRAM IO enable.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	IHC_IOADDR[7:0]	7:0	IHC IO address.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : WO**
	-	7:1	Reserved.	
	IHC_IORE	0	IHC IO read enable.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	IHC_IOWDATA[7:0]	7:0	IHC IO write data.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	IHC_IOWE	0	IHC IO write enable.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : RO**
	IHC_IORDATA[7:0]	7:0	IHC IO read data.	

PEAKING Register (Bank = 102F, Sub-bank = 19)

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_BAND12_PEAKING_EN	3	Main window band12 peaking enable.	
	MAIN_BAND11_PEAKING_EN	2	Main window band11 peaking enable.	
	MAIN_BAND10_PEAKING_EN	1	Main window band10 peaking enable.	
	MAIN_BAND9_PEAKING_EN	0	Main window band9 peaking enable.	
0Ch (102F19h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_BAND12_PEAKING_EN	3	Sub window band12 peaking enable.	
	SUB_BAND11_PEAKING_EN	2	Sub window band11 peaking enable.	
	SUB_BAND10_PEAKING_EN	1	Sub window band10 peaking enable.	
	SUB_BAND9_PEAKING_EN	0	Sub window band9 peaking enable.	
0Dh (102F1Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND12_COEF_STEP[1:0]	7:6	Main window band12 coefficient step.	
	MAIN_BAND11_COEF_STEP[1:0]	5:4	Main window band11 coefficient step.	
	MAIN_BAND10_COEF_STEP[1:0]	3:2	Main window band10 coefficient step.	
	MAIN_BAND9_COEF_STEP[1:0]	1:0	Main window band9 coefficient step.	
0Fh	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BAND12_COEF_STEP[1:0]	7:6	Sub window band12 coefficient step.	
	SUB_BAND11_COEF_STEP[1:0]	5:4	Sub window band11 coefficient step.	
	SUB_BAND10_COEF_STEP[1:0]	3:2	Sub window band10 coefficient step.	
	SUB_BAND9_COEF_STEP[1:0]	1:0	Sub window band9 coefficient step.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	VPS_SRAM_ACT	7	2D peaking line-buffer SRAM active.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2	Reserved.	
	HLPF_DITHER_EN	1	H Low pass filter dither bit enable.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_PEAKING_EN	7	Main window band8 peaking enable.	
	MAIN_BAND7_PEAKING_EN	6	Main window band7 peaking enable.	
	MAIN_BAND6_PEAKING_EN	5	Main window band6 peaking enable.	
	MAIN_BAND5_PEAKING_EN	4	Main window band5 peaking enable.	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.	
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.	
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_COEF_STEP[1:0]	7:6	Main window band8 coefficient step.	
	MAIN_BAND7_COEF_STEP[1:0]	5:4	Main window band7 coefficient step.	
	MAIN_BAND6_COEF_STEP[1:0]	3:2	Main window band6 coefficient step.	
	MAIN_BAND5_COEF_STEP[1:0]	1:0	Main window band5 coefficient step.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_V_NOISE_MASKING_EN	7	Main window vertical Y noise-masking enable.	
	MAIN_V_COLOR_NOISE_MASKING_EN	6	Main window vertical Y noise-masking color adaptive enable.	
	MAIN_V_NOISE_MASK_GAIN[5:0]	5:0	Main window vertical Y noise-masking gain.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_V_LPF_COEF_2[2:0]	6:4	Main window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	
	MAIN_V_LPF_COEF_1[2:0]	2:0	Main window vertical up-down pixel Y LPF coefficient.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	MAIN_OSD_SHARPNESS_C	6:0	Main window user sharpness adjust (Sxx.xxxx).	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TRL[6:0]			
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_Y_LPF_COEF[2:0]	6:4	Sub window horizontal Y LPF coefficient.	
	MAIN_SUB_EXCHANGE_EN	3	Main/Sub window swap enable.	
	-	2:1	Reserved.	
	SUB_POST_PEAKING_EN	0	Sub window 2D peaking enable.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND8_PEAKING_EN	7	Sub window band8 peaking enable.	
	SUB_BAND7_PEAKING_EN	6	Sub window band7 peaking enable.	
	SUB_BAND6_PEAKING_EN	5	Sub window band6 peaking enable.	
	SUB_BAND5_PEAKING_EN	4	Sub window band5 peaking enable.	
	SUB_BAND4_PEAKING_EN	3	Sub window band4 peaking enable.	
	SUB_BAND3_PEAKING_EN	2	Sub window band3 peaking enable.	
	SUB_BAND2_PEAKING_EN	1	Sub window band2 peaking enable.	
	SUB_BAND1_PEAKING_EN	0	Sub window band1 peaking enable.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND4_COEF_STEP[1:0]	7:6	Sub window band4 coefficient step.	
	SUB_BAND3_COEF_STEP[1:0]	5:4	Sub window band3 coefficient step.	
	SUB_BAND2_COEF_STEP[1:0]	3:2	Sub window band2 coefficient step.	
	SUB_BAND1_COEF_STEP[1:0]	1:0	Sub window band1 coefficient step.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND8_COEF_STEP[1:0]	7:6	Sub window band8 coefficient step.	
	SUB_BAND7_COEF_STEP[1:0]	5:4	Sub window band7 coefficient step.	
	SUB_BAND6_COEF_STEP[1:0]	3:2	Sub window band6 coefficient step.	
	SUB_BAND5_COEF_STEP[1:0]	1:0	Sub window band5 coefficient step.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_V_NOISE_MASKING_EN	7	Sub window vertical Y noise-masking enable.	
	SUB_V_COLOR_NOISE_MASKING_EN	6	Sub window vertical Y noise-masking color adaptive enable.	
	SUB_V_NOISE_MASK_GAIN[5:0]	5:0	Sub window vertical Y noise-masking gain.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_V_LPF_COEF_2[2:0]	6:4	Sub window vertical central pixel Y LPF coefficient.	
	-	3	Reserved.	
	SUB_V_LPF_COEF_1[2:0]	2:0	Sub window vertical up-down pixel Y LPF coefficient.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CORING_THRD_2[3:0]	7:4	Sub window coring threshold 2.	
	SUB_CORING_THRD_1[3:0]	3:0	Sub window coring threshold 1.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	SUB_OSD_SHARPNESS_CTRL[6:0]	6:0	Sub window user sharpness adjust (Sxx.xxxx).	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND1_COEF[6:0]	6:0	Main window band1 coefficient (Sxxx.xxx).	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND2_COEF[6:0]	6:0	Main window band2 coefficient (Sxxx.xxx).	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND3_COEF[6:0]	6:0	Main window band3 coefficient (Sxxx.xxx).	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND4_COEF[6:0]	6:0	Main window band4 coefficient (Sxxx.xxx).	
1Ah	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7	Reserved.	
	MAIN_BAND5_COEF[6:0]	6:0	Main window band5 coefficient (Sxxx.xxx).	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND6_COEF[6:0]	6:0	Main window band6 coefficient (Sxxx.xxx).	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND7_COEF[6:0]	6:0	Main window band7 coefficient (Sxxx.xxx).	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND8_COEF[6:0]	6:0	Main window band8 coefficient (Sxxx.xxx).	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PEAKING_TERM2_SELECT[3:0]	7:4	Main window peaking term2 select.	
	MAIN_PEAKING_TERM1_SELECT[3:0]	3:0	Main window peaking term1 select.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PEAKING_TERM4_SELECT[3:0]	7:4	Main window peaking term4 select.	
	MAIN_PEAKING_TERM3_SELECT[3:0]	3:0	Main window peaking term3 select.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PEAKING_TERM6_SELECT[3:0]	7:4	Main window peaking term6 select.	
	MAIN_PEAKING_TERM5_SELECT[3:0]	3:0	Main window peaking term5 select.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PEAKING_TERM8_SELECT[3:0]	7:4	Main window peaking term8 select.	
	MAIN_PEAKING_TERM7_SELECT[3:0]	3:0	Main window peaking term7 select.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PEAKING_TERM10_SELECT[3:0]	7:4	Main window peaking term10 select.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_PEAKING_TERM9_SELECT[3:0]	3:0	Main window peaking term9 select.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PEAKING_TERM12_SELECT[3:0]	7:4	Main window peaking term12 select.	
	MAIN_PEAKING_TERM11_SELECT[3:0]	3:0	Main window peaking term11 select.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PEAKING_TERM14_SELECT[3:0]	7:4	Main window peaking term14 select.	
	MAIN_PEAKING_TERM13_SELECT[3:0]	3:0	Main window peaking term13 select.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PEAKING_TERM16_SELECT[3:0]	7:4	Main window peaking term16 select.	
	MAIN_PEAKING_TERM15_SELECT[3:0]	3:0	Main window peaking term15 select.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND1_OVERSHOOT_LIMIT[7:0]	7:0	Window band1 overshoot limit.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND2_OVERSHOOT_LIMIT[7:0]	7:0	Window band2 overshoot limit.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND3_OVERSHOOT_LIMIT[7:0]	7:0	Window band3 overshoot limit.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND4_OVERSHOOT_LIMIT[7:0]	7:0	Window band4 overshoot limit.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND5_OVERSHOOT_LIMIT[7:0]	7:0	Window band5 overshoot limit.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND6_OVERSHOOT_LIMIT[7:0]	7:0	Window band6 overshoot limit.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND7_OVERSHOOT_LIMIT[7:0]	7:0	Window band7 overshoot limit.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND8_OVERSHOOT_LIMIT[7:0]	7:0	Window band8 overshoot limit.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND1_UNDERSHOOT_LIMIT[7:0]	7:0	Window band1 undershoot limit.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND2_UNDERSHOOT_LIMIT[7:0]	7:0	Window band2 undershoot limit.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND3_UNDERSHOOT_LIMIT[7:0]	7:0	Window band3 undershoot limit.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND4_UNDERSHOOT_LIMIT[7:0]	7:0	Window band4 undershoot limit.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND5_UNDERSHOOT_LIMIT[7:0]	7:0	Window band5 undershoot limit.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND6_UNDERSHOOT_LIMIT[7:0]	7:0	Window band6 undershoot limit.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND7_UNDERSHOOT_LIMIT[7:0]	7:0	Window band7 undershoot limit.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND8_UNDERSHOOT_LIMIT[7:0]	7:0	Window band8 undershoot limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND1_COEF[6:0]	6:0	Sub window band1 coefficient (Sxxx.xxx).	
28h	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7	Reserved.	
	SUB_BAND2_COEF[6:0]	6:0	Sub window band2 coefficient (Sxxx.xxx).	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND3_COEF[6:0]	6:0	Sub window band3 coefficient (Sxxx.xxx).	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND4_COEF[6:0]	6:0	Sub window band4 coefficient (Sxxx.xxx).	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND5_COEF[6:0]	6:0	Sub window band5 coefficient (Sxxx.xxx).	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND6_COEF[6:0]	6:0	Sub window band6 coefficient (Sxxx.xxx).	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND7_COEF[6:0]	6:0	Sub window band7 coefficient (Sxxx.xxx).	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND8_COEF[6:0]	6:0	Sub window band8 coefficient (Sxxx.xxx).	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PEAKING_TERM2_SELECT[3:0]	7:4	Sub window peaking term2 select.	
	SUB_PEAKING_TERM1_SELECT[3:0]	3:0	Sub window peaking term1 select.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PEAKING_TERM4_SELECT[3:0]	7:4	Sub window peaking term4 select.	
	SUB_PEAKING_TERM3_SELECT[3:0]	3:0	Sub window peaking term3 select.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PEAKING_TERM6_SELECT[3:0]	7:4	Sub window peaking term6 select.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_PEAKING_TERM5_SELECT[3:0]	3:0	Sub window peaking term5 select.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PEAKING_TERM8_SELECT[3:0]	7:4	Sub window peaking term8 select.	
	SUB_PEAKING_TERM7_SELECT[3:0]	3:0	Sub window peaking term7 select.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PEAKING_TERM10_SELECT[3:0]	7:4	Sub window peaking term10 select.	
	SUB_PEAKING_TERM9_SELECT[3:0]	3:0	Sub window peaking term9 select.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PEAKING_TERM12_SELECT[3:0]	7:4	Sub window peaking term12 select.	
	SUB_PEAKING_TERM11_SELECT[3:0]	3:0	Sub window peaking term11 select.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PEAKING_TERM14_SELECT[3:0]	7:4	Sub window peaking term14 select.	
	SUB_PEAKING_TERM13_SELECT[3:0]	3:0	Sub window peaking term13 select.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_PEAKING_TERM16_SELECT[3:0]	7:4	Sub window peaking term16 select.	
	SUB_PEAKING_TERM15_SELECT[3:0]	3:0	Sub window peaking term15 select.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_COLOR_PEAKING_EN	7	Main window color adaptive peaking enable.	
	MAIN_COLOR_FACTOR_LPF_EN	6	Main window color factor LPF enable.	
	-	5:4	Reserved.	
	SUB_COLOR_PEAKING_EN	3	Sub window color adaptive peaking enable.	
	SUB_COLOR_FACTOR_LPF	2	Sub window color factor LPF enable.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	_EN			
	SUB_PK_COLOR_CTRL_SEP_EN	1	Sub window peaking color factor control separate enable.	
	MAIN_PK_COLOR_CTRL_SEP_EN	0	Main window peaking color factor control separate enable.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x33**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CORING_THRD_STEP[1:0]	5:4	Main window coring step.	
	SUB_COLOR_CORING_EN	3	Sub window color adaptive coring enable.	
	-	2	Reserved.	
	SUB_CORING_THRD_STEP[1:0]	1:0	Sub window coring step.	
31h ~ 32h (102F62h ~ 102F65h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND2_CORING_THRD[3:0]	7:4	Main window band2 coring threshold.	
	MAIN_BAND1_CORING_THRD[3:0]	3:0	Main window band1 coring threshold.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND4_CORING_THRD[3:0]	7:4	Main window band4 coring threshold.	
	MAIN_BAND3_CORING_THRD[3:0]	3:0	Main window band3 coring threshold.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND6_CORING_THRD[3:0]	7:4	Main window band6 coring threshold.	
	MAIN_BAND5_CORING_THRD[3:0]	3:0	Main window band5 coring threshold.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND8_CORING_THRD[3:0]	7:4	Main window band8 coring threshold.	
	MAIN_BAND7_CORING_TH	3:0	Main window band7 coring threshold.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	RD[3:0]			
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND2_CORING_THRD[3:0]	7:4	Sub window band2 coring threshold.	
	SUB_BAND1_CORING_THRD[3:0]	3:0	Sub window band1 coring threshold.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND4_CORING_THRD[3:0]	7:4	Sub window band4 coring threshold.	
	SUB_BAND3_CORING_THRD[3:0]	3:0	Sub window band3 coring threshold.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND6_CORING_THRD[3:0]	7:4	Sub window band6 coring threshold.	
	SUB_BAND5_CORING_THRD[3:0]	3:0	Sub window band5 coring threshold.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND8_CORING_THRD[3:0]	7:4	Sub window band8 coring threshold.	
	SUB_BAND7_CORING_THRD[3:0]	3:0	Sub window band7 coring threshold.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CORING_THRD_SEC[5:0]	5:0	Main window color coring limit.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CORING_THRD_SEC[5:0]	5:0	Sub window color coring limit.	
38h ~ 38h (102F70h ~ 102F71h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_Y_V_NM_MIN_THRD[3:0]	7:4	Main window vertical Y NOISE_MASKING min value threshold.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_Y_V_NM_MAX_THRD[3:0]	3:0	Main window vertical Y NOISE_MASKING max value threshold.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SUB_Y_V_NM_MIN_THRD[3:0]	7:4	Sub window vertical Y NOISE_MASKING min value threshold.	
	SUB_Y_V_NM_MAX_THRD[3:0]	3:0	Sub window vertical Y NOISE_MASKING max value threshold.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CR_DELAY_NUM[1:0]	7:6	Sub window cr delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
	MAIN_CR_DELAY_NUM[1:0]	5:4	Main window cr delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
	-	3:2	Reserved.	
	SUB_YC_DELAY_EN	1	Sub window yc delay enable.	
	MAIN_YC_DELAY_EN	0	Main window yc delay enable.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CB_DELAY_NUM[1:0]	7:6	Sub window cb delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
	SUB_Y_DELAY_NUM[1:0]	5:4	Sub window y delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
	MAIN_CB_DELAY_NUM[1:0]	3:2	Main window cb delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_Y_DELAY_NUM[1:0]	1:0	Main window y delay number. 0: No delay. 1: Delay 1T. 2: Delay 2T. 3: Delay 3T.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND10_CORING_THRD[3:0]	7:4	Main window band2 coring threshold.	
	MAIN_BAND9_CORING_THRD[3:0]	3:0	Main window band1 coring threshold.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BAND12_CORING_THRD[3:0]	7:4	Main window band4 coring threshold.	
	MAIN_BAND11_CORING_THRD[3:0]	3:0	Main window band3 coring threshold.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND10_CORING_THRD[3:0]	7:4	Sub window band10 coring threshold.	
	SUB_BAND9_CORING_THRD[3:0]	3:0	Sub window band9 coring threshold.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BAND12_CORING_THRD[3:0]	7:4	Sub window band12 coring threshold.	
	SUB_BAND11_CORING_THRD[3:0]	3:0	Sub window band11 coring threshold.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x10**	**Access : R/W**
	MAIN_OSD_SHARPNESS_SEP_HV_EN	7	Main window user sharpness separate HV enable.	
	MAIN_OSD_SHARPNESS_CTRL_H[6:0]	6:0	Main window user sharpness horizontal adjust (Sxx.xxxx).	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	MAIN_OSD_SHARPNESS_CTRL_V[6:0]	6:0	Main window user sharpness vertical adjust (Sxx.xxxx).	
3Fh	**REG102F7E**	**7:0**	**Default : 0x10**	**Access : R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_OSD_SHARPNESS_SEP_HV_EN	7	Sub window user sharpness separate HV enable.	
	SUB_OSD_SHARPNESS_CTRL_H[6:0]	6:0	Sub window user sharpness horizontal adjust (Sxx.xxxx).	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7	Reserved.	
	SUB_OSD_SHARPNESS_CTRL_V[6:0]	6:0	Sub window user sharpness vertical adjust (Sxx.xxxx).	
40h ~ 50h (102F80h ~ 102FA1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_PK_ADP_Y_STEP[1:0]	5:4	Main window peaking adaptive y alpha step.	
	-	3:2	Reserved.	
	MAIN_PK_ADP_Y_ALPHA_LPF_EN	1	Main window peaking adaptive y alpha low pass filter enable.	
	MAIN_PK_ADP_Y_EN	0	Main window peaking adaptive y enable.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_PK_Y_LOW_THRD[7:0]	7:0	Main window peaking adaptive y low threshold.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x54**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_1[3:0]	7:4	Main window peaking adaptive y alpha LUT 1.	
	MAIN_PK_ADP_Y_ALPHA_LUT_0[3:0]	3:0	Main window peaking adaptive y alpha LUT 0.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x76**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_3[3:0]	7:4	Main window peaking adaptive y alpha LUT 3.	
	MAIN_PK_ADP_Y_ALPHA_LUT_2[3:0]	3:0	Main window peaking adaptive y alpha LUT 2.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_5[3:0]	7:4	Main window peaking adaptive y alpha LUT 5.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_PK_ADP_Y_ALPHA_LUT_4[3:0]	3:0	Main window peaking adaptive y alpha LUT 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_7[3:0]	7:4	Main window peaking adaptive y alpha LUT 7.	
	MAIN_PK_ADP_Y_ALPHA_LUT_6[3:0]	3:0	Main window peaking adaptive y alpha LUT 6.	
58h ~ 5Fh (102FB0h ~ 102FBEh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_GAUSS_LUT_STEP[1:0]	5:4	Main window Gaussian SNR LUT step.	
	-	3:1	Reserved.	
	MAIN_GAUSS_NR_EN	0	Main window Gaussian SNR enable.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_GAUSS_LUT_STEP[1:0]	5:4	Sub window Gaussian SNR LUT step.	
	-	3:1	Reserved.	
	SUB_GAUSS_NR_EN	0	Sub window green Gaussian SNR bypass enable.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_DERING_REF_WIDTH[1:0]	5:4	Main window dering reference width. 0: 5 pixel. 1: 4 pixel. 2: 3 pixel. 3: 2 pixel.	
	-	3	Reserved.	
	MAIN_DERING_INT_MUX[1:0]	2:1	Main window dering intensity mux.	
	MAIN_DERING_EN	0	Main window dering enable.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_DERING_REF_WIDTH [1:0]	5:4	Sub window dering reference width. 0: 5 pixel. 1: 4 pixel. 2: 3 pixel. 3: 2 pixel.	
	-	3	Reserved.	
	SUB_DERING_INT_MUX[1:0]	2:1	Sub window dering intensity mux.	
	SUB_DERING_EN	0	Sub window dering enable.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_DERING_BRIGHT_GAIN[3:0]	7:4	Sub window dering bright strength gain (x.xxx).	
	MAIN_DERING_BRIGHT_GAIN[3:0]	3:0	Main window dering bright strength gain (x.xxx).	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_DERING_DARK_GAIN [3:0]	7:4	Sub window dering dark strength gain (x.xxx).	
	MAIN_DERING_DARK_GAIN[3:0]	3:0	Main window dering dark strength gain (x.xxx).	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_0[7:0]	7:0	Gaussian SNR Table 0.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_1[7:0]	7:0	Gaussian SNR Table 1.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_2[7:0]	7:0	Gaussian SNR Table 2.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_3[7:0]	7:0	Gaussian SNR Table 3.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_4[7:0]	7:0	Gaussian SNR Table 4.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_5[7:0]	7:0	Gaussian SNR Table 5.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SNR_LUT_6[7:0]	7:0	Gaussian SNR Table 6.	
67h	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SNR_LUT_7[7:0]	7:0	Gaussian SNR Table 7.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND9_COEF[6:0]	6:0	Main window band9 coefficient (Sxxx.xxx).	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND10_COEF[6:0]	6:0	Main window band10 coefficient (Sxxx.xxx).	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND11_COEF[6:0]	6:0	Main window band11 coefficient (Sxxx.xxx).	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BAND12_COEF[6:0]	6:0	Main window band12 coefficient (Sxxx.xxx).	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND9_COEF[6:0]	6:0	Sub window band9 coefficient (Sxxx.xxx).	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND10_COEF[6:0]	6:0	Sub window band10 coefficient (Sxxx.xxx).	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND11_COEF[6:0]	6:0	Sub window band11 coefficient (Sxxx.xxx).	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_BAND12_COEF[6:0]	6:0	Sub window band12 coefficient (Sxxx.xxx).	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_PK_ADP_Y_STEP[1:0]	5:4	Sub window peaking adaptive y alpha step.	
	-	3:2	Reserved.	
	SUB_PK_ADP_Y_ALPHA_LPF_EN	1	Sub window peaking adaptive y alpha low pass filter enable.	
	SUB_PK_ADP_Y_EN	0	Sub window peaking adaptive y enable.	
6Dh	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_PK_Y_LOW_THRD[7:0]	7:0	Sub window peaking adaptive y low threshold.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x54**	**Access : R/W**
	SUB_PK_ADP_Y_ALPHA_LUT_1[3:0]	7:4	Sub window peaking adaptive y alpha LUT 1.	
	SUB_PK_ADP_Y_ALPHA_LUT_0[3:0]	3:0	Sub window peaking adaptive y alpha LUT 0.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default : 0x76**	**Access : R/W**
	SUB_PK_ADP_Y_ALPHA_LUT_3[3:0]	7:4	Sub window peaking adaptive y alpha LUT 3.	
	SUB_PK_ADP_Y_ALPHA_LUT_2[3:0]	3:0	Sub window peaking adaptive y alpha LUT 2.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_PK_ADP_Y_ALPHA_LUT_5[3:0]	7:4	Sub window peaking adaptive y alpha LUT 5.	
	SUB_PK_ADP_Y_ALPHA_LUT_4[3:0]	3:0	Sub window peaking adaptive y alpha LUT 4.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_PK_ADP_Y_ALPHA_LUT_7[3:0]	7:4	Sub window peaking adaptive y alpha LUT 7.	
	SUB_PK_ADP_Y_ALPHA_LUT_6[3:0]	3:0	Sub window peaking adaptive y alpha LUT 6.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND9_OVERSHOOT_LIMIT[7:0]	7:0	Window band9 overshoot limit.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND10_OVERSHOOT_LIMIT[7:0]	7:0	Window band10 overshoot limit.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND11_OVERSHOOT_LIMIT[7:0]	7:0	Window band11 overshoot limit.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND12_OVERSHOOT_LIMIT[7:0]	7:0	Window band12 overshoot limit.	
72h	**REG102FE4**	**7:0**	**Default : 0xFF**	**Access : R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BAND9_UNDERSHOOT_LIMIT[7:0]	7:0	Window band9 undershoot limit.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND10_UNDERSHOOT_LIMIT[7:0]	7:0	Window band10 undershoot limit.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND11_UNDERSHOOT_LIMIT[7:0]	7:0	Window band11 undershoot limit.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	BAND12_UNDERSHOOT_LIMIT[7:0]	7:0	Window band12 undershoot limit.	
74h ~ 78h (102FE8h ~ 102FF1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_V_NM_LOW_Y_EN	4	Sub window vertical mosquito noise low y mode enable.	
	-	3:1	Reserved.	
	MAIN_V_NM_LOW_Y_EN	0	Main window vertical mosquito noise low y mode enable.	
7Bh (102FF7h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x10**	**Access : R/W**
	MAIN_V_NM_LOW_Y_TH[7:0]	7:0	Main window vertical mosquito noise low y mode threshold.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_V_NM_LOW_Y_GAIN[5:0]	5:0	Main window vertical mosquito noise low y mode gain.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_V_NM_LOW_Y_STEP[1:0]	1:0	Main window vertical mosquito noise low y mode step.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x10**	**Access : R/W**
	SUB_V_NM_LOW_Y_TH[7:	7:0	Sub window vertical mosquito noise low y mode threshold.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	0]			
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_V_NM_LOW_Y_GAIN[5:0]	5:0	Sub window vertical mosquito noise low y mode gain.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_V_NM_LOW_Y_STEP[1:0]	1:0	Sub window vertical mosquito noise low y mode step.	

DLC Register (Bank = 102F, Sub-bank = 1A)

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_STATISTIC_V_START[7:0]	7:0	Main window histogram vertical start.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_STATISTIC_V_END[7:0]	7:0	Main window histogram vertical end.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_STATISTIC_V_START[7:0]	7:0	Sub window histogram vertical start.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_STATISTIC_V_END[7:0]	7:0	Sub window histogram vertical end.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	MAIN_CURVE_FIT_EN	7	Main window luma curve enable.	
	SUB_CURVE_FIT_EN	6	Sub window luma curve enable.	
	-	5	Reserved.	
	HISTOGRAM_MODE	4	0: 3 sections. 1: 8 sections.	
	STATISTIC_ACK	3	Histogram Acknowledge.	
	STATISTIC_REQUEST	2	Histogram Request.	
	MAIN_STATISTIC_EN	1	Main window statistic enable.	
	SUB_STATISTIC_EN	0	Sub window statistic enable.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CURVE_FIT_RGB_EN	5	Main window luma curve enable as PC(RGB) mode enable.	
	SUB_CURVE_FIT_RGB_EN	4	Sub window luma curve enable as PC(RGB) mode enable.	
	PRE_BRI_DITHER_EN	3	Pre- brightness adjust dither bit enable.	
	HIS_Y_RGB_MODE_EN	2	Histogram Y report as PC(RGB) mode enable.	
	ACC_COUNTER22_EN	1	Histogram report sum accumulator add 1bit.	
	VARIABLE_RANGE_EN	0	Variable 8 section of histogram enable.	
05h ~ 05h	**-**	**7:0**	**Default : -**	**Access : -**

DLC Register (Bank = 102F, Sub-bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	-	-	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_TOTAL_PIXEL_WEIGHT[7:0]	7:0	Main window histogram report sum of total Y.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_TOTAL_PIXEL_WEIGHT[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_TOTAL_PIXEL_COUNT[7:0]	7:0	Main window histogram report sum of pixel number.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_TOTAL_PIXEL_COUNT[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_RANGE_EN	7	Main window histogram range enable.	
	MAIN_BLE_EN	6	Firmware main window black level extension enable.	
	MAIN_WLE_EN	5	Firmware main window white level extension enable.	
	-	4	Reserved.	
	SUB_RANGE_EN	3	Sub window histogram range enable.	
	SUB_BLE_EN	2	Firmware sub window black level extension enable.	
	SUB_WLE_EN	1	Firmware sub window white level extension enable.	
	HIS_ACCELERATE_EN	0	Histogram report accelerate enable.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	UVC_DITHER_EN	7	UV compensate dither enable.	
	-	6:5	Reserved.	
	SUB_UVC_EN	4	Sub window UV compensate enable.	
	-	3:1	Reserved.	
	MAIN_UVC_EN	0	Main window UV compensate enable.	
09h ~ 0Ah (102F12h ~ 102F15h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximum pixel.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MAX_PIXEL[7:0]	7:0	Sub window maximum pixel.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_MIN_PIXEL[7:0]	7:0	Sub window minimum pixel.	
0Dh ~ 0Dh (102F1Ah ~ 102F1Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_BRI_ADJUST_LSB[1:0]	1:0	Sub window Y adjust low bit.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust (2's complement).	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_BRI_ADJUST[7:0]	7:0	Sub window Y adjust (2's complement).	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x40**	**Access : R/W**
	MAIN_Y_GAIN[7:0]	7:0	Main window Y gain.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x40**	**Access : R/W**
	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x40**	**Access : R/W**
	SUB_Y_GAIN[7:0]	7:0	Sub window Y gain.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x40**	**Access : R/W**
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x40**	**Access : R/W**
	MAIN_PRE_Y_GAIN[7:0]	7:0	Main window pre- Y gain.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x40**	**Access : R/W**
	SUB_PRE_Y_GAIN[7:0]	7:0	Sub window pre- Y gain.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_SECOND_POST_BRI_ADJUST_LSB[1:0]	3:2	Main window second post Y adjust low bit (2's complement).	
	MAIN_POST_BRI_ADJUST_LSB[1:0]	1:0	Main window post Y adjust low bit (2's complement).	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_SECOND_POST_BRI_ADJUST_LSB[1:0]	3:2	Sub window second post Y adjust low bit (2's complement).	
	SUB_POST_BRI_ADJUST_LSB[1:0]	1:0	Sub window post Y adjust low bit (2's complement).	
18h	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**

DLC Register (Bank = 102F, Sub-bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_POST_BRI_ADJUST[7:0]	7:0	Main window post Y adjust.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_POST_BRI_ADJUST[7:0]	7:0	Sub window post Y adjust.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SECOND_POST_BRI_ADJUST[7:0]	7:0	Main window second post Y adjust.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SECOND_POST_BRI_ADJUST[7:0]	7:0	Sub window second post Y adjust.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_STATISTIC_H_START[7:0]	7:0	Main window histogram horizontal start.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_STATISTIC_H_END[7:0]	7:0	Main window histogram horizontal end.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_STATISTIC_H_START[7:0]	7:0	Sub window histogram horizontal start.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_STATISTIC_H_END[7:0]	7:0	Sub window histogram horizontal end.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x20**	**Access : R/W**
	HISTOGRAM_RANGE1[7:0]	7:0	Variable 8 section of histogram range 1.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x40**	**Access : R/W**
	HISTOGRAM_RANGE2[7:0]	7:0	Variable 8 section of histogram range 2.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x60**	**Access : R/W**
	HISTOGRAM_RANGE3[7:0]	7:0	Variable 8 section of histogram range 3.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x80**	**Access : R/W**
	HISTOGRAM_RANGE4[7:0]	7:0	Variable 8 section of histogram range 4.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0xA0**	**Access : R/W**
	HISTOGRAM_RANGE5[7:0]	7:0	Variable 8 section of histogram range 5.	
1Eh	**REG102F3D**	**7:0**	**Default : 0xC0**	**Access : R/W**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HISTOGRAM_RANGE6[7:0]	7:0	Variable 8 section of histogram range 6.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xE0**	**Access : R/W**
	HISTOGRAM_RANGE7[7:0]	7:0	Variable 8 section of histogram range 7.	
20h ~ 27h (102F40h ~ 102F4Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_1F_00[7:0]	7:0	Histogram report section1.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_1F_00[15:8]	7:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_3F_20[7:0]	7:0	Histogram report section2.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_3F_20[15:8]	7:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_5F_40[7:0]	7:0	Histogram report section3.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_5F_40[15:8]	7:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_7F_60[7:0]	7:0	Histogram report section4.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_7F_60[15:8]	7:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_9F_80[7:0]	7:0	Histogram report section5.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_9F_80[15:8]	7:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_BF_A0[7:0]	7:0	Histogram report section6.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_BF_A0[15:8]	7:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_DF_C0[7:0]	7:0	Histogram report section7.	
2Eh	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TOTAL_DF_C0[15:8]	7:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_FF_E0[7:0]	7:0	Histogram report section8.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_FF_E0[15:8]	7:0	See description of '102F5Eh'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x18**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x28**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x38**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x48**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x58**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x68**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x78**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x98**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_	7:0	Main window curve table 9.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	9[7:0]			
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0xA8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0xC8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0xE8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x08**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_0[7:0]	7:0	Sub window curve table 0.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x18**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_1[7:0]	7:0	Sub window curve table 1.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x28**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_2[7:0]	7:0	Sub window curve table 2.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x38**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_3[7:0]	7:0	Sub window curve table 3.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x48**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_4[7:0]	7:0	Sub window curve table 4.	
3Ah	**REG102F75**	**7:0**	**Default : 0x58**	**Access : R/W**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_CURVE_FIT_TABLE_5 [7:0]	7:0	Sub window curve table 5.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x68**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_6 [7:0]	7:0	Sub window curve table 6.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x78**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_7 [7:0]	7:0	Sub window curve table 7.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_8 [7:0]	7:0	Sub window curve table 8.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x98**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_9 [7:0]	7:0	Sub window curve table 9.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0xA8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_10[7:0]	7:0	Sub window curve table 10.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_11[7:0]	7:0	Sub window curve table 11.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0xC8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_12[7:0]	7:0	Sub window curve table 12.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0xD8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_13[7:0]	7:0	Sub window curve table 13.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0xE8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_14[7:0]	7:0	Sub window curve table 14.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0xF8**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_15[7:0]	7:0	Sub window curve table 15.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_0[7:0]	7:0	Histogram report section 32_0.	
40h	**REG102F81**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TOTAL_32_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_1[7:0]	7:0	Histogram report section 32_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_4[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_5[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_6[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_7[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.	
48h	**REG102F91**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TOTAL_32_8[15:8]	7:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_9[15:8]	7:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_10[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_11[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_12[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_13[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_14[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_15[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.	
50h	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TOTAL_32_16[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_17[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_18[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_19[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_20[15:8]	7:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_21[15:8]	7:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_22[15:8]	7:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_23[15:8]	7:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.	
58h	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TOTAL_32_24[15:8]	7:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_25[15:8]	7:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_26[15:8]	7:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[7:0]	7:0	Histogram report section 32_27.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_27[15:8]	7:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[7:0]	7:0	Histogram report section 32_28.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_28[15:8]	7:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[7:0]	7:0	Histogram report section 32_29.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_29[15:8]	7:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[7:0]	7:0	Histogram report section 32_30.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_30[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[7:0]	7:0	Histogram report section 32_31.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	TOTAL_32_31[15:8]	7:0	See description of '102FBEh'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : RO**
	MAIN_TOTAL_PIXEL_DIFF[7:0]	7:0	Main window histogram report sum of difference Y.	
63h	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_TOTAL_PIXEL_DIFF[15:8]	7:0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x60**	**Access : R/W**
	MAIN_UVC_GAIN_HIGH_LIMIT[7:0]	7:0	Main window UV compensate gain up limit (format is 4.8).	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_HIGH_LIMIT[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0xC0**	**Access : R/W**
	MAIN_UVC_GAIN_LOW_LIMIT[7:0]	7:0	Main window UV compensate gain down limit (format is 4.8).	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_LOW_LIMIT[11:8]	3:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x60**	**Access : R/W**
	SUB_UVC_GAIN_HIGH_LIMIT[7:0]	7:0	Sub window UV compensate gain up limit (format is 4.8).	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_UVC_GAIN_HIGH_LIMIT[11:8]	3:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0xC0**	**Access : R/W**
	SUB_UVC_GAIN_LOW_LIMIT[7:0]	7:0	Sub window UV compensate gain down limit (format is 4.8).	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_UVC_GAIN_LOW_LIMIT[11:8]	3:0	See description of '102FCEh'.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_TOTAL_PIXEL_COUNT[7:0]	7:0	Sub window histogram report sum of pixel number.	
72h	**REG102FE5**	**7:0**	**Default : 0x00**	**Access : RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_TOTAL_PIXEL_COUNT[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_TOTAL_PIXEL_WEIGHT[7:0]	7:0	Sub window histogram report sum of total Y.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_TOTAL_PIXEL_WEIGHT[15:8]	7:0	See description of '102FE6h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_TOTAL_PIXEL_DIFF[7:0]	7:0	Sub window histogram report sum of difference Y.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : RO**
	SUB_TOTAL_PIXEL_DIFF[15:8]	7:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_N0[7:0]	7:0	Main window curve table left point, MSB is sign bit.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_N0[8]	0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x08**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_16[7:0]	7:0	Main window curve table 16.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_16[8]	0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_LSB_2[1:0]	7:6	Main window curve table 2 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_1[1:0]	5:4	Main window curve table 1 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_0[1:0]	3:2	Main window curve table 0 LSB.	

DLC Register (Bank = 102F, Sub-bank = 1A)

Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_CURVE_FIT_TABLE_LSB_N0[1:0]	1:0	Main window curve table n0 LSB.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_LSB_6[1:0]	7:6	Main window curve table 6 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_5[1:0]	5:4	Main window curve table 5 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_4[1:0]	3:2	Main window curve table 4 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_3[1:0]	1:0	Main window curve table 3 LSB.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_LSB_10[1:0]	7:6	Main window curve table 10 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_9[1:0]	5:4	Main window curve table 9 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_8[1:0]	3:2	Main window curve table 8 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_7[1:0]	1:0	Main window curve table 7 LSB.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CURVE_FIT_TABLE_LSB_14[1:0]	7:6	Main window curve table 14 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_13[1:0]	5:4	Main window curve table 13 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_12[1:0]	3:2	Main window curve table 12 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_11[1:0]	1:0	Main window curve table 11 LSB.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CURVE_FIT_TABLE_LSB_16[1:0]	3:2	Main window curve table 16 LSB.	
	MAIN_CURVE_FIT_TABLE_LSB_15[1:0]	1:0	Main window curve table 15 LSB.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_LSB_2[1:0]	7:6	Sub window curve table 2 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_1[1:0]	5:4	Sub window curve table 1 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_0[1:0]	3:2	Sub window curve table 0 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_N0[1:0]	1:0	Sub window curve table n0 LSB.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_LSB_6[1:0]	7:6	Sub window curve table 6 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_5[1:0]	5:4	Sub window curve table 5 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_4[1:0]	3:2	Sub window curve table 4 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_3[1:0]	1:0	Sub window curve table 3 LSB.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_LSB_10[1:0]	7:6	Sub window curve table 10 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_9[1:0]	5:4	Sub window curve table 9 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_8[1:0]	3:2	Sub window curve table 8 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_7[1:0]	1:0	Sub window curve table 7 LSB.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_LSB_14[1:0]	7:6	Sub window curve table 14 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_13[1:0]	5:4	Sub window curve table 13 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_12[1:0]	3:2	Sub window curve table 12 LSB.	
	SUB_CURVE_FIT_TABLE_L	1:0	Sub window curve table 11 LSB.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SB_11[1:0]			
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_CURVE_FIT_TABLE_LSB_16[1:0]	3:2	Sub window curve table 16 LSB.	
	SUB_CURVE_FIT_TABLE_LSB_15[1:0]	1:0	Sub window curve table 15 LSB.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x08**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_N0[7:0]	7:0	Sub window curve table left point, MSB is sign bit.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SUB_CURVE_FIT_TABLE_N0[8]	0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x08**	**Access : R/W**
	SUB_CURVE_FIT_TABLE_16[7:0]	7:0	Sub window curve table 16.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:1	Reserved.	
	SUB_CURVE_FIT_TABLE_16[8]	0	See description of '102FFEh'.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)

DLC2 Register (Bank = 102F, Sub-bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_FCC_FR_EN	1	Sub window FCC region 1 enable for full range.	
	MAIN_FCC_FR_EN	0	Main window FCC region 1 enable for full range.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T2_LSB[1:0]	7:6	FCC region 2 cr target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CB_T2_LSB[1:0]	5:4	FCC region 2 cb target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CR_T1_LSB[1:0]	3:2	FCC region 1 cr target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CB_T1_LSB[1:0]	1:0	FCC region 1 cb target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T4_LSB[1:0]	7:6	FCC region 4 cr target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CB_T4_LSB[1:0]	5:4	FCC region 4 cb target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CR_T3_LSB[1:0]	3:2	FCC region 3 cr target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CB_T3_LSB[1:0]	1:0	FCC region 3 cb target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T6_LSB[1:0]	7:6	FCC region 6 cr target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CB_T6_LSB[1:0]	5:4	FCC region 6 cb target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CR_T5_LSB[1:0]	3:2	FCC region 5 cr target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
	FCC_FR_CB_T5_LSB[1:0]	1:0	FCC region 5 cb target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_CR_T8_LSB[1:0]	7:6	FCC region 8 cr target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description
	FCC_FR_CB_T8_LSB[1:0]	5:4	FCC region 8 cb target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.
	FCC_FR_CR_T7_LSB[1:0]	3:2	FCC region 7 cr target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.
	FCC_FR_CB_T7_LSB[1:0]	1:0	FCC region 7 cb target for full range, LSB. FCC_FR_CB_T1 = {FCC_CB_T1,FCC_FR_CB_T1_LSB}.
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00** **Access : R/W**
	FCC_FR_CB_T9[7:0]	7:0	FCC region 9 cb target for full range.
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:2	Reserved.
	FCC_FR_CB_T9[9:8]	1:0	See description of '102F66h'.
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00** **Access : R/W**
	FCC_FR_CR_T9[7:0]	7:0	FCC region 9 cr target for full range.
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:2	Reserved.
	FCC_FR_CR_T9[9:8]	1:0	See description of '102F68h'.
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00** **Access : R/W**
	FCC_FR_WIN1_CR_DOWN[7:0]	7:0	FCC region 1 target cr down distance for full range,
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:2	Reserved.
	FCC_FR_WIN1_CR_DOWN[9:8]	1:0	See description of '102F6Ah'.
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00** **Access : R/W**
	FCC_FR_WIN1_CR_UP[7:0]	7:0	FCC region 1 target cr up distance for full range.
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00** **Access : R/W**
	-	7:2	Reserved.
	FCC_FR_WIN1_CR_UP[9:8]	1:0	See description of '102F6Ch'.
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00** **Access : R/W**
	FCC_FR_WIN1_CB_DOWN[7:0]	7:0	FCC region 1 target cb down distance for full range.
37h	**REG102F6F**	**7:0**	**Default : 0x00** **Access : R/W**

DLC2 Register (Bank = 102F, Sub-bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
	-	7:2	Reserved.	
	FCC_FR_WIN1_CB_DOWN[9:8]	1:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN1_CB_UP[7:0]	7:0	FCC region 1 target cb up distance for full range.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN1_CB_UP[9:8]	1:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN2_CR_DOWN[7:0]	7:0	FCC region 2 target cr down distance for full range.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN2_CR_DOWN[9:8]	1:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN2_CR_UP[7:0]	7:0	FCC region 2 target cr up distance for full range.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN2_CR_UP[9:8]	1:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN2_CB_DOWN[7:0]	7:0	FCC region 2 target cb down distance for full range.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN2_CB_DOWN[9:8]	1:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN2_CB_UP[7:0]	7:0	FCC region 2 target cb up distance for full range.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN2_CB_UP[9:8]	1:0	See description of '102F78h'.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN3_CR_DOWN[7:0]	7:0	FCC region 3 target cr down distance for full range.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN3_CR_DOWN[9:8]	1:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN3_CR_UP[7:0]	7:0	FCC region 3 target cr up distance for full range.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN3_CR_UP[9:8]	1:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN3_CB_DOWN[7:0]	7:0	FCC region 3 target cb down distance for full range.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN3_CB_DOWN[9:8]	1:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN3_CB_UP[7:0]	7:0	FCC region 3 target cb up distance for full range.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN3_CB_UP[9:8]	1:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN4_CR_DOWN[7:0]	7:0	FCC region 4 target cr down distance for full range.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN4_CR_DOWN[9:8]	1:0	See description of '102F82h'.	
42h	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**

DLC2 Register (Bank = 102F, Sub-bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
	FCC_FR_WIN4_CR_UP[7:0]	7:0	FCC region 4 target cr up distance for full range.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN4_CR_UP[9:8]	1:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN4_CB_DOWN[7:0]	7:0	FCC region 4 target cb down distance for full range.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN4_CB_DOWN[9:8]	1:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN4_CB_UP[7:0]	7:0	FCC region 4 target cb up distance for full range.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN4_CB_UP[9:8]	1:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN5_CR_DOWN[7:0]	7:0	FCC region 5 target cr down distance for full range.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN5_CR_DOWN[9:8]	1:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN5_CR_UP[7:0]	7:0	FCC region 5 target cr up distance for full range.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN5_CR_UP[9:8]	1:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN5_CB_DOWN[	7:0	FCC region 5 target cb down distance for full range.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
	7:0]			
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN5_CB_DOWN[9:8]	1:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN5_CB_UP[7:0]	7:0	FCC region 5 target cb up distance for full range.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN5_CB_UP[9:8]	1:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN6_CR_DOWN[7:0]	7:0	FCC region 6 target cr down distance for full range.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN6_CR_DOWN[9:8]	1:0	See description of '102F92h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN6_CR_UP[7:0]	7:0	FCC region 6 target cr up distance for full range.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN6_CR_UP[9:8]	1:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN6_CB_DOWN[7:0]	7:0	FCC region 6 target cb down distance for full range.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN6_CB_DOWN[9:8]	1:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN6_CB_UP[7:0]	7:0	FCC region 6target cb up distance for full range.	
52h	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**

DLC2 Register (Bank = 102F, Sub-bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:2	Reserved.	
	FCC_FR_WIN6_CB_UP[9:8]	1:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN7_CR_DOWN[7:0]	7:0	FCC region 7 target cr down distance for full range.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN7_CR_DOWN[9:8]	1:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN7_CR_UP[7:0]	7:0	FCC region 7 target cr up distance for full range.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN7_CR_UP[9:8]	1:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN7_CB_DOWN[7:0]	7:0	FCC region 7 target cb down distance for full range.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN7_CB_DOWN[9:8]	1:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN7_CB_UP[7:0]	7:0	FCC region 7 target cb up distance for full range.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN7_CB_UP[9:8]	1:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN8_CR_DOWN[7:0]	7:0	FCC region 8 target cr down distance for full range.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN8_CR_DOWN[	1:0	See description of '102FAEh'.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
	9:8]			
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN8_CR_UP[7:0]	7:0	FCC region 8 target cr up distance for full range.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN8_CR_UP[9:8]	1:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN8_CB_DOWN[7:0]	7:0	FCC region 8 target cb down distance for full range.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN8_CB_DOWN[9:8]	1:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN8_CB_UP[7:0]	7:0	FCC region 8 target cb up distance for full range.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN8_CB_UP[9:8]	1:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN9_CR_DOWN[7:0]	7:0	FCC region 9 target cr down distance for full range.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN9_CR_DOWN[9:8]	1:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN9_CR_UP[7:0]	7:0	FCC region 9 target cr up distance for full range.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN9_CR_UP[9:8]	1:0	See description of '102FB8h'.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN9_CB_DOWN[7:0]	7:0	FCC region 9 target cb down distance for full range.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN9_CB_DOWN[9:8]	1:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	FCC_FR_WIN9_CB_UP[7:0]	7:0	FCC region 9 target cb up distance for full range.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FCC_FR_WIN9_CB_UP[9:8]	1:0	See description of '102FBCh'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VIP_MAIN_CLAMP_EN	0	Vip main window clamp enable.	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VIP_SUB_CLAMP_EN	0	Vip sub window clamp enable.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_Y_MAX_CLAMP[7:0]	7:0	Main window y maximum clamp.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_Y_MAX_CLAMP[9:8]	1:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_Y_MIN_CLAMP[7:0]	7:0	Main window y minimum clamp.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_Y_MIN_CLAMP[9:8]	1:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_CB_MAX_CLAMP[7:0]	7:0	Main window cb maximum clamp.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	

DLC2 Register (Bank = 102F, Sub-bank = 1B)

Index (Absolute)	Mnemonic	Bit	Description	
	MAIN_CB_MAX_CLAMP[9:8]	1:0	See description of '102FE8h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CB_MIN_CLAMP[7:0]	7:0	Main window cb minimum clamp.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_CB_MIN_CLAMP[9:8]	1:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	MAIN_CR_MAX_CLAMP[7:0]	7:0	Main window cr maximum clamp.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_CR_MAX_CLAMP[9:8]	1:0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_CR_MIN_CLAMP[7:0]	7:0	Main window cr minimum clamp.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	MAIN_CR_MIN_CLAMP[9:8]	1:0	See description of '102FEEh'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SUB_Y_MAX_CLAMP[7:0]	7:0	Sub window y maximum clamp.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_Y_MAX_CLAMP[9:8]	1:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_Y_MIN_CLAMP[7:0]	7:0	Sub window y minimum clamp.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_Y_MIN_CLAMP[9:8]	1:0	See description of '102FF6h'.	
7Ch	**REG102FF8**	**7:0**	**Default : 0xFF**	**Access : R/W**

DLC2 Register (Bank = 102F, Sub-bank = 1B)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_CB_MAX_CLAMP[7:0]	7:0	Sub window cb maximum clamp.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_CB_MAX_CLAMP[9:8]	1:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CB_MIN_CLAMP[7:0]	7:0	Sub window cb minimum clamp.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_CB_MIN_CLAMP[9:8]	1:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	SUB_CR_MAX_CLAMP[7:0]	7:0	Sub window cr maximum clamp.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_CR_MAX_CLAMP[9:8]	1:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_CR_MIN_CLAMP[7:0]	7:0	Sub window cr minimum clamp.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SUB_CR_MIN_CLAMP[9:8]	1:0	See description of '102FFEh'.	

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_IDX_DEPTH[7:0]	7:0	The number of menuload data. 0: Disable menuload.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_IDX_DEPTH[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_EN	7	Menuload enable.	
	-	6:4	Reserved.	
	MLOAD_REQ_LEN[3:0]	3:0	Length of menuload DMA's request. 0: Disable menuload.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[7:0]	7:0	Base address of allocated memory for menuload.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLOAD_BASE_ADR[23:16]	7:0	See description of '102F06h'.	
04h (102F09h)	**REG102F09**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	MLOAD_BASE_ADR[24]	0	See description of '102F06h'.	
08h ~ 0Bh (102F10h ~ 102F17h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_REQ_LEN[3:0]	7:4	Length of dynamic scaling DMA's request. 0: Disable dynamic scaling.	
	DS_REQ_TH[3:0]	3:0	Threshold for one dynamic scaling DMA request.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_IPM2MI_SEL	7	Main IP dynamic scaling miu selection.	
	DS_IPS2MI_SEL	6	Sub IP dynamic scaling miu selection.	
	DS_OP2MI_SEL	5	OP dynamic scaling miu selection.	
	DS_RIU_WE	4	Enable write register through RIU.	
	IPM_DS_EN	3	Enable main IP2 dynamic scaling.	

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
	IPS_DS_EN	2	Enable sub IP2 dynamic scaling.	
	OP_DS_EN	1	Enable OP dynamic scaling.	
	DS_REQ_PRI	0	User specified priority of MIU.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[7:0]	7:0	Base address of allocated memory for dynamic scaling.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[15:8]	7:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_BASE_ADR[23:16]	7:0	See description of '102F22h'.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DS_BASE_ADR[24]	0	See description of '102F22h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	DS_IDX_DEPTH[7:0]	7:0	The number of dynamic scaling data per index. 0: Disable dynamic scaling.	
13h ~ 16h (102F27h ~ 102F2Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	DS_RIU_BE[1:0]	1:0	Byte enable for DS RIU interface.	
18h ~ 1Bh (102F30h ~ 102F37h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_V_BASEADDR[7:0]	7:0	DRAM base address for keystone vertical parameter.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_V_BASEADDR[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_V_BASEADDR[23:16]	7:0	See description of '102F40h'.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	KST_V_BASEADDR[24]	0	See description of '102F40h'.	

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)

Index (Absolute)	Mnemonic	Bit	Description	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_H_BASEADDR[7:0]	7:0	DRAM base address for keystone horizontal parameter.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_H_BASEADDR[15:8]	7:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_H_BASEADDR[23:16]	7:0	See description of '102F44h'.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	KST_H_BASEADDR[24]	0	See description of '102F44h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	KST_V_NONLINEAR_EN	1	Keystone vertical nonlinear enable.	
	KST_EN	0	Keystone enable.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x01**	**Access : R/W**
	KST_TRIG_DLY[7:0]	7:0	Generate keystone trigger pulse from delayed line of Vsync.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SEL_KST[1:0]	7:6	Select the source to trigger menuload. 0: Falling edge of VFDE. 1: Rising edge of Vsync. 2: Falling edge of Vsync. 3: Delay line set by KST_TRIG_DLY.	
	-	5:4	Reserved.	
	KST_TRIG_DLY[11:8]	3:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_VSF_INI[7:0]	7:0	Initial vertical scaling ratio for keystone vertical nonlinear function.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_VSF_INI[15:8]	7:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	KST_VSF_INI[23:16]	7:0	See description of '102F4Ch'.	
30h ~ 47h (102F60h ~ 102F8Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x01**	**Access : R/W**
	PIP_DISABLE	7	Disable PIP Function.	
	-	6	Reserved.	
	SC2LB_EN	5	Enable HD side by side line buffer mode.	
	-	4:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	SW_SUB_EN	1	Enable sub window shown on the screen.	
	MAIN_EN	0	Enable main window shown on the screen.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	
	FBL_MASK_OVERLAP	5	Do not write overlapped portion of FBL channel to line buffer.	
	FBL_SEL	4	Select FBL source. b0: Source F2 is FBL. b1: Source F1 is FBL.	
	VBLANK_SUB	3	Fill the sub windows line buffer in vertical blanking.	
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.	
	F2_IS_SUB	1	Set main window display on the foreground.	
	MAIN_IS_TOP	0	Set second channel display in sub-window.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x70**	**Access : R/W**
	-	7	Reserved.	
	EXTRA_POS[2:0]	6:4	Enable extra request at specified region. [0] Enable at bottom B session. [1] Enable at bottom A session. [2] Enable at top session.	
	EXTRA_TH_LN[3:0]	3:0	Enable extra request for overlapping when the jumping line less than this threshold.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x07**	**Access : R/W**
	EXTRA_EN	7	Enable extra request engine.	
	VBLANK_OVL	6	Doing the extra request in vertical blanking.	
	EXTRA_Y_HALF	5	Reduce the EXTRA_Y to half.	
	-	4:3	Reserved.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	BO_LENGTH[2:0]	2:0	Select the length of extra request. h0: 16 pixel. h1: 32 pixel. h2: 64 pixel. h3: 128 pixel. h4: (overlap length) / 8. h5: (overlap length) / 4. h6: (overlap length) / 2. h7: (overlap length).	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F2[7:0]	7:0	The starting address of f2 stored at line buffer.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F2[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCLB_BASE_F1[7:0]	7:0	The starting address of f1 stored at line buffer.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F1[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BA_RIGHT[7:0]	7:0	Extend the pixel of bottom A session at the right side.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x08**	**Access : R/W**
	HEXT_BB_LEFT[7:0]	7:0	Extend the pixel of bottom B session at the left side.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F2[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	VLEN_F1[7:0]	7:0	Set the maximum request lines for first channel.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	VLEN_F1[11:8]	3:0	See description of '102F2Ch'.	
17h	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EXT_SUB_BORDER[3:0]	7:4	Extend the specified line in sub window to insert additional border.	
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional border.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x02**	**Access : R/W**
	EXTRA_ADV_LINE[3:0]	7:4	Advance the specified lines of extra end line (2's complement).	
	EXTRA_FETCH_LINE[3:0]	3:0	How many line will be fetched by extra request. Minimum is 1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	FORCE_F2_EN	1	Force F1 use F2's register setting.	
	ATP_EN	0	Manual tune parameter.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xB8**	**Access : R/W**
	-	7	Reserved.	
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter. 0: Vsync of SC_TOP. 1: Delay one line of VFDE.	
	SEL_DISP[1:0]	5:4	Select the trig point to start op1 engine. h0: DOWN_EQ7. h1: DOWN_EQ8. h2: DOWN_EQ9. h3: Delay lines set by DISP_TRIG_DLY.	
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. h0: Falling edge of Vsync. h1: Nearly raising edge of Vsync. h2: Delay line set by ATP_TRIG_DLY. h3: Manual trig by set ATP_EN.	
	SEL_SYNC[1:0]	1:0	Select the trig point for sync to initial engine. h0: Falling edge of Vsync. h1: Raising edge of Vsync. h2: Reserved. h3: Reserved.	
19h (102F33h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Ah	**REG102F34**	**7:0**	**Default : 0x03**	**Access : R/W**

OP1_TOP Register (Bank = 102F, Sub-bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
	ATP_TRIG_DLY[7:0]	7:0	Generate TRAIN_TRIG_P from delayed line of Vsync.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	ATP_TRIG_DLY[11:8]	3:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x05**	**Access : R/W**
	DISP_TRIG_DLY[7:0]	7:0	Generate DISP_TRIG_P from delayed line of Vsync.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HOVERSCAN_F1[7:0]	7:0	Offset line buffer position of F1 in right direction.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x10**	**Access : R/W**
	MIN_OVERLAP_TH[7:0]	7:0	Threshold of overlapped length. EXTRA_EQ will be disabled when overlapped length less then this threshold.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	MIN_OVERLAP_CNT[7:0]	7:0	Stop count between two extra request.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0xC2**	**Access : R/W**
	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. h0: 2 pixel. h1: 4 pixel. h2: 8 pixel. h3: 16 pixel.	
	DISP_START_MODE	5	Select the display line buffer start mode. 0: Start at advance 1 display line. 1: Start at falling edge of VSYNC_INIT.	
	DISP_LB_MODE	4	Select the trig mode. 0: Line base.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)

Index (Absolute)	Mnemonic	Bit	Description	
			1: Fill line buffer.	
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. h0: Before 8 pixel. h1: Before 16 pixel. h2: Before 32 pixel. h3: Before 64 pixel.	
	DISP_RLN_MODE[1:0]	1:0	Select the UNDER_RUN value of display level. h0: Update by Hsync (not optimum performance). h1: Update when session done (may error). h2: Update when line done (DISP_TRIG_MODE = 0). h3: Reserved.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SCLB_HALIGN2	5	Align the train result to specified pixel. h0: According to REG_SCLB_HALIGN setting. h1: 32 pixels.	
	-	4	Reserved.	
	DISP_UNDER_MODE	3	Select the UNDER_RUN value of display level. 0: 16'h0000. 1: 16'hffff.	
	DISP_PAT_EN	2	Enable internal pattern of OP1_DISP.	
	DISP_LB_WEZ	1	Disable wen of display line buffer.	
	DISP_TRIG_MODE	0	Select the trig mode. 0: Trigged by SELF_COUNTER. 1: Trigged by op2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0xFF**	**Access : R/W**
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x07**	**Access : R/W**
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x01**	**Access : R/W**
	DS_TRIG_DLY[7:0]	7:0	Generate DS_TRIG_P from delayed line of Vsync.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DS_TRIG_DLY[11:8]	3:0	See description of '102F42h'.	
22h	**REG102F44**	**7:0**	**Default : 0x01**	**Access : R/W**

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MLOAD_TRIG_DLY[7:0]	7:0	Generate MLOAD_TRIG_P from delayed line of Vsync.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MLOAD_TRIG_DLY[11:8]	3:0	See description of '102F44h'.	
23h ~ 28h (102F46h ~ 102F51h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FLAG_BB_ADR_INI	2	Status of CNT_BB_ADR_INI, write 1 to switch back to hardware. h0: Calculated by hardware. h1: Written by software.	
	FLAG_BO_END_LN	1	Status of LINE_BASE_BOT, write 1 to switch back to hardware. h0: Calculated by hardware. h1: Written by software.	
	-	0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BO_END_LN[7:0]	7:0	Software mode to set the LINE_BASE_BOT for extra request.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_BO_END_LN[11:8]	3:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_BB_ADR_INI[7:0]	7:0	Software mode to set the CNT_BB_ADR_INI.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SW_BB_ADR_INI[11:8]	3:0	See description of '102F64h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	DISPLAY_UNDERRUN	0	Indicate that the display line buffer is underrun in previous frame.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : RO**
	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line cnt of first display position.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line cnt of minimum display level occure.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	MIN_DISP_LINE[11:8]	3:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : RO**
	MIN_DISP_CNT[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : RO**
	MAX_DISP_CNT[15:8]	7:0	See description of '102F88h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_ADR_INI[7:0]	7:0	Read SCLB_TF_ADR_INI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_ADR_INI[11:8]	3:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_ADR_INI[7:0]	7:0	Read SCLB_BB_ADR_INI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_ADR_INI[11:8]	3:0	See description of '102FA4h'.	
53h	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : RO**

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCLB_BO_ADR_INI[7:0]	7:0	Read SCLB_BO_ADR_INI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BO_ADR_INI[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_TF_LEN[7:0]	7:0	Read SCLB_TF_LEN.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_TF_LEN[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BF_LEN[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BA_LEN[7:0]	7:0	Read SCLB_BA_LEN.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BA_LEN[11:8]	3:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : RO**
	SCLB_BB_LEN[7:0]	7:0	Read SCLB_BB_LEN.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	SCLB_BB_LEN[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1A[7:0]	7:0	Read FETCH_NUM_F1A.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1A[11:8]	3:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F1B[7:0]	7:0	Read FETCH_NUM_F1B.	
59h	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : RO**

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	FETCH_NUM_F1B[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2A[7:0]	7:0	Read FETCH_NUM_F2A.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2A[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_NUM_F2B[7:0]	7:0	Read FETCH_NUM_F2B.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2B[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : RO**
	FETCH_OFFSET_B[7:0]	7:0	Read FETCH_OFFSET_B.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	FETCH_OFFSET_B[11:8]	3:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_LENGTH_RD[7:0]	7:0	Read BO_LENGTH.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_LENGTH_RD[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_START_LN[7:0]	7:0	Read BO_START_LN.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_START_LN[11:8]	3:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : RO**
	BO_END_LN[7:0]	7:0	Read BO_END_LN.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	BO_END_LN[11:8]	3:0	See description of '102FBEh'.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_ADR_INI[7:0]	7:0	Read DISP_TF_ADR_INI.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_ADR_INI[11:8]	3:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_ADR_INI[7:0]	7:0	Read DISP_BB_ADR_INI.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_ADR_INI[11:8]	3:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_TF_LEN[7:0]	7:0	Read DISP_TF_LEN.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_TF_LEN[11:8]	3:0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BA_LEN[7:0]	7:0	Read DISP_BA_LEN.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BA_LEN[11:8]	3:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : RO**
	DISP_BB_LEN[7:0]	7:0	Read DISP_BB_LEN.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	DISP_BB_LEN[11:8]	3:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : RO**
	HSPR_BB_ADR_INI[7:0]	7:0	Read HSPR_BB_ADR_INI.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	HSPR_BB_ADR_INI[11:8]	3:0	See description of '102FCEh'.	
70h ~ 70h (102FE0h ~ 102FE1h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

ELA Register (Bank = 102F, Sub-bank = 21)

ELA Register (Bank = 102F, Sub-bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 0Fh (102F02h ~ 102F1Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. 1: Enable. 0: Disable.	
11h ~ 31h (102F22h ~ 102F63h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EODI_EN_F1	0	F1 window EODi enable. 0: Disable. 1: Enable.	
70h ~ 7Fh (102FE0h ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

TDDI Register (Bank = 102F, Sub-bank = 22)

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x04**	**Access : R/W**
	RATIO_DIV_YCSEP_F2	7	Main window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F2[2:0]	2:0	Main window ratio divide mode when Y/C separate.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F2[2:0]	5:3	Main window ratio divide mode.	
	RATIO_MD_F2[2:0]	2:0	Main window ratio filter mode.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x80**	**Access : R/W**
	RATIO_C_INDEP_F2	7	Main window C ratio independent mode. 0: Disable C ratio filter. 1: Enable C ratio filter.	
	RSV_02_2_F2[2:0]	6:4	Reserved.	
	RATIO_C_MIN_F2[3:0]	3:0	Main window C minimum ratio in independent mode.	
02h (102F05h)	**REG102F05**	**7:0**	**Default : 0x02**	**Access : R/W**
	RSV_02_0_F2[2:0]	7:5	Reserved.	
	-	4	Reserved.	
	RSV_02_1_F2[1:0]	3:2	Reserved.	
	RATIO_C_YMAX_SEL_F2	1	Main window C ratio takes Y ratio mode. 0: Select Y ratio before SST. 1: Select Y ratio after SST.	
	RATIO_C_YMAX_DIS_F2	0	Main window C ratio takes Y ratio mode disable. 0: Enable. 1: Disable.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	FILM_EODIW_EN_F2	7	Main window EODi weight compensation enable in film mode.	
	-	6:0	Reserved.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PRE_MOT_OFFSET_F2[5:0]	5:0	Main Window pre-memory motion offset for motion calculation.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PRE_MOT_GAIN_F2[3:0]	3:0	Main Window pre-memory motion gain for motion calculation.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	POST_MOT_OFFSET_F2[5:0]	5:0	Main Window post-memory motion offset for motion calculation.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x88**	**Access : R/W**
	POST_MOT_CGAIN_F2[3:0]	7:4	Main Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F2[3:0]	3:0	Main Window post-memory motion gain for C motion calculation.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x86**	**Access : R/W**
	POST_MOT_YMAX_EN_F2	7	Main Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F2[2:0]	2:0	Main Window history weighting.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x07**	**Access : R/W**
	RSV_STAT_0_F2[1:0]	7:6	Reserved.	
	STAT_INC_MODE_F2	5	Main window ratio statistics: ratio incremental mode.	
	STAT_SEL_C_F2	4	Main window ratio statistics: ratio selection.	
	STAT_CORE_F2[3:0]	3:0	Main window ratio statistics: coring threshold.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[7:0]	7:0	Main window ratio statistics: motion status.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : RO**
	MOTION_STATUS_F2[23:16]	7:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x4A**	**Access : R/W**
	ADAPT_MED_EN_F2	7	Main window adaptive DFK enable.	
	WEGT_MED_EN_F2	6	Main window weighted DFK enable.	
	RSV_MED_0_F2	5	Reserved.	
	MED_MANUAL_EN_F2	4	Main window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F2[3:0]	3:0	Main window DFK manual weighting.	

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F2[4:0]	4:0	Main window weighted DFK low-frequency begin.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F2[3:0]	3:0	Main window weighted DFK low-frequency slope adjustment.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x14**	**Access : R/W**
	-	7:5	Reserved.	
	MED_HF_BEGIN_F2[4:0]	4:0	Main window weighted DFK high-frequency begin.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F2[3:0]	3:0	Main window weighted DFK high-frequency slope adjustment.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x30**	**Access : R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F2[5:0]	5:0	Main window adaptive DFK motion threshold.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x13**	**Access : R/W**
	SST_EN_F2	7	Main window SST enable.	
	-	6	Reserved.	
	RSV_SST_0_F2	5	Reserved.	
	SST_MOTION_LPF_EN_F2	4	Main window SST low-pass on motion enable.	
	SST_MOTION_TH_F2[3:0]	3:0	Main window SST motion threshold.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x27**	**Access : R/W**
	RSV_SST_1_F2[1:0]	7:6	Reserved.	
	SST_ERODE_MODE_F2[1:0]	5:4	Main window SST motion area erosion mode.	
	RSV_SST_2_F2	3	Reserved.	
	SST_DILATE_MODE_F2[2:0]	2:0	Main window SST motion area dilation mode.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0xDF**	**Access : R/W**
	SST_POSTLPF_EN_F2	7	Main window SST post-LPF enable.	
	SST_POSTLPF_MAX_F2	6	Main window SST post-LPF maximum function enable.	
	SST_DYNAMIC_CORE_TH_F2[5:0]	5:0	Main window SST dynamic motion coring threshold.	

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x85**	**Access : R/W**
	SST_DYNAMIC_SGAIN_F2[3:0]	7:4	Main window SST dynamic motion spatial difference gain.	
	SST_DYNAMIC_TGAIN_F2[3:0]	3:0	Main window SST dynamic motion temporal difference gain.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	RSV_SST_3_F2[1:0]	7:6	Reserved.	
	SST_STATIC_CORE_TH_F2[5:0]	5:0	Main window SST static motion coring threshold.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x22**	**Access : R/W**
	SST_STATIC_SGAIN_F2[3:0]	7:4	Main window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F2[3:0]	3:0	Main window SST static motion temporal difference gain.	
20h ~ 2Ch (102F40h ~ 102F58h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	ADAPT_MED_EN_F1	7	Sub window adaptive DFK enable.	
	-	6:0	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	SST_EN_F1	7	Sub window SST enable.	
	-	6:0	Reserved.	
50h ~ 72h (102FA0h ~ 102FE4h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	FBASE_LVL_STATUS[1:0]	1:0	Frame-based level status.	
78h ~ 7Fh (102FF0h ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

HVSP Register (Bank = 102F, Sub-bank = 23)

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '102F02h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h (102F07h)	**REG102F07**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '102F06h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '102F0Ah'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '102F0Eh'.	

HVSP Register (Bank = 102F, Sub-bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_SHIFT_MODE_EN_F2	1	Main window horizontal scaling shift mode enable.	
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.	
09h (102F13h)	**REG102F13**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '102F12h'.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F2	7	Main window data format is 422.	
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F2	5	Main CR_LOAD initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.	
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.	
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.	
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.	
0Dh	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HSP_CORING_TH_Y_F2[7:0]	7:0	Main window horizontal Y coring threshold.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_DE_RING_G_ON_F2	7	Main window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F2[2:0]	6:4	Main window horizontal de-ringing threshold1.	
	-	3:2	Reserved.	
	HSP_DE_RING_TH0_F2[1:0]	1:0	Main window horizontal de-ringing threshold0.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HSP_DE_RING_METHOD_F2	0	Main window horizontal de-ringing method. 0: Blending. 1: Min-max + blending.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.	
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.	
	-	5	Reserved.	
	HSP_6TAP_EN_F2	4	Main window horizontal Y 6tap scaling enable.	
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F2	1	Main window field polarity switch.	
	2_INIFAC_MD_F2	0	Main window two initial factors mode.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F2	7	Main window vertical 3tap scaling enable.	
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width2 LSB.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width0 LSB.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width0.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width1.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width0.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BW_FIFO_EN_F2	0	Main window BW_FIFO enable.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO_F2[7:0]	7:0	Main window dynamic horizontal scaling factor.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO_F2[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_HO_F2[23:16]	7:0	See description of '102F38h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE_F2[7:0]	7:0	Main window dynamic vertical scaling factor.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE_F2[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_VE_F2[23:16]	7:0	See description of '102F3Ch'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[7:0]	7:0	MWE window horizontal initial factor.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR_HO_F1[15:8]	7:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F1[19:16]	3:0	See description of '102F42h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[7:0]	7:0	MWE window vertical initial factor 1.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[15:8]	7:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR1_VE_F1[23:16]	7:0	See description of '102F46h'.	
25h	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INI_FACTOR2_VE_F1[7:0]	7:0	MWE window vertical initial factor 2.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[15:8]	7:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	INI_FACTOR2_VE_F1[23:16]	7:0	See description of '102F4Ah'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[7:0]	7:0	MWE window horizontal scaling factor.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[15:8]	7:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_HO_F1[23:16]	7:0	See description of '102F4Eh'.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	H_SHIFT_MODE_EN_F1	1	MWE window horizontal scaling shift mode enable.	
	SCALE_HO_EN_F1	0	MWE window horizontal scaling enable.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[7:0]	7:0	MWE window vertical scaling factor.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[15:8]	7:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	SCALE_FACTOR_VE_F1[23:16]	7:0	See description of '102F52h'.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x80**	**Access : R/W**
	VFAC_DEC1_MD_F1	7	MWE window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F1	0	MWE window vertical scaling enable.	
2Bh	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	Y_RAM_SEL_HO_F1	7	MWE window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F1	6	MWE window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F1	5	MWE window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F1	4	MWE window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F1[2:0]	3:1	MWE window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F1	0	MWE window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	Y_RAM_SEL_VE_F1	7	MWE window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F1	6	MWE window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F1	5	MWE window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F1	4	MWE window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F1[2:0]	3:1	MWE window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F1	0	MWE window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0xC0**	**Access : R/W**
	FORMAT_422_F1	7	MWE window data format is 422.	

HVSP Register (Bank = 102F, Sub-bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
	422_INTP_F1	6	MWE window 422 Cb Cr interpolation enable.	
	-	5:2	Reserved.	
	VSP_DITH_EN_F1	1	MWE window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F1	0	MWE window dithering enable for horizontal scaling process.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F1	3	MWE window vertical Y coring enable.	
	VSP_CORING_EN_C_F1	2	MWE window vertical C coring enable.	
	HSP_CORING_EN_Y_F1	1	MWE window horizontal Y coring enable.	
	HSP_CORING_EN_C_F1	0	MWE window horizontal C coring enable.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_C_F1[7:0]	7:0	MWE window horizontal C coring threshold.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_CORING_TH_Y_F1[7:0]	7:0	MWE window horizontal Y coring threshold.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_C_F1[7:0]	7:0	MWE window vertical C coring threshold.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_CORING_TH_Y_F1[7:0]	7:0	MWE window vertical Y coring threshold.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	HSP_DE_RING_G_ON_F1	7	MWE window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F1[2:0]	6:4	MWE window horizontal de-ringing threshold1.	
	-	3:2	Reserved.	
	HSP_DE_RING_TH0_F1[1:0]	1:0	MWE window horizontal de-ringing threshold0.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	HSP_DE_RING_METHOD_F1	0	MWE window horizontal de-ringing method. 0: Blending. 1: Min-max + blending.	

HVSP Register (Bank = 102F, Sub-bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	HSP_6TAP_EN_F1	4	MWE window horizontal Y 6tap scaling enable.	
	-	3	Reserved.	
	OP_FIELD_SEL_F1	2	MWE window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F1	1	MWE window field polarity switch.	
	2_INIFAC_MD_F1	0	MWE window two initial factors mode.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	VSP_3TAP_EN_F1	7	MWE window vertical 3tap scaling enable.	
	-	6:0	Reserved.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	BW_FIFO_EN_F1	0	MWE window BW_FIFO enable.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO_F1[7:0]	7:0	MWE window dynamic horizontal scaling factor.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_HO_F1[15:8]	7:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_HO_F1[23:16]	7:0	See description of '102F78h'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE_F1[7:0]	7:0	MWE window dynamic vertical scaling factor.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DY_FACTOR_VE_F1[15:8]	7:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x10**	**Access : R/W**
	DY_FACTOR_VE_F1[23:16]	7:0	See description of '102F7Ch'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_CEN	7	SRAM CEN.	
	-	6:2	Reserved.	
	CRAM_RW_EN	1	C SRAM read/write enable.	
	YRAM_RW_EN	0	Y SRAM read/write enable.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	RAM_R_PULSE	1	SRAM read data pulse.	
	RAM_W_PULSE	0	SRAM write data pulse.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_ADDR[7:0]	7:0	For each C SRAM download: Bit5~0: address (0~63). Bit7,6: 00: C SRAM 0. 01: C SRAM 1. 10: C SRAM 2. 11: C SRAM 3. For each Y SRAM download: Bit6~0: address (0~127). bit7: 0: Y SRAM 0. 1: Y SRAM 1.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	YRAM_UPPER_SEL	0	Y SRAM upper address selection. 0: Address 0~127. 1: Address 128~255.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_48BIT[7:0]	7:0	SRAM write data[47:0].	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_48BIT[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_48BIT[23:16]	7:0	See description of '102F86h'.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_48BIT[31:24]	7:0	See description of '102F86h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_48BIT[39:32]	7:0	See description of '102F86h'.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_48BIT[47:40	7:0	See description of '102F86h'.	

HVSP Register (Bank = 102F, Sub-bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
	]			
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_48BIT[7:0]	7:0	SRAM read data[47:0].	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_48BIT[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_48BIT[23:16]	7:0	See description of '102F8Ch'.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_48BIT[31:24]	7:0	See description of '102F8Ch'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_48BIT[39:32]	7:0	See description of '102F8Ch'.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_48BIT[47:40]	7:0	See description of '102F8Ch'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	RAM_WDATA_12BIT[7:0]	7:0	SRAM write data[59:48].	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	RAM_WDATA_12BIT[11:8]	3:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : RO**
	RAM_RDATA_12BIT[7:0]	7:0	SRAM read data[59:48].	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	RAM_RDATA_12BIT[11:8]	3:0	See description of '102F9Ah'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x41**	**Access : R/W**
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.	
	FACTOR_MANUAL	6	Vertical factor manual mode.	
	VDOWN_SEL	5	Vertical scaling down selection. 0: Bottom. 1: Top.	
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.	
	-	3	Reserved.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.	
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VDOWN_SW_VALUE	3	Vertical scaling down software value. 0: No vertical scaling down. 1: Vertical scaling down.	
	VDOWN_SW_MODE	2	Vertical scaling down software mode.	
	HDOWN_SW_VALUE	1	Horizontal scaling down software value. 0: No horizontal scaling down. 1: Horizontal scaling down.	
	HDOWN_SW_MODE	0	Horizontal scaling down software mode.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish. 1: DE end.	
	-	6:0	Reserved.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	3DLR_SIDE2LINE_EN	7	3D LR side-by-side to line-by-line enable.	
	-	6:0	Reserved.	
58h ~ 5Fh (102FB0h ~ 102FBFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTI_STEP_F2[3:0]	7:4	Main window CTI step.	
	-	3	Reserved.	
	CTI_LPF_COEF_F2[2:0]	2:0	Main window CTI LPF coefficients.	
61h (102FC2h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F2	7	Main window CTI enable.	
	-	6:0	Reserved.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CTI_MUTUAL_THD_F2[3:0]	3:0	Main window CTI mutual threshold.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F2[2:0]	2:0	Main window CTI mutual step.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F2[1:0]	1:0	Main window CTI patch mode. 0: None. 1: Trans. 2: Clfp/wts. 3: Both.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F2[4:0]	4:0	Main window CTI mutual level patch threshold.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F2[5:0]	5:0	Main window CTI mutual trans level slope gain.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F2[4:0]	4:0	Main window CTI mutual C low freq threshold.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F2[5:0]	5:0	Main window CTI mutual C low freq slope gain.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_CLFP_STEP_F2[1:0]	1:0	Main window CTI mutual C low freq step.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x80**	**Access : R/W**
	CTI_STEP_F1[3:0]	7:4	MWE window CTI step.	
	-	3	Reserved.	
	CTI_LPF_COEF_F1[2:0]	2:0	MWE window CTI LPF coefficients.	
71h	**-**	**7:0**	**Default : -**	**Access : -**

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	-	Reserved.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	CTI_EN_F1	7	MWE window CTI enable.	
	-	6:0	Reserved.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F1[3:0]	3:0	MWE window CTI mutual threshold.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F1[2:0]	2:0	MWE window CTI mutual step.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F1[1:0]	1:0	MWE window CTI patch mode. 0: None. 1: Trans. 2: CLFP/WTS. 3: Both.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x04**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F1[4:0]	4:0	MWE window CTI mutual level patch threshold.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F1[5:0]	5:0	MWE window CTI mutual trans level slope gain.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F1[4:0]	4:0	MWE window CTI mutual C low freq threshold.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F1[5:0]	5:0	MWE window CTI mutual C low freq slope gain.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	

HVSP Register (Bank = 102F, Sub-bank = 23)

Index (Absolute)	Mnemonic	Bit	Description	
	CTI_CLFP_STEP_F1[1:0]	1:0	MWE window CTI mutual C low freq step.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	EXTRA_FACTOR_EN	0	Extra horizontal initial factor enable.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_1 [7:0]	7:0	Extra horizontal initial factor 1.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_1 [15:8]	7:0	See description of '102FF0h'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_1 [23:16]	7:0	See description of '102FF0h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_2 [7:0]	7:0	Extra horizontal initial factor 2.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_2 [15:8]	7:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_2 [23:16]	7:0	See description of '102FF4h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_3 [7:0]	7:0	Extra horizontal initial factor 3.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_3 [15:8]	7:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_3 [23:16]	7:0	See description of '102FF8h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_4 [7:0]	7:0	Extra horizontal initial factor 4.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_4 [15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXTRA_INI_FACTOR_HO_4 [23:16]	7:0	See description of '102FFCh'.	

FRC Register (Bank = 102F, Sub-bank = 24)

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x1B**	**Access : R/W**
	-	7:5	Reserved.	
	TAILCUT	4	TAILCUT enable.	
	NOISE_DITH_DISABLE	3	PAFRC mixed with noise dither disable. 0: Enable. 1: Disable.	
	DITH_BITS	2	Dithering bits. 0: 2-bits. 1: 4-bits.	
	TCON_OFF_EN	1	TCON FRC_GAMMA function off signal enable. 0: Ignore TCON gamma/dither turn off signal. 1: Gamma/dither function turn off by TCON FRC_GAMMA_OFF signal.	
	FRC_ON	0	PAFRC enable.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_ROTATE_EN	7	Box A/B/C/D relation rotation enable.	
	TOP_BOX_UNIT_FLAG[1:0]	6:5	Top box A/B/C/D swap flag. 00: Per 2x2 box. 01: Per 4x4 box. 1x: Per 8x8 box.	
	TOP_BOX_FREEZE	4	Top box freeze.	
	TOP_BOX_SHRINK	3	Top box shrink to 2x2 from 4x4.	
	FR_C2_BIT	2	Top box frame rotation step bit location for codexx10. 0: Bit[0]. 1: Bit[1].	
	C2X2_ROT_B_DIR_S	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_B_DIR_S	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	G_V_SWAP	6	Green channel vertical swap, avoid polarity not consistent.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	G_H_SWAP	5	Green channel horizontal swap, avoid polarity not consistent.	
	B_D_SWAP	4	Blue channel diagonal swap.	
	BOX_FR_SW	3	FRAME_CNT bit [1:0] swap for box rotate.	
	BOX4X4_FR_SW	2	FRAME_CNT bit [1:0] swap for box4x4 rotate.	
	BOX8X8_ROT_UNIT	1	0: Rotate step under per A, B, C or D. 1: Rotate step between A/B/C/D.	
	BOX_FREEZE	0	Box local rotation freeze.	
41h (102F82h)	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**
	C2X2_ROT_G_DIR	7	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_G_DIR	6	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_G_DIR_S	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_G_DIR_S	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	A2X2_ROT_B_DIR	3	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_B_DIR	2	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_B_DIR	1	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_B_DIR	0	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x00**	**Access : R/W**
	A2X2_ROT_R_DIR	7	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	

FRC Register (Bank = 102F, Sub-bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
	B2X2_ROT_R_DIR	6	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_R_DIR	5	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	D2X2_ROT_R_DIR	4	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	C2X2_ROT_R_DIR_S	3	C 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	D2X2_ROT_R_DIR_S	2	D 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise, 2nd.	
	A2X2_ROT_G_DIR	1	A 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
	B2X2_ROT_G_DIR	0	B 2x2 block rotation direction. 0: Counterwise. 1: Backcounterwise.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_SEQ2[7:0]	7:0	Top box frame 2nd 4 frame rotation step.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_SEQ1[7:0]	7:0	Top box frame 1st 4 frame rotation step.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_SEQ4[7:0]	7:0	Top box frame 4th 4 frame rotation step.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_SEQ3[7:0]	7:0	Top box frame 3rd 4 frame rotation step.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_C2_SEQ34[7:0]	7:0	Top box frame 3rd/4th 4 frame rotation step for codexx10.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x00**	**Access : R/W**
	TOP_BOX_FR_C2_SEQ12[7:0]	7:0	Top box frame 1st/2nd 4 frame rotation step for codexx10.	

FRC Register (Bank = 102F, Sub-bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_A_ROT_DIR	7	Location A frame counter direction. 0: Counterwise. 1: Back.	
	BOX_B_ROT_DIR	6	Location B frame counter direction. 0: Counterwise. 1: Back.	
	BOX_C_ROT_DIR	5	Location C frame counter direction. 0: Counterwise. 1: Back.	
	BOX_D_ROT_DIR	4	Location D frame counter direction. 0: Counterwise. 1: Back.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX8X8_ROT_00[1:0]	7:6	Box8x8 entity 00 rotation step by reference.	
	BOX8X8_ROT_01[1:0]	5:4	Box8x8 entity 01 rotation step by reference.	
	BOX8X8_ROT_11[1:0]	3:2	Box8x8 entity 11 rotation step by reference.	
	BOX8X8_ROT_10[1:0]	1:0	Box8x8 entity 10 rotation step by reference.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_LU_00[1:0]	7:6	B 2x2 block left up entity.	
	B_RU_01[1:0]	5:4	B 2x2 block right up entity.	
	B_RD_11[1:0]	3:2	B 2x2 block right down entity.	
	B_LD_10[1:0]	1:0	B 2x2 block left down entity.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default : 0x00**	**Access : R/W**
	A_LU_00[1:0]	7:6	A 2x2 block left up entity.	
	A_RU_01[1:0]	5:4	A 2x2 block right up entity.	
	A_RD_11[1:0]	3:2	A 2x2 block right down entity.	
	A_LD_10[1:0]	1:0	A 2x2 block left down entity.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	D_LU_00[1:0]	7:6	D 2x2 block left up entity.	
	D_RU_01[1:0]	5:4	D 2x2 block right up entity.	
	D_RD_11[1:0]	3:2	D 2x2 block right down entity.	
	D_LD_10[1:0]	1:0	D 2x2 block left down entity.	

FRC Register (Bank = 102F, Sub-bank = 24)

Index (Absolute)	Mnemonic	Bit	Description	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LU_00[1:0]	7:6	C 2x2 block left up entity.	
	C_RU_01[1:0]	5:4	C 2x2 block right up entity.	
	C_RD_11[1:0]	3:2	C 2x2 block right down entity.	
	C_LD_10[1:0]	1:0	C 2x2 block left down entity.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	D_LU_00_S[1:0]	7:6	D 2x2 block left up entity, 2nd.	
	D_RU_01_S[1:0]	5:4	D 2x2 block right up entity, 2nd.	
	D_RD_11_S[1:0]	3:2	D 2x2 block right down entity, 2nd.	
	D_LD_10_S[1:0]	1:0	D 2x2 block left down entity, 2nd.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	C_LU_00_S[1:0]	7:6	C 2x2 block left up entity, 2nd.	
	C_RU_01_S[1:0]	5:4	C 2x2 block right up entity, 2nd.	
	C_RD_11_S[1:0]	3:2	C 2x2 block right down entity, 2nd.	
	C_LD_10_S[1:0]	1:0	C 2x2 block left down entity, 2nd.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_B_LU_00[1:0]	7:6	Location B block A LSB 2 bits plus value.	
	BOX_B_RU_01[1:0]	5:4	Location B block B LSB 2 bits plus value.	
	BOX_B_RD_11[1:0]	3:2	Location B block C LSB 2 bits plus value.	
	BOX_B_LD_10[1:0]	1:0	Location B block D LSB 2 bits plus value.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_A_LU_00[1:0]	7:6	Location A block A LSB 2 bits plus value.	
	BOX_A_RU_01[1:0]	5:4	Location A block B LSB 2 bits plus value.	
	BOX_A_RD_11[1:0]	3:2	Location A block C LSB 2 bits plus value.	
	BOX_A_LD_10[1:0]	1:0	Location A block D LSB 2 bits plus value.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_D_LU_00[1:0]	7:6	Location D block A LSB 2 bits plus value.	
	BOX_D_RU_01[1:0]	5:4	Location D block B LSB 2 bits plus value.	
	BOX_D_RD_11[1:0]	3:2	Location D block C LSB 2 bits plus value.	
	BOX_D_LD_10[1:0]	1:0	Location D block D LSB 2 bits plus value.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**
	BOX_C_LU_00[1:0]	7:6	Location C block A LSB 2 bits plus value.	

FRC Register (Bank = 102F, Sub-bank = 24)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	BOX_C_RU_01[1:0]	5:4	Location C block B LSB 2 bits plus value.
	BOX_C_RD_11[1:0]	3:2	Location C block C LSB 2 bits plus value.
	BOX_C_LD_10[1:0]	1:0	Location C block D LSB 2 bits plus value.

XVYCC Register (Bank = 102F, Sub-bank = 25)

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	-	3:0	Reserved.	
01h (102F03h)	**REG102F03**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_RGB_COMPRESS_SEE_SAT_EN	7	Main window RGB compress by saturation enable.	
	-	6:3	Reserved.	
	XV_YCC_MAIN_RGB_COMPRESS_DITHER_EN	2	Main window RGB compress dither bit enable.	
	XV_YCC_MAIN_RGB_COMPRESS_EN	1	Main window RGB compress enable.	
	-	0	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	
	POST_SUB_BRI_EN	4	Sub window post brightness enable.	
	-	3:0	Reserved.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_RGB_COMPRESS_SEE_SAT_EN	7	Sub window RGB compress by saturation enable.	
	-	6:3	Reserved.	
	XV_YCC_SUB_RGB_COMPRESS_DITHER_EN	2	Sub window RGB compress dither bit enable.	
	XV_YCC_SUB_RGB_COMPRESS_EN	1	Sub window RGB compress function enable.	
	-	0	Reserved.	
21h	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post R channel offset.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post G channel offset.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post B channel offset.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post R channel gain.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post G channel gain.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F4Ah'.	

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_MAIN_B_CON_GAIN [7:0]	7:0	Main window post B channel gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN [11:8]	3:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_BRI_OFFSET [7:0]	7:0	Sub window post R channel offset.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET [10:8]	2:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_BRI_OFFSET [7:0]	7:0	Sub window post G channel offset.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET [10:8]	2:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_BRI_OFFSET [7:0]	7:0	Sub window post B channel offset.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	POST_SUB_B_BRI_OFFSET [10:8]	2:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post R channel gain.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[	3:0	See description of '102F54h'.	

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	11:8]			
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post G channel gain.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default : 0x00**	**Access : R/W**
	POST_SUB_B_CON_GAIN[7:0]	7:0	Sub window post B channel gain.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[11:8]	3:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GAIN1_TH[7:0]	7:0	Hbc gain1 threshold.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	GAMMA_OD_PIPE_SEL	0	Gamma and OD pipe select. 0: Gamma before OD. 1: Gamma after OD.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0[7:0]	7:0	Dummy register.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY0[15:8]	7:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1[7:0]	7:0	Dummy register.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default : 0x00**	**Access : R/W**
	DUMMY1[15:8]	7:0	See description of '102F5Eh'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	PAT_SWITCH	4	Initial pattern switch for pixel or dot pattern.	
	AUTO_FIT_EN	3	Enable auto fit window size.	

XVYCC Register (Bank = 102F, Sub-bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	SW_FREEZE_IDX	2	Software freeze pattern enable.	
	AUTO_IDX_EN	1	Auto run pattern enable.	
	PG_EN	0	Pattern generate enable.	
30h (102F61h)	**REG102F61**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PAT_DELTA[3:0]	3:0	Pattern increase delta value.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SW_SET_IDX[4:0]	4:0	Software set pattern idx.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	PAT_PERIOD[7:0]	7:0	Per pattern period, unit is frame.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAT_R[7:0]	7:0	R fix color.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	PAT_R[9:8]	1:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAT_G[7:0]	7:0	G fix color.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	PAT_G[9:8]	1:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PAT_B[7:0]	7:0	B fix color.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	PAT_B[9:8]	1:0	See description of '102F68h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_R_BLACK_START[6:0]	6:0	Main window R channel black start.	
40h (102F81h)	**REG102F81**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_R_BLACK_SLOP[7:0]	7:0	Main window R channel black slope.	
41h	**REG102F82**	**7:0**	**Default : 0x00**	**Access : R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7	Reserved.	
	MAIN_R_WHITE_START[6:0]	6:0	Main window R channel white start.	
41h (102F83h)	**REG102F83**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_R_WHITE_SLOP[7:0]	7:0	Main window R channel white slope.	
42h (102F84h)	**REG102F84**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_R_BLACK_START[6:0]	6:0	Sub window R channel black start.	
42h (102F85h)	**REG102F85**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_R_BLACK_SLOP[7:0]	7:0	Sub window R channel black slope.	
43h (102F86h)	**REG102F86**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_R_WHITE_START[6:0]	6:0	Sub window R channel white start.	
43h (102F87h)	**REG102F87**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_R_WHITE_SLOP[7:0]	7:0	Sub window R channel white slope.	
44h (102F88h)	**REG102F88**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_B_BLACK_START[6:0]	6:0	Main window B channel black start.	
44h (102F89h)	**REG102F89**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_B_BLACK_SLOP[7:0]	7:0	Main window B channel black slope.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_B_WHITE_START[6:0]	6:0	Main window B channel white start.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default : 0x80**	**Access : R/W**
	MAIN_B_WHITE_SLOP[7:0]	7:0	Main window B channel white slope.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_B_BLACK_START[6:0]	6:0	Sub window B channel black start.	
46h	**REG102F8D**	**7:0**	**Default : 0x80**	**Access : R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_B_BLACK_SLOP[7:0]	7:0	Sub window B channel black slope.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_B_WHITE_START[6:0]	6:0	Sub window B channel white start.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default : 0x80**	**Access : R/W**
	SUB_B_WHITE_SLOP[7:0]	7:0	Sub window B channel white slope.	
48h (102F90h)	**REG102F90**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_RGB_COMPRESS_SAT_THRD[7:0]	7:0	Main window RGB compress by saturation threshold: 10-bit precision.	
48h (102F91h)	**REG102F91**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_RGB_COMPRESS_START_SLOP[3:0]	7:4	Main window RGB compress by saturation start point slope.	
	-	3:2	Reserved.	
	MAIN_RGB_COMPRESS_SAT_THRD[9:8]	1:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_RGB_COMPRESS_SAT_THRD[7:0]	7:0	Sub window RGB compress by saturation threshold.	
49h (102F93h)	**REG102F93**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_RGB_COMPRESS_START_SLOP[3:0]	7:4	Sub window RGB compress by saturation start point slop.	
	-	3:2	Reserved.	
	SUB_RGB_COMPRESS_SAT_THRD[9:8]	1:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MAIN_RGB_COMPRESS_PRMCLR_MN_LIM_EN	2	Main window RGB compress by RGB primary color minimum value limit enable.	
	MAIN_RGB_COMPRESS_PRMCLR_MX_LIM_EN	1	Main window RGB compress by RGB primary color maximum value limit enable.	
	MAIN_RGB_COMPRESS_SEE_PRMCLR_EN	0	Main window RGB compress by RGB primary color enable.	
4Ah	**REG102F95**	**7:0**	**Default : 0x00**	**Access : R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	-	7:4	Reserved.	
	MAIN_RGB_COMPRESS_PRMCLR_START_SLOP[3:0]	3:0	Main window RGB compress by RGB primary color start point slope.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_RGB_COMPRESS_PRMCLR_THRD[7:0]	7:0	Main window RGB compress by RGB primary color threshold: 13-bit precision.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	MAIN_RGB_COMPRESS_PRMCLR_THRD[12:8]	4:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	SUB_RGB_COMPRESS_PRMCLR_MN_LIM_EN	2	Sub window RGB compress by RGB primary color minimum value limit enable.	
	SUB_RGB_COMPRESS_PRMCLR_MX_LIM_EN	1	Sub window RGB compress by RGB primary color maximum value limit enable.	
	SUB_RGB_COMPRESS_SEE_PRMCLR_EN	0	Sub window RGB compress by RGB primary color enable.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_RGB_COMPRESS_PRMCLR_START_SLOP[3:0]	3:0	Sub window RGB compress by RGB primary color start point slope.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_RGB_COMPRESS_PRMCLR_THRD[7:0]	7:0	Sub window RGB compress by RGB primary color threshold: 13-bit precision.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_RGB_COMPRESS_PRMCLR_THRD[12:8]	4:0	See description of '102F9Ah'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN0_X0[7:0]	7:0	OSD window0 x0 position.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN0_X0[11:8]	3:0	See description of '102FA0h'.	

XVYCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN0_X1[7:0]	7:0	OSD window0 x1 position.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN0_X1[11:8]	3:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN0_Y0[7:0]	7:0	OSD window0 y0 position.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN0_Y0[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN0_Y1[7:0]	7:0	OSD window0 y1 position.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN0_Y1[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN1_X0[7:0]	7:0	OSD window1 x0 position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN1_X0[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN1_X1[7:0]	7:0	OSD window1 x1 position.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN1_X1[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN1_Y0[7:0]	7:0	OSD window1 y0 position.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN1_Y0[11:8]	3:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN1_Y1[7:0]	7:0	OSD window1 y1 position.	

XVYCC Register (Bank = 102F, Sub-bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN1_Y1[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN2_X0[7:0]	7:0	OSD window2 x0 position.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN2_X0[11:8]	3:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN2_X1[7:0]	7:0	OSD window2 x1 position.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN2_X1[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN2_Y0[7:0]	7:0	OSD window2 y0 position.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN2_Y0[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN2_Y1[7:0]	7:0	OSD window2 y1 position.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN2_Y1[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN3_X0[7:0]	7:0	OSD window3 x0 position.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN3_X0[11:8]	3:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN3_X1[7:0]	7:0	OSD window3 x1 position.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	

XVYCC Register (Bank = 102F, Sub-bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	OSD_WIN3_X1[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN3_Y0[7:0]	7:0	OSD window3 y0 position.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN3_Y0[11:8]	3:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN3_Y1[7:0]	7:0	OSD window3 y1 position.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN3_Y1[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN4_X0[7:0]	7:0	OSD window4 x0 position.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN4_X0[11:8]	3:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN4_X1[7:0]	7:0	OSD window4 x1 position.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN4_X1[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN4_Y0[7:0]	7:0	OSD window4 y0 position.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN4_Y0[11:8]	3:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_WIN4_Y1[7:0]	7:0	OSD window4 y1 position.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_WIN4_Y1[11:8]	3:0	See description of '102FC6h'.	
64h	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**

XVYCC Register (Bank = 102F, Sub-bank = 25)

Index (Absolute)	Mnemonic	Bit	Description	
	LENGTH[7:0]	7:0	LVDS vbi tx data LENGTH.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LENGTH[9:8]	1:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	WAIT_CNT[7:0]	7:0	LVDS vbi tx wait cycle.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	TYPE[7:0]	7:0	LVDS vbi tx TYPE.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	TYPE[9:8]	1:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	HEADER_PW[7:0]	7:0	LVDS vbi header passwd.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	HEADER_PW[9:8]	1:0	See description of '102FCEh'.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	OSD_WIN_VALID[4:0]	4:0	OSD window valid bit.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBI_FIRE	7	LVDS vbi fire.	
	-	6:1	Reserved.	
	LVDS_VBI_EN	0	LVDS vbi tx enable.	

DMS Register (Bank = 102F, Sub-bank = 26)

DMS Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:6	Reserved.	
	DMS_CEN_MODE_VER_F2	5	Mosquito noise reduction center mode Vertical F2. 0: Original judge. 1: Advance judge.	
	DMS_CEN_MODE_HOR_F2	4	Mosquito noise reduction center mode Horizontal F2. 0: Original judge. 1: Advance judge.	
	-	3	Reserved.	
	DMS_VER_EN_F2	2	Mosquito noise reduction vertical enable F2.	
	DMS_ALPHA_LPF_EN_F2	1	Alpha low pass filter enable F2.	
	DMS_EN_F2	0	Mosquito noise reduction enable F2.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	DMS_LINE_8_EN	7	Mosquito noise reduction 8 line date input enable. (move to SRAM control) , BK20_10[4].	
	-	6:5	Reserved.	
	DMS_STRENGTH_F2[4:0]	4:0	Mosquito noise reduction strength F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_LOW_THRD_HOR_F2[7:0]	7:0	Horizontal std low threshold F2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:2	Reserved.	
	LUT_STEP_HOR_F2[1:0]	1:0	Horizontal look-up-table step F2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_LOW_THRD_CEN_HOR_F2[7:0]	7:0	Center std low threshold horizontal F2.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:3	Reserved.	
	LUT_STEP_CEN_HOR_F2[2:0]	2:0	Center look-up-table step horizontal F2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_LOW_THRD_CEN_VER_F2[7:0]	7:0	Center std low threshold vertical F2.	

DMS Register (Bank = 102F, Sub-bank = 26)

Index (Absolute)	Mnemonic	Bit	Description	
13h (102F27h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	DMS_EN_F1	0	Mosquito noise reduction enable F1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	STD_LOW_THRD_VER_F2[7:0]	7:0	Vertical std low threshold F2.	
18h (102F31h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SPIKE_NR_EN_F1	4	Spike NR Enable F1.	
	SPIKE_NR_MR_EN	3	Spike NR motion ratio enable.	
	-	2	Reserved.	
	V_C_LPF_EN_F2	1	Vertical C Low Pass Filter Enable F2.	
	SPIKE_NR_EN_F2	0	Spike NR Enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SPIKE_NR_COEF[3:0]	3:0	Spike NR Coefficient.	
51h (102FA2h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	P_THRD_1[4:0]	4:0	Spike NR P threshold 1.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_THRD_2[7:0]	7:0	Spike NR P threshold 2.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_THRD_3[7:0]	7:0	Spike NR P threshold 3.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	D_31_STEP[2:0]	6:4	Spike NR D31 Step.	
	-	3	Reserved.	

DMS Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	D_11_21_STEP[2:0]	2:0	Spike NR D11_21 Step.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	YP_22_STEP[2:0]	2:0	Spike NR YP22 Step.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	SPK_MR_LPF_EN_F2	0	Spike NR motion ratio low pass filter enable F2 (lpf is 3x3 mask).	
54h (102FA9h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x10**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_0[7:0]	7:0	Spike NR motion ratio look-up-table 0.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x32**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_1[7:0]	7:0	Spike NR motion ratio look-up-table 1.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x54**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_2[7:0]	7:0	Spike NR motion ratio look-up-table 2.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x76**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_3[7:0]	7:0	Spike NR motion ratio look-up-table 3.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x98**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_4[7:0]	7:0	Spike NR motion ratio look-up-table 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0xBA**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_5[7:0]	7:0	Spike NR motion ratio look-up-table 5.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0xDC**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_6[7:0]	7:0	Spike NR motion ratio look-up-table 6.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0xFE**	**Access : R/W**
	SPIKE_NR_MOTION_LUT_7[7:0]	7:0	Spike NR motion ratio look-up-table 7.	

ACE2 Register (Bank = 102F, Sub-bank = 27)

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_R_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0 for Red.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_R_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1 for Red.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_R_Y_2[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 2 for Red.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_R_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3 for Red.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_G_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0 for Green.	
12h (102F25h)	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_G_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1 for Green.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_G_Y_2[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 2 for Green.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_G_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3 for Green.	
14h (102F28h)	**REG102F28**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_B_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0 for Blue.	
14h (102F29h)	**REG102F29**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_B_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1 for Blue.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_B_Y_2[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 2 for Blue.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_B_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3 for Blue.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_C_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0 for Cyan.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_C_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1 for Cyan.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_C_Y_2[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 2 for Cyan.	
17h	**REG102F2F**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_IHC_ICC_C_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3 for Cyan.	
18h (102F30h)	**REG102F30**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_M_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0 for Magenta.	
18h (102F31h)	**REG102F31**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_M_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1 for Magenta.	
19h (102F32h)	**REG102F32**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_M_Y_2[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 2 for Magenta.	
19h (102F33h)	**REG102F33**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_M_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3 for Magenta.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_Y_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0 for Yellow.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_Y_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1 for Yellow.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_Y_Y_2[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 2 for Yellow.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_Y_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3 for Yellow.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_F_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0 for Flesh.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_F_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1 for Flesh.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_F_Y_2[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 2 for Flesh.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_F_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3 for Flesh.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_NC_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0 for Other.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_NC_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1 for Other.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_NC_Y_2[7:0	7:0	Sub window IHC, ICC adaptive Y in section 2 for Other.	

ACE2 Register (Bank = 102F, Sub-bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
	]			
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_NC_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3 for Other.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	SUB_CTI_EN	4	Sub window CTI enable.	
	-	3:1	Reserved.	
	MAIN_CTI_EN	0	Main window CTI enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CTI_STEP[1:0]	5:4	Main window CTI step.	
	-	3:0	Reserved.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	MAIN_CTI_CORING_THRD[3:0]	3:0	Main window CTI coring threshold.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	MAIN_CTI_BAND_COEF[5:0]	5:0	Main window CTI band pass filter coefficient.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CTI_STEP[1:0]	5:4	Sub window CTI step.	
	-	3:0	Reserved.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_CTI_CORING_THRD[3:0]	3:0	Sub window CTI coring threshold.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	SUB_CTI_BAND_COEF[5:0]	5:0	Sub window CTI band pass filter coefficient.	
25h	**REG102F4A**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:4	Reserved.	
	MAIN_CTI_GRAY_THRD[3:0]	3:0	Main window CTI gray patch threshold.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	SUB_CTI_GRAY_THRD[3:0]	3:0	Sub window CTI gray patch threshold.	
28h (102F50h)	**REG102F50**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_G_STRENGTH[3:0]	7:4	Main window color adaptive for peaking of G.	
	MAIN_R_STRENGTH[3:0]	3:0	Main window color adaptive for peaking of R.	
28h (102F51h)	**REG102F51**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_C_STRENGTH[3:0]	7:4	Main window color adaptive for peaking of C.	
	MAIN_B_STRENGTH[3:0]	3:0	Main window color adaptive for peaking of B.	
29h (102F52h)	**REG102F52**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_Y_STRENGTH[3:0]	7:4	Main window color adaptive for peaking of Y.	
	MAIN_M_STRENGTH[3:0]	3:0	Main window color adaptive for peaking of M.	
29h (102F53h)	**REG102F53**	**7:0**	**Default : 0x88**	**Access : R/W**
	MAIN_NC_STRENGTH[3:0]	7:4	Main window color adaptive for peaking of other color.	
	MAIN_F_STRENGTH[3:0]	3:0	Main window color adaptive for peaking of F.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_G_STRENGTH[3:0]	7:4	Sub window color adaptive for peaking of G.	
	SUB_R_STRENGTH[3:0]	3:0	Sub window color adaptive for peaking of R.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_C_STRENGTH[3:0]	7:4	Sub window color adaptive for peaking of C.	
	SUB_B_STRENGTH[3:0]	3:0	Sub window color adaptive for peaking of B.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_Y_STRENGTH[3:0]	7:4	Sub window color adaptive for peaking of Y.	
	SUB_M_STRENGTH[3:0]	3:0	Sub window color adaptive for peaking of M.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_NC_STRENGTH[3:0]	7:4	Sub window color adaptive for peaking of other color.	
	SUB_F_STRENGTH[3:0]	3:0	Sub window color adaptive for peaking of F.	
2Ch ~ 2Fh (102F58h ~	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_ICC_Y_MODE_EN	7	Main window ICC adaptive Y mode enable.	
	SUB_ICC_Y_MODE_EN	6	Sub window ICC adaptive Y mode enable.	
	-	5:2	Reserved.	
	MAIN_ICC_Y_MODE_DIFF_COLOR_EN	1	Main window ICC adaptive Y mode in different color enable.	
	SUB_ICC_Y_MODE_DIFF_COLOR_EN	0	Sub window ICC adaptive Y mode in different color enable.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_R_0[3:0]	7:4	Sub window ICC saturation adjustment of R in section 0.	
	MAIN_SA_USER_R_0[3:0]	3:0	Main window ICC saturation adjustment of R in section 0.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_G_0[3:0]	7:4	Sub window ICC saturation adjustment of G in section 0.	
	MAIN_SA_USER_G_0[3:0]	3:0	Main window ICC saturation adjustment of G in section 0.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_B_0[3:0]	7:4	Sub window ICC saturation adjustment of B in section 0.	
	MAIN_SA_USER_B_0[3:0]	3:0	Main window ICC saturation adjustment of B in section 0.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_C_0[3:0]	7:4	Sub window ICC saturation adjustment of C in section 0.	
	MAIN_SA_USER_C_0[3:0]	3:0	Main window ICC saturation adjustment of C in section 0.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_M_0[3:0]	7:4	Sub window ICC saturation adjustment of M in section 0.	
	MAIN_SA_USER_M_0[3:0]	3:0	Main window ICC saturation adjustment of M in section 0.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_Y_0[3:0]	7:4	Sub window ICC saturation adjustment of Y in section 0.	
	MAIN_SA_USER_Y_0[3:0]	3:0	Main window ICC saturation adjustment of Y in section 0.	
34h (102F68h)	**REG102F68**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_F_0[3:0]	7:4	Sub window ICC saturation adjustment of F in section 0.	
	MAIN_SA_USER_F_0[3:0]	3:0	Main window ICC saturation adjustment of F in section 0.	
34h (102F69h)	**REG102F69**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_SA_USER_NC_0[3:0]	7:4	Sub window ICC saturation adjustment of other color in section 0.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_SA_USER_NC_0[3:0]	3:0	Main window ICC saturation adjustment of other color in section 0.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER_0[7:0]	7:0	Main window ICC decrease saturation in section 0. [7]: Flesh. [6]: Yellow. [5]: Magenta. [4]: Cyan. [3]: Blue. [2]: Green. [1]: Red. [0]: Other.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SIGN_SA_USER_0[7:0]	7:0	Sub window ICC decrease saturation in section 0. [7]: Flesh. [6]: Yellow. [5]: Magenta. [4]: Cyan. [3]: Blue. [2]: Green. [1]: Red. [0]: Other.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_R_1[3:0]	7:4	Sub window ICC saturation adjustment of R in section 1.	
	MAIN_SA_USER_R_1[3:0]	3:0	Main window ICC saturation adjustment of R in section 1.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_G_1[3:0]	7:4	Sub window ICC saturation adjustment of G in section 1.	
	MAIN_SA_USER_G_1[3:0]	3:0	Main window ICC saturation adjustment of G in section 1.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_B_1[3:0]	7:4	Sub window ICC saturation adjustment of B in section 1.	
	MAIN_SA_USER_B_1[3:0]	3:0	Main window ICC saturation adjustment of B in section 1.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_C_1[3:0]	7:4	Sub window ICC saturation adjustment of C in section 1.	
	MAIN_SA_USER_C_1[3:0]	3:0	Main window ICC saturation adjustment of C in section 1.	
38h (102F70h)	**REG102F70**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_M_1[3:0]	7:4	Sub window ICC saturation adjustment of M in section 1.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_SA_USER_M_1[3:0]	3:0	Main window ICC saturation adjustment of M in section 1.	
38h (102F71h)	**REG102F71**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_Y_1[3:0]	7:4	Sub window ICC saturation adjustment of Y in section 1.	
	MAIN_SA_USER_Y_1[3:0]	3:0	Main window ICC saturation adjustment of Y in section 1.	
39h (102F72h)	**REG102F72**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_F_1[3:0]	7:4	Sub window ICC saturation adjustment of F in section 1.	
	MAIN_SA_USER_F_1[3:0]	3:0	Main window ICC saturation adjustment of F in section 1.	
39h (102F73h)	**REG102F73**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_SA_USER_NC_1[3:0]	7:4	Sub window ICC saturation adjustment of other color in section 1.	
	MAIN_SA_USER_NC_1[3:0]	3:0	Main window ICC saturation adjustment of other color in section 1.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER_1[7:0]	7:0	Main window ICC decrease saturation in section 1. [7]: Flesh. [6]: Yellow. [5]: Magenta. [4]: Cyan. [3]: Blue. [2]: Green. [1]: Red. [0]: Other.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SIGN_SA_USER_1[7:0]	7:0	Sub window ICC decrease saturation in section 1. [7]: Flesh. [6]: Yellow. [5]: Magenta. [4]: Cyan. [3]: Blue. [2]: Green. [1]: Red. [0]: Other.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_R_2[3:0]	7:4	Sub window ICC saturation adjustment of R in section 2.	
	MAIN_SA_USER_R_2[3:0]	3:0	Main window ICC saturation adjustment of R in section 2.	
3Bh	**REG102F77**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE2 Register (Bank = 102F, Sub-bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
	SUB_SA_USER_G_2[3:0]	7:4	Sub window ICC saturation adjustment of G in section 2.	
	MAIN_SA_USER_G_2[3:0]	3:0	Main window ICC saturation adjustment of G in section 2.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_B_2[3:0]	7:4	Sub window ICC saturation adjustment of B in section 2.	
	MAIN_SA_USER_B_2[3:0]	3:0	Main window ICC saturation adjustment of B in section 2.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_C_2[3:0]	7:4	Sub window ICC saturation adjustment of C in section 2.	
	MAIN_SA_USER_C_2[3:0]	3:0	Main window ICC saturation adjustment of C in section 2.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_M_2[3:0]	7:4	Sub window ICC saturation adjustment of M in section 2.	
	MAIN_SA_USER_M_2[3:0]	3:0	Main window ICC saturation adjustment of M in section 2.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_Y_2[3:0]	7:4	Sub window ICC saturation adjustment of Y in section 2.	
	MAIN_SA_USER_Y_2[3:0]	3:0	Main window ICC saturation adjustment of Y in section 2.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SA_USER_F_2[3:0]	7:4	Sub window ICC saturation adjustment of F in section 2.	
	MAIN_SA_USER_F_2[3:0]	3:0	Main window ICC saturation adjustment of F in section 2.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default : 0x88**	**Access : R/W**
	SUB_SA_USER_NC_2[3:0]	7:4	Sub window ICC saturation adjustment of other color in section 2.	
	MAIN_SA_USER_NC_2[3:0]	3:0	Main window ICC saturation adjustment of other color in section 2.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_SIGN_SA_USER_2[7:0]	7:0	Main window ICC decrease saturation in section 2. [7]: Flesh. [6]: Yellow. [5]: Magenta. [4]: Cyan. [3]: Blue. [2]: Green. [1]: Red. [0]: Other.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_SIGN_SA_USER_2[7:0]	7:0	Sub window ICC decrease saturation in section 2. [7]: Flesh.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[6]: Yellow. [5]: Magenta. [4]: Cyan. [3]: Blue. [2]: Green. [1]: Red. [0]: Other.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_R_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for Red.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_R_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for Red.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_R_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for Red.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_R_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for Red.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_G_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for Green.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_G_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for Green.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_G_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for Green.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_G_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for Green.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_B_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for Blue.	
54h	**REG102FA9**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_IHC_ICC_B_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for Blue.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_B_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for Blue.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_B_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for Blue.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_C_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for Cyan.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_C_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for Cyan.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_C_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for Cyan.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_C_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for Cyan.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_M_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for Magenta.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_M_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for Magenta.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_M_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for Magenta.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_M_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for Magenta.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for Yellow.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for Yellow.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for Yellow.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for Yellow.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_F_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for Flesh.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_F_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for Flesh.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_F_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for Flesh.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_F_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for Flesh.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_NC_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0 for Other.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_NC_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1 for Other.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_NC_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2 for Other.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_NC_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3 for Other.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_Y_MODE_EN	7	Main window IHC adaptive Y mode enable.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_IHC_Y_MODE_EN	6	Sub window IHC adaptive Y mode enable.	
	-	5:2	Reserved.	
	MAIN_IHC_Y_MODE_DIFF_COLOR_EN	1	Main window IHC adaptive Y mode in different color enable.	
	SUB_IHC_Y_MODE_DIFF_COLOR_EN	0	Sub window IHC adaptive Y mode in different color enable.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_0[7:0]	7:0	Main window IHC, ICC adaptive Y in section 0.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_1[7:0]	7:0	Main window IHC, ICC adaptive Y in section 1.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_2[7:0]	7:0	Main window IHC, ICC adaptive Y in section 2.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default : 0x00**	**Access : R/W**
	MAIN_IHC_ICC_Y_3[7:0]	7:0	Main window IHC, ICC adaptive Y in section 3.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R_0[6:0]	6:0	Main window IHC hue adjustment of R in section 0.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G_0[6:0]	6:0	Main window IHC hue adjustment of G in section 0.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B_0[6:0]	6:0	Main window IHC hue adjustment of B in section 0.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C_0[6:0]	6:0	Main window IHC hue adjustment of C in section 0.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M_0[6:0]	6:0	Main window IHC hue adjustment of M in section 0.	

ACE2 Register (Bank = 102F, Sub-bank = 27)

Index (Absolute)	Mnemonic	Bit	Description	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y_0[6:0]	6:0	Main window IHC hue adjustment of Y in section 0.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F_0[6:0]	6:0	Main window IHC hue adjustment of F in section 0.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R_1[6:0]	6:0	Main window IHC hue adjustment of R in section 1.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G_1[6:0]	6:0	Main window IHC hue adjustment of G in section 1.	
68h (102FD0h)	**REG102FD0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B_1[6:0]	6:0	Main window IHC hue adjustment of B in section 1.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C_1[6:0]	6:0	Main window IHC hue adjustment of C in section 1.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M_1[6:0]	6:0	Main window IHC hue adjustment of M in section 1.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y_1[6:0]	6:0	Main window IHC hue adjustment of Y in section 1.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F_1[6:0]	6:0	Main window IHC hue adjustment of F in section 1.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Bh (102FD6h)	**REG102FD6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R_2[6:0]	6:0	Main window IHC hue adjustment of R in section 2.	
6Bh (102FD7h)	**REG102FD7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G_2[6:0]	6:0	Main window IHC hue adjustment of G in section 2.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B_2[6:0]	6:0	Main window IHC hue adjustment of B in section 2.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C_2[6:0]	6:0	Main window IHC hue adjustment of C in section 2.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M_2[6:0]	6:0	Main window IHC hue adjustment of M in section 2.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y_2[6:0]	6:0	Main window IHC hue adjustment of Y in section 2.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F_2[6:0]	6:0	Main window IHC hue adjustment of F in section 2.	
6Fh ~ 6Fh (102FDEh ~ 102FDFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	VIP_FUN_BYPASS_EN	0	VIP all function bypass enable.	
71h	**REG102FE2**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_IHC_ICC_Y_0[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 0.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_Y_1[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 1.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_Y_2[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 2.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default : 0x00**	**Access : R/W**
	SUB_IHC_ICC_Y_3[7:0]	7:0	Sub window IHC, ICC adaptive Y in section 3.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_R_0[6:0]	6:0	Sub window IHC hue adjustment of R in section 0.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_G_0[6:0]	6:0	Sub window IHC hue adjustment of G in section 0.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_B_0[6:0]	6:0	Sub window IHC hue adjustment of B in section 0.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_C_0[6:0]	6:0	Sub window IHC hue adjustment of C in section 0.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_M_0[6:0]	6:0	Sub window IHC hue adjustment of M in section 0.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_Y_0[6:0]	6:0	Sub window IHC hue adjustment of Y in section 0.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_F_0[6:0]	6:0	Sub window IHC hue adjustment of F in section 0.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_R_1[6:0]	6:0	Sub window IHC hue adjustment of R in section 1.	
77h	**REG102FEF**	**7:0**	**Default : 0x00**	**Access : R/W**

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7	Reserved.	
	SUB_HUE_USER_G_1[6:0]	6:0	Sub window IHC hue adjustment of G in section 1.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_B_1[6:0]	6:0	Sub window IHC hue adjustment of B in section 1.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_C_1[6:0]	6:0	Sub window IHC hue adjustment of C in section 1.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_M_1[6:0]	6:0	Sub window IHC hue adjustment of M in section 1.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_Y_1[6:0]	6:0	Sub window IHC hue adjustment of Y in section 1.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_F_1[6:0]	6:0	Sub window IHC hue adjustment of F in section 1.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_R_2[6:0]	6:0	Sub window IHC hue adjustment of R in section 2.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_G_2[6:0]	6:0	Sub window IHC hue adjustment of G in section 2.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_B_2[6:0]	6:0	Sub window IHC hue adjustment of B in section 2.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_C_2[6:0]	6:0	Sub window IHC hue adjustment of C in section 2.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_M_2[6:0]	6:0	Sub window IHC hue adjustment of M in section 2.	

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_Y_2[6:0]	6:0	Sub window IHC hue adjustment of Y in section 2.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	SUB_HUE_USER_F_2[6:0]	6:0	Sub window IHC hue adjustment of F in section 2.	

NR Register (Bank = 102F, Sub-bank = 2A)

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h ~ 06h (102F04h ~ 102F0Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default : 0x00**	**Access : R/W**
	MED_AUTO	7	Median auto.	
	MED_EN	6	Median enable.	
	SNR_EN_F2	5	SNR enable.	
	PATCH_W4_EN	4	Patch w4 enable.	
	PATCH_W3_EN	3	Patch w3 enable.	
	PATCH_W2_EN	2	Patch w2 enable.	
	UCE_FILM_EN	1	Film act use UltraClear Engine data.	
	MCNR_EN_F2	0	MCNR enable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default : 0x00**	**Access : R/W**
	NR_EN_F2	7	NR enable.	
	PDNR_EN_F2	6	PDNR enable.	
	RANDOM_MOTION_CHECK_DIFF	5	Random motion check diff enable.	
	RANDOM_MOTION_EN	4	Random motion enable.	
	DITHER_EN	3	Dither enable.	
	KEEP_DETAIL_EN	2	Keep detail enable.	
	FAVOR_MV0_EN	1	Favor mv0 enable.	
	C_PDNR_EN_F2	0	PDNR c enable.	
08h (102F10h)	**REG102F10**	**7:0**	**Default : 0xEE**	**Access : R/W**
	NR_LUT_2[7:4]	7:4	NR look up table 2.	
	NR_LUT_3[3:0]	3:0	NR look up table 3.	
08h (102F11h)	**REG102F11**	**7:0**	**Default : 0xFF**	**Access : R/W**
	NR_LUT_0[15:12]	7:4	NR look up table 0.	
	NR_LUT_1[11:8]	3:0	NR look up table 1.	
09h (102F12h)	**REG102F12**	**7:0**	**Default : 0xCC**	**Access : R/W**
	NR_LUT_6[7:4]	7:4	NR look up table 6.	
	NR_LUT_7[3:0]	3:0	NR look up table 7.	
09h	**REG102F13**	**7:0**	**Default : 0xDD**	**Access : R/W**

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NR_LUT_4[15:12]	7:4	NR look up table 4.	
	NR_LUT_5[11:8]	3:0	NR look up table 5.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default : 0xAA**	**Access : R/W**
	NR_LUT_10[7:4]	7:4	NR look up table 10.	
	NR_LUT_11[3:0]	3:0	NR look up table 11.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default : 0xBB**	**Access : R/W**
	NR_LUT_8[15:12]	7:4	NR look up table 8.	
	NR_LUT_9[11:8]	3:0	NR look up table 9.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default : 0x88**	**Access : R/W**
	NR_LUT_14[7:4]	7:4	NR look up table 14.	
	NR_LUT_15[3:0]	3:0	NR look up table 15.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default : 0x99**	**Access : R/W**
	NR_LUT_12[15:12]	7:4	NR look up table 12.	
	NR_LUT_13[11:8]	3:0	NR look up table 13.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default : 0x66**	**Access : R/W**
	NR_LUT_18[7:4]	7:4	NR look up table 18.	
	NR_LUT_19[3:0]	3:0	NR look up table 19.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default : 0x77**	**Access : R/W**
	NR_LUT_16[15:12]	7:4	NR look up table 16.	
	NR_LUT_17[11:8]	3:0	NR look up table 17.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x44**	**Access : R/W**
	NR_LUT_22[7:4]	7:4	NR look up table 22.	
	NR_LUT_23[3:0]	3:0	NR look up table 23.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x55**	**Access : R/W**
	NR_LUT_20[15:12]	7:4	NR look up table 20.	
	NR_LUT_21[11:8]	3:0	NR look up table 21.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x22**	**Access : R/W**
	NR_LUT_26[7:4]	7:4	NR look up table 26.	
	NR_LUT_27[3:0]	3:0	NR look up table 27.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x33**	**Access : R/W**
	NR_LUT_24[15:12]	7:4	NR look up table 24.	
	NR_LUT_25[11:8]	3:0	NR look up table 25.	

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	NR_LUT_30[7:4]	7:4	NR look up table 30.	
	NR_LUT_31[3:0]	3:0	NR look up table 31.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x11**	**Access : R/W**
	NR_LUT_28[15:12]	7:4	NR look up table 28.	
	NR_LUT_29[11:8]	3:0	NR look up table 29.	
10h ~ 1Fh (102F20h ~ 102F3Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h (102F40h)	**REG102F40**	**7:0**	**Default : 0x88**	**Access : R/W**
	PDNR_LOW_LUT_2[7:4]	7:4	PDNR low look up table 2.	
	PDNR_LOW_LUT_3[3:0]	3:0	PDNR low look up table 3.	
20h (102F41h)	**REG102F41**	**7:0**	**Default : 0x88**	**Access : R/W**
	PDNR_LOW_LUT_0[15:12]	7:4	PDNR low look up table 0.	
	PDNR_LOW_LUT_1[11:8]	3:0	PDNR low look up table 1.	
21h (102F42h)	**REG102F42**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_6[7:4]	7:4	PDNR low look up table 6.	
	PDNR_LOW_LUT_7[3:0]	3:0	PDNR low look up table 7.	
21h (102F43h)	**REG102F43**	**7:0**	**Default : 0x51**	**Access : R/W**
	PDNR_LOW_LUT_4[15:12]	7:4	PDNR low look up table 4.	
	PDNR_LOW_LUT_5[11:8]	3:0	PDNR low look up table 5.	
22h (102F44h)	**REG102F44**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_10[7:4]	7:4	PDNR low look up table 10.	
	PDNR_LOW_LUT_11[3:0]	3:0	PDNR low look up table 11.	
22h (102F45h)	**REG102F45**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_8[15:12]	7:4	PDNR low look up table 8.	
	PDNR_LOW_LUT_9[11:8]	3:0	PDNR low look up table 9.	
23h (102F46h)	**REG102F46**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_14[7:4]	7:4	PDNR low look up table 14.	
	PDNR_LOW_LUT_15[3:0]	3:0	PDNR low look up table 15.	
23h (102F47h)	**REG102F47**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_LOW_LUT_12[15:12]	7:4	PDNR low look up table 12.	

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PDNR_LOW_LUT_13[11:8]	3:0	PDNR low look up table 13.	
24h (102F48h)	**REG102F48**	**7:0**	**Default : 0xDC**	**Access : R/W**
	PDNR_HIGH_LUT_2[7:4]	7:4	PDNR high look up table 2.	
	PDNR_HIGH_LUT_3[3:0]	3:0	PDNR high look up table 3.	
24h (102F49h)	**REG102F49**	**7:0**	**Default : 0xFE**	**Access : R/W**
	PDNR_HIGH_LUT_0[15:12]	7:4	PDNR high look up table 0.	
	PDNR_HIGH_LUT_1[11:8]	3:0	PDNR high look up table 1.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default : 0x98**	**Access : R/W**
	PDNR_HIGH_LUT_6[7:4]	7:4	PDNR high look up table 6.	
	PDNR_HIGH_LUT_7[3:0]	3:0	PDNR high look up table 7.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default : 0xBA**	**Access : R/W**
	PDNR_HIGH_LUT_4[15:12]	7:4	PDNR high look up table 4.	
	PDNR_HIGH_LUT_5[11:8]	3:0	PDNR high look up table 5.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default : 0x54**	**Access : R/W**
	PDNR_HIGH_LUT_10[7:4]	7:4	PDNR high look up table 10.	
	PDNR_HIGH_LUT_11[3:0]	3:0	PDNR high look up table 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default : 0x76**	**Access : R/W**
	PDNR_HIGH_LUT_8[15:12]	7:4	PDNR high look up table 8.	
	PDNR_HIGH_LUT_9[11:8]	3:0	PDNR high look up table 9.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default : 0x10**	**Access : R/W**
	PDNR_HIGH_LUT_14[7:4]	7:4	PDNR high look up table 14.	
	PDNR_HIGH_LUT_15[3:0]	3:0	PDNR high look up table 15.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default : 0x32**	**Access : R/W**
	PDNR_HIGH_LUT_12[15:12]	7:4	PDNR high look up table 12.	
	PDNR_HIGH_LUT_13[11:8]	3:0	PDNR high look up table 13.	
28h ~ 2Fh (102F50h ~ 102F5Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default : 0x88**	**Access : R/W**
	PDNR_C_LUT_2[7:4]	7:4	PDNR c look up table 2.	
	PDNR_C_LUT_3[3:0]	3:0	PDNR c look up table 3.	
30h	**REG102F61**	**7:0**	**Default : 0x88**	**Access : R/W**

NR Register (Bank = 102F, Sub-bank = 2A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PDNR_C_LUT_0[15:12]	7:4	PDNR c look up table 0.	
	PDNR_C_LUT_1[11:8]	3:0	PDNR c look up table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_6[7:4]	7:4	PDNR c look up table 6.	
	PDNR_C_LUT_7[3:0]	3:0	PDNR c look up table 7.	
31h (102F63h)	**REG102F63**	**7:0**	**Default : 0x51**	**Access : R/W**
	PDNR_C_LUT_4[15:12]	7:4	PDNR c look up table 4.	
	PDNR_C_LUT_5[11:8]	3:0	PDNR c look up table 5.	
32h (102F64h)	**REG102F64**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_10[7:4]	7:4	PDNR c look up table 10.	
	PDNR_C_LUT_11[3:0]	3:0	PDNR c look up table 11.	
32h (102F65h)	**REG102F65**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_8[15:12]	7:4	PDNR c look up table 8.	
	PDNR_C_LUT_9[11:8]	3:0	PDNR c look up table 9.	
33h (102F66h)	**REG102F66**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_14[7:4]	7:4	PDNR c look up table 14.	
	PDNR_C_LUT_15[3:0]	3:0	PDNR c look up table 15.	
33h (102F67h)	**REG102F67**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDNR_C_LUT_12[15:12]	7:4	PDNR c look up table 12.	
	PDNR_C_LUT_13[11:8]	3:0	PDNR c look up table 13.	
34h ~ 7Fh (102F68h ~ 102FFFh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

VOP2_RP Register (Bank = 102F, Sub-bank = 2D)

VOP2_RP Register (Bank = 102F, Sub-bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 0Ch (102F02h ~ 102F18h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default : 0x00**	**Access : R/W**
	R_TH[7:0]	7:0	R channel threshold for pixel count.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	R_TH[9:8]	1:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default : 0x00**	**Access : R/W**
	G_TH[7:0]	7:0	G channel threshold for pixel count.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	G_TH[9:8]	1:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default : 0x00**	**Access : R/W**
	B_TH[7:0]	7:0	B channel threshold for pixel count.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	B_TH[9:8]	1:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_ST[7:0]	7:0	For OSD reference HS start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_NEW_REF	7	OSD new reference HS/VFDE enable.	
	-	6:4	Reserved.	
	OSD_HS_ST[11:8]	3:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_HS_END[7:0]	7:0	For OSD reference HS end.	
11h (102F23h)	**REG102F23**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	OSD_HS_END[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_ST[7:0]	7:0	For OSD reference VFDE start.	
12h	**REG102F25**	**7:0**	**Default : 0x00**	**Access : R/W**

VOP2_RP Register (Bank = 102F, Sub-bank = 2D)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	7:3	Reserved.	
	OSD_VFDE_ST[10:8]	2:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default : 0x00**	**Access : R/W**
	OSD_VFDE_END[7:0]	7:0	For OSD reference VFDE end.	
13h (102F27h)	**REG102F27**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	OSD_VFDE_END[10:8]	2:0	See description of '102F26h'.	

Scaler2 Register (Bank = 1030)

DISP_TC Register (Bank = 1030, Sub-bank = 00)

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (103006h)	**REG103006**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	TCON	2	TCON enable. (TCON = bounding & TCON).	
	-	1:0	Reserved.	
03h (103007h)	**REG103007**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	TC_CNT_EN	6	Enable TCON_CNT.	
	SEP_PUA	5	Enable separate PUA. 0: All GPO will be controlled by PUA. 1: Each GPO's PUA is controlled by itself PUA.	
	-	4:0	Reserved.	
04h (103008h)	**REG103008**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H1END_ODD[7:0]	7:0	The odd line HEND of GPO1 for Special Over Mode / 2nd horizontal end of GPO1.	
04h (103009h)	**REG103009**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7	Reserved.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OVER_MODE_1	6	Special over mode enable of GPO1. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H1END_ODD.	
	HEAD_PROC_EN_1	5	Head process enable of GPO1.	
	HEAD_MODE_1	4	Head mode enable of GPO1.	
	TC_H1END_ODD[11:8]	3:0	See description of '103008h'.	
05h (10300Ah)	**REG10300A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H2END_ODD[7:0]	7:0	The odd line HEND of GPO2 for Special Over Mode / 2nd horizontal end of GPO2.	
05h (10300Bh)	**REG10300B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7	Reserved.	
	OVER_MODE_2	6	Special over mode enable of GPO2. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H2END_ODD.	
	HEAD_PROC_EN_2	5	Head process enable of GPO2.	
	HEAD_MODE_2	4	Head mode enable of GPO2.	
	TC_H2END_ODD[11:8]	3:0	See description of '10300Ah'.	
0Dh (10301Ah)	**REG10301A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_V0ST[7:0]	7:0	Vertical start of GPO0.	
0Dh (10301Bh)	**REG10301B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	FRAME_TOG0_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO0.	
	TC_V0ST[11:8]	3:0	See description of '10301Ah'.	
0Eh (10301Ch)	**REG10301C**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_V0END[7:0]	7:0	Vertical end of GPO0.	
0Eh (10301Dh)	**REG10301D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	FRAME_TOG0_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO0. (if set 2, means 3 frame toggle once).	
	TC_V0END[11:8]	3:0	See description of '10301Ch'.	
0Fh (10301Eh)	**REG10301E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H0ST[7:0]	7:0	Horizontal start of GPO0.	
0Fh (10301Fh)	**REG10301F**	**7:0**	**Default : 0x0F**	**Access : R/W**
	LINE_TOG0_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO0.	
	TC_H0ST[11:8]	3:0	See description of '10301Eh'.	
10h	**REG103020**	**7:0**	**Default : 0xFF**	**Access : R/W**

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_H0END[7:0]	7:0	Horizontal end of GPO0.	
10h (103021h)	**REG103021**	**7:0**	**Default : 0x0F**	**Access : R/W**
	LINE_TOG0_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO0. (if set 2, means 3 line toggle once).	
	TC_H0END[11:8]	3:0	See description of '103020h'.	
11h (103022h)	**REG103022**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_V1ST[7:0]	7:0	Vertical start of GPO1.	
11h (103023h)	**REG103023**	**7:0**	**Default : 0x0F**	**Access : R/W**
	FRAME_TOG1_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO1.	
	TC_V1ST[11:8]	3:0	See description of '103022h'.	
12h (103024h)	**REG103024**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_V1END[7:0]	7:0	Vertical end of GPO1.	
12h (103025h)	**REG103025**	**7:0**	**Default : 0x0F**	**Access : R/W**
	FRAME_TOG1_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO1. (if set 2, means 3 frame toggle once).	
	TC_V1END[11:8]	3:0	See description of '103024h'.	
13h (103026h)	**REG103026**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H1ST[7:0]	7:0	Horizontal start of GPO1.	
13h (103027h)	**REG103027**	**7:0**	**Default : 0x0F**	**Access : R/W**
	LINE_TOG1_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO1.	
	TC_H1ST[11:8]	3:0	See description of '103026h'.	
14h (103028h)	**REG103028**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H1END[7:0]	7:0	Horizontal end of GPO1.	
14h (103029h)	**REG103029**	**7:0**	**Default : 0x0F**	**Access : R/W**
	LINE_TOG1_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO1. (if set 2, means 3 line toggle once).	
	TC_H1END[11:8]	3:0	See description of '103028h'.	
15h (10302Ah)	**REG10302A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_V2ST[7:0]	7:0	Vertical start of GPO2.	
15h (10302Bh)	**REG10302B**	**7:0**	**Default : 0x0F**	**Access : R/W**
	FRAME_TOG2_H4[3:0]	7:4	Frame tog number MSB 4 bit of GPO2.	
	TC_V2ST[11:8]	3:0	See description of '10302Ah'.	
16h	**REG10302C**	**7:0**	**Default : 0xFF**	**Access : R/W**

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_V2END[7:0]	7:0	Vertical end of GPO2.	
16h (10302Dh)	**REG10302D**	**7:0**	**Default : 0x0F**	**Access : R/W**
	FRAME_TOG2_L4[3:0]	7:4	Frame tog number LSB 4 bit of GPO2. (if set 2, means 3 frame toggle once).	
	TC_V2END[11:8]	3:0	See description of '10302Ch'.	
17h (10302Eh)	**REG10302E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H2ST[7:0]	7:0	Horizontal start of GPO2.	
17h (10302Fh)	**REG10302F**	**7:0**	**Default : 0x0F**	**Access : R/W**
	LINE_TOG2_H4[3:0]	7:4	Line tog number MSB 4 bit of GPO2.	
	TC_H2ST[11:8]	3:0	See description of '10302Eh'.	
18h (103030h)	**REG103030**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H2END[7:0]	7:0	Horizontal end of GPO2.	
18h (103031h)	**REG103031**	**7:0**	**Default : 0x0F**	**Access : R/W**
	LINE_TOG2_L4[3:0]	7:4	Line tog number LSB 4 bit of GPO2. (if set 2, means 3 line toggle once).	
	TC_H2END[11:8]	3:0	See description of '103030h'.	
39h (103072h)	**REG103072**	**7:0**	**Default : 0x00**	**Access : R/W**
	G0OP	7	GPO0 Output Polarity. 0: Active high. 1: Active low.	
	G0TC	6	GPO0 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.	
	G0ES	5	GPO0 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	G0TS[1:0]	4:3	GPO0 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.
	G0CS[2:0]	2:0	GPO0 Combination Select. 000: No combination. 001: AND (GPO# & GPO#-1). 010: OR (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR (GPO# ^ GPO#-1).
39h (103073h)	**REG103073**	**7:0**	**Default : 0x00** **Access : R/W**
	G1OP	7	GPO1 Output Polarity. 0: Active high. 1: Active low.
	G1TC	6	GPO1 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.
	G1ES	5	GPO1 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	G1TS[1:0]	4:3	GPO1 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G1CS[2:0]	2:0	GPO1 Combination Select. 000: No combination. 001: AND (GPO# & GPO#-1). 010: OR (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR (GPO# ^ GPO#-1).	
3Ah (103074h)	**REG103074**	**7:0**	**Default : 0x00**	**Access : R/W**
	G2OP	7	GPO2 Output Polarity. 0: Active high. 1: Active low.	
	G2TC	6	GPO2 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd # in the vertical duration when in toggle mode.	
	G2ES	5	GPO2 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	G2TS[1:0]	4:3	GPO2 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G2CS[2:0]	2:0	GPO2 Combination Select. 000: No combination. 001: AND (GPO# & GPO#-1). 010: OR (GPO# | GPO#-1). 011: Select GPO# and GPO#-1 on alternating frames. 1xx: XOR (GPO# ^ GPO#-1).	
3Fh (10307Eh)	**REG10307E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	GPO2_EN	4	GPO2 enable of POL.	
	GPO1_EN	3	GPO1 enable of POL.	
	GPO0_EN	2	GPO0 enable of POL.	
	-	1:0	Reserved.	
4Ch (103098h)	**REG103098**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H1ST2[7:0]	7:0	2nd horizontal start of GPO1.	
4Ch (103099h)	**REG103099**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPO0_PS[3:0]	7:4	Frame count for power sequence of gpo0. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H1ST2[11:8]	3:0	See description of '103098h'.	
4Dh (10309Ah)	**REG10309A**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H1ST3[7:0]	7:0	3rd horizontal start of GPO1.	
4Dh (10309Bh)	**REG10309B**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPO1_PS[3:0]	7:4	Frame count for power sequence of gpo1. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H1ST3[11:8]	3:0	See description of '10309Ah'.	
4Eh	**REG10309C**	**7:0**	**Default : 0xFF**	**Access : R/W**

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_H1END3[7:0]	7:0	3rd horizontal end of GPO1.	
4Eh (10309Dh)	**REG10309D**	**7:0**	**Default : 0xFF**	**Access : R/W**
	GPO2_PS[3:0]	7:4	Frame count for power sequence of gpo2. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H1END3[11:8]	3:0	See description of '10309Ch'.	
4Fh (10309Eh)	**REG10309E**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H2ST2[7:0]	7:0	2nd horizontal start of GPO2.	
4Fh (10309Fh)	**REG10309F**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H2ST2[11:8]	3:0	See description of '10309Eh'.	
50h (1030A0h)	**REG1030A0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H2ST3[7:0]	7:0	3rd horizontal start of GPO2.	
50h (1030A1h)	**REG1030A1**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H2ST3[11:8]	3:0	See description of '1030A0h'.	
51h (1030A2h)	**REG1030A2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	TC_H2END3[7:0]	7:0	3rd horizontal end of GPO2.	
51h (1030A3h)	**REG1030A3**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	TC_H2END3[11:8]	3:0	See description of '1030A2h'.	
61h (1030C2h)	**REG1030C2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GPO2_FF_OEN	2	GPO2_FF output enable.	
	GPO1_FF_OEN	1	GPO1_FF output enable.	
	GPO0_FF_OEN	0	GPO0_FF output enable.	
6Eh (1030DCh)	**REG1030DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GPO2_N_1_SEL	2	Select the signal which is used for GPO2 Combination Select (G2CS). (GPO2 n 1 select). 0: Use GPO1. 1: Use an always Low signal(1'b0).	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPO1_N_1_SEL	1	Select the signal which is used for GPO1 Combination Select (G1CS). (GPO1 n 1 select). 0: Use GPO0. 1: Use an always Low signal(1'b0).	
	GPO0_N_1_SEL	0	Select the signal which is used for GPO0 Combination Select (G0CS). (GPO0 n 1 select). 0: Use GPOD. 1: Use an always Low signal(1'b0).	
6Fh (1030DEh)	**REG1030DE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GPO2_EN_3HV[1:0]	5:4	GPO2 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO1_EN_3HV[1:0]	3:2	GPO1 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO0_EN_3HV[1:0]	1:0	GPO0 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
71h (1030E2h)	**REG1030E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	FRAME_TOG2_MD	2	GPO2 frame toggle mode enable.	
	FRAME_TOG1_MD	1	GPO1 frame toggle mode enable.	
	FRAME_TOG0_MD	0	GPO0 frame toggle mode enable.	
72h (1030E4h)	**REG1030E4**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	LINE_TOG2_MD	2	GPO2 line toggle mode enable.	
	LINE_TOG1_MD	1	GPO1 line toggle mode enable.	
	LINE_TOG0_MD	0	GPO0 line toggle mode enable.	
73h (1030E6h)	**REG1030E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FIRST_2H2_MD	2	GPO2 first 2H mode enable. (a n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H1_MD	1	GPO1 first 2H mode enable. (a n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H0_MD	0	GPO0 first 2H mode enable. (a n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
74h (1030E8h)	**REG1030E8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	GPO2_PUA	2	GPO2 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO1_PUA	1	GPO1 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO0_PUA	0	GPO0 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
76h (1030ECh)	**REG1030EC**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GPO2_STH_SEL[1:0]	5:4	Gpo2 sth pulse width select.	
	GPO1_STH_SEL[1:0]	3:2	Gpo1 sth pulse width select.	
	GPO0_STH_SEL[1:0]	1:0	Gpo0 sth pulse width select. 00: 1T positive clock sample (GPO_POS). 01: 1T negative clock sample (GPO_NEG). 10: 1.5T positive clock sample (GPO_POS | GPO_NEG). 11: 1.5T negative clock sample (GPO_NEG | GPO_2ND).	
78h (1030F0h)	**REG1030F0**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPO2_TAIL_MINUS1_MD	2	GPO2 tail minus 1H mode enable. (a n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO1_TAIL_MINUS1_MD	1	GPO1 tail minus 1H mode enable. (a n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO0_TAIL_MINUS1_MD	0	GPO0 tail minus 1H mode enable. (a n-Line toggle TCON signal need (n-1)-line toggle at last line).	
79h (1030F2h)	**REG1030F2**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	G2AT	2	GPO2 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G1AT	1	GPO1 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G0AT	0	GPO0 Auto Toggle for POL. 0: Disable. 1: Enable.	
7Fh (1030FEh)	**REG1030FE**	**7:0**	**Default : 0x00**	**Access : R/W**
	TC_DUMMY0[7:0]	7:0	TCON dummy register 0. Bit[0]:Enable or disable POL 2 line special mode. Odd frame is 2H mode, and even frame is normal mode. 0: Disable. 1: Enable. Bit[1]:Enable or disable POL frame toggle mode. 0: Disable. 1: Enable.	
7Fh (1030FFh)	**REG1030FF**	**7:0**	**Default : 0x00**	**Access : R/W**
	TC_DUMMY0[15:8]	7:0	See description of '1030FEh'.	

DISP_TC Register (Bank = 1030, Sub-bank = 01)

DISP_TC Register (Bank = 1030, Sub-bank = 01)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**

DISP_TC Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Eh (10301Dh)	**REG10301D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RDY_FCNT[3:0]	7:4	Ready frame counter for display.	
	-	3:0	Reserved.	
0Fh (10301Fh)	**REG10301F**	**7:0**	**Default : 0x08**	**Access : R/W**
	-	7:4	Reserved.	
	NO_SIGNAL_EN	3	Enable no-signal SRAM mask.	
	-	2:0	Reserved.	
11h (103022h)	**REG103022**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	EN_FCNT	2	Enable frame counter.	
	VCNT_RESET_SEL	1	TCON V counter reset by. 0: VOP2_VS. 1: TCON_TGEN_VS.	
	HCNT_RESET_SEL	0	TCON h counter reset by. 0: VOP2_HS. 1: TCON_TGEN_HS.	
20h (103040h)	**REG103040**	**7:0**	**Default : 0x00**	**Access : R/W**
	VCNT_DELAY[7:0]	7:0	Delay for timing adjust in h-reset. (Unit: ODCLK).	
20h (103041h)	**REG103041**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	VCNT_DELAY[11:8]	3:0	See description of '103040h'.	
21h (103042h)	**REG103042**	**7:0**	**Default : 0x00**	**Access : R/W**
	HCNT_DELAY[7:0]	7:0	Delay for timing adjust in h-reset.	
21h (103043h)	**REG103043**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	HCNT_DELAY[11:8]	3:0	See description of '103042h'.	
29h (103052h)	**REG103052**	**7:0**	**Default : 0x00**	**Access : R/W**
	INSERT_DUMMY_PT[7:0]	7:0	Single pixel insert point.	
29h (103053h)	**REG103053**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_DUMMY_INSERT	7	Enable dummy pixel insert.	
	-	6	Reserved.	
	EN_DUMMY_MUX[1:0]	5:4	Enable dummy pixel number.	

DISP_TC Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INSERT_DUMMY_PT[11:8]	3:0	See description of '103052h'.	
40h (103080h)	**REG103080**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPO2_HEAD_PLUS[1:0]	3:2	Add more line toggle mode at head of GPO2.	
	GPO1_HEAD_PLUS[1:0]	1:0	Add more line toggle mode at head of GPO1.	
42h (103084h)	**REG103084**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GPO2_TAIL_PLUS[1:0]	3:2	Add more line toggle mode at tail of GPO2.	
	GPO1_TAIL_PLUS[1:0]	1:0	Add more line toggle mode at tail of GPO1.	
44h (103088h)	**REG103088**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	GPO2_ONLY_HEAD_TAIL	1	Only head and tail line toggle part of GPO2.	
	GPO1_ONLY_HEAD_TAIL	0	Only head and tail line toggle part of GPO1.	
45h ~ 46h (10308Ah ~ 10308Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

Scaler3 Register (Bank = 1031)

LPLL Register (Bank = 1031)

LPLL Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (103100h)	**REG103100**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control: 00: /1. 01: /2. 10: /4. 11: /8.	
00h (103101h)	**REG103101**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N); 0: Divide 1. 1: Divide 1. 2: Divide 2.	

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
			3: Divide 3. 4: Divide 4.	
01h (103102h)	**REG103102**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control: 00: /1. 01: /2. 10: /4. 11: /8.	
01h (103103h)	**REG103103**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio=(1/N); Default ratio=8; 0: Divide 1. 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4.	
02h (103104h)	**REG103104**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL1_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
02h (103105h)	**REG103105**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_OUTPUT_DIV_SECOND[7:0]	7:0	Output divider.	
03h (103106h)	**REG103106**	**7:0**	**Default : 0x23**	**Access : R/W**
	LPLL1_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL1_2CHIP_SYN_EN	6		
	LPLL1_PD	5	Power down control to PLL (active high).	
	LPLL1_EN_HFLVDS	4		
	LPLL1_IBIAS_ICTRL[1:0]	3:2		
	LPLL1_ICP_ICTRL[1:0]	1:0	LPLL current control.	
03h (103107h)	**REG103107**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LPLL1_HIGH_FLAG	7		
	LPLL1_LOCK	6		

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	-	5	Reserved.	
	LPLL1_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL1_EN_SKEW_DIVIDER	1		
	LPLL1_ENFRUN	0		
04h (103108h)	**REG103108**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL1_SKEW_CLKP_PHASE_SEL[4:0]	4:0		
04h (103109h)	**REG103109**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL1_SKEW_CLKM_PHASE_SEL[4:0]	4:0		
05h (10310Ah)	**REG10310A**	**7:0**	**Default : 0x22**	**Access : R/W**
	PRD_LOCK_THRESH[3:0]	7:4	PRD lock thresh.	
	PRD_STABLE_THRESH[3:0]	3:0	Clock stable thresh.	
05h (10310Bh)	**REG10310B**	**7:0**	**Default : 0x02**	**Access : R/W**
	PHASE_LOCK_THRESH[7:0]	7:0	Phase lock thresh.	
06h (10310Ch)	**REG10310C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[7:0]	7:0	Limit for clock freq correction modification.	
06h (10310Dh)	**REG10310D**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[15:8]	7:0	See description of '10310Ch'.	
07h (10310Eh)	**REG10310E**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7[23:16]	7:0	See description of '10310Ch'.	
08h (103110h)	**REG103110**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[7:0]	7:0	Limit for phase correction modification.	
08h (103111h)	**REG103111**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[15:8]	7:0	See description of '103110h'.	
09h (103112h)	**REG103112**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_D5D6D7_RK[23:16]	7:0	See description of '103110h'.	
0Ah	**REG103114**	**7:0**	**Default : 0x00**	**Access : R/W**

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	LIMIT_LPLL_OFFSET[7:0]	7:0	Limit for LPLL phase offset.	
0Ah (103115h)	**REG103115**	**7:0**	**Default : 0x00**	**Access : R/W**
	LIMIT_LPLL_OFFSET[15:8]	7:0	See description of '103114h'.	
0Bh (103116h)	**REG103116**	**7:0**	**Default : 0x10**	**Access : R/W**
	P_GAIN_PRD[3:0]	7:4	P_GAIN for PRD_LOCK, gain setting is same as I_GAIN_PRD.	
	I_GAIN_PRD[3:0]	3:0	I_GAIN for PRD lock. 0: >> 5. 1: >> 4. 2: >> 3. 3: >> 2. 4: >> 1. 5: Same. 6: << 1. 7: << 2. 8: << 3. 9: << 4. 10: << 5. 11: << 6. 12: << 7. 13: << 8. 14: << 9. 15: << 10.	
0Bh (103117h)	**REG103117**	**7:0**	**Default : 0x10**	**Access : R/W**
	P_GAIN_PHASE[3:0]	7:4	P_GAIN for phase lock, gain setting is same as I_GAIN_PRD.	
	I_GAIN_PHASE[3:0]	3:0	I_GAIN for phase lock, game setting is same as I_GAIN_PRD.	
0Ch (103118h)	**REG103118**	**7:0**	**Default : 0x00**	**Access : R/W**
	P_GAIN_PHASE_ZERO	7	Disable P_GAIN for lock phase.	
	I_GAIN_PHASE_ZERO	6	Disable I_GAIN for lock phase.	
	P_GAIN_PRD_ZERO	5	Disable P_GAIN for lock PRD.	
	I_GAIN_PRD_ZERO	4	Disable I_GAIN for lock PRD.	
	FRAME_LPLL_EN	3	Frame LPLL enable.	
	-	2	Reserved.	
	FPLL_MODE[1:0]	1:0	FPLL Mode. 00: Lock phase mode.	
0Ch (103119h)	**REG103119**	**7:0**	**Default : 0x00**	**Access : R/W**
	OVS_FRAME_DIV[3:0]	7:4	Output fame DIV for frame sync.	

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	IVS_FRAME_DIV[3:0]	3:0	Input frame DIV for frame sync.	
0Dh (10311Ah)	**REG10311A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	EN_2_LIMIT	4	Enable 2 limit.	
	FORCE_PHASE_CLOSE_DONE	3	S.W. Force phase close done.	
	FORCE_PHASE_REDUCE_DONE	2	S.W. Force phase reduce done.	
	FORCE_PRD_LOCK_DONE	1	S.W. Force PRD lock done.	
	FORCE_PRD_STABLE	0	S.W. Force PRD stable check ok.	
0Dh (10311Bh)	**REG10311B**	**7:0**	**Default : 0x03**	**Access : R/W**
	-	7:4	Reserved.	
	SSC_EN	3	SSC mode enable.	
	PRD_SEL_ORI_VS	2	Select ORI OVS as lock PRD reference.	
	NON_STABLE_EN	1	Frame PLL disable when NON_STABLE flag high.	
	NO_SIGNAL_EN	0	Frame PLL disable when NO_SIGNAL flag high.	
0Fh (10311Eh)	**REG10311E**	**7:0**	**Default : 0x44**	**Access : R/W**
	LPLL_SET[7:0]	7:0	LPLL initial setting value.	
0Fh (10311Fh)	**REG10311F**	**7:0**	**Default : 0x55**	**Access : R/W**
	LPLL_SET[15:8]	7:0	See description of '10311Eh'.	
10h (103120h)	**REG103120**	**7:0**	**Default : 0x24**	**Access : R/W**
	LPLL_SET[23:16]	7:0	See description of '10311Eh'.	
11h (103122h)	**REG103122**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_DIF[7:0]	7:0	Phase dif value.	
11h (103123h)	**REG103123**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_DIF[15:8]	7:0	See description of '103122h'.	
12h (103124h)	**REG103124**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PHASE_UP	0	OVS leading or lagging related to IVS. 0: Leading. 1: Lagging.	
13h (103126h)	**REG103126**	**7:0**	**Default : 0x00**	**Access : RO**
	PRD_DIF[7:0]	7:0	Reference signal PRD difference value.	

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
13h (103127h)	**REG103127**	**7:0**	**Default : 0x00**	**Access : RO**
	PRD_DIF[15:8]	7:0	See description of '103126h'.	
14h (103128h)	**REG103128**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PRD_UP	0	OVS PRD related to IVS PRD. 0: Faster. 1: Slower.	
16h ~ 16h (10312Ch ~ 10312Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
17h (10312Eh)	**REG10312E**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL_STEP[7:0]	7:0	Output PLL spread spectrum step.	
17h (10312Fh)	**REG10312F**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_STEP[9:8]	1:0	See description of '10312Eh'.	
18h (103130h)	**REG103130**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL_SPAN[7:0]	7:0	Output PLL spread spectrum span.	
18h (103131h)	**REG103131**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_SPAN[13:8]	5:0	See description of '103130h'.	
19h ~ 1Eh (103132h ~ 10313Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
1Fh (10313Eh)	**REG10313E**	**7:0**	**Default : 0x80**	**Access : R/W**
	PHASE_CLOSE_THRESH[7:0]	7:0	Phase close done thresh.	
1Fh (10313Fh)	**REG10313F**	**7:0**	**Default : 0x30**	**Access : R/W**
	REDUCE_DONE_THRESH[3:0]	7:4	Phase reduce done thresh.	
	PHASE_CLOSE_THRESH[11:8]	3:0	See description of '10313Eh'.	
20h (103140h)	**REG103140**	**7:0**	**Default : 0x52**	**Access : R/W**
	-	7	Reserved.	
	HIS_CNT_HIGH_THRESH[2	6:4	History counter high thresh.	

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	:0]			
	-	3	Reserved.	
	HIS_CNT_LOW_THRESH[2:0]	2:0	History counter low thresh.	
21h (103142h)	**REG103142**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[7:0]	7:0	IVS PRD value.	
21h (103143h)	**REG103143**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[15:8]	7:0	See description of '103142h'.	
22h (103144h)	**REG103144**	**7:0**	**Default : 0x00**	**Access : RO**
	IVS_PRD_VALUE[23:16]	7:0	See description of '103142h'.	
23h (103146h)	**REG103146**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[7:0]	7:0	OVS PRD value.	
23h (103147h)	**REG103147**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[15:8]	7:0	See description of '103146h'.	
24h (103148h)	**REG103148**	**7:0**	**Default : 0x00**	**Access : RO**
	OVS_PRD_VALUE[23:16]	7:0	See description of '103146h'.	
26h ~ 27h (10314Ch ~ 10314Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
28h (103150h)	**REG103150**	**7:0**	**Default : 0x00**	**Access : RO**
	LPLL_SET_USING[7:0]	7:0	LPLL_SET value for using.	
28h (103151h)	**REG103151**	**7:0**	**Default : 0x00**	**Access : RO**
	LPLL_SET_USING[15:8]	7:0	See description of '103150h'.	
29h (103152h)	**REG103152**	**7:0**	**Default : 0x00**	**Access : RO**
	LPLL_SET_USING[23:16]	7:0	See description of '103150h'.	
2Ah (103154h)	**REG103154**	**7:0**	**Default : 0x00**	**Access : RO**
	PHASE_REDUCE_DONE	7	Phase reduce done flag.	
	PRD_LOCK_DONE	6	PRD lock done flag.	
	IVS_PRD_STABLE	5	IDCLK stable flag.	
	OVS_PRD_STABLE	4	ODCLK stable flag.	
	-	3	Reserved.	
	CS_STATE[2:0]	2:0	Frame PLL FSM state. 3'h0: Free run.	

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
			3'h1: LOCK_FREQ. 3'h2: REDUCE_PHASE. 3'h3: Wait PHASE_CLOSE. 3'h4: LOCK_PHASE. Others: Reserved.	
2Ah (103155h)	**REG103155**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	PHASE_LOCK_DONE	0	Phase lock done flag.	
2Bh ~ 2Dh (103156h ~ 10315Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
2Eh (10315Ch)	**REG10315C**	**7:0**	**Default : 0xC3**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_PDREG	1	LPLL REG power down.	
	LPL_PDBG	0	LPLL BG power down.	
2Eh (10315Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
30h (103160h)	**REG103160**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control: 00: /1. 01: /2. 10: /4. 11: /8.	
30h (103161h)	**REG103161**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N); 0: Divide 1. 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4.	
31h (103162h)	**REG103162**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control: 00: /1. 01: /2.	

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
			10: /4. 11: /8.	
31h (103163h)	**REG103163**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_LOOP_DIV_SECOND [7:0]	7:0	Loop divider ratio control: divide ratio=(1/N); Default ratio=8; 0: Divide 1. 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4.	
32h (103164h)	**REG103164**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL2_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
32h (103165h)	**REG103165**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_OUTPUT_DIV_SECOND[7:0]	7:0	Output divider.	
33h (103166h)	**REG103166**	**7:0**	**Default : 0x20**	**Access : R/W**
	LPLL2_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL2_2CHIP_SYN_EN	6		
	LPLL2_PD	5	Power down control to PLL (active high).	
	LPLL2_EN_HFLVDS	4	Reset digital circuit in LPLL.	
	LPLL2_IBIAS_ICTRL[1:0]	3:2		
	LPLL2_ICP_ICTRL[1:0]	1:0	LPLL current control.	
33h (103167h)	**REG103167**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	LPLL2_HIGH_FLAG	7		
	LPLL2_LOCK	6		
	-	5	Reserved.	
	LPLL2_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL2_EN_SKEW_DIVIDER	1		
	LPLL2_ENFRUN	0		
34h (103168h)	**REG103168**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	

LPLL Register (Bank = 1031)

Index (Absolute)	Mnemonic	Bit	Description	
	LPLL2_SKEW_CLKP_PHASE_SEL[4:0]	4:0		
34h (103169h)	**REG103169**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:5	Reserved.	
	LPLL2_SKEW_CLKM_PHASE_SEL[4:0]	4:0		
35h (10316Ah)	**REG10316A**	**7:0**	**Default : 0x10**	**Access : R/W**
	-	7:6	Reserved.	
	LPLL_2NDPLL_CLK_SEL	5		
	LPLL_POSTDIV_RESET	4		
	-	3	Reserved.	
	LPLL_2CHIP_REFIN_SEL	2		
	LPLL_2CHIP_FBIN_SEL	1		
	LPLL_2CHIP_CLKOUT_SEL	0		
36h (10316Ch)	**REG10316C**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[7:0]	7:0	LPLL1_TEST.	
36h (10316Dh)	**REG10316D**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[15:8]	7:0	See description of '10316Ch'.	
37h (10316Eh)	**REG10316E**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[23:16]	7:0	See description of '10316Ch'.	
37h (10316Fh)	**REG10316F**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL1_TEST[31:24]	7:0	See description of '10316Ch'.	
38h (103170h)	**REG103170**	**7:0**	**Default : 0x01**	**Access : R/W**
	-	7:2	Reserved.	
	LPLL_SCALAR_FB_DIV2_EN	1		
	LPLL_NCO_RETIME_SEL	0		
39h (103172h)	**REG103172**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_TEST[7:0]	7:0	LPLL2_TEST.	
39h (103173h)	**REG103173**	**7:0**	**Default : 0x00**	**Access : R/W**
	LPLL2_TEST[15:8]	7:0	See description of '103172h'.	
3Ah (103174h)	**REG103174**	**7:0**	**Default : 0x0C**	**Access : R/W**
	-	7:5	Reserved.	

LPLL Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LPLL_2CHIP_SCALAR_FB_DIV2_EN	4		
	OEN_FBIN	3		
	OEN_REFIN	2		
	LPLL1_RX_CLKFB_SEL	1		
	LPLL1_CLKIN_SEL	0		
3Bh ~ 3Eh (103176h ~ 10317Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Fh (10317Eh)	**REG10317E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:1	Reserved.	
	LPLL_RESET	0	LPLL software reset, high active.	
7Fh (1031FEh)	**REG1031FE**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	SW_TRIG_DB_LOAD	1	Trig to load double buffer register.	
	DB_EN	0	Enable LPLL register double.	

Scaler4 Register (Bank = 1032)

MOD Register (Bank = 1032, Sub-bank = 00)

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 07h (103203h ~ 10320Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h (103241h)	**REG103241**	**7:0**	**Default : 0x11**	**Access : R/W**
	CKG_DOT_MINI_PRE[3:0]	7:4	Clock gen register of CLK_DOT_MINI_PRE. Bit[0]: Gating. Bit[1]: Invert. Bit[3:2] = 00, enable.	
	CKG_DOT_MINI[3:0]	3:0	Clock gen register of CLK_DOT_MINI. Bit[0]: Gating. Bit[1]: Invert. Bit[3:2] = 00, enable.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h ~ 22h (103242h ~ 103245h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
23h (103246h)	**REG103246**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_PE_ADJ_CH2[1:0]	7:6	Differential output data/clock pre-emphasis level adjust of ch2.	
	GCR_PE_ADJ_CH1[2:0]	5:3	Differential output data/clock pre-emphasis level adjust of ch1.	
	GCR_PE_ADJ_CH0[2:0]	2:0	Differential output data/clock pre-emphasis level adjust of ch0.	
23h (103247h)	**REG103247**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GCR_PE_ADJ_CH4[2:0]	6:4	Differential output data/clock pre-emphasis level adjust of ch4.	
	GCR_PE_ADJ_CH3[2:0]	3:1	Differential output data/clock pre-emphasis level adjust of ch3.	
	GCR_PE_ADJ_CH2[2]	0	See description of '103246h'.	
24h (103248h)	**REG103248**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_PE_ADJ_CH7[1:0]	7:6	Differential output data/clock pre-emphasis level adjust of ch7.	
	GCR_PE_ADJ_CH6[2:0]	5:3	Differential output data/clock pre-emphasis level adjust of ch6.	
	GCR_PE_ADJ_CH5[2:0]	2:0	Differential output data/clock pre-emphasis level adjust of ch5.	
24h (103249h)	**REG103249**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GCR_PE_ADJ_CH9[2:0]	6:4	Differential output data/clock pre-emphasis level adjust of ch9.	
	GCR_PE_ADJ_CH8[2:0]	3:1	Differential output data/clock pre-emphasis level adjust of ch8.	
	GCR_PE_ADJ_CH7[2]	0	See description of '103248h'.	
25h (10324Ah)	**REG10324A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	GCR_PE_ADJ_CH11[2:0]	5:3	Differential output data/clock pre-emphasis level adjust of ch11.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GCR_PE_ADJ_CH10[2:0]	2:0	Differential output data/clock pre-emphasis level adjust of ch10.	
29h (103252h)	**REG103252**	**7:0**	**Default : 0xA0**	**Access : R/W**
	GCR_ICON_CH0[3:0]	7:4	Control swing of ch0. Swing = offset(150mV) + code*10mV.	
	-	3:0	Reserved.	
29h (103253h)	**REG103253**	**7:0**	**Default : 0x28**	**Access : R/W**
	GCR_ICON_CH1[5:0]	7:2	Control swing of ch1.	
	GCR_ICON_CH0[5:4]	1:0	See description of '103252h'.	
2Ah (103254h)	**REG103254**	**7:0**	**Default : 0x8A**	**Access : R/W**
	GCR_ICON_CH3[1:0]	7:6	Control swing of ch3.	
	GCR_ICON_CH2[5:0]	5:0	Control swing of ch2.	
2Ah (103255h)	**REG103255**	**7:0**	**Default : 0xA2**	**Access : R/W**
	GCR_ICON_CH4[3:0]	7:4	Control swing of ch4.	
	GCR_ICON_CH3[5:2]	3:0	See description of '103254h'.	
2Bh (103256h)	**REG103256**	**7:0**	**Default : 0x28**	**Access : R/W**
	GCR_ICON_CH5[5:0]	7:2	Control swing of ch5.	
	GCR_ICON_CH4[5:4]	1:0	See description of '103255h'.	
2Bh (103257h)	**REG103257**	**7:0**	**Default : 0x8A**	**Access : R/W**
	GCR_ICON_CH7[1:0]	7:6	Control swing of ch7.	
	GCR_ICON_CH6[5:0]	5:0	Control swing of ch6.	
2Ch (103258h)	**REG103258**	**7:0**	**Default : 0xA2**	**Access : R/W**
	GCR_ICON_CH8[3:0]	7:4	Control swing of ch8.	
	GCR_ICON_CH7[5:2]	3:0	See description of '103257h'.	
2Ch (103259h)	**REG103259**	**7:0**	**Default : 0x28**	**Access : R/W**
	GCR_ICON_CH9[5:0]	7:2	Control swing of ch9.	
	GCR_ICON_CH8[5:4]	1:0	See description of '103258h'.	
2Dh (10325Ah)	**REG10325A**	**7:0**	**Default : 0x8A**	**Access : R/W**
	GCR_ICON_CH11[1:0]	7:6	Control swing of ch11.	
	GCR_ICON_CH10[5:0]	5:0	Control swing of ch10.	
2Dh (10325Bh)	**REG10325B**	**7:0**	**Default : 0x02**	**Access : R/W**
	-	7:4	Reserved.	
	GCR_ICON_CH11[5:2]	3:0	See description of '10325Ah'.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
33h (103266h)	**REG103266**	**7:0**	**Default : 0x00**	**Access : R/W**
	SWUPLIMIT[0]	7	MOD_SERI_TOP software up limit.	
	SWLOWLIMIT[2:0]	6:4	MOD_SERI_TOP software low limit.	
	SWCHECK_POINT[3:0]	3:0	MOD_SERI_TOP software check point.	
33h (103267h)	**REG103267**	**7:0**	**Default : 0x80**	**Access : R/W**
	CHECKENABLE	7	MOD_SERI_TOP CHECKENABLE.	
	DATA_FORMAT	6	MOD_DATA format.	
	SWRST_POINT[2:0]	5:3	MOD_SERI_TOP software reset point.	
	SWMODE_EN	2	MOD_SERI_TOP software mode enable.	
	SWUPLIMIT[2:1]	1:0	See description of '103266h'.	
35h ~ 36h (10326Ah ~ 10326Dh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
37h (10326Eh)	**REG10326E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	GCR_PVDD_2P5	6	MOD PVDD power. 0: 3.3V. 1: 2.5V.	
	GCR_VCM_0P9	5	Differential output common mode voltage adjust. 0: 1.25V. 1: 0.94V.	
	-	4:0	Reserved.	
38h ~ 3Ch (103270h ~ 103279h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
3Dh (10327Ah)	**REG10327A**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:6	Reserved.	
	ICON_RESULT[5:0]	5:0	Calibration icon result.	
3Dh (10327Bh)	**REG10327B**	**7:0**	**Default : 0x00**	**Access : RO, R/W**
	-	7	Reserved.	
	CAL_FINISH	6	Calibration finish flag.	
	CAL_FAIL	5	Calibration fail flag.	
	-	4:0	Reserved.	
40h	**REG103280**	**7:0**	**Default : 0x08**	**Access : R/W**

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LVDS_OSD_A	7	LVDS OSD enable for Channel A.	
	CH_SWAP	6	For pair swapping with 0x40[3].	
	CH_POLARITY	5	Channel polarity p/n swap for LVDS pair.	
	LVDS_PLASMA_A	4	LVDS_PLASMA for Channel A.	
	PDP_10BIT	3	PDP_10BIT for pair swap with 0x40[5].	
	LVDS_TI	2	LVDS_TI. 0: JEIDA mode. 1: VESA mode with 0x4b[1:0].	
	-	0:1	Reserved.	
40h (103281h)	**REG103281**	**7:0**	**Default : 0x00**	**Access : R/W**
	ECLKDLYSEL[3:0]	7:4	De delay for TTL output.	
	CLKDLYSEL[3:0]	3:0	Clock delay for TTL output.	
41h (103282h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
41h (103283h)	**REG103283**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDP_MASK_EN_A	7	PDP_MASK_EN DE channel A.	
	PDP_MASK_SET_A	6	PDP_MASK_SET DE channel A.	
	PDP_CH3_EN_A	5	PDP_CH3_EN channel A.	
	PDP_CH3_SET_A	4	PDP_CH3_SET channel A.	
	PDP_CH4_EN_A	3	PDP_CH4_EN channel A.	
	PDP_CH4_SET_A	2	PDP_CH4_SET for channel A.	
	-	1:0	Reserved.	
42h (103284h)	**REG103284**	**7:0**	**Default : 0x00**	**Access : R/W**
	SHIFT_LVDS_PAIR[1:0]	7:6	Shift LVDS arrangement for different substrate.	
	PDP_10BIT_MOR[1:0]	5:4	More pair swap mode.	
	-	3	Reserved.	
	EN_VS_ON_OSD	2	Vsync on OSD enable.	
	PAIR_SWAP_MOR[1:0]	1:0	More pair swap mode.	
42h (103285h)	**REG103285**	**7:0**	**Default : 0x10**	**Access : R/W**
	OSD_DE_INV	7	Invert OSD DE.	
	OSD_ON_DE_B	6	PDP OSD de on DE channel B.	
	OSD_ON_DE_A	5	PDP OSD de on DE channel A.	
	SW_RST	4	Software reset.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LVDS_OSD_B	3	LVDS OSD enable for Channel B.	
	LVDS_PLASMA_B	2	LVDS_PLASMA for Channel B.	
	-	1	Reserved.	
	EN_MORE_PAIR_SWAP	0	Enable more pair swap.	
43h (103286h)	**REG103286**	**7:0**	**Default : 0xC6**	**Access : R/W**
	LVDS_CLOCK_PHASE[6:0]	7:1	Clock phase could be set by register.	
	-	0	Reserved.	
43h (103287h)	**REG103287**	**7:0**	**Default : 0x00**	**Access : R/W**
	PDP_MASK_EN_B	7	PDP_MASK_EN DE channel B.	
	PDP_MASK_SET_B	6	PDP_MASK_SET DE channel B.	
	PDP_CH3_EN_B	5	PDP_CH3_EN channel B.	
	PDP_CH3_SET_B	4	PDP_CH3_SET channel B.	
	PDP_CH4_EN_B	3	PDP_CH4_EN channel B.	
	PDP_CH4_SET_B	2	PDP_CH4_SET for channel B.	
	-	1:0	Reserved.	
44h (103289h)	**REG103289**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	LCK_PHASE_SEL	3	Phase select of TTL clkx2. 1: Phase ahead 90 degree.	
	-	2:0	Reserved.	
45h (10328Ah)	**REG10328A**	**7:0**	**Default : 0x3F**	**Access : R/W**
	-	7:6	Reserved.	
	LVDS_LA_OEZ	5	LVDS_LA_OEZ.	
	LVDS_LB_OEZ	4	LVDS_LB_OEZ.	
	CK_OEZ	3	TTL-CK_OEZ.	
	DE_OEZ	2	TTL-DE_OEZ.	
	HS_OEZ	1	TTL-HS_OEZ.	
	VS_OEZ	0	TTL-VS_OEZ.	
45h (10328Bh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
46h (10328Ch)	**REG10328C**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXT_DATA_EN[7:0]	7:0	External/ test bus enable mode for pair0~11.	
46h	**REG10328D**	**7:0**	**Default : 0x00**	**Access : R/W**

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EXT_DATA_EN[15:8]	7:0	See description of '10328Ch'.	
47h (10328Eh)	**REG10328E**	**7:0**	**Default : 0x00**	**Access : R/W**
	EXT_DATA_EN[23:16]	7:0	See description of '10328Ch'.	
48h ~ 48h (103290h ~ 103291h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
49h (103292h)	**REG103292**	**7:0**	**Default : 0x00**	**Access : R/W**
	MLX_METHOD[1:0]	7:6	Output format selection for TTL output. 10: 8-bit. 01: 6-bit. Other: 10-bit.	
	ERGX	5	Even channel red and green channel swap.	
	EGBX	4	Even channel green and blue channel swap.	
	ORGX	3	Odd channel red and green channel swap.	
	OGBX	2	Odd channel green and blue channel swap.	
	-	1:0	Reserved.	
49h (103293h)	**REG103293**	**7:0**	**Default : 0x00**	**Access : R/W**
	GATE_DE	7	Output de gating.	
	EMLX	6	Even LSB and MSB swapping.	
	ERBX	5	Even channel red and blue channel swap.	
	OMLX	4	Odd LSB and MSB swapping.	
	ORBX	3	Odd channel red and blue channel swap.	
	OBN	2	Reserved.	
	WDG	1	Blanking time data become all 1.	
	REVL	0	Reverse output pix.	
4Ah (103294h)	**REG103294**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	TTL_LVDS	6	TTL dual clock output.	
	-	5	Reserved.	
	CLK_INVERT	4	Output clock invert.	
	VS_INVERT	3	Output Vsync invert.	
	DE_INVERT	2	Output DE invert.	
	DUALMODE	1	Dual LVDS channel selection.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ABSWITCH	0	Odd -even LVDS channel switch.	
4Ah (103295h)	**REG103295**	**7:0**	**Default : 0x00**	**Access : R/W**
	AUTOVS_EARLY	7	Auto Vsync early DE.	
	INTER_HS	6	Interlace Hsync.	
	INTERLACE_HS_GATE	5	Interlace Hsync gate.	
	HS_INVERT	4	Hsync invert.	
	HS_REMO	3	GPO or original Hsync selection.	
	-	2:1	Reserved.	
	PUA	0	VSYNC and CLOCK for TTL gating.	
4Bh (103296h)	**REG103296**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:3	Reserved.	
	MASK_TTL_DUAL	2	Mask dual channel de output.	
	TI_BITMODE[1:0]	1:0	TI bit mode. 0x: 10-bit. 10: 8-bit. 11: 6-bit.	
4Ch (103298h)	**REG103298**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CRC_EN	3	CRC testing enable.	
	CHANNEL_SEL[2:0]	2:0	CRC testing channel selection.	
4Dh (10329Ah)	**REG10329A**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_SEL[7:0]	7:0	General purpose output for pair0~11.	
4Dh (10329Bh)	**REG10329B**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_SEL[15:8]	7:0	See description of '10329Ah'.	
4Eh (10329Ch)	**REG10329C**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_SEL[23:16]	7:0	See description of '10329Ah'.	
4Fh (10329Eh)	**REG10329E**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[7:0]	7:0	General purpose data-in for pair0~11.	
4Fh (10329Fh)	**REG10329F**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[15:8]	7:0	See description of '10329Eh'.	
50h (1032A0h)	**REG1032A0**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_DATAIN[23:16]	7:0	See description of '10329Eh'.	
51h	**REG1032A2**	**7:0**	**Default : 0x00**	**Access : R/W**

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPO_OEZ[7:0]	7:0	General purpose pad direction for pair0~11. 0: Output. 1: Input.	
51h (1032A3h)	**REG1032A3**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_OEZ[15:8]	7:0	See description of '1032A2h'.	
52h (1032A4h)	**REG1032A4**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPO_OEZ[23:16]	7:0	See description of '1032A2h'.	
53h (1032A7h)	**REG1032A7**	**7:0**	**Default : 0x00**	**Access : R/W**
	VBI_EN	7	VBI information on LVDS enable.	
	-	6:0	Reserved.	
54h (1032A8h)	**REG1032A8**	**7:0**	**Default : 0x00**	**Access : RO**
	CRC_OUT[7:0]	7:0	CRC testing result.	
54h (1032A9h)	**REG1032A9**	**7:0**	**Default : 0x00**	**Access : RO**
	CRC_OUT[15:8]	7:0	See description of '1032A8h'.	
55h (1032AAh)	**REG1032AA**	**7:0**	**Default : 0x00**	**Access : RO**
	MOD_GPI[7:0]	7:0	General purpose input for pair0~11.	
55h (1032ABh)	**REG1032AB**	**7:0**	**Default : 0x00**	**Access : RO**
	MOD_GPI[15:8]	7:0	See description of '1032AAh'.	
56h (1032ACh)	**REG1032AC**	**7:0**	**Default : 0x00**	**Access : RO**
	MOD_GPI[23:16]	7:0	See description of '1032AAh'.	
57h ~ 59h (1032AEh ~ 1032B3h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
5Ah (1032B5h)	**REG1032B5**	**7:0**	**Default : 0x00**	**Access : R/W**
	3D_CH3_EN_A	7	Enable 3d flag on LVDS channel A pair 3.	
	3D_CH4_EN_A	6	Enable 3d flag on LVDS channel A pair 4.	
	3D_CH3_EN_B	5	Enable 3d flag on LVDS channel B pair 3.	
	3D_CH4_EN_B	4	Enable 3d flag on LVDS channel B pair 4.	
	-	3:0	Reserved.	
6Ch (1032D9h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
6Dh (1032DAh)	**REG1032DA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_OUTCONF_CH3[1:0]	7:6	Output mode configuration for channel 3.	

MOD Register (Bank = 1032, Sub-bank = 00)

Index (Absolute)	Mnemonic	Bit	Description	
	GCR_OUTCONF_CH2[1:0]	5:4	Output mode configuration for channel 2.	
	GCR_OUTCONF_CH1[1:0]	3:2	Output mode configuration for channel 1.	
	GCR_OUTCONF_CH0[1:0]	1:0	Output mode configuration for channel 0. 2'b00: TTL mode/Standby mode. 2'b01: LVDS/EPI/RSDS/mini-LVDS data output mode. 2'b10: RSDS/mini-LVDS clock output mode. 2'b11: Test clock output mode.	
6Dh (1032DBh)	**REG1032DB**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_OUTCONF_CH7[1:0]	7:6	Output mode configuration for channel 7.	
	GCR_OUTCONF_CH6[1:0]	5:4	Output mode configuration for channel 6.	
	GCR_OUTCONF_CH5[1:0]	3:2	Output mode configuration for channel 5.	
	GCR_OUTCONF_CH4[1:0]	1:0	Output mode configuration for channel 4.	
6Eh (1032DCh)	**REG1032DC**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_OUTCONF_CH11[1:0]	7:6	Output mode configuration for channel 11.	
	GCR_OUTCONF_CH10[1:0]	5:4	Output mode configuration for channel 10.	
	GCR_OUTCONF_CH9[1:0]	3:2	Output mode configuration for channel 9.	
	GCR_OUTCONF_CH8[1:0]	1:0	Output mode configuration for channel 8.	
71h (1032E2h)	**REG1032E2**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_PE_EN_CH[7:0]	7:0	Differential output pre-emphasis enable for channel [11:0].	
71h (1032E3h)	**REG1032E3**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GCR_PE_EN_CH[11:8]	3:0	See description of '1032E2h'.	
73h (1032E6h)	**REG1032E6**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_DS_POL_CH[7:0]	7:0	Differential output polarity swap for channel [11:0].	
73h (1032E7h)	**REG1032E7**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GCR_DS_POL_CH[11:8]	3:0	See description of '1032E6h'.	
75h (1032EAh)	**REG1032EA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_EN_RINT_CH[7:0]	7:0	Internal resistor enable.	
75h (1032EBh)	**REG1032EB**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	GCR_EN_RINT_CH[11:8]	3:0	See description of '1032EAh'.	
77h	**REG1032EE**	**7:0**	**Default : 0x00**	**Access : R/W**

MOD Register (Bank = 1032, Sub-bank = 00)

Index (Absolute)	Mnemonic	Bit	Description	
	-	7:5	Reserved.	
	EN_CK_PD	4	Part C LVDS/EPI clock enable. This pin is used for CH14~CH21.	
	EN_CK_PC	3	Part C LVDS/EPI clock enable. This pin is used for CH8~CH13.	
	EN_CK_PB	2	Part B LVDS/EPI clock enable. This pin is used for CH2~CH7.	
	EN_CK_PA	1	Part A LVDS/EPI clock enable. This pin is used for CH0~CH1.	
	GCR_CKEN	0	Part A, B, C LVDS/EPI clock enable. This pin is used for CH0~CH13.	
78h (1032F0h)	**REG1032F0**	**7:0**	**Default : 0xF1**	**Access : R/W**
	-	7:1	Reserved.	
	PD_IB_MOD	0	Power down mod bias current source.	
78h ~ 7Bh (1032F1h ~ 1032F6h)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
7Dh (1032FAh)	**REG1032FA**	**7:0**	**Default : 0x00**	**Access : R/W**
	GCR_CAL_EN	7	Enable calibration function.	
	-	6:4	Reserved.	
	GCR_CAL_SRC[1:0]	3:2	Select calibration source pair.	
	GCR_CAL_LEVEL[1:0]	1:0	Select calibration target voltage (may change before tape-out). 00: 239mV. 01: 335mV. 10: 287mV. 11: 201mV.	
7Dh (1032FBh)	**REG1032FB**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:1	Reserved.	
	C_CAL_OUT	0	Calibration result output. 0: Lower than target. 1: Higher than target.	

PWM Register (Bank = 1032, Sub-bank = 01)

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (103204h)	**REG103204**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_PERIOD[7:0]	7:0	PWM0 period.	
02h (103205h)	**REG103205**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_PERIOD[15:8]	7:0	See description of '103204h'.	
03h (103206h)	**REG103206**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_DUTY[7:0]	7:0	PWM0 duty.	
03h (103207h)	**REG103207**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_DUTY[15:8]	7:0	See description of '103206h'.	
04h (103208h)	**REG103208**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_DIV[7:0]	7:0	PWM0 divider.	
04h (103209h)	**REG103209**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	PWM0_VDBEN_SW	6	PWM0 Vsync double buffer enable by software. 0: Disable. 1: Enable.	
	-	5:4	Reserved.	
	PWM0_DBEN	3	PWM0 double buffer enable.	
	PWM0_RESET_EN	2	PWM0 Vsync reset0.	
	PWM0_VDBEN	1	PWM0 Vsync double buffer enable.	
	PWM0_POLARITY	0	PWM0 polarity.	
05h (10320Ah)	**REG10320A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_PERIOD[7:0]	7:0	PWM1 period.	
05h (10320Bh)	**REG10320B**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_PERIOD[15:8]	7:0	See description of '10320Ah'.	
06h (10320Ch)	**REG10320C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_DUTY[7:0]	7:0	PWM1 duty.	
06h (10320Dh)	**REG10320D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_DUTY[15:8]	7:0	See description of '10320Ch'.	
07h (10320Eh)	**REG10320E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_DIV[7:0]	7:0	PWM1 divider.	
07h (10320Fh)	**REG10320F**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	

PWM Register (Bank = 1032, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	PWM1_VDBEN_SW	6	PWM1 Vsync double buffer enable by software. 0: Disable. 1: Enable.	
	-	5:4	Reserved.	
	PWM1_DBEN	3	PWM1 double buffer enable.	
	PWM1_RESET_EN	2	PWM1 Vsync reset1.	
	PWM1_VDBEN	1	PWM1 Vsync double buffer enable.	
	PWM1_POLARITY	0	PWM1 polarity.	
08h (103210h)	**REG103210**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_PERIOD[7:0]	7:0	PWM2 period.	
08h (103211h)	**REG103211**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_PERIOD[15:8]	7:0	See description of '103210h'.	
09h (103212h)	**REG103212**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_DUTY[7:0]	7:0	PWM2 duty.	
09h (103213h)	**REG103213**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_DUTY[15:8]	7:0	See description of '103212h'.	
0Ah (103214h)	**REG103214**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_DIV[7:0]	7:0	PWM2 divider.	
0Ah (103215h)	**REG103215**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	PWM2_VDBEN_SW	6	PWM2 Vsync double buffer enable by software. 0: Disable. 1: Enable.	
	-	5:4	Reserved.	
	PWM2_DBEN	3	PWM2 double buffer enable.	
	PWM2_RESET_EN	2	PWM2 Vsync reset2.	
	PWM2_VDBEN	1	PWM2 Vsync double buffer enable.	
	PWM2_POLARITY	0	PWM2 polarity.	
0Bh (103216h)	**REG103216**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_PERIOD[7:0]	7:0	PWM3 period.	
0Bh (103217h)	**REG103217**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_PERIOD[15:8]	7:0	See description of '103216h'.	
0Ch	**REG103218**	**7:0**	**Default : 0x00**	**Access : R/W**

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM3_DUTY[7:0]	7:0	PWM3 duty.	
0Ch (103219h)	**REG103219**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_DUTY[15:8]	7:0	See description of '103218h'.	
0Dh (10321Ah)	**REG10321A**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_DIV[7:0]	7:0	PWM3 divider.	
0Dh (10321Bh)	**REG10321B**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	PWM3_VDBEN_SW	6	PWM3 Vsync double buffer enable by software. 0: Disable. 1: Enable.	
	-	5:4	Reserved.	
	PWM3_DBEN	3	PWM3 double buffer enable.	
	PWM3_RESET_EN	2	PWM3 Vsync reset3.	
	PWM3_VDBEN	1	PWM3 Vsync double buffer enable.	
	PWM3_POLARITY	0	PWM3 polarity.	
0Eh (10321Ch)	**REG10321C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_PERIOD[7:0]	7:0	PWM4 period.	
0Eh (10321Dh)	**REG10321D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_PERIOD[15:8]	7:0	See description of '10321Ch'.	
0Fh (10321Eh)	**REG10321E**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_DUTY[7:0]	7:0	PWM4 duty.	
0Fh (10321Fh)	**REG10321F**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_DUTY[15:8]	7:0	See description of '10321Eh'.	
10h (103220h)	**REG103220**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_DIV[7:0]	7:0	PWM4 divider.	
10h (103221h)	**REG103221**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	PWM4_VDBEN_SW	6	PWM4 Vsync double buffer enable by software. 0: Disable. 1: Enable.	
	-	5:4	Reserved.	
	PWM4_DBEN	3	PWM4 double buffer enable.	
	PWM4_RESET_EN	2	PWM4 Vsync reset4.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM4_VDBEN	1	PWM4 Vsync double buffer enable.	
	PWM4_POLARITY	0	PWM4 polarity.	
11h (103222h)	**REG103222**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_PERIOD[7:0]	7:0	PWM5 period.	
11h (103223h)	**REG103223**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_PERIOD[15:8]	7:0	See description of '103222h'.	
12h (103224h)	**REG103224**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_DUTY[7:0]	7:0	PWM5 duty.	
12h (103225h)	**REG103225**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_DUTY[15:8]	7:0	See description of '103224h'.	
13h (103226h)	**REG103226**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_DIV[7:0]	7:0	PWM5 divider.	
13h (103227h)	**REG103227**	**7:0**	**Default : 0x40**	**Access : R/W**
	-	7	Reserved.	
	PWM5_VDBEN_SW	6	PWM5 Vsync double buffer enable by software. 0: Disable. 1: Enable.	
	-	5:4	Reserved.	
	PWM5_DBEN	3	PWM5 double buffer enable.	
	PWM5_RESET_EN	2	PWM5 Vsync reset5.	
	PWM5_VDBEN	1	PWM5 Vsync double buffer enable.	
	PWM5_POLARITY	0	PWM5 polarity.	
14h (103228h)	**REG103228**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX1	7	PWM1 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT1[3:0]	3:0	PWM1 Hsync reset counter.	
14h (103229h)	**REG103229**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX0	7	PWM0 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT0[3:0]	3:0	PWM0 Hsync reset counter.	
15h (10322Ah)	**REG10322A**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX3	7	PWM3 reset mux.	
	-	6:4	Reserved.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HS_RST_CNT3[3:0]	3:0	PWM3 Hsync reset counter.	
15h (10322Bh)	**REG10322B**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX2	7	PWM2 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT2[3:0]	3:0	PWM2 Hsync reset counter.	
16h (10322Ch)	**REG10322C**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX5	7	PWM5 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT5[3:0]	3:0	PWM5 Hsync reset counter.	
16h (10322Dh)	**REG10322D**	**7:0**	**Default : 0x00**	**Access : R/W**
	RST_MUX4	7	PWM4 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT4[3:0]	3:0	PWM4 Hsync reset counter.	
17h ~ 1Fh (10322Eh ~ 10323Fh)	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	
20h (103240h)	**REG103240**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_PERIOD_EXT[1:0]	7:6	PWM3 extra 2 bit period setting.	
	PWM2_PERIOD_EXT[1:0]	5:4	PWM2 extra 2 bit period setting.	
	PWM1_PERIOD_EXT[1:0]	3:2	PWM1 extra 2 bit period setting.	
	PWM0_PERIOD_EXT[1:0]	1:0	PWM0 extra 2 bit period setting.	
20h (103241h)	**REG103241**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWM5_PERIOD_EXT[1:0]	3:2	PWM5 extra 2 bit period setting.	
	PWM4_PERIOD_EXT[1:0]	1:0	PWM4 extra 2 bit period setting.	
21h (103242h)	**REG103242**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_DUTY_EXT[1:0]	7:6	PWM3 extra 2 bit duty setting.	
	PWM2_DUTY_EXT[1:0]	5:4	PWM2 extra 2 bit duty setting.	
	PWM1_DUTY_EXT[1:0]	3:2	PWM1 extra 2 bit duty setting.	
	PWM0_DUTY_EXT[1:0]	1:0	PWM0 extra 2 bit duty setting.	
21h (103243h)	**REG103243**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWM5_DUTY_EXT[1:0]	3:2	PWM5 extra 2 bit duty setting.	

PWM Register (Bank = 1032, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
	PWM4_DUTY_EXT[1:0]	1:0	PWM4 extra 2 bit duty setting.	
22h (103244h)	**REG103244**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_DIV_EXT[7:0]	7:0	PWM0 extra 8 bit divider setting.	
22h (103245h)	**REG103245**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_DIV_EXT[7:0]	7:0	PWM1 extra 8 bit divider setting.	
23h (103246h)	**REG103246**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_DIV_EXT[7:0]	7:0	PWM2 extra 8 bit divider setting.	
23h (103247h)	**REG103247**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_DIV_EXT[7:0]	7:0	PWM3 extra 8 bit divider setting.	
24h (103248h)	**REG103248**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_DIV_EXT[7:0]	7:0	PWM4 extra 8 bit divider setting.	
24h (103249h)	**REG103249**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_DIV_EXT[7:0]	7:0	PWM5 extra 8 bit divider setting.	
28h (103250h)	**REG103250**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_SHIFT[7:0]	7:0	PWM0 rising point shift counter.	
28h (103251h)	**REG103251**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM0_SHIFT[15:8]	7:0	See description of '103250h'.	
29h (103252h)	**REG103252**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWM0_O_CTRL[1:0]	3:2	PWM0 output value control.	
	PWM0_SHIFT[17:16]	1:0	See description of '103250h'.	
2Ah (103254h)	**REG103254**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_SHIFT[7:0]	7:0	PWM1 rising point shift counter.	
2Ah (103255h)	**REG103255**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM1_SHIFT[15:8]	7:0	See description of '103254h'.	
2Bh (103256h)	**REG103256**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWM1_O_CTRL[1:0]	3:2	PWM1 output value control.	
	PWM1_SHIFT[17:16]	1:0	See description of '103254h'.	
2Ch (103258h)	**REG103258**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM2_SHIFT[7:0]	7:0	PWM2 rising point shift counter.	
2Ch	**REG103259**	**7:0**	**Default : 0x00**	**Access : R/W**

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM2_SHIFT[15:8]	7:0	See description of '103258h'.	
2Dh (10325Ah)	**REG10325A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWM2_O_CTRL[1:0]	3:2	PWM2 output value control.	
	PWM2_SHIFT[17:16]	1:0	See description of '103258h'.	
2Eh (10325Ch)	**REG10325C**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_SHIFT[7:0]	7:0	PWM3 rising point shift counter.	
2Eh (10325Dh)	**REG10325D**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM3_SHIFT[15:8]	7:0	See description of '10325Ch'.	
2Fh (10325Eh)	**REG10325E**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWM3_O_CTRL[1:0]	3:2	PWM3 output value control.	
	PWM3_SHIFT[17:16]	1:0	See description of '10325Ch'.	
30h (103260h)	**REG103260**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_SHIFT[7:0]	7:0	PWM4 rising point shift counter.	
30h (103261h)	**REG103261**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM4_SHIFT[15:8]	7:0	See description of '103260h'.	
31h (103262h)	**REG103262**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWM4_O_CTRL[1:0]	3:2	PWM4 output value control.	
	PWM4_SHIFT[17:16]	1:0	See description of '103260h'.	
32h (103264h)	**REG103264**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_SHIFT[7:0]	7:0	PWM5 rising point shift counter.	
32h (103265h)	**REG103265**	**7:0**	**Default : 0x00**	**Access : R/W**
	PWM5_SHIFT[15:8]	7:0	See description of '103264h'.	
33h (103266h)	**REG103266**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	PWM5_O_CTRL[1:0]	3:2	PWM5 output value control.	
	PWM5_SHIFT[17:16]	1:0	See description of '103264h'.	
34h (103268h)	**REG103268**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	NVS_RST_EN5	5	PWM5 enable nvsync reset function.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NVS_RST_EN4	4	PWM4 enable nvsync reset function.	
	NVS_RST_EN3	3	PWM3 enable nvsync reset function.	
	NVS_RST_EN2	2	PWM2 enable nvsync reset function.	
	NVS_RST_EN1	1	PWM1 enable nvsync reset function.	
	NVS_RST_EN0	0	PWM0 enable nvsync reset function.	
34h (103269h)	**REG103269**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	NVS_ALIGN_INV5	5	PWM5 select nvsync align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV4	4	PWM4 select nvsync align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV3	3	PWM3 select nvsync align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV2	2	PWM2 select nvsync align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV1	1	PWM1 select nvsync align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV0	0	PWM0 select nvsync align with left flag inv. 0: Align with left. 1: Align with right.	
35h (10326Ah)	**REG10326A**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	NVS_ALIGN_EN5	5	PWM5 enable nvsync align left flag function.	
	NVS_ALIGN_EN4	4	PWM4 enable nvsync align left flag function.	
	NVS_ALIGN_EN3	3	PWM3 enable nvsync align left flag function.	
	NVS_ALIGN_EN2	2	PWM2 enable nvsync align left flag function.	
	NVS_ALIGN_EN1	1	PWM1 enable nvsync align left flag function.	
	NVS_ALIGN_EN0	0	PWM0 enable nvsync align left flag function.	
36h ~ 37h (10326Ch ~	**-**	**7:0**	**Default : -**	**Access : -**
	-	-	Reserved.	

PWM Register (Bank = 1032, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
38h (103270h)	**REG103270**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	DIFF_P_EN	3	Enable multiple differential pulse whith mode.	
	LC_HIT_SEL[2:0]	2:0	Edge signal selection mux.	
38h (103271h)	**REG103271**	**7:0**	**Default : 0x00**	**Access : R/W**
	V_CNT_SEL	7	V_CNT sel.	
	-	6	Reserved.	
	COMB_PWM0_SEL[1:0]	5:4	PWM0 combine mode.	
	-	3:2	Reserved.	
	PWM_OUT_SHIFT_SEL[1:0]	1:0	PWM output array selection.	
39h (103272h)	**REG103272**	**7:0**	**Default : 0x00**	**Access : RO**
	LINE_CNT_RPT[7:0]	7:0	Line counter report.	
39h (103273h)	**REG103273**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	LINE_CNT_RPT[11:8]	3:0	See description of '103272h'.	
50h (1032A0h)	**REG1032A0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_SHIFT4[7:0]	7:0	PWM0 fourth rising edge.	
50h (1032A1h)	**REG1032A1**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_SHIFT4[15:8]	7:0	See description of '1032A0h'.	
51h (1032A2h)	**REG1032A2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_DUTY4[7:0]	7:0	PWM0 fourth falling edge.	
51h (1032A3h)	**REG1032A3**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_DUTY4[15:8]	7:0	See description of '1032A2h'.	
52h (1032A4h)	**REG1032A4**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_SHIFT4[7:0]	7:0	PWM1 fourth rising edge.	
52h (1032A5h)	**REG1032A5**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_SHIFT4[15:8]	7:0	See description of '1032A4h'.	
53h (1032A6h)	**REG1032A6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_DUTY4[7:0]	7:0	PWM1 fourth falling edge.	
53h (1032A7h)	**REG1032A7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_DUTY4[15:8]	7:0	See description of '1032A6h'.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
54h (1032A8h)	**REG1032A8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_HIT_CNT_ST[7:0]	7:0	PWM0 period hit cnt start for mask/SHIFT2[14:0].	
54h (1032A9h)	**REG1032A9**	**7:0**	**Default : 0x7F**	**Access : R/W**
	PWM0_EN_MASK	7	PWM0 mask enable/SHIFT2[15].	
	PWM0_HIT_CNT_ST[14:8]	6:0	See description of '1032A8h'.	
55h (1032AAh)	**REG1032AA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_HIT_CNT_END[7:0]	7:0	PWM0 period hit cnt end for mask/DUTY2[15:0].	
55h (1032ABh)	**REG1032AB**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_HIT_CNT_END[15:8]	7:0	See description of '1032AAh'.	
56h (1032ACh)	**REG1032AC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_HIT_CNT_ST[7:0]	7:0	PWM1 period hit cnt start for mask/SHIFT2[14:0].	
56h (1032ADh)	**REG1032AD**	**7:0**	**Default : 0x7F**	**Access : R/W**
	PWM1_EN_MASK	7	PWM1 mask enable/SHIFT2[15].	
	PWM1_HIT_CNT_ST[14:8]	6:0	See description of '1032ACh'.	
57h (1032AEh)	**REG1032AE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_HIT_CNT_END[7:0]	7:0	PWM1 period hit cnt end for mask/DUTY2[15:0].	
57h (1032AFh)	**REG1032AF**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_HIT_CNT_END[15:8]	7:0	See description of '1032AEh'.	
58h (1032B0h)	**REG1032B0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM2_HIT_CNT_ST[7:0]	7:0	PWM2 period hit cnt start for mask.	
58h (1032B1h)	**REG1032B1**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PWM2_EN_MASK	7	PWM2 mask enable.	
	-	6:4	Reserved.	
	PWM2_HIT_CNT_ST[11:8]	3:0	See description of '1032B0h'.	
59h (1032B2h)	**REG1032B2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM2_HIT_CNT_END[7:0]	7:0	PWM2 period hit cnt end for mask.	
59h (1032B3h)	**REG1032B3**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PWM2_HIT_CNT_END[11:8]	3:0	See description of '1032B2h'.	
5Ah	**REG1032B4**	**7:0**	**Default : 0xFF**	**Access : R/W**

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM3_HIT_CNT_ST[7:0]	7:0	PWM3 period hit cnt start for mask.	
5Ah (1032B5h)	**REG1032B5**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PWM3_EN_MASK	7	PWM3 mask enable.	
	-	6:4	Reserved.	
	PWM3_HIT_CNT_ST[11:8]	3:0	See description of '1032B4h'.	
5Bh (1032B6h)	**REG1032B6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM3_HIT_CNT_END[7:0]	7:0	PWM3 period hit cnt end for mask.	
5Bh (1032B7h)	**REG1032B7**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PWM3_HIT_CNT_END[11:8]	3:0	See description of '1032B6h'.	
5Ch (1032B8h)	**REG1032B8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM4_HIT_CNT_ST[7:0]	7:0	PWM4 period hit cnt start for mask.	
5Ch (1032B9h)	**REG1032B9**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PWM4_EN_MASK	7	PWM4 mask enable.	
	-	6:4	Reserved.	
	PWM4_HIT_CNT_ST[11:8]	3:0	See description of '1032B8h'.	
5Dh (1032BAh)	**REG1032BA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM4_HIT_CNT_END[7:0]	7:0	PWM4period hit cnt end for mask.	
5Dh (1032BBh)	**REG1032BB**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PWM4_HIT_CNT_END[11:8]	3:0	See description of '1032BAh'.	
5Eh (1032BCh)	**REG1032BC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM5_HIT_CNT_ST[7:0]	7:0	PWM5 period hit cnt start for mask.	
5Eh (1032BDh)	**REG1032BD**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PWM5_EN_MASK	7	PWM5 mask enable.	
	-	6:4	Reserved.	
	PWM5_HIT_CNT_ST[11:8]	3:0	See description of '1032BCh'.	
5Fh (1032BEh)	**REG1032BE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM5_HIT_CNT_END[7:0]	7:0	PWM5 period hit cnt end for mask.	
5Fh (1032BFh)	**REG1032BF**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM5_HIT_CNT_END[11:8]	3:0	See description of '1032BEh'.	
64h (1032C8h)	**REG1032C8**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PWM5_LEFT_MASK	5	PWM5 mask left enable.	
	PWM4_LEFT_MASK	4	PWM4 mask left enable.	
	PWM3_LEFT_MASK	3	PWM3 mask left enable.	
	PWM2_LEFT_MASK	2	PWM2 mask left enable.	
	PWM1_LEFT_MASK	1	PWM1 mask left enable.	
	PWM0_LEFT_MASK	0	PWM0 mask left enable.	
65h (1032CAh)	**REG1032CA**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:6	Reserved.	
	PWM5_INV_LEFT	5	Inverse LEFT_INPUT for right of PWM5.	
	PWM4_INV_LEFT	4	Inverse LEFT_INPUT for right of PWM4.	
	PWM3_INV_LEFT	3	Inverse LEFT_INPUT for right of PWM3.	
	PWM2_INV_LEFT	2	Inverse LEFT_INPUT for right of PWM2.	
	PWM1_INV_LEFT	1	Inverse LEFT_INPUT for right of PWM1.	
	PWM0_INV_LEFT	0	Inverse LEFT_INPUT for right of PWM0.	
66h (1032CCh)	**REG1032CC**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_FP_L_INT3	7	Enable falling pulse interrupt of PWM3 of left.	
	EN_RP_L_INT3	6	Enable rising pulse interrupt of PWM3 of left.	
	EN_FP_L_INT2	5	Enable falling pulse interrupt of PWM2 of left.	
	EN_RP_L_INT2	4	Enable rising pulse interrupt of PWM2 of left.	
	EN_FP_L_INT1	3	Enable falling pulse interrupt of PWM1 of left.	
	EN_RP_L_INT1	2	Enable rising pulse interrupt of PWM1 of left.	
	EN_FP_L_INT0	1	Enable falling pulse interrupt of PWM0 of left.	
	EN_RP_L_INT0	0	Enable rising pulse interrupt of PWM0 of left.	
66h (1032CDh)	**REG1032CD**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	EN_FP_L_INT5	3	Enable falling pulse interrupt of PWM5 of left.	
	EN_RP_L_INT5	2	Enable rising pulse interrupt of PWM5 of left.	
	EN_FP_L_INT4	1	Enable falling pulse interrupt of PWM4 of left.	
	EN_RP_L_INT4	0	Enable rising pulse interrupt of PWM4 of left.	

PWM Register (Bank = 1032, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
67h (1032CEh)	**REG1032CE**	**7:0**	**Default : 0x00**	**Access : R/W**
	EN_FP_R_INT3	7	Enable falling pulse interrupt of PWM3 of right.	
	EN_RP_R_INT3	6	Enable rising pulse interrupt of PWM3 of right.	
	EN_FP_R_INT2	5	Enable falling pulse interrupt of PWM2 of right.	
	EN_RP_R_INT2	4	Enable rising pulse interrupt of PWM2 of right.	
	EN_FP_R_INT1	3	Enable falling pulse interrupt of PWM1 of right.	
	EN_RP_R_INT1	2	Enable rising pulse interrupt of PWM1 of right.	
	EN_FP_R_INT0	1	Enable falling pulse interrupt of PWM0 of right.	
	EN_RP_R_INT0	0	Enable rising pulse interrupt of PWM0 of right.	
67h (1032CFh)	**REG1032CF**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	EN_FP_R_INT5	3	Enable falling pulse interrupt of PWM5 of right.	
	EN_RP_R_INT5	2	Enable rising pulse interrupt of PWM5 of right.	
	EN_FP_R_INT4	1	Enable falling pulse interrupt of PWM4 of right.	
	EN_RP_R_INT4	0	Enable rising pulse interrupt of PWM4 of right.	
68h (1032D0h)	**REG1032D0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_HIT_CNT_ST2[7:0]	7:0	PWM0 period hit cnt start for mask2[11:0]/SHIFT3[14:0].	
68h (1032D1h)	**REG1032D1**	**7:0**	**Default : 0x7F**	**Access : R/W**
	PWM0_EN_LR_MASK	7	PWM0 LR mask enable/SHIFT3[15].	
	PWM0_HIT_CNT_ST2[14:8]	6:0	See description of '1032D0h'.	
69h (1032D2h)	**REG1032D2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_HIT_CNT_END2[7:0]	7:0	PWM0 period hit cnt end for mask2[11:0]/DUTY3[15:0].	
69h (1032D3h)	**REG1032D3**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM0_HIT_CNT_END2[15:8]	7:0	See description of '1032D2h'.	
6Ah (1032D4h)	**REG1032D4**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_HIT_CNT_ST2[7:0]	7:0	PWM1 period hit cnt start for mask2/SHIFT3[14:0].	
6Ah (1032D5h)	**REG1032D5**	**7:0**	**Default : 0x7F**	**Access : R/W**
	PWM1_EN_LR_MASK	7	PWM1 LR mask enable/SHIFT3[15].	
	PWM1_HIT_CNT_ST2[14:8]	6:0	See description of '1032D4h'.	

PWM Register (Bank = 1032, Sub-bank = 01)

Index (Absolute)	Mnemonic	Bit	Description	
6Bh (1032D6h)	**REG1032D6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_HIT_CNT_END2[7:0]	7:0	PWM1 period hit cnt end for mask2/DUTY3[15:0].	
6Bh (1032D7h)	**REG1032D7**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM1_HIT_CNT_END2[15:8]	7:0	See description of '1032D6h'.	
6Ch (1032D8h)	**REG1032D8**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM2_HIT_CNT_ST2[7:0]	7:0	PWM2 period hit cnt start for mask2.	
6Ch (1032D9h)	**REG1032D9**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PWM2_EN_LR_MASK	7	PWM2 LR mask enable.	
	-	6:4	Reserved.	
	PWM2_HIT_CNT_ST2[11:8]	3:0	See description of '1032D8h'.	
6Dh (1032DAh)	**REG1032DA**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM2_HIT_CNT_END2[7:0]	7:0	PWM2 period hit cnt end for mask2.	
6Dh (1032DBh)	**REG1032DB**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PWM2_HIT_CNT_END2[11:8]	3:0	See description of '1032DAh'.	
6Eh (1032DCh)	**REG1032DC**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM3_HIT_CNT_ST2[7:0]	7:0	PWM3 period hit cnt start for mask2.	
6Eh (1032DDh)	**REG1032DD**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PWM3_EN_LR_MASK	7	PWM3 LR mask enable.	
	-	6:4	Reserved.	
	PWM3_HIT_CNT_ST2[11:8]	3:0	See description of '1032DCh'.	
6Fh (1032DEh)	**REG1032DE**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM3_HIT_CNT_END2[7:0]	7:0	PWM3 period hit cnt end for mask2.	
6Fh (1032DFh)	**REG1032DF**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PWM3_HIT_CNT_END2[11:8]	3:0	See description of '1032DEh'.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (1032E0h)	**REG1032E0**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM4_HIT_CNT_ST2[7:0]	7:0	PWM4 period hit cnt start for mask2.	
70h (1032E1h)	**REG1032E1**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PWM4_EN_LR_MASK	7	PWM4 LR mask enable.	
	-	6:4	Reserved.	
	PWM4_HIT_CNT_ST2[11:8]	3:0	See description of '1032E0h'.	
71h (1032E2h)	**REG1032E2**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM4_HIT_CNT_END2[7:0]	7:0	PWM4 period hit cnt end for mask2.	
71h (1032E3h)	**REG1032E3**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PWM4_HIT_CNT_END2[11:8]	3:0	See description of '1032E2h'.	
72h (1032E4h)	**REG1032E4**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM5_HIT_CNT_ST2[7:0]	7:0	PWM5 period hit cnt start for mask2.	
72h (1032E5h)	**REG1032E5**	**7:0**	**Default : 0x0F**	**Access : R/W**
	PWM5_EN_LR_MASK	7	PWM5 LR mask enable.	
	-	6:4	Reserved.	
	PWM5_HIT_CNT_ST2[11:8]	3:0	See description of '1032E4h'.	
73h (1032E6h)	**REG1032E6**	**7:0**	**Default : 0xFF**	**Access : R/W**
	PWM5_HIT_CNT_END2[7:0]	7:0	PWM5 period hit cnt end for mask2.	
73h (1032E7h)	**REG1032E7**	**7:0**	**Default : 0x0F**	**Access : R/W**
	-	7:4	Reserved.	
	PWM5_HIT_CNT_END2[11:8]	3:0	See description of '1032E6h'.	
78h (1032F1h)	**REG1032F1**	**7:0**	**Default : 0x00**	**Access : R/W**
	INV_3D_FLAG	7	Inverse 3D flag.	
	-	6:0	Reserved.	

PM_SLEEP Register (Bank = 0E)

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (0E10h)	**REG0E10**	**7:0**	**Default : 0xFF**	**Access : R/W**
	WK_IRQ_MASK[7:0]	7:0	IRQ mask for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
08h (0E11h)	**REG0E11**	**7:0**	**Default : 0x00**	**Access : R/W**
	WK_IRQ_FORCE[7:0]	7:0	IRQ force for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
09h (0E12h)	**REG0E12**	**7:0**	**Default : 0x00**	**Access : R/W**
	WK_IRQ_POL[7:0]	7:0	IRQ polarity for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
09h (0E13h)	**REG0E13**	**7:0**	**Default : 0x00**	**Access : R/W**
	DEEP_SLEEP	7	1: Deep sleep (using internal crystal). 0: Sleep (using external crystal).	
	WAKEUP_RST_51_EN	6	1: Wake up 8051 from address 0x0. 0: Wake up 8051 from last address.	
	WAKEUP_RST_CHIP_TOP_EN	5	Reset CHIP_TOP w/s 512 cycles of CLK_PM_SLEEP when waking up.	

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HK51_UART0_EN	4	Select UART source via PAD_DDCA. 1: HK MCU51 UART0. 0: DIG_MUX (REG_UART_SEL0).	
	UART_RX_ENABLE	3	1: Enable UART RX via PAD_DDCA for DIG_MUX (REG_UART_SEL0).	
	-	2:0	Reserved.	
0Eh (0E1Ch)	**REG0E1C**	**7:0**	**Default : 0x00**	**Access : RO**
	WK_IRQ_FINAL_STATUS[7:0]	7:0	IRQ final status for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
0Eh (0E1Dh)	**REG0E1D**	**7:0**	**Default : 0x00**	**Access : RO**
	WK_IRQ_RAW_STATUS[7:0]	7:0	IRQ raw status for level wake-up source. [0]: CEC. [1]: SAR. [2]: Reserved. [3]: Sync detection. [4]: RTC0. [5]: Reserved. [6]: AV link. [7]: RTC1.	
12h (0E24h)	**REG0E24**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_LOCK[7:0]	7:0	The password to control the GPIO that is used for controlling external LDO (16'hbabe). The password to enter sleep mode (16'hbabe).	
12h (0E25h)	**REG0E25**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_LOCK[15:8]	7:0	See description of '0E24h'.	
13h (0E26h)	**REG0E26**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_LOCK2[7:0]	7:0	The password to control isolation & reset die-domain (16'hbabe).	
13h (0E27h)	**REG0E27**	**7:0**	**Default : 0x00**	**Access : R/W**
	GPIO_PM_LOCK2[15:8]	7:0	See description of '0E26h'.	

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
1Ch (0E38h)	**REG0E38**	**7:0**	**Default : 0x00**	**Access : R/W**
	AV_LNK_IS_GPIO	7	'd0: Normal use. 'd1: PAD_AV_LNK is used as GPIO.	
	CEC_IS_GPIO	6	'd0: Normal use. 'd1: PAD_CEC is used as GPIO.	
	-	5	Reserved.	
	IR_IS_GPIO	4	'd0: Normal use. 'd1: PAD_IRIN is used as GPIO.	
	-	3:0	Reserved.	
20h (0E40h)	**REG0E40**	**7:0**	**Default : 0x00**	**Access : R/W**
	SW_MCU_CLK	7	Switch CLK MCU by glitch-free clock switch (between CLK_MCU_P and CLK_EXT_XTALI_BUF).	
	-	6	Reserved.	
	CKG_MCU[5:0]	5:0	Clock selection for CLK MCU. [0]: Gate. [1]: Invert. [5:2]: See the following: 'd0: 170 MHz. 'd1: 160MHz. 'd2: 144MHz. 'd3: 123MHz. 'd4: 108MHz. 'd5: MEMPLL_CLK_BUF. 'd6: MEMPLL_CLK_BUF /2. 'd7: CLK_INT_XTALI_BUF. 'd8: CLK_EXT_XTALI_BUF /8. 'd9: 24MHz. 'd10: CLK_INT_XTALI_BUF divided to 1MHz. 'd11: CLK_EXT_XTALI_BUF /16. 'd12: CLK_EXT_XTALI_BUF /2. 'd13: CLK_EXT_XTALI_BUF /4. 'd14: 216MHz. 'd15: 192MHz.	
21h (0E42h)	**REG0E42**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_IR[2:0]	7:5	Clock selection for CLK_IR. [0]: Gate. [1]: Invert. [4:2]: See the following:	

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
	CKG_DDC[4:0]	4:0	Clock selection for CLK_DDC. [0]: Gate. [1]: Invert. [4:2]: See the following: 'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
21h (0E43h)	**REG0E43**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:2	Reserved.	
	CKG_IR[4:3]	1:0	See description of '0E42h'.	
22h (0E44h)	**REG0E44**	**7:0**	**Default : 0x00**	**Access : R/W**
	CKG_SAR[2:0]	7:5	Clock selection for CLK_SAR. [0]: Gate. [1]: Invert. [4:2]: See the following: 'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
	CKG_RTC[4:0]	4:0	Clock selection for CLK_RTC. [0]: Gate. [1]: Invert.	

PM_SLEEP Register (Bank = 0E)

Index (Absolute)	Mnemonic	Bit	Description	
			[4:2]: See the following: 'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
22h (0E45h)	**REG0E45**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7	Reserved.	
	CKG_PM_SLEEP[4:0]	6:2	Clock selection for CLK_PM_SLEEP (cannot be either inversed or gated). [4:2]: See the following: 'd0: CLK_EXT_XTALI_BUF. 'd1: CLK_INT_XTALI_BUF. 'd2: CLK_EXT_XTALI_BUF /8. 'd3: CLK_EXT_XTALI_BUF divided to 1MHz. 'd4: CLK_INT_XTALI_BUF /4. 'd5: CLK_EXT_XTALI_BUF /16. 'd6: CLK_EXT_XTALI_BUF /2. 'd7: CLK_EXT_XTALI_BUF /4.	
	CKG_SAR[4:3]	1:0	See description of '0E44h'.	
23h (0E46h)	**REG0E46**	**7:0**	**Default : 0x00**	**Access : R/W**
	-	7:4	Reserved.	
	CKG_CEC[3:0]	3:0	Clock selection for CLK_CEC. [0]: Gate. [1]: Invert. [3:2]: See the following: 'd0: CLK_EXT_XTALI_BUF divided to 1MHz. 'd1: CLK_INT_XTALI_BUF /4. 'd2: CLK_INT_XTALI_BUF. 'd3: 0.	
27h (0E4Eh)	**REG0E4E**	**7:0**	**Default : 0x0F**	**Access : R/W**
	HOTPLUG_OUT[3:0]	7:4	Hot plug out. [0]: Hot plug A. [1]: Hot plug B. [2]: Hot plug C.	

PM_SLEEP Register (Bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[3]: Hot plug D.	
	HOTPLUG_OEN[3:0]	3:0	Hot plug OEN. [0]: Hot plug A. [1]: Hot plug B. [2]: Hot plug C. [3]: Hot plug D.	
27h (0E4Fh)	**REG0E4F**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	HOTPLUG_IN[3:0]	3:0	Hot plug in. [0]: Hot plug A. [1]: Hot plug B. [2]: Hot plug C. [3]: Hot plug D.	
30h (0E60h)	**REG0E60**	**7:0**	**Default : 0x20**	**Access : R/W**
	-	7:6	Reserved.	
	EXT_XTALI_SEL[1:0]	5:4	External crystal settings (driving strength).	
	-	3	Reserved.	
	INT_XTALI_DEGLITCH[2:0]	2:0	Test bits for internal crystal clock.	
30h (0E61h)	**REG0E61**	**7:0**	**Default : 0x18**	**Access : R/W**
	-	7	Reserved.	
	EXT_XTALI_AMP_GAIN[1:0]	6:5	External crystal amplitude gain.	
	EXT_XTALI_FRSEL	4	External crystal frequency selection.	
	INT_XTALI_FREQ_TUNE[3:0]	3:0	Frequency tune for internal clock.	
31h (0E63h)	**REG0E63**	**7:0**	**Default : 0x00**	**Access : R/W**
	RTC1_SW_RST	7	Software reset (active high) for RTC1.	
	RTC0_SW_RST	6	Software reset (active high) for RTC0.	
	-	5	Reserved.	
	CEC_SW_RST	4	Software reset (active high) for CEC.	
	AV_LNK_SW_RST	3	Software reset (active high) for AV_LNK_TOP.	
	SAR_SW_RST	2	Software reset (active high) for SAR_TOP.	
	-	1:0	Reserved.	
32h (0E64h)	**REG0E64**	**7:0**	**Default : 0x00**	**Access : R/W**
	XTAL_OFF_KEY[7:0]	7:0	Key to turn off external crystal (32'h9f8e9f8e).	
32h	**REG0E65**	**7:0**	**Default : 0x00**	**Access : R/W**

PM_SLEEP Register (Bank = 0E)

Index (Absolute)	Mnemonic	Bit	Description	
	XTAL_OFF_KEY[15:8]	7:0	See description of '0E64h'.	
33h (0E66h)	**REG0E66**	**7:0**	**Default : 0x00**	**Access : R/W**
	XTAL_OFF_KEY[23:16]	7:0	See description of '0E64h'.	
33h (0E67h)	**REG0E67**	**7:0**	**Default : 0x00**	**Access : R/W**
	XTAL_OFF_KEY[31:24]	7:0	See description of '0E64h'.	
35h (0E6Bh)	**REG0E6B**	**7:0**	**Default : 0x00**	**Access : R/W**
	TESTBUS_SW[1:0]	7:6	Testbus switch.	
	ISO_CONTROL[1:0]	5:4	[0]: Isolation control selection. 0: By PM_ATOP. 1: By software. [1]: Isolation control. 0: Not isolate. 1: Isolate.	
	UART_IS_GPIO[3:0]	3:0	[0]: Switch GPIO_PM[5] to HK51's UART_RX1 and GPIO_PM[8] to HK51's UART_TX1. [1]: Switch GPIO_PM[5] to HK51's UART_RX1 and GPIO_PM[1] to HK51's UART_TX1. [3:2]: Reserved.	
50h (0EA0h)	**REG0EA0**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[7:0]	7:0	Key to off RIU_CKSUM_PROT (h51685168).	
50h (0EA1h)	**REG0EA1**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[15:8]	7:0	See description of '0EA0h'.	
51h (0EA2h)	**REG0EA2**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[23:16]	7:0	See description of '0EA0h'.	
51h (0EA3h)	**REG0EA3**	**7:0**	**Default : 0x00**	**Access : R/W**
	RIU_CKSUM_PROT_OFF[31:24]	7:0	See description of '0EA0h'.	
60h (0EC0h)	**REG0EC0**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:2	Reserved.	
	BOND_STAT[1:0]	1:0	Bonding status. [0]: Clock selection. [1]: Security.	
61h (0EC2h)	**REG0EC2**	**7:0**	**Default : 0x00**	**Access : RO**
	-	7:4	Reserved.	
	CHIP_TOP_POWERGOOD_DEGLITCH	3	DVDD_CORE_PWRGD after de-glitch and ISO_CONTROL.	

PM_SLEEP Register (Bank = 0E)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	CHIP_TOP_POWERGOOD[2:0]	2:0	CHIP_TOP'S powergood from PM_ATOP. [0]: NODIE_PWRGD. [1]: DVDD_CORE_PWRGD. [2]: VD33_SHUTDN_PWRGD.

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
5/10/2011		Ÿ Created first version.