Attention Please: Under the technology license agreement between MStar and Dolby/SRS/BBE/DivX/Microsoft/QSound, MStar is obliged not to provide samples that incorporate Dolby/SRS/BBE/DivX/Microsoft/QSound technology to any third party who is not a qualified licensee of Dolby/SRS/BBE/DivX/Microsoft/QSound respectively.

FEATURES

MST6M182VG, a single chip Multimedia TV SoC that supports TV channel decoding, and media-centre functionality enabled by a high performance AV CODEC and CPU

Key features includes,

1. *Analog TV Front-End Demodulator*
2. *A Multi-Standard A/V Format Decoder*
3. *The MStarACE-5 Video Processor*
4. *Home Theater Sound Processor*
5. *Peripheral and Power Management*

- High Performance Micro-processor
  - High speed/performance 32-bit RISC CPU
  - Two full duplex UARTs
  - Supports USB and ISP programming
  - DMA Engine
- MPEG-2 Video Decoder
  - ISO/IEC 13818-2 MPEG-2 video MP@HL
  - Automatic frame rate conversion
  - Supports resolution up to HDTV (1080i, 720p) and SDTV
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding
  - Supports resolutions up to HDTV (1080p@30fps)
  - Supports DivX[1] Home Theater & HD profiles[Optional]
- RealMedia Decoder
  - Supports maximum resolution up to 1080p@30fps
  - Supports RV8, RV9, RV10, RA8-LBR and HE-AAC decoders
  - Supports file formats with RM and RMVB
  - Supports Picture Re-sampling
  - Supports in-loop de-block for B-frame
- Hardware JPEG
  - Supports sequential mode, single scan
  - Supports both color and grayscale pictures
  - Following the file header scan the hardware decoder fully handles the decode process
  - Supports programmable Region of Interest (ROI)
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2, 1/4, 1/8
  - Supports picture rotation
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - Three configurable CVBS & Y/C S-video inputs
  - Supports Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE
- Multi-Standard TV Sound Processor
  - SIF audio decoding
  - Supports BTSC/A2/EIA-J demodulation
  - Supports FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC/ EIA-J mode
  - Supports Mono/Stereo/Dual in A2 mode
  - Built-in audio sampling rate conversion (SRC)
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
  - Advanced sound processing options available, for example: Dolby[2], SRS[3], BBE[4], QSound[5]
  - Supports digital audio format decoding:
    - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3) [Optional], AAC-LC, WMA
    - Dolby Digital Plus [Optional]

[1] **Trademark of DivX, Inc.**

[Optional] **Please see Ordering Guide for details.**

[2] **Trademark of Dolby Laboratories**

[3] **Trademark of SRS Labs, Inc.**

[4] **Registered trademark of BBE Sound, Inc.**

[5] **Registered trademark of QSound Labs, Inc.**

- Audio Interface
  - Four L/R audio line-inputs
  - Two L/R outputs for main speakers and additional line-outputs
  - I2S digital audio input & output
  - S/PDIF digital audio output
  - HDMI audio channel processing
  - Programmable delay for audio/video synchronization
- Analog RGB Compliant Input Ports
  - Two analog ports support up to 1080P
  - Supports PC RGB input up to SXGA@75Hz
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG Sync-on-Green
  - Automatic color calibration
  - AV-link support
- Analogue RGB Auto-Configuration & Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
  - Sync Detection for H/V Sync
- DVI/HDCP/HDMI Compliant Input Port
  - One HDMI/DVI Input port
  - HDMI 1.3/1.4 Compliant
  - HDCP 1.2 Compliant
  - 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
  - Supports CEC
  - Supports HDMI 3D format input
  - Supports HDMI 4Kx2K input
  - Supports HDMI ARC
  - Single link DVI 1.0 compliant
  - Robust receiver with excellent long-cable support
- MStar Advanced Color Engine (MStarACE-5)
  - Fully programmable multi-function scaling engine
    - Nonlinear video scaling supports various modes including Panorama
    - Supports dynamic scaling for RM, VC-1
  - Advanced video processing engine
    - 3D video deinterlacer with edge and artifact smoother
    - Edge-oriented deinterlacer with edge and artifact smoother
    - Automatic 3:2/2:2/M:N pull-down detection and recovery
    - 3D noise reduction for lousy air/cable input
    - Motion adaptive SNR
    - Arbitrary frame rate conversion
  - MStar Professional Picture Enhancement:
    - Dynamic brilliant and fresh color
    - Dynamic *Blue Stretch*
    - Intensified contrast and details
    - Dynamic *Vivid Skin*
    - Dynamic sharpened Luma/Chroma edges
    - Global and local dynamic depth of field perception
    - Accurate and independent color control
    - Supports sRGB and xvYCC color processing
    - Supports HDMI 1.3 deep color format
  - Programmable 12-bit RGB gamma CLUT

- Output Interface
  - Single/dual link 8/10-bit Mini-LVDS output
  - Supports panel resolution up to Full-HD (1920x1080) @ 60Hz
  - Programmable TCON control signals generation
  - Supports TH/TI format
  - Supports dithering options to 6/8-bit output
  - Spread spectrum output for EMI suppression
  - Supports 60Hz 3D passive panel (Line alternative mode)
- CVBS Video Outputs
  - Supports CVBS bypass output
- 3D-like Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill, text draw and trapezoid draw
  - BitBlt, stretch BitBlt, trapezoid BitBlt, mirror BitBlt and rotate BitBlt
  - Supports alpha and destination alpha compare
  - Raster Operation (ROP)
  - Support Porter-Duff
- VIF Demodulator
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
  - Digital low IF architecture
  - Audio/Video dual-path processor
  - Stepped-gain PGA with 25 dB tuning range and 1 dB tuning resolution
  - Maximum IF gain of 37 dB
  - Programmable TOP to accommodate different tuner gain and SAW filter insertion loss to optimize noise and linearity performance
  - Multi-standard processing with single SAW or sawless
  - Supports silicon tuner low IF output architecture
- Connectivity
  - Two USB 2.0 host ports
  - USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Miscellaneous
  - Bootable SPI interface with serial flash support
  - Power control module in standby mode
  - 13.5x13.5 BGA package
  - Operating Voltages: 1.26V (core), 1.8V (DDR2), 2.5V and 3.3V (I/O and analog)

GENERAL DESCRIPTION

The MST6M182VG is MStar's most up-to-date system-on-chip solution for flat panel integrated digital television products. Building on the success of MStar's preceding SOC series, the MST6M182VG provides most cost-effective solution for multimedia TV application with creative and attractive features exclusively presented by MStar.

The MST6M182VG integrates TV/multi-media all-purpose AV decoder, VIF demodulator, and advanced Sound/Video processor into a single device. This allows the overall BOM to be reduced significantly making the MST6M182VG a very competitive multi-media TV solution.

The powerful multimedia A/V decoder inside MST6M182VG is hosted with a dedicated hardware video codec engine to secure fast and stable video stream playback, an audio application specific DSP for digital audio format decoding and advanced sound effects, and a high performance RISC CPU to manipulate all possible user playback and control activities. With extendable USB 2.0 connectivity, an MST6M182VG based system can be switched to a high quality media-center in a simple manner.

For standard users, the MST6M182VG provides multi-standard analog TV support with adaptive 3D video decoding and VBI data extraction. The build-in audio decoder is capable of decoding FM, AM, A2, BTSC and EIA-J sound standards. The MST6M182VG supplies all the necessary A/V inputs and outputs to complete a receiver design including a HDMI receiver and component video ADC. All input selection multiplexed for video and audio are integrated, including full SCART support with CVBS output. The equipped MStar MStarACE-5 color engine is the latest masterpiece of MStar famous color engine series providing excellent video and picture quality in Full-HD and large-scale displaying system.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MST6M182VG has an ultra low power standby mode.

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		TBD		LSB
Integral Nonlinearity		TBD		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum		0.5		V p-p
Maximum		TBD		V p-p
Input Bias Current			1	uA
SWITCHING PERFORMANCE				
Maximum Conversion Rate	170			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		170	MHz
PLL Jitter		TBD		ps p-p
Sampling Phase Tempco		TBD		ps/°C
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		0.2		V
Output High		1.2		V
AUDIO				
ADC Input		2.8		V p-p
DAC Output		2.8		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p

Parameter	Min	Typ	Max	Unit
SAR ADC Input	0		3.3	V
FB ADC Input*	0		1.2	V

Specifications subject to change without notice.
Note: Input full scale is 1.2V, but input range is 0 ~ 3.3V.

Recommended Operating Power Conditions

Parameter	Symbol	Min	Typ	Max	Units
3.3V Supply Voltages	V_{VDD_33}	3.14		3.46	V
1.8V Supply Voltages	$V_{VDD\ 18}$	1.70		1.90	V
1.26V Supply Voltages	V_{VDD_126}	1.20		1.32	V

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
3.3V Supply Voltages	V_{VDD_33}		3.6	V
1.8V Supply Voltages	V_{VDD_18}		1.98	V
1.26V Supply Voltages	V_{VDD_126}		1.32	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{STG}	-40	150	°C
Junction Temperature	T_J		150	°C

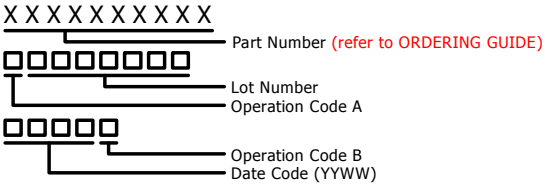
Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
MST6M182VG-LF	0°C to +70°C	BGA	200
MST6M182VG-LF-XX	0°C to +70°C	BGA	200

Note:
XX suffix represents advanced features. Please contact MStar sales for details.

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. MST6M182VG comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
MST6M182VG_ds_v01	• Initial release	Aug 2011
MST6M182VG_ds_v02	• Updated Features	Aug 2011

REGISTER DESCRIPTION

Scaler 1 Register (Bank = 102F)

GOP_INT Register (Bank = 102F, Sub-bank = 00)

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (102F00h)	**REG102F00**	**7:0**	**Default: 0xFF**	**Access: R/W**
	SC_RIU_BANK[7:0]	7:0	Bank selection for scaler.	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	DBL_VS	2	Double buffer load by Vsync.	
	DBL_M	1	Double buffer load by manual.	
	DBC_EN	0	Double buffer enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	SWRST1[7:0]	7:0	Reset control. SWRST1[7]: OSCCLK domain. SWRST1[6]: FCLK domain. SWRST1[5]. SWRST1[4]: IP, include F1 and F2. SWRST1[3]: OP include OP1, VIP and VOP. SWRST1[2]: IP_F2. SWRST1[1]: IP_F1. SWRST1[0]: All engines.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	PDMD[1:0]	1:0	PowerDown mode. 01: IDCLK. Others: IDCLK and ODCLK.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	VSINT_EDGE	1	OP2 VS INT Edge. 1: Tailing. 0: Leading.	
	IPVSINT_EDGE	0	IP VS INT Edge. 1: Tailing. 0: Leading.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CHG_HMD	0	CHG_HMD: H Change Mode for INT. 0: Only in Leading/Tailing of CHG Period. 1: Every Line Gen INT Pulse during CHG Period.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	IP_SYNC_TO_GOP_SEL[1:0]	7:6	Sync signal to GOP select. 01: IP channel 1. 10: IP channel 2.	
	GOP2IP_EN	5	GOP blending to IP enable.	
	-	4:0	Reserved.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GOP2IP_DATA_SEL[1:0]	5:4	Select GOP source for IP. 01: GOP 1. 10: GOP 2.	
	-	3:0	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	COP_EN	7	Enable cop for VOP2.	
	GOP2_EN	6	Enable GOP_2 for VOP2.	
	GOP1_EN	5	Enable GOP_1 for VOP2.	
	-	4:0	Reserved.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	TST_MUX_SEL[4:0]	4:0	Test mux selection.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: RO**
	IRQ_FINAL_STATUS_7_0[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: RO**
	IRQ_FINAL_STATUS_15_8[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: IPHCS_DET_INT_F1.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: RO**
	IRQ_FINAL_STATUS_23_16[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: RO**
	IRQ_FINAL_STATUS_31_24[7:0]	7:0	The final status of interrupt in SC_TOP. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_CLEAR_7_0[7:0]	7:0	Clear interrupt for. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	
12h	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F25h)	IRQ_CLEAR_15_8[7:0]	7:0	Clear interrupt for. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_CLEAR_23_16[7:0]	7:0	Clear interrupt for. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_CLEAR_31_24[7:0]	7:0	Clear interrupt for. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0xFF**	**Access: R/W**
	IRQ_MASK_7_0[7:0]	7:0	Mask IRQ. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A. D[0]: N/A.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0xFF**	**Access: R/W**
	IRQ_MASK_15_8[7:0]	7:0	Mask IRQ. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	IRQ_MASK_23_15[7:0]	7:0	Mask IRQ. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0xFF**	**Access: R/W**
	IRQ_MASK_31_24[7:0]	7:0	Mask IRQ. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_FORCE_7_0[7:0]	7:0	Force a fake interrupt. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A. D[2]: N/A. D[1]: N/A.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[0]: N/A.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_FORCE_15_8[7:0]	7:0	Force a fake interrupt. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_FORCE_23_16[7:0]	7:0	Force a fake interrupt. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	IRQ_FORCE_31_24[7:0]	7:0	Force a fake interrupt. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: RO**
	IRQ_RAW_STATUS_7_0[7:0]	7:0	The raw status of interrupt source. D[7]: VTT_CHG_INT_F1. D[6]: VTT_LOSE_INT_F2. D[5]: VSINT. D[4]: TUNE_FAIL_P. D[3]: N/A.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			D[2]: N/A. D[1]: N/A. D[0]: N/A.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: RO**
	IRQ_RAW_STATUS_15_8[7:0]	7:0	The raw status of interrupt source. D[7]: IPHCS_DET_INT_F1. D[6]: IPHCS_DET_INT_F2. D[5]: IPVS_SB_INT_F1. D[4]: IPVS_SB_INT_F2. D[3]: JITTER_INT_F1. D[2]: JITTER_INT_F2. D[1]: VS_LOSE_INT_F1. D[0]: VS_LOSE_INT_F2.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: RO**
	IRQ_RAW_STATUS_23_16[7:0]	7:0	The raw status of interrupt source. D[7]: DVI_CK_LOSE_INT_F1. D[6]: DVI_CK_LOSE_INT_F2. D[5]: HS_LOSE_INT_F1. D[4]: HS_LOSE_INT_F2. D[3]: HTT_CHG_INT_F1. D[2]: HTT_CHG_INT_F2. D[1]: IPHCS1_DET_INT_F1. D[0]: IPHCS1_DET_INT_F2.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: RO**
	IRQ_RAW_STATUS_31_24[7:0]	7:0	The raw status of interrupt source. D[7]: ATG_READY_INT_F1. D[6]: ATG_READY_INT_F2. D[5]: ATP_READY_INT_F1. D[4]: ATP_READY_INT_F2. D[3]: ATS_READY_INT_F1. D[2]: ATS_READY_INT_F2. D[1]: CSOG_INT_F1. D[0]: CSOG_INT_F2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x00**	**Access: RO**
	BIST_FAIL_0[7:0]	7:0	BIST fail status for LBI.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:3	Reserved.	
	BIST_FAIL_0[10:8]	2:0	See description of '102F40h'.	

GOP_INT Register (Bank = 102F, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7	Reserved.	
	BIST_FAIL_1[6:0]	6:0	BIST fail status for OP1.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: RO**
	BIST_FAIL_2[7:0]	7:0	BIST fail status for VOP, VIP.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:5	Reserved.	
	BIST_FAIL_2[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: RO**
	BIST_FAIL_3[7:0]	7:0	BIST fail status for SCF.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:1	Reserved.	
	BIST_FAIL_3[8]	0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: RO**
	BIST_FAIL_4[7:0]	7:0	BIST fail status for OD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:6	Reserved.	
	BIST_FAIL_4[13:8]	5:0	See description of '102F48h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0xE1**	**Access: R/W**
	WDT_VSEL[3:0]	7:4	Vsync lose watch dog timer flag select.	
	WDT_HSEL[3:0]	3:0	Hsync lose watch dog timer flag select.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	WDT_EN	0	H/V sync lose watch dog timer count enable.	

IP1_M Register (Bank = 102F, Sub-bank = 01)

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x83**	**Access: R/W**
	NO_SIGNAL	7	Input source enable. 0: Enable. 1: Disable; output is free-run.	
	AUTO_DETSRC[1:0]	6:5	Input Sync Type. 00: Auto detected. 01: Input is separated HSYNC and VSYNC. 10: Input is Composite sync. 11: Input is sync-on-green (SOG).	
	COMP_SRC	4	CSYNC/SOG select (only useful when STYPE = 00). 0: CSYNC. 1: SOG.	
	CSC_EN	3	Input CSC function. 0: Disable (RGB -> RGB, default). 1: Enable (RGB -> YCbCr).	
	SOURCE_SELECT[2:0]	2:0	Input Source Select. 000: Analog 1. 001: Analog 2. 010: Analog 3. 011: DVI. 100: Video. 101: HDTV. 111: HDMI.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	FVDO_DIVSEL	7	Force Input Clock Divide Function. 0: Disable (Auto selected by h/W, used when input is video, default). 1: Enable (use 02h[14:12] as divider).	
	-	6	Reserved.	
	VD_PORT_SEL	5	External VD Port. 0: Port 0. 1: Port 1.	
	VD_ITU	4	VD ITU656 out, and Digital In for scaler.	
	VDEXT_SYNMD	3	External VD Using Sync. 0: Sync is Generated from Data Internally. 1: Sync from External Source.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	YCBCR_EN	2	Input Source is YPbPr Format.	
	VIDEO_SELECT[1:0]	1:0	Video Port Select. 00: External 8/10 bits video port. 01: Internal video decoder mode A. 10: External 16/20 bits video port. 11: Internal video decoder mode B.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x18**	**Access: R/W**
	DIRECT_DE	7	Digital Input Horizontal Sample Range. 0: Use DE as sample range, only V position can be adjusted. 1: Use SPRHST and SPRHDC as sample range, both H and V position can be adjusted.	
	DE_ONLY_ORI	6	DE Only. HSYNC and VSYNC are ignored. 0: Disable. 1: Enable.	
	VS_DLYMD	5	Input VSYNC Delay select. 0: Delay 1/4 input HSYNC. 1: No delay.	
	HS_REFEG	4	Input HSYNC reference edge select. 0: From HSYNC leading edge. 1: From HSYNC tailing edge.	
	VS_REFEG	3	Input VSYNC reference edge select. 0: From VSYNC leading edge. 1: From VSYNC tailing edge.	
	EXTEND_EARLY_LN	2	Early Sample Line Select. 0: 8 lines. 1: 16 lines.	
	VWRAP	1	Input image Vertical wrap. 0: Disable. 1: Enable.	
	HARDWARERAP	0	Input image Horizontal wrap. 0: Disable. 1: Enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x80**	**Access: R/W**
	FRCV	7	Source Sync Enable. 1: Display will adaptively follow the Source, if Display Select this source. 0: Display Free Run, if Display Select this source.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AUTO_UNLOCK	6	Auto Lost Sync Detect Enable. When Mode Change, the Sync Process for this window will be stop until Set Source Sync Enable = 1 again. This is the backup solution for Coast.	
	FREE_FOLLOW	5	No memory bank control (used when FRCV=1).	
	FRC_FREEMD	4	Force output odd/even toggle when 2DDi for interlace input.	
	DATA10BIT	3	Set 10-bit input mode.	
	DATA8_ROUND	2	Use rounding for 8-bit input mode.	
	VD16_C_AHEAD	1	Video 16-bit mode fine tune Y/C order.	
	RESERVED	0		
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x01**	**Access: R/W**
	SPRANGE_VST[7:0]	7:0	Image vertical sample start point, count by input HSYNC.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SPRANGE_VST[10:8]	2:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x01**	**Access: R/W**
	SPRANGE_HST[7:0]	7:0	Image horizontal sample start point, count by input HSYNC.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SPRANGE_HST[10:8]	2:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x10**	**Access: R/W**
	SPRANGE_VDC[7:0]	7:0	Image vertical resolution (vertical display enable area count by line).	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SPRANGE_VDC[10:8]	2:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x10**	**Access: R/W**
	SPRANGE_HDC[7:0]	7:0	Image horizontal resolution (vertical display enable area count by line).	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SPRANGE_HDC[10:8]	2:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x20**	**Access: R/W**
	FOSVDCNT_MD	7	Force Ext VD count adjustment Mode.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	VDCNT[1:0]	6:5	VD count for adjusting order of UV, count from Hsync to first pixel UV order. 00: Normal. 01: 1. 10: 2. 11: 3.	
	VD_NOMASK	4	EAV/SAV Mask for Video. 0: Mask. 1: No mask.	
	IHSU	3	Input Hsync Usage. When ISEL = 000 or 001 or 010: (ADC) 0: Use Hsync to perform mode detection, HSOUT from ADC to sample pixel. 1: Use Hsync only. When ISEL = 011: (DVI) 0: Normal. 1: Enable DE Ahead/Delay adjust. When ISEL = 100: (VD) 0: Normal. 1: Output Black at blanking.	
	INTLAC_LOCKAVG	2	Field time average (Interlace Lock Position Average).	
	VDO_YC_SWAP	1	Y/C Swap (only useful for 16/20-bit video inputs). 0: Normal. 1: Y/C swap.	
	VDO_ML_SWAP	0	MSB/LSB Swap. 0: Normal. 1: MSB/LSB swap.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	VDCLK_INV	7	External VD Port 0 Clock Inverse.	
	-	6	Reserved.	
	YPBPR_HS_SEPMD	5	YPbPr HSYNC Select Mode to Mode Detector. 0: Use Separate Hs for Coast Period. 1: Use PLL Hsout for Coast Period.	
	-	4	Reserved.	
	VDCLK_DLY[3:0]	3:0	External VD Port 0 Clock delay.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	CSC_DITHEN	7	CSC Dithering Enable when 02h[3]=1.	
	INTLAC_DET_EDGE	6	Interlace detect Reference Edge. 0: Leading edge. 1: Tailing edge.	
	FILED_ABSMD	5	Interlace detect using Middle Point Method. (03h[5]=0 is better).	
	INTLAC_AUTO	4	Interlace /Progressive Manual Switch mode. 0: Auto Switch VST(04), VDC (06). 1: Disable Auto Switch VST(04), VDC(06).	
	Y_LOCK[3:0]	3:0	Early Sample Line for Capture Port Frame information Switch. 0000: 8 Lines Ahead from SPRANGE_VST. 0001: 1 Line Ahead from SPRANGE_VST. 0010: 2 Lines Ahead from SPRANGE_VST. 0011: 3 Lines Ahead from SPRANGE_VST. .. 1111: 15 Lines Ahead from SPRANGE_VST.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	IP_INT_SEL[7:0]	7:0	No load (Reserved).	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_MIR	7	H Mirror Enable.	
	-	6:0	Reserved.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	AUTO_INTLAC_INV	1	Auto Filed Switch Mode Filed Inverse.	
	AUTO_INTLAC_MD	0	Auto Field Switch Mode for Vtt = 2N+1 and 4N+1.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**
	CS_DET_CNT[7:0]	7:0	Composite Sync Separate Decision Count. 0: Hardware Auto Decide. 1: Software Program.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	OVERSAP_EN	7	FIR Down Sample Enable, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5-tap support. 1: Down Enable, ratio / tap depend on 0D[3:0].	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OVERSAP_PHS[2:0]	6:4	FIR Down Sample Divider Phase.	
	OVERSAP_CNT[3:0]	3:0	FIR Down Sample Divider, for FIR Double rate 2x -> 1x after FIR Purpose. 0: No down, 5 taps. 1: 2 to 1 down, 11 taps. Others: Reserved. For ExtVD is CCIR656, set to 0 and OVERSAP_EN = 1 will do 2X oversample.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	ATG_HIR	7	Max value flag for R channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_HIG	6	Max value flag for G channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_HIB	5	Max value flag for B channel (Read Only). 0: Normal. 1: Max value (255) value when ATG_DATA_MD = 0. Output over max value (255) when ATG_DATA_MD = 1.	
	ATG_CALMD	4	ADC Calibration Enable. 0: Disable. 1: Reserved.	
	ATG_DATA_MD	3	Auto Gain Result selection. 0: Output has max/min value. 1: Output is overflow/underflow.	
	ATG_HISMD	2	Auto Gain Mode. 0: Normal mode (result will be cleared every frame). 1: History mode (result remains not cleared till ATG_EN = 0).	
	ATG_READY	1	Auto Gain Result Ready. 0: Result not ready. 1: Result ready.	
	ATG_EN	0	Auto Gain Function Enable. 0: Disable. 1: Enable.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	ATG_10BIT	7	Auto gain 10-bit mode.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	AV_DET	6	AV Detect for Cb Cr. 0: CbCr Range is define by 03[2]. YCBCR_EN. 1: Cb Cr Min is define in 89 ATP_GTH. Cb Cr Max is defined in 8A ATP_TH.	
	-	5:3	Reserved.	
	ATG_UPR	2	Min value flag for R channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPG	1	Min value flag for G channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
	ATG_UPB	0	Min value flag for B channel. 0: Normal. 1: Min value present when ATG_CALMD = 0, ATG_DATA_MD = 0. Calibration result (needs to decrease offset) when ACE = 1.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	AUTO_COAST	7	Auto Coast enable when mode change. 0: Disable. 1: Enable.	
	OP2_COAST	6	Coast Status (Read only). 0: Coast is inactive. 1: Coast is active (free run).	
	ATPSEL[1:0]	5:4	Auto Phase Value Select (read from registers 0x8C~0x8F). 00: R/G/B total value. 01: Only R value. 10: Only G value. 11: Only B value.	
	PIP_SW_DOUBLE	3	Double Sample for. 1. VD. 2. Ext VD 656 Format. 3. Ext 444 Format. The Purpose is to provide 2X Pixel Rate.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			For FIR Down Sample, and give 11 TAP Filter.	
	ATGSEL[2:0]	2:0	Select Auto Gain Report for Reg 7D. 000: Minimum R value. 001: Minimum G value. 010: Minimum G value. 011: Maximum R value. 100: Maximum G value. 101: Maximum B value. 11x: Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	JIT_R	7	Jitter function Left / Right result for 86h and 87h. 0: Left result. 1: Right result.	
	JIT_SWCLR_SB	6	Jitter Software clear. 0: Not clear. 1: Clear.	
	-	5	Reserved.	
	JITTER_HISMD	4	Jitter function Mode. 0: Update every frame. 1: Keep the history value.	
	JITTER	3	JITTER function Result. 0: No jitter. 1: Jitter present.	
	ATS_HISMD	2	Auto position function Mode. 0: Update every frame. 1: Keep the history value.	
	ATS_READY	1	Auto position result Ready. 0: Result ready. 1: Result not ready.	
	ATS_EN	0	Auto position function Enable. 0: Disable. 1: Enable. Disable-to-enable needs at least 2 frame apart for ready bit to settle.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	THOLD[3:0]	7:4	Auto position Valid Data Value. 0000: Valid if data >= 0000 0000. 0001: Valid if data >= 0001 0000.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0010: Valid if data >= 0010 0000. ... 1111: Valid if data >= 1111 0000.	
	-	3:1	Reserved.	
	ATS_PIXMD	0	Auto Position Force Pixel Mode. 0: DE or Pixel decided by the Source. 1: Force Pixel Mode.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: RO**
	ATGSEL_VALUE[7:0]	7:0	Auto Gain Value. (Selected by register 0Fh[2:0]).	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:2	Reserved.	
	ATGSEL_VALUE[9:8]	1:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: RO**
	ATS_VSTDBUF[7:0]	7:0	Auto position detected result Vertical Starting point.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:3	Reserved.	
	ATS_VSTDBUF[10:8]	2:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: RO**
	ATS_HSTDBUF[7:0]	7:0	Auto position detected result Horizontal Starting point.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	ATS_HSTDBUF[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: RO**
	ATS_VEDDBUF[7:0]	7:0	Auto position detected result Vertical End point.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:3	Reserved.	
	ATS_VEDDBUF[10:8]	2:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: RO**
	ATS_HEDDBUF[7:0]	7:0	Auto position detected result Horizontal End point.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	ATS_HEDDBUF[11:8]	3:0	See description of '102F2Ah'.	
16h	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: RO**

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Ch)	REG_JLST[7:0]	7:0	Jitter function detected Left/Right most point state (previous frame) depend on REG_10H[7] (default = 7ffh).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	REG_JLST[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	L12_LIMIT_EN	5	Background Noise reduction Enable. 0: Disable. 1: Enable.	
	HIPX_LIMIT_EN	4	High level Noise reduction Enable. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	PIX_TH[2:0]	2:0	Auto Noise Level. 111: Noise level = 16.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x01**	**Access: R/W**
	ATP_GTH[7:0]	7:0	Auto Phase Gray scale Threshold for ATP[23:16] when ATPN[31:24] = 0.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x10**	**Access: R/W**
	ATP_TH[7:0]	7:0	Auto Phase Text Threshold for ATP[31:24] .	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7	Reserved.	
	ATP_GRY	6	Auto Phase Gray scale detect (Read Only).	
	ATP_TXT	5	Auto Phase Text detect (Read Only).	
	ATPMASK[2:0]	4:2	Auto Phase Nose Mask. 000: Mask 0 bit, default value. 001: Mask 1 bit. 010: Mask 2 bits. 011: Mask 3 bits. 100: Mask 4 bits. 101: Mask 5 bits. 110: Mask 6 bits. 111: Mask 7 bits.	
	ATP_READY	1	Auto Phase Result ready. 0: Result not ready.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Result ready.	
	ATP_EN	0	Auto Phase function Enable. 0: Disable. 1: Enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATP[7:0]	7:0	Auto Phase Value.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATP[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATP[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATP[31:24]	7:0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	LB_TUNE_READY	7	Input VSYNC Blanking Status. 0: In display. 1: In blanking.	
	DELAYLN_NUM[2:0]	6:4	Delay Line After Sample V Start for Input Trigger Point.	
	-	3:2	Reserved.	
	UNDERRUN	1	Under run status for FIFO.	
	OVERRUN	0	Over run status for FIFO.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x05**	**Access: R/W**
	-	7	Reserved.	
	DE_LOCKH_MD	6	DE Lock H Position Mode.	
	HSTOL[5:0]	5:0	HSYNC Tolerance for Mode Change. 5: Default value.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x01**	**Access: R/W**
	VDO_VEDGE	7	Interlace mode VSYNC reference edge.	
	RAW_VSMD	6	Bypass mode Raw VSYNC output from SYNC Separator.	
	HTT_FILTERMD	5	Auto No signal Filter mode. 0: Disable. 1: Enable (update Htt after 4 sequential lines over tolerance).	
	AUTO_NO_SIGNAL	4	Auto No signal Enable. This Will Auto Set Current Bank 02[7] = 1 if Mode Change.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VS_TOL[3:0]	3:0	VSYNC Tolerance for Mode Change. 1: Default value.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	SOG_OFFMUX[1:0]	7:6	Off Line SOG source select. 00: Select analog 1 SOG. 01: Select analog 2 SOG. 10: Select analog 3 SOG.	
	IPHCS0_ACT	5	Analog 1 HSYNC Pin Active.	
	IPHCS1_ACT	4	Analog 2 HSYNC Pin Active.	
	IPHS_SB_S	3	Input normalized HSYNC pin Monitor. Show input HSYNC pin directly. (Active Low).	
	IPVS_SB_S	2	Input normalized VSYNC pin Monitor. Show input VSYNC pin directly. (Active Low).	
	OPHS	1	Output normalized HSYNC pin Monitor. Show output HSYNC pin directly. (Active Low).	
	OPVS	0	Output normalized VSYNC pin Monitor. Show output VSYNC pin directly. (Active Low).	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: RO**
	IPVS_ACT	7	Input On Line Source VSYNC Active. 0: Not active. 1: Active.	
	IPHS_ACT	6	Input On Line Source HSYNC Active. 0: Not active. 1: Active.	
	CS_DET	5	Composite Sync Detected status. 0: Input is not composite sync. 1: Input is detected as composite sync.	
	SOG_DET	4	Sync-On-Green Detected status. 0: Input is not SOG. 1: Input is detected as SOG.	
	INTLAC_DET	3	Interlace / Non-interlace detecting result by this chip. 0: Non-interlace. 1: Interlace.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FIELD_DET	2	Input odd/even field detecting result by this chip. 0: Even. 1: Odd.	
	HSPOL	1	Input On Line Source HSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
	VSPOL	0	Input On Line Source VSYNC polarity detecting result by this chip. 0: Active low. 1: Active high.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	VTT[7:0]	7:0	Input Vertical Total, count by HSYNC.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	VS_PW_VDOMD	7	VSYNC Raw Pulse Width for Measurement.	
	-	6	Reserved.	
	HSPW_SEL	5	Vsync Pulse Width Read Enable. The Report is shown in Current Bank 22.	
	-	4:3	Reserved.	
	VTT[10:8]	2:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x00**	**Access: R/W**
	HTT_FOR_READ[7:0]	7:0	Input Horizontal Period, count by reference clock.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: R/W**
	LN4_DETMD	7	Input HSYNC period Detect Mode. 0: 1 line. 1: 8 lines.	
	TEST_CSHTT	6	Report Sync Separator Htt by E5, E4. 0: Htt Report by Mode Detector. 1: Htt Report by Sync Separator.	
	HTT_FOR_READ[13:8]	5:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	FIELD_SWMD	7	Shift Line Method When Field Switch. 0: Old method. 1: New method.	
	COAST_HS_SEPMD	6	HSYNC in coast for Data Capture. 0: HSOUT (recommended).	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Re-shaped HSYNC.	
	USR_VSPOL	5	User defined input VSYNC Polarity, active when USR_VSPOLMD =1. 0: Active low. 1: Active high.	
	USR_VSPOLMD	4	Input VSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_VSPOL).	
	USR_HSPOL	3	User defined input HSYNC Polarity, active when USR_HSPOLMD =1. 0: Active low. 1: Active high.	
	USR_HSPOLMD	2	Input HSYNC polarity judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_HSPOL).	
	USR_INTLAC	1	User defined non-interlace/interlace, active when USR_INTLACMD = 1. 0: Non-interlace. 1: Interlace.	
	USR_INTLACMD	0	Interlace judgment. 0: Use result of internal circuit detection. 1: Defined by user (USR_INTLAC).	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	MEMSYN_TO_VS[1:0]	7:6	Memory control Switch Method. 00: Sample V End. 01: Sample V Start. 10: Sample V Start Ahead by Current Bank 09[3:0]. 11: Sample V Start Ahead by Current Bank 09[3:0] x 2.	
	DE_ONLY_HTT_CHGMD	5	DE Only mode Htt Change status mode. 0: Mode Change Provide in data clock Domain. 1: Mode Change Provide in data clock and Fix Clock Domain (recommended).	
	DE_ONLY_HTT_SRC	4	DE Only mode Htt Report Source. 0: Form Input DE. 1: From Re-generated DE.	
	ADC_VIDEO_FINV	3	Component Video Field Inversion when ADC_VIDEO = 1 for Data Align. 0: Normal.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Invert.	
	EXT_FIELDMD	2	Video External Field. 0: Use result of internal circuit detection. 1: Use external field.	
	FIELD_DETMD	1	Interlace Field detect method select. 0: Use the HSYNC numbers of a field to judge. 1: Use the relationship of VSYNC and HSYNC to judge.	
	FIELD_INV	0	Interlace Field Invert. 0: Normal. 1: Invert.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: RO**
	HSPW[7:0]	7:0	Pulse Width Report. If Current Bank HSPW_SEL (1F[13]) = 0, Report HSYNC. If Current Bank HSPW_SEL (1F[13]) = 1, Report VSYNC.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x1E**	**Access: R/W**
	DVICK_WIDTH[7:0]	7:0	DVI clock detection threshold, see Cah for usage (default 0x1E). Cah[6] = 0: DVI clock is OK, Freq(DVI) > Freq(xtal) * 23h/128. Cah[6] = 1: DVI clock is missing, Freq(DVI) < Freq(xtal) * 23h/128. Where Ebh default to 0x1E(30).	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VD_FREE	7	Video in Free Run Mode (Read Only).	
	MIN_VTT[6:0]	6:0	Minimum Vtt. When detected Vtt < MIN_VTT[6:0] x 16, into the video interlace freerun mode.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	VS_SEP_SEL	7	SYNC Separator VSYNC for Mode Detect. 0: RAW VSYNC (H / V Relationship is Keep for Interlace Detect). 1: HSYNC Align VSYNC (H / V Relationship is lose for Interlace Detect).	
	VIDEO_D1L_H	6	Component Video Delay Line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Lines for Another Field.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: Delay 3 Lines for Another Field. 11: Delay 4 Lines for Another Field.	
	ADC_VIDEO	5	ADC Input Select. 0: PC Source. 1: Component Video.	
	VIDEO_D1L_L	4	Component Video Delay Line. (VIDEO_D1L_H + VIDEO_D1L_L) = 00: Delay 1 Line for Another Field. 01: Delay 2 Lines for Another Field. 10: Delay 3 Lines for Another Field. 11: Delay 4 Lines for Another Field.	
	CS_CUT_MD	3	Composite SYNC cut mode. (Test Purpose). 0: Disable. 1: Enable.	
	EXTVS_SEPINV	2	External VSYNC polarity (only used when COAST_SRCS is 1). 0: Normal. 1: Invert.	
	COAST_SRC	1	Coast VSYNC Select. 0: Internal Separated VSYNC (Default). 1: External VSYNC (Test Purpose).	
	COAST_POL	0	Coast Polarity to PAD.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	COAST_FBD[7:0]	7:0	Front tuning. 00: Coast start from 1 HSYNC leading edge. 01: Coast start from 2 HSYNC leading edge, default value. ... 254: Coast start from 255 HSYNC leading edge. 255: Coast start from 256 HSYNC leading edge.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	COAST_BBD[7:0]	7:0	End tuning. 00: Coast end at 1 HSYNC leading edge. 01: Coast end at 2 HSYNC leading edge, default value. ... 254: Coast end at 255 HSYNC leading edge. 255: Coast end at 256 HSYNC leading edge.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	GR_DE_EN	7	DE or HSYNC post Glitch removal function Enable.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	FILTER_NUM[2:0]	6:4	DE or HSYNC post Glitch removal Range. Analog: 000: 0 XTAL clock. 001: 1 XTAL clock. 010: 2 XTAL clock. 111: 7 XTAL clock. DVI: 000: 0x8 input clock. 001: 1x8 input clock. 010: 2x8 input clock. 111: 7x8 input clock.	
	GR_HS_VIDEO	3	Input HSYNC Filter. When input source is analog: 0: Filter off. 1: Filter on. When input source is DVI: 0: Normal. 1: More tolerance for unstable DE.	
	GR_EN	2	Input sync sample mode. 0: Normal. 1: Glitch-removal.	
	HVTT_LOSE_MD	1	Htt/Vtt Lost Mode for INT. 0: By counter overflow. 1: By counter overflow + Active Detect IPVS_ACT, IPHS_ACT (E1[7:6]) (recommended).	
	IDCLK_INV	0	Capture Port Sample CLK Invert. 0: Normal. 1: Invert.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	AFT	7	ATP Filter for Text (4 frames). 0: Disable. 1: Enable.	
	IDHTT	6	DE only mode HTT count by IDCLK. 0: Disable. 1: Enable.	
	VSGR	5	VSYNC glitch removal with line less than 2 (DE Only).	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	VSP	4	VSYNC Protect with V total (DE Only). 0: Disable. 1: Enable.	
	-	3	Reserved.	
	DEGP	2	DE only mode Glitch Protect for position. 0: Disable. 1: Enable.	
	-	1:0	Reserved.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VS_SEP_SEL_1	7	New Interlace Detect Method by Big and Small line counts for a field.	
	VS_SEP_SEL_0	6	Hardware Auto Vsync Start Line Method Select.	
	INTLAC_DET_MODE[1:0]	5:4	Interlace detect mode. 00: Off. 01: Only for line total number is even. 10: All case. 11: Off.	
	EUP_AU_HDTV_DET	3	Europe/Australia 1080i HDTV Detect.	
	EUP_HDTV_DET	2	EUROPE 1080i HDTV Detect.	
	EUP_AUTOFIELD	1	EUR/AUS 1080i HDTV Auto Field Mode.	
	EUP_HDTV	0	EUR/AUS 1080i HDTV Force Field Mode.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	LOCK2LOCK_REPORT[3:0]	7:4	Check Lock to Lock Line Count for Interlace Auto-Correct.	
	-	3:1	Reserved.	
	ATRANGE_EN	0	Auto Range Enable. 0: Define Automatically. 1: Define by Current Bank 2a-2b.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATRANGE_VST[7:0]	7:0	Auto Function (Position, Gain Phase) vertical start point, count by input HSYNC.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	ATRANGE_VST[10:8]	2:0	See description of '102F54h'.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATRANGE_HST[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal start point, count by input dot clock.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	ATRANGE_HST[10:8]	2:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATRANGE_VDC[7:0]	7:0	Auto Function (Position, Gain Phase) vertical resolution, count by input HSYNC.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	ATRANGE_VDC[10:8]	2:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: 0x00**	**Access: R/W**
	ATRANGE_HDC[7:0]	7:0	Auto Function (Position, Gain Phase) horizontal resolution, count by input dot clock.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	ATRANGE_HDC[10:8]	2:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	GOP_CLK_FREE	1	GOP clock gating enable. 0: Can gate the GOP clock. 1: Don't gate the GOP clock.	
	IP2_CLK_GATE_EN	0	IP2 clock gating enable. 0: Don't gate the IDCLK. 1: Can gate the IDCLK.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	INSERT_NUM[7:0]	7:0	Vsync INSERT_NUMBER_OFFSET.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x00**	**Access: R/W**
	INSERT_SEL	7	Vsync INSERT_NUMBER_OFFSET enable.	
	-	6:3	Reserved.	
	INSERT_NUM[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOCK_NUM[7:0]	7:0	Vsync LOCK_NUMBER_OFFSET.	

IP1_M Register (Bank = 102F, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOCK_SEL	7	Vsync LOCK_NUMBER_OFFSET enable.	
	-	6:3	Reserved.	
	LOCK_NUM[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	VLOCK[7:0]	7:0	VLOCK.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	MEMSYN_TO_VS_NEW[1:0]	7:6	Memory control Switch Method. 0x: Reference 21[15:14]. 10: Sample V end delay 3 lines. 11: Sample V end delay 4 lines.	
	-	5:3	Reserved.	
	AUTO_NOS_HV_LOSE	2	Auto no signal set enable when H/V sync at the same.	
	AUTO_NOS_V_LOSE	1	Auto no signal set enable when V sync lose.	
	AUTO_NOS_H_LOSE	0	Auto no signal set enable when H sync lose.	

IP2_M Register (Bank = 102F, Sub-bank = 02)

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_SHT	7	VSD factor shift enable.	
	VFAC_SHT_INV	6	VSD field inverse.	
	IP2_F422EN	5	Force IP 442 format enable.	
	IP2_F422	4	1: IP 422. 0: IP 444.	
	-	3	Reserved.	
	CSC_DITHEN	2	CSC dither function enable.	
	VSD_DITHEN	1	VSD dither function enable.	
	HSD_DITHEN	0	HSD dither function enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	VOUT_PROC	5	VOUT_PROC.	
	HOUT_PROC	4	HOUT_PROC.	
	-	3:0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	HFAC_SET_IP[7:0]	7:0	HSD initial factor.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	HFAC_SET_IP[15:8]	7:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	HFAC_SET_IP[19:16]	3:0	See description of '102F04h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	HFACIN[7:0]	7:0	HSD factor, format [3.20].	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	HFACIN[15:8]	7:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	HFACIN[22:16]	6:0	See description of '102F08h'.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	IP2HSDEN	7	H Scaling Down enable.	
	PREHSDMODE	6	Pre-H scaling down mode.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Accumulator mode, fac = OUT/IN (format [0.20]). 1: 6TapY/4TapC filter mode, fac = IN/OUT (format [3.20]).	
	-	5:0	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_INI_T[7:0]	7:0	VSD initial factor for top field.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_INI_T[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_INI_B[7:0]	7:0	VSD initial factor for bottom.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFAC_INI_B[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFACIN[7:0]	7:0	VSD factor, format CB: [0.20], Bilinear [3.20].	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	VFACIN[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	VFACIN[22:16]	6:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	PRE_VDOWN	7	V Scaling Down enable.	
	PRE_VDOWN_MODE	6	V Scaling Down Mode. 0: CB. 1: Bilinear.	
	-	5:0	Reserved.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x08**	**Access: R/W**
	C_FILTER	7	444 to 422 filter mode.	
	CBCR_SWAP[1:0]	6:5	Cb/Cr swap for 444 to 422.	
	YDELAY_EN	4	Y delay enable.	
	DE_DLY_WITH_Y	3	DE_DLY_WITH_Y.	
	YCDELAY_STEP[2:0]	2:0	Y/C delay pipe step.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	PRE_ALIGN_EN	7	Insert pixel number enable for mirror mode.	
	-	6:4	Reserved.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PRE_ALIGN_WIDTH[3:0]	3:0	Insert pixel number for mirror mode.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x01**	**Access: R/W**
	IP2_STATUS_CLR	7	IP2 status clear.	
	-	6:1	Reserved.	
	DLAST_ALIGN_EN	0	Data last signal align with IPM fetch number.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	FLOW_CTRL_VALUE[3:0]	3:0	IP2 flow control count.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0x00**	**Access: RO**
	MAX_LBUF_CNT[7:0]	7:0	IP2 line buffer max pixels count.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:5	Reserved.	
	BW_NOT_ENOUGH	4	IP2 line buffer full.	
	-	3:1	Reserved.	
	MAX_LBUF_CNT[8]	0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: 0x00**	**Access: RO**
	READ_HSD_OUT_CNT[7:0]	7:0	HSD output pixel count.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	READ_HSD_OUT_CNT[11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: 0x00**	**Access: RO**
	READ_VSD_OUT_CNT[7:0]	7:0	VSD output pixel count.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:3	Reserved.	
	READ_VSD_OUT_CNT[10:8]	2:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:5	Reserved.	
	FIR_BD_CTRL	4	FIR_BD_CTRL.	
	IP2_CSC_EN	3	IP2 CSC enable.	
	-	2	Reserved.	
	RGB2YCBCR_EQ_SEL[1:0]	1:0	CSC coefficient select.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	PRE_Y_TAP0[5:0]	5:0	IP2 Pre-Filter coefficient 0 [s.3].	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	PRE_FILTER_EN	7	IP2 Pre-Filter enable.	
	FIR_DITH_EN	6	IP2 Pre-Filter dithering enable.	
	-	5:0	Reserved.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:6	Reserved.	
	PRE_Y_TAP1[5:0]	5:0	IP2 Pre-Filter coefficient 1 [s.6] (M10).	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x30**	**Access: R/W**
	-	7:6	Reserved.	
	PRE_Y_TAP2[5:0]	5:0	IP2 Pre-Filter coefficient 2 [s.6] (M10).	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x1D**	**Access: R/W**
	-	7:6	Reserved.	
	PRE_Y_TAP3[5:0]	5:0	IP2 Pre-Filter coefficient 3 [s.7] (M10).	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x5E**	**Access: R/W**
	-	7	Reserved.	
	PRE_Y_TAP4[6:0]	6:0	IP2 Pre-Filter coefficient 4 [s.8] (M10).	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	ADJ_HI_PRI[7:0]	7:0	Adjust memory priority.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	PSEUDO_STOP	0	Enable BPSEUDO blanking.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x08**	**Access: R/W**
	SPLIT_BLANK[7:0]	7:0	Pseudo blank cycle.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	EXT_LR_EN	4	Enable external LR signal.	
	-	3:1	Reserved.	
	INIT_3D_STAT	0	Initialize 3d stat.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	WAIT_LEFT_FRM	4	WAIT_LEFT_FRM.	
	-	3:1	Reserved.	
	EXT_LR_INV	0	Inverse external LR signal.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	INI_LR_IDX	4	0: L is the first frame. 1: R is the first frame.	
	-	3:2	Reserved.	
	LR_CHG_MODE[1:0]	1:0	0: Line. 1: Block. 2: Frame.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAX_LOOP[2:0]	6:4	3d mode setting.	
	-	3:1	Reserved.	
	SPLIT_HALF	0	Split 1 frame into 2 frames.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	VACT_SPC_EN[1:0]	5:4	3d mode setting.	
	-	3	Reserved.	
	MASK_EN[2:0]	2:0	3d mode setting.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default: 0x00**	**Access: R/W**
	GEN_VS_ACT[3:0]	7:4	Enable gen pseudo Vsync in 3d.	
	GEN_VS_EN[3:0]	3:0	Enable gen pseudo Vsync in 3d.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0x00**	**Access: R/W**
	VACT_VIDEO[7:0]	7:0	V_ACTIVE region.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	VACT_VIDEO[12:8]	4:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default: 0x00**	**Access: R/W**
	VACT_SPC_0[7:0]	7:0	V blanking between field1&field2 or field3&field4.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	

IP2_M Register (Bank = 102F, Sub-bank = 02)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VACT_SPC_0[12:8]	4:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x00**	**Access: R/W**
	VACT_SPC_1[7:0]	7:0	V blanking between field2&field3.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	VACT_SPC_1[12:8]	4:0	See description of '102FCEh'.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	FORCE_OUTACK	1	Enable DAT_ADJ to SRC force ready.	
	ADJ_AUTO	0	ADJ_AUTO.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default: 0x00**	**Access: RO**
	DATA_ADJ_DEBUG[7:0]	7:0	Debug.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default: 0x00**	**Access: RO**
	DATA_ADJ_DEBUG[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default: 0x00**	**Access: RO**
	FIFO_DIFF[7:0]	7:0	Number of FIFO.	
6Ah (102FD5h)	**REG102FD5**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:1	Reserved.	
	FIFO_DIFF[8]	0	See description of '102FD4h'.	

PNR Register (Bank = 102F, Sub-bank = 05)

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PNR_ENY_F1	3	Sub Window Post Noise Reduction for Y.	
	PNR_ENC_F1	2	Sub Window Post Noise Reduction for C.	
	RATIOYC_F1[1:0]	1:0	Sub Window Motion Ratio.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	PNR_BYPASS_F1	2	Sub Window PNR function bypass enable.	
	NR_EN_F1	1	Sub Window Post NR enable.	
	PCCS_EN_F1	0	Sub Window Post CCS enable.	
0Bh (102F16h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	DITHER_FRAME_RST_CNT[1:0]	2:1	Dither frame reset count.	
	DITHER_FRAME_RST_EN	0	Dither frame reset enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	FIELD_AVG_C_EN_F2	7	Main Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F2	6	Main Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F2	5	Main Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F2	4	Main Window Y blending threshold automatically carry to 16 when 15.	
	PNR_ENY_F2	3	Main Window Post Noise Reduction for Y.	
	PNR_ENC_F2	2	Main Window Post Noise Reduction for C.	
	RATIOYC_F2[1:0]	1:0	Main Window Motion Ratio.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F2	0	Main Window select next field inverter for noc_sel.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x18**	**Access: R/W**
	DHD_3F_EN_F2	7	Main Window DHD 3f mode enable.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PCCS_3F_EN_F2	6	Main Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F2	4	Main Window PCCS dither enable.	
	DHD_DITHER_EN_F2	3	Main Window DHD dither enable.	
	PNR_BYPASS_F2	2	Main Window PNR function bypass enable.	
	NR_EN_F2	1	Main Window Post NR enable.	
	PCCS_EN_F2	0	Main Window Post CCS enable.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	PAL_EN_F2	6	Main Window PAL enable.	
	-	5:0	Reserved.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	POS_MOTIONC_TH1_F2[2:0]	7:5	Main Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F2[2:0]	4:2	Main Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F2	1	Main Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F2	0	Main Window user-defined Y motion threshold enable.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F2	6	Main Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F2	5	Main Window enable select max motion for C.	
	YMOT_MAX_SEL_F2	4	Main Window enable select max motion for Y.	
	CMOT_DIV_MODE_F2[1:0]	3:2	Main Window C motion divide mode.	
	YMOT_DIV_MODE_F2[1:0]	1:0	Main Window Y motion divide mode.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F2	5	Main Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F2	4	Main Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F2	3	Main Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F2	2	Main Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F2	1	Main Window DHD YMR02 enable.	
	DHD_EN_F2	0	Main Window DHD enable.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_HMR_INT_INV_F1	5	Sub Window DHD Interleaved History MR invert.	
	DHD_HMR_INT_EN_F1	4	Sub Window DHD Interleaved History MR enable.	
	DHD_CMR_IIR_EN_F1	3	Sub Window DHD CMR IIR enable.	
	DHD_YMR_IIR_EN_F1	2	Sub Window DHD YMR IIR enable.	
	DHD_YMR02_EN_F1	1	Sub Window DHD YMR02 enable.	
	DHD_EN_F1	0	Sub Window DHD enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x1C**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_YMR02_TH[5:0]	5:0	DHD YMR02 threshold.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:3	Reserved.	
	DHD_YMR02_GAIN[2:0]	2:0	DHD YMR02 gain.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x18**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_YMR04_TH[5:0]	5:0	DHD YMR04 threshold.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:3	Reserved.	
	DHD_YMR04_GAIN[2:0]	2:0	DHD YMR04 gain.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x40**	**Access: R/W**
	DHD_CVAL_GAIN[7:0]	7:0	DHD C value gain.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:4	Reserved.	
	DHD_DIFFPIX_GAIN[3:0]	3:0	DHD pixel diff gain.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x18**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_CMR02_TH[5:0]	5:0	DHD C motion02 threshold.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:3	Reserved.	
	DHD_CMR02_GAIN[2:0]	2:0	DHD C motion02 gain.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:6	Reserved.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DHD_CMR04_TH[5:0]	5:0	DHD C motion04 threshold.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:3	Reserved.	
	DHD_CMR04_GAIN[2:0]	2:0	DHD C motion04 gain.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x30**	**Access: R/W**
	DHD_CEDGE_GAIN[7:0]	7:0	DHD C edge gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x40**	**Access: R/W**
	DHD_YEDGE_GAIN[7:0]	7:0	DHD Y edge gain.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DHD_DEBUG0_EN	7	DHD debug0 enable.	
	DHD_DEBUG1_EN	6	DHD debug1 enable.	
	-	5:0	Reserved.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x63**	**Access: R/W**
	-	7	Reserved.	
	DHD_YMR_IIR_ALPHA[2:0]	6:4	DHD YMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_YMR_IIR_STEP[1:0]	1:0	DHD YMR IIR step.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x63**	**Access: R/W**
	-	7	Reserved.	
	DHD_CMR_IIR_ALPHA[2:0]	6:4	DHD CMR IIR alpha.	
	-	3:2	Reserved.	
	DHD_CMR_IIR_STEP[1:0]	1:0	DHD CMR IIR step.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DHD_CEDGE_TH[3:0]	3:0	DHD C edge threshold.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	DHD_YEDGE_TH[5:0]	5:0	DHD Y edge threshold.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DHD_CVAL_TH[3:0]	3:0	DHD C value threshold.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	INV_SAT_OFFSET[6:0]	6:0	PCCS invert saturation offset.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	INV_SAT_POWNUM[2:0]	6:4	PCCS invert saturation POWNUM.	
	INV_SAT_W[3:0]	3:0	PCCS invert saturation weight.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: 0x00**	**Access: R/W**
	TDELTA_C_POWNUM[3:0]	7:4	PCCS inv-saturation delta POWNUM.	
	TDELTA_C_W[3:0]	3:0	PCCS inv-saturation delta weight.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	YDIFF_FNFN2_CORING_THRD[6:0]	6:0	PCCS Y Fn Fn-2 coring threshold.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	YDIFF_FNFN2_PRE_W[2:0]	2:0	PCCS Y Fn Fn-2 pre weight.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	YDIFF_FNFN2_POST_POWNUM[2:0]	6:4	PCCS Y Fn Fn-2 post POWNUM.	
	-	3	Reserved.	
	YDIFF_FNFN2_POST_W[2:0]	2:0	PCCS Y Fn Fn-2 post weight.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	CDIFF_FNFN2_CORING_THRD[6:0]	6:0	PCCS C Fn Fn-2 coring threshold.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	CDIFF_FNFN2_PRE_W[2:0]	2:0	PCCS C Fn Fn-2 pre weight.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	CDIFF_FNFN2_POST_POWNUM[2:0]	6:4	PCCS C Fn Fn-2 post POWNUM.	
	-	3	Reserved.	
	CDIFF_FNFN2_POST_W[2:0]	2:0	PCCS C Fn Fn-2 post weight.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	RC_EV_POWNUM[2:0]	6:4	PCCS real color edge value POWNUM.	
	RC_EV_W[3:0]	3:0	PCCS real color edge value weight.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	CCMODIFYFAC_POWNUM[3:0]	7:4	PCCS cross color edge value POWNUM.	
	CCMODIFYFAC_W[3:0]	3:0	PCCS cross color edge value weight.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: R/W**
	YEDGEFAC_UP_OFFSET[7:0]	7:0	PCCS Y edge offset.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	YEDGEFAC_POWNUM[2:0]	6:4	PCCS Y edge POWNUM.	
	YEDGEFAC_W[3:0]	3:0	PCCS Y edge weight.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	BLEND_LPF_TURN_OFF	1	PCCS factor low-pass filter off.	
	MEDIAN_TURN_OFF	0	PCCS factor median filter off.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	INV_CDIFF_FNFN2_POWNUM[3:0]	7:4	PCCS invert C Fn Fn-2 diff POWNUM.	
	INV_CDIFF_FNFN2_W[3:0]	3:0	PCCS invert C Fn Fn-2 diff weight.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	CDIFF_FNFN4_CORING_THRD[6:0]	6:0	PCCS C Fn Fn-4 diff threshold.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	CDIFF_FNFN4_PRE_W[2:0]	2:0	PCCS C Fn Fn-4 diff pre weight.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	CDIFF_FNFN4_POST_POWNUM[2:0]	6:4	PCCS C Fn Fn-4 diff post POWNUM.	
	-	3	Reserved.	

PNR Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CDIFF_FNFN4_POST_W[2:0]	2:0	PCCS C Fn Fn-4 diff post weight.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	YDIFF_3F_POST_POWNUM[2:0]	6:4	PCCS Y 3F diff post POWNUM.	
	-	3	Reserved.	
	YDIFF_3F_POST_W[2:0]	2:0	PCCS Y 3F diff post weight.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE[7:0]	7:0	PCCS Table.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE[15:8]	7:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE[23:16]	7:0	See description of '102FC0h'.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE[31:24]	7:0	See description of '102FC0h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE[39:32]	7:0	See description of '102FC0h'.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE[47:40]	7:0	See description of '102FC0h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE[55:48]	7:0	See description of '102FC0h'.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: R/W**
	PCCS_TABLE[63:56]	7:0	See description of '102FC0h'.	
78h ~ 78h (102FF0h ~ 102FF1h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

PNR_SUB Register (Bank = 102F, Sub-bank = 05)

PNR_SUB Register (Bank = 102F, Sub-bank = 05)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	FIELD_AVG_C_EN_F1	7	Sub Window C average mode when dotline cycle.	
	FIELD_AVG_Y_EN_F1	6	Sub Window Y average mode when dotline cycle.	
	PNR_RATIOC_F100_F1	5	Sub Window C blending threshold automatically carry to 16 when 15.	
	PNR_RATIOY_F100_F1	4	Sub Window Y blending threshold automatically carry to 16 when 15.	
	-	3:0	Reserved.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SEL_NEXT_FIELD_INV_F1	0	Sub Window select next field inverter for noc_sel.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x18**	**Access: R/W**
	DHD_3F_EN_F1	7	Sub Window DHD 3f mode enable.	
	PCCS_3F_EN_F1	6	Sub Window PCCS 3f mode enable.	
	-	5	Reserved.	
	PCCS_DITHER_EN_F1	4	Sub Window PCCS dither enable.	
	DHD_DITHER_EN_F1	3	Sub Window DHD dither enable.	
	-	2:0	Reserved.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	PAL_EN_F1	6	Sub Window PAL enable.	
	-	5:0	Reserved.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	POS_MOTIONC_TH1_F1[2:0]	7:5	Sub Window user-defined C motion threshold value.	
	POS_MOTIONY_TH1_F1[2:0]	4:2	Sub Window user-defined Y motion threshold value.	
	POS_MOTIONC_SEL_F1	1	Sub Window user-defined C motion threshold enable.	
	POS_MOTIONY_SEL_F1	0	Sub Window user-defined Y motion threshold enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	NR_Y_ROUND_F1	6	Sub Window rounding when NR blending for Y.	
	CMOT_MAX_SEL_F1	5	Sub Window enable select max motion for c.	

PNR_SUB Register (Bank = 102F, Sub-bank = 05)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	YMOT_MAX_SEL_F1	4	Sub Window enable select max motion for y.
	CMOT_DIV_MODE_F1[1:0]	3:2	Sub Window C motion divide mode.
	YMOT_DIV_MODE_F1[1:0]	1:0	Sub Window Y motion divide mode.

DNR Register (Bank = 102F, Sub-bank = 06)

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	F2_MR_SOURCE_NRY	4	F2 Motion Source Cur Select. 0: Cur after NR. 1: Cur non-NR.	
	-	3:2	Reserved.	
	F2_DNR_CORE_EN	1	F2 DNR core function enable.	
	F2_DNR_EN	0	F2 DNR ALL (PRESNR + MED+ CORE) function enable.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	F2_SNR_MD_MODE_EN	1	F2 SNR Motion Mode enable.	
	F2_SNR_EN	0	F2 SNR function enable.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	F2_NR_ROUND_BIT_C	5	Set C_ROUND described as above.	
	F2_NR_ROUND_BIT_Y	4	Set Y_ROUND described as above.	
	-	3:0	Reserved.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	F2_MOTION_PRE_SHIFT_C [1:0]	6:5	F2_MOTION_PRE_SHIFT_C.	
	-	4	Reserved.	
	F2_MOTION_PRE_SHIFT_Y [1:0]	3:2	F2_MOTION_PRE_SHIFT_Y.	
	-	1:0	Reserved.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	F2_DNR_LPF_C_EN	6	F2_DNR_LPF_C_EN.	
	-	5	Reserved.	
	F2_DNR_LPF_Y_EN	4	F2_DNR_LPF_Y_EN.	
	-	3:0	Reserved.	
2Bh	**REG102F56**	**7:0**	**Default: 0x01**	**Access: R/W**

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F56h)	-	7:3	Reserved.	
	F2_SHARP_LEVEL[2:0]	2:0	F2 SNR sharpness level.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	F2_POW_NUM[2:0]	2:0	F2 SNR power number.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0xBD**	**Access: R/W**
	DNR_TABLEY_0[7:0]	7:0	DNR TABLEY_0.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x79**	**Access: R/W**
	DNR_TABLEY_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x56**	**Access: R/W**
	DNR_TABLEY_1[7:0]	7:0	DNR TABLEY_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x34**	**Access: R/W**
	DNR_TABLEY_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x12**	**Access: R/W**
	DNR_TABLEY_2[7:0]	7:0	DNR TABLEY_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEY_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEY_3[7:0]	7:0	DNR TABLEY_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEY_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0xBD**	**Access: R/W**
	DNR_TABLEC_0[7:0]	7:0	DNR TABLEC_0.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x79**	**Access: R/W**
	DNR_TABLEC_0[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x56**	**Access: R/W**
	DNR_TABLEC_1[7:0]	7:0	DNR TABLEC_1.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x34**	**Access: R/W**
	DNR_TABLEC_1[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x12**	**Access: R/W**
	DNR_TABLEC_2[7:0]	7:0	DNR TABLEC_2.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEC_2[15:8]	7:0	See description of '102F8Ch'.	

DNR Register (Bank = 102F, Sub-bank = 06)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEC_3[7:0]	7:0	DNR TABLEC_3.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DNR_TABLEC_3[15:8]	7:0	See description of '102F8Eh'.	
58h ~ 70h (102FB0h ~ 102FE1h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0x08**	**Access: R/W**
	RESERVED_TABLE_0[7:0]	7:0	Reserved.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default: 0x18**	**Access: R/W**
	RESERVED_TABLE_0[15:8]	7:0	See description of '102FE8h'.	

FILM Register (Bank = 102F, Sub-bank = 0A)

FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (102F04h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7	Reserved.	
	DET_FIELD_SEL_LC	6	DET_FIELD_SEL_LC.	
	-	5	Reserved.	
	DIFF_TH[12:8]	4:0	Difference threshold.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x08**	**Access: R/W**
	32_CUR_ERROR_TH_F2[7:0]	7:0	32 current error threshold.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x08**	**Access: R/W**
	32_PRE_ERROR_TH_F2[15:8]	7:0	32 previous error threshold.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x04**	**Access: R/W**
	22_CUR_ERROR_TH_F2[7:0]	7:0	22 current error threshold.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x04**	**Access: R/W**
	22_PRE_ERROR_TH_F2[15:8]	7:0	22 previous error threshold.	
05h ~ 05h (102F0Ah ~ 102F0Bh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x10**	**Access: R/W**
	32_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	32 total error max threshold.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x7F**	**Access: R/W**
	32_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	32 total error sum threshold.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x08**	**Access: R/W**
	22_TOTAL_ERROR_MAX_TH_F2[7:0]	7:0	22 total error max threshold.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x7F**	**Access: R/W**
	22_TOTAL_ERROR_SUM_TH_F2[15:8]	7:0	22 total error sum threshold.	

FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h ~ 09h (102F10h ~ 102F12h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:5	Reserved.	
	FIX_DIFF_TH[12:8]	4:0	Cur error sum threshold.	
0Ah ~ 0Bh (102F14h ~ 102F17h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0xFF**	**Access: R/W**
	POINT_UNMATCH_1_TH_F2[7:0]	7:0	F2 counter 1 threshold.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0xFF**	**Access: R/W**
	POINT_UNMATCH_1_TH_F2[15:8]	7:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	POINT_UNMATCH_3_TH_F2[7:0]	7:0	F2 counter 3 threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0xFF**	**Access: R/W**
	POINT_UNMATCH_3_TH_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	POINT_UNMATCH_FIX_TH_F2[7:0]	7:0	F2 counter fix threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0xFF**	**Access: R/W**
	POINT_UNMATCH_FIX_TH_F2[15:8]	7:0	See description of '102F1Ch'.	
0Fh ~ 10h (102F1Eh ~ 102F20h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x30**	**Access: R/W**
	FILM32_EN_F2	7	F2 32 film mode enable.	
	FILM22_EN_F2	6	F2 22 film mode enable.	
	-	5:4	Reserved.	
	PRE32_F2	3	F2 pre32.	

FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	2:0	Reserved.	
11h ~ 14h (102F22h ~ 102F29h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0xEE**	**Access: R/W**
	MOT_TH_PATCH_F2[7:4]	7:4	F2 patch motion threshold.	
	FM_MOT_PIXTH_F2[3:0]	3:0	F2 motion ratio threshold.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x14**	**Access: R/W**
	FM_MOT_CNTTH_F2[15:8]	7:0	F2 unmatch threshold.	
16h ~ 17h (102F2Ch ~ 102F2Eh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0xC0**	**Access: R/W**
	FILM32_N1_EN_F2	7	F2 N1 film32 enable.	
	FILM22_N1_EN_F2	6	F2 N1 film22 enable.	
	-	5:0	Reserved.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: RO**
	MOTION_CNT_ALL_STATUS_F2[7:0]	7:0	F2 read status.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: RO**
	MOTION_CNT_ALL_STATUS_F2[15:8]	7:0	See description of '102F30h'.	
19h ~ 19h (102F32h ~ 102F33h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[7:0]	7:0	F2 patch read status.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: RO**
	MOTION_CNT_ALL_PATCH_STATUS_F2[15:8]	7:0	See description of '102F34h'.	
1Bh ~ 1Dh (102F36h ~ 102F3Bh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Eh	**REG102F3C**	**7:0**	**Default: 0x50**	**Access: R/W**

FILM Register (Bank = 102F, Sub-bank = 0A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Ch)	MULT_COEF_F2[7:4]	7:4	F2 multiplicand ratio.	
	-	3:1	Reserved.	
	RELATIVE_FM_EN_F2	0	F2 relative film mode frame diff enable.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x05**	**Access: R/W**
	LOWER_BOUND_FM_32_F2[15:8]	7:0	F2 frame diff lower bound.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	UPPER_BOUND_FM_32_F2[7:0]	7:0	F2 frame diff upper bound.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x03**	**Access: R/W**
	UPPER_BOUND_FM_32_F2[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x0F**	**Access: R/W**
	CHECK_SEQ_F2[7:0]	7:0	F2 lock threshold to enter 22.	
20h ~ 22h (102F41h ~ 102F45h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x44**	**Access: R/W**
	SPEEDUP_STEP_F2[7:4]	7:4	F2 speedup step.	
	SPEEDUP_SHIFT_F2[3:0]	3:0	F2 speedup shift value.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x80**	**Access: R/W**
	SPEEDUP_EN_F2	7	F2 speedup enable.	
	-	6:0	Reserved.	
24h ~ 57h (102F48h ~ 102FAFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

SNR Register (Bank = 102F, Sub-bank = 0C)

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SNR_STD_MOTION_RATIO_EN_F1	6	De-blocking and SNR active threshold motion ratio enable F1.	
	SNR_MOTION_RATIO_EN_F1	5	SNR motion ratio enable F1.	
	SNR_EN_F1	4	SNR enable F1.	
	-	3	Reserved.	
	SNR_STD_MOTION_RATIO_EN_F2	2	De-blocking and SNR active threshold motion ratio enable F2.	
	SNR_MOTION_RATIO_EN_F2	1	SNR motion ratio enable F2.	
	SNR_EN_F2	0	SNR enable F2.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x0A**	**Access: R/W**
	SNR_STD_LOW_THRD[7:0]	7:0	SNR active threshold.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x48**	**Access: R/W**
	SNR_ALPHA_STEP[2:0]	7:5	SNR alpha step.	
	-	4	Reserved.	
	SNR_STRENGTH_GAIN_F2[3:0]	3:0	SNR strength F2.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:4	Reserved.	
	SNR_STRENGTH_GAIN_F1[3:0]	3:0	SNR strength F1.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0xCF**	**Access: R/W**
	SNR_TABLE_01[7:0]	7:0	SNR LUT_01.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x69**	**Access: R/W**
	SNR_TABLE_23[7:0]	7:0	SNR LUT_23.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x24**	**Access: R/W**
	SNR_TABLE_45[7:0]	7:0	SNR LUT_45.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x01**	**Access: R/W**
	SNR_TABLE_67[7:0]	7:0	SNR LUT_67.	
36h	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Ch)	SNR_TABLE_89[7:0]	7:0	SNR LUT_89.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_TABLE_AB[7:0]	7:0	SNR LUT_AB.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_TABLE_CD[7:0]	7:0	SNR LUT_CD.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_TABLE_EF[7:0]	7:0	SNR LUT_EF.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	SNR_NM_DITHER_EN	7	Noise masking dither enable.	
	-	6	Reserved.	
	SNR_NM_MOTION_RATIO_EN_F1	5	Noise masking motion ratio enable F1.	
	SNR_NM_FILTER_EN_F1	4	Noise masking enable F1.	
	-	3:2	Reserved.	
	SNR_NM_MOTION_RATIO_EN_F2	1	Noise masking motion ratio enable F2.	
	SNR_NM_FILTER_EN_F2	0	Noise masking enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_SNR_15[1:0]	7:6	Reserved.	
	-	5:0	Reserved.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SNR_MR_LPF_EN_F1	4	De-blocking and SNR motion ratio low pass filter enable F1 (LPF is 3x3 mask).	
	-	3:1	Reserved.	
	SNR_MR_LPF_EN_F2	0	De-blocking and SNR motion ratio low pass filter enable F2 (LPF is 3x3 mask).	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_SNR_9[1:0]	7:6	Reserved.	
	SNR_NM_GAIN_F2[5:0]	5:0	Noise masking gain F2.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	RESERVED_SNR_10[1:0]	7:6	Reserved.	
	SNR_NM_GAIN_F1[5:0]	5:0	Noise masking gain F1.	
55h	**REG102FAA**	**7:0**	**Default: 0xFF**	**Access: R/W**

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FAAh)	SNR_NM_MIN_THRD[3:0]	7:4	Noise masking min threshold bound.	
	SNR_NM_MAX_THRD[3:0]	3:0	Noise masking max threshold bound.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x10**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_01[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_01.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x32**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_23[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_23.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x54**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_45[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_45.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x76**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_67[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_67.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x98**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_89[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_89.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0xBA**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_AB[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_AB.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0xDC**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_CD[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_CD.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0xFE**	**Access: R/W**
	SNR_STD_LOW_MOTION_TABLE_EF[7:0]	7:0	De-blocking and SNR active threshold motion ratio LUT_EF.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x10**	**Access: R/W**
	SNR_MOTION_TABLE_01[7:0]	7:0	SNR motion ratio LUT_01.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x32**	**Access: R/W**
	SNR_MOTION_TABLE_23[7:0]	7:0	SNR motion ratio LUT_23.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x54**	**Access: R/W**
	SNR_MOTION_TABLE_45[7:0]	7:0	SNR motion ratio LUT_45.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x76**	**Access: R/W**
	SNR_MOTION_TABLE_67[7:0]	7:0	SNR motion ratio LUT_67.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x98**	**Access: R/W**
	SNR_MOTION_TABLE_89[7:0]	7:0	SNR motion ratio LUT_89.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0xBA**	**Access: R/W**
	SNR_MOTION_TABLE_AB[7:0]	7:0	SNR motion ratio LUT_AB.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0xDC**	**Access: R/W**
	SNR_MOTION_TABLE_CD[7:0]	7:0	SNR motion ratio LUT_CD.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: 0xFE**	**Access: R/W**
	SNR_MOTION_TABLE_EF[7:0]	7:0	SNR motion ratio LUT_EF.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default: 0x10**	**Access: R/W**
	SNR_NM_MOTION_TABLE_01[7:0]	7:0	Noise masking motion ratio LUT_01.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default: 0x32**	**Access: R/W**
	SNR_NM_MOTION_TABLE_23[7:0]	7:0	Noise masking motion ratio LUT_23.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default: 0x54**	**Access: R/W**
	SNR_NM_MOTION_TABLE_45[7:0]	7:0	Noise masking motion ratio LUT_45.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default: 0x76**	**Access: R/W**
	SNR_NM_MOTION_TABLE_67[7:0]	7:0	Noise masking motion ratio LUT_67.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default: 0x98**	**Access: R/W**
	SNR_NM_MOTION_TABLE_89[7:0]	7:0	Noise masking motion ratio LUT_89.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default: 0xBA**	**Access: R/W**
	SNR_NM_MOTION_TABLE_AB[7:0]	7:0	Noise masking motion ratio LUT_AB.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default: 0xDC**	**Access: R/W**
	SNR_NM_MOTION_TABLE_	7:0	Noise masking motion ratio LUT_CD.	

SNR Register (Bank = 102F, Sub-bank = 0C)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	CD[7:0]			
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default: 0xFE**	**Access: R/W**
	SNR_NM_MOTION_TABLE_EF[7:0]	7:0	Noise masking motion ratio LUT_EF.	
70h ~ 70h (102FE0h ~ 102FE1h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

HISDNR_1D Register (Bank = 102F, Sub-bank = 0E)

HISDNR_1D Register (Bank = 102F, Sub-bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0xC0**	**Access: R/W**
	FM_HIS_H_RANGE_EN	7	Frame Histogram Report Define H Range Enable.	
	FM_HIS_RANGE_EN	6	Frame Histogram Report Define Range Enable.	
	-	5	Reserved.	
	DNR_USE_HISDNR_EN	4	DNR Function Use HISDNR Enable.	
	-	3:2	Reserved.	
	PSNR_EN	1	PSNR Enable.	
	HISDNR_EN	0	HISDNR enable.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x0D**	**Access: R/W**
	-	7:1	Reserved.	
	FM_HIS_V_RANGE_EN	0	Frame Histogram Report Define V Range Enable.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x2C**	**Access: R/W**
	HISDNR_MD_ADJUST_LEVEL_0123[3:0]	7:4	Motion difference adjust level 0123: 0.5 format.	
	MD_ADJUST_SHIFT	3	Motion difference adjust shift.	
	HISMATCH_BIT[2:0]	2:0	Histogram matching result shift bits (0 to 7).	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	FM_HIS_STD_THRD[7:0]	7:0	Frame Histogram STD Threshold.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	HISDNR_HISMATCH_STEP_LEVEL_0123[1:0]	1:0	Histogram matching step 0123.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x80**	**Access: R/W**
	HISDNR_HISMATCH_THRD_LEVEL_0123[7:0]	7:0	Histogram matching threshold 0123.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	HISDNR_STD_THRD_LEVEL_0123[3:0]	7:4	Standard Deviation threshold 0123.	
	-	3:2	Reserved.	
	HISDNR_STD_STEP_LEVEL_0123[1:0]	1:0	Standard Deviation step 0123.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:6	Reserved.	

HISDNR_1D Register (Bank = 102F, Sub-bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HISDNR_STRENGTH_GAIN [5:0]	5:0	HISDNR strength gain 2.4 format.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_1[7:0]	7:0	Frame motion histogram report section 1.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_1[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_2[7:0]	7:0	Frame motion histogram report section 2.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_2[15:8]	7:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_3[7:0]	7:0	Frame motion histogram report section 3.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_3[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_4[7:0]	7:0	Frame motion histogram report section 4.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_4[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_5[7:0]	7:0	Frame motion histogram report section 5.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_5[15:8]	7:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_6[7:0]	7:0	Frame motion histogram report section 6.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_6[15:8]	7:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_7[7:0]	7:0	Frame motion histogram report section 7.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_7[15:8]	7:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_8[7:0]	7:0	Frame motion histogram report section 8.	
0Ch	**REG102F19**	**7:0**	**Default: 0x00**	**Access: RO**

HISDNR_1D Register (Bank = 102F, Sub-bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F19h)	FM_HIS_16_8[15:8]	7:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_9[7:0]	7:0	Frame motion histogram report section 9.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_9[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_31[7:0]	7:0	Frame motion histogram report section 31.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_HIS_16_31[15:8]	7:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	NFM_HIS_16_0[7:0]	7:0	Normalized frame motion histogram section 0.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_0[8]	0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	NFM_HIS_16_1[7:0]	7:0	Normalized frame motion histogram section 1.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_1[8]	0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	NFM_HIS_16_2[7:0]	7:0	Normalized frame motion histogram section 2.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_2[8]	0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	NFM_HIS_16_3[7:0]	7:0	Normalized frame motion histogram section 3.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_3[8]	0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	NFM_HIS_16_4[7:0]	7:0	Normalized frame motion histogram section 4.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	

HISDNR_1D Register (Bank = 102F, Sub-bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NFM_HIS_16_4[8]	0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	NFM_HIS_16_5[7:0]	7:0	Normalized frame motion histogram section 5.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_5[8]	0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	NFM_HIS_16_6[7:0]	7:0	Normalized frame motion histogram section 6.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_6[8]	0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	NFM_HIS_16_7[7:0]	7:0	Normalized frame motion histogram section 7.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	NFM_HIS_16_7[8]	0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:6	Reserved.	
	PSNR_STRENGTH_GAIN[5:0]	5:0	PSNR strength gain: 2.4 format.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:2	Reserved.	
	PSNR_MH_BS[1:0]	1:0	PSNR motion history shift bits (0 to 7).	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:2	Reserved.	
	PSNR_STD_STEP_LEVEL_0123[1:0]	1:0	PSNR Standard Deviation step 0123.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x13**	**Access: R/W**
	PSNR_STD_THRD_LEVEL_0123[7:0]	7:0	PSNR STD threshold 0123.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	FM_HIS_H_ST[7:0]	7:0	Frame Histogram Report H Range Start.	
19h	**REG102F33**	**7:0**	**Default: 0x5B**	**Access: R/W**

HISDNR_1D Register (Bank = 102F, Sub-bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F33h)	FM_HIS_H_END[7:0]	7:0	Frame Histogram Report H Range End.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x01**	**Access: R/W**
	FM_HIS_V_ST[7:0]	7:0	Frame Histogram Report V Range Start.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x1D**	**Access: R/W**
	FM_HIS_V_END[7:0]	7:0	Frame Histogram Report V Range End.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_LUMA_SUM[7:0]	7:0	Total luma sum for assigned window. 16MSBs of 30 bit total sum.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: RO**
	FM_LUMA_SUM[15:8]	7:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_0[7:0]	7:0	Frame motion matching histogram report section 0.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_0[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_1[7:0]	7:0	Frame motion matching histogram report section 1.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_1[15:8]	7:0	See description of '102F3Ah'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_2[7:0]	7:0	Frame motion matching histogram report section 2.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_2[15:8]	7:0	See description of '102F3Eh'.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_3[7:0]	7:0	Frame motion matching histogram report section 3.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_3[15:8]	7:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_4[7:0]	7:0	Frame motion matching histogram report section 4.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_4[15:8]	7:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_5[7:0]	7:0	Frame motion matching histogram report section 5.	
22h	**REG102F45**	**7:0**	**Default: 0x00**	**Access: RO**

HISDNR_1D Register (Bank = 102F, Sub-bank = 0E)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F45h)	MAT_FM_HIS_16_5[15:8]	7:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_6[7:0]	7:0	Frame motion matching histogram report section 6.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_6[15:8]	7:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_7[7:0]	7:0	Frame motion matching histogram report section 7.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: RO**
	MAT_FM_HIS_16_7[15:8]	7:0	See description of '102F48h'.	
25h (102F4Ah)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	SW_BORDER_EN	7	Sub window (F1) border enable.	
	-	6:0	Reserved.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDLO[3:0]	7:4	Sub window Border Outside height of Left side.	
	BDLI[3:0]	3:0	Sub window Border Inside height of Left side.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDLO_BO[3:0]	7:4	Main window border outside height of Left side.	
	BDLI_BO[3:0]	3:0	Main window inside height of left side.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDRO[3:0]	7:4	Sub window Border Outside height of Right side.	
	BDRI[3:0]	3:0	Sub window Border Inside height of Right side.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDRO_BO[3:0]	7:4	Main window Border Outside height of Right side.	
	BDRI_BO[3:0]	3:0	Main window Border Inside height of Right side.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDUO[3:0]	7:4	Sub window Border Outside width of Upper side.	
	BDUI[3:0]	3:0	Sub window Border Inside width of Upper side.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDUO_BO[3:0]	7:4	Main window Border Outside width of Upper side.	
	BDUI_BO[3:0]	3:0	Main window Border Inside width of Upper side.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDDO[3:0]	7:4	Sub window Border Outside width of Down side.	
	BDDI[3:0]	3:0	Sub window Border Inside width of Down side.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	BDDO_BO[3:0]	7:4	Main window Border Outside width of Down side.	
	BDDI_BO[3:0]	3:0	Main window Border Inside width of Down side.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	4WINEN	6	4th Window Enable. 0: Disable. 1: Enable.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	3WINEN	5	3rd Window Enable. 0: Disable. 1: Enable.	
	2WINEN	4	2nd Window Enable. 0: Disable. 1: Enable.	
	-	3:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEST[7:0]	7:0	Sub window Horizontal Start.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEST[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEEND[7:0]	7:0	Sub window Horizontal End.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEEND[11:8]	3:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEST[7:0]	7:0	Sub window Vertical Star.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEST[11:8]	3:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEEND[7:0]	7:0	Sub window Vertical End.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEEND[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEST_2ND[7:0]	7:0	2nd Sub window Horizontal Start for MWE.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEST_2ND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEEND_2ND[7:0]	7:0	2nd Sub window Horizontal End for MWE.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEEND_2ND[11:8]	3:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEST_2ND[7:0]	7:0	2nd Sub window Vertical Start for MWE.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEST_2ND[11:8]	3:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEEND_2ND[7:0]	7:0	2nd Sub window Vertical End for MWE.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEEND_2ND[11:8]	3:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEST_3RD[7:0]	7:0	3rd Sub window Horizontal Start for MWE.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEST_3RD[11:8]	3:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEEND_3RD[7:0]	7:0	3rd Sub window Horizontal End for MWE.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEEND_3RD[11:8]	3:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEST_3RD[7:0]	7:0	3rd Sub window Vertical Start for MWE.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEST_3RD[11:8]	3:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEEND_3RD[7:0]	7:0	3rd Sub window Vertical End for MWE.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEEND_3RD[11:8]	3:0	See description of '102F24h'.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEST_4TH[7:0]	7:0	4th Sub window Horizontal Start for MWE.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEST_4TH[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_HDEEND_4TH[7:0]	7:0	4th Sub window Horizontal End for MWE.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_HDEEND_4TH[11:8]	3:0	See description of '102F28h'.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEST_4TH[7:0]	7:0	4th Sub window Vertical Start for MWE.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEST_4TH[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_VDEEND_4TH[7:0]	7:0	4th Sub window Vertical End for MWE.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	S_VDEEND_4TH[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SWBCOL[7:0]	7:0	Sub Window Border Color.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SWNS_COL[7:0]	7:0	Sub Window No Signal Color.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SGCR	4	Sub window Gamma. Correction Rounding function. 0: Disable. 1: Enable.	
	-	3:1	Reserved.	
	SGCB	0	Sub window Gamma Correction function control. 0: Bypass gamma correction function. 1: Enable gamma correction function.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
19h ~ 1Ah (102F32h ~ 102F35h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_HOFFS[7:0]	7:0	Keystone Horizontal position Offset.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	KST_HOFFSSN	7	Keystone Horizontal position initial Offset Sign. 0: Positive value. 1: Negative value.	
	KST_HOFFS[14:8]	6:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	KSTPD[7:0]	7:0	Keystone Horizontal position Delta per line.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	KSTPD[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F3Ah'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F3Eh'.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F40h'.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F44h'.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	CMRND	5	Color Matrix Rounding control.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: 128~127.	
	GRAN	1	Green Range. 0: 0~255. 1: 128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: 128~127.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SMEN	7	SVM Main window Enable.	
	SMTE	6	SVM Main window Tap Enable.	
	SMFT[1:0]	5:4	SVM Main window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
	SSWEN	3	SVM Sub window Enable.	
	SSWETE	2	SVM Sub window Tap Enable.	
	SSWFT[1:0]	1:0	SVM Sub window Filter Tap. 00: 2 taps. 01: 3 taps. 10: 4 taps. 11: 5 taps.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSDY	7	OSD color Space. 0: OSD color space. 1: OSD is YUV color space.	
	SINV	6	SMV polarity Invert. 0: Normal. 1: Invert.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SVMBYS[1:0]	5:4	SVM Bypass Y Select. 0x: SMV data. 10: Original Y data. 11: Y with tap filter.	
	SCORING[3:0]	3:0	SVM Coring.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SVMLMT[7:0]	7:0	SVM Limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SMSTP[2:0]	6:4	SVM Main window Step.	
	SMGAIN[3:0]	3:0	SVM Main window Gain.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SSWSTP[2:0]	6:4	SVM Sub window Step.	
	SWGAIN[3:0]	3:0	SVM Sub window Gain.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SPAJ[1:0]	6:5	SVM Pipe Adjust.	
	SDLYAJ[4:0]	4:0	SVM Delay Adjust.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	SVM_SEP_DLY	7	SVM Separate Delay Enable.	
	OVERLAP_SEL[1:0]	6:5	Overlap Select. 00: Average. 01: No Action. 10: Keep slow down result. 11: Keep speed up result.	
	SVM_SD_DLY[4:0]	4:0	SVM Slow down delay.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SBPMC	6	Scaler Bypass Mode Control. 0: Disable. 1: Enable.	
	IPFI	5	To Pad Field Invert enable.	
	-	4:2	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IOFI	1	Interlace Output Field Invert.	
	IOEN	0	Interlace Output Enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DISABLE_ALL_VOP2_FUNCTION	4	Disable all VOP2 function.	
	-	3:0	Reserved.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	IP_FINV	7	IP Field Inverse.	
	IP_ITLC	6	IP Interlace.	
	-	5:4	Reserved.	
	BES[1:0]	3:2	Border Extend for SVM.	
	OES[1:0]	1:0	OSD Extend for SVM.	
2Ch (102F58h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	OP1INTERLACE_OUT	7	OP1 output is interlace mode.	
	-	6:0	Reserved.	
2Dh ~ 2Fh (102F5Ah ~ 102F5Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	R_BRI_OFFSET[7:0]	7:0	Offset for R data.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x00**	**Access: R/W**
	BRI_EN	7	Brightness enable (after gamma).	
	CON_EN	6	Contrast enable (after gamma).	
	NOISE_ROUND_EN	5	Noise rounding enable for contrast brightness function.	
	-	4:3	Reserved.	
	R_BRI_OFFSET[10:8]	2:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	G_BRI_OFFSET[7:0]	7:0	Offset for G data.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	G_BRI_OFFSET[10:8]	2:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_BRI_OFFSET[7:0]	7:0	Offset for B data.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	B_BRI_OFFSET[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	R_CON_GAIN[7:0]	7:0	Contrast gain for R data.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	R_CON_GAIN[11:8]	3:0	See description of '102F66h'.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	G_CON_GAIN[7:0]	7:0	Contrast gain for G data.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	G_CON_GAIN[11:8]	3:0	See description of '102F68h'.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_CON_GAIN[7:0]	7:0	Contrast gain for B data.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	B_CON_GAIN[11:8]	3:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	M_BRI_R[7:0]	7:0	Brightness offset (bri_function) for main window R.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	SS_MODE	7	Brightness offset (before gamma) range control. 0: From -1024 ~ 1023. 1: From -512 ~ 511.	
	-	6:3	Reserved.	
	M_BRI_R[10:8]	2:0	See description of '102F6Ch'.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	M_BRI_G[7:0]	7:0	Brightness offset (bri_function) for main window G.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	M_BRI_G[10:8]	2:0	See description of '102F6Eh'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: 0x00**	**Access: R/W**
	M_BRI_B[7:0]	7:0	Brightness offset (bri_function) for main window B.	
38h (102F71h)	**REG102F71**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	M_BRI_B[10:8]	2:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_BRI_R[7:0]	7:0	Brightness offset (bri_function) for sub window R.	
39h (102F73h)	**REG102F73**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	S_BRI_R[10:8]	2:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_BRI_G[7:0]	7:0	Brightness offset (bri_function) for sub window G.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	S_BRI_G[10:8]	2:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x00**	**Access: R/W**
	S_BRI_B[7:0]	7:0	Brightness offset (bri_function) for sub window B.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	S_BRI_B[10:8]	2:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_R_BASE0[7:0]	7:0	Check value for auto mload base0 R channel.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_R_ERR_0	7	Base0 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE0[11:8]	3:0	See description of '102F78h'.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_R_BASE1[7:0]	7:0	Check value for auto mload base1 R channel.	
3Dh	**REG102F7B**	**7:0**	**Default: 0x00**	**Access: RO, R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F7Bh)	GAMMA_MLOAD_CHECK_R_ERR_1	7	Base1 R channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_R_BASE1[11:8]	3:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_G_BASE0[7:0]	7:0	Check value for auto mload base0 G channel.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_0	7	Base0 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE0[11:8]	3:0	See description of '102F7Ch'.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_G_BASE1[7:0]	7:0	Check value for auto mload base1 G channel.	
3Fh (102F7Fh)	**REG102F7F**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_G_ERR_1	7	Base1 G channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_G_BASE1[11:8]	3:0	See description of '102F7Eh'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_B_BASE0[7:0]	7:0	Check value for auto mload base0 B channel.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_0	7	Base0 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE0[11:8]	3:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAMMA_MLOAD_CHECK_B_BASE1[7:0]	7:0	Check value for auto mload base1 B channel.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	GAMMA_MLOAD_CHECK_B_ERR_1	7	Base1 B channel check error.	
	-	6:4	Reserved.	
	GAMMA_MLOAD_CHECK_B_BASE1[11:8]	3:0	See description of '102F82h'.	
42h ~ 45h (102F84h ~ 102F8Bh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CAP_STAGE	4	Capture stage selection. 0: Before OSD. 1: After OSD.	
	-	3:0	Reserved.	
46h (102F8Dh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_R_CON_GAIN[7:0]	7:0	Main window R gain for pre-gamma CON_BRI.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_CON_GAIN[7:0]	7:0	Main window G gain for pre-gamma CON_BRI.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_B_CON_GAIN[7:0]	7:0	Main window B gain for pre-gamma CON_BRI.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_R_CON_GAIN[7:0]	7:0	Sub window R gain for pre-gamma CON_BRI.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_R_CON_GAIN[11:8]	3:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_CON_GAIN[7:0]	7:0	Sub window G gain for pre-gamma CON_BRI.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_G_CON_GAIN[11:8]	3:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_B_CON_GAIN[7:0]	7:0	Sub window B gain for pre-gamma CON_BRI.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_B_CON_GAIN[11:8]	3:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_R_BRI_OFFSET[7:0]	7:0	Main window R offset for pre-gamma CON_BRI.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_BRI_OFFSET[7:0]	7:0	Main window G offset for pre-gamma CON_BRI.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_B_BRI_OFFSET[7:0]	7:0	Main window B offset for pre-gamma CON_BRI.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_R_BRI_OFFSET[7:0]	7:0	Sub window R offset for pre-gamma CON_BRI.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_BRI_OFFSET[7:0]	7:0	Sub window G offset for pre-gamma CON_BRI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_G_BRI_OFFSET[10:8]	2:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_B_BRI_OFFSET[7:0]	7:0	Sub window B offset for pre-gamma CON_BRI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_B_BRI_OFFSET[10:8]	2:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MAIN_NOISE_ROUND_EN	2	Main window noise rounding enable for pre-gamma CON_BRI.	
	MAIN_BRI_EN	1	Main window brightness enable for pre-gamma CON_BRI.	
	MAIN_CON_EN	0	Main window contrast enable for pre-gamma CON_BRI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	SUB_NOISE_ROUND_EN	2	Sub window noise rounding enable for pre-gamma CON_BRI.	
	SUB_BRI_EN	1	Sub window brightness enable for pre-gamma CON_BRI.	
	SUB_CON_EN	0	Sub window contrast enable for pre-gamma CON_BRI.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	FREEZ_VCNT_VALUE[7:0]	7:0	Output v-counter freeze position.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	FREEZ_VCNT_VALUE[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: R/W**
	LOCK_VCNT_VALUE[7:0]	7:0	V-counter generates output reference signal value. This register is active when REG_NEW_LOCK_POINT is set high.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	LOCK_VCNT_VALUE[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	PSEUDO_VS_EN	6	Enable pseudo Vsync for freeze region.	
	OUTPUT_FIELD_SEL	5	Select field for output reference signal.	
	OTUPUT_FIELD_INV	4	Invert field for output reference signal.	
	SW_RESET_VCNT_FREEZ	3	Software clear v-counter freeze status.	
	IVS_SEL	2	Select insert_end point as input reference for frame PLL.	
	NEW_LOCK_POINT	1	New output reference signal for frame PLL enable.	
	INPUT_FREEZ	0	V-counter freeze enable.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	VCNT_FREEZ_REGION	7	In V-counter freeze status.	
	-	6:2	Reserved.	
	IVS_CNT[9:8]	1:0	Frame number for input reference generate.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_SUB_16	7	Sub input Y signal sub 16 enable for CCIR656 format.	
	MAIN_Y_SUB_16	6	Main input Y signal sub 16 enable for CCIR656 format.	
	SUB_R_MIN_SIGN	5	Sub R min limit for BRI is negative value.	
	SUB_BRI_LIMIT_EN	4	Sub enable BRI input source limit.	
	MAIN_B_MIN_SIGN	3	Main B min limit for BRI is negative value.	
	MAIN_G_MIN_SIGN	2	Main G min limit for BRI is negative value.	
	MAIN_R_MIN_SIGN	1	Main R min limit for BRI is negative value.	
	MAIN_BRI_LIMIT_EN	0	Main enable BRI input source limit.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	PSEUDO_DE_SHIFT_ONLY	6	Random noise shift only during valid data period enable.	
	NOISE_DITH_EN	5	Noise dither enable.	
	GAMMA_REPEAT_MAX	4	Repeat gamma table max value for interpolation.	
	CAP_EN	3	Capture image to IP enable.	
	-	2:0	Reserved.	
58h	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: R/W**

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB0h)	MAIN_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. REG_MAIN_R_MIN_SIGN = 1. MAIN_R_MIN = -MAIN_R_MIN_LIMIT. REG_MAIN_R_MIN_SIGN = 0. MAIN_R_MIN = MAIN_R_MIN_LIMIT.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	MAIN_R_MIN_LIMIT[12:8]	4:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_R_MAX_LIMIT[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_MAIN_G_MIN_SIGN = 1. MAIN_G_MIN = -MAIN_G_MIN_LIMIT. REG_MAIN_G_MIN_SIGN = 0. MAIN_G_MIN = MAIN_G_MIN_LIMIT.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	MAIN_G_MIN_LIMIT[12:8]	4:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_G_MAX_LIMIT[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_MAIN_B_MIN_SIGN = 1. MAIN_R_MIN = -MAIN_B_MIN_LIMIT. REG_MAIN_B_MIN_SIGN = 0. MAIN_R_MIN = MAIN_B_MIN_LIMIT.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_B_MIN_LIMIT[12:8]	4:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_B_MAX_LIMIT[11:8]	3:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_R_MIN_LIMIT[7:0]	7:0	Main R min limit value, s.12 format sign bit is bit-12. REG_SUB_R_MIN_SIGN = 1: MAIN_R_MIN = -SUB_R_MIN_LIMIT. REG_SUB_R_MIN_SIGN = 0: MAIN_R_MIN = SUB_R_MIN_LIMIT.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_R_MIN_LIMIT[12:8]	4:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_R_MAX_LIMIT[7:0]	7:0	Main R max limit value, 12 format.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_R_MAX_LIMIT[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_MIN_LIMIT[7:0]	7:0	Main G min limit value, s.12 format sign bit is bit-12. REG_SUB_G_MIN_SIGN = 1. MAIN_G_MIN = -SUB_G_MIN_LIMIT. REG_SUB_G_MIN_SIGN = 0. MAIN_G_MIN = SUB_G_MIN_LIMIT.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_G_MIN_LIMIT[12:8]	4:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_G_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_G_MAX_LIMIT[11:8]	3:0	See description of '102FC2h'.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_B_MIN_LIMIT[7:0]	7:0	Main B min limit value, s.12 format sign bit is bit-12. REG_SUB_B_MIN_SIGN = 1. MAIN_R_MIN = -SUB_B_MIN_LIMIT. REG_SUB_B_MIN_SIGN = 0. MAIN_R_MIN = SUB_B_MIN_LIMIT.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_B_MIN_LIMIT[12:8]	4:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_B_MAX_LIMIT[7:0]	7:0	Main R max limit value 12 format.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_B_MAX_LIMIT[11:8]	3:0	See description of '102FC6h'.	
64h ~ 69h (102FC8h ~ 102FD3h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default: 0x00**	**Access: R/W**
	RGB_COMPRESSION_MODE[7:0]	7:0	New add function for RGB_compression.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default: 0x00**	**Access: R/W**
	RGB_COMPRESSION_MODE[15:8]	7:0	See description of '102FD8h'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	FWC_SUB_EN	4		
	-	3:2	Reserved.	
	FWC_DITHER_EN	1		
	FWC_MAIN_EN	0		
70h (102FE1h)	**REG102FE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	FWC_STRENGTH[3:0]	3:0		
71h (102FE2h)	**REG102FE2**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FWC_SLOPE[5:0]	5:0		
71h (102FE3h)	**REG102FE3**	**7:0**	**Default: 0x00**	**Access: R/W**
	FWC_CTH[7:0]	7:0		
72h (102FE4h)	**REG102FE4**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[7:0]	7:0		
72h (102FE5h)	**REG102FE5**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[15:8]	7:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[23:16]	7:0	See description of '102FE4h'.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[31:24]	7:0	See description of '102FE4h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[39:32]	7:0	See description of '102FE4h'.	
74h (102FE9h)	**REG102FE9**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[47:40]	7:0	See description of '102FE4h'.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[55:48]	7:0	See description of '102FE4h'.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[63:56]	7:0	See description of '102FE4h'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[71:64]	7:0	See description of '102FE4h'.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[79:72]	7:0	See description of '102FE4h'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[87:80]	7:0	See description of '102FE4h'.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_R[95:88]	7:0	See description of '102FE4h'.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[7:0]	7:0		
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[15:8]	7:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[23:16]	7:0	See description of '102FF4h'.	

S_VOP Register (Bank = 102F, Sub-bank = 0F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[31:24]	7:0	See description of '102FF4h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[39:32]	7:0	See description of '102FF4h'.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[47:40]	7:0	See description of '102FF4h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[55:48]	7:0	See description of '102FF4h'.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[63:56]	7:0	See description of '102FF4h'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[71:64]	7:0	See description of '102FF4h'.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[79:72]	7:0	See description of '102FF4h'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[87:80]	7:0	See description of '102FF4h'.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default: 0x80**	**Access: R/W**
	FWC_DELTA_B[95:88]	7:0	See description of '102FF4h'.	

VOP Register (Bank = 102F, Sub-bank = 10)

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSEND0[7:0]	7:0	20h: Recommended value (power on default value is 0).	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	DB_MASK	0	Double buffer register mask signal. The double buffer register is updated when DB_MASK and DB_LOAD.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSST_10_0[7:0]	7:0	Output VSYNC start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	VSST_11	4	Output VSYNC D[11]start (only useful when AOVS=1). 302h: Recommended value for XGA output (power on default value is 3). 402h: Recommended value for SXGA output.	
	VSRU	3	VSYNC Register Usage. 0: Registers 20h - 23h are used to define output VSYNC. 1: Registers 20h and 21h are used to define No Signal VSYNC. Registers 22h and 23h are used to define minimum H total.	
	VSST_10_0[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSEND[7:0]	7:0	Output VSYNC END (only useful when AOVS=1). 304h: Recommended value for XGA output (power on default value is 6). 404h: Recommended value for SXGA output.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	VSEND[11:8]	3:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEHST[7:0]	7:0	External VD Using Sync. 0: Sync is Generated from Data Internally.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Sync from External Source.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DEHST[12:8]	4:0	See description of '102F08h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEHEND[7:0]	7:0	Output DE Horizontal END. 447h: Recommended value for XGA output (power on default value is 0). 547h: Recommended value for SXGA output.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	DEHEND[12:8]	4:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEVST[7:0]	7:0	Output DE Vertical Start. 00: Default value.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSTSEL	7	Vertical Start Select. 0: DEVST[10:0] is Output DE vertical start. 1: DEVST[10:0] is Scaling Image Window vertical start.	
	-	6:4	Reserved.	
	DEVST[11:8]	3:0	See description of '102F0Ch'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**
	DEVEND[7:0]	7:0	Output DE Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DEVEND[11:8]	3:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	SIHST[7:0]	7:0	Scaling Image window Horizontal Start. 48h: Recommended value (power on default is 0).	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SIHST[12:8]	4:0	See description of '102F10h'.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	SIHEND[7:0]	7:0	447h: Recommended value for XGA output (power on default is 0). 547h: Recommended value for SXGA output.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SIHEND[12:8]	4:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	SIVST[7:0]	7:0	Scaling Image window Vertical Start.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SIVST[11:8]	3:0	See description of '102F14h'.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: R/W**
	SIVEND[7:0]	7:0	Scaling Image window Vertical END. 2FFh: Recommended value for XGA output (power on default value is 6). 3FFh: Recommended value for SXGA output.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SIVEND[11:8]	3:0	See description of '102F16h'.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: R/W**
	HDTOT[7:0]	7:0	Output Horizontal Total. 53fh: Recommended value for XGA output (power on default value is 3). 697h: Recommended value for SXGA output.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	HDTOT[12:8]	4:0	See description of '102F18h'.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	VDTOT[7:0]	7:0	Output Vertical Total. 326h: Recommended value for XGA output (power on default value is 3). 42Ah: Recommended value for SXGA output.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	VDTOT[11:8]	3:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSEND[7:0]	7:0	20h: Recommended value (power on default value is 0).	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x4C**	**Access: R/W**
	AOVS	7	Auto Output VSYNC. 0: OVSYNC is defined automatically. 1: OVSYNC is defined manually (register 0x20 - 0x23).	
	OUTM	6	Output Mode. 0: Mode 0. 1: Mode 1.	
	-	5:4	Reserved.	
	EHTT	3	Even H Total. 0: Enable, Output H Total is always even pixels. 1: Disable, Output H Total is always odd pixels.	
	MOD2	2	Mode 2. 0: Disable. 1: Enable.	
	AHRT	1	Auto H total and Read start Tuning enable. 0: Disable. 1: Enable.	
	CTRL	0	ATCTRL function enable. 0: Disable. 1: Enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	FPLLMD0	7	Frame PLL Mode 0.	
	SL_TUNE_EN	6	Short line tune enable.	
	AUTO_H_TOTAL_UPDATE_EN	5	Enable update AUTO_H_TOTAL value to H_TOTAL.	
	-	4:2	Reserved.	
	SSC_SHIFT	1	0: Enable. 1: Disable.	
	CLKDIV2_POINT_SELECT	0	0: Original. 1: New.	
11h (102F23h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
12h	**REG102F24**	**7:0**	**Default: 0x20**	**Access: R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F24h)	LCK_TH[7:0]	7:0	Frame PLL Lock Threshold.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x08**	**Access: R/W**
	LCK_TH[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x10**	**Access: R/W**
	FTNS[3:0]	7:4	Tune Frame Number of Short-line tune.	
	-	3	Reserved.	
	PIP_REG_EN	2	PIP Register Enable.	
	-	1	Reserved.	
	NOISY_GEN	0	Noise Generator.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	PFLL_LMT1[7:0]	7:0	Frame PLL Limit.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	PFLL_LMT0[7:0]	7:0	Frame PLL Limit.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	PFLL_LMT[7:0]	7:0	Frame PLL Limit.	
15h ~ 16h (102F2Bh ~ 102F2Ch)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	BRC	0	Brightness function. 0: Off. 1: On.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: RO**
	INTLX_VS_OFFSET[7:0]	7:0	The interlace Vsync offset.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:6	Reserved.	
	INTLX_VS_EN	5	Interlace Vsync enable.	
	INTLX_VS_OFFSET[12:8]	4:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	BY_STAGE_VIP[3:0]	7:4	VIP report point stage.	
	BY_STAGE_OP2[3:0]	3:0	Report point stage.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	REP_RD_TRID	0	Report SW read trigger.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SWBLBK	6	Sub window Blue screen color. 0: Black color. 1: Blue color.	
	SWBLUE	5	Sub window Blue screen control. 0: Off. 1: On.	
	-	4:3	Reserved.	
	MBD_EN	2	Main window Border Enable.	
	MBLK	1	Main window Black screen control. 0: Off. 1: On.	
	NOSC_EN	0	No Signal Color Enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCL_G[7:0]	7:0	Frame Color - Green.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCL_B[7:0]	7:0	Frame Color - Blue.	
1Bh ~ 1Bh (102F36h ~ 102F37h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	RST_E_4_FRAME	7	Reset noise generator by frames enable.	
	NDMD	6	Noise Dithering Method.	
	DATP	5	Dither based on Auto Phase threshold. 0: Disable. 1: Enable.	
	DRT	4	Dither Rotate Type. 0: EOR. 1: Rotate.	
	DT3	3	Dither Type 2 control. 0: Disable dither type 2.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Enable dither type 2.	
	DT2	2	Dither Type 2. 0: Output data bits 1 and 0 according to input pixel value. 1: Output data bits 2, 1 and 0 according to input pixel value.	
	DT1	1	Dither Type 1. 0: Normal. 1: Output data bits 1 and 0 are always 00.	
	TDFNC	0	Tempo-Dither Frame Number Control. 0: Tempo-dither every frame. 1: Tempo-dither every 2 frames.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SHORT_1LINE_DISABLE	6	1: Disable. 0: Enable.	
	-	5	Reserved.	
	EGWT	4	Encode Gamma Write.	
	-	3:1	Reserved.	
	OUTFRR_EN0	0	Output Free-run Enable.	
1Dh (102F3Ah)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x07**	**Access: R/W**
	TUNE_FIELD_IP	7	Select insert point of one field for VOP_DISP inset signal.	
	-	6:0	Reserved.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	LMT_ADD_NMB[7:0]	7:0	Limit adjust Number in ACC_FPLL mode.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	FPLL_MD1	7	FPLL Mode 1.	
	FPLL_DIS	6	FPLL Stop.	
	-	5:3	Reserved.	
	ADD_LINE_SEL	2	Select Add Line into frame or pixel into line.	
	-	1:0	Reserved.	
1Fh ~ 21h (102F3Eh ~ 102F42h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	DOT	6	Differential Output Type. 0: Normal LVDS/RSDS operation. 1: Reduced-swing LVDS/Increased-swing RSDS.	
	WHTS	5	White Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	BLSK	4	Black Screen (including Main window and Sub window). 0: Disable. 1: Enable.	
	REVERSE	3	REVERSE luminosity. 0: Off. 1: On.	
	-	2:0	Reserved.	
22h (102F44h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	FBLALL_SET	7	Frame buffer less all set.	
	-	6:0	Reserved.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSDCHBLEND	7	OSD Character Blending mode.	
	-	6	Reserved.	
	NBM	5	New Blending Level. 0: Original blending level (BLENDL = 000 means 0% transparency). 1: New blending level (BLENDL = 000 means 12.5% transparency).	
	-	4	Reserved.	
	GATP	3	Gamma Automatically On/Off based on Auto Phase value. 0: Disable. 1: Enable.	
	BLENDL[2:0]	2:0	OSD alpha blending Level. 000: 12.5% transparency. 001: 25.0% transparency. 010: 37.5% transparency.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			011: 50.0%% transparency. 100: 62.5% transparency. 101: 75.0% transparency. 110: 87.5% transparency. 111: 100% transparency.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	MNS_COL[7:0]	7:0	Main Window No Signal Color.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	MBCOL[7:0]	7:0	Main Window Border Color.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	FPLL_NEW_EN	7	Select FPLL output lock point.	
	-	6:0	Reserved.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	GATED_LVL[1:0]	7:6	ODCLK gated level.	
	FLOCK_DL_LN[2:0]	5:3	Delay line number in Flock mode.	
	FLOCK_AH_LN[2:0]	2:0	Ahead line in Flock mode.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM11[7:0]	7:0	Color Matrix Coefficient 11.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM11[12:8]	4:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM12[7:0]	7:0	Color Matrix Coefficient 12.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM12[12:8]	4:0	See description of '102F4Eh'.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM13[7:0]	7:0	Color Matrix Coefficient 13.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM13[12:8]	4:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM21[7:0]	7:0	Color Matrix Coefficient 21.	
29h	**REG102F53**	**7:0**	**Default: 0x00**	**Access: R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F53h)	-	7:5	Reserved.	
	CM21[12:8]	4:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM22[7:0]	7:0	Color Matrix Coefficient 22.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM22[12:8]	4:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM23[7:0]	7:0	Color Matrix Coefficient 23.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM23[12:8]	4:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM31[7:0]	7:0	Color Matrix Coefficient 31.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM31[12:8]	4:0	See description of '102F58h'.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM32[7:0]	7:0	Color Matrix Coefficient 32.	
2Dh (102F5Bh)	**REG102F5B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM32[12:8]	4:0	See description of '102F5Ah'.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: 0x00**	**Access: R/W**
	CM33[7:0]	7:0	Color Matrix Coefficient 33.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CM33[12:8]	4:0	See description of '102F5Ch'.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	FTPS	6	Front-TPSCR. 0: Disable. 1: Enable.	
	CMRND	5	Color Matrix Rounding control.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Disable. 1: Enable.	
	CMC	4	Color Matrix Control. 0: Disable. 1: Enable.	
	-	3	Reserved.	
	RRAN	2	Red Range. 0: 0~255. 1: -128~127.	
	GRAN	1	Green Range. 0: 0~255.1: -128~127.	
	BRAN	0	Blue Range. 0: 0~255. 1: -128~127.	
2Fh (102F5Fh)	**REG102F5F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SSFD	7	Sub window Shift Field. 0: Shift even field. 0: Shift odd field.	
	SSLN[1:0]	6:5	Sub window Shift Line Numbers. 00: Shift 0 line between odd and even field. 01: Shift 1 line between odd and even field. 10: Shift 2 lines between odd and even field. 11: Shift 3 lines between odd and even field.	
	ILIM	4	Insert Line when Interlace Mode. 0: Do not insert. 1: Insert.	
	MSFD	3	Main window Shift Field. 0: Shift even field. 1: Shift odd field.	
	MSLN[2:0]	2:0	Main window Shift Line Numbers. 000: Shift 0 line between odd and even field. 001: Shift 1 line between odd and even field. 010: Shift 2 lines between odd and even field. 011: Shift 3 lines between odd and even field. 1xx: Shift 4 lines between odd and even field.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: RO**
	IFVP[7:0]	7:0	Insert Fraction Vertical Position.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x00**	**Access: RO**
	IFVP[15:8]	7:0	See description of '102F60h'.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: RO**
	IFRACTW[7:0]	7:0	Insert Fraction Width. PD Down value.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: RO**
	IFRACTW[15:8]	7:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: RO**
	OVSSTAT[7:0]	7:0	Output Vertical Total Status. Lock status. Equal to 1 when phase error less than 29h/2Ah.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7	Reserved.	
	OVERDESTAT	6	Output Vertical DE Status.	
	-	5:3	Reserved.	
	OVSSTAT[10:8]	2:0	See description of '102F64h'.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	OHTSTAT0[7:0]	7:0	OHSTAT initial value.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: RO**
	OHTSTAT1[7:0]	7:0	Output H Total Status.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OHTSTAT2[3:0]	3:0	OHSTAT initial value.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	OHTSTAT3[3:0]	3:0	OHSTAT initial value.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0x00**	**Access: R/W**
	FRACST0[7:0]	7:0	Fraction initial value.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: 0x00**	**Access: RO**
	FRACST1[7:0]	7:0	Fraction Status.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	FRACST2[2:0]	2:0	Fraction Status.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:3	Reserved.	
	FRACST3[2:0]	2:0	Fraction Status.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x00**	**Access: R/W**
	HTTMGN[7:0]	7:0	H Total Margin.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x00**	**Access: R/W**
	SSCMGN[7:0]	7:0	SSC Margin.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0x00**	**Access: R/W**
	RSTVALUE0[7:0]	7:0	Read Start initial value.	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0x00**	**Access: RO**
	RSTVALUE1[7:0]	7:0	Read Start Value.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	RSTVALUE2[4:0]	4:0	Read Start initial value.	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:5	Reserved.	
	RSTVALUE3[4:0]	4:0	Read Start Value.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FRONT_BACK	5	Set front back mode.	
	-	4:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	INP8	7	This bit with REG_INE_DRV3 to enable G replace R and B for gamma mapping.	
	ONE_DRV3	6	Gamma use G replace R and B for gamma mapping.	
	GABYP	5	By pass gamma function.	
	-	4:3	Reserved.	
	TUN_FPLL_DL_LN[2:0]	2:0	Delay line numbers of FPLL mode.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: R/W**
	TSTDATA[7:0]	7:0	Reserved.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	LFCOEF1[2:0]	7:5	Loop filter coefficient 1.	
	LFCOEF2[4:0]	4:0	Loop filter coefficient 2.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
42h (102F85h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	TFRACN[7:0]	7:0	Target Fraction Number. / Frame PLL limit RK[7:0].	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7	Reserved.	
	PDP_MASK_EN	6	Reserved.	
	-	5	Reserved.	
	FX_PROT	4	Frame Change Protect.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x40**	**Access: R/W**
	TSTMD_REG_EN	7	Test Mode Register Enable. 0: Disable. 1: Enable.	
	-	6	Reserved.	
	SEE_DEBUG_SEL[2:0]	5:3	See Debug bus output byte enable. Bit0: DI[7:0]. Bit1: DI[15:8]. Bit2: DI[23:16].	
	-	2:0	Reserved.	
46h ~ 48h (102F8Ch ~ 102F90h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	TEST_CLK_MODE	7	0: Disable. 1: Enable.	
	-	6	Reserved.	
	DDR_TEST	5	1: Select DDR 29est bus.	
	TEST_MD_D	4	1: Enable 24-bit test bus output.	
	TEST_MD[3:0]	3:0	Reserved.	
49h ~ 49h (102F92h ~ 102F93h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
4Ah	**REG102F94**	**7:0**	**Default: 0x00**	**Access: RO**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F94h)	BOND_STS[7:0]	7:0	Reserved.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x44**	**Access: R/W**
	LP_SET0[7:0]	7:0	Output PLL Set.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: 0x55**	**Access: R/W**
	LP_SET0[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x00**	**Access: R/W**
	LP_SET1[7:0]	7:0	Output PLL Set.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	OBN10	7	10-bit Bus enable.	
	DITHER_MINUS	6	1: Enable.	
	-	5	Reserved.	
	M_GRG	4	Main window Gamma Rounding.	
	-	3:1	Reserved.	
	GCFE	0	Gamma correction function enable. 0: Off. 1: On.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_HS_ST[7:0]	7:0	OSD new reference h start.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_NEW_REF	7	OSD new reference enable.	
	-	6:4	Reserved.	
	OSD_HS_ST[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_HS_END[7:0]	7:0	OSD new reference h end.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OSD_HS_END[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	OSD_VFDE_ST[7:0]	7:0	OSD new reference v start.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	OSD_VFDE_ST[10:8]	2:0	See description of '102FA8h'.	
55h	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FAAh)	OSD_VFDE_END[7:0]	7:0	OSD new reference v end.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	OSD_VFDE_END[10:8]	2:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIM_HS	7	Limit Htotal by PWM counter enable.	
	NEW_FIELD_SEL	6	Select field created method. 0: Created by Vsync and Hsync. 1: Created by VFDE.	
	SEL_OSD_AL	5	Select OSD down count index. 0: VFDE end. 1: Vsync end.	
	-	4:0	Reserved.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: RO**
	REM[7:0]	7:0	Htoal Remainder value.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	REM[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5DIV[7:0]	7:0	PWM5 CLK div factor.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	PWM5DIV[8]	0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5DUTY[7:0]	7:0	PWM5 period.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: R/W**
	TRACE_PHASE_HTOTAL[7:0]	7:0	New Htotal for fast phase offset reduce, only active when REG_TRACE_PHASE_EN is set to 1.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	TRACE_PHASE_EN	4	Enable modify Htotal for fast phase offset reduce.	
	TRACE_PHASE_HTOTAL[11:8]	3:0	See description of '102FB4h'.	
64h	**REG102FC8**	**7:0**	**Default: 0x07**	**Access: R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FC8h)	BIUCLK_DIV[7:0]	7:0	Calculate VDE ratio BIUCLK divider.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	RPT_VRATIO_EN	0	Report VDE Vtotal ratio enable.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_0_REG[7:0]	7:0		
65h (102FCBh)	**REG102FCB**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_1_REG[7:0]	7:0		
66h (102FCCh)	**REG102FCC**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_2_REG[7:0]	7:0		
66h (102FCDh)	**REG102FCD**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_3_REG[7:0]	7:0		
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_4_REG[7:0]	7:0		
67h (102FCFh)	**REG102FCF**	**7:0**	**Default: 0x00**	**Access: R/W**
	PIP_OP2_5_REG[7:0]	7:0		
68h (102FD0h)	**REG102FD0**	**7:0**	**Default: 0x00**	**Access: RO**
	VDE_PRD_VALUE[7:0]	7:0	Input VDE PRD value.	
68h (102FD1h)	**REG102FD1**	**7:0**	**Default: 0x00**	**Access: RO**
	VDE_PRD_VALUE[15:8]	7:0	See description of '102FD0h'.	
69h (102FD2h)	**REG102FD2**	**7:0**	**Default: 0x00**	**Access: RO**
	VTT_PRD_VALUE[7:0]	7:0	Input Vtt PRD value.	
69h (102FD3h)	**REG102FD3**	**7:0**	**Default: 0x00**	**Access: RO**
	VTT_PRD_VALUE[15:8]	7:0	See description of '102FD2h'.	
6Ah (102FD4h)	**REG102FD4**	**7:0**	**Default: 0x00**	**Access: R/W**
	HIFRC_SROT	7	Enable HIFRC spatial rotation.	
	RAN[1:0]	6:5	Enable HIFRC Random noise latch for rotation.	
	F2_EN	4	Enable noise repeats 2 frames.	
	NEW_DITH_M	3	New dither method select.	
	-	2	Reserved.	
	PSEUDO_EN_T	1	Enable dither pattern rotation line by line.	
	PSEUDO_EN_S	0	Enable dither pattern rotation frame by frame.	
6Ah	**REG102FD5**	**7:0**	**Default: 0x00**	**Access: R/W**

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FD5h)	-	7	Reserved.	
	OSD_HDE_SEL	6	Select OSD_HDE with VFDE signal. 0: OSD_HDE = HFDE. 1: OSD_HDE = HFDE & VFDE.	
	PSE_RST_NUM[1:0]	5:4	Frame period for dither pseudo noise reset.	
	H_RAN_EN	3	H direction using random noise enable for HIFRC.	
	NEW_ACBD	2	Swap HIFRC probability sequence.	
	OLD_HIFRC	1	Select old HIFRC dither method.	
	RAN_DIR_EN	0	Enable noise as rotate direction.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default: 0x00**	**Access: R/W**
	LUT_RAM_ADDRESS[7:0]	7:0	LUT table r/w address.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default: 0x00**	**Access: R/W**
	LUT_W_FLAG2	7	LUT table blue write command.	
	LUT_W_FLAG1	6	LUT table green write command.	
	LUT_W_FLAG0	5	LUT table red write command.	
	-	4:0	Reserved.	
6Dh (102FDBh)	**REG102FDB**	**7:0**	**Default: 0x00**	**Access: R/W**
	LUT_R_FLAG2	7	LUT table blue read command.	
	LUT_R_FLAG1	6	LUT table green read command.	
	LUT_R_FLAG0	5	LUT table red read command.	
	-	4:0	Reserved.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default: 0x00**	**Access: R/W**
	WR_R[7:0]	7:0	Data write to R LUT SRAM.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	WR_R[11:8]	3:0	See description of '102FDCh'.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default: 0x00**	**Access: R/W**
	WR_G[7:0]	7:0	Data write to G LUT SRAM.	
6Fh (102FDFh)	**REG102FDF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	WR_G[11:8]	3:0	See description of '102FDEh'.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	WR_B[7:0]	7:0	Data write to B LUT SRAM.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (102FE1h)	**REG102FE1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	WR_B[11:8]	3:0	See description of '102FE0h'.	
71h (102FE2h)	**REG102FE2**	**7:0**	**Default: 0x00**	**Access: RO**
	RD_R[7:0]	7:0	Data read from R LUT SRAM.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	RD_R[11:8]	3:0	See description of '102FE2h'.	
72h (102FE4h)	**REG102FE4**	**7:0**	**Default: 0x00**	**Access: RO**
	RD_G[7:0]	7:0	Data read from G LUT SRAM.	
72h (102FE5h)	**REG102FE5**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	RD_G[11:8]	3:0	See description of '102FE4h'.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default: 0x00**	**Access: RO**
	RD_B[7:0]	7:0	Data read from B LUT SRAM.	
73h (102FE7h)	**REG102FE7**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	RD_B[11:8]	3:0	See description of '102FE6h'.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7:4	Reserved.	
	CLR_MLOAD_TOO_SLOW	3	Clear auto mload gamma too slow flag.	
	MLOAD_TOO_SLOW	2	Auto mload gamma too slow flag.	
	AUTO_MLOAD_SWITCH	1	Enable auto mload gamma switch gamma table by frame.	
	AUTO_MLOAD_GAMMA	0	Enable auto mload gamma function.	
75h (102FEAh)	**REG102FEA**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE0[7:0]	7:0	Gamma table base address 0.	
75h (102FEBh)	**REG102FEB**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE0[15:8]	7:0	See description of '102FEAh'.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE0[23:16]	7:0	See description of '102FEAh'.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE1[7:0]	7:0	Gamma table base address 1.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE1[15:8]	7:0	See description of '102FEEh'.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_GAMMA_BASE1[23:16]	7:0	See description of '102FEEh'.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_CNT[7:0]	7:0	Load gamma table from DRAM number.	
7Ah (102FF4h)	**REG102FF4**	**7:0**	**Default: 0x00**	**Access: R/W**
	R_MAX_BASE0[7:0]	7:0	Max value for R channel gamma table 0.	
7Ah (102FF5h)	**REG102FF5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	R_MAX_BASE0[11:8]	3:0	See description of '102FF4h'.	
7Bh (102FF6h)	**REG102FF6**	**7:0**	**Default: 0x00**	**Access: R/W**
	R_MAX_BASE1[7:0]	7:0	Max value for R channel gamma table 1.	
7Bh (102FF7h)	**REG102FF7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	R_MAX_BASE1[11:8]	3:0	See description of '102FF6h'.	
7Ch (102FF8h)	**REG102FF8**	**7:0**	**Default: 0x00**	**Access: R/W**
	G_MAX_BASE0[7:0]	7:0	Max value for G channel gamma table 0.	
7Ch (102FF9h)	**REG102FF9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	G_MAX_BASE0[11:8]	3:0	See description of '102FF8h'.	
7Dh (102FFAh)	**REG102FFA**	**7:0**	**Default: 0x00**	**Access: R/W**
	G_MAX_BASE1[7:0]	7:0	Max value for G channel gamma table 1.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	G_MAX_BASE1[11:8]	3:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_MAX_BASE0[7:0]	7:0	Max value for B channel gamma table 0.	

VOP Register (Bank = 102F, Sub-bank = 10)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	B_MAX_BASE0[11:8]	3:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_MAX_BASE1[7:0]	7:0	Max value for B channel gamma table 1.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	B_MAX_BASE1[11:8]	3:0	See description of '102FFEh'.	

SCMI Register (Bank = 102F, Sub-bank = 12)

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	FBL_ONLY	7	F2 frame buffer less mode enable.	
	-	6	Reserved.	
	RGB_YUV444_10BIT_F2	5	F2 RGB/YUV 444 10-bit format.	
	RGB_YUV444_8BIT_F2	4	F2 RGB/YUV 444 8-bit format.	
	MEM_MODE6_TO_7_F2	3	F2 memory data configuration from mode 6 change to mode 7.	
	MEM_MODE5_TO_7_F2	2	F2 memory data configuration from mode 5 change to mode 7.	
	MEM_MODE5_TO_6_F2	1	F2 memory data configuration from mode 5 change to mode 6.	
	MEM_MODE5_TO_4_F2	0	F2 memory data configuration from mode 5 change to mode 4.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_F1_EN	7	Enable OPM F1 register.	
	MOTION_TH1_F2[2:0]	6:4	F2 Motion Threshold for normal case.	
	STILL_MODE_F2	3	F2 image freeze enable.	
	DE_INTL_MD_F2[2:0]	2:0	F2 IP memory data format.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_MEM_CONFIG_F2[3:0]	7:4	F2 OP memory data format.	
	IPM_MEM_CONFIG_F2[3:0]	3:0	F2 IP memory data format.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	CAPTURE_START_F2	7	F2 image capture start.	
	IPM_READ_OFF_F2	6	F2 force IP read request disable.	
	MADI_FORCE_OFF_F2	5	F2 force MADi off.	
	MADI_FORCE_ON_F2	4	F2 force MADi on.	
	FBL_25D	3	F2 frame buffer less de-interlace mode.	
	-	2	Reserved.	
	OPM_CONFIG_DEFINE_F2	1	F2 OP enable define memory data format.	
	IPM_CONFIG_DEFINE_F2	0	F2 IP enable define memory data format.	
03h	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F06h)	IPM_REQ_RST_F2	7	F2 reset IP to MIU request signal.	
	OPM_LINEAR_BASE_SEL_F2	6	F2 linear mode base address selection.	
	OPM_LINEAR_EN_F2	5	F2 OP linear address enable.	
	-	4	Reserved.	
	OPM_4READ_EN_F2	3	F2 OP read 4 fields enable.	
	OPM_3READ_EN_F2	2	F2 OP read 3 fields enable.	
	OPM_2READ_EN_F2	1	F2 OP read 2 fields enable.	
	OPM_1READ_EN_F2	0	F2 OP read 1 field enable.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x08**	**Access: R/W**
	FRC_AUTO	7	Insert/Lock Vsync signal FRC auto select.	
	LOCK_F1	6	Insert/Lock Vsync signal lock with F1.	
	IPM_V_MIRROR_F2	5	F2 IP Vertical mirror enable.	
	IPM_H_MIRROR_F2	4	F2 IP Horizontal mirror enable.	
	FILM_HIGH_PRI_F2	3	F2 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F2	2	F2 OP film dot line data select.	
	DOT_LN_PON_SEL_F2	1	F2 OP MADi dot line data select.	
	YC_SWAP_EN_F2	0	F2 OP Y/C data swap enable.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	3FRAME_MODE_F2	7	F2 3 frames buffer for progressive mode.	
	-	6:4	Reserved.	
	Y8_M4_ONLY_MODE_F2	3	F2 FB store Y8/M4 only mode.	
	Y8_ONLY_MODE_F2	2	F2 FB store Y-8bit only.	
	BOB_YMR_10_EN_F2	1	F2 10-bit Bob mode with Y motion.	
	BOB_YMR_8_EN_F2	0	F2 8-bit Bob mode with Y motion.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	DUMMY04_14_14	6	F2 FB store Y-8bits only.	
	IPM_444_READ_EN_F2	5	F2 IP 444 format read from memory enable.	
	IP_BYPASS_INTERLACE_FILM_F2	4	Film-supported bypass interlace mode.	
	IP_BYPASS_ALL_F2	3	F2 IP bypass to OPM, OPM read request off.	
	IP_BYPASS_INTERLACE_F2	2	F2 IP bypass to OPM, OPM interlace read from MIU/IP.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	IPM_Y_ONLY_W_F2	1	F2 IP write Y only.	
	IPM_Y_ONLY_R_F2	0	F2 IP read Y only.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	W_BANK_RST_F2	7	F2 MEMYSNC write bank reset.	
	IPM_WREQ_HPRI_SEL_F2	6	F2 IPM WREQ high priority selection. 0: IPM local priority. 1: IP2_ADJ priority.	
	FRC_FREEMD_F2	5	F2 Force output odd/even toggle when 2DDi for interlace input.	
	MIU_SELECT_F2	4	F2 access MIU0 or MIU1 select.	
	FRC_WITH_LCNT_F2	3	F2 frame rate convert dependence with IP write line count.	
	W_LCNT_STATUS_SEL_F2[2:0]	2:0	F2 IP write line count status select.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY05_9_15[6:0]	7:1		
	BK_FIELD_SEL_F2	0	F2 MEMYSNC FD selection.	
06h (102F0Ch)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
06h (102F0Dh)	**REG102F0D**	**7:0**	**Default: 0x00**	**Access: R/W**
	RW_BANK_MAP_MSB_F2	7	F2 MSB bit of read/write bank mapping mode.	
	OPM_RBANK_SEL_MSB_F2	6	F2 OP force read bank select MSB.	
	-	5:0	Reserved.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x88**	**Access: R/W**
	W_VP_CNT_CLR_F2	7	F2 IP write mask field count clear.	
	W_MASK_MODE_F2[2:0]	6:4	F2 IP write mask number by field.	
	IPM_STATUS_CLR_F2	3	F2 IP status clear enable.	
	IPM_RREQ_FORCE_F2	2	F2 IP read request force enable.	
	IPM_RREQ_OFF_F2	1	F2 IP read request disable.	
	IPM_WREQ_OFF_F2	0	F2 IP write request disable.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x40**	**Access: R/W**
	RW_BANK_MAP_F2[2:0]	7:5	F2 read/write bank mapping mode.	
	BK_FIELD_INV_F2	4	F2 read/write bank inverse.	
	OPM_RBANK_FORCE_F2	3	F2 OP force read bank enable.	
	OPM_RBANK_SEL_F2[2:0]	2:0	F2 OP force read bank select.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR0_F2[7:0]	7:0	F2 IP frame buffer base address 0.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F10h'.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F10h'.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	IPM_BASE_ADDR0_F2[24]	0	See description of '102F10h'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_OFFSET_F2[7:0]	7:0	F2 IP frame buffer line offset (pixel unit).	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	IPM_OFFSET_F2[12:8]	4:0	See description of '102F1Ch'.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_FETCH_NUM_F2[7:0]	7:0	F2 IP fetch pixel number of one line.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	IPM_FETCH_NUM_F2[12:8]	4:0	See description of '102F1Eh'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F2[7:0]	7:0	F2 OP frame buffer base address 0.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F2[15:8]	7:0	See description of '102F20h'.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F2[23:16]	7:0	See description of '102F20h'.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR0_F2[24]	0	See description of '102F20h'.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F2[7:0]	7:0	F2 OP frame buffer base address 1.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F2[15:8]	7:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F2[23:16]	7:0	See description of '102F24h'.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR1_F2[24]	0	See description of '102F24h'.	
14h ~ 14h (102F28h ~ 102F29h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_OFFSET_F2[7:0]	7:0	F2 OP frame buffer line offset (pixel unit).	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F2[12:8]	4:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_FETCH_NUM_F2[7:0]	7:0	F2 OP fetch pixel number of one line.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F2[11:8]	3:0	See description of '102F2Eh'.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_VCNT_LIMIT_NUM_F2[7:0]	7:0	F2 IP line count limit number for frame buffer write.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_VCNT_LIMIT_EN_F2	7	F2 IP line count limit enable.	
	-	6:5	Reserved.	
	IPM_VCNT_LIMIT_NUM_F2[12:8]	4:0	See description of '102F30h'.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:5	Reserved.	
	FIELD_NUM_F2[4:0]	4:0	F2 field number.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x10**	**Access: R/W**
	OPM_FIELD_NUM_DEFINE_F2	7	Enable OPM F2 field number define.	
	OPM_FIELD_NUM_F2[4:0]	6:2	OPM F2 field number.	
	OPM_8READ_EN_F2	1	F2 OPM 8 read mode enable.	
	OPM_6READ_EN_F2	0	F2 OPM 6 read mode enable.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_W_LIMIT_ADR_F2[7:0]	7:0	F2 IP write limit address.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_W_LIMIT_ADR_F2[15:8]	7:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_W_LIMIT_ADR_F2[23:16]	7:0	See description of '102F34h'.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	IPM_W_LIMIT_EN_F2	7	F2 IP write limit enable.	
	IPM_W_LIMIT_MIN_F2	6	F2 IP write limit flag. 0: maximum. 1: minimum.	
	-	5:1	Reserved.	
	IPM_W_LIMIT_ADR_F2[24]	0	See description of '102F34h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	SW_HMIR_OFFSET_F2[7:0]	7:0	F2 IP H mirror line offset.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	SW_HMIR_OFFSET_EN_F2	7	F2 IP H mirror line offset software setting enable.	
	SW_HMIR_OFFSET_F2[14:8]	6:0	See description of '102F38h'.	
1Dh ~ 1Fh	**-**	**7:0**	**Default: -**	**Access: -**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F3Ah ~ 102F3Fh)	-	-	Reserved.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_RREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for read request.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_RREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for read request.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_WREQ_THRD_F2[7:0]	7:0	F2 IP FIFO threshold for write request.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_WREQ_HPRI_F2[7:0]	7:0	F2 IP high priority threshold for write request.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_RREQ_MAX_F2[7:0]	7:0	F2 IP read request max number.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x10**	**Access: R/W**
	IPM_WREQ_MAX_F2[7:0]	7:0	F2 IP write request max number.	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x10**	**Access: R/W**
	OPM_RREQ_THRD[7:0]	7:0	OP FIFO threshold for read request.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x10**	**Access: R/W**
	OPM_RREQ_HPRI[7:0]	7:0	OP high priority threshold for read request.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x20**	**Access: R/W**
	OPM_RREQ_MAX[7:0]	7:0	OP read request max number.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_LBUF_LEN_EN	7	OP define line buffer length enable.	
	OPM_LBUF_LENGTH[6:0]	6:0	OP line buffer length for memory data read.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x28**	**Access: R/W**
	IPM_RFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data read.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x28**	**Access: R/W**
	IPM_WFIFO_DEPTH_F2[7:0]	7:0	F2 IP line buffer length for memory data write.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_FLOW_CTRL_CNT[7:0]	7:0	OP request flow control count.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:5	Reserved.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OPM_PRE_DELTA_0_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at real line case.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
2Dh (102F5Ah)	**REG102F5A**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F2[4:0]	4:0	F2 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
2Eh (102F5Ch)	**REG102F5C**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at real line case.	
2Eh (102F5Dh)	**REG102F5D**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
2Fh (102F5Eh)	**REG102F5E**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F2[4:0]	4:0	F2 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	IPM_3D_SBS_FORCE_EN_F2	1	F2 IPM 3D side by side input enable.	
	IPM_3D_EN_F2	0	F2 IPM 3D input enable.	
31h ~ 33h (102F62h ~ 102F67h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY34_7_7	7	HDMI 3D OPM side by side read using PIP.	
	-	6:0	Reserved.	
35h	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: RO**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F6Ah)	STATUS_READ_35_F2[7:0]	7:0	F2 status read out for debug.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_35_F2[15:8]	7:0	See description of '102F6Ah'.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_36_F2[7:0]	7:0	F2 status read out for debug.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_36_F2[15:8]	7:0	See description of '102F6Ch'.	
38h (102F70h)	**REG102F70**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_38_F2[7:0]	7:0	F2 status read out for debug.	
38h (102F71h)	**REG102F71**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_38_F2[15:8]	7:0	See description of '102F70h'.	
39h (102F72h)	**REG102F72**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_39_F2[7:0]	7:0	F2 status read out for debug.	
39h (102F73h)	**REG102F73**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_39_F2[15:8]	7:0	See description of '102F72h'.	
3Ah (102F74h)	**REG102F74**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3A_F2[7:0]	7:0	F2 status read out for debug.	
3Ah (102F75h)	**REG102F75**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3A_F2[15:8]	7:0	See description of '102F74h'.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3B_F2[7:0]	7:0	F2 status read out for debug.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3B_F2[15:8]	7:0	See description of '102F76h'.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3C_F2[7:0]	7:0	F2 status read out for debug.	
3Ch (102F79h)	**REG102F79**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3C_F2[15:8]	7:0	See description of '102F78h'.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Dh (102F7Ah)	**REG102F7A**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3D_F2[7:0]	7:0	F2 status read out for debug.	
3Dh (102F7Bh)	**REG102F7B**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3D_F2[15:8]	7:0	See description of '102F7Ah'.	
3Eh (102F7Ch)	**REG102F7C**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3E_F2[7:0]	7:0	F2 status read out for debug.	
3Eh (102F7Dh)	**REG102F7D**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_3E_F2[15:8]	7:0	See description of '102F7Ch'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x08**	**Access: R/W**
	DUMMY40_4_15[3:0]	7:4		
	UPDATE_MEM_CONFIG_EN	3	Update memory format enable.	
	-	2	Reserved.	
	IPM_REG_DBF_EN_F2	1	F2 Register latch with input V sync enable.	
	OPM_REG_DBF_EN	0	Register latch with output V sync enable.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY40_4_15[11:4]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY41_7_6[1:0]	7:6		
	-	5:0	Reserved.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MADI_FORCE_OFF_F1	5	F1 force MADi off.	
	MADI_FORCE_ON_F1	4	F1 force MADi on.	
	-	3:0	Reserved.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OPM_4READ_EN_F1	3	F1 OP read 4 fields enable.	
	OPM_3READ_EN_F1	2	F1 OP read 3 fields enable.	
	OPM_2READ_EN_F1	1	F1 OP read 2 fields enable.	
	OPM_1READ_EN_F1	0	F1 OP read 1 field enable.	
43h	**REG102F87**	**7:0**	**Default: 0x08**	**Access: R/W**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F87h)	-	7:4	Reserved.	
	FILM_HIGH_PRI_F1	3	F1 OP dot line select high priority when film mode active.	
	FILM_NOC_INVERT_F1	2	F1 OP film dot line data select.	
	DOT_LN_PON_SEL_F1	1	F1 OP MADi dot line data select.	
	-	0	Reserved.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DUMMY44_2_3[1:0]	3:2		
	-	1:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY45_9_15[6:0]	7:1		
	-	0	Reserved.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY46_0_7[7:0]	7:0		
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F1[7:0]	7:0	F1 OP frame buffer base address 0.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F1[15:8]	7:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR0_F1[23:16]	7:0	See description of '102FA0h'.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR0_F1[24]	0	See description of '102FA0h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F1[7:0]	7:0	F1 OP frame buffer base address 1.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F1[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_BASE_ADDR1_F1[23:	7:0	See description of '102FA4h'.	

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	16]			
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	OPM_BASE_ADDR1_F1[24]	0	See description of '102FA4h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_MWE_OFFSET_F1[7:0]	7:0	F1 OP demo mode pixel offset (pixel unit).	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OPM_MWE_OFFSET_F1[11:8]	3:0	See description of '102FA8h'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_OFFSET_F1[7:0]	7:0	F1 OP frame buffer line offset (pixel unit).	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_OFFSET_F1[12:8]	4:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: R/W**
	OPM_FETCH_NUM_F1[7:0]	7:0	F1 OP fetch pixel number of one line.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	OPM_FETCH_NUM_F1[11:8]	3:0	See description of '102FAEh'.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	OPM_8READ_EN_F1	1	F1 OPM 8read mode enable.	
	OPM_6READ_EN_F1	0	F1 OPM 6read mode enable.	
5Eh ~ 5Fh (102FBCh ~ 102FBFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY66_13_15[2:0]	7:5		
	-	4:0	Reserved.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY67_4_15[3:0]	7:4		

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:0	Reserved.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY67_4_15[11:4]	7:0	See description of '102FCEh'.	
6Ch (102FD8h)	**REG102FD8**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_0_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at real line case.	
6Ch (102FD9h)	**REG102FD9**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_1_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC0 case.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_PRE_DELTA_2_F1[4:0]	4:0	F1 OP previous data rbank difference between current data rbank at dot line and NOC1 case.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_0_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at real line case.	
6Eh (102FDDh)	**REG102FDD**	**7:0**	**Default: 0x12**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_1_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC0 case.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:5	Reserved.	
	OPM_EXT_DELTA_2_F1[4:0]	4:0	F1 OP extend data rbank difference between current data rbank at dot line and NOC1 case.	
70h ~ 73h (102FE0h ~ 102FE6h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
74h (102FE8h)	**REG102FE8**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY74_7_7	7		
	-	6:0	Reserved.	
7Dh	**REG102FFA**	**7:0**	**Default: 0x00**	**Access: RO**

SCMI Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FFAh)	STATUS_READ_7D_F1[7:0]	7:0	F1 status read out for debug.	
7Dh (102FFBh)	**REG102FFB**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_7D_F1[15:8]	7:0	See description of '102FFAh'.	
7Eh (102FFCh)	**REG102FFC**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_7E_F1[7:0]	7:0	F1 status read out for debug.	
7Eh (102FFDh)	**REG102FFD**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_7E_F1[15:8]	7:0	See description of '102FFCh'.	
7Fh (102FFEh)	**REG102FFE**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_7F_F1[7:0]	7:0	F1 status read out for debug.	
7Fh (102FFFh)	**REG102FFF**	**7:0**	**Default: 0x00**	**Access: RO**
	STATUS_READ_7F_F1[15:8]	7:0	See description of '102FFEh'.	

SCMI_SUB Register (Bank = 102F, Sub-bank = 12)

SCMI_SUB Register (Bank = 102F, Sub-bank = 12)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h ~ 44h (102F80h ~ 102F89h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: R/W**
	W_BANK_RST_F1	7	F1 MEMYSNC write bank reset.	
	IPM_WREQ_HPRI_SEL_F1	6	F1 IPM WREQ high priority selection. 0: IPM local priority. 1: IP2_ADJ priority.	
	-	5:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	BK_FIELD_SEL_F1	0	F2 MEMYSNC FD selection.	
46h ~ 7Ch (102F8Dh ~ 102FF9h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

ACE Register (Bank = 102F, Sub-bank = 18)

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_FCC_8T_EN	7	Main window FCC region 8 enable.	
	MAIN_FCC_7T_EN	6	Main window FCC region 7 enable.	
	MAIN_FCC_6T_EN	5	Main window FCC region 6 enable.	
	MAIN_FCC_5T_EN	4	Main window FCC region 5 enable.	
	MAIN_FCC_4T_EN	3	Main window FCC region 4 enable.	
	MAIN_FCC_3T_EN	2	Main window FCC region 3 enable.	
	MAIN_FCC_2T_EN	1	Main window FCC region 2 enable.	
	MAIN_FCC_1T_EN	0	Main window FCC region 1 enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	FCC_DITHER_EN	6	FCC dither bit enable.	
	FCC_RESERVED_1[4:0]	5:1	Reserved.	
	MAIN_FCC_9T_EN	0	Main window FCC window 9 enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_FCC_8T_EN	7	Sub window FCC region 8 enable.	
	SUB_FCC_7T_EN	6	Sub window FCC region 7 enable.	
	SUB_FCC_6T_EN	5	Sub window FCC region 6 enable.	
	SUB_FCC_5T_EN	4	Sub window FCC region 5 enable.	
	SUB_FCC_4T_EN	3	Sub window FCC region 4 enable.	
	SUB_FCC_3T_EN	2	Sub window FCC region 3 enable.	
	SUB_FCC_2T_EN	1	Sub window FCC region 2 enable.	
	SUB_FCC_1T_EN	0	Sub window FCC region 1 enable.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SUB_FCC_9T_EN	0	Sub window FCC region 9 enable.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T1[7:0]	7:0	FCC region 1 Cb target.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T1[7:0]	7:0	FCC region 1 Cr target.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T2[7:0]	7:0	FCC region 2 Cb target.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T2[7:0]	7:0	FCC region 2 Cr target.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T3[7:0]	7:0	FCC region 3 Cb target.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T3[7:0]	7:0	FCC region 3 Cr target.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T4[7:0]	7:0	FCC region 4 Cb target.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T4[7:0]	7:0	FCC region 4 Cr target.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T5[7:0]	7:0	FCC region 5 Cb target.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T5[7:0]	7:0	FCC region 5 Cr target.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T6[7:0]	7:0	FCC region 6 Cb target.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T6[7:0]	7:0	FCC region 6 Cr target.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T7[7:0]	7:0	FCC region 7 Cb target.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T7[7:0]	7:0	FCC region 7 Cr target.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CB_T8[7:0]	7:0	FCC region 8 Cb target.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_CR_T8[7:0]	7:0	FCC region 8 Cr target.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FCC_K_2T[3:0]	7:4	FCC region 2 strength.	
	FCC_K_1T[3:0]	3:0	FCC region 1 strength.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FCC_K_4T[3:0]	7:4	FCC region 4 strength.	
	FCC_K_3T[3:0]	3:0	FCC region 3 strength.	
21h	**REG102F42**	**7:0**	**Default: 0xFF**	**Access: R/W**

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F42h)	FCC_K_6T[3:0]	7:4	FCC region 6 strength.	
	FCC_K_5T[3:0]	3:0	FCC region 5 strength.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FCC_K_8T[3:0]	7:4	FCC region 8 strength.	
	FCC_K_7T[3:0]	3:0	FCC region 7 strength.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	FCC_K_9T[3:0]	3:0	FCC region 9 strength.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN1_CB_UP[1:0]	7:6	FCC region 1 target Cb up distance.	
	FCC_WIN1_CB_DOWN[1:0]	5:4	FCC region 1 target Cb down distance.	
	FCC_WIN1_CR_UP[1:0]	3:2	FCC region 1 target Cr up distance.	
	FCC_WIN1_CR_DOWN[1:0]	1:0	FCC region 1 target Cr down distance.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN2_CB_UP[1:0]	7:6	FCC region 2 target Cb up distance.	
	FCC_WIN2_CB_DOWN[1:0]	5:4	FCC region 2 target Cb down distance.	
	FCC_WIN2_CR_UP[1:0]	3:2	FCC region 2 target Cr up distance.	
	FCC_WIN2_CR_DOWN[1:0]	1:0	FCC region 2 target Cr down distance.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN3_CB_UP[1:0]	7:6	FCC region 3 target Cb up distance.	
	FCC_WIN3_CB_DOWN[1:0]	5:4	FCC region 3 target Cb down distance.	
	FCC_WIN3_CR_UP[1:0]	3:2	FCC region 3 target Cr up distance.	
	FCC_WIN3_CR_DOWN[1:0]	1:0	FCC region 3 target Cr down distance.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN4_CB_UP[1:0]	7:6	FCC region 4 target Cb up distance.	
	FCC_WIN4_CB_DOWN[1:0]	5:4	FCC region 4 target Cb down distance.	
	FCC_WIN4_CR_UP[1:0]	3:2	FCC region 4 target Cr up distance.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FCC_WIN4_CR_DOWN[1:0]	1:0	FCC region 4 target Cr down distance.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN5_CB_UP[1:0]	7:6	FCC region 5 target Cb up distance.	
	FCC_WIN5_CB_DOWN[1:0]	5:4	FCC region 5 target Cb down distance.	
	FCC_WIN5_CR_UP[1:0]	3:2	FCC region 5 target Cr up distance.	
	FCC_WIN5_CR_DOWN[1:0]	1:0	FCC region 5 target Cr down distance.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN6_CB_UP[1:0]	7:6	FCC region 6 target Cb up distance.	
	FCC_WIN6_CB_DOWN[1:0]	5:4	FCC region 6 target Cb down distance.	
	FCC_WIN6_CR_UP[1:0]	3:2	FCC region 6 target Cr up distance.	
	FCC_WIN6_CR_DOWN[1:0]	1:0	FCC region 6 target Cr down distance.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN7_CB_UP[1:0]	7:6	FCC region 7 target Cb up distance.	
	FCC_WIN7_CB_DOWN[1:0]	5:4	FCC region 7 target Cb down distance.	
	FCC_WIN7_CR_UP[1:0]	3:2	FCC region 7 target Cr up distance.	
	FCC_WIN7_CR_DOWN[1:0]	1:0	FCC region 7 target Cr down distance.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	FCC_WIN8_CB_UP[1:0]	7:6	FCC region 8 target Cb up distance.	
	FCC_WIN8_CB_DOWN[1:0]	5:4	FCC region 8 target Cb down distance.	
	FCC_WIN8_CR_UP[1:0]	3:2	FCC region 8 target Cr up distance.	
	FCC_WIN8_CR_DOWN[1:0]	1:0	FCC region 8 target Cr down distance.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FCC_WIN9_CB[2:0]	5:3	FCC region 9 target Cb distance.	
	FCC_WIN9_CR[2:0]	2:0	FCC region 9 target Cr distance.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (102F51h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_ICC_EN	6	Main window ICC enable.	
	-	5:3	Reserved.	
	SUB_ICC_EN	2	Sub window ICC enable.	
	-	1:0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_R[3:0]	3:0	Main window ICC saturation adjustment of R.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_G[3:0]	3:0	Main window ICC saturation adjustment of G.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_B[3:0]	3:0	Main window ICC saturation adjustment of B.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_C[3:0]	3:0	Main window ICC saturation adjustment of C.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_M[3:0]	3:0	Main window ICC saturation adjustment of M.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_Y[3:0]	3:0	Main window ICC saturation adjustment of Y.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_SA_USER_F[3:0]	3:0	Main window ICC saturation adjustment of F.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_SIGN_SA_USER[7:0]	7:0	Main window ICC decrease saturation. [0]: Other color. [1]: Red.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			[2]: Green. [3]: Blue. [4]: Cyan. [5]: Magenta. [6]: Yellow. [7]: Flesh.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_SIGN_SA_USER[7:0]	7:0	Sub window ICC decrease saturation. [0]: Other color. [1]: Red. [2]: Green. [3]: Blue. [4]: Cyan. [5]: Magenta. [6]: Yellow. [7]: Flesh.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	COMMON_MINUS_GAIN[4:0]	4:0	ICC decrease saturation common gain.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SA_MIN[6:0]	6:0	ICC decrease saturation minimum threshold.	
37h ~ 3Bh (102F6Eh ~ 102F77h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
3Ch (102F78h)	**REG102F78**	**7:0**	**Default: 0xFF**	**Access: R/W**
	WPL_WHITE_PEAK_LIMIT_THRD[7:0]	7:0	White peak limit threshold.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_IBC_EN	7	Main window IBC enable.	
	SUB_IBC_EN	6	Sub window IBC enable.	
	-	5:0	Reserved.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YR_ADJ[5:0]	5:0	Main window IBC Y adjustment of R.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YG_ADJ[5:0]	5:0	Main window IBC Y adjustment of G.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YB_ADJ[5:0]	5:0	Main window IBC Y adjustment of B.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YC_ADJ[5:0]	5:0	Main window IBC Y adjustment of C.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YM_ADJ[5:0]	5:0	Main window IBC Y adjustment of M.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YY_ADJ[5:0]	5:0	Main window IBC Y adjustment of Y.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_YF_ADJ[5:0]	5:0	Main window IBC Y adjustment of F.	
48h (102F91h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_HIGH_PASS_EN	7	Main window Y H_coring as high pass filter.	
	MAIN_Y_TABLE_STEP[2:0]	6:4	Main window Y H_coring LUT step.	
	MAIN_PC_MODE	3	Main window PC mode.	
	-	2	Reserved.	
	MAIN_Y_BAND2_H_CORING_EN	1	Main window Y band2 H_coring enable.	
	MAIN_Y_BAND1_H_CORING_EN	0	Main window Y band1 H_coring enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_HIGH_PASS_EN	7	Main window C H_coring as high pass filter.	
	MAIN_C_TABLE_STEP[2:0]	6:4	Main window C H_coring LUT step.	
	MAIN_WHITE_PEAK_LIMIT	3	Main window white peak limit enable.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	_EN			
	-	2	Reserved.	
	MAIN_C_BAND2_H_CORING_EN	1	Main window C band2 H_coring enable.	
	MAIN_C_BAND1_H_CORING_EN	0	Main window C band1 H_coring enable.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_GAIN_TABLE1[7:0]	7:0	Main window Y gain table 1.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_GAIN_TABLE2[7:0]	7:0	Main window Y gain table 2.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_GAIN_TABLE3[7:0]	7:0	Main window Y gain table 3.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_GAIN_TABLE4[7:0]	7:0	Main window Y gain table 4.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_GAIN_TABLE1[7:0]	7:0	Main window C gain table 1.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_GAIN_TABLE2[7:0]	7:0	Main window C gain table 2.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_GAIN_TABLE3[7:0]	7:0	Main window C gain table 3.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_C_GAIN_TABLE4[7:0]	7:0	Main window C gain table 4.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_Y_NOISE_MASKING_EN	7	Main window horizontal Y NMR enable.	
	MAIN_Y_COLOR_NOISE_MASKING_EN	6	Main window horizontal Y NMR color adaptive enable.	

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MAIN_Y_NOISE_MASK_GAIN[5:0]	5:0	Main window horizontal Y NMR gain (xxxx.xx).	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	MAIN_Y_NM_MIN_THRD[3:0]	7:4	Main window Y mosquito noise REMOVEMIN value threshold.	
	MAIN_Y_NM_MAX_THRD[3:0]	3:0	Main window Y mosquito noise remove max value threshold.	
57h ~ 58h (102FAEh ~ 102FB0h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_WHITE_PEAK_LIMIT_EN	3	Sub window white peak limit enable.	
	-	2:0	Reserved.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_Y_NOISE_MASKING_EN	7	Sub window horizontal Y NMR enable.	
	SUB_Y_COLOR_NOISE_MASKING_EN	6	Sub window horizontal Y NMR color adaptive enable.	
	-	5:0	Reserved.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_Y_DITHER_EN	6	Sub window horizontal Y NMR dither enable.	
	-	5	Reserved.	
	MAIN_Y_DITHER_EN	4	Main window horizontal Y NMR dither enable.	
	-	3:0	Reserved.	
5Fh (102FBFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_IHC_EN	7	Main window IHC enable.	
	SUB_IHC_EN	6	Sub window IHC enable.	
	-	5:0	Reserved.	
60h	**-**	**7:0**	**Default: -**	**Access: -**

ACE Register (Bank = 102F, Sub-bank = 18)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FC1h)	-	-	Reserved.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_R[6:0]	6:0	Main window IHC hue adjustment of R.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_G[6:0]	6:0	Main window IHC hue adjustment of G.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_B[6:0]	6:0	Main window IHC hue adjustment of B.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_C[6:0]	6:0	Main window IHC hue adjustment of C.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_M[6:0]	6:0	Main window IHC hue adjustment of M.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_Y[6:0]	6:0	Main window IHC hue adjustment of Y.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_HUE_USER_F[6:0]	6:0	Main window IHC hue adjustment of F.	
6Eh (102FDCh)	**REG102FDC**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_R2Y_EN	4	Sub window RGB to YCbCr enable.	
	-	3:2	Reserved.	
	R2Y_DITHER_EN	1	RGB to YCbCr dither enable.	
	MAIN_R2Y_EN	0	Main window RGB to YCbCr enable.	
6Eh (102FDDh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
6Fh (102FDEh)	**REG102FDE**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_R2Y_EQ_SEL[1:0]	5:4	Sub window RGB to YCbCr equation selection.	

ACE Register (Bank = 102F, Sub-bank = 18)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
	-	3:2	Reserved.
	MAIN_R2Y_EQ_SEL[1:0]	1:0	Main window RGB to YCbCr equation selection.

PEAKING Register (Bank = 102F, Sub-bank = 19)

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_Y_LPF_COEF[2:0]	6:4	Main window horizontal Y low pass filter coefficient.	
	SUB_IS_MWE_EN	3	Sub window is MWE.	
	-	2:1	Reserved.	
	MAIN_POST_PEAKING_EN	0	Main window 2D peaking enable.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_BAND4_PEAKING_EN	3	Main window band4 peaking enable.	
	MAIN_BAND3_PEAKING_EN	2	Main window band3 peaking enable.	
	MAIN_BAND2_PEAKING_EN	1	Main window band2 peaking enable.	
	MAIN_BAND1_PEAKING_EN	0	Main window band1 peaking enable.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BAND4_COEF_STEP[1:0]	7:6	Main window band4 coefficient step.	
	MAIN_BAND3_COEF_STEP[1:0]	5:4	Main window band3 coefficient step.	
	MAIN_BAND2_COEF_STEP[1:0]	3:2	Main window band2 coefficient step.	
	MAIN_BAND1_COEF_STEP[1:0]	1:0	Main window band1 coefficient step.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CORING_THRD_2[3:0]	7:4	Main window coring threshold 2.	
	MAIN_CORING_THRD_1[3:0]	3:0	Main window coring threshold 1.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_OSD_SHARPNESS_CTRL[5:0]	5:0	Main window user sharpness adjust.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_Y_LPF_COEF[2:0]	6:4	Sub window horizontal Y LPF coefficient.	
	-	3:1	Reserved.	
	SUB_POST_PEAKING_EN	0	Sub window 2D peaking enable.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SUB_BAND4_PEAKING_EN	3	Sub window band4 peaking enable.	
	SUB_BAND3_PEAKING_EN	2	Sub window band3 peaking enable.	
	SUB_BAND2_PEAKING_EN	1	Sub window band2 peaking enable.	
	SUB_BAND1_PEAKING_EN	0	Sub window band1 peaking enable.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_CORING_THRD_2[3:0]	7:4	Sub window coring threshold 2.	
	SUB_CORING_THRD_1[3:0]	3:0	Sub window coring threshold 1.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_OSD_SHARPNESS_CTRL[5:0]	5:0	Sub window user sharpness adjust.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND1_COEF[5:0]	5:0	Main window band1 coefficient.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND2_COEF[5:0]	5:0	Main window band2 coefficient.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND3_COEF[5:0]	5:0	Main window band3 coefficient.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_BAND4_COEF[5:0]	5:0	Main window band4 coefficient.	
20h	**REG102F40**	**7:0**	**Default: 0xFF**	**Access: R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F40h)	BAND1_OVERSHOOT_LIMIT[7:0]	7:0	Main window band1 overshoot limit.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND2_OVERSHOOT_LIMIT[7:0]	7:0	Main window band2 overshoot limit.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND3_OVERSHOOT_LIMIT[7:0]	7:0	Main window band3 overshoot limit.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND4_OVERSHOOT_LIMIT[7:0]	7:0	Main window band4 overshoot limit.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND1_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band1 undershoot limit.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND2_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band2 undershoot limit.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND3_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band3 undershoot limit.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BAND4_UNDERSHOOT_LIMIT[7:0]	7:0	Main window band4 undershoot limit.	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND1_COEF[5:0]	5:0	Sub window band1 coefficient.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND2_COEF[5:0]	5:0	Sub window band2 coefficient.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_BAND3_COEF[5:0]	5:0	Sub window band3 coefficient.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_BAND4_COEF[5:0]	5:0	Sub window band4 coefficient.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_COLOR_PEAKING_EN	7	Main window color adaptive peaking enable.	
	MAIN_COLOR_FACTOR_LPF_EN	6	Main window color factor LPF enable.	
	-	5:0	Reserved.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x33**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_CORING_THRD_STEP[1:0]	5:4	Main window coring step.	
	-	3:2	Reserved.	
	SUB_CORING_THRD_STEP[1:0]	1:0	Sub window coring step.	
31h ~ 37h (102F62h ~ 102F6Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
3Bh (102F76h)	**REG102F76**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_CR_DELAY_NUM	6	Sub window Cr delay number. 0: No delay. 1: Delay 1T.	
	-	5	Reserved.	
	MAIN_CR_DELAY_NUM	4	Main window Cr delay number. 0: No delay. 1: Delay 1T.	
	-	3:2	Reserved.	
	SUB_YC_DELAY_EN	1	Sub window yc delay enable.	
	MAIN_YC_DELAY_EN	0	Main window yc delay enable.	
3Bh (102F77h)	**REG102F77**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_CB_DELAY_NUM	6	Sub window Cb delay number. 0: No delay. 1: Delay 1T.	
	-	5	Reserved.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SUB_Y_DELAY_NUM	4	Sub window Y delay number. 0: No delay. 1: Delay 1T.	
	-	3	Reserved.	
	MAIN_CB_DELAY_NUM	2	Main window Cb delay number. 0: No delay. 1: Delay 1T.	
	-	1	Reserved.	
	MAIN_Y_DELAY_NUM	0	Main window Y delay number. 0: No delay. 1: Delay 1T.	
40h ~ 47h (102F80h ~ 102F8Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_COLOR_PK_WIN4_EN	7	Sub window color adaptive win4 enable.	
	SUB_COLOR_PK_WIN3_EN	6	Sub window color adaptive win3 enable.	
	SUB_COLOR_PK_WIN2_EN	5	Sub window color adaptive win2 enable.	
	SUB_COLOR_PK_WIN1_EN	4	Sub window color adaptive win1 enable.	
	MAIN_COLOR_PK_WIN4_EN	3	Main window color adaptive win4 enable.	
	MAIN_COLOR_PK_WIN3_EN	2	Main window color adaptive win3 enable.	
	MAIN_COLOR_PK_WIN2_EN	1	Main window color adaptive win2 enable.	
	MAIN_COLOR_PK_WIN1_EN	0	Main window color adaptive win1 enable.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN4_TRANSITION_STEP[1:0]	7:6	Color adaptive win4 transition step.	
	COLOR_PK_WIN3_TRANSITION_STEP[1:0]	5:4	Color adaptive win3 transition step.	
	COLOR_PK_WIN2_TRANSITION_STEP[1:0]	3:2	Color adaptive win2 transition step.	
	COLOR_PK_WIN1_TRANSITION_STEP[1:0]	1:0	Color adaptive win1 transition step.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_ENTRY_VALUE[3:0]	7:4	Color adaptive win2 strength.	
	COLOR_PK_WIN1_ENTRY_VALUE[3:0]	3:0	Color adaptive win1 strength.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN4_ENTRY_VALUE[3:0]	7:4	Color adaptive win4 strength.	
	COLOR_PK_WIN3_ENTRY_VALUE[3:0]	3:0	Color adaptive win3 strength.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	COLOR_PK_TEST_EN[3:0]	3:0	Color adaptive test mode enable.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x30**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_PK_ADP_Y_STEP[1:0]	5:4	Main window peaking adaptive Y alpha step.	
	-	3:2	Reserved.	
	MAIN_PK_ADP_Y_ALPHA_LPF_EN	1	Main window peaking adaptive Y alpha low pass filter enable.	
	MAIN_PK_ADP_Y_EN	0	Main window peaking adaptive Y enable.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_PK_Y_LOW_THRD[7:0]	7:0	Main window peaking adaptive Y low threshold.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x54**	**Access: R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_1[3:0]	7:4	Main window peaking adaptive Y alpha LUT 1.	
	MAIN_PK_ADP_Y_ALPHA_LUT_0[3:0]	3:0	Main window peaking adaptive Y alpha LUT 0, format is x.xxx, range is 0~F.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x76**	**Access: R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_3[3:0]	7:4	Main window peaking adaptive Y alpha LUT 3.	
	MAIN_PK_ADP_Y_ALPHA_LUT_2[3:0]	3:0	Main window peaking adaptive Y alpha LUT 2.	
57h	**REG102FAE**	**7:0**	**Default: 0x88**	**Access: R/W**

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FAEh)	MAIN_PK_ADP_Y_ALPHA_LUT_5[3:0]	7:4	Main window peaking adaptive Y alpha LUT 5.	
	MAIN_PK_ADP_Y_ALPHA_LUT_4[3:0]	3:0	Main window peaking adaptive Y alpha LUT 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x88**	**Access: R/W**
	MAIN_PK_ADP_Y_ALPHA_LUT_7[3:0]	7:4	Main window peaking adaptive Y alpha LUT 7.	
	MAIN_PK_ADP_Y_ALPHA_LUT_6[3:0]	3:0	Main window peaking adaptive Y alpha LUT 6.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN1_CB_UP[7:0]	7:0	Color adaptive win1 Cb up.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN1_CR_UP[7:0]	7:0	Color adaptive win1 Cr up.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN1_CB_DOWN[7:0]	7:0	Color adaptive win1 Cb down.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN1_CR_DOWN[7:0]	7:0	Color adaptive win1 Cr down.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_CB_UP[7:0]	7:0	Color adaptive win2 Cb up.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_CR_UP[7:0]	7:0	Color adaptive win2 Cr up.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_CB_DOWN[7:0]	7:0	Color adaptive win2 Cb down.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN2_CR_DOWN[7:0]	7:0	Color adaptive win2 Cr down.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN3_CB_UP[	7:0	Color adaptive win3 Cb up.	

PEAKING Register (Bank = 102F, Sub-bank = 19)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	7:0]			
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN3_CR_UP[7:0]	7:0	Color adaptive win3 Cr up.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN3_CB_DOWN[7:0]	7:0	Color adaptive win3 Cb down.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN3_CR_DOWN[7:0]	7:0	Color adaptive win3 Cr down.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN4_CB_UP[7:0]	7:0	Color adaptive win4 Cb up.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN4_CR_UP[7:0]	7:0	Color adaptive win4 Cr up.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN4_CB_DOWN[7:0]	7:0	Color adaptive win4 Cb down.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: 0x00**	**Access: R/W**
	COLOR_PK_WIN4_CR_DOWN[7:0]	7:0	Color adaptive win4 Cr down.	
6Dh (102FDAh)	**REG102FDA**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_PK_ADP_Y_ALPHA_LPF_EN	1	Sub window peaking adaptive Y alpha low pass filter enable.	
	SUB_PK_ADP_Y_EN	0	Sub window peaking adaptive Y enable.	

DLC Register (Bank = 102F, Sub-bank = 1A)

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 08h (102F02h ~ 102F10h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	UVC_DITHER_EN	7	UV compensate dither enable.	
	-	6	Reserved.	
	SUB_UVC_LOCATE	5	Sub window UV compensate reference location. 0: After BLE/WLE. 1: After curve fit.	
	SUB_UVC_EN	4	Sub window UV compensate enable.	
	-	3:2	Reserved.	
	MAIN_UVC_LOCATE	1	Main window UV compensate reference location. 0: After BLE/WLE. 1: After curve fit0.	
	MAIN_UVC_EN	0	Main window UV compensate enable.	
09h ~ 0Ah (102F12h ~ 102F15h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: RO**
	MAIN_MAX_PIXEL[7:0]	7:0	Main window maximun pixel.	
0Bh (102F17h)	**REG102F17**	**7:0**	**Default: 0x00**	**Access: RO**
	MAIN_MIN_PIXEL[7:0]	7:0	Main window minimum pixel.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x00**	**Access: RO**
	SUB_MAX_PIXEL[7:0]	7:0	Sub window maximun pixel.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: RO**
	SUB_MIN_PIXEL[7:0]	7:0	Sub window minimum pixel.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_BRI_ADJUST_LSB[1:0]	1:0	Main window Y adjust low bit.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_BRI_ADJUST_LSB[1:0]	1:0	Sub window Y adjust low bit.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_BRI_ADJUST[7:0]	7:0	Main window Y adjust.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_BRI_ADJUST[7:0]	7:0	Sub window Y adjust.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_BLACK_START[6:0]	6:0	Main window black start.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_BLACK_SLOP[7:0]	7:0	Main window black slope.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_WHITE_START[6:0]	6:0	Main window white start.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x80**	**Access: R/W**
	MAIN_WHITE_SLOP[7:0]	7:0	Main window white slope.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_BLACK_START[6:0]	6:0	Sub window black start.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_BLACK_SLOP[7:0]	7:0	Sub window black slope.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	SUB_WHITE_START[6:0]	6:0	Sub window white start.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x80**	**Access: R/W**
	SUB_WHITE_SLOP[7:0]	7:0	Sub window white slope.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x40**	**Access: R/W**
	MAIN_Y_GAIN[7:0]	7:0	Main window Y gain.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x40**	**Access: R/W**
	MAIN_C_GAIN[7:0]	7:0	Main window C gain.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x40**	**Access: R/W**
	SUB_Y_GAIN[7:0]	7:0	Sub window Y gain.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x40**	**Access: R/W**
	SUB_C_GAIN[7:0]	7:0	Sub window C gain.	
16h	**REG102F2C**	**7:0**	**Default: 0x40**	**Access: R/W**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Ch)	MAIN_PRE_Y_GAIN[7:0]	7:0	Main window pre- Y gain.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x40**	**Access: R/W**
	SUB_PRE_Y_GAIN[7:0]	7:0	Sub window pre- Y gain.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MAIN_POST_BRI_ADJUST_LSB[1:0]	1:0	Main window post Y adjust low bit (2's complement).	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SUB_POST_BRI_ADJUST_LSB[1:0]	1:0	Sub window post Y adjust low bit (2's complement).	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_POST_BRI_ADJUST[7:0]	7:0	Main window post Y adjust.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	SUB_POST_BRI_ADJUST[7:0]	7:0	Sub window post Y adjust.	
1Ah ~ 27h (102F34h ~ 102F4Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x08**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_0[7:0]	7:0	Main window curve table 0.	
30h (102F61h)	**REG102F61**	**7:0**	**Default: 0x18**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_1[7:0]	7:0	Main window curve table 1.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x28**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_2[7:0]	7:0	Main window curve table 2.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x38**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_3[7:0]	7:0	Main window curve table 3.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x48**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_4[7:0]	7:0	Main window curve table 4.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x58**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_5[7:0]	7:0	Main window curve table 5.	
33h (102F66h)	**REG102F66**	**7:0**	**Default: 0x68**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_6[7:0]	7:0	Main window curve table 6.	
33h (102F67h)	**REG102F67**	**7:0**	**Default: 0x78**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_7[7:0]	7:0	Main window curve table 7.	
34h (102F68h)	**REG102F68**	**7:0**	**Default: 0x88**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_8[7:0]	7:0	Main window curve table 8.	
34h (102F69h)	**REG102F69**	**7:0**	**Default: 0x98**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_9[7:0]	7:0	Main window curve table 9.	
35h (102F6Ah)	**REG102F6A**	**7:0**	**Default: 0xA8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_10[7:0]	7:0	Main window curve table 10.	
35h (102F6Bh)	**REG102F6B**	**7:0**	**Default: 0x00**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_11[7:0]	7:0	Main window curve table 11.	
36h (102F6Ch)	**REG102F6C**	**7:0**	**Default: 0xC8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_12[7:0]	7:0	Main window curve table 12.	
36h (102F6Dh)	**REG102F6D**	**7:0**	**Default: 0xD8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_13[7:0]	7:0	Main window curve table 13.	
37h (102F6Eh)	**REG102F6E**	**7:0**	**Default: 0xE8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_14[7:0]	7:0	Main window curve table 14.	
37h (102F6Fh)	**REG102F6F**	**7:0**	**Default: 0xF8**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_15[7:0]	7:0	Main window curve table 15.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_0[7:0]	7:0	Histogram report section 32_0.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_0[15:8]	7:0	See description of '102F80h'.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_1[7:0]	7:0	Histogram report section 32_1.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_1[15:8]	7:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_2[7:0]	7:0	Histogram report section 32_2.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_2[15:8]	7:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_3[7:0]	7:0	Histogram report section 32_3.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_3[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_4[7:0]	7:0	Histogram report section 32_4.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_4[15:8]	7:0	See description of '102F88h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_5[7:0]	7:0	Histogram report section 32_5.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_5[15:8]	7:0	See description of '102F8Ah'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_6[7:0]	7:0	Histogram report section 32_6.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_6[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_7[7:0]	7:0	Histogram report section 32_7.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_7[15:8]	7:0	See description of '102F8Eh'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_8[7:0]	7:0	Histogram report section 32_8.	
48h	**REG102F91**	**7:0**	**Default: 0x00**	**Access: RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F91h)	TOTAL_32_8[15:8]	7:0	See description of '102F90h'.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_9[7:0]	7:0	Histogram report section 32_9.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_9[15:8]	7:0	See description of '102F92h'.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_10[7:0]	7:0	Histogram report section 32_10.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_10[15:8]	7:0	See description of '102F94h'.	
4Bh (102F96h)	**REG102F96**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_11[7:0]	7:0	Histogram report section 32_11.	
4Bh (102F97h)	**REG102F97**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_11[15:8]	7:0	See description of '102F96h'.	
4Ch (102F98h)	**REG102F98**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_12[7:0]	7:0	Histogram report section 32_12.	
4Ch (102F99h)	**REG102F99**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_12[15:8]	7:0	See description of '102F98h'.	
4Dh (102F9Ah)	**REG102F9A**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_13[7:0]	7:0	Histogram report section 32_13.	
4Dh (102F9Bh)	**REG102F9B**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_13[15:8]	7:0	See description of '102F9Ah'.	
4Eh (102F9Ch)	**REG102F9C**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_14[7:0]	7:0	Histogram report section 32_14.	
4Eh (102F9Dh)	**REG102F9D**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_14[15:8]	7:0	See description of '102F9Ch'.	
4Fh (102F9Eh)	**REG102F9E**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_15[7:0]	7:0	Histogram report section 32_15.	
4Fh (102F9Fh)	**REG102F9F**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_15[15:8]	7:0	See description of '102F9Eh'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_16[7:0]	7:0	Histogram report section 32_16.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_16[15:8]	7:0	See description of '102FA0h'.	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_17[7:0]	7:0	Histogram report section 32_17.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_17[15:8]	7:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_18[7:0]	7:0	Histogram report section 32_18.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_18[15:8]	7:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_19[7:0]	7:0	Histogram report section 32_19.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_19[15:8]	7:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_20[7:0]	7:0	Histogram report section 32_20.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_20[15:8]	7:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_21[7:0]	7:0	Histogram report section 32_21.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_21[15:8]	7:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_22[7:0]	7:0	Histogram report section 32_22.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_22[15:8]	7:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_23[7:0]	7:0	Histogram report section 32_23.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_23[15:8]	7:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_24[7:0]	7:0	Histogram report section 32_24.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_24[15:8]	7:0	See description of '102FB0h'.	
59h	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: RO**

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FB2h)	TOTAL_32_25[7:0]	7:0	Histogram report section 32_25.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_25[15:8]	7:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_26[7:0]	7:0	Histogram report section 32_26.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_26[15:8]	7:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_27[7:0]	7:0	Histogram report section 32_27.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_27[15:8]	7:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_28[7:0]	7:0	Histogram report section 32_28.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_28[15:8]	7:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_29[7:0]	7:0	Histogram report section 32_29.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_29[15:8]	7:0	See description of '102FBAh'.	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_30[7:0]	7:0	Histogram report section 32_30.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_30[15:8]	7:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_31[7:0]	7:0	Histogram report section 32_31.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: 0x00**	**Access: RO**
	TOTAL_32_31[15:8]	7:0	See description of '102FBEh'.	
63h ~ 63h (102FC6h ~ 102FC7h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x60**	**Access: R/W**
	MAIN_UVC_GAIN_HIGH_LIMIT[7:0]	7:0	Main window UV compensate gain up limit (format is 4.8).	

DLC Register (Bank = 102F, Sub-bank = 1A)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_HIGH_LIMIT[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0xC0**	**Access: R/W**
	MAIN_UVC_GAIN_LOW_LIMIT[7:0]	7:0	Main window UV compensate gain down limit (format is 4.8).	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_UVC_GAIN_LOW_LIMIT[11:8]	3:0	See description of '102FCAh'.	
6Fh (102FDEh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
76h (102FECh)	**REG102FEC**	**7:0**	**Default: 0x08**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_N0[7:0]	7:0	Main window curve table left point.	
76h (102FEDh)	**REG102FED**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_N0[8]	0	See description of '102FECh'.	
77h (102FEEh)	**REG102FEE**	**7:0**	**Default: 0x08**	**Access: R/W**
	MAIN_CURVE_FIT_TABLE_16[7:0]	7:0	Main window curve table 16.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:1	Reserved.	
	MAIN_CURVE_FIT_TABLE_16[8]	0	See description of '102FEEh'.	

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_IDX_DEPTH[7:0]	7:0	The number of menuload data. 0: Disable menuload.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_IDX_DEPTH[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_REQ_LEN[7:0]	7:0	Length of menuload DMA's request. 0: Disable menuload.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_EN	7	Menuload enable.	
	-	6:3	Reserved.	
	MLOAD_REQ_LEN[10:8]	2:0	See description of '102F04h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_BASE_ADR[7:0]	7:0	Base address of allocated memory for menuload.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_BASE_ADR[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLOAD_BASE_ADR[23:16]	7:0	See description of '102F06h'.	
04h (102F09h)	**REG102F09**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	MLOAD_BASE_ADR[24]	0	See description of '102F06h'.	
08h ~ 0Bh (102F10h ~ 102F17h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x01**	**Access: R/W**
	MLOAD_TRIG_DLY[7:0]	7:0	Generate MLAOD_TRIG_P from delayed line of Vsync.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0xC0**	**Access: R/W**
	SEL_MLOAD[1:0]	7:6	Select the source to trigger menuload. 0: Falling edge of VFDE. 1: Rising edge of Vsync. 2: Falling edge of Vsync. 3: Delay line set by REG_MLOAD_TRIG_DLY.	
	-	5:4	Reserved.	

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	MLOAD_TRIG_DLY[11:8]	3:0	See description of '102F18h'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_REQ_LEN[3:0]	7:4	Length of dynamic scaling DMA's request. 0: Disable dynamic scaling.	
	DS_REQ_TH[3:0]	3:0	Threshold for one dynamic scaling DMA request.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_IPM2MI_SEL	7	Main IP dynamic scaling MIU selection.	
	DS_IPS2MI_SEL	6	Sub IP dynamic scaling MIU selection.	
	DS_OP2MI_SEL	5	OP dynamic scaling MIU selection.	
	DS_RIU_WE	4	Enable write register through RIU.	
	IPM_DS_EN	3	Enable main IP2 dynamic scaling.	
	IPS_DS_EN	2	Enable sub IP2 dynamic scaling.	
	OP_DS_EN	1	Enable OP dynamic scaling.	
	DS_REQ_PRI	0	User specified priority of MIU.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_BASE_ADR[7:0]	7:0	Base address of allocated memory for dynamic scaling.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_BASE_ADR[15:8]	7:0	See description of '102F22h'.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_BASE_ADR[23:16]	7:0	See description of '102F22h'.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	DS_BASE_ADR[24]	0	See description of '102F22h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	DS_IDX_DEPTH[7:0]	7:0	The number of dynamic scaling data per index. 0: Disable dynamic scaling.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SC_INDEX_F2_SEL	1	F2 dynamic scaling index select. 0: From main. 1: From sub.	
	SC_INDEX_F1_SEL	0	F1 dynamic scaling index select. 0: From main. 1: From sub.	

DYN_SCL Register (Bank = 102F, Sub-bank = 1F)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
14h ~ 16h (102F28h ~ 102F2Dh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	DS_RIU_BE[1:0]	1:0	Byte enable for DS RIU interface.	
18h ~ 1Bh (102F30h ~ 102F37h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x01**	**Access: R/W**
	DS_TRIG_DLY[7:0]	7:0	Generate DS_TRIG_P from delayed line of Vsync.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x40**	**Access: R/W**
	-	7	Reserved.	
	SEL_DS	6	Select the source to trigger dynamic scaling. 0: Falling edge of Vsync. 1: Delay line set by REG_DS_TRIG_DLY.	
	-	5:4	Reserved.	
	DS_TRIG_DLY[11:8]	3:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	SEL_OPM_LOCK[1:0]	1:0	Select init reference signal to lock the memory read bank. 0: From initial state machine. 1: Falling edge of Vsync. 2: From TRAIN_TRIG_P. 3: From DS_LOAD_P (for dynamic scaling enabled).	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x01**	**Access: R/W**
	PIP_DISABLE	7	Disable PIP Function.	
	-	6:3	Reserved.	
	MWE_EN	2	Enable MWE function.	
	SW_SUB_EN	1	Enable sub window shown on the screen.	
	MAIN_EN	0	Enable main window shown on the screen.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x20**	**Access: R/W**
	-	7	Reserved.	
	FBL_HANDSHAKE_EN	6	Enable the handshake with DNR in FBL mode.	
	FBL_MASK_OVERLAP	5	Do not write overlapped portion of FBL channel to line buffer.	
	FBL_SEL	4	Select FBL source. b0: Source F2 is FBL. b1: Source F1 is FBL.	
	VBLANK_SUB	3	Fill the sub windows line buffer in vertical blanking.	
	VBLANK_MAIN	2	Fill the main window's line buffer in vertical blanking.	
	F2_IS_SUB	1	Set main window display on the foreground.	
	MAIN_IS_TOP	0	Set second channel display in sub-window.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x70**	**Access: R/W**
	-	7	Reserved.	
	EXTRA_POS[2:0]	6:4	Enable extra request at specified region. [0] Enable at bottom B session. [1] Enable at bottom A session. [2] Enable at top session.	
	EXTRA_TH_LN[3:0]	3:0	Enable extra request for overlapping when the jumping line less than this threshold.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x07**	**Access: R/W**
	EXTRA_EN	7	Enable extra request engine.	
	VBLANK_OVL	6	Doing the extra request in vertical blanking.	
	EXTRA_Y_HALF	5	Reduce the EXTRA_Y to half.	
	-	4:3	Reserved.	
	BO_LENGTH[2:0]	2:0	Select the length of extra request. h0: 16 pixels. h1: 32 pixels.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			h2: 64 pixels. h3: 128 pixels. h4: (overlap length) / 8. h5: (overlap length) / 4. h6: (overlap length) / 2. h7: (overlap length).	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCLB_BASE_F2[7:0]	7:0	The starting address of f2 stored at line buffer.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F2[11:8]	3:0	See description of '102F24h'.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCLB_BASE_F1[7:0]	7:0	The starting address of f1 stored at line buffer.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:4	Reserved.	
	SCLB_BASE_F1[11:8]	3:0	See description of '102F26h'.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x08**	**Access: R/W**
	HEXT_BA_RIGHT[7:0]	7:0	Extend the pixel of bottom A session at the right side.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x08**	**Access: R/W**
	HEXT_BB_LEFT[7:0]	7:0	Extend the pixel of bottom B session at the left side.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	VLEN_F2[7:0]	7:0	Set the maximum request lines for second channel.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	VLEN_F2[11:8]	3:0	See description of '102F2Ah'.	
16h (102F2Ch)	**REG102F2C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	VLEN_F1[7:0]	7:0	Set the maximum request lines for first channel.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	VLEN_F1[11:8]	3:0	See description of '102F2Ch'.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	EXT_SUB_BORDER[3:0]	7:4	Extend the specified line in sub window to insert additional border.	
	EXT_MAIN_BORDER[3:0]	3:0	Extend the specified line in main window to insert additional	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			border.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x02**	**Access: R/W**
	EXTRA_ADV_LINE[3:0]	7:4	Advance the specified lines of extra end line (2's complement).	
	EXTRA_FETCH_LINE[3:0]	3:0	The number of lines that will be fetched by extra request. Minimum is 1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	FORCE_F2_EN	1	Force F1 use F2's register setting.	
	ATP_EN	0	Manual tune parameter.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x38**	**Access: R/W**
	-	7	Reserved.	
	SEL_DLY_INIT	6	Select init reference signal to clear delayed line counter. 0: Vsync of SC_TOP. 1: Delay one line of VFDE.	
	SEL_DISP[1:0]	5:4	Select the trig point to start op1 engine. h0: DOWN_EQ7. h1: DOWN_EQ8. h2: DOWN_EQ9. h3: Delay lines set by REG_DISP_TRIG_DLY.	
	SEL_ATP[1:0]	3:2	Select the source to trigger auto tune function. h0: Falling edge of Vsync. h1: Nearly raising edge of Vsync. h2: Delay line set by REG_ATP_TRIG_DLY. h3: Manual trig by set REG_ATP_EN.	
	SEL_SYNC[1:0]	1:0	Select the trig point for sync to initial engine. h0: Falling edge of VFDE. h1: Raising edge of Vsync. h2: Reserved. h3: Reserved.	
19h (102F33h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x03**	**Access: R/W**
	ATP_TRIG_DLY[7:0]	7:0	Generate TRAIN_TRIG_P from delayed line of Vsync.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	ATP_TRIG_DLY[11:8]	3:0	See description of '102F34h'.	
1Bh (102F36h)	**REG102F36**	**7:0**	**Default: 0x05**	**Access: R/W**
	DISP_TRIG_DLY[7:0]	7:0	Generate DISP_TRIG_P from delayed line of Vsync.	
1Bh (102F37h)	**REG102F37**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DISP_TRIG_DLY[11:8]	3:0	See description of '102F36h'.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	HOFFSET_MAIN[7:0]	7:0	Offset main display window in right direction.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	HOFFSET_SUB[7:0]	7:0	Offset sub display window in right direction.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x00**	**Access: R/W**
	HOVERSCAN_F2[7:0]	7:0	Offset line buffer position of F2 in right direction.	
1Dh (102F3Bh)	**REG102F3B**	**7:0**	**Default: 0x00**	**Access: R/W**
	HOVERSCAN_F1[7:0]	7:0	Offset line buffer position of F1 in right direction.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x10**	**Access: R/W**
	MIN_OVERLAP_TH[7:0]	7:0	Threshold of overlapped length. EXTRA_EQ will be disabled when overlapped length less then this threshold.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	MIN_OVERLAP_CNT[7:0]	7:0	Stop count between two extra request.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0xC2**	**Access: R/W**
	SCLB_HALIGN[1:0]	7:6	Align the train result to specified pixel. h0: 2 pixels. h1: 4 pixels. h2: 8 pixels. h3: 16 pixels.	
	DISP_START_MODE	5	Select the display line buffer start mode. 0: Start at advance 1 display line. 1: Start at falling edge of VSYNC_INIT.	
	DISP_LB_MODE	4	Select the trig mode. 0: Line base. 1: Fill line buffer.	
	DISP_WSTOP_MODE[1:0]	3:2	Stop the write of display before full to avoid overflow. h0: Before 8 pixels. h1: Before 16 pixels.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			h2: Before 32 pixels. h3: Before 64 pixels	
	DISP_RLN_MODE[1:0]	1:0	Select the UNDER_RUN value of display level. h0: Update by Hsync (not optimum performance). h1: Update when session done (may error). h2: Update when line done (REG_DISP_TRIG_MODE = 0). h3: Reserved.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	DISP_UNDER_MODE	3	Select the UNDER_RUN value of display level. 0: 16'h0000. 1: 16'hffff.	
	DISP_PAT_EN	2	Enable internal pattern of OP1_DISP.	
	DISP_LB_WEZ	1	Disable WEN of display line buffer.	
	DISP_TRIG_MODE	0	Select the trig mode. 0: Trigged by SELF_COUNTER. 1: Trigged by op2.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0xFF**	**Access: R/W**
	DISP_LB_FULL_LVL[7:0]	7:0	Set the maximum depth of display line buffer.	
20h (102F41h)	**REG102F41**	**7:0**	**Default: 0x07**	**Access: R/W**
	DISP_LB_FULL_LVL[15:8]	7:0	See description of '102F40h'.	
30h (102F60h)	**REG102F60**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	FLAG_BB_ADR_INI	2	Status of CNT_BB_ADR_INI, write 1 to switch back to hardware. h0: Calculated by hardware. h1: Written by software.	
	FLAG_BO_END_LN	1	Status of LINE_BASE_BOT, write 1 to switch back to hardware. h0: Calculated by hardware. h1: Written by software.	
	-	0	Reserved.	
31h (102F62h)	**REG102F62**	**7:0**	**Default: 0x00**	**Access: R/W**
	SW_BO_END_LN[7:0]	7:0	Software mode to set the LINE_BASE_BOT for extra request.	
31h (102F63h)	**REG102F63**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SW_BO_END_LN[11:8]	3:0	See description of '102F62h'.	
32h (102F64h)	**REG102F64**	**7:0**	**Default: 0x00**	**Access: R/W**
	SW_BB_ADR_INI[7:0]	7:0	Software mode to set the CNT_BB_ADR_INI.	
32h (102F65h)	**REG102F65**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SW_BB_ADR_INI[11:8]	3:0	See description of '102F64h'.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:1	Reserved.	
	DISPLAY_UNDERRUN	0	Indicate that the display line buffer is underrun in previous frame.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: RO**
	DISPLAY_FIRST_LN[7:0]	7:0	Indicate the display line count of first display position.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	DISPLAY_FIRST_LN[11:8]	3:0	See description of '102F82h'.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: RO**
	MIN_DISP_LINE[7:0]	7:0	Indicate the display line count of minimum display level occurs.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	MIN_DISP_LINE[11:8]	3:0	See description of '102F84h'.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: RO**
	MIN_DISP_CNT[7:0]	7:0	Indicate the minimum display level.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: RO**
	MIN_DISP_CNT[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: RO**
	MAX_DISP_CNT[7:0]	7:0	Indicate the maximum display level.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x00**	**Access: RO**
	MAX_DISP_CNT[15:8]	7:0	See description of '102F88h'.	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x00**	**Access: RO**
	SCLB_TF_ADR_INI[7:0]	7:0	Read SCLB_TF_ADR_INI.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SCLB_TF_ADR_INI[11:8]	3:0	See description of '102FA0h'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x00**	**Access: RO**
	SCLB_BA_ADR_INI[7:0]	7:0	Read SCLB_BA_ADR_INI.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_BA_ADR_INI[11:8]	3:0	See description of '102FA2h'.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: RO**
	SCLB_BB_ADR_INI[7:0]	7:0	Read SCLB_BB_ADR_INI.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_BB_ADR_INI[11:8]	3:0	See description of '102FA4h'.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: RO**
	SCLB_BO_ADR_INI[7:0]	7:0	Read SCLB_BO_ADR_INI.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_BO_ADR_INI[11:8]	3:0	See description of '102FA6h'.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: RO**
	SCLB_TF_LEN[7:0]	7:0	Read SCLB_TF_LEN.	
54h (102FA9h)	**REG102FA9**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_TF_LEN[11:8]	3:0	See description of '102FA8h'.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x00**	**Access: RO**
	SCLB_BF_LEN[7:0]	7:0	Read SCLB_BF_LEN.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_BF_LEN[11:8]	3:0	See description of '102FAAh'.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x00**	**Access: RO**
	SCLB_BA_LEN[7:0]	7:0	Read SCLB_BA_LEN.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_BA_LEN[11:8]	3:0	See description of '102FACh'.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x00**	**Access: RO**
	SCLB_BB_LEN[7:0]	7:0	Read SCLB_BB_LEN.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	SCLB_BB_LEN[11:8]	3:0	See description of '102FAEh'.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0x00**	**Access: RO**
	FETCH_NUM_F1A[7:0]	7:0	Read FETCH_NUM_F1A.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1A[11:8]	3:0	See description of '102FB0h'.	
59h (102FB2h)	**REG102FB2**	**7:0**	**Default: 0x00**	**Access: RO**
	FETCH_NUM_F1B[7:0]	7:0	Read FETCH_NUM_F1B.	
59h (102FB3h)	**REG102FB3**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	FETCH_NUM_F1B[11:8]	3:0	See description of '102FB2h'.	
5Ah (102FB4h)	**REG102FB4**	**7:0**	**Default: 0x00**	**Access: RO**
	FETCH_NUM_F2A[7:0]	7:0	Read FETCH_NUM_F2A.	
5Ah (102FB5h)	**REG102FB5**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2A[11:8]	3:0	See description of '102FB4h'.	
5Bh (102FB6h)	**REG102FB6**	**7:0**	**Default: 0x00**	**Access: RO**
	FETCH_NUM_F2B[7:0]	7:0	Read FETCH_NUM_F2B.	
5Bh (102FB7h)	**REG102FB7**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	FETCH_NUM_F2B[11:8]	3:0	See description of '102FB6h'.	
5Ch (102FB8h)	**REG102FB8**	**7:0**	**Default: 0x00**	**Access: RO**
	FETCH_OFFSET_B[7:0]	7:0	Read FETCH_OFFSET_B.	
5Ch (102FB9h)	**REG102FB9**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	FETCH_OFFSET_B[11:8]	3:0	See description of '102FB8h'.	
5Dh (102FBAh)	**REG102FBA**	**7:0**	**Default: 0x00**	**Access: RO**
	BO_LENGTH_RD[7:0]	7:0	Read BO_LENGTH.	
5Dh (102FBBh)	**REG102FBB**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	BO_LENGTH_RD[11:8]	3:0	See description of '102FBAh'.	

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Eh (102FBCh)	**REG102FBC**	**7:0**	**Default: 0x00**	**Access: RO**
	BO_START_LN[7:0]	7:0	Read BO_START_LN.	
5Eh (102FBDh)	**REG102FBD**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	BO_START_LN[11:8]	3:0	See description of '102FBCh'.	
5Fh (102FBEh)	**REG102FBE**	**7:0**	**Default: 0x00**	**Access: RO**
	BO_END_LN[7:0]	7:0	Read BO_END_LN.	
5Fh (102FBFh)	**REG102FBF**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	BO_END_LN[11:8]	3:0	See description of '102FBEh'.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x00**	**Access: RO**
	DISP_TF_ADR_INI[7:0]	7:0	Read DISP_TF_ADR_INI.	
60h (102FC1h)	**REG102FC1**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	DISP_TF_ADR_INI[11:8]	3:0	See description of '102FC0h'.	
61h (102FC2h)	**REG102FC2**	**7:0**	**Default: 0x00**	**Access: RO**
	DISP_BA_ADR_INI[7:0]	7:0	Read DISP_BA_ADR_INI.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	DISP_BA_ADR_INI[11:8]	3:0	See description of '102FC2h'.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: RO**
	DISP_BB_ADR_INI[7:0]	7:0	Read DISP_BB_ADR_INI.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	DISP_BB_ADR_INI[11:8]	3:0	See description of '102FC4h'.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x00**	**Access: RO**
	DISP_TF_LEN[7:0]	7:0	Read DISP_TF_LEN.	
63h (102FC7h)	**REG102FC7**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	DISP_TF_LEN[11:8]	3:0	See description of '102FC6h'.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x00**	**Access: RO**
	DISP_BF_LEN[7:0]	7:0	Read DISP_BF_LEN.	
64h	**REG102FC9**	**7:0**	**Default: 0x00**	**Access: RO**

OP1_TOP Register (Bank = 102F, Sub-bank = 20)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102FC9h)	-	7:4	Reserved.	
	DISP_BF_LEN[11:8]	3:0	See description of '102FC8h'.	
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0x00**	**Access: RO**
	DISP_BA_LEN[7:0]	7:0	Read DISP_BA_LEN.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	DISP_BA_LEN[11:8]	3:0	See description of '102FCAh'.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default: 0x00**	**Access: RO**
	DISP_BB_LEN[7:0]	7:0	Read DISP_BB_LEN.	
66h (102FCDh)	**REG102FCD**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	DISP_BB_LEN[11:8]	3:0	See description of '102FCCh'.	
67h (102FCEh)	**REG102FCE**	**7:0**	**Default: 0x00**	**Access: RO**
	HSPR_BB_ADR_INI[7:0]	7:0	Read HSPR_BB_ADR_INI.	
67h (102FCFh)	**REG102FCF**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	HSPR_BB_ADR_INI[11:8]	3:0	See description of '102FCEh'.	

ELA Register (Bank = 102F, Sub-bank = 21)

ELA Register (Bank = 102F, Sub-bank = 21)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 0Fh (102F02h ~ 102F1Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:1	Reserved.	
	EODI_EN_F2	0	F2 window EODi enable. 1: Enable. 0: Disable.	
11h ~ 31h (102F22h ~ 102F63h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

TDDI Register (Bank = 102F, Sub-bank = 22)

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x04**	**Access: R/W**
	RATIO_DIV_YCSEP_F2	7	Main window ratio divide Y/C separate.	
	-	6:3	Reserved.	
	RATIO_DIV_MD_C_F2[2:0]	2:0	Main window ratio divide mode when Y/C separate.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:6	Reserved.	
	RATIO_DIV_MD_F2[2:0]	5:3	Main window ratio divide mode.	
	RATIO_MD_F2[2:0]	2:0	Main window ratio filter mode.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x80**	**Access: R/W**
	RATIO_C_INDEP_F2	7	Main window C ratio independent mode. 0: Disable C ratio filter. 1: Enable C ratio filter.	
	RATIO_C_LOWBOUND_F2	6	Main window C ratio lower bound enable.	
	RSV_02_2_F2[1:0]	5:4	Reserved.	
	RATIO_C_MIN_F2[3:0]	3:0	Main window C minimum ratio in independent mode.	
02h (102F05h)	**REG102F05**	**7:0**	**Default: 0x00**	**Access: R/W**
	RSV_02_0_F2[2:0]	7:5	Reserved.	
	-	4	Reserved.	
	RSV_02_1_F2[1:0]	3:2	Reserved.	
	-	1	Reserved.	
	RATIO_C_YMAX_DIS_F2	0	Main window C ratio takes Y ratio mode disable. 0: Enable. 1: Disable.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	PRE_MOT_OFFSET_F2[5:0]	5:0	Main Window pre-memory motion offset for motion calculation.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:4	Reserved.	
	PRE_MOT_GAIN_F2[3:0]	3:0	Main Window pre-memory motion gain for motion calculation.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	POST_MOT_OFFSET_F2[5:0]	5:0	Main Window post-memory motion offset for motion calculation.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x88**	**Access: R/W**
	POST_MOT_CGAIN_F2[3:0]	7:4	Main Window post-memory motion gain for Y motion calculation.	
	POST_MOT_YGAIN_F2[3:0]	3:0	Main Window post-memory motion gain for C motion calculation.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x86**	**Access: R/W**
	POST_MOT_YMAX_EN_F2	7	Main Window pre-/post-memory Y motion maximum enable.	
	-	6:3	Reserved.	
	HIS_WT_F2[2:0]	2:0	Main Window history weighting.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:4	Reserved.	
	HIS_RATIO_OFFSET_F2[3:0]	3:0	Main Window history ratio offset.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0x07**	**Access: R/W**
	RSV_STAT_0_F2[1:0]	7:6	Reserved.	
	STAT_INC_MODE_F2	5	Main window ratio statistics: Ratio incremental mode.	
	STAT_SEL_C_F2	4	Main window ratio statistics: Ratio selection.	
	STAT_CORE_F2[3:0]	3:0	Main window ratio statistics: Coring threshold.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: RO**
	MOTION_STATUS_F2[7:0]	7:0	Main window ratio statistics: Motion status.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: RO**
	MOTION_STATUS_F2[15:8]	7:0	See description of '102F1Ah'.	
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: RO**
	MOTION_STATUS_F2[23:16]	7:0	See description of '102F1Ah'.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x4A**	**Access: R/W**
	ADAPT_MED_EN_F2	7	Main window adaptive DFK enable.	
	WEGT_MED_EN_F2	6	Main window weighted DFK enable.	
	-	5	Reserved.	
	MED_MANUAL_EN_F2	4	Main window DFK manual mode enable.	
	MED_MANUAL_WEIGHT_F	3:0	Main window DFK manual weighting.	

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	2[3:0]			
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:5	Reserved.	
	MED_LF_BEGIN_F2[4:0]	4:0	Main window weighted DFK low-frequency begin.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:4	Reserved.	
	MED_LF_SLOPE_F2[3:0]	3:0	Main window weighted DFK low-frequency slope adjustment.	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:5	Reserved.	
	MED_HF_BEGIN_F2[4:0]	4:0	Main window weighted DFK high-frequency begin.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x04**	**Access: R/W**
	-	7:4	Reserved.	
	MED_HF_SLOPE_F2[3:0]	3:0	Main window weighted DFK high-frequency slope adjustment.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x30**	**Access: R/W**
	-	7:6	Reserved.	
	MED_MOT_TH_F2[5:0]	5:0	Main window adaptive DFK motion threshold.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	SST_EN_F2	7	Main window SST enable.	
	-	6:0	Reserved.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0xC0**	**Access: R/W**
	SST_POSTLPF_EN_F2	7	Main window SST post-LPF enable.	
	SST_POSTLPF_MAX_F2	6	Main window SST post-LPF maximum function enable.	
	-	5:0	Reserved.	
1Ah (102F34h)	**REG102F34**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SST_STATIC_CORE_TH_F2[5:0]	5:0	Main window SST static motion coring threshold.	
1Ah (102F35h)	**REG102F35**	**7:0**	**Default: 0x22**	**Access: R/W**
	SST_STATIC_SGAIN_F2[3:0]	7:4	Main window SST static motion spatial difference gain.	
	SST_STATIC_TGAIN_F2[3:0]	3:0	Main window SST static motion temporal difference gain.	
20h ~ 25h	**-**	**7:0**	**Default: -**	**Access: -**

TDDI Register (Bank = 102F, Sub-bank = 22)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F40h ~ 102F4Bh)	-	-	Reserved.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	ADAPT_MED_EN_F1	7	Sub window adaptive DFK enable.	
	-	6:0	Reserved.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	SST_EN_F1	7	Sub window SST enable.	
	-	6:0	Reserved.	
50h ~ 72h (102FA0h ~ 102FE4h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
73h (102FE6h)	**REG102FE6**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:2	Reserved.	
	FBASE_LVL_STATUS[1:0]	1:0	Frame-based level status.	
78h ~ 7Fh (102FF0h ~ 102FFFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

HVSP Register (Bank = 102F, Sub-bank = 23)

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR_HO_F2[7:0]	7:0	Main window horizontal initial factor.	
01h (102F03h)	**REG102F03**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR_HO_F2[15:8]	7:0	See description of '102F02h'.	
02h (102F04h)	**REG102F04**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	INI_FACTOR_HO_F2[19:16]	3:0	See description of '102F02h'.	
03h (102F06h)	**REG102F06**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR1_VE_F2[7:0]	7:0	Main window vertical initial factor 1.	
03h (102F07h)	**REG102F07**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR1_VE_F2[15:8]	7:0	See description of '102F06h'.	
04h (102F08h)	**REG102F08**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR1_VE_F2[23:16]	7:0	See description of '102F06h'.	
05h (102F0Ah)	**REG102F0A**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR2_VE_F2[7:0]	7:0	Main window vertical initial factor 2.	
05h (102F0Bh)	**REG102F0B**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR2_VE_F2[15:8]	7:0	See description of '102F0Ah'.	
06h (102F0Ch)	**REG102F0C**	**7:0**	**Default: 0x00**	**Access: R/W**
	INI_FACTOR2_VE_F2[23:16]	7:0	See description of '102F0Ah'.	
07h (102F0Eh)	**REG102F0E**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_HO_F2[7:0]	7:0	Main window horizontal scaling factor.	
07h (102F0Fh)	**REG102F0F**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_HO_F2[15:8]	7:0	See description of '102F0Eh'.	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_HO_F2[23:16]	7:0	See description of '102F0Eh'.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F2	0	Main window horizontal scaling enable.	
09h (102F12h)	**REG102F12**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_VE_F2[7:0]	7:0	Main window vertical scaling factor.	
09h (102F13h)	**REG102F13**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_VE_F2[15:8]	7:0	See description of '102F12h'.	
0Ah (102F14h)	**REG102F14**	**7:0**	**Default: 0x00**	**Access: R/W**
	SCALE_FACTOR_VE_F2[23:16]	7:0	See description of '102F12h'.	
0Ah (102F15h)	**REG102F15**	**7:0**	**Default: 0x80**	**Access: R/W**
	VFAC_DEC1_MD_F2	7	Main window vertical factor dec1 mode.	
	-	6:1	Reserved.	
	SCALE_VE_EN_F2	0	Main window vertical scaling enable.	
0Bh (102F16h)	**REG102F16**	**7:0**	**Default: 0x00**	**Access: R/W**
	Y_RAM_SEL_HO_F2	7	Main window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F2	6	Main window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F2	5	Main window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F2	4	Main window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F2[2:0]	3:1	Main window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F2	0	Main window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Bh	**REG102F17**	**7:0**	**Default: 0x00**	**Access: R/W**

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F17h)	Y_RAM_SEL_VE_F2	7	Main window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F2	6	Main window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F2	5	Main window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F2	4	Main window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F2[2:0]	3:1	Main window vertical C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F2	0	Main window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
0Ch (102F18h)	**REG102F18**	**7:0**	**Default: 0xC0**	**Access: R/W**
	FORMAT_422_F2	7	Main window data format is 422.	
	422_INTP_F2	6	Main window 422 Cb Cr interpolation enable.	
	CR_LOAD_INI_F2	5	Main Cr_load initial value.	
	-	4:2	Reserved.	
	VSP_DITH_EN_F2	1	Main window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F2	0	Main window dithering enable for horizontal scaling process.	
0Ch (102F19h)	**REG102F19**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F2	3	Main window vertical Y coring enable.	
	VSP_CORING_EN_C_F2	2	Main window vertical C coring enable.	
	HSP_CORING_EN_Y_F2	1	Main window horizontal Y coring enable.	
	HSP_CORING_EN_C_F2	0	Main window horizontal C coring enable.	
0Dh (102F1Ah)	**REG102F1A**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSP_CORING_TH_C_F2[7:0]	7:0	Main window horizontal C coring threshold.	
0Dh (102F1Bh)	**REG102F1B**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSP_CORING_TH_Y_F2[7:	7:0	Main window horizontal Y coring threshold.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	0]			
0Eh (102F1Ch)	**REG102F1C**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSP_CORING_TH_C_F2[7:0]	7:0	Main window vertical C coring threshold.	
0Eh (102F1Dh)	**REG102F1D**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSP_CORING_TH_Y_F2[7:0]	7:0	Main window vertical Y coring threshold.	
0Fh (102F1Eh)	**REG102F1E**	**7:0**	**Default: 0x38**	**Access: R/W**
	HSP_DE_RING_G_ON_F2	7	Main window horizontal Y de-ringing enable.	
	HSP_DE_RING_TH1_F2[2:0]	6:4	Main window horizontal de-ringing threshold1.	
	HSP_DE_RING_TH0_F2[3:0]	3:0	Main window horizontal de-ringing threshold0.	
0Fh (102F1Fh)	**REG102F1F**	**7:0**	**Default: 0x58**	**Access: R/W**
	HSP_DE_RING_RB_ON_F2	7	Main window horizontal C de-ringing enable.	
	HSP_DE_RING_TH3_F2[2:0]	6:4	Main window horizontal de-ringing threshold3.	
	HSP_DE_RING_TH2_F2[3:0]	3:0	Main window horizontal de-ringing threshold2.	
10h (102F20h)	**REG102F20**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSP_OFFSET_F2[7:0]	7:0	Main window horizontal de-ringing offset.	
10h (102F21h)	**REG102F21**	**7:0**	**Default: 0x00**	**Access: R/W**
	HSP_OFFSET2_F2[7:0]	7:0	Main window horizontal de-ringing offset2.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x38**	**Access: R/W**
	VSP_DE_RING_G_ON_F2	7	Main window vertical Y de-ringing enable.	
	VSP_DE_RING_TH1_F2[2:0]	6:4	Main window vertical de-ringing threshold1.	
	VSP_DE_RING_TH0_F2[3:0]	3:0	Main window vertical de-ringing threshold0.	
11h (102F23h)	**REG102F23**	**7:0**	**Default: 0x58**	**Access: R/W**
	VSP_DE_RING_RB_ON_F2	7	Main window vertical C de-ringing enable.	
	VSP_DE_RING_TH3_F2[2:0]	6:4	Main window vertical de-ringing threshold3.	
	VSP_DE_RING_TH2_F2[3:0]	3:0	Main window vertical de-ringing threshold2.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
12h (102F24h)	**REG102F24**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSP_OFFSET_F2[7:0]	7:0	Main window vertical de-ringing offset.	
12h (102F25h)	**REG102F25**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSP_OFFSET2_F2[7:0]	7:0	Main window vertical de-ringing offset2.	
13h (102F26h)	**REG102F26**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_EN_F2	7	Main window vertical nonlinear scaling enable.	
	H_NL_EN_F2	6	Main window horizontal nonlinear scaling enable.	
	-	5:4	Reserved.	
	PREV_BOUND_MD_F2	3	Main window pre-V down scaling boundary mode.	
	OP_FIELD_SEL_F2	2	Main window field source selection. 0: From output timing. 1: From input timing.	
	FIELD_POL_F2	1	Main window field polarity switch.	
	2_INIFAC_MD_F2	0	Main window two initial factors mode.	
13h (102F27h)	**REG102F27**	**7:0**	**Default: 0x00**	**Access: R/W**
	VSP_3TAP_EN_F2	7	Main window vertical 3tap scaling enable.	
	V_NL_W2_LSB_F2	6	Main window vertical nonlinear scaling width2 LSB.	
	V_NL_W1_LSB_F2	5	Main window vertical nonlinear scaling width1 LSB.	
	V_NL_W0_LSB_F2	4	Main window vertical nonlinear scaling width0 LSB.	
	-	3	Reserved.	
	H_NL_W2_LSB_F2	2	Main window horizontal nonlinear scaling width2 LSB.	
	H_NL_W1_LSB_F2	1	Main window horizontal nonlinear scaling width1 LSB.	
	H_NL_W0_LSB_F2	0	Main window horizontal nonlinear scaling width0 LSB.	
14h (102F28h)	**REG102F28**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_W0_F2[7:0]	7:0	Main window horizontal nonlinear scaling width0.	
14h (102F29h)	**REG102F29**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_W1_F2[7:0]	7:0	Main window horizontal nonlinear scaling width1.	
15h (102F2Ah)	**REG102F2A**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_W2_F2[7:0]	7:0	Main window horizontal nonlinear scaling width2.	
15h (102F2Bh)	**REG102F2B**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_S_INI_F2	7	Main window horizontal nonlinear scaling initial sign.	
	H_NL_D_INI_F2[6:0]	6:0	Main window horizontal nonlinear scaling initial value.	
16h	**REG102F2C**	**7:0**	**Default: 0x00**	**Access: R/W**

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F2Ch)	H_NL_D0_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 0.	
16h (102F2Dh)	**REG102F2D**	**7:0**	**Default: 0x00**	**Access: R/W**
	H_NL_D1_F2[7:0]	7:0	Main window horizontal nonlinear scaling delta 1.	
17h (102F2Eh)	**REG102F2E**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_W0_F2[7:0]	7:0	Main window vertical nonlinear scaling width0.	
17h (102F2Fh)	**REG102F2F**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_W1_F2[7:0]	7:0	Main window vertical nonlinear scaling width1.	
18h (102F30h)	**REG102F30**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_W2_F2[7:0]	7:0	Main window vertical nonlinear scaling width2.	
18h (102F31h)	**REG102F31**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_S_INI_F2	7	Main window vertical nonlinear scaling initial sign.	
	V_NL_D_INI_F2[6:0]	6:0	Main window vertical nonlinear scaling initial value.	
19h (102F32h)	**REG102F32**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_D0_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 0.	
19h (102F33h)	**REG102F33**	**7:0**	**Default: 0x00**	**Access: R/W**
	V_NL_D1_F2[7:0]	7:0	Main window vertical nonlinear scaling delta 1.	
1Bh (102F36h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Ch (102F38h)	**REG102F38**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_FACTOR_HO[7:0]	7:0	Dynamic horizontal scaling factor.	
1Ch (102F39h)	**REG102F39**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_FACTOR_HO[15:8]	7:0	See description of '102F38h'.	
1Dh (102F3Ah)	**REG102F3A**	**7:0**	**Default: 0x10**	**Access: R/W**
	DY_FACTOR_HO[23:16]	7:0	See description of '102F38h'.	
1Eh (102F3Ch)	**REG102F3C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_FACTOR_VE[7:0]	7:0	Dynamic vertical scaling factor.	
1Eh (102F3Dh)	**REG102F3D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_FACTOR_VE[15:8]	7:0	See description of '102F3Ch'.	
1Fh (102F3Eh)	**REG102F3E**	**7:0**	**Default: 0x10**	**Access: R/W**
	DY_FACTOR_VE[23:16]	7:0	See description of '102F3Ch'.	
1Fh (102F3Fh)	**REG102F3F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DY_SELECT	7	Dynamic scaling factor usage. 0: For main window.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: For sub window.	
	-	6:0	Reserved.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SCALE_HO_EN_F1	0	Sub window horizontal scaling enable.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	SCALE_VE_EN_F1	0	Sub window vertical scaling enable.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	Y_RAM_SEL_HO_F1	7	Sub window horizontal Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_HO_F1	6	Sub window horizontal Y scaling filter SRAM usage enable.	
	C_RAM_SEL_HO_F1	5	Sub window horizontal C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_HO_F1	4	Sub window horizontal C scaling filter SRAM usage enable.	
	MODE_C_HO_F1[2:0]	3:1	Sub window horizontal C scaling filter mode. 0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_HO_F1	0	Sub window horizontal Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	Y_RAM_SEL_VE_F1	7	Sub window vertical Y scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	Y_RAM_EN_VE_F1	6	Sub window vertical Y scaling filter SRAM usage enable.	
	C_RAM_SEL_VE_F1	5	Sub window vertical C scaling filter SRAM selection. 0: SRAM 0. 1: SRAM 1.	
	C_RAM_EN_VE_F1	4	Sub window vertical C scaling filter SRAM usage enable.	
	MODE_C_VE_F1[2:0]	3:1	Sub window vertical C scaling filter mode.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Bypass. 1: Bilinear. 2: ROM Table 0. 3: ROM Table 1. 4: ROM Table 2.	
	MODE_Y_VE_F1	0	Sub window vertical Y scaling filter mode. 0: Bypass. 1: Bilinear.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x80**	**Access: R/W**
	FORMAT_422_F1	7	Sub window data format is 422.	
	-	6:2	Reserved.	
	VSP_DITH_EN_F1	1	Sub window dithering enable for vertical scaling process.	
	HSP_DITH_EN_F1	0	Sub window dithering enable for horizontal scaling process.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	VSP_CORING_EN_Y_F1	3	Sub window vertical Y coring enable.	
	VSP_CORING_EN_C_F1	2	Sub window vertical C coring enable.	
	HSP_CORING_EN_Y_F1	1	Sub window horizontal Y coring enable.	
	HSP_CORING_EN_C_F1	0	Sub window horizontal C coring enable.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	CRAM_RW_EN	1	C SRAM read/write enable.	
	YRAM_RW_EN	0	Y SRAM read/write enable.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	RAM_R_PULSE	1	SRAM read data pulse.	
	RAM_W_PULSE	0	SRAM write data pulse.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_ADDR[7:0]	7:0	SRAM read/write address. 0: Address 0~127. 1: Address 128~255.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_WDATA[7:0]	7:0	SRAM write data.	
43h	**REG102F87**	**7:0**	**Default: 0x00**	**Access: R/W**

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(102F87h)	RAM_WDATA[15:8]	7:0	See description of '102F86h'.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_WDATA[23:16]	7:0	See description of '102F86h'.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_WDATA[31:24]	7:0	See description of '102F86h'.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: R/W**
	RAM_WDATA[39:32]	7:0	See description of '102F86h'.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: RO**
	RAM_RDATA[7:0]	7:0	SRAM read data.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x00**	**Access: RO**
	RAM_RDATA[15:8]	7:0	See description of '102F8Ch'.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: RO**
	RAM_RDATA[23:16]	7:0	See description of '102F8Ch'.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: RO**
	RAM_RDATA[31:24]	7:0	See description of '102F8Ch'.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: RO**
	RAM_RDATA[39:32]	7:0	See description of '102F8Ch'.	
51h (102FA2h)	**REG102FA2**	**7:0**	**Default: 0x41**	**Access: R/W**
	SIMPLE_INTP	7	Simple interpolation for 422 to 444 conversion.	
	FACTOR_MANUAL	6	Vertical factor manual mode.	
	VDOWN_SEL	5	Vertical scaling down selection. 0: Bottom. 1: Top.	
	HDOWN_SEL	4	Horizontal scaling down selection. 0: Bottom. 1: Top.	
	-	3	Reserved.	
	PSEUDO_VCLR_NO[1:0]	2:1	Dither pseudo code Vsync clear number.	
	PSEUDO_VCLR_EN	0	Dither pseudo code Vsync clear enable.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	FBL_R_TRIG_SEL	7	FBL read trigger selection. 0: Command finish. 1: DE end.	
	-	6:0	Reserved.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x08**	**Access: R/W**
	3DLR_SIDE2LINE_EN	7	3D LR side-by-side to line-to-line enable.	
	-	6:0	Reserved.	
58h ~ 5Fh (102FB0h ~ 102FBFh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
60h (102FC0h)	**REG102FC0**	**7:0**	**Default: 0x80**	**Access: R/W**
	CTI_STEP_F2[1:0]	7:6	Main window CTI step.	
	-	5:3	Reserved.	
	CTI_LPF_COEF_F2[2:0]	2:0	Main window CTI LPF coefficients.	
61h (102FC3h)	**REG102FC3**	**7:0**	**Default: 0x00**	**Access: R/W**
	CTI_EN_F2	7	Main window CTI enable.	
	-	6:0	Reserved.	
62h (102FC4h)	**REG102FC4**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	CTI_MUTUAL_THD_F2[3:0]	3:0	Main window CTI mutual threshold.	
62h (102FC5h)	**REG102FC5**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:3	Reserved.	
	CTI_MUTUAL_STEP_F2[2:0]	2:0	Main window CTI mutual step.	
63h (102FC6h)	**REG102FC6**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	CTI_PATCH_MODE_F2[1:0]	1:0	Main window CTI patch mode. 0: None. 1: Trans. 2: CLFP/WTS. 3: Both.	
64h (102FC8h)	**REG102FC8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	CTI_TRANS_OFFSET_F2[4:0]	4:0	Main window CTI mutual level patch threshold.	
64h (102FC9h)	**REG102FC9**	**7:0**	**Default: 0x28**	**Access: R/W**
	-	7:6	Reserved.	
	CTI_TRANS_SLOPE_F2[5:0	5:0	Main window CTI mutual trans level slope gain.	

HVSP Register (Bank = 102F, Sub-bank = 23)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	]			
65h (102FCAh)	**REG102FCA**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:5	Reserved.	
	CTI_CLFP_OFFSET_F2[4:0]	4:0	Main window CTI mutual C low freq threshold.	
65h (102FCBh)	**REG102FCB**	**7:0**	**Default: 0x14**	**Access: R/W**
	-	7:6	Reserved.	
	CTI_CLFP_SLOPE_F2[5:0]	5:0	Main window CTI mutual C low freq slope gain.	
66h (102FCCh)	**REG102FCC**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	CTI_CLFP_STEP_F2	0	Main window CTI mutual C low freq step.	
70h (102FE0h)	**REG102FE0**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	CTI_LPF_COEF_F1[2:0]	2:0	Sub window CTI LPF coefficients.	
71h (102FE3h)	**REG102FE3**	**7:0**	**Default: 0x00**	**Access: R/W**
	CTI_EN_F1	7	Sub window CTI enable.	
	-	6:0	Reserved.	
77h (102FEFh)	**REG102FEF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	EXTRA_FACTOR_EN	0	Extra horizontal initial factor enable.	
78h (102FF0h)	**REG102FF0**	**7:0**	**Default: 0x00**	**Access: R/W**
	EXTRA_INI_FACTOR_HO_1 [7:0]	7:0	Extra horizontal initial factor 1.	
78h (102FF1h)	**REG102FF1**	**7:0**	**Default: 0x00**	**Access: R/W**
	EXTRA_INI_FACTOR_HO_2 [7:0]	7:0	Extra horizontal initial factor 2.	
79h (102FF2h)	**REG102FF2**	**7:0**	**Default: 0x00**	**Access: R/W**
	EXTRA_INI_FACTOR_HO_3 [7:0]	7:0	Extra horizontal initial factor 3.	
79h (102FF3h)	**REG102FF3**	**7:0**	**Default: 0x00**	**Access: R/W**
	EXTRA_INI_FACTOR_HO_4 [7:0]	7:0	Extra horizontal initial factor 4.	

FRC Register (Bank = 102F, Sub-bank = 24)

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
3Fh (102F7Eh)	**REG102F7E**	**7:0**	**Default: 0x13**	**Access: R/W**
	-	7:5	Reserved.	
	TAILCUT	4	TAILCUT enable.	
	NOISE_DITH_DISABLE	3	PAFRC mixed with noise dither disable. 0: Disable. 1: Enable.	
	DITH_BITS	2	Dithering bits. 0: 2-bits. 1: 4-bits.	
	TCON_OFF_EN	1	TCON FRC_GAMMA function off signal enable. 0: Ignore TCON gamma/dither turn off signal. 1: Gamma/dither function turn off by TCON FRC_GAMMA_OFF signal.	
	FRC_ON	0	PAFRC enable.	
40h (102F80h)	**REG102F80**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_ROTATE_EN	7	Box A/B/C/D relation rotation enable.	
	TOP_BOX_UNIT_FLAG[1:0]	6:5	Top box A/B/C/D swap flag. 00: Per 2x2 box. 01: Per 4x4 box. 1x: Per 8x8 box.	
	TOP_BOX_FREEZE	4	Top box freeze.	
	TOP_BOX_SHRINK	3	Top box shrink to 2x2 from 4x4.	
	FR_C2_BIT	2	Top box frame rotation step bit location for codexx10. 0: Bit[0]. 1: Bit[1].	
	C2X2_ROT_B_DIR_S	1	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	D2X2_ROT_B_DIR_S	0	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
40h (102F81h)	**REG102F81**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	G_V_SWAP	6	Green channel vertical swap, avoid polarity not consistent.	
	G_H_SWAP	5	Green channel horizontal swap, avoid polarity not consistent.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	B_D_SWAP	4	Blue channel diagonal swap.	
	BOX_FR_SW	3	FRAME_CNT bit [1:0] swap for box rotate.	
	BOX4X4_FR_SW	2	FRAME_CNT bit [1:0] swap for box4x4 rotate.	
	BOX8X8_ROT_UNIT	1	0: Rotate step under per A, B, C or D. 1: Rotate step between A/B/C/D.	
	BOX_FREEZE	0	Box local rotation freeze.	
41h (102F82h)	**REG102F82**	**7:0**	**Default: 0x00**	**Access: R/W**
	C2X2_ROT_G_DIR	7	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	D2X2_ROT_G_DIR	6	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	C2X2_ROT_G_DIR_S	5	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	D2X2_ROT_G_DIR_S	4	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	A2X2_ROT_B_DIR	3	A 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	B2X2_ROT_B_DIR	2	B 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	C2X2_ROT_B_DIR	1	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	D2X2_ROT_B_DIR	0	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
41h (102F83h)	**REG102F83**	**7:0**	**Default: 0x00**	**Access: R/W**
	A2X2_ROT_R_DIR	7	A 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	B2X2_ROT_R_DIR	6	B 2x2 block rotation direction. 0: Clockwise.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Counterclockwise.	
	C2X2_ROT_R_DIR	5	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	D2X2_ROT_R_DIR	4	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	C2X2_ROT_R_DIR_S	3	C 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	D2X2_ROT_R_DIR_S	2	D 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise, 2nd.	
	A2X2_ROT_G_DIR	1	A 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
	B2X2_ROT_G_DIR	0	B 2x2 block rotation direction. 0: Clockwise. 1: Counterclockwise.	
42h (102F84h)	**REG102F84**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_SEQ2[7:0]	7:0	Top box frame 2nd 4 frame rotation step.	
42h (102F85h)	**REG102F85**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_SEQ1[7:0]	7:0	Top box frame 1st 4 frame rotation step.	
43h (102F86h)	**REG102F86**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_SEQ4[7:0]	7:0	Top box frame 4th 4 frame rotation step.	
43h (102F87h)	**REG102F87**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_SEQ3[7:0]	7:0	Top box frame 3rd 4 frame rotation step.	
44h (102F88h)	**REG102F88**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_C2_SEQ34[7:0]	7:0	Top box frame 3rd/4th 4 frame rotation step for codexx10.	
44h (102F89h)	**REG102F89**	**7:0**	**Default: 0x00**	**Access: R/W**
	TOP_BOX_FR_C2_SEQ12[7:0]	7:0	Top box frame 1st/2nd 4 frame rotation step for codexx10.	
45h (102F8Ah)	**REG102F8A**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_A_ROT_DIR	7	Location A frame counter direction. 0: Clockwise.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Back.	
	BOX_B_ROT_DIR	6	Location B frame counter direction. 0: Clockwise. 1: Back.	
	BOX_C_ROT_DIR	5	Location C frame counter direction. 0: Clockwise. 1: Back.	
	BOX_D_ROT_DIR	4	Location D frame counter direction. 0: Clockwise. 1: Back.	
	-	3:0	Reserved.	
45h (102F8Bh)	**REG102F8B**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX8X8_ROT_00[1:0]	7:6	Box8x8 entity 00 rotation step by reference.	
	BOX8X8_ROT_01[1:0]	5:4	Box8x8 entity 01 rotation step by reference.	
	BOX8X8_ROT_11[1:0]	3:2	Box8x8 entity 11 rotation step by reference.	
	BOX8X8_ROT_10[1:0]	1:0	Box8x8 entity 10 rotation step by reference.	
46h (102F8Ch)	**REG102F8C**	**7:0**	**Default: 0x00**	**Access: R/W**
	B_LU_00[1:0]	7:6	B 2x2 block left up entity.	
	B_RU_01[1:0]	5:4	B 2x2 block right up entity.	
	B_RD_11[1:0]	3:2	B 2x2 block right down entity.	
	B_LD_10[1:0]	1:0	B 2x2 block left down entity.	
46h (102F8Dh)	**REG102F8D**	**7:0**	**Default: 0x00**	**Access: R/W**
	A_LU_00[1:0]	7:6	A 2x2 block left up entity.	
	A_RU_01[1:0]	5:4	A 2x2 block right up entity.	
	A_RD_11[1:0]	3:2	A 2x2 block right down entity.	
	A_LD_10[1:0]	1:0	A 2x2 block left down entity.	
47h (102F8Eh)	**REG102F8E**	**7:0**	**Default: 0x00**	**Access: R/W**
	D_LU_00[1:0]	7:6	D 2x2 block left up entity.	
	D_RU_01[1:0]	5:4	D 2x2 block right up entity.	
	D_RD_11[1:0]	3:2	D 2x2 block right down entity.	
	D_LD_10[1:0]	1:0	D 2x2 block left down entity.	
47h (102F8Fh)	**REG102F8F**	**7:0**	**Default: 0x00**	**Access: R/W**
	C_LU_00[1:0]	7:6	C 2x2 block left up entity.	
	C_RU_01[1:0]	5:4	C 2x2 block right up entity.	

FRC Register (Bank = 102F, Sub-bank = 24)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	C_RD_11[1:0]	3:2	C 2x2 block right down entity.	
	C_LD_10[1:0]	1:0	C 2x2 block left down entity.	
48h (102F90h)	**REG102F90**	**7:0**	**Default: 0x00**	**Access: R/W**
	D_LU_00_S[1:0]	7:6	D 2x2 block left up entity, 2nd.	
	D_RU_01_S[1:0]	5:4	D 2x2 block right up entity, 2nd.	
	D_RD_11_S[1:0]	3:2	D 2x2 block right down entity, 2nd.	
	D_LD_10_S[1:0]	1:0	D 2x2 block left down entity, 2nd.	
48h (102F91h)	**REG102F91**	**7:0**	**Default: 0x00**	**Access: R/W**
	C_LU_00_S[1:0]	7:6	C 2x2 block left up entity, 2nd.	
	C_RU_01_S[1:0]	5:4	C 2x2 block right up entity, 2nd.	
	C_RD_11_S[1:0]	3:2	C 2x2 block right down entity, 2nd.	
	C_LD_10_S[1:0]	1:0	C 2x2 block left down entity, 2nd.	
49h (102F92h)	**REG102F92**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_B_LU_00[1:0]	7:6	Location B block A LSB 2 bits plus value.	
	BOX_B_RU_01[1:0]	5:4	Location B block B LSB 2 bits plus value.	
	BOX_B_RD_11[1:0]	3:2	Location B block C LSB 2 bits plus value.	
	BOX_B_LD_10[1:0]	1:0	Location B block D LSB 2 bits plus value.	
49h (102F93h)	**REG102F93**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_A_LU_00[1:0]	7:6	Location A block A LSB 2 bits plus value.	
	BOX_A_RU_01[1:0]	5:4	Location A block B LSB 2 bits plus value.	
	BOX_A_RD_11[1:0]	3:2	Location A block C LSB 2 bits plus value.	
	BOX_A_LD_10[1:0]	1:0	Location A block D LSB 2 bits plus value.	
4Ah (102F94h)	**REG102F94**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_D_LU_00[1:0]	7:6	Location D block A LSB 2 bits plus value.	
	BOX_D_RU_01[1:0]	5:4	Location D block B LSB 2 bits plus value.	
	BOX_D_RD_11[1:0]	3:2	Location D block C LSB 2 bits plus value.	
	BOX_D_LD_10[1:0]	1:0	Location D block D LSB 2 bits plus value.	
4Ah (102F95h)	**REG102F95**	**7:0**	**Default: 0x00**	**Access: R/W**
	BOX_C_LU_00[1:0]	7:6	Location C block A LSB 2 bits plus value.	
	BOX_C_RU_01[1:0]	5:4	Location C block B LSB 2 bits plus value.	
	BOX_C_RD_11[1:0]	3:2	Location C block C LSB 2 bits plus value.	
	BOX_C_LD_10[1:0]	1:0	Location C block D LSB 2 bits plus value.	

XV_YCC Register (Bank = 102F, Sub-bank = 25)

XV_YCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (102F02h)	**REG102F02**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	POST_MAIN_NOISE_ROUND_EN	6	Main window post noise rounding enable.	
	POST_MAIN_CON_EN	5	Main window post contrast enable.	
	POST_MAIN_BRI_EN	4	Main window post brightness enable.	
	-	3:0	Reserved.	
01h ~ 10h (102F03h ~ 102F21h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
11h (102F22h)	**REG102F22**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	POST_SUB_NOISE_ROUND_EN	6	Sub window post noise rounding enable.	
	POST_SUB_CON_EN	5	Sub window post contrast enable.	
	POST_SUB_BRI_EN	4	Sub window post brightness enable.	
	-	3:0	Reserved.	
11h ~ 20h (102F23h ~ 102F41h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_R_BRI_OFFSET[7:0]	7:0	Main window post R channel offset.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_MAIN_R_BRI_OFFSET[10:8]	2:0	See description of '102F42h'.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_G_BRI_OFFSET[7:0]	7:0	Main window post G channel offset.	
22h (102F45h)	**REG102F45**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_MAIN_G_BRI_OFFSET[10:8]	2:0	See description of '102F44h'.	

XV_YCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
23h (102F46h)	**REG102F46**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_B_BRI_OFFSET[7:0]	7:0	Main window post B channel offset.	
23h (102F47h)	**REG102F47**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_MAIN_B_BRI_OFFSET[10:8]	2:0	See description of '102F46h'.	
24h (102F48h)	**REG102F48**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_R_CON_GAIN[7:0]	7:0	Main window post R channel gain.	
24h (102F49h)	**REG102F49**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_MAIN_R_CON_GAIN[11:8]	3:0	See description of '102F48h'.	
25h (102F4Ah)	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_G_CON_GAIN[7:0]	7:0	Main window post G channel gain.	
25h (102F4Bh)	**REG102F4B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_MAIN_G_CON_GAIN[11:8]	3:0	See description of '102F4Ah'.	
26h (102F4Ch)	**REG102F4C**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_MAIN_B_CON_GAIN[7:0]	7:0	Main window post B channel gain.	
26h (102F4Dh)	**REG102F4D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_MAIN_B_CON_GAIN[11:8]	3:0	See description of '102F4Ch'.	
27h (102F4Eh)	**REG102F4E**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_R_BRI_OFFSET[7:0]	7:0	Sub window post R channel offset.	
27h (102F4Fh)	**REG102F4F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_SUB_R_BRI_OFFSET[10:8]	2:0	See description of '102F4Eh'.	

XV_YCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
28h (102F50h)	**REG102F50**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_G_BRI_OFFSET [7:0]	7:0	Sub window post G channel offset.	
28h (102F51h)	**REG102F51**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_SUB_G_BRI_OFFSET [10:8]	2:0	See description of '102F50h'.	
29h (102F52h)	**REG102F52**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_B_BRI_OFFSET [7:0]	7:0	Sub window post B channel offset.	
29h (102F53h)	**REG102F53**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	POST_SUB_B_BRI_OFFSET [10:8]	2:0	See description of '102F52h'.	
2Ah (102F54h)	**REG102F54**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_R_CON_GAIN[7:0]	7:0	Sub window post R channel gain.	
2Ah (102F55h)	**REG102F55**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_SUB_R_CON_GAIN[11:8]	3:0	See description of '102F54h'.	
2Bh (102F56h)	**REG102F56**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_G_CON_GAIN[7:0]	7:0	Sub window post G channel gain.	
2Bh (102F57h)	**REG102F57**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_SUB_G_CON_GAIN[11:8]	3:0	See description of '102F56h'.	
2Ch (102F58h)	**REG102F58**	**7:0**	**Default: 0x00**	**Access: R/W**
	POST_SUB_B_CON_GAIN[7 :0]	7:0	Sub window post B channel gain.	
2Ch (102F59h)	**REG102F59**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	POST_SUB_B_CON_GAIN[1 1:8]	3:0	See description of '102F58h'.	

XV_YCC Register (Bank = 102F, Sub-bank = 25)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
2Dh ~ 6Ah (102F5Ah ~ 102FD4h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

SPIKE_NR Register (Bank = 102F, Sub-bank = 26)

SPIKE_NR Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
50h (102FA0h)	**REG102FA0**	**7:0**	**Default: 0x44**	**Access: R/W**
	-	7:6	Reserved.	
	V_C_LPF_EN_F1	5	Vertical C Low Pass Filter Enable F1.	
	SPIKE_NR_EN_F1	4	Spike NR Enable F1.	
	SPIKE_NR_MR_EN	3	Spike NR motion ratio enable.	
	-	2	Reserved.	
	V_C_LPF_EN_F2	1	Vertical C Low Pass Filter Enable F2.	
	SPIKE_NR_EN_F2	0	Spike NR Enable F2.	
50h (102FA1h)	**REG102FA1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SPIKE_NR_COEF[3:0]	3:0	Spike NR Coefficient.	
51h (102FA2h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
51h (102FA3h)	**REG102FA3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	P_THRD_1[4:0]	4:0	Spike NR P threshold 1.	
52h (102FA4h)	**REG102FA4**	**7:0**	**Default: 0x00**	**Access: R/W**
	P_THRD_2[7:0]	7:0	Spike NR P threshold 2.	
52h (102FA5h)	**REG102FA5**	**7:0**	**Default: 0x00**	**Access: R/W**
	P_THRD_3[7:0]	7:0	Spike NR P threshold 3.	
53h (102FA6h)	**REG102FA6**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	D_31_STEP[2:0]	6:4	Spike NR D31 Step.	
	-	3	Reserved.	
	D_11_21_STEP[2:0]	2:0	Spike NR D11_21 Step.	
53h (102FA7h)	**REG102FA7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	YP_22_STEP[2:0]	2:0	Spike NR YP22 Step.	
54h (102FA8h)	**REG102FA8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SPK_MR_LPF_EN_F1	4	Spike NR motion ratio low pass filter enable F1 (LPF is 3x3 mask).	

SPIKE_NR Register (Bank = 102F, Sub-bank = 26)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3:1	Reserved.	
	SPK_MR_LPF_EN_F2	0	Spike NR motion ratio low pass filter enable F2 (LPF is 3x3 mask).	
54h (102FA9h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
55h (102FAAh)	**REG102FAA**	**7:0**	**Default: 0x10**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_0[7:0]	7:0	Spike NR motion ratio look-up-table 0.	
55h (102FABh)	**REG102FAB**	**7:0**	**Default: 0x32**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_1[7:0]	7:0	Spike NR motion ratio look-up-table 1.	
56h (102FACh)	**REG102FAC**	**7:0**	**Default: 0x54**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_2[7:0]	7:0	Spike NR motion ratio look-up-table 2.	
56h (102FADh)	**REG102FAD**	**7:0**	**Default: 0x76**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_3[7:0]	7:0	Spike NR motion ratio look-up-table 3.	
57h (102FAEh)	**REG102FAE**	**7:0**	**Default: 0x98**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_4[7:0]	7:0	Spike NR motion ratio look-up-table 4.	
57h (102FAFh)	**REG102FAF**	**7:0**	**Default: 0xBA**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_5[7:0]	7:0	Spike NR motion ratio look-up-table 5.	
58h (102FB0h)	**REG102FB0**	**7:0**	**Default: 0xDC**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_6[7:0]	7:0	Spike NR motion ratio look-up-table 6.	
58h (102FB1h)	**REG102FB1**	**7:0**	**Default: 0xFE**	**Access: R/W**
	SPIKE_NR_MOTION_LUT_7[7:0]	7:0	Spike NR motion ratio look-up-table 7.	

ACE2 Register (Bank = 102F, Sub-bank = 27)

ACE2 Register (Bank = 102F, Sub-bank = 27)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
08h (102F10h)	**REG102F10**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	SUB_CURVE_FIT_CF_LPF_EN	5	Sub window color factor low pass filter enable for luma curve [1 2 1].	
	SUB_COLOR_CURVE_FIT_EN	4	Sub window color adaptive enable for luma curve.	
	-	3:2	Reserved.	
	MAIN_CURVE_FIT_CF_LPF_EN	1	Main window color factor low pass filter enable for luma curve [1 2 1].	
	MAIN_COLOR_CURVE_FIT_EN	0	Main window color adaptive enable for luma curve.	
08h (102F11h)	**REG102F11**	**7:0**	**Default: 0x08**	**Access: R/W**
	-	7:4	Reserved.	
	COLOR_PK_WIN1_CF_ENTRY_VALUE[3:0]	3:0	Flesh color adaptive noise masking strength (x.xxx), color defined from peaking, format is x.xxx; range is 4'h0~4'h8.	
20h (102F40h)	**REG102F40**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	SUB_CTI_EN	4	Sub window CTI enable.	
	-	3:1	Reserved.	
	MAIN_CTI_EN	0	Main window CTI enable.	
21h (102F42h)	**REG102F42**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	MAIN_CTI_STEP[2:0]	6:4	Main window CTI step.	
	-	3:0	Reserved.	
21h (102F43h)	**REG102F43**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	MAIN_CTI_CORING_THRD[3:0]	3:0	Main window CTI coring threshold.	
22h (102F44h)	**REG102F44**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	MAIN_CTI_BAND_COEF[5:0]	5:0	Main window CTI band pass filter coefficient.	
25h	**REG102F4A**	**7:0**	**Default: 0x00**	**Access: R/W**

ACE2 Register (Bank = 102F, Sub-bank = 27)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
(102F4Ah)	-	7:4	Reserved.
	MAIN_CTI_GRAY_THRD[3:0]	3:0	Main window CTI gray patch threshold.

Scaler 2 Register (Bank = 1030)

DISP_TC Register (Bank = 1030, Sub-bank = 00)

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
03h (103006h)	**REG103006**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	TCON	2	TCON enable. (TCON = bounding & TCON).	
	-	1:0	Reserved.	
03h (103007h)	**REG103007**	**7:0**	**Default: 0x00**	**Access: R/W**
	PUA	7	Power-up Active. When PUA=1, TCON signals start to output to PAD. Reg003 bit 14 (PUA = PUA | !TCON).	
	TC_CNT_EN	6	Enable TCON_CNT.	
	SEP_PUA	5	Enable separate PUA. 0: All GPO will be controlled by PUA. 1: Each GPO_S PUA is controlled by itself PUA.	
	-	4:0	Reserved.	
04h (103008h)	**REG103008**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H1END_ODD[7:0]	7:0	The odd line HEND of GPO1 for Special Over Mode / 2nd horizontal end of GPO1.	
04h (103009h)	**REG103009**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7	Reserved.	
	OVER_MODE_1	6	Special over mode enable of GPO1. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H1END_ODD.	
	HEAD_PROC_EN_1	5	Head process enable of GPO1.	
	HEAD_MODE_1	4	Head mode enable of GPO1.	
	TC_H1END_ODD[11:8]	3:0	See description of '103008h'.	
05h (10300Ah)	**REG10300A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H2END_ODD[7:0]	7:0	The odd line HEND of GPO2 for Special Over Mode / 2nd horizontal end of GPO2.	
05h (10300Bh)	**REG10300B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7	Reserved.	
	OVER_MODE_2	6	Special over mode enable of GPO2. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H2END_ODD.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HEAD_PROC_EN_2	5	Head process enable of GPO2.	
	HEAD_MODE_2	4	Head mode enable of GPO2.	
	TC_H2END_ODD[11:8]	3:0	See description of '10300Ah'.	
06h (10300Ch)	**REG10300C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H3END_ODD[7:0]	7:0	The odd line HEND of GPO3 for Special Over Mode / 2nd horizontal end of GPO3.	
06h (10300Dh)	**REG10300D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7	Reserved.	
	OVER_MODE_3	6	Special over mode enable of GPO3. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H3END_ODD.	
	HEAD_PROC_EN_3	5	Head process enable of GPO3.	
	HEAD_MODE_3	4	Head mode enable of GPO3.	
	TC_H3END_ODD[11:8]	3:0	See description of '10300Ch'.	
07h (10300Eh)	**REG10300E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H4END_ODD[7:0]	7:0	The odd line HEND of GPO4 for Special Over Mode / 2nd horizontal end of GPO4.	
07h (10300Fh)	**REG10300F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7	Reserved.	
	OVER_MODE_4	6	Special over mode enable of GPO4. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H4END_ODD.	
	HEAD_PROC_EN_4	5	Head process enable of GPO4.	
	HEAD_MODE_4	4	Head mode enable of GPO4.	
	TC_H4END_ODD[11:8]	3:0	See description of '10300Eh'.	
08h (103010h)	**REG103010**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H5END_ODD[7:0]	7:0	The odd line HEND of GPO5 for Special Over Mode / 2nd horizontal end of GPO5.	
08h (103011h)	**REG103011**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7	Reserved.	
	OVER_MODE_5	6	Special over mode enable of GPO5. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H5END_ODD.	
	HEAD_PROC_EN_5	5	Head process enable of GPO5.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	HEAD_MODE_5	4	Head mode enable of GPO5.	
	TC_H5END_ODD[11:8]	3:0	See description of '103010h'.	
09h (103012h)	**REG103012**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H6END_ODD[7:0]	7:0	The odd line HEND of GPO6 for Special Over Mode / 2nd horizontal end of GPO9.	
09h (103013h)	**REG103013**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7	Reserved.	
	OVER_MODE_6	6	Special over mode enable of GPO6. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H6END_ODD.	
	HEAD_PROC_EN_6	5	Head process enable of GPO6.	
	HEAD_MODE_6	4	Head mode enable of GPO6.	
	TC_H6END_ODD[11:8]	3:0	See description of '103012h'.	
0Ah (103014h)	**REG103014**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H7END_ODD[7:0]	7:0	The odd line HEND of GPO7 for Special Over Mode / 2nd horizontal end of GPOA.	
0Ah (103015h)	**REG103015**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7	Reserved.	
	OVER_MODE_7	6	Special over mode enable of GPO7. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H7END_ODD.	
	HEAD_PROC_EN_7	5	Head process enable of GPO7.	
	HEAD_MODE_7	4	Head mode enable of GPO7.	
	TC_H7END_ODD[11:8]	3:0	See description of '103014h'.	
0Bh (103016h)	**REG103016**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H8END_ODD[7:0]	7:0	The odd line HEND of GPO8 for Special Over Mode / 2nd horizontal end of GPOB.	
0Bh (103017h)	**REG103017**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7	Reserved.	
	OVER_MODE_8	6	Special over mode enable of GPO8. 1: If the 1st GPO end position is at odd line, its horizontal end position will be determined by TC_H8END_ODD.	
	HEAD_PROC_EN_8	5	Head process enable of GPO8.	
	HEAD_MODE_8	4	Head mode enable of GPO8.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_H8END_ODD[11:8]	3:0	See description of '103016h'.	
0Dh (10301Ah)	**REG10301A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V0ST[7:0]	7:0	Vertical start of GPO0.	
0Dh (10301Bh)	**REG10301B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG0_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO0.	
	TC_V0ST[11:8]	3:0	See description of '10301Ah'.	
0Eh (10301Ch)	**REG10301C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V0END[7:0]	7:0	Vertical end of GPO0.	
0Eh (10301Dh)	**REG10301D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG0_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO0. (If set to 2, it means 3 frame toggle once.)	
	TC_V0END[11:8]	3:0	See description of '10301Ch'.	
0Fh (10301Eh)	**REG10301E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H0ST[7:0]	7:0	Horizontal start of GPO0.	
0Fh (10301Fh)	**REG10301F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG0_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO0.	
	TC_H0ST[11:8]	3:0	See description of '10301Eh'.	
10h (103020h)	**REG103020**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H0END[7:0]	7:0	Horizontal end of GPO0.	
10h (103021h)	**REG103021**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG0_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO0. (If set to 2, it means 3 lines toggle once.)	
	TC_H0END[11:8]	3:0	See description of '103020h'.	
11h (103022h)	**REG103022**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V1ST[7:0]	7:0	Vertical start of GPO1.	
11h (103023h)	**REG103023**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG1_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO1.	
	TC_V1ST[11:8]	3:0	See description of '103022h'.	
12h (103024h)	**REG103024**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V1END[7:0]	7:0	Vertical end of GPO1.	
12h (103025h)	**REG103025**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG1_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO1. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_V1END[11:8]	3:0	See description of '103024h'.	
13h (103026h)	**REG103026**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H1ST[7:0]	7:0	Horizontal start of GPO1.	
13h (103027h)	**REG103027**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG1_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO1.	
	TC_H1ST[11:8]	3:0	See description of '103026h'.	
14h (103028h)	**REG103028**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H1END[7:0]	7:0	Horizontal end of GPO1.	
14h (103029h)	**REG103029**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG1_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO1. (If set to 2, it means 3 lines toggle once.)	
	TC_H1END[11:8]	3:0	See description of '103028h'.	
15h (10302Ah)	**REG10302A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V2ST[7:0]	7:0	Vertical start of GPO2.	
15h (10302Bh)	**REG10302B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG2_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO2.	
	TC_V2ST[11:8]	3:0	See description of '10302Ah'.	
16h (10302Ch)	**REG10302C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V2END[7:0]	7:0	Vertical end of GPO2.	
16h (10302Dh)	**REG10302D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG2_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO2. (If set to 2, it means 3 lines toggle once.)	
	TC_V2END[11:8]	3:0	See description of '10302Ch'.	
17h (10302Eh)	**REG10302E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H2ST[7:0]	7:0	Horizontal start of GPO2.	
17h (10302Fh)	**REG10302F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG2_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO2.	
	TC_H2ST[11:8]	3:0	See description of '10302Eh'.	
18h (103030h)	**REG103030**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H2END[7:0]	7:0	Horizontal end of GPO2.	
18h (103031h)	**REG103031**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG2_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO2. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_H2END[11:8]	3:0	See description of '103030h'.	
19h (103032h)	**REG103032**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V3ST[7:0]	7:0	Vertical start of GPO3.	
19h (103033h)	**REG103033**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG3_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO3.	
	TC_V3ST[11:8]	3:0	See description of '103032h'.	
1Ah (103034h)	**REG103034**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V3END[7:0]	7:0	Vertical end of GPO3.	
1Ah (103035h)	**REG103035**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG3_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO3. (If set to 2, it means 3 lines toggle once.)	
	TC_V3END[11:8]	3:0	See description of '103034h'.	
1Bh (103036h)	**REG103036**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H3ST[7:0]	7:0	Horizontal start of GPO3.	
1Bh (103037h)	**REG103037**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG3_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO3.	
	TC_H3ST[11:8]	3:0	See description of '103036h'.	
1Ch (103038h)	**REG103038**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H3END[7:0]	7:0	Horizontal end of GPO3.	
1Ch (103039h)	**REG103039**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG3_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO3. (If set to 2, it means 3 lines toggle once.)	
	TC_H3END[11:8]	3:0	See description of '103038h'.	
1Dh (10303Ah)	**REG10303A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V4ST[7:0]	7:0	Vertical start of GPO4.	
1Dh (10303Bh)	**REG10303B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG4_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO4.	
	TC_V4ST[11:8]	3:0	See description of '10303Ah'.	
1Eh (10303Ch)	**REG10303C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V4END[7:0]	7:0	Vertical end of GPO4.	
1Eh (10303Dh)	**REG10303D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG4_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO4. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_V4END[11:8]	3:0	See description of '10303Ch'.	
1Fh (10303Eh)	**REG10303E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H4ST[7:0]	7:0	Horizontal start of GPO4.	
1Fh (10303Fh)	**REG10303F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG4_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO4.	
	TC_H4ST[11:8]	3:0	See description of '10303Eh'.	
20h (103040h)	**REG103040**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H4END[7:0]	7:0	Horizontal end of GPO4.	
20h (103041h)	**REG103041**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG4_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO4. (If set to 2, it means 3 lines toggle once.)	
	TC_H4END[11:8]	3:0	See description of '103040h'.	
21h (103042h)	**REG103042**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V5ST[7:0]	7:0	Vertical start of GPO5.	
21h (103043h)	**REG103043**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG5_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO5.	
	TC_V5ST[11:8]	3:0	See description of '103042h'.	
22h (103044h)	**REG103044**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V5END[7:0]	7:0	Vertical end of GPO5.	
22h (103045h)	**REG103045**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG5_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO5. (If set to 2, it means 3 lines toggle once.)	
	TC_V5END[11:8]	3:0	See description of '103044h'.	
23h (103046h)	**REG103046**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H5ST[7:0]	7:0	Horizontal start of GPO5.	
23h (103047h)	**REG103047**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG5_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO5.	
	TC_H5ST[11:8]	3:0	See description of '103046h'.	
24h (103048h)	**REG103048**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H5END[7:0]	7:0	Horizontal end of GPO5.	
24h (103049h)	**REG103049**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG5_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO5. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_H5END[11:8]	3:0	See description of '103048h'.	
25h (10304Ah)	**REG10304A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V6ST[7:0]	7:0	Vertical start of GPO6.	
25h (10304Bh)	**REG10304B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG6_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO6.	
	TC_V6ST[11:8]	3:0	See description of '10304Ah'.	
26h (10304Ch)	**REG10304C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V6END[7:0]	7:0	Vertical end of GPO6.	
26h (10304Dh)	**REG10304D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG6_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO6. (If set to 2, it means 3 lines toggle once.)	
	TC_V6END[11:8]	3:0	See description of '10304Ch'.	
27h (10304Eh)	**REG10304E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H6ST[7:0]	7:0	Horizontal start of GPO6.	
27h (10304Fh)	**REG10304F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG6_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO6.	
	TC_H6ST[11:8]	3:0	See description of '10304Eh'.	
28h (103050h)	**REG103050**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H6END[7:0]	7:0	Horizontal end of GPO6.	
28h (103051h)	**REG103051**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG6_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO6. (If set to 2, it means 3 lines toggle once.)	
	TC_H6END[11:8]	3:0	See description of '103050h'.	
29h (103052h)	**REG103052**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V7ST[7:0]	7:0	Vertical start of GPO7.	
29h (103053h)	**REG103053**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG7_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO7.	
	TC_V7ST[11:8]	3:0	See description of '103052h'.	
2Ah (103054h)	**REG103054**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V7END[7:0]	7:0	Vertical end of GPO7.	
2Ah (103055h)	**REG103055**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG7_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO7. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_V7END[11:8]	3:0	See description of '103054h'.	
2Bh (103056h)	**REG103056**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H7ST[7:0]	7:0	Horizontal start of GPO7.	
2Bh (103057h)	**REG103057**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG7_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO7.	
	TC_H7ST[11:8]	3:0	See description of '103056h'.	
2Ch (103058h)	**REG103058**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H7END[7:0]	7:0	Horizontal end of GPO7.	
2Ch (103059h)	**REG103059**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG7_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO7. (If set to 2, it means 3 lines toggle once.)	
	TC_H7END[11:8]	3:0	See description of '103058h'.	
2Dh (10305Ah)	**REG10305A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V8ST[7:0]	7:0	Vertical start of GPO8.	
2Dh (10305Bh)	**REG10305B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG8_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO8.	
	TC_V8ST[11:8]	3:0	See description of '10305Ah'.	
2Eh (10305Ch)	**REG10305C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V8END[7:0]	7:0	Vertical end of GPO8.	
2Eh (10305Dh)	**REG10305D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG8_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO8. (If set to 2, it means 3 lines toggle once.)	
	TC_V8END[11:8]	3:0	See description of '10305Ch'.	
2Fh (10305Eh)	**REG10305E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H8ST[7:0]	7:0	Horizontal start of GPO8.	
2Fh (10305Fh)	**REG10305F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG8_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO8.	
	TC_H8ST[11:8]	3:0	See description of '10305Eh'.	
30h (103060h)	**REG103060**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H8END[7:0]	7:0	Horizontal end of GPO8.	
30h (103061h)	**REG103061**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG8_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO8. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_H8END[11:8]	3:0	See description of '103060h'.	
31h (103062h)	**REG103062**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V9ST[7:0]	7:0	Vertical start of GPO9.	
31h (103063h)	**REG103063**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG9_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPO9.	
	TC_V9ST[11:8]	3:0	See description of '103062h'.	
32h (103064h)	**REG103064**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_V9END[7:0]	7:0	Vertical end of GPO9.	
32h (103065h)	**REG103065**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOG9_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPO9. (If set to 2, it means 3 lines toggle once.)	
	TC_V9END[11:8]	3:0	See description of '103064h'.	
33h (103066h)	**REG103066**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H9ST[7:0]	7:0	Horizontal start of GPO9.	
33h (103067h)	**REG103067**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG9_H4[3:0]	7:4	Line tog number MSB 4 bits of GPO9.	
	TC_H9ST[11:8]	3:0	See description of '103066h'.	
34h (103068h)	**REG103068**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H9END[7:0]	7:0	Horizontal end of GPO9.	
34h (103069h)	**REG103069**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOG9_L4[3:0]	7:4	Line tog number LSB 4 bits of GPO9. (If set to 2, it means 3 lines toggle once.)	
	TC_H9END[11:8]	3:0	See description of '103068h'.	
35h (10306Ah)	**REG10306A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_VAST[7:0]	7:0	Vertical start of GPOA.	
35h (10306Bh)	**REG10306B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOGA_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPOA.	
	TC_VAST[11:8]	3:0	See description of '10306Ah'.	
36h (10306Ch)	**REG10306C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_VAEND[7:0]	7:0	Vertical end of GPOA.	
36h (10306Dh)	**REG10306D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOGA_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPOA. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_VAEND[11:8]	3:0	See description of '10306Ch'.	
37h (10306Eh)	**REG10306E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HAST[7:0]	7:0	Horizontal start of GPOA.	
37h (10306Fh)	**REG10306F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOGA_H4[3:0]	7:4	Line tog number MSB 4 bits of GPOA.	
	TC_HAST[11:8]	3:0	See description of '10306Eh'.	
38h (103070h)	**REG103070**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HAEND[7:0]	7:0	Horizontal end of GPOA.	
38h (103071h)	**REG103071**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOGA_L4[3:0]	7:4	Line tog number LSB 4 bits of GPOA. (If set to 2, it means 3 lines toggle once.)	
	TC_HAEND[11:8]	3:0	See description of '103070h'.	
39h (103072h)	**REG103072**	**7:0**	**Default: 0x00**	**Access: R/W**
	G0OP	7	GPO0 Output Polarity. 0: Active high. 1: Active low.	
	G0TC	6	GPO0 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	G0ES	5	GPO0 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	G0TS[1:0]	4:3	GPO0 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G0CS[2:0]	2:0	GPO0 Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
39h (103073h)	**REG103073**	**7:0**	**Default: 0x00**	**Access: R/W**
	G1OP	7	GPO1 Output Polarity. 0: Active high. 1: Active low.	
	G1TC	6	GPO1 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	G1ES	5	GPO1 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	G1TS[1:0]	4:3	GPO1 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G1CS[2:0]	2:0	GPO1 Combination Select. 000: No combination.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Ah (103074h)	**REG103074**	**7:0**	**Default: 0x00**	**Access: R/W**
	G2OP	7	GPO2 Output Polarity. 0: Active high. 1: Active low.	
	G2TC	6	GPO2 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	G2ES	5	GPO2 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	G2TS[1:0]	4:3	GPO2 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G2CS[2:0]	2:0	GPO2 Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Ah	**REG103075**	**7:0**	**Default: 0x00**	**Access: R/W**

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103075h)	G3OP	7	GPO3 Output Polarity. 0: Active high. 1: Active low.	
	G3TC	6	GPO3 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	G3ES	5	GPO3 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	G3TS[1:0]	4:3	GPO3 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G3CS[2:0]	2:0	GPO3 Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Bh (103076h)	**REG103076**	**7:0**	**Default: 0x00**	**Access: R/W**
	G4OP	7	GPO4 Output Polarity. 0: Active high. 1: Active low.	
	G4TC	6	GPO4 Toggle Circuit enable. 0: Normal.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	G4ES	5	GPO4 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	G4TS[1:0]	4:3	GPO4 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G4CS[2:0]	2:0	GPO4 Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Bh (103077h)	**REG103077**	**7:0**	**Default: 0x00**	**Access: R/W**
	G5OP	7	GPO5 Output Polarity. 0: Active high. 1: Active low.	
	G5TC	6	GPO5 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	G5ES	5	GPO5 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	G5TS[1:0]	4:3	GPO5 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G5CS[2:0]	2:0	GPO5 Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Ch (103078h)	**REG103078**	**7:0**	**Default: 0x00**	**Access: R/W**
	G6OP	7	GPO6 Output Polarity. 0: Active high. 1: Active low.	
	G6TC	6	GPO6 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	G6ES	5	GPO6 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Vertical Start position.	
	G6TS[1:0]	4:3	GPO6 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G6CS[2:0]	2:0	GPO6 Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Ch (103079h)	**REG103079**	**7:0**	**Default: 0x00**	**Access: R/W**
	G7OP	7	GPO7 Output Polarity. 0: Active high. 1: Active low.	
	G7TC	6	GPO7 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	G7ES	5	GPO7 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	G7TS[1:0]	4:3	GPO7 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line).	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	G7CS[2:0]	2:0	GPO7 Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Dh (10307Ah)	**REG10307A**	**7:0**	**Default: 0x00**	**Access: R/W**
	G8OP	7	GPO8 Output Polarity. 0: Active high. 1: Active low.	
	G8TC	6	GPO8 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	G8ES	5	GPO8 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	G8TS[1:0]	4:3	GPO8 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)			
Index (Absolute)	**Mnemonic**	**Bit**	**Description**
			10: Two lines toggle. 11: Three lines toggle.
	G8CS[2:0]	2:0	GPO8 Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).
3Dh (10307Bh)	**REG10307B**	**7:0**	**Default: 0x00** **Access: R/W**
	G9OP	7	GPO9 Output Polarity. 0: Active high. 1: Active low.
	G9TC	6	GPO9 Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.
	G9ES	5	GPO9 Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.
	G9TS[1:0]	4:3	GPO9 Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.
	G9CS[2:0]	2:0	GPO9 Combination Select. 000: No combination. 001: AND (GPO& GPO-1).

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Eh (10307Ch)	**REG10307C**	**7:0**	**Default: 0x00**	**Access: R/W**
	GAOP	7	GPOA Output Polarity. 0: Active high. 1: Active low.	
	GATC	6	GPOA Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	GAES	5	GPOA Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	GATS[1:0]	4:3	GPOA Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	GACS[2:0]	2:0	GPOA Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Eh	**REG10307D**	**7:0**	**Default: 0x00**	**Access: R/W**

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10307Dh)	GBOP	7	GPOB Output Polarity. 0: Active high. 1: Active low.	
	GBTC	6	GPOB Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	GBES	5	GPOB Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	GBTS[1:0]	4:3	GPOB Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	GBCS[2:0]	2:0	GPOB Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
3Fh (10307Eh)	**REG10307E**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO5_EN	7	GPO5 enable of POL.	
	GPO4_EN	6	GPO4 enable of POL.	
	GPO3_EN	5	GPO3 enable of POL.	
	GPO2_EN	4	GPO2 enable of POL.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPO1_EN	3	GPO1 enable of POL.	
	GPO0_EN	2	GPO0 enable of POL.	
	-	1:0	Reserved.	
3Fh (10307Fh)	**REG10307F**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPOD_EN	7	GPOD enable of POL.	
	GPOC_EN	6	GPOC enable of POL.	
	GPOB_EN	5	GPOB enable of POL.	
	GPOA_EN	4	GPOA enable of POL.	
	GPO9_EN	3	GPO9 enable of POL.	
	GPO8_EN	2	GPO8 enable of POL.	
	GPO7_EN	1	GPO7 enable of POL.	
	GPO6_EN	0	GPO6 enable of POL.	
40h (103080h)	**REG103080**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_VBST[7:0]	7:0	Vertical start of GPOB.	
40h (103081h)	**REG103081**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOGB_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPOB.	
	TC_VBST[11:8]	3:0	See description of '103080h'.	
41h (103082h)	**REG103082**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_VBEND[7:0]	7:0	Vertical end of GPOB.	
41h (103083h)	**REG103083**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOGB_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPOB. (If set to 2, it means 3 lines toggle once.)	
	TC_VBEND[11:8]	3:0	See description of '103082h'.	
42h (103084h)	**REG103084**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HBST[7:0]	7:0	Horizontal start of GPOB.	
42h (103085h)	**REG103085**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOGB_H4[3:0]	7:4	Line tog number MSB 4 bits of GPOB.	
	TC_HBST[11:8]	3:0	See description of '103084h'.	
43h (103086h)	**REG103086**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HBEND[7:0]	7:0	Horizontal end of GPOB.	
43h (103087h)	**REG103087**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOGB_L4[3:0]	7:4	Line tog number LSB 4 bits of GPOB. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_HBEND[11:8]	3:0	See description of '103086h'.	
44h (103088h)	**REG103088**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_VCST[7:0]	7:0	Vertical start of GPOC.	
44h (103089h)	**REG103089**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOGC_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPOC.	
	TC_VCST[11:8]	3:0	See description of '103088h'.	
45h (10308Ah)	**REG10308A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_VCEND[7:0]	7:0	Vertical end of GPOC.	
45h (10308Bh)	**REG10308B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOGC_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPOC. (If set to 2, it means 3 lines toggle once.)	
	TC_VCEND[11:8]	3:0	See description of '10308Ah'.	
46h (10308Ch)	**REG10308C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HCST[7:0]	7:0	Horizontal start of GPOC.	
46h (10308Dh)	**REG10308D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOGC_H4[3:0]	7:4	Line tog number MSB 4 bits of GPOC.	
	TC_HCST[11:8]	3:0	See description of '10308Ch'.	
47h (10308Eh)	**REG10308E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HCEND[7:0]	7:0	Horizontal end of GPOC.	
47h (10308Fh)	**REG10308F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOGC_L4[3:0]	7:4	Line tog number LSB 4 bits of GPOC. (If set to 2, it means 3 lines toggle once.)	
	TC_HCEND[11:8]	3:0	See description of '10308Eh'.	
48h (103090h)	**REG103090**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_VDST[7:0]	7:0	Vertical start of GPOD.	
48h (103091h)	**REG103091**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOGD_H4[3:0]	7:4	Frame tog number MSB 4 bits of GPOD.	
	TC_VDST[11:8]	3:0	See description of '103090h'.	
49h (103092h)	**REG103092**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_VDEND[7:0]	7:0	Vertical end of GPOD.	
49h (103093h)	**REG103093**	**7:0**	**Default: 0x0F**	**Access: R/W**
	FRAME_TOGD_L4[3:0]	7:4	Frame tog number LSB 4 bits of GPOD. (If set to 2, it means 3 lines toggle once.)	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_VDEND[11:8]	3:0	See description of '103092h'.	
4Ah (103094h)	**REG103094**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HDST[7:0]	7:0	Horizontal start of GPOD.	
4Ah (103095h)	**REG103095**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOGD_H4[3:0]	7:4	Line tog number MSB 4 bits of GPOD.	
	TC_HDST[11:8]	3:0	See description of '103094h'.	
4Bh (103096h)	**REG103096**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HDEND[7:0]	7:0	Horizontal end of GPOD.	
4Bh (103097h)	**REG103097**	**7:0**	**Default: 0x0F**	**Access: R/W**
	LINE_TOGD_L4[3:0]	7:4	Line tog number LSB 4 bits of GPOD. (If set to 2, it means 3 lines toggle once.)	
	TC_HDEND[11:8]	3:0	See description of '103096h'.	
4Ch (103098h)	**REG103098**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H1ST2[7:0]	7:0	2nd horizontal start of GPO1.	
4Ch (103099h)	**REG103099**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO0_PS[3:0]	7:4	Frame count for power sequence of GPO0. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H1ST2[11:8]	3:0	See description of '103098h'.	
4Dh (10309Ah)	**REG10309A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H1ST3[7:0]	7:0	3rd horizontal start of GPO1.	
4Dh (10309Bh)	**REG10309B**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO1_PS[3:0]	7:4	Frame count for power sequence of GPO1. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H1ST3[11:8]	3:0	See description of '10309Ah'.	
4Eh (10309Ch)	**REG10309C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H1END3[7:0]	7:0	3rd horizontal end of GPO1.	
4Eh (10309Dh)	**REG10309D**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO2_PS[3:0]	7:4	Frame count for power sequence of GPO2. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H1END3[11:8]	3:0	See description of '10309Ch'.	
4Fh (10309Eh)	**REG10309E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H2ST2[7:0]	7:0	2nd horizontal start of GPO2.	
4Fh (10309Fh)	**REG10309F**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO3_PS[3:0]	7:4	Frame count for power sequence of GPO3.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Only active with Frame counter enable (EN_FCNT=1).	
	TC_H2ST2[11:8]	3:0	See description of '10309Eh'.	
50h (1030A0h)	**REG1030A0**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H2ST3[7:0]	7:0	3rd horizontal start of GPO2.	
50h (1030A1h)	**REG1030A1**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO4_PS[3:0]	7:4	Frame count for power sequence of GPO4. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H2ST3[11:8]	3:0	See description of '1030A0h'.	
51h (1030A2h)	**REG1030A2**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H2END3[7:0]	7:0	3rd horizontal end of GPO2.	
51h (1030A3h)	**REG1030A3**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO5_PS[3:0]	7:4	Frame count for power sequence of GPO5. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H2END3[11:8]	3:0	See description of '1030A2h'.	
52h (1030A4h)	**REG1030A4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H3ST2[7:0]	7:0	2nd horizontal start of GPO3.	
52h (1030A5h)	**REG1030A5**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPOB_PS[3:0]	7:4	Frame count for power sequence of GPOb. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H3ST2[11:8]	3:0	See description of '1030A4h'.	
53h (1030A6h)	**REG1030A6**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H3ST3[7:0]	7:0	3rd horizontal start of GPO3.	
53h (1030A7h)	**REG1030A7**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPOC_PS[3:0]	7:4	Frame count for power sequence of GPOc. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H3ST3[11:8]	3:0	See description of '1030A6h'.	
54h (1030A8h)	**REG1030A8**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H3END3[7:0]	7:0	3rd horizontal end of GPO3.	
54h (1030A9h)	**REG1030A9**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPOD_PS[3:0]	7:4	Frame count for power sequence of GPOd. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H3END3[11:8]	3:0	See description of '1030A8h'.	
55h (1030AAh)	**REG1030AA**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H4ST2[7:0]	7:0	2nd horizontal start of GPO4.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
55h (1030ABh)	**REG1030AB**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_H4ST2[11:8]	3:0	See description of '1030AAh'.	
56h (1030ACh)	**REG1030AC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H4ST3[7:0]	7:0	3rd horizontal start of GPO4.	
56h (1030ADh)	**REG1030AD**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_H4ST3[11:8]	3:0	See description of '1030ACh'.	
57h (1030AEh)	**REG1030AE**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H4END3[7:0]	7:0	3rd horizontal end of GPO4.	
57h (1030AFh)	**REG1030AF**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_H4END3[11:8]	3:0	See description of '1030AEh'.	
58h (1030B0h)	**REG1030B0**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H5ST2[7:0]	7:0	2nd horizontal start of GPO5.	
58h (1030B1h)	**REG1030B1**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_H5ST2[11:8]	3:0	See description of '1030B0h'.	
59h (1030B2h)	**REG1030B2**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H5ST3[7:0]	7:0	3rd horizontal start of GPO5.	
59h (1030B3h)	**REG1030B3**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_H5ST3[11:8]	3:0	See description of '1030B2h'.	
5Ah (1030B4h)	**REG1030B4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H5END3[7:0]	7:0	3rd horizontal end of GPO5.	
5Ah (1030B5h)	**REG1030B5**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_H5END3[11:8]	3:0	See description of '1030B4h'.	
5Bh (1030B6h)	**REG1030B6**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H9ST2[7:0]	7:0	2nd horizontal start of GPO9.	
5Bh (1030B7h)	**REG1030B7**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO6_PS[3:0]	7:4	Frame count for power sequence of GPO6. Only active with Frame counter enable (EN_FCNT=1).	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TC_H9ST2[11:8]	3:0	See description of '1030B6h'.	
5Ch (1030B8h)	**REG1030B8**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H9ST3[7:0]	7:0	3rd horizontal start of GPO9.	
5Ch (1030B9h)	**REG1030B9**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO7_PS[3:0]	7:4	Frame count for power sequence of GPO7. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H9ST3[11:8]	3:0	See description of '1030B8h'.	
5Dh (1030BAh)	**REG1030BA**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_H9END3[7:0]	7:0	3rd horizontal end of GPO9.	
5Dh (1030BBh)	**REG1030BB**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO8_PS[3:0]	7:4	Frame count for power sequence of GPO8. Only active with Frame counter enable (EN_FCNT=1).	
	TC_H9END3[11:8]	3:0	See description of '1030BAh'.	
5Eh (1030BCh)	**REG1030BC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HAST2[7:0]	7:0	2nd horizontal start of GPOA.	
5Eh (1030BDh)	**REG1030BD**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPO9_PS[3:0]	7:4	Frame count for power sequence of GPO9. Only active with Frame counter enable (EN_FCNT=1).	
	TC_HAST2[11:8]	3:0	See description of '1030BCh'.	
5Fh (1030BEh)	**REG1030BE**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HAST3[7:0]	7:0	3rd horizontal start of GPOA.	
5Fh (1030BFh)	**REG1030BF**	**7:0**	**Default: 0xFF**	**Access: R/W**
	GPOA_PS[3:0]	7:4	Frame count for power sequence of GPOa. Only active with Frame counter enable (EN_FCNT=1).	
	TC_HAST3[11:8]	3:0	See description of '1030BEh'.	
60h (1030C0h)	**REG1030C0**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HAEND3[7:0]	7:0	3rd horizontal end of GPOA.	
60h (1030C1h)	**REG1030C1**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_HAEND3[11:8]	3:0	See description of '1030C0h'.	
61h (1030C2h)	**REG1030C2**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO7_FF_OEN	7	GPO7_FF output enable.	
	GPO6_FF_OEN	6	GPO6_FF output enable.	
	GPO5_FF_OEN	5	GPO5_FF output enable.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPO4_FF_OEN	4	GPO4_FF output enable.	
	GPO3_FF_OEN	3	GPO3_FF output enable.	
	GPO2_FF_OEN	2	GPO2_FF output enable.	
	GPO1_FF_OEN	1	GPO1_FF output enable.	
	GPO0_FF_OEN	0	GPO0_FF output enable.	
61h (1030C3h)	**REG1030C3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GPOD_FF_OEN	5	GPOD_FF output enable.	
	GPOC_FF_OEN	4	GPOC_FF output enable.	
	GPOB_FF_OEN	3	GPOB_FF output enable.	
	GPOA_FF_OEN	2	GPOA_FF output enable.	
	GPO9_FF_OEN	1	GPO9_FF output enable.	
	GPO8_FF_OEN	0	GPO8_FF output enable.	
62h ~ 69h (1030C4h ~ 1030D3h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
6Ah (1030D4h)	**REG1030D4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HBST2[7:0]	7:0	2nd horizontal start of GPOB.	
6Ah (1030D5h)	**REG1030D5**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_HBST2[11:8]	3:0	See description of '1030D4h'.	
6Bh (1030D6h)	**REG1030D6**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HBST3[7:0]	7:0	3rd horizontal start of GPOB.	
6Bh (1030D7h)	**REG1030D7**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_HBST3[11:8]	3:0	See description of '1030D6h'.	
6Ch (1030D8h)	**REG1030D8**	**7:0**	**Default: 0xFF**	**Access: R/W**
	TC_HBEND3[7:0]	7:0	3rd horizontal end of GPOB.	
6Ch (1030D9h)	**REG1030D9**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	TC_HBEND3[11:8]	3:0	See description of '1030D8h'.	
6Dh (1030DAh)	**REG1030DA**	**7:0**	**Default: 0x00**	**Access: R/W**
	GCOP	7	GPOC Output Polarity.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Active high. 1: Active low.	
	GCTC	6	GPOC Toggle Circuit enable. 0: Normal. 1: Toggle. Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	GCES	5	GPOC Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	GCTS[1:0]	4:3	GPOC Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	GCCS[2:0]	2:0	GPOC Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
6Dh (1030DBh)	**REG1030DB**	**7:0**	**Default: 0x00**	**Access: R/W**
	GDOP	7	GPOD Output Polarity. 0: Active high. 1: Active low.	
	GDTC	6	GPOD Toggle Circuit enable. 0: Normal. 1: Toggle.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Toggle mode is useful in POL generation when alternating polarity is required from line to line. Frame to frame polarity changes are made by programming an odd in the vertical duration when in toggle mode.	
	GDES	5	GPOD Early Start function. 0: Normal. 1: Early start capability. The value in the Vertical Start Register (G0VST) is subtracted from the total number of lines/frames to determine the Vertical Start position.	
	GDTS[1:0]	4:3	GPOD Type Select. When toggle mode=0: 00: Normal. 01: Duration is greater than a line time (over1line). 10: Every two lines have one GPO pulse (skip1line). 11: Every three lines have one GPO pulse (skip2line). When toggle mode=1: 00: One line toggle. 01: Reserved. 10: Two lines toggle. 11: Three lines toggle.	
	GDCS[2:0]	2:0	GPOD Combination Select. 000: No combination. 001: AND (GPO& GPO-1). 010: OR (GPO| GPO-1). 011: Select GPO and GPO-1 on alternating frames. 1xx: XOR (GPO^ GPO-1).	
6Eh (1030DCh)	**REG1030DC**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO7_N_1_SEL	7	Select the signal which is used for GPO7 Combination Select (G7CS). (GPO7 n 1 select). 0: Use GPO6. 1: Use an always Low signal(0).	
	GPO6_N_1_SEL	6	Select the signal which is used for GPO6 Combination Select (G6CS). (GPO6 n 1 select). 0: Use GPO5. 1: Use an always Low signal(0).	
	GPO5_N_1_SEL	5	Select the signal which is used for GPO5 Combination Select	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			(G5CS). (GPO5 n 1 select). 0: Use GPO4. 1: Use an always Low signal(0).	
	GPO4_N_1_SEL	4	Select the signal which is used for GPO4 Combination Select (G4CS). (GPO4 n 1 select). 0: Use GPO3. 1: Use an always Low signal(0).	
	GPO3_N_1_SEL	3	Select the signal which is used for GPO3 Combination Select (G3CS). (GPO3 n 1 select). 0: Use GPO2. 1: Use an always Low signal(0).	
	GPO2_N_1_SEL	2	Select the signal which is used for GPO2 Combination Select (G2CS). (GPO2 n 1 select). 0: Use GPO1. 1: Use an always Low signal(0).	
	GPO1_N_1_SEL	1	Select the signal which is used for GPO1 Combination Select (G1CS). (GPO1 n 1 select). 0: Use GPO0. 1: Use an always Low signal(0).	
	GPO0_N_1_SEL	0	Select the signal which is used for GPO0 Combination Select (G0CS). (GPO0 n 1 select). 0: Use GPOD. 1: Use an always Low signal(0).	
6Eh (1030DDh)	**REG1030DD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GPOD_N_1_SEL	5	Select the signal which is used for GPOD Combination Select (GDCS). (GPOD n 1 select). 0: Use GPOC. 1: Use an always Low signal(0).	
	GPOC_N_1_SEL	4	Select the signal which is used for GPOC Combination Select (GCCS).	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			(GPOC n 1 select). 0: Use GPOB. 1: Use an always Low signal(0).	
	GPOB_N_1_SEL	3	Select the signal which is used for GPOB Combination Select (GBCS). (GPOB n 1 select). 0: Use GPOA. 1: Use an always Low signal(0).	
	GPOA_N_1_SEL	2	Select the signal which is used for GPOA Combination Select (GACS). (GPOA n 1 select). 0: Use GPO9. 1: Use an always Low signal(0).	
	GPO9_N_1_SEL	1	Select the signal which is used for GPO9 Combination Select (G9CS). (GPO9 n 1 select). 0: Use GPO8. 1: Use an always Low signal(0).	
	GPO8_N_1_SEL	0	Select the signal which is used for GPO8 Combination Select (G8CS). (GPO8 n 1 select). 0: Use GPO7. 1: Use an always Low signal(0).	
6Fh (1030DEh)	**REG1030DE**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO3_EN_3HV[1:0]	7:6	GPO3 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO2_EN_3HV[1:0]	5:4	GPO2 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO1_EN_3HV[1:0]	3:2	GPO1 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO0_EN_3HV[1:0]	1:0	GPO0 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
6Fh (1030DFh)	**REG1030DF**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO7_EN_3HV[1:0]	7:6	GPO7 3hv enable.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO6_EN_3HV[1:0]	5:4	GPO6 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO5_EN_3HV[1:0]	3:2	GPO5 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO4_EN_3HV[1:0]	1:0	GPO4 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
70h (1030E0h)	**REG1030E0**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPOB_EN_3HV[1:0]	7:6	GPOB 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPOA_EN_3HV[1:0]	5:4	GPOA 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO9_EN_3HV[1:0]	3:2	GPO9 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPO8_EN_3HV[1:0]	1:0	GPO8 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
70h (1030E1h)	**REG1030E1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	GPOD_EN_3HV[1:0]	3:2	GPOD 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
	GPOC_EN_3HV[1:0]	1:0	GPOC 3hv enable. Bit[0]: Enable 2nd hv. Bit[1]: Enable 3rd hv.	
71h (1030E2h)	**REG1030E2**	**7:0**	**Default: 0x00**	**Access: R/W**
	FRAME_TOG7_MD	7	GPO7 frame toggle mode enable.	
	FRAME_TOG6_MD	6	GPO6 frame toggle mode enable.	
	FRAME_TOG5_MD	5	GPO5 frame toggle mode enable.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	FRAME_TOG4_MD	4	GPO4 frame toggle mode enable.	
	FRAME_TOG3_MD	3	GPO3 frame toggle mode enable.	
	FRAME_TOG2_MD	2	GPO2 frame toggle mode enable.	
	FRAME_TOG1_MD	1	GPO1 frame toggle mode enable.	
	FRAME_TOG0_MD	0	GPO0 frame toggle mode enable.	
71h (1030E3h)	**REG1030E3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FRAME_TOGD_MD	5	GPOD frame toggle mode enable.	
	FRAME_TOGC_MD	4	GPOC frame toggle mode enable.	
	FRAME_TOGB_MD	3	GPOB frame toggle mode enable.	
	FRAME_TOGA_MD	2	GPOA frame toggle mode enable.	
	FRAME_TOG9_MD	1	GPO9 frame toggle mode enable.	
	FRAME_TOG8_MD	0	GPO8 frame toggle mode enable.	
72h (1030E4h)	**REG1030E4**	**7:0**	**Default: 0x00**	**Access: R/W**
	LINE_TOG7_MD	7	GPO7 line toggle mode enable.	
	LINE_TOG6_MD	6	GPO6 line toggle mode enable.	
	LINE_TOG5_MD	5	GPO5 line toggle mode enable.	
	LINE_TOG4_MD	4	GPO4 line toggle mode enable.	
	LINE_TOG3_MD	3	GPO3 line toggle mode enable.	
	LINE_TOG2_MD	2	GPO2 line toggle mode enable.	
	LINE_TOG1_MD	1	GPO1 line toggle mode enable.	
	LINE_TOG0_MD	0	GPO0 line toggle mode enable.	
72h (1030E5h)	**REG1030E5**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	LINE_TOGD_MD	5	GPOD line toggle mode enable.	
	LINE_TOGC_MD	4	GPOC line toggle mode enable.	
	LINE_TOGB_MD	3	GPOB line toggle mode enable.	
	LINE_TOGA_MD	2	GPOA line toggle mode enable.	
	LINE_TOG9_MD	1	GPO9 line toggle mode enable.	
	LINE_TOG8_MD	0	GPO8 line toggle mode enable.	
73h (1030E6h)	**REG1030E6**	**7:0**	**Default: 0x00**	**Access: R/W**
	FIRST_2H7_MD	7	GPO7 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			line).	
	FIRST_2H6_MD	6	GPO6 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H5_MD	5	GPO5 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H4_MD	4	GPO4 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H3_MD	3	GPO3 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H2_MD	2	GPO2 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H1_MD	1	GPO1 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H0_MD	0	GPO0 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
73h (1030E7h)	**REG1030E7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	FIRST_2HD_MD	5	GPOD first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2HC_MD	4	GPOC first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2HB_MD	3	GPOB first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2HA_MD	2	GPOA first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H9_MD	1	GPO9 first 2H mode enable.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			(An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
	FIRST_2H8_MD	0	GPO8 first 2H mode enable. (An n-Line toggle TCON signal needs (n-1)-line toggle at first line).	
74h (1030E8h)	**REG1030E8**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO7_PUA	7	GPO7 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO6_PUA	6	GPO6 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO5_PUA	5	GPO5 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO4_PUA	4	GPO4Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO3_PUA	3	GPO3 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO2_PUA	2	GPO2 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO1_PUA	1	GPO1 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO0_PUA	0	GPO0 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
74h (1030E9h)	**REG1030E9**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GPOD_PUA	5	GPOD Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPOC_PUA	4	GPOC Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPOB_PUA	3	GPOB Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPOA_PUA	2	GPOA Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO9_PUA	1	GPO9 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
	GPO8_PUA	0	GPO8 Power-up Active. Only active when SEP_PUA=1. 0: Outputs inactive. 1: Outputs active.	
75h (1030EAh)	**REG1030EA**	**7:0**	**Default: 0x40**	**Access: R/W**
	FLK_OPTION	7	1: Enable FLK option "FLK13 = FLK13 & FLK24, FLK24 keep low". 0: No change for FLK13, FLK24.	
	EN_POL_SEL	6	Enable POL_SEL from LG block.	
	TCON_TYPE[2:0]	5:3	TCON type. 0: Normal. 1: LTD. 2: GIP.	
	TCON_GRP2_CLK_GATE_EN	2	Enable CLK gate of TCON group 2 (GPO9~GPOD).	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	TCON_GRP1_CLK_GATE_EN	1	Enable CLK gate of TCON group 1 (GPO7~GPO8).	
	TCON_GRP0_CLK_GATE_EN	0	Enable CLK gate of TCON group 0 (GPO0~GPO6).	
75h (1030EBh)	**REG1030EB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	ICLK_RESET_OPTION	4	1: Enable ICLK_RESET option with 2 pulse (GPO9 | GPOA). 0: No change for ICLK_RESET (only use GPO9).	
	ICLK4_OPTION	3	1: Enable ICLK option "ICLK4 = ICLK4 | ICLK_RESET". 0: No change for ICLK4.	
	ICLK3_OPTION	2	1: Enable ICLK option "ICLK3 = ICLK3 | ICLK_RESET". 0: No change for ICLK3.	
	ICLK2_OPTION	1	1: Enable ICLK option "ICLK2 = ICLK2 | ICLK_RESET". 0: No change for ICLK2.	
	ICLK1_OPTION	0	1: Enable ICLK option "ICLK1: ICLK1 | ICLK_RESET". 0: No change for ICLK1.	
76h (1030ECh)	**REG1030EC**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO3_STH_SEL[1:0]	7:6	GPO3 STH pulse width select.	
	GPO2_STH_SEL[1:0]	5:4	GPO2 STH pulse width select.	
	GPO1_STH_SEL[1:0]	3:2	GPO1 STH pulse width select.	
	GPO0_STH_SEL[1:0]	1:0	GPO0 STH pulse width select. 00: 1T positive clock sample (GPO_POS). 01: 1T negative clock sample (GPO_NEG). 10: 1.5T positive clock sample (GPO_POS | GPO_NEG). 11: 1.5T negative clock sample (GPO_NEG | GPO_2ND).	
76h (1030EDh)	**REG1030ED**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO7_STH_SEL[1:0]	7:6	GPO7 STH pulse width select.	
	GPO6_STH_SEL[1:0]	5:4	GPO6 STH pulse width select.	
	GPO5_STH_SEL[1:0]	3:2	GPO5 STH pulse width select.	
	GPO4_STH_SEL[1:0]	1:0	GPO4 STH pulse width select.	
77h (1030EEh)	**REG1030EE**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPOB_STH_SEL[1:0]	7:6	GPOb STH pulse width select.	
	GPOA_STH_SEL[1:0]	5:4	GPOa STH pulse width select.	
	GPO9_STH_SEL[1:0]	3:2	GPO9 STH pulse width select.	
	GPO8_STH_SEL[1:0]	1:0	GPO8 STH pulse width select.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
77h (1030EFh)	**REG1030EF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	GPOD_STH_SEL[1:0]	3:2	GPOd STH pulse width select.	
	GPOC_STH_SEL[1:0]	1:0	GPOc STH pulse width select.	
78h (1030F0h)	**REG1030F0**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO7_TAIL_MINUS1_MD	7	GPO7 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO6_TAIL_MINUS1_MD	6	GPO6 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO5_TAIL_MINUS1_MD	5	GPO5 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO4_TAIL_MINUS1_MD	4	GPO4 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO3_TAIL_MINUS1_MD	3	GPO3 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO2_TAIL_MINUS1_MD	2	GPO2 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO1_TAIL_MINUS1_MD	1	GPO1 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO0_TAIL_MINUS1_MD	0	GPO0 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
78h (1030F1h)	**REG1030F1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GPOD_TAIL_MINUS1_MD	5	GPOD tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPOC_TAIL_MINUS1_MD	4	GPOC tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPOB_TAIL_MINUS1_MD	3	GPOB tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPOA_TAIL_MINUS1_MD	2	GPOA tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO9_TAIL_MINUS1_MD	1	GPO9 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
	GPO8_TAIL_MINUS1_MD	0	GPO8 tail minus 1H mode enable. (An n-Line toggle TCON signal need (n-1)-line toggle at last line).	
79h (1030F2h)	**REG1030F2**	**7:0**	**Default: 0x00**	**Access: R/W**
	G7AT	7	GPO7 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G6AT	6	GPO6 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G5AT	5	GPO5 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G4AT	4	GPO4 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G3AT	3	GPO3 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G2AT	2	GPO2 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G1AT	1	GPO1 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G0AT	0	GPO0 Auto Toggle for POL. 0: Disable. 1: Enable.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
79h (1030F3h)	**REG1030F3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GDAT	5	GPOD Auto Toggle for POL. 0: Disable. 1: Enable.	
	GCAT	4	GPOC Auto Toggle for POL. 0: Disable. 1: Enable.	
	GBAT	3	GPOB Auto Toggle for POL. 0: Disable. 1: Enable.	
	GAAT	2	GPOA Auto Toggle for POL. 0: Disable. 1: Enable.	
	G9AT	1	GPO9 Auto Toggle for POL. 0: Disable. 1: Enable.	
	G8AT	0	GPO8 Auto Toggle for POL. 0: Disable. 1: Enable.	
7Ah (1030F4h)	**REG1030F4**	**7:0**	**Default: 0x00**	**Access: R/W**
	MINI_GPO_OEN[7:0]	7:0	GPO OEN of mini-LVDS.	
7Ah (1030F5h)	**REG1030F5**	**7:0**	**Default: 0x00**	**Access: R/W**
	MINI_GPO[7:0]	7:0	GPO of mini -LVDS.	
7Bh (1030F6h)	**REG1030F6**	**7:0**	**Default: 0x00**	**Access: R/W**
	POL_INV_2[7:0]	7:0	POL inversion registers set2.	
7Bh (1030F7h)	**REG1030F7**	**7:0**	**Default: 0x00**	**Access: R/W**
	POL_INV_1[7:0]	7:0	POL inversion registers set1.	
7Ch (1030F8h)	**REG1030F8**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_SET_HIGH[7:0]	7:0	0: Keep original GPO value. 1: Set GPO value HIGH when at GPO mask mode. (GPO_SET_LOW priority is higher than GPO_SET_HIGH).	
7Ch (1030F9h)	**REG1030F9**	**7:0**	**Default: 0x00**	**Access: R/W**
	SW_GPO_RECOVER	7	Recover GPO from mask when GPO_MASK_SEL=0 and GPO_MASK_MODE=0.	
	GPO_MASK_SEL	6	Select GPO mask mode.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Mask GPO output when input VSYNC or HSYNC change. 1: Mask GPO output when the detected frame count doesn't achieve GPO hardware recover frame count (GPO_RECOVER_FRAME[3:0]).	
	GPO_SET_HIGH[13:8]	5:0	See description of '1030F8h'.	
7Dh (1030FAh)	**REG1030FA**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_SET_LOW[7:0]	7:0	0: Keep original GPO value. 1: Set GPO value LOW when at GPO mask mode. (GPO_SET_LOW priority is higher than GPO_SET_HIGH).	
7Dh (1030FBh)	**REG1030FB**	**7:0**	**Default: 0x00**	**Access: R/W**
	INT1_TCON_EN	7	1: Enable VSYNC change mask for TCON.	
	INT2_TCON_EN	6	1: Enable HSYNC change mask for TCON.	
	GPO_SET_LOW[13:8]	5:0	See description of '1030FAh'.	
7Eh (1030FCh)	**REG1030FC**	**7:0**	**Default: 0xE4**	**Access: R/W**
	ICLK_MUX[7:0]	7:0	ICLK mux select. 00: Select to ICLK1. 01: Select to ICLK2. 10: Select to ICLK2. 11: Select to ICLK3. Bit[1:0] ICLK1 select. Bit[3:2] ICLK2 select. Bit[5:4] ICLK3 select. Bit[7:6] ICLK4 select.	
7Eh (1030FDh)	**REG1030FD**	**7:0**	**Default: 0xF0**	**Access: R/W**
	GPO_RECOVER_FRAME[3:0]	7:4	Set GPO hardware recover frame count.	
	GPO_MASK_MODE	3	GPO mask mode select 2.	
	-	2	Reserved.	
	INT3_TCON_EN	1	Enable interrupt3 for TCON.	
	INT4_TCON_EN	0	Enable interrupt4 for TCON.	
7Fh (1030FEh)	**REG1030FE**	**7:0**	**Default: 0x00**	**Access: R/W**
	TC_DUMMY0[7:0]	7:0	TCON dummy register 0. Bit[0]: Enable or disable POL 2 line special mode. Odd frame is 2H mode, and even frame is normal mode. 0: Disable. 1: Enable.	

DISP_TC Register (Bank = 1030, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Bit[1]: Enable or disable POL frame toggle mode. 0: Disable. 1: Enable.	
7Fh (1030FFh)	**REG1030FF**	**7:0**	**Default: 0x00**	**Access: R/W**
	TC_DUMMY0[15:8]	7:0	See description of '1030FEh'.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h (103002h)	**REG103002**	**7:0**	**Default: 0xFF**	**Access: R/W**
	VMDEST[7:0]	7:0	Regenerate VMDEST start point.	
01h (103003h)	**REG103003**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	VMDEST[11:8]	3:0	See description of '103002h'.	
02h (103004h)	**REG103004**	**7:0**	**Default: 0xFF**	**Access: R/W**
	HMDEST[7:0]	7:0	Regenerate 1st HMDEST start point.	
02h (103005h)	**REG103005**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	HMDEST[11:8]	3:0	See description of '103004h'.	
03h (103006h)	**REG103006**	**7:0**	**Default: 0xFF**	**Access: R/W**
	HMDEST2[7:0]	7:0	Regenerate 2nd HMDEST start point. Its setting value should follow the rule below. DRD case: HMDEST2 - HMDEST == htotal/2. TRD case: HMDEST2 - HMDEST == htotal/3. Others: HMDEST2 == HMDEST.	
03h (103007h)	**REG103007**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	HMDEST2[11:8]	3:0	See description of '103006h'.	
04h (103008h)	**REG103008**	**7:0**	**Default: 0xFF**	**Access: R/W**
	HMDEST3[7:0]	7:0	Regenerate 3rd HMDEST start point. Its setting value should follow the rule below. TRD case: HMDEST3 - HMDEST2 == htotal/3. Others: HMDEST3 == HMDEST.	
04h (103009h)	**REG103009**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	HMDEST3[11:8]	3:0	See description of '103008h'.	
05h (10300Ah)	**REG10300A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	HMDEACT[7:0]	7:0	Regenerate HMDE DE width. DRD case: HMDEACT == (HORIZONTAL_DISPLAY_RESOLUTION)/2. TRD case: HMDEACT == (HORIZONTAL_DISPLAY_RESOLUTION)/3. Others: HMDEACT ==	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			(HORIZONTAL_DISPLAY_RESOLUTION).	
05h (10300Bh)	**REG10300B**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	HMDEACT[11:8]	3:0	See description of '10300Ah'.	
06h (10300Ch)	**REG10300C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	HSPRE[7:0]	7:0	Horizontal sync offset before HMDEST by pixel unit.	
07h (10300Eh)	**REG10300E**	**7:0**	**Default: 0x00**	**Access: R/W**
	RD_INV[1:0]	7:6	LB read address reverse enable.	
	WR_A1	5	LB write cycle add 1 when write finish.	
	-	4	Reserved.	
	LB_BANK_SWAP[1:0]	3:2	LB read bank swap. (High-bank (Bit[35:18]) and Low-bank (Bit[17:0]) swap). Bit[0]: For line buffer 0 (L-channel). Bit[1]: For line buffer 1 (R-channel).	
	LB_BYTE_SWAP[1:0]	1:0	LB read byte ml swap. (Byte5~Byte0 swap). Bit[0]: For line buffer 0 (L-channel). Bit[1]: For line buffer 1 (R-channel).	
07h (10300Fh)	**REG10300F**	**7:0**	**Default: 0x00**	**Access: R/W**
	COUT_TYPE	7	Output single/dual mode select. 1: Single mode. 0: Dual mode.	
	BYTE_SHIFT[2:0]	6:4	LB output data byte shift number.	
	OTYPE_SEL[3:0]	3:0	Output data type select. [0]: Normal - no-LB. [1]: 1G output LB. [2]: 2G output LB (DRD). [3]: 3G output LB (TRD).	
08h (103010h)	**REG103010**	**7:0**	**Default: 0xFF**	**Access: R/W**
	BANK_LEN[7:0]	7:0	LB read bank offset.	
08h (103011h)	**REG103011**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:2	Reserved.	
	BANK_LEN[9:8]	1:0	See description of '103010h'.	
09h (103012h)	**REG103012**	**7:0**	**Default: 0x00**	**Access: R/W**
	RADDR_OFFSET[7:0]	7:0	LB read line address offset.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
09h (103013h)	**REG103013**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	RADDR_OFFSET[9:8]	1:0	See description of '103012h'.	
0Ah (103014h)	**REG103014**	**7:0**	**Default: 0x00**	**Access: R/W**
	LB_PAIR_SWAP_F[7:0]	7:0	First bank LB read byte even/odd swap. Bit[0]: For Byte1 and Byte0 swap. Bit[1]: For Byte3 and Byte2 swap. Bit[2]: For Byte5 and Byte4 swap. Bit[8:3]: Reserved.	
0Ah (103015h)	**REG103015**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	LB_PAIR_SWAP_F[8]	0	See description of '103014h'.	
0Bh (103016h)	**REG103016**	**7:0**	**Default: 0x00**	**Access: R/W**
	LB_PAIR_SWAP_S[7:0]	7:0	Second bank LB read byte even/odd swap. Bit[0]: For Byte1 and Byte0 swap. Bit[1]: For Byte3 and Byte2 swap. Bit[2]: For Byte5 and Byte4 swap. Bit[8:3]: Reserved.	
0Bh (103017h)	**REG103017**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	LB_PAIR_SWAP_S[8]	0	See description of '103016h'.	
0Ch (103018h)	**REG103018**	**7:0**	**Default: 0x00**	**Access: R/W**
	LB_GRAY_LEVEL[7:0]	7:0	Force line buffer output value in vertical blanking. Only active with LB_GRAY_EN=1.	
0Ch (103019h)	**REG103019**	**7:0**	**Default: 0x00**	**Access: R/W**
	LB_GRAY_EN	7	Enable line buffer control force value which is determined by register LB_GRAY_LEVEL in vertical blanking.	
	-	6:0	Reserved.	
0Dh (10301Ah)	**REG10301A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	LB_RD_DLY[4:0]	4:0	LB read delay to match REG_DE_DELAY.	
0Dh (10301Bh)	**REG10301B**	**7:0**	**Default: 0x00**	**Access: R/W**
	LB_SRAM_CTRL[3:0]	7:4	Line buffer SRAM control no used.	
	LB_DE_BLANK_EN	3	Enable line buffer de toggle in vblanking.	
	BYTE_SHIFT_FORCE	2	Force both byte shift in LB write for First and Second bank.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Byte shift number is determined by register BYTE_SHIFT.	
	-	1	Reserved.	
	CHANNEL_MAX_3	0	LB read delay to match REG_DE_DELAY.	
0Eh (10301Ch)	**REG10301C**	**7:0**	**Default: 0x00**	**Access: R/W**
	FIFO_DE_LEN[7:0]	7:0	FIFO data valid length.	
0Eh (10301Dh)	**REG10301D**	**7:0**	**Default: 0x00**	**Access: R/W**
	RDY_FCNT[3:0]	7:4	Ready frame counter for display.	
	FIFO_DE_LEN[11:8]	3:0	See description of '10301Ch'.	
0Fh (10301Eh)	**REG10301E**	**7:0**	**Default: 0x00**	**Access: R/W**
	ODATA_STH_SEL	7	Select STH signal for Mini-LVDS reset pulse of ODATA. 0: GPO8. 1: GPO6.	
	CONT_DE_SEL	6	1: Select continue de as HMDE.	
	RST_ON_DEST	5	Mini-LVDS reset pulse insert delay select. The delay unit is Mini-FIFO clock. Only active with MINI_DM_EN=1.	
	-	4	Reserved.	
	MINI_DM_SEL[3:0]	3:0	Mini-LVDS reset pulse insert delay select.	
0Fh (10301Fh)	**REG10301F**	**7:0**	**Default: 0x08**	**Access: R/W**
	MINILVDS_EN	7	1: Mini-LVDS enable.	
	BIT_FLAG	6	Mini-LVDS bit flag. 1: 8-bit mode. 0: 6-bit mode.	
	TP_RST_EN	5	1: Using signal TP (SOE) rising edge to reset mini-FIFO DE.	
	MINI_DM_EN	4	1: Enable mini-LVDS reset pulse insert delay, use STH to control reset pulse.	
	NO_SIGNAL_EN	3	Enable no-signal SRAM mask.	
	CHANNEL_MAX[2:0]	2:0	Channel number of mini-LVDS.	
10h (103020h)	**REG103020**	**7:0**	**Default: 0x00**	**Access: R/W**
	TMINI_RST_ON[7:0]	7:0	LSB bit of timing TP1 (SOE) to reset on.	
10h (103021h)	**REG103021**	**7:0**	**Default: 0x00**	**Access: R/W**
	TMINI_RST_OFF[3:0]	7:4	Timing TP1 (SOE) to reset off.	
	DE_DELAY[3:0]	3:0	Data valid delay.	
11h	**REG103022**	**7:0**	**Default: 0x00**	**Access: R/W**

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103022h)	SWAP_CHANNEL_R	7	Mini-LVDS R channel swap. (CH5~CH0 --> CH0~CH5).	
	SWAP_CHANNEL_L	6	Mini-LVDS L channel swap. (CH5~CH0 --> CH0~CH5).	
	IVMD	5	Blanking data set value. Only active with IVMD_EN=1.	
	IVMD_EN	4	Blanking data set enable.	
	DREV	3	RSDS output data inverse.	
	EN_FCNT	2	Enable frame counter.	
	VCNT_RESET_SEL	1	TCON v counter reset by. 0: VOP2_VS. 1: TCON_TGEN_VS.	
	HCNT_RESET_SEL	0	TCON h counter reset by. 0: VOP2_HS. 1: TCON_TGEN_HS.	
11h (103023h)	**REG103023**	**7:0**	**Default: 0x00**	**Access: R/W**
	6BIT_R	7	Align 6-bit ML swap.	
	6BIT_L	6	Align 6-bit ML swap.	
	SWAP_ML_S	5	FIFO Output ML swap for R-channel.	
	SWAP_ML_F	4	FIFO Output ML swap for L-channel.	
	BANK_SWAP	3	FIFO Output LR bank swap.	
	PAIR_SWAP	2	FIFO Output pair bit swap.	
	RSDS_GCK_SWAP_S	1	Swap RSDS G and CLK for R-channel.	
	RSDS_GCK_SWAP_F	0	Swap RSDS G and CLK for L-channel.	
12h (103024h)	**REG103024**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	LVD2_CHASSIGNL[2:0]	6:4	Mini-LVDS L channel2 data select. 0: Channel 2. 1: Channel 1. 2: Channel 0. 3: Channel 3. 4: Channel 4. Others: Channel 5.	
	-	3	Reserved.	
	LVD3_CHASSIGNL[2:0]	2:0	Mini-LVDS L channel3 data select.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0: Channel 3. 1: Channel 1. 2: Channel 2. 3: Channel 0. 4: Channel 4. Others: Channel 5.	
12h (103025h)	**REG103025**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	LVD0_CHASSIGNL[2:0]	6:4	Mini-LVDS L channel0 data select. 0: Channel 0. 1: Channel 1. 2: Channel 2. 3: Channel 3. 4: Channel 4. Others: Channel 5.	
	-	3	Reserved.	
	LVD1_CHASSIGNL[2:0]	2:0	Mini-LVDS L channel1 data select. 0: Channel 1. 1: Channel 0. 2: Channel 2. 3: Channel 3. 4: Channel 4. Others: Channel 5.	
13h (103026h)	**REG103026**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	CKDATA_ASSIGNL[2:0]	6:4	Mini-LVDS L clock/data channel select. 0: Channel 0. 1: Channel 1. 2: Channel 2. 3: Channel 3. 4: Channel 4. Others: Channel 5.	
	-	3:0	Reserved.	
13h (103027h)	**REG103027**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	LVD4_CHASSIGNL[2:0]	6:4	Mini-LVDS L channel4 data select. 0: Channel 4. 1: Channel 1.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2: Channel 2. 3: Channel 3. 4: Channel 0. Others: Channel 5.	
	-	3	Reserved.	
	LVD5_CHASSIGNL[2:0]	2:0	Mini-LVDS L channel5 data select. 0: Channel 5. 1: Channel 1. 2: Channel 2. 3: Channel 3. 4: Channel 4. Others: Channel 0.	
14h (103028h)	**REG103028**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	LVD2_CHASSIGNR[2:0]	6:4	Mini-LVDS R channel2 data select. 0: Channel 2. 1: Channel 1. 2: Channel 0. 3: Channel 3. 4: Channel 4. Others: Channel 5.	
	-	3	Reserved.	
	LVD3_CHASSIGNR[2:0]	2:0	Mini-LVDS R channel3 data select. 0: Channel 3. 1: Channel 1. 2: Channel 2. 3: Channel 0. 4: Channel 4. Others: Channel 5.	
14h (103029h)	**REG103029**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	LVD0_CHASSIGNR[2:0]	6:4	Mini-LVDS R channel0 data select. 0: Channel 0. 1: Channel 1. 2: Channel 2. 3: Channel 3. 4: Channel 4. Others: Channel 5.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	3	Reserved.	
	LVD1_CHASSIGNR[2:0]	2:0	Mini-LVDS R channel1 data select. 0: Channel 1. 1: Channel 0. 2: Channel 2. 3: Channel 3. 4: Channel 4. Others: Channel 5.	
15h (10302Ah)	**REG10302A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	CKDATA_ASSIGNR[2:0]	6:4	Mini-LVDS R clock/data channel select. 0: Channel 0. 1: Channel 1. 2: Channel 2. 3: Channel 3. 4: Channel 4. Others: Channel 5.	
	-	3:0	Reserved.	
15h (10302Bh)	**REG10302B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	LVD4_CHASSIGNR[2:0]	6:4	Mini-LVDS R channel4 data select. 0: Channel 4. 1: Channel 1. 2: Channel 2. 3: Channel 3. 4: Channel 0. Others: Channel 5.	
	-	3	Reserved.	
	LVD5_CHASSIGNR[2:0]	2:0	Mini-LVDS R channel5 data select. 0: Channel 5. 1: Channel 1. 2: Channel 2. 3: Channel 3. 4: Channel 4. Others: Channel 0.	
16h (10302Ch)	**REG10302C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_B1[3:0]	7:4	Source data mapping B channel select for pixel1. 1G: 2.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2GM0 (DRD normal): 5. 2GM1 (DRD Bi-Scan): 1.	
	DSEL_IMAP_R2[3:0]	3:0	Source data mapping R channel select for pixel2. 1G: 0. 2GM0 (DRD normal): 1. 2GM1 (DRD Bi-Scan): 5.	
16h (10302Dh)	**REG10302D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_R1[3:0]	7:4	Source data mapping R channel select for pixel1. 1G: 0. 2GM0 (DRD normal): 0. 2GM1 (DRD Bi-Scan): 4.	
	DSEL_IMAP_G1[3:0]	3:0	Source data mapping G channel select for pixel1. 1G: 1. 2GM0 (DRD normal): 3. 2GM1 (DRD Bi-Scan): 3.	
17h (10302Eh)	**REG10302E**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_R3[3:0]	7:4	Source data mapping R channel select for pixel3. 1G: 0. 2GM0 (DRD normal): 0. 2GM1 (DRD Bi-Scan): 4.	
	DSEL_IMAP_G3[3:0]	3:0	Source data mapping G channel select for pixel3. 1G: 1. 2GM0 (DRD normal): 3. 2GM1 (DRD Bi-Scan): 3.	
17h (10302Fh)	**REG10302F**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_G2[3:0]	7:4	Source data mapping G channel select for pixel2. 1G: 1. 2GM0 (DRD normal): 2. 2GM1 (DRD Bi-Scan): 2.	
	DSEL_IMAP_B2[3:0]	3:0	Source data mapping B channel select for pixel2. 1G: 2. 2GM0 (DRD normal): 4. 2GM1 (DRD Bi-Scan): 0.	
18h (103030h)	**REG103030**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_G4[3:0]	7:4	Source data mapping G channel select for pixel4. 1G: 1. 2GM0 (DRD normal): 2. 2GM1 (DRD Bi-Scan): 2.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DSEL_IMAP_B4[3:0]	3:0	Source data mapping B channel select for pixel4. 1G: 2. 2GM0 (DRD normal): 4. 2GM1 (DRD Bi-Scan): 0.	
18h (103031h)	**REG103031**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_B3[3:0]	7:4	Source data mapping B channel select for pixel3. 1G: 2. 2GM0 (DRD normal): 5. 2GM1 (DRD Bi-Scan): 1.	
	DSEL_IMAP_R4[3:0]	3:0	Source data mapping R channel select for pixel4. 1G: 0. 2GM0 (DRD normal): 1. 2GM1 (DRD Bi-Scan): 5.	
19h (103032h)	**REG103032**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_B5[3:0]	7:4	Source data mapping B channel select for pixel5. 1G: 2. 2GM0 (DRD normal): 5. 2GM1 (DRD Bi-Scan): 1.	
	DSEL_IMAP_R6[3:0]	3:0	Source data mapping R channel select for pixel6. 1G: 0. 2GM0 (DRD normal): 1. 2GM1 (DRD Bi-Scan): 5.	
19h (103033h)	**REG103033**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_R5[3:0]	7:4	Source data mapping R channel select for pixel5. 1G: 0. 2GM0 (DRD normal): 0. 2GM1 (DRD Bi-Scan): 4.	
	DSEL_IMAP_G5[3:0]	3:0	Source data mapping G channel select for pixel5. 1G: 1. 2GM0 (DRD normal): 3. 2GM1 (DRD Bi-Scan): 3.	
1Ah (103034h)	**REG103034**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_R7[3:0]	7:4	Source data mapping R channel select for pixel7. 1G: 0. 2GM0 (DRD normal): 0. 2GM1 (DRD Bi-Scan): 4.	
	DSEL_IMAP_G7[3:0]	3:0	Source data mapping G channel select for pixel7. 1G: 1.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			2GM0 (DRD normal): 3. 2GM1 (DRD Bi-Scan): 3.	
1Ah (103035h)	**REG103035**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_G6[3:0]	7:4	Source data mapping G channel select for pixel6. 1G: 1. 2GM0 (DRD normal): 2. 2GM1 (DRD Bi-Scan): 2.	
	DSEL_IMAP_B6[3:0]	3:0	Source data mapping B channel select for pixel6. 1G: 2. 2GM0 (DRD normal): 4. 2GM1 (DRD Bi-Scan): 0.	
1Bh (103036h)	**REG103036**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_G8[3:0]	7:4	Source data mapping G channel select for pixel8. 1G: 1. 2GM0 (DRD normal): 2. 2GM1 (DRD Bi-Scan): 2.	
	DSEL_IMAP_B8[3:0]	3:0	Source data mapping B channel select for pixel8. 1G: 2. 2GM0 (DRD normal): 4. 2GM1 (DRD Bi-Scan): 0.	
1Bh (103037h)	**REG103037**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_IMAP_B7[3:0]	7:4	Source data mapping B channel select for pixel7. 1G: 2. 2GM0 (DRD normal): 5. 2GM1 (DRD Bi-Scan): 1.	
	DSEL_IMAP_R8[3:0]	3:0	Source data mapping R channel select for pixel8. 1G: 0. 2GM0 (DRD normal): 1. 2GM1 (DRD Bi-Scan): 5.	
1Ch (103039h)	**REG103039**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_DMY	7	Data mapping input FIFO dummy data insert enable.	
	-	6:0	Reserved.	
1Dh (10303Ah)	**REG10303A**	**7:0**	**Default: 0x00**	**Access: R/W**
	DSEL_PIX[7:0]	7:0	G1G2 data frame select control, 8 frames. 0: A. 1: B.	
1Dh	**REG10303B**	**7:0**	**Default: 0x00**	**Access: R/W**

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10303Bh)	DSEL_DMY_LEVEL[7:0]	7:0	Data mapping input FIFO dummy data insert value.	
1Eh (10303Ch)	**REG10303C**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY_LINE_VA[7:0]	7:0	Dummy line value.	
1Eh (10303Dh)	**REG10303D**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY_LINE_EN	7	Enable dummy line.	
	ALL_BLK_DUMMY	6	V blank all dummy enable. Please set CONT_DE_SEL=1 before enable this function.	
	-	5:4	Reserved.	
	DUMMY_LINE_HEAD[1:0]	3:2	Dummy line number at head.	
	DUMMY_LINE_TAIL[1:0]	1:0	Dummy line number at tail.	
1Fh (10303Eh)	**REG10303E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	VMDEEND[7:0]	7:0	Delay for timing adjust in v-reset (unit: Hsync).	
1Fh (10303Fh)	**REG10303F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	VMDEEND[11:8]	3:0	See description of '10303Eh'.	
20h (103040h)	**REG103040**	**7:0**	**Default: 0x00**	**Access: R/W**
	VCNT_DELAY[7:0]	7:0	Delay for timing adjust in h-reset (unit: ODCLK).	
20h (103041h)	**REG103041**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	VCNT_DELAY[11:8]	3:0	See description of '103040h'.	
21h (103042h)	**REG103042**	**7:0**	**Default: 0x00**	**Access: R/W**
	HCNT_DELAY[7:0]	7:0	Delay for timing adjust in h-reset.	
21h (103043h)	**REG103043**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	HCNT_DELAY[11:8]	3:0	See description of '103042h'.	
22h (103044h)	**REG103044**	**7:0**	**Default: 0x00**	**Access: RO**
	VTOTAL_ODD[7:0]	7:0	Vtotal value of odd field.	
22h (103045h)	**REG103045**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	VTOTAL_ODD[11:8]	3:0	See description of '103044h'.	
23h (103046h)	**REG103046**	**7:0**	**Default: 0x00**	**Access: RO**
	VTOTAL_EVEN[7:0]	7:0	Vtotal value of even field.	
23h	**REG103047**	**7:0**	**Default: 0x00**	**Access: RO**

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103047h)	-	7:4	Reserved.	
	VTOTAL_EVEN[11:8]	3:0	See description of '103046h'.	
24h (103048h)	**REG103048**	**7:0**	**Default: 0x00**	**Access: RO**
	HTOTAL_ODD[7:0]	7:0	Htotal value of odd field.	
24h (103049h)	**REG103049**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	HTOTAL_ODD[11:8]	3:0	See description of '103048h'.	
25h (10304Ah)	**REG10304A**	**7:0**	**Default: 0x00**	**Access: RO**
	HTOTAL_EVEN[7:0]	7:0	Htotal value of even field.	
25h (10304Bh)	**REG10304B**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	HTOTAL_EVEN[11:8]	3:0	See description of '10304Ah'.	
26h (10304Ch)	**REG10304C**	**7:0**	**Default: 0x00**	**Access: R/W**
	HTT[7:0]	7:0	Htotal value setting for h blank value auto set.	
26h (10304Dh)	**REG10304D**	**7:0**	**Default: 0x20**	**Access: R/W**
	USE_AUTO_HTT	7	Use auto HTT to set h blank value.	
	USE_HTT_HBLK	6	Use HTT to set h blank value.	
	EN_HBLK	5	Enable HBLK to delay GPO.	
	-	4	Reserved.	
	HTT[11:8]	3:0	See description of '10304Ch'.	
27h (10304Eh)	**REG10304E**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	LB_BIST_FAIL[3:0]	3:0	Line buffer BIST fail flag.	
27h (10304Fh)	**REG10304F**	**7:0**	**Default: 0x00**	**Access: R/W**
	LB_RD_DUMMY[7:0]	7:0	Lb read dummy.	
28h (103050h)	**REG103050**	**7:0**	**Default: 0x00**	**Access: R/W**
	DUMMY_ADDR[7:0]	7:0	The insert address which to insert dummy pixels.	
28h (103051h)	**REG103051**	**7:0**	**Default: 0x00**	**Access: R/W**
	EN_MIDDLE_DUMMY	7	Enable middle dummy pixel function.	
	-	6	Reserved.	
	DUMMY_OFFSET[3:0]	5:2	How many dummy pixel need to insert.	
	DUMMY_ADDR[9:8]	1:0	See description of '103050h'.	
29h	**REG103052**	**7:0**	**Default: 0x00**	**Access: R/W**

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103052h)	INSERT_DUMMY_PT[7:0]	7:0	Single pixel insert point.	
29h (103053h)	**REG103053**	**7:0**	**Default: 0x00**	**Access: R/W**
	EN_DUMMY_INSERT	7	Enable single pixel insert.	
	-	6:4	Reserved.	
	INSERT_DUMMY_PT[11:8]	3:0	See description of '103052h'.	
30h ~ 31h (103060h ~ 103063h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
40h (103080h)	**REG103080**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO4_HEAD_PLUS[1:0]	7:6	Add more line toggle mode at head of GPO4.	
	GPO3_HEAD_PLUS[1:0]	5:4	Add more line toggle mode at head of GPO3.	
	GPO2_HEAD_PLUS[1:0]	3:2	Add more line toggle mode at head of GPO2.	
	GPO1_HEAD_PLUS[1:0]	1:0	Add more line toggle mode at head of GPO1.	
40h (103081h)	**REG103081**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPOC_HEAD_PLUS[1:0]	7:6	Add more line toggle mode at head of GPOc.	
	GPOB_HEAD_PLUS[1:0]	5:4	Add more line toggle mode at head of GPOb.	
	GPOA_HEAD_PLUS[1:0]	3:2	Add more line toggle mode at head of GPOa.	
	GPO9_HEAD_PLUS[1:0]	1:0	Add more line toggle mode at head of GPO9.	
41h (103082h)	**REG103082**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	GPOD_HEAD_PLUS[1:0]	1:0	Add more line toggle mode at head of GPOd.	
42h (103084h)	**REG103084**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO4_TAIL_PLUS[1:0]	7:6	Add more line toggle mode at tail of GPO4.	
	GPO3_TAIL_PLUS[1:0]	5:4	Add more line toggle mode at tail of GPO3.	
	GPO2_TAIL_PLUS[1:0]	3:2	Add more line toggle mode at tail of GPO2.	
	GPO1_TAIL_PLUS[1:0]	1:0	Add more line toggle mode at tail of GPO1.	
42h (103085h)	**REG103085**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPOC_TAIL_PLUS[1:0]	7:6	Add more line toggle mode at tail of GPOc.	
	GPOB_TAIL_PLUS[1:0]	5:4	Add more line toggle mode at tail of GPOb.	
	GPOA_TAIL_PLUS[1:0]	3:2	Add more line toggle mode at tail of GPOa.	
	GPO9_TAIL_PLUS[1:0]	1:0	Add more line toggle mode at tail of GPO9.	
43h (103086h)	**REG103086**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	

DISP_TC_BK1 Register (Bank = 1030, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	GPOD_TAIL_PLUS[1:0]	1:0	Add more line toggle mode at tail of GPOd.	
44h (103088h)	**REG103088**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPOC_ONLY_HEAD_TAIL	7	Only head and tail line toggle part of GPOc.	
	GPOB_ONLY_HEAD_TAIL	6	Only head and tail line toggle part of GPOb.	
	GPOA_ONLY_HEAD_TAIL	5	Only head and tail line toggle part of GPOa.	
	GPO9_ONLY_HEAD_TAIL	4	Only head and tail line toggle part of GPO9.	
	GPO4_ONLY_HEAD_TAIL	3	Only head and tail line toggle part of GPO4.	
	GPO3_ONLY_HEAD_TAIL	2	Only head and tail line toggle part of GPO3.	
	GPO2_ONLY_HEAD_TAIL	1	Only head and tail line toggle part of GPO2.	
	GPO1_ONLY_HEAD_TAIL	0	Only head and tail line toggle part of GPO1.	
44h (103089h)	**REG103089**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	GPOD_ONLY_HEAD_TAIL	0	Only head and tail line toggle part of GPOd.	

Scaler 3 LPLL_ANA Register (Bank = 1031)

Scaler 3 LPLL_ANA Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
00h (103100h)	**REG103100**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LPLL1_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control. 00: /1. 01: /2. 10: /4. 11: /8.	
00h (103101h)	**REG103101**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL1_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N). 0: Divide 1. 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4. ...	
01h (103102h)	**REG103102**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:2	Reserved.	
	LPLL1_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control. 00: /1. 01: /2. 10: /4. 11: /8.	
01h (103103h)	**REG103103**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL1_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio=(1/N). Default ratio=8. 0: Divide 1. 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4. ...	
02h (103104h)	**REG103104**	**7:0**	**Default: 0x02**	**Access: R/W**
	-	7:2	Reserved.	
	LPLL1_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
02h	**REG103105**	**7:0**	**Default: 0x00**	**Access: R/W**

Scaler 3 LPLL_ANA Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103105h)	LPLL1_OUTPUT_DIV_SECOND[7:0]	7:0	Output divider.	
03h (103106h)	**REG103106**	**7:0**	**Default: 0x23**	**Access: R/W**
	LPLL1_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL1_2CHIP_SYN_EN	6		
	LPLL1_PD	5	Power down control to PLL (active high).	
	LPLL1_EN_HFLVDS	4		
	LPLL1_IBIAS_ICTRL[1:0]	3:2		
	LPLL1_ICP_ICTRL[1:0]	1:0	LPLL current control.	
03h (103107h)	**REG103107**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	LPLL1_HIGH_FLAG	7		
	LPLL1_LOCK	6		
	-	5	Reserved.	
	LPLL1_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL1_EN_SKEW_DIVIDER	1		
	LPLL1_ENFRUN	0		
04h (103108h)	**REG103108**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	LPLL1_SKEW_CLKP_PHASE_SEL[4:0]	4:0		
04h (103109h)	**REG103109**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	LPLL1_SKEW_CLKM_PHASE_SEL[4:0]	4:0		
0Dh (10311Bh)	**REG10311B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	SSC_EN	3	SSC mode enable.	
	-	2:0	Reserved.	
17h (10312Eh)	**REG10312E**	**7:0**	**Default: 0x20**	**Access: R/W**
	LPLL_STEP[7:0]	7:0	Output PLL spread spectrum step.	
17h (10312Fh)	**REG10312F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	

Scaler 3 LPLL_ANA Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	LPLL_STEP[9:8]	1:0	See description of '10312Eh'.	
18h (103130h)	**REG103130**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL_SPAN[7:0]	7:0	Output PLL spread spectrum span.	
18h (103131h)	**REG103131**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	LPLL_SPAN[13:8]	5:0	See description of '103130h'.	
2Bh ~ 2Dh (103156h ~ 10315Bh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
2Eh (10315Ch)	**REG10315C**	**7:0**	**Default: 0x43**	**Access: R/W**
	-	7:2	Reserved.	
	LPLL_PDREG	1	LPLL reg power down.	
	LPL_PDBG	0	LPLL bg power down.	
30h (103160h)	**REG103160**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LPLL2_INPUT_DIV_FIRST[1:0]	1:0	Input divider ratio control. 00: /1. 01: /2. 10: /4. 11: /8.	
30h (103161h)	**REG103161**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL2_INPUT_DIV_SECOND[7:0]	7:0	Input divider ratio control: divide ratio=(1/N). 0: Divide 1 . 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4. ...	
31h (103162h)	**REG103162**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LPLL2_LOOP_DIV_FIRST[1:0]	1:0	Loop divider ratio control. 00: /1. 01: /2. 10: /4. 11: /8.	
31h	**REG103163**	**7:0**	**Default: 0x00**	**Access: R/W**

Scaler 3 LPLL_ANA Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103163h)	LPLL2_LOOP_DIV_SECOND[7:0]	7:0	Loop divider ratio control: divide ratio=(1/N). Default ratio=8. 0: Divide 1 . 1: Divide 1. 2: Divide 2. 3: Divide 3. 4: Divide 4. …	
32h (103164h)	**REG103164**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	LPLL2_OUTPUT_DIV_FIRST[1:0]	1:0	Output divider.	
32h (103165h)	**REG103165**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL2_OUTPUT_DIV_SECOND[7:0]	7:0	Output divider.	
33h (103166h)	**REG103166**	**7:0**	**Default: 0x20**	**Access: R/W**
	LPLL2_SKEW_DIVIDER_DIV2_SEL	7		
	LPLL2_2CHIP_SYN_EN	6		
	LPLL2_PD	5	Power down control to PLL (active high).	
	LPLL2_EN_HFLVDS	4	Reset digital circuit in LPLL.	
	LPLL2_IBIAS_ICTRL[1:0]	3:2		
	LPLL2_ICP_ICTRL[1:0]	1:0	LPLL current control.	
33h (103167h)	**REG103167**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	LPLL2_HIGH_FLAG	7		
	LPLL2_LOCK	6		
	-	5	Reserved.	
	LPLL2_SCALAR_DIV_SEL[2:0]	4:2		
	LPLL2_EN_SKEW_DIVIDER	1		
	LPLL2_ENFRUN	0		
34h (103168h)	**REG103168**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	LPLL2_SKEW_CLKP_PHASE_SEL[4:0]	4:0		

Scaler 3 LPLL_ANA Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
34h (103169h)	**REG103169**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	LPLL2_SKEW_CLKM_PHASE_SEL[4:0]	4:0		
35h (10316Ah)	**REG10316A**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:6	Reserved.	
	LPLL_2NDPLL_CLK_SEL	5		
	LPLL_POSTDIV_RESET	4		
	-	3	Reserved.	
	LPLL_2CHIP_REFIN_SEL	2		
	LPLL_2CHIP_FBIN_SEL	1		
	LPLL_2CHIP_CLKOUT_SEL	0		
36h (10316Ch)	**REG10316C**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL1_TEST[7:0]	7:0	LPLL1_TEST.	
36h (10316Dh)	**REG10316D**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL1_TEST[15:8]	7:0	See description of '10316Ch'.	
37h (10316Eh)	**REG10316E**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL1_TEST[23:16]	7:0	See description of '10316Ch'.	
37h (10316Fh)	**REG10316F**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL1_TEST[31:24]	7:0	See description of '10316Ch'.	
38h (103170h)	**REG103170**	**7:0**	**Default: 0x01**	**Access: R/W**
	-	7:2	Reserved.	
	LPLL_SCALAR_FB_DIV2_EN	1		
	LPLL_NCO_RETIME_SEL	0		
39h (103172h)	**REG103172**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL2_TEST[7:0]	7:0	LPLL2_TEST.	
39h (103173h)	**REG103173**	**7:0**	**Default: 0x00**	**Access: R/W**
	LPLL2_TEST[15:8]	7:0	See description of '103172h'.	
3Ah (103174h)	**REG103174**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	LPLL_2CHIP_SCALAR_FB_DIV2_EN	4		

Scaler 3 LPLL_ANA Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OEN_FBIN	3		
	OEN_REFIN	2		
	LPLL1_RX_CLKFB_SEL	1		
	LPLL1_CLKIN_SEL	0		
3Dh ~ 3Eh (10317Ah ~ 10317Dh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
3Fh (10317Eh)	**REG10317E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:1	Reserved.	
	LPLL_RESET	0	LPLL software reset, high active.	

Scaler 3 LPLL_DIG Register (Bank = 1031)

Scaler 3 LPLL_DIG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
05h (10310Ah)	**REG10310A**	**7:0**	**Default: 0x22**	**Access: R/W**
	PRD_LOCK_THRESH[3:0]	7:4	Period lock threshold.	
	PRD_STABLE_THRESH[3:0]	3:0	Clock stable threshold.	
05h (10310Bh)	**REG10310B**	**7:0**	**Default: 0x02**	**Access: R/W**
	PHASE_LOCK_THRESH[7:0]	7:0	Phase lock threshold.	
06h (10310Ch)	**REG10310C**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIMIT_D5D6D7[7:0]	7:0	Limit for clock frequency correction modification.	
06h (10310Dh)	**REG10310D**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIMIT_D5D6D7[15:8]	7:0	See description of '10310Ch'.	
07h (10310Eh)	**REG10310E**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIMIT_D5D6D7[23:16]	7:0	See description of '10310Ch'.	
08h (103110h)	**REG103110**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIMIT_D5D6D7_RK[7:0]	7:0	Limit for phase correction modification.	
08h (103111h)	**REG103111**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIMIT_D5D6D7_RK[15:8]	7:0	See description of '103110h'.	
09h (103112h)	**REG103112**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIMIT_D5D6D7_RK[23:16]	7:0	See description of '103110h'.	
0Ah (103114h)	**REG103114**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIMIT_LPLL_OFFSET[7:0]	7:0	Limit for LPLL phase offset.	
0Ah (103115h)	**REG103115**	**7:0**	**Default: 0x00**	**Access: R/W**
	LIMIT_LPLL_OFFSET[15:8]	7:0	See description of '103114h'.	
0Bh (103116h)	**REG103116**	**7:0**	**Default: 0x10**	**Access: R/W**
	P_GAIN_PRD[3:0]	7:4	P_GAIN for PRD_LOCK, gain setting is same as I_GAIN_PRD.	
	I_GAIN_PRD[3:0]	3:0	I_GAIN for period lock. 0: >> 5. 1: >> 4. 2: >> 3. 3: >> 2. 4: >> 1. 5: Same. 6: << 1. 7: << 2.	

Scaler 3 LPLL_DIG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			8: << 3. 9: << 4. 10: << 5. 11: << 6. 12: << 7. 13: << 8. 14: << 9. 15: << 10.	
0Bh (103117h)	**REG103117**	**7:0**	**Default: 0x10**	**Access: R/W**
	P_GAIN_PHASE[3:0]	7:4	P_GAIN for phase lock, gain setting is same as I_GAIN_PRD.	
	I_GAIN_PHASE[3:0]	3:0	I_GAIN for phase lock, game setting is same as I_GAIN_PRD.	
0Ch (103118h)	**REG103118**	**7:0**	**Default: 0x00**	**Access: R/W**
	P_GAIN_PHASE_ZERO	7	Disable P_GAIN for lock phase.	
	I_GAIN_PHASE_ZERO	6	Disable I_GAIN for lock phase.	
	P_GAIN_PRD_ZERO	5	Disable P_GAIN for lock period.	
	I_GAIN_PRD_ZERO	4	Disable I_GAIN for lock period.	
	FRAME_LPLL_EN	3	Frame LPLL enable.	
	-	2	Reserved.	
	FPLL_MODE[1:0]	1:0	FPLL Mode. 00: Lock phase mode.	
0Ch (103119h)	**REG103119**	**7:0**	**Default: 0x00**	**Access: R/W**
	OVS_FRAME_DIV[3:0]	7:4	Output fame div for frame sync.	
	IVS_FRAME_DIV[3:0]	3:0	Input frame div for frame sync.	
0Dh (10311Ah)	**REG10311A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:5	Reserved.	
	EN_2_LIMIT	4	Enable 2 limit.	
	FORCE_PHASE_CLOSE_DONE	3	S.W. Force phase close done.	
	FORCE_PHASE_REDUCE_DONE	2	S.W. Force phase reduce done.	
	FORCE_PRD_LOCK_DONE	1	S.W. Force period lock done.	
	FORCE_PRD_STABLE	0	S.W.	

Scaler 3 LPLL_DIG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			Force period stable check ok.	
0Dh (10311Bh)	**REG10311B**	**7:0**	**Default: 0x03**	**Access: R/W**
	-	7:3	Reserved.	
	PRD_SEL_ORI_VS	2	Select ORI OVS as lock period reference.	
	NON_STABLE_EN	1	Frame PLL disable when NON_STABLE flag high.	
	NO_SIGNAL_EN	0	Frame PLL disable when NO_SIGNAL flag high.	
0Fh (10311Eh)	**REG10311E**	**7:0**	**Default: 0x44**	**Access: R/W**
	LPLL_SET[7:0]	7:0	LPLL initial setting value.	
0Fh (10311Fh)	**REG10311F**	**7:0**	**Default: 0x55**	**Access: R/W**
	LPLL_SET[15:8]	7:0	See description of '10311Eh'.	
10h (103120h)	**REG103120**	**7:0**	**Default: 0x24**	**Access: R/W**
	LPLL_SET[23:16]	7:0	See description of '10311Eh'.	
11h (103122h)	**REG103122**	**7:0**	**Default: 0x00**	**Access: RO**
	PHASE_DIF[7:0]	7:0	Phase dif value.	
11h (103123h)	**REG103123**	**7:0**	**Default: 0x00**	**Access: RO**
	PHASE_DIF[15:8]	7:0	See description of '103122h'.	
12h (103124h)	**REG103124**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:1	Reserved.	
	PHASE_UP	0	OVS leading or lagging related to IVS. 0: Leading. 1: Lagging.	
13h (103126h)	**REG103126**	**7:0**	**Default: 0x00**	**Access: RO**
	PRD_DIF[7:0]	7:0	Reference signal period difference value.	
13h (103127h)	**REG103127**	**7:0**	**Default: 0x00**	**Access: RO**
	PRD_DIF[15:8]	7:0	See description of '103126h'.	
14h (103128h)	**REG103128**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:1	Reserved.	
	PRD_UP	0	OVS period related to IVS period. 0: Faster. 1: Slower.	
16h ~ 1Eh (10312Ch ~ 10313Dh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
1Fh	**REG10313E**	**7:0**	**Default: 0x80**	**Access: R/W**

Scaler 3 LPLL_DIG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10313Eh)	PHASE_CLOSE_THRESH[7:0]	7:0	Phase close done threshold.	
1Fh (10313Fh)	**REG10313F**	**7:0**	**Default: 0x30**	**Access: R/W**
	REDUCE_DONE_THRESH[3:0]	7:4	Phase reduce done threshold.	
	PHASE_CLOSE_THRESH[11:8]	3:0	See description of '10313Eh'.	
20h (103140h)	**REG103140**	**7:0**	**Default: 0x52**	**Access: R/W**
	-	7	Reserved.	
	HIS_CNT_HIGH_THRESH[2:0]	6:4	History counter high threshold.	
	-	3	Reserved.	
	HIS_CNT_LOW_THRESH[2:0]	2:0	History counter low threshold.	
21h (103142h)	**REG103142**	**7:0**	**Default: 0x00**	**Access: RO**
	IVS_PRD_VALUE[7:0]	7:0	IVS period value.	
21h (103143h)	**REG103143**	**7:0**	**Default: 0x00**	**Access: RO**
	IVS_PRD_VALUE[15:8]	7:0	See description of '103142h'.	
22h (103144h)	**REG103144**	**7:0**	**Default: 0x00**	**Access: RO**
	IVS_PRD_VALUE[23:16]	7:0	See description of '103142h'.	
23h (103146h)	**REG103146**	**7:0**	**Default: 0x00**	**Access: RO**
	OVS_PRD_VALUE[7:0]	7:0	OVS period value.	
23h (103147h)	**REG103147**	**7:0**	**Default: 0x00**	**Access: RO**
	OVS_PRD_VALUE[15:8]	7:0	See description of '103146h'.	
24h (103148h)	**REG103148**	**7:0**	**Default: 0x00**	**Access: RO**
	OVS_PRD_VALUE[23:16]	7:0	See description of '103146h'.	
26h ~ 27h (10314Ch ~ 10314Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
28h (103150h)	**REG103150**	**7:0**	**Default: 0x00**	**Access: RO**
	LPLL_SET_USING[7:0]	7:0	LPLL_SET value for using.	
28h (103151h)	**REG103151**	**7:0**	**Default: 0x00**	**Access: RO**
	LPLL_SET_USING[15:8]	7:0	See description of '103150h'.	
29h	**REG103152**	**7:0**	**Default: 0x00**	**Access: RO**

Scaler 3 LPLL_DIG Register (Bank = 1031)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103152h)	LPLL_SET_USING[23:16]	7:0	See description of '103150h'.	
2Ah (103154h)	**REG103154**	**7:0**	**Default: 0x00**	**Access: RO**
	PHASE_REDUCE_DONE	7	Phase reduce done flag.	
	PRD_LOCK_DONE	6	Period lock done flag.	
	IVS_PRD_STABLE	5	IDCLK stable flag.	
	OVS_PRD_STABLE	4	ODCLK stable flag.	
	-	3	Reserved.	
	CS_STATE[2:0]	2:0	Frame PLL FSM state. 3'h0: Free run. 3'h1: LOCK_FREQ. 3'h2: REDUCE_PHASE. 3'h3: Wait PHASE_CLOSE. 3'h4: LOCK_PHASE. Others: Reserved.	
2Ah (103155h)	**REG103155**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:1	Reserved.	
	PHASE_LOCK_DONE	0	Phase lock done flag.	
2Bh ~ 3Ch (103156h ~ 103179h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	

Scaler 4 Register (Bank = 1032)

MOD Register (Bank = 1032, Sub-bank = 00)

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
01h ~ 07h (103203h ~ 10320Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
10h (103220h)	**REG103220**	**7:0**	**Default: 0xFF**	**Access: R/W**
	V_BLK_ST1_VPOS[7:0]	7:0	Bt656 v blanking 1st start v position.	
10h (103221h)	**REG103221**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	V_BLK_ST1_VPOS[11:8]	3:0	See description of '103220h'.	
11h (103222h)	**REG103222**	**7:0**	**Default: 0xFF**	**Access: R/W**
	V_BLK_ST1_HPOS[7:0]	7:0	Bt656 v blanking 1st start h position.	
11h (103223h)	**REG103223**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	V_BLK_ST1_HPOS[11:8]	3:0	See description of '103222h'.	
12h (103224h)	**REG103224**	**7:0**	**Default: 0xFF**	**Access: R/W**
	V_BLK_END1_VPOS[7:0]	7:0	Bt656 v blanking 1st endt v position.	
12h (103225h)	**REG103225**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	V_BLK_END1_VPOS[11:8]	3:0	See description of '103224h'.	
13h (103226h)	**REG103226**	**7:0**	**Default: 0xFF**	**Access: R/W**
	V_BLK_END1_HPOS[7:0]	7:0	Bt656 v blanking 1st end h position.	
13h (103227h)	**REG103227**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	V_BLK_END1_HPOS[11:8]	3:0	See description of '103226h'.	
14h (103228h)	**REG103228**	**7:0**	**Default: 0xFF**	**Access: R/W**
	V_BLK_ST2_VPOS[7:0]	7:0	Bt656 v blanking 2nd start v position.	
14h (103229h)	**REG103229**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	V_BLK_ST2_VPOS[11:8]	3:0	See description of '103228h'.	
15h (10322Ah)	**REG10322A**	**7:0**	**Default: 0xFF**	**Access: R/W**
	V_BLK_ST2_HPOS[7:0]	7:0	Bt656 v blanking 2nd start h position.	
15h	**REG10322B**	**7:0**	**Default: 0x0F**	**Access: R/W**

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10322Bh)	-	7:4	Reserved.	
	V_BLK_ST2_HPOS[11:8]	3:0	See description of '10322Ah'.	
16h (10322Ch)	**REG10322C**	**7:0**	**Default: 0xFF**	**Access: R/W**
	V_BLK_END2_VPOS[7:0]	7:0	Bt656 v blanking 2nd endt v position.	
16h (10322Dh)	**REG10322D**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	V_BLK_END2_VPOS[11:8]	3:0	See description of '10322Ch'.	
17h (10322Eh)	**REG10322E**	**7:0**	**Default: 0xFF**	**Access: R/W**
	V_BLK_END2_HPOS[7:0]	7:0	Bt656 v blanking 2nd end h position.	
17h (10322Fh)	**REG10322F**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	V_BLK_END2_HPOS[11:8]	3:0	See description of '10322Eh'.	
18h (103230h)	**REG103230**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FLD_ST1_VPOS[7:0]	7:0	Bt656 field1 start v position.	
18h (103231h)	**REG103231**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	FLD_ST1_VPOS[11:8]	3:0	See description of '103230h'.	
19h (103232h)	**REG103232**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FLD_ST1_HPOS[7:0]	7:0	Bt656 field1 start h position.	
19h (103233h)	**REG103233**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	FLD_ST1_HPOS[11:8]	3:0	See description of '103232h'.	
1Ah (103234h)	**REG103234**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FLD_ST2_VPOS[7:0]	7:0	Bt656 field2 start v position.	
1Ah (103235h)	**REG103235**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	FLD_ST2_VPOS[11:8]	3:0	See description of '103234h'.	
1Bh (103236h)	**REG103236**	**7:0**	**Default: 0xFF**	**Access: R/W**
	FLD_ST2_HPOS[7:0]	7:0	Bt656 field2 start h position.	
1Bh (103237h)	**REG103237**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	FLD_ST2_HPOS[11:8]	3:0	See description of '103236h'.	
1Ch	**REG103238**	**7:0**	**Default: 0x00**	**Access: R/W**

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103238h)	MASK_Y_BLK_VA[7:0]	7:0	Bt656 mask Y blanking value.	
1Ch (103239h)	**REG103239**	**7:0**	**Default: 0x08**	**Access: R/W**
	BT656_EN	7	Bt656 enable.	
	BT656_8BIT	6	Bt656 8-bit mode.	
	DDR_HL_SWAP	5	Bt656 DDR high low swap.	
	CRCB_SWAP	4	Swap CrCb position in 422.	
	444_BYPASS	3	Enable 444 to 422 conversion.	
	MASK_Y_BLK_EN	2	Bt656 mask Y blanking enable.	
	MASK_Y_BLK_VA[9:8]	1:0	See description of '103238h'.	
1Dh (10323Ah)	**REG10323A**	**7:0**	**Default: 0x00**	**Access: R/W**
	MASK_C_BLK_VA[7:0]	7:0	Bt656 mask C blanking value.	
1Dh (10323Bh)	**REG10323B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MASK_C_BLK_EN	2	Bt656 mask C blanking enable.	
	MASK_C_BLK_VA[9:8]	1:0	See description of '10323Ah'.	
20h (103241h)	**REG103241**	**7:0**	**Default: 0x11**	**Access: R/W**
	CKG_DOT_MINI_PRE[3:0]	7:4	Clock Gen register of CLK_DOT_MINI_PRE. Bit[0]: Gating. Bit[1]: Invert. Bit[3:2] = 00, enable.	
	CKG_DOT_MINI[3:0]	3:0	Clock Gen register of CLK_DOT_MINI. Bit[0]: Gating. Bit[1]: Invert. Bit[3:2] = 00, enable.	
21h ~ 22h (103242h ~ 103245h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
23h (103246h)	**REG103246**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	GCR_PE_ADJ_LVB_CLK[2:0]	6:4	Differential output data/clock pre-emphasis level adjust of LVDS channel B or mini-LVDS bank R clock pair.	
	-	3	Reserved.	
	GCR_PE_ADJ_LVB_DATA[2:0]	2:0	Differential output data/clock pre-emphasis level adjust of LVDS channel B or mini-LVDS bank R data pairs.	
23h	**REG103247**	**7:0**	**Default: 0x00**	**Access: R/W**

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103247h)	-	7	Reserved.	
	GCR_PE_ADJ_LVA_CLK[2:0]	6:4	Differential output data/clock pre-emphasis level adjust of LVDS channel A or mini-LVDS bank L clock pair.	
	-	3	Reserved.	
	GCR_PE_ADJ_LVA_DATA[2:0]	2:0	Differential output data/clock pre-emphasis level adjust of LVDS channel A or mini-LVDS bank L data pairs.	
2Bh (103256h)	**REG103256**	**7:0**	**Default: 0x0A**	**Access: R/W**
	-	7:6	Reserved.	
	GCR_ICON_LVB_DATA[5:0]	5:0	Control swing of LVDS channel B or mini-LVDS bank R data pairs. Swing=offset(150mV)+code*10mV.	
2Bh (103257h)	**REG103257**	**7:0**	**Default: 0x0A**	**Access: R/W**
	-	7:6	Reserved.	
	GCR_ICON_LVB_CLK[5:0]	5:0	Control swing of LVDS channel B or mini-LVDS bank R clock pair. Swing=offset(150mV)+code*10mV.	
2Ch (103258h)	**REG103258**	**7:0**	**Default: 0x0A**	**Access: R/W**
	-	7:6	Reserved.	
	GCR_ICON_LVA_DATA[5:0]	5:0	Control swing of LVDS channel A or mini-LVDS bank L data pairs. Swing=offset(150mV)+code*10mV.	
2Ch (103259h)	**REG103259**	**7:0**	**Default: 0x0A**	**Access: R/W**
	-	7:6	Reserved.	
	GCR_ICON_LVA_CLK[5:0]	5:0	Control swing of LVDS channel A or mini-LVDS bank L clock pair. Swing=offset(150mV)+code*10mV.	
32h (103264h)	**REG103264**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	MINI_CLK_GATE_EN	1	Gate mini FIFO CLK enable.	
	MOD_CLK_GATE_EN	0	Gate mod CLK enable.	
33h (103266h)	**REG103266**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBIT_NUM[4:0]	7:3	Digital serializer input data bit. 2: Mini-LVDS. 7: LVDS. Others: Reserved.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	DBIT_STR[2:0]	2:0	Digital serializer start counter number.	
33h (103267h)	**REG103267**	**7:0**	**Default: 0x00**	**Access: R/W**
	DBIT_CHK[7:0]	7:0	Digital serializer check counter number.	
34h (103268h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
34h (103269h)	**REG103269**	**7:0**	**Default: 0x00**	**Access: R/W**
	DATAX_SEL[1:0]	7:6	Digital serializer source mux. 00: LVDS. 01: Mini-LVDS. 1x: Reserved.	
	-	5:0	Reserved.	
35h (10326Ah)	**REG10326A**	**7:0**	**Default: 0x00**	**Access: RO**
	FIFO_RD_CNT_ERR	7	FIFO read counter error.	
	-	6	Reserved.	
	FIFO_RD_RPT[5:0]	5:0	Digital serializer FIFO read report.	
37h (10326Eh)	**REG10326E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	GCR_PVDD_2P5	6	MOD PVDD power. 0: 3.3V. 1: 2.5V.	
	GCR_VCM_0P9	5	Differential output common mode voltage adjust. 0: 1.25V. 1: 0.94V.	
	-	4:0	Reserved.	
38h ~ 3Ch (103270h ~ 103279h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
3Dh (10327Ah)	**REG10327A**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:6	Reserved.	
	ICON_RESULT[5:0]	5:0	Calibration icon result.	
3Dh (10327Bh)	**REG10327B**	**7:0**	**Default: 0x00**	**Access: RO, R/W**
	-	7	Reserved.	
	CAL_FINISH	6	Calibration finish flag.	
	CAL_FAIL	5	Calibration fail flag.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	-	4:0	Reserved.	
40h (103280h)	**REG103280**	**7:0**	**Default: 0x08**	**Access: R/W**
	LVDS_OSD_A	7	LVDS OSD enable for Channel A.	
	CH_SWAP	6	For pair swapping with 0x40[3].	
	CH_POLARITY	5	Channel polarity p/n swap for LVDS pair.	
	LVDS_PLASMA_A	4	LVDS_PLASMA for Channel A.	
	PDP_10BIT	3	PDP_10BIT for pair swap with 0x40[5].	
	LVDS_TI	2	LVDS_TI. 0: JEIDA mode. 1: VESA mode with 0x4b[1:0].	
	-	1	Reserved.	
	CLKB	0	CLKB.	
40h (103281h)	**REG103281**	**7:0**	**Default: 0x00**	**Access: R/W**
	ECLKDLYSEL[3:0]	7:4	De delay for TTL output.	
	CLKDLYSEL[3:0]	3:0	Clock delay for TTL output.	
41h (103282h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
41h (103283h)	**REG103283**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDP_MASK_EN_A	7	PDP_MASK_EN DE channel A.	
	PDP_MASK_SET_A	6	PDP_MASK_SET DE channel A.	
	PDP_CH3_EN_A	5	PDP_CH3_EN channel A.	
	PDP_CH3_SET_A	4	PDP_CH3_SET channel A.	
	PDP_CH4_EN_A	3	PDP_CH4_EN channel A.	
	PDP_CH4_SET_A	2	PDP_CH4_SET for channel A.	
	SKEW[1:0]	1:0	ODD Red TTL data SKEW.	
42h (103284h)	**REG103284**	**7:0**	**Default: 0x00**	**Access: R/W**
	SHIFT_LVDS_PAIR[1:0]	7:6	Shift LVDS arrangement for different substrate.	
	PDP_10BIT_MOR[1:0]	5:4	More pair swap mode.	
	-	3	Reserved.	
	EN_VS_ON_OSD	2	Vsync on OSD enable.	
	PAIR_SWAP_MOR[1:0]	1:0	More pair swap mode.	
42h (103285h)	**REG103285**	**7:0**	**Default: 0x10**	**Access: R/W**
	OSD_DE_INV	7	Invert OSD DE.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OSD_ON_DE_B	6	PDP OSD de on DE channel B.	
	OSD_ON_DE_A	5	PDP OSD de on DE channel A.	
	SW_RST	4	Software reset.	
	LVDS_OSD_B	3	LVDS OSD enable for Channel B.	
	LVDS_PLASMA_B	2	LVDS_PLASMA for Channel B.	
	-	1	Reserved.	
	EN_MORE_PAIR_SWAP	0	Enable more pair swap.	
43h (103286h)	**REG103286**	**7:0**	**Default: 0xC6**	**Access: R/W**
	LVDS_CLOCK_PHASE[6:0]	7:1	Clock phase could be set by register.	
	-	0	Reserved.	
43h (103287h)	**REG103287**	**7:0**	**Default: 0x00**	**Access: R/W**
	PDP_MASK_EN_B	7	PDP_MASK_EN DE channel B.	
	PDP_MASK_SET_B	6	PDP_MASK_SET DE channel B.	
	PDP_CH3_EN_B	5	PDP_CH3_EN channel B.	
	PDP_CH3_SET_B	4	PDP_CH3_SET channel B.	
	PDP_CH4_EN_B	3	PDP_CH4_EN channel B.	
	PDP_CH4_SET_B	2	PDP_CH4_SET for channel B.	
	-	1:0	Reserved.	
44h (103288h)	**REG103288**	**7:0**	**Default: 0x00**	**Access: R/W**
	SKEW_OTHER[7:0]	7:0	TTL skew for others. [1:0]: ODD Green. [3:2]: ODD Blue. [5:4]: EVEN Red. [7:6]: EVEN Green. [9:8]: EVEN Blue.	
44h (103289h)	**REG103289**	**7:0**	**Default: 0x10**	**Access: R/W**
	-	7:6	Reserved.	
	EN_HLOAD	5	Enable HLOAD mechanism.	
	EN_LOADZ_SYNC	4	Enable new HLOAD mechanism for LOADZ sync. 0: Single LVDS channel. 1: Dual LVDS channel.	
	LCK_PHASE_SEL	3	Phase select of TTL CLKx2. 1: Phase ahead 90 degree.	
	-	2	Reserved.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	SKEW_OTHER[9:8]	1:0	See description of '103288h'.	
45h (10328Ah)	**REG10328A**	**7:0**	**Default: 0x3F**	**Access: R/W**
	BOUND_RSDS	7	RSDS mode.	
	-	6	Reserved.	
	LVDS_LA_OEZ	5	LVDS_LA_OEZ.	
	LVDS_LB_OEZ	4	LVDS_LB_OEZ.	
	CK_OEZ	3	TTL-CK_OEZ.	
	DE_OEZ	2	TTL-DE_OEZ.	
	HS_OEZ	1	TTL-HS_OEZ.	
	VS_OEZ	0	TTL-VS_OEZ.	
45h (10328Bh)	**REG10328B**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	BOUNDING	1	Bonding.	
	BOUND_MINI	0	Mini-LVDS mode.	
46h (10328Ch)	**REG10328C**	**7:0**	**Default: 0x00**	**Access: R/W**
	EXT_DATA_EN[7:0]	7:0	External/ test bus enable mode for pair0~13.	
46h (10328Dh)	**REG10328D**	**7:0**	**Default: 0x00**	**Access: R/W**
	EXT_DATA_EN[15:8]	7:0	See description of '10328Ch'.	
47h (10328Eh)	**REG10328E**	**7:0**	**Default: 0x00**	**Access: R/W**
	EXT_DATA_EN[23:16]	7:0	See description of '10328Ch'.	
47h (10328Fh)	**REG10328F**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	EXT_DATA_EN[27:24]	3:0	See description of '10328Ch'.	
48h (103291h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
49h (103292h)	**REG103292**	**7:0**	**Default: 0x00**	**Access: R/W**
	MLX_METHOD[1:0]	7:6	Output format selection for TTL output. 10: 8-bit. 01: 6-bit. Others: 10-bit.	
	ERGX	5	Even channel red and green channel swap.	
	EGBX	4	Even channel green and blue channel swap.	
	ORGX	3	Odd channel red and green channel swap.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	OGBX	2	Odd channel green and blue channel swap.	
	-	1:0	Reserved.	
49h (103293h)	**REG103293**	**7:0**	**Default: 0x00**	**Access: R/W**
	GATE_DE	7	Output de gating.	
	EMLX	6	Even LSB and MSB swapping.	
	ERBX	5	Even channel red and blue channel swap.	
	OMLX	4	Odd LSB and MSB swapping.	
	ORBX	3	Odd channel red and blue channel swap.	
	OBN	2	Reserved.	
	WDG	1	Blanking time data become all 1.	
	REVL	0	Reverse output pix.	
4Ah (103294h)	**REG103294**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7	Reserved.	
	TTL_LVDS	6	TTL dual clock output.	
	CLKB_TC_REG	5	GPOA clock gating.	
	CLK_INVERT	4	Output clock invert.	
	VS_INVERT	3	Output Vsync invert.	
	DE_INVERT	2	Output DE invert.	
	DUALMODE	1	Dual LVDS channel selection.	
	ABSWITCH	0	Odd -even LVDS channel switch.	
4Ah (103295h)	**REG103295**	**7:0**	**Default: 0x00**	**Access: R/W**
	AUTOVS_EARLY	7	Auto Vsync early DE.	
	INTER_HS	6	Interlace Hsync.	
	INTERLACE_HS_GATE	5	Interlace Hsync gate.	
	HS_INVERT	4	Hsync invert.	
	HS_REMO	3	GPO or original Hsync selection.	
	OCP	2	TC clock invert 2.	
	ECP	1	TC clock invert 1.	
	PUA	0	VSYNC and CLOCK for TTL gating.	
4Bh (103296h)	**REG103296**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:3	Reserved.	
	MASK_TTL_DUAL	2	Mask dual channel de output.	
	TI_BITMODE[1:0]	1:0	TI bitmode.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			0x: 10-bit. 10: 8-bit. 11: 6-bit.	
4Ch (103298h)	**REG103298**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	CRC_EN	3	CRC testing enable.	
	CHANNEL_SEL[2:0]	2:0	CRC testing channel selection.	
4Dh (10329Ah)	**REG10329A**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_SEL[7:0]	7:0	General purpose output for pair0~13.	
4Dh (10329Bh)	**REG10329B**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_SEL[15:8]	7:0	See description of '10329Ah'.	
4Eh (10329Ch)	**REG10329C**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_SEL[23:16]	7:0	See description of '10329Ah'.	
4Eh (10329Dh)	**REG10329D**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	GPO_SEL[27:24]	3:0	See description of '10329Ah'.	
4Fh (10329Eh)	**REG10329E**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_DATAIN[7:0]	7:0	General purpose datain for pair0~13.	
4Fh (10329Fh)	**REG10329F**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_DATAIN[15:8]	7:0	See description of '10329Eh'.	
50h (1032A0h)	**REG1032A0**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_DATAIN[23:16]	7:0	See description of '10329Eh'.	
50h (1032A1h)	**REG1032A1**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	GPO_DATAIN[27:24]	3:0	See description of '10329Eh'.	
51h (1032A2h)	**REG1032A2**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_OEZ[7:0]	7:0	General purpose pad direction for pair0~13. 0: Output. 1: Input.	
51h (1032A3h)	**REG1032A3**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_OEZ[15:8]	7:0	See description of '1032A2h'.	
52h (1032A4h)	**REG1032A4**	**7:0**	**Default: 0x00**	**Access: R/W**
	GPO_OEZ[23:16]	7:0	See description of '1032A2h'.	
52h	**REG1032A5**	**7:0**	**Default: 0x00**	**Access: R/W**

MOD Register (Bank = 1032, Sub-bank = 00)

Index (Absolute)	Mnemonic	Bit	Description	
(1032A5h)	-	7:4	Reserved.	
	GPO_OEZ[27:24]	3:0	See description of '1032A2h'.	
53h (1032A7h)	**REG1032A7**	**7:0**	**Default: 0x00**	**Access: R/W**
	VBI_EN	7	VBI information on LVDS enable.	
	-	6:0	Reserved.	
54h (1032A8h)	**REG1032A8**	**7:0**	**Default: 0x00**	**Access: RO**
	CRC_OUT[7:0]	7:0	CRC testing result.	
54h (1032A9h)	**REG1032A9**	**7:0**	**Default: 0x00**	**Access: RO**
	CRC_OUT[15:8]	7:0	See description of '1032A8h'.	
55h (1032AAh)	**REG1032AA**	**7:0**	**Default: 0x00**	**Access: RO**
	MOD_GPI[7:0]	7:0	General purpose input for pair0~13.	
55h (1032ABh)	**REG1032AB**	**7:0**	**Default: 0x00**	**Access: RO**
	MOD_GPI[15:8]	7:0	See description of '1032AAh'.	
56h (1032ACh)	**REG1032AC**	**7:0**	**Default: 0x00**	**Access: RO**
	MOD_GPI[23:16]	7:0	See description of '1032AAh'.	
56h (1032ADh)	**REG1032AD**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:4	Reserved.	
	MOD_GPI[27:24]	3:0	See description of '1032AAh'.	
57h ~ 59h (1032AEh ~ 1032B3h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
5Ah (1032B5h)	**REG1032B5**	**7:0**	**Default: 0x00**	**Access: R/W**
	3D_CH3_EN_A	7	Enable 3d flag on LVDS channel A pair 3.	
	3D_CH4_EN_A	6	Enable 3d flag on LVDS channel A pair 4.	
	3D_CH3_EN_B	5	Enable 3d flag on LVDS channel B pair 3.	
	3D_CH4_EN_B	4	Enable 3d flag on LVDS channel B pair 4.	
	-	3:0	Reserved.	
6Ch (1032D9h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
6Dh (1032DAh)	**REG1032DA**	**7:0**	**Default: 0x00**	**Access: R/W**
	GCR_OUTCONF_CH3[1:0]	7:6	Output mode configuration for channel 3. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
			11: Test clock output mode.	
	GCR_OUTCONF_CH2[1:0]	5:4	Output mode configuration for channel 2. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH1[1:0]	3:2	Output mode configuration for channel 1. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH0[1:0]	1:0	Output mode configuration for channel 0. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
6Dh (1032DBh)	**REG1032DB**	**7:0**	**Default: 0x00**	**Access: R/W**
	GCR_OUTCONF_CH7[1:0]	7:6	Output mode configuration for channel 7. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH6[1:0]	5:4	Output mode configuration for channel 6. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH5[1:0]	3:2	Output mode configuration for channel 5. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH4[1:0]	1:0	Output mode configuration for channel 4. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
6Eh	**REG1032DC**	**7:0**	**Default: 0x00**	**Access: R/W**

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1032DCh)	GCR_OUTCONF_CH11[1:0]	7:6	Output mode configuration for channel 11. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH10[1:0]	5:4	Output mode configuration for channel 10. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH9[1:0]	3:2	Output mode configuration for channel 9. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH8[1:0]	1:0	Output mode configuration for channel 8. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
6Eh (1032DDh)	**REG1032DD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	GCR_OUTCONF_CH13[1:0]	3:2	Output mode configuration for channel 13. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
	GCR_OUTCONF_CH12[1:0]	1:0	Output mode configuration for channel 12. 00: TTL mode/Standby mode. 01: LVDS/EPI/RSDS/mini-LVDS data output mode. 10: RSDS/mini-LVDS clock output mode. 11: Test clock output mode.	
71h (1032E2h)	**REG1032E2**	**7:0**	**Default: 0x00**	**Access: R/W**
	GCR_PE_EN_CH[7:0]	7:0	Differential output pre-emphasis enable for channel [13:0].	
71h (1032E3h)	**REG1032E3**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GCR_PE_EN_CH[13:8]	5:0	See description of '1032E2h'.	

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
73h (1032E6h)	**REG1032E6**	**7:0**	**Default: 0x00**	**Access: R/W**
	GCR_DS_POL_CH[7:0]	7:0	Differential output polarity swap for channel [13:0].	
73h (1032E7h)	**REG1032E7**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GCR_DS_POL_CH[13:8]	5:0	See description of '1032E6h'.	
75h (1032EAh)	**REG1032EA**	**7:0**	**Default: 0x00**	**Access: R/W**
	GCR_EN_RINT_CH[7:0]	7:0	Internal resistor enable.	
75h (1032EBh)	**REG1032EB**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	GCR_EN_RINT_CH[13:8]	5:0	See description of '1032EAh'.	
77h (1032EEh)	**REG1032EE**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	EN_CK_PC	3	Part C LVDS/EPI clock enable. This pin is used for CH8~CH13.	
	EN_CK_PB	2	Part B LVDS/EPI clock enable. This pin is used for CH2~CH7.	
	EN_CK_PA	1	Part A LVDS/EPI clock enable. This pin is used for CH0~CH1.	
	GCR_CKEN	0	Part A, B, C LVDS/EPI clock enable. This pin is used for CH0~CH13.	
77h (1032EFh)	**REG1032EF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	EN_SKEWCLK_PA	1	Part A RSDS/mini-LVDS clock enable. This pin is used for CH.	
	EN_SKEWCLK_PB	0	Part B RSDS/mini-LVDS clock enable. This pin is used for CH.	
78h (1032F0h)	**REG1032F0**	**7:0**	**Default: 0xF1**	**Access: R/W**
	GCR_PD_REG_A	7	Power down regulator for CH0~6.	
	GCR_PD_REG_B	6	Power down regulator for CH7~13.	
	GCR_PD_REG_A_DRV	5	Power down regulator for CH0~6 Driver.	
	GCR_PD_REG_B_DRV	4	Power down regulator for CH7~13 Driver.	
	-	3:1	Reserved.	
	PD_IB_MOD	0	Power down mod bias current source.	
78h ~ 79h	**-**	**7:0**	**Default: -**	**Access: -**

MOD Register (Bank = 1032, Sub-bank = 00)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1032F1h ~ 1032F3h)	-	-	Reserved.	
7Bh (1032F6h)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
7Dh (1032FAh)	**REG1032FA**	**7:0**	**Default: 0x00**	**Access: R/W**
	GCR_CAL_EN	7	Enable calibration function.	
	-	6:3	Reserved.	
	GCR_CAL_SRC	2	Select calibration source pair. 0: Pair6 (PAD_G_ODD[7]/PAD_G_ODD[6]). 1: Pair9 (PAD_G_ODD[1]/PAD_G_ODD[0]).	
	GCR_CAL_LEVEL[1:0]	1:0	Select calibration target voltage. Select calibration target voltage. 00: 239mV. 01: 335mV. 10: 287mV. 11: 201mV.	
7Dh (1032FBh)	**REG1032FB**	**7:0**	**Default: 0x00**	**Access: RO**
	-	7:1	Reserved.	
	C_CAL_OUT	0	Calibration result output. 1: Higher than target. 0: Lower than target.	

PWM Register (Bank = 1032, Sub-bank = 01)

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
02h (103204h)	**REG103204**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM0_PERIOD[7:0]	7:0	PWM0 period.	
02h (103205h)	**REG103205**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM0_PERIOD[15:8]	7:0	See description of '103204h'.	
03h (103206h)	**REG103206**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM0_DUTY[7:0]	7:0	PWM0 duty.	
03h (103207h)	**REG103207**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM0_DUTY[15:8]	7:0	See description of '103206h'.	
04h (103208h)	**REG103208**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM0_DIV[7:0]	7:0	PWM0 divider.	
04h (103209h)	**REG103209**	**7:0**	**Default: 0x40**	**Access: R/W**
	-	7	Reserved.	
	PWM0_VDBEN_SW	6	PWM0 Vsync double buffer enable by software. 1: Enable. 0: Disable.	
	-	5:4	Reserved.	
	PWM0_DBEN	3	PWM0 double buffer enable.	
	PWM0_RESET_EN	2	PWM0 Vsync reset0.	
	PWM0_VDBEN	1	PWM0 Vsync double buffer enable.	
	PWM0_POLARITY	0	PWM0 polarity.	
05h (10320Ah)	**REG10320A**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM1_PERIOD[7:0]	7:0	PWM1 period.	
05h (10320Bh)	**REG10320B**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM1_PERIOD[15:8]	7:0	See description of '10320Ah'.	
06h (10320Ch)	**REG10320C**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM1_DUTY[7:0]	7:0	PWM1 duty.	
06h (10320Dh)	**REG10320D**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM1_DUTY[15:8]	7:0	See description of '10320Ch'.	
07h (10320Eh)	**REG10320E**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM1_DIV[7:0]	7:0	PWM1 divider.	
07h (10320Fh)	**REG10320F**	**7:0**	**Default: 0x40**	**Access: R/W**
	-	7	Reserved.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM1_VDBEN_SW	6	PWM1 Vsync double buffer enable by software. 1: Enable. 0: Disable.	
	-	5:4	Reserved.	
	PWM1_DBEN	3	PWM1 double buffer enable.	
	PWM1_RESET_EN	2	PWM1 Vsync reset1.	
	PWM1_VDBEN	1	PWM1 Vsync double buffer enable.	
	PWM1_POLARITY	0	PWM1 polarity.	
08h (103210h)	**REG103210**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM2_PERIOD[7:0]	7:0	PWM2 period.	
08h (103211h)	**REG103211**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM2_PERIOD[15:8]	7:0	See description of '103210h'.	
09h (103212h)	**REG103212**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM2_DUTY[7:0]	7:0	PWM2 duty.	
09h (103213h)	**REG103213**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM2_DUTY[15:8]	7:0	See description of '103212h'.	
0Ah (103214h)	**REG103214**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM2_DIV[7:0]	7:0	PWM2 divider.	
0Ah (103215h)	**REG103215**	**7:0**	**Default: 0x40**	**Access: R/W**
	-	7	Reserved.	
	PWM2_VDBEN_SW	6	PWM2 Vsync double buffer enable by software. 1: Enable. 0: Disable.	
	-	5:4	Reserved.	
	PWM2_DBEN	3	PWM2 double buffer enable.	
	PWM2_RESET_EN	2	PWM2 Vsync reset2.	
	PWM2_VDBEN	1	PWM2 Vsync double buffer enable.	
	PWM2_POLARITY	0	PWM2 polarity.	
0Bh (103216h)	**REG103216**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_PERIOD[7:0]	7:0	PWM3 period.	
0Bh (103217h)	**REG103217**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_PERIOD[15:8]	7:0	See description of '103216h'.	
0Ch (103218h)	**REG103218**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_DUTY[7:0]	7:0	PWM3 duty.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
0Ch (103219h)	**REG103219**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_DUTY[15:8]	7:0	See description of '103218h'.	
0Dh (10321Ah)	**REG10321A**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_DIV[7:0]	7:0	PWM3 divider.	
0Dh (10321Bh)	**REG10321B**	**7:0**	**Default: 0x40**	**Access: R/W**
	-	7	Reserved.	
	PWM3_VDBEN_SW	6	PWM3 Vsync double buffer enable by software. 1: Enable. 0: Disable.	
	-	5:4	Reserved.	
	PWM3_DBEN	3	PWM3 double buffer enable.	
	PWM3_RESET_EN	2	PWM3 Vsync reset3.	
	PWM3_VDBEN	1	PWM3 Vsync double buffer enable.	
	PWM3_POLARITY	0	PWM3 polarity.	
0Eh (10321Ch)	**REG10321C**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM4_PERIOD[7:0]	7:0	PWM4 period.	
0Eh (10321Dh)	**REG10321D**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM4_PERIOD[15:8]	7:0	See description of '10321Ch'.	
0Fh (10321Eh)	**REG10321E**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM4_DUTY[7:0]	7:0	PWM4 duty.	
0Fh (10321Fh)	**REG10321F**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM4_DUTY[15:8]	7:0	See description of '10321Eh'.	
10h (103220h)	**REG103220**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM4_DIV[7:0]	7:0	PWM4 divider.	
10h (103221h)	**REG103221**	**7:0**	**Default: 0x40**	**Access: R/W**
	-	7	Reserved.	
	PWM4_VDBEN_SW	6	PWM4 Vsync double buffer enable by software. 1: Enable. 0: Disable.	
	-	5:4	Reserved.	
	PWM4_DBEN	3	PWM4 double buffer enable.	
	PWM4_RESET_EN	2	PWM4 Vsync reset4.	
	PWM4_VDBEN	1	PWM4 Vsync double buffer enable.	
	PWM4_POLARITY	0	PWM4 polarity.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
11h (103222h)	**REG103222**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5_PERIOD[7:0]	7:0	PWM5 period.	
11h (103223h)	**REG103223**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5_PERIOD[15:8]	7:0	See description of '103222h'.	
12h (103224h)	**REG103224**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5_DUTY[7:0]	7:0	PWM5 duty.	
12h (103225h)	**REG103225**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5_DUTY[15:8]	7:0	See description of '103224h'.	
13h (103226h)	**REG103226**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5_DIV[7:0]	7:0	PWM5 divider.	
13h (103227h)	**REG103227**	**7:0**	**Default: 0x40**	**Access: R/W**
	-	7	Reserved.	
	PWM5_VDBEN_SW	6	PWM5 Vsync double buffer enable by software. 1: Enable. 0: Disable.	
	-	5:4	Reserved.	
	PWM5_DBEN	3	PWM5 double buffer enable.	
	PWM5_RESET_EN	2	PWM5 Vsync reset5.	
	PWM5_VDBEN	1	PWM5 Vsync double buffer enable.	
	PWM5_POLARITY	0	PWM5 polarity.	
14h (103228h)	**REG103228**	**7:0**	**Default: 0x00**	**Access: R/W**
	RST_MUX1	7	PWM1 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT1[3:0]	3:0	PWM1 Hsync reset counter.	
14h (103229h)	**REG103229**	**7:0**	**Default: 0x00**	**Access: R/W**
	RST_MUX0	7	PWM0 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT0[3:0]	3:0	PWM0 Hsync reset counter.	
15h (10322Ah)	**REG10322A**	**7:0**	**Default: 0x00**	**Access: R/W**
	RST_MUX3	7	PWM3 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT3[3:0]	3:0	PWM3 Hsync reset counter.	
15h	**REG10322B**	**7:0**	**Default: 0x00**	**Access: R/W**

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10322Bh)	RST_MUX2	7	PWM2 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT2[3:0]	3:0	PWM2 Hsync reset counter.	
16h (10322Ch)	**REG10322C**	**7:0**	**Default: 0x00**	**Access: R/W**
	RST_MUX5	7	PWM5 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT5[3:0]	3:0	PWM5 Hsync reset counter.	
16h (10322Dh)	**REG10322D**	**7:0**	**Default: 0x00**	**Access: R/W**
	RST_MUX4	7	PWM4 reset mux.	
	-	6:4	Reserved.	
	HS_RST_CNT4[3:0]	3:0	PWM4 Hsync reset counter.	
17h ~ 1Fh (10322Eh ~ 10323Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
20h (103240h)	**REG103240**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_PERIOD_EXT[1:0]	7:6	PWM3 extra 2-bit period setting.	
	PWM2_PERIOD_EXT[1:0]	5:4	PWM2 extra 2-bit period setting.	
	PWM1_PERIOD_EXT[1:0]	3:2	PWM1 extra 2-bit period setting.	
	PWM0_PERIOD_EXT[1:0]	1:0	PWM0 extra 2-bit period setting.	
20h (103241h)	**REG103241**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PWM5_PERIOD_EXT[1:0]	3:2	PWM5 extra 2-bit period setting.	
	PWM4_PERIOD_EXT[1:0]	1:0	PWM4 extra 2-bit period setting.	
21h (103242h)	**REG103242**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_DUTY_EXT[1:0]	7:6	PWM3 extra 2-bit duty setting.	
	PWM2_DUTY_EXT[1:0]	5:4	PWM2 extra 2-bit duty setting.	
	PWM1_DUTY_EXT[1:0]	3:2	PWM1 extra 2-bit duty setting.	
	PWM0_DUTY_EXT[1:0]	1:0	PWM0 extra 2-bit duty setting.	
21h (103243h)	**REG103243**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	PWM5_DUTY_EXT[1:0]	3:2	PWM5 extra 2-bit duty setting.	
	PWM4_DUTY_EXT[1:0]	1:0	PWM4 extra 2-bit duty setting.	
22h	**REG103244**	**7:0**	**Default: 0x00**	**Access: R/W**

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(103244h)	PWM0_DIV_EXT[7:0]	7:0	PWM0 extra 8-bit divider setting.	
22h (103245h)	**REG103245**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM1_DIV_EXT[7:0]	7:0	PWM1 extra 8-bit divider setting.	
23h (103246h)	**REG103246**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM2_DIV_EXT[7:0]	7:0	PWM2 extra 8-bit divider setting.	
23h (103247h)	**REG103247**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_DIV_EXT[7:0]	7:0	PWM3 extra 8-bit divider setting.	
24h (103248h)	**REG103248**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM4_DIV_EXT[7:0]	7:0	PWM4 extra 8-bit divider setting.	
24h (103249h)	**REG103249**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5_DIV_EXT[7:0]	7:0	PWM5 extra 8-bit divider setting.	
28h (103250h)	**REG103250**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM0_SHIFT[7:0]	7:0	PWM0 rising point shift counter.	
28h (103251h)	**REG103251**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM0_SHIFT[15:8]	7:0	See description of '103250h'.	
29h (103252h)	**REG103252**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	PWM0_SHIFT[17:16]	1:0	See description of '103250h'.	
2Ah (103254h)	**REG103254**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM1_SHIFT[7:0]	7:0	PWM1 rising point shift counter.	
2Ah (103255h)	**REG103255**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM1_SHIFT[15:8]	7:0	See description of '103254h'.	
2Bh (103256h)	**REG103256**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	PWM1_SHIFT[17:16]	1:0	See description of '103254h'.	
2Ch (103258h)	**REG103258**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM2_SHIFT[7:0]	7:0	PWM2 rising point shift counter.	
2Ch (103259h)	**REG103259**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM2_SHIFT[15:8]	7:0	See description of '103258h'.	
2Dh (10325Ah)	**REG10325A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	PWM2_SHIFT[17:16]	1:0	See description of '103258h'.	
2Eh	**REG10325C**	**7:0**	**Default: 0x00**	**Access: R/W**

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(10325Ch)	PWM3_SHIFT[7:0]	7:0	PWM3 rising point shift counter.	
2Eh (10325Dh)	**REG10325D**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM3_SHIFT[15:8]	7:0	See description of '10325Ch'.	
2Fh (10325Eh)	**REG10325E**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	PWM3_SHIFT[17:16]	1:0	See description of '10325Ch'.	
30h (103260h)	**REG103260**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM4_SHIFT[7:0]	7:0	PWM4 rising point shift counter.	
30h (103261h)	**REG103261**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM4_SHIFT[15:8]	7:0	See description of '103260h'.	
31h (103262h)	**REG103262**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	PWM4_SHIFT[17:16]	1:0	See description of '103260h'.	
32h (103264h)	**REG103264**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5_SHIFT[7:0]	7:0	PWM5 rising point shift counter.	
32h (103265h)	**REG103265**	**7:0**	**Default: 0x00**	**Access: R/W**
	PWM5_SHIFT[15:8]	7:0	See description of '103264h'.	
33h (103266h)	**REG103266**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:2	Reserved.	
	PWM5_SHIFT[17:16]	1:0	See description of '103264h'.	
34h (103268h)	**REG103268**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	NVS_RST_EN5	5	PWM5 enable NVSYNC reset function.	
	NVS_RST_EN4	4	PWM4 enable NVSYNC reset function.	
	NVS_RST_EN3	3	PWM3 enable NVSYNC reset function.	
	NVS_RST_EN2	2	PWM2 enable NVSYNC reset function.	
	NVS_RST_EN1	1	PWM1 enable NVSYNC reset function.	
	NVS_RST_EN0	0	PWM0 enable NVSYNC reset function.	
34h (103269h)	**REG103269**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	NVS_ALIGN_INV5	5	PWM5 select NVSYNC align with left flag inv. 0: Align with left. 1: Align with right.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	NVS_ALIGN_INV4	4	PWM4 select NVSYNC align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV3	3	PWM3 select NVSYNC align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV2	2	PWM2 select NVSYNC align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV1	1	PWM1 select NVSYNC align with left flag inv. 0: Align with left. 1: Align with right.	
	NVS_ALIGN_INV0	0	PWM0 select NVSYNC align with left flag inv. 0: Align with left. 1: Align with right.	
35h (10326Ah)	**REG10326A**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	NVS_ALIGN_EN5	5	PWM5 enable NVSYNC align left flag function.	
	NVS_ALIGN_EN4	4	PWM4 enable NVSYNC align left flag function.	
	NVS_ALIGN_EN3	3	PWM3 enable NVSYNC align left flag function.	
	NVS_ALIGN_EN2	2	PWM2 enable NVSYNC align left flag function.	
	NVS_ALIGN_EN1	1	PWM1 enable NVSYNC align left flag function.	
	NVS_ALIGN_EN0	0	PWM0 enable NVSYNC align left flag function.	
36h ~ 37h (10326Ch ~ 10326Fh)	**-**	**7:0**	**Default: -**	**Access: -**
	-	-	Reserved.	
54h (1032A8h)	**REG1032A8**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM0_HIT_CNT_ST[7:0]	7:0	PWM0 period hit count start for mask.	
54h (1032A9h)	**REG1032A9**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM0_EN_MASK	7	PWM0 mask enable.	
	-	6:4	Reserved.	
	PWM0_HIT_CNT_ST[11:8]	3:0	See description of '1032A8h'.	
55h (1032AAh)	**REG1032AA**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM0_HIT_CNT_END[7:0]	7:0	PWM0 period hit count end for mask.	
55h	**REG1032AB**	**7:0**	**Default: 0x0F**	**Access: R/W**

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
(1032ABh)	-	7:4	Reserved.	
	PWM0_HIT_CNT_END[11:8]	3:0	See description of '1032AAh'.	
56h (1032ACh)	**REG1032AC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM1_HIT_CNT_ST[7:0]	7:0	PWM1 period hit count start for mask.	
56h (1032ADh)	**REG1032AD**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM1_EN_MASK	7	PWM1 mask enable.	
	-	6:4	Reserved.	
	PWM1_HIT_CNT_ST[11:8]	3:0	See description of '1032ACh'.	
57h (1032AEh)	**REG1032AE**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM1_HIT_CNT_END[7:0]	7:0	PWM1 period hit count end for mask.	
57h (1032AFh)	**REG1032AF**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM1_HIT_CNT_END[11:8]	3:0	See description of '1032AEh'.	
58h (1032B0h)	**REG1032B0**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM2_HIT_CNT_ST[7:0]	7:0	PWM2 period hit count start for mask.	
58h (1032B1h)	**REG1032B1**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM2_EN_MASK	7	PWM2 mask enable.	
	-	6:4	Reserved.	
	PWM2_HIT_CNT_ST[11:8]	3:0	See description of '1032B0h'.	
59h (1032B2h)	**REG1032B2**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM2_HIT_CNT_END[7:0]	7:0	PWM2 period hit count end for mask.	
59h (1032B3h)	**REG1032B3**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM2_HIT_CNT_END[11:8]	3:0	See description of '1032B2h'.	
5Ah (1032B4h)	**REG1032B4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM3_HIT_CNT_ST[7:0]	7:0	PWM3 period hit count start for mask.	
5Ah (1032B5h)	**REG1032B5**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM3_EN_MASK	7	PWM3 mask enable.	
	-	6:4	Reserved.	
	PWM3_HIT_CNT_ST[11:8]	3:0	See description of '1032B4h'.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
5Bh (1032B6h)	**REG1032B6**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM3_HIT_CNT_END[7:0]	7:0	PWM3 period hit count end for mask.	
5Bh (1032B7h)	**REG1032B7**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM3_HIT_CNT_END[11:8]	3:0	See description of '1032B6h'.	
5Ch (1032B8h)	**REG1032B8**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM4_HIT_CNT_ST[7:0]	7:0	PWM4 period hit count start for mask.	
5Ch (1032B9h)	**REG1032B9**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM4_EN_MASK	7	PWM4 mask enable.	
	-	6:4	Reserved.	
	PWM4_HIT_CNT_ST[11:8]	3:0	See description of '1032B8h'.	
5Dh (1032BAh)	**REG1032BA**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM4_HIT_CNT_END[7:0]	7:0	PWM4period hit count end for mask.	
5Dh (1032BBh)	**REG1032BB**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM4_HIT_CNT_END[11:8]	3:0	See description of '1032BAh'.	
5Eh (1032BCh)	**REG1032BC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM5_HIT_CNT_ST[7:0]	7:0	PWM5 period hit count start for mask.	
5Eh (1032BDh)	**REG1032BD**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM5_EN_MASK	7	PWM5 mask enable.	
	-	6:4	Reserved.	
	PWM5_HIT_CNT_ST[11:8]	3:0	See description of '1032BCh'.	
5Fh (1032BEh)	**REG1032BE**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM5_HIT_CNT_END[7:0]	7:0	PWM5 period hit count end for mask.	
5Fh (1032BFh)	**REG1032BF**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM5_HIT_CNT_END[11:8]	3:0	See description of '1032BEh'.	
64h (1032C8h)	**REG1032C8**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	PWM5_LEFT_MASK	5	PWM5 mask left enable.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	PWM4_LEFT_MASK	4	PWM4 mask left enable.	
	PWM3_LEFT_MASK	3	PWM3 mask left enable.	
	PWM2_LEFT_MASK	2	PWM2 mask left enable.	
	PWM1_LEFT_MASK	1	PWM1 mask left enable.	
	PWM0_LEFT_MASK	0	PWM0 mask left enable.	
65h (1032CAh)	**REG1032CA**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:6	Reserved.	
	PWM5_INV_LEFT	5	Inverse left_input for right of PWM5.	
	PWM4_INV_LEFT	4	Inverse left_input for right of PWM4.	
	PWM3_INV_LEFT	3	Inverse left_input for right of PWM3.	
	PWM2_INV_LEFT	2	Inverse left_input for right of PWM2.	
	PWM1_INV_LEFT	1	Inverse left_input for right of PWM1.	
	PWM0_INV_LEFT	0	Inverse left_input for right of PWM0.	
66h (1032CCh)	**REG1032CC**	**7:0**	**Default: 0x00**	**Access: R/W**
	EN_FP_L_INT3	7	Enable falling pulse interrupt of PWM3 of left.	
	EN_RP_L_INT3	6	Enable rising pulse interrupt of PWM3 of left.	
	EN_FP_L_INT2	5	Enable falling pulse interrupt of PWM2 of left.	
	EN_RP_L_INT2	4	Enable rising pulse interrupt of PWM2 of left.	
	EN_FP_L_INT1	3	Enable falling pulse interrupt of PWM1 of left.	
	EN_RP_L_INT1	2	Enable rising pulse interrupt of PWM1 of left.	
	EN_FP_L_INT0	1	Enable falling pulse interrupt of PWM0 of left.	
	EN_RP_L_INT0	0	Enable rising pulse interrupt of PWM0 of left.	
66h (1032CDh)	**REG1032CD**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	EN_FP_L_INT5	3	Enable falling pulse interrupt of PWM5 of left.	
	EN_RP_L_INT5	2	Enable rising pulse interrupt of PWM5 of left.	
	EN_FP_L_INT4	1	Enable falling pulse interrupt of PWM4 of left.	
	EN_RP_L_INT4	0	Enable rising pulse interrupt of PWM4 of left.	
67h (1032CEh)	**REG1032CE**	**7:0**	**Default: 0x00**	**Access: R/W**
	EN_FP_R_INT3	7	Enable falling pulse interrupt of PWM3 of right.	
	EN_RP_R_INT3	6	Enable rising pulse interrupt of PWM3 of right.	
	EN_FP_R_INT2	5	Enable falling pulse interrupt of PWM2 of right.	
	EN_RP_R_INT2	4	Enable rising pulse interrupt of PWM2 of right.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
	EN_FP_R_INT1	3	Enable falling pulse interrupt of PWM1 of right.	
	EN_RP_R_INT1	2	Enable rising pulse interrupt of PWM1 of right.	
	EN_FP_R_INT0	1	Enable falling pulse interrupt of PWM0 of right.	
	EN_RP_R_INT0	0	Enable rising pulse interrupt of PWM0 of right.	
67h (1032CFh)	**REG1032CF**	**7:0**	**Default: 0x00**	**Access: R/W**
	-	7:4	Reserved.	
	EN_FP_R_INT5	3	Enable falling pulse interrupt of PWM5 of right.	
	EN_RP_R_INT5	2	Enable rising pulse interrupt of PWM5 of right.	
	EN_FP_R_INT4	1	Enable falling pulse interrupt of PWM4 of right.	
	EN_RP_R_INT4	0	Enable rising pulse interrupt of PWM4 of right.	
68h (1032D0h)	**REG1032D0**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM0_HIT_CNT_ST2[7:0]	7:0	PWM0 period hit count start for mask2.	
68h (1032D1h)	**REG1032D1**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM0_EN_LR_MASK	7	PWM0 LR mask enable.	
	-	6:4	Reserved.	
	PWM0_HIT_CNT_ST2[11:8]	3:0	See description of '1032D0h'.	
69h (1032D2h)	**REG1032D2**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM0_HIT_CNT_END2[7:0]	7:0	PWM0 period hit count end for mask2.	
69h (1032D3h)	**REG1032D3**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM0_HIT_CNT_END2[11:8]	3:0	See description of '1032D2h'.	
6Ah (1032D4h)	**REG1032D4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM1_HIT_CNT_ST2[7:0]	7:0	PWM1 period hit count start for mask2.	
6Ah (1032D5h)	**REG1032D5**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM1_EN_LR_MASK	7	PWM1 LR mask enable.	
	-	6:4	Reserved.	
	PWM1_HIT_CNT_ST2[11:8]	3:0	See description of '1032D4h'.	
6Bh (1032D6h)	**REG1032D6**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM1_HIT_CNT_END2[7:0]	7:0	PWM1 period hit count end for mask2.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
6Bh (1032D7h)	**REG1032D7**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM1_HIT_CNT_END2[11:8]	3:0	See description of '1032D6h'.	
6Ch (1032D8h)	**REG1032D8**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM2_HIT_CNT_ST2[7:0]	7:0	PWM2 period hit count start for mask2.	
6Ch (1032D9h)	**REG1032D9**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM2_EN_LR_MASK	7	PWM2 LR mask enable.	
	-	6:4	Reserved.	
	PWM2_HIT_CNT_ST2[11:8]	3:0	See description of '1032D8h'.	
6Dh (1032DAh)	**REG1032DA**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM2_HIT_CNT_END2[7:0]	7:0	PWM2 period hit count end for mask2.	
6Dh (1032DBh)	**REG1032DB**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM2_HIT_CNT_END2[11:8]	3:0	See description of '1032DAh'.	
6Eh (1032DCh)	**REG1032DC**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM3_HIT_CNT_ST2[7:0]	7:0	PWM3 period hit count start for mask2.	
6Eh (1032DDh)	**REG1032DD**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM3_EN_LR_MASK	7	PWM3 LR mask enable.	
	-	6:4	Reserved.	
	PWM3_HIT_CNT_ST2[11:8]	3:0	See description of '1032DCh'.	
6Fh (1032DEh)	**REG1032DE**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM3_HIT_CNT_END2[7:0]	7:0	PWM3 period hit count end for mask2.	
6Fh (1032DFh)	**REG1032DF**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM3_HIT_CNT_END2[11:8]	3:0	See description of '1032DEh'.	
70h (1032E0h)	**REG1032E0**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM4_HIT_CNT_ST2[7:0]	7:0	PWM4 period hit count start for mask2.	

PWM Register (Bank = 1032, Sub-bank = 01)				
Index (Absolute)	**Mnemonic**	**Bit**	**Description**	
70h (1032E1h)	**REG1032E1**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM4_EN_LR_MASK	7	PWM4 LR mask enable.	
	-	6:4	Reserved.	
	PWM4_HIT_CNT_ST2[11:8]	3:0	See description of '1032E0h'.	
71h (1032E2h)	**REG1032E2**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM4_HIT_CNT_END2[7:0]	7:0	PWM4 period hit count end for mask2.	
71h (1032E3h)	**REG1032E3**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM4_HIT_CNT_END2[11:8]	3:0	See description of '1032E2h'.	
72h (1032E4h)	**REG1032E4**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM5_HIT_CNT_ST2[7:0]	7:0	PWM5 period hit count start for mask2.	
72h (1032E5h)	**REG1032E5**	**7:0**	**Default: 0x0F**	**Access: R/W**
	PWM5_EN_LR_MASK	7	PWM5 LR mask enable.	
	-	6:4	Reserved.	
	PWM5_HIT_CNT_ST2[11:8]	3:0	See description of '1032E4h'.	
73h (1032E6h)	**REG1032E6**	**7:0**	**Default: 0xFF**	**Access: R/W**
	PWM5_HIT_CNT_END2[7:0]	7:0	PWM5 period hit count end for mask2.	
73h (1032E7h)	**REG1032E7**	**7:0**	**Default: 0x0F**	**Access: R/W**
	-	7:4	Reserved.	
	PWM5_HIT_CNT_END2[11:8]	3:0	See description of '1032E6h'.	
78h (1032F1h)	**REG1032F1**	**7:0**	**Default: 0x00**	**Access: R/W**
	INV_3D_FLAG	7	Inverse 3D flag.	
	-	6:0	Reserved.	

REGISTER TABLE REVISION HISTORY

Date	Bank	Register
07/22/2010		• Created first version.