

File No		 Repair guide	It intends to compile	Deng Yizheng
Maintanence project	S9 Arithmetic board		Check	
File Version	V 1.8	Century cloud core	date: 2016.12.28	Approve

The first **6** book

Altogether **20** page

File Type: Maintenance Program

This book content: focuses on **S9** Various arithmetic board fault investigation, how accurate positioning with the test cassette.

: Suitable for all **S9** Production, sale, outsourcing maintenance of the site

A maintenance platform requirements :

1 , Heated iron (350 degree- 400 degree), Pointed tip for welding and other small SMD chip resistor capacitor.

2 , Hot hairdryer for welding die disassembly, be careful not to avoid prolonged heating PCB foaming.

3 , APW3 power (Export 12V , 133A Max), Board testing for calculation using measured.

4 ,multimeter , Tweezers , S9 Test the rule (Conditions can be configured oscilloscope) .

5 Flux, washer water plus ethanol ; Washer water for cleaning flux residues and the appearance after repair.

6 , Sik tin fixtures , Tin steel plant , Paste ; Replacement of the chip , We must give the chip plant tin.

7 , Thermal plastic Black (3461) , After re-glue fins for servicing.

two, Job Requirements :

1, maintenance staff must have some knowledge of electronics , More than one year of maintenance experience , QFN package of welding skill mastered.

2, after the maintenance operation panel to be tested are more than twice as OK , Only by !

3, pay attention to work practices when replacing chip , After replacing any parts of PCB no significant deformation, replacement parts and checking whether a neighboring member less open shortest path problem.

4, to determine a respective object position repairman test software parameters, test the rule.

5. Check tool , Whether the rule can work

Third, the principle and structure:

- Principles outlined

1. **S9** by twenty one Voltage domain in series , Each domain has a voltage 3 Stars BM1387 chip , Total full board 63 Stars BM1387 chip.

2. **BM1387** Buck diode chip built , Chip pins is specified with the buck diode function.

3. **S9** Yes twenty one Voltage domain (S5 + Yes 16 Voltage domain, S7 54 Chip 18 Voltage domain, S7 45 The chip is 15 Voltage domain); S9 clock 25M Single crystal , In series by The first 1 A chip pass to the last one chip .

4. **S9** Each chip has its own small positive and negative heat sink , Front fins is small SMT placement, the back surface is small at the beginning of the plate fin heat conductive adhesive after the test fixed to the back by IC. Repair and replacement chip test After the test by the need evenly black thermal plastic IC surface, and heat-fixed.

have to be aware of is :

During maintenance , When the plate member, or the replacement chip , In order to reduce the temperature of the air gun PCB Board and chip damage , Required small fins near the first defective elements , and PCB After the back surface of the small plate fin taken down , Then replaced.

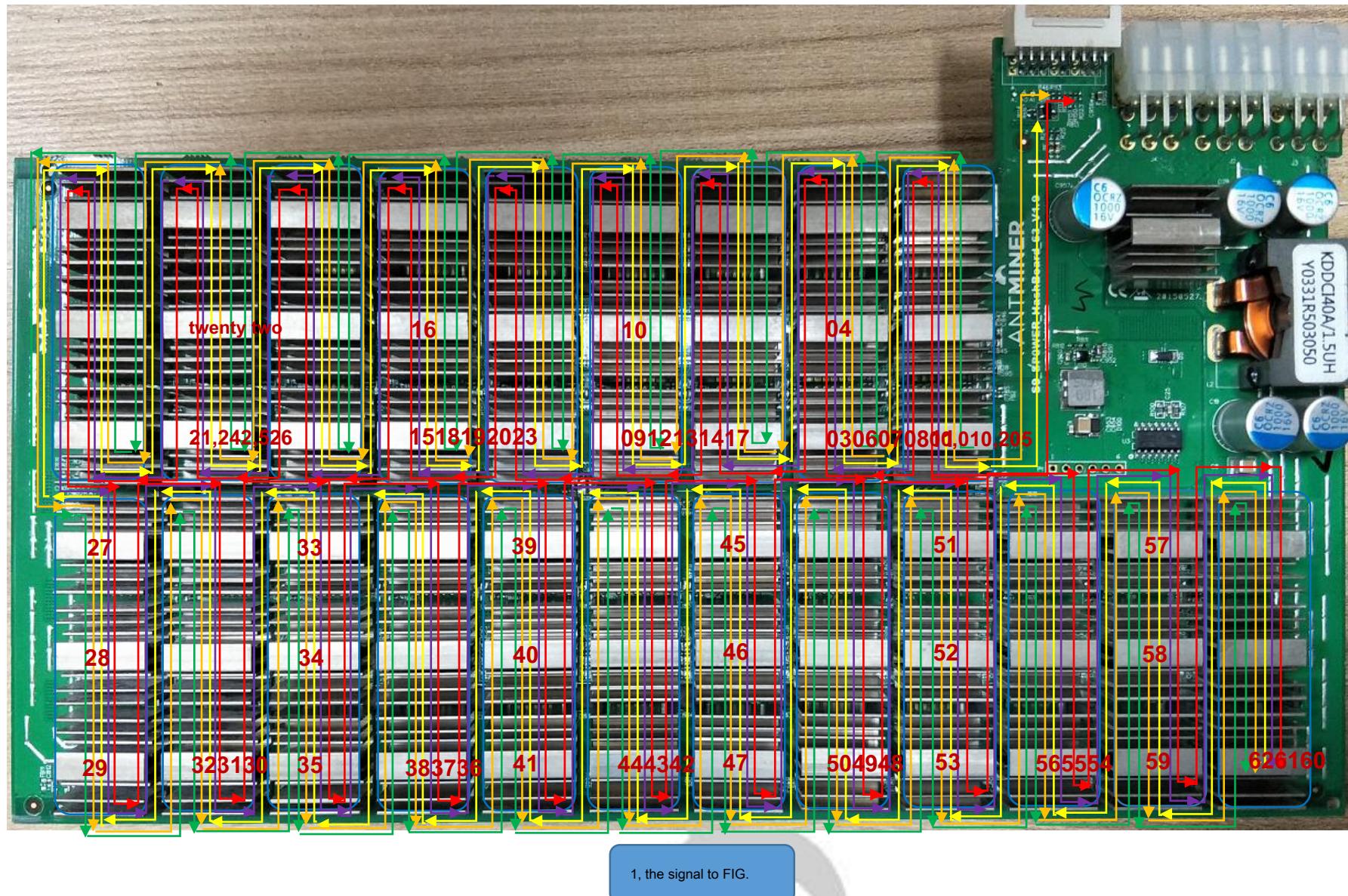
PCB Anyway, we have a positive board test points , When maintenance of production , in PCB A heat sink is not affixed to the front , Use positive test points ; Finished repair (Repairs), due to PCB The positive and negative heat sink are covered , Required by PCB

Test point fault location, purpose-built elongated leads probe into the fin gap measurement, but the SMT small fins contact a respective voltage domain, the so measured, to be noted that insulating lead to avoid lead shorting. .

- The key point analysis:

1, the signal S9 below shows a schematic view of the signal plate to:

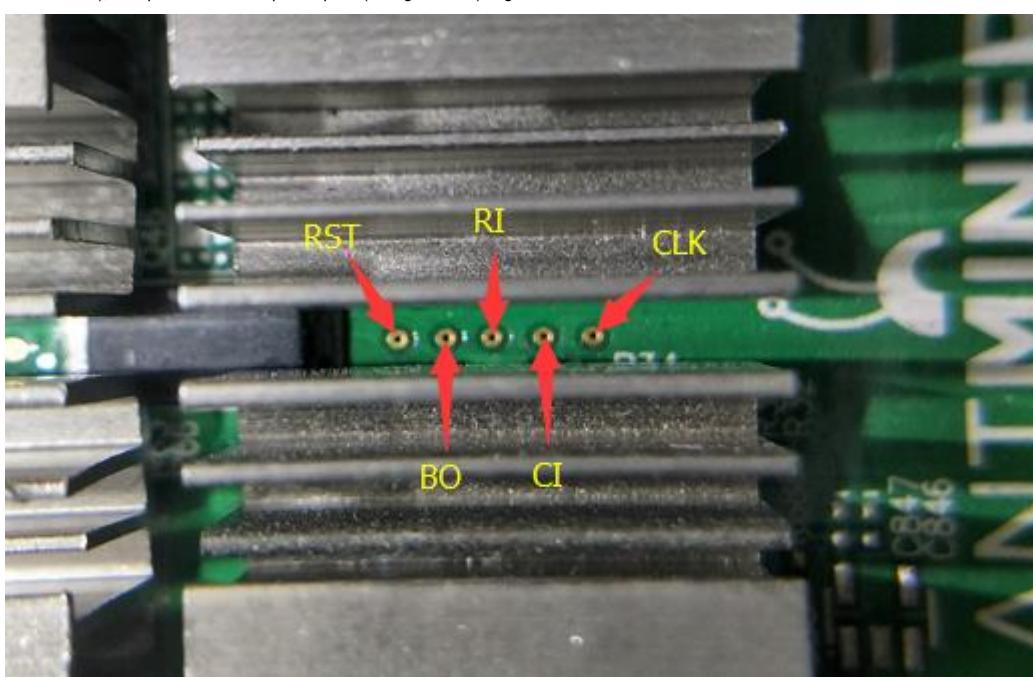
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- Green → Green CLK Signal flow from Y1 25M Crystal generated from 00 No. chips to 62 No. transmission chip; standby operational voltage are both 0.9V .
 - Orange → Orange is TX (CI , CO) Signal flow, from IO mouth 1 Foot forward, then by 00 No. chips to 62 No. transmission chip; unplugged IO When signal line voltage 0 When operation voltage 1.8V .
 - Yellow ← Yellow RX (RI , RO) Signal flow, from the 62 No. chips to 00 No. chip returned, and then from IO mouth 12 Return foot board; not plugged IO When the signal line voltage is 1.8V , Operations When the voltage is 1.8V
 - Purple → Purple is B (BI , BO) Signal flow, from the 00 No. chips to 62 Pulled low; no plug IO When the signal line, when the standby 0V When operation is 0.3 Left and right pulse signal.
 - Red → Red for RST Signal flow, from IO mouth 15 Foot forward, then by 00 No. chips to 62 No. transmission chip; unplugged IO When the signal line, when the standby 0V When operation is 1.8V .

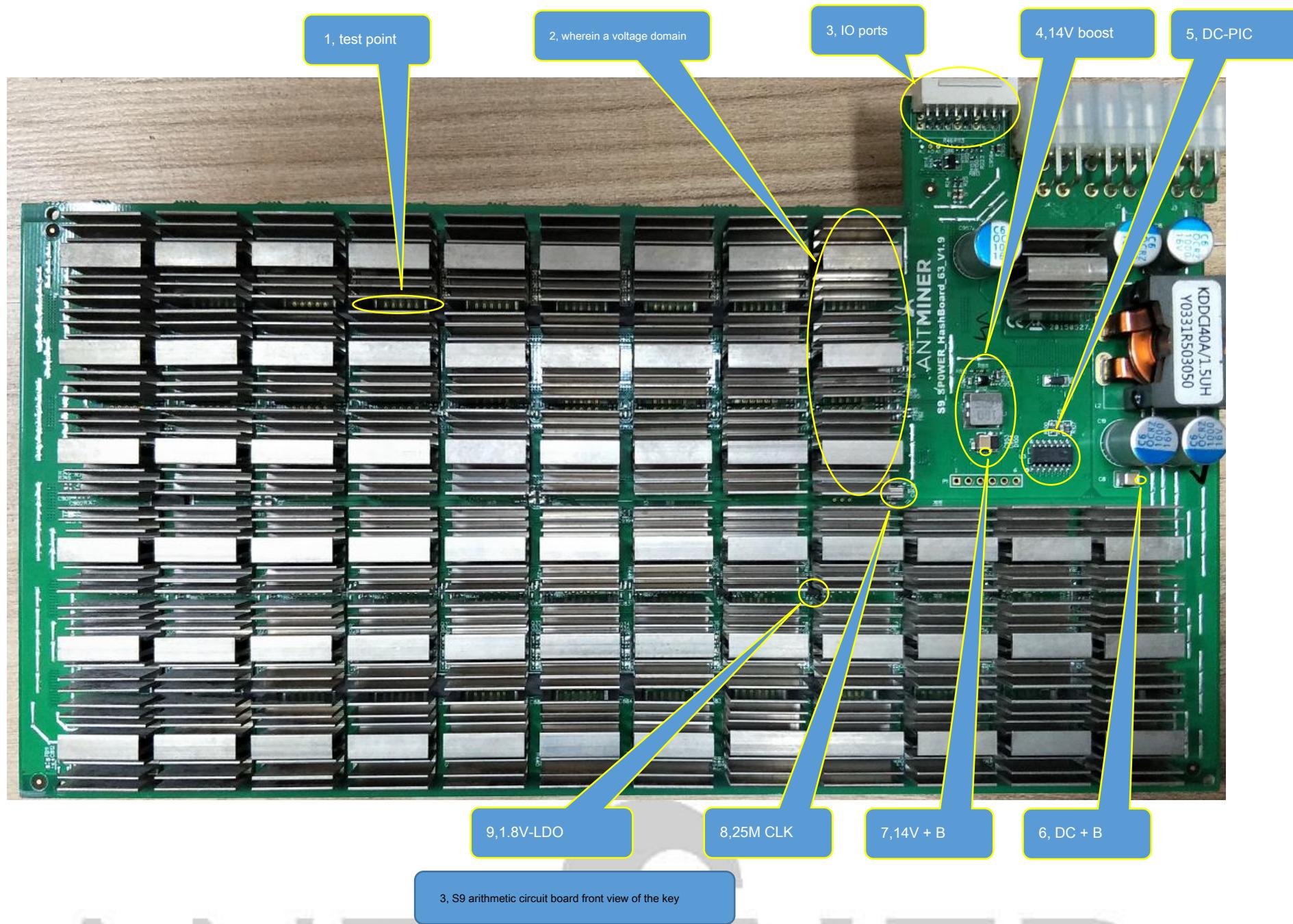
2, FIG. 3 is a front S9 operation of the key circuit board.

1), the space between chips test point (enlarged below): Figure 2



2. the inter-chip test point

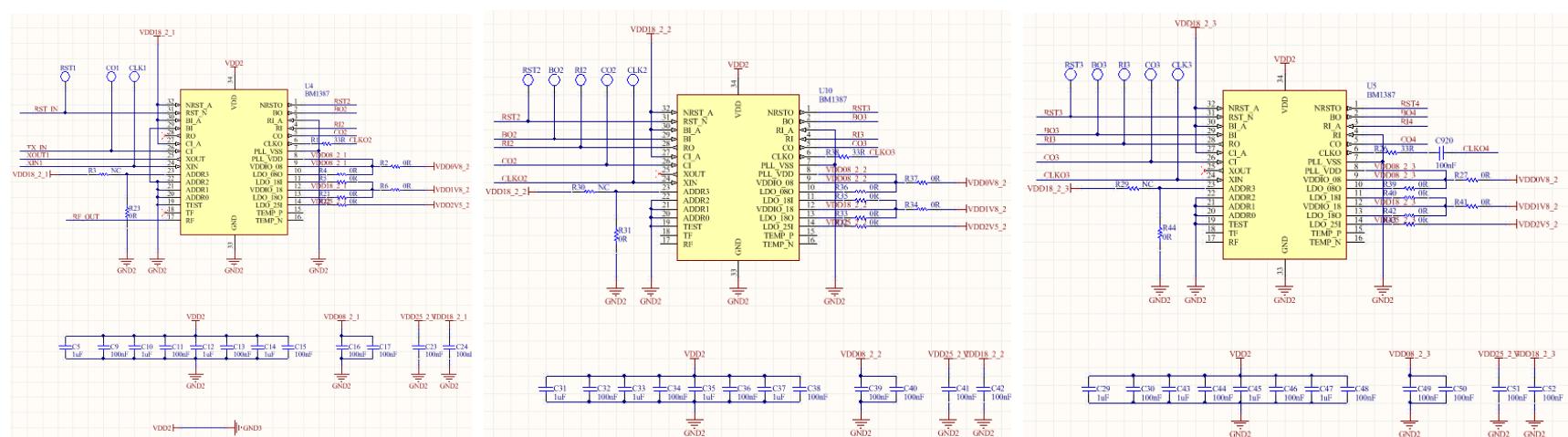
Maintenance, test points between the test chip is the most direct way of fault location. Arrangement S9 arithmetic board test points: the arrangement order of the discharge voltage domain 9: RST, B0, RI (RX), C0 (TX), CLK signal. Lower row voltage domain 12 in turn in the order: CLK, CO (TX), RI (RX), BO, RST.



2) , Voltage domain: the whole plate has

twenty one A voltage domain, each chip has three voltage. In the same voltage domain 3 Power supply chips is associated, then the series is associated with another voltage domain. Each voltage domain 3 Chips circuit configuration as FIG.

4 Below:



4, S9 operational front view of the key circuit board

Note: Because the version S9 operation panel not exactly the same, LDO-1.8V power supply voltage domain earlier versions of each is independent peripheral chip 3 LOD power supply of each chip voltage domain, to later versions chip internal power supply (BM1387 LDO chip power supply circuit is provided with input 2.5V, 1.8V output), except for the last six voltage domain by the external power supply 14V boost the LDO, the other chip by chip in each peak provides the present LDO1. 8V power supply, and PLL-0.8V per chip by a first voltage domain LDO-1.8V resultant pressure (later versions) divided by the dividing resistors.

Analysis of the principle of single-chip voltage domain (see below 5 Fig. 6):

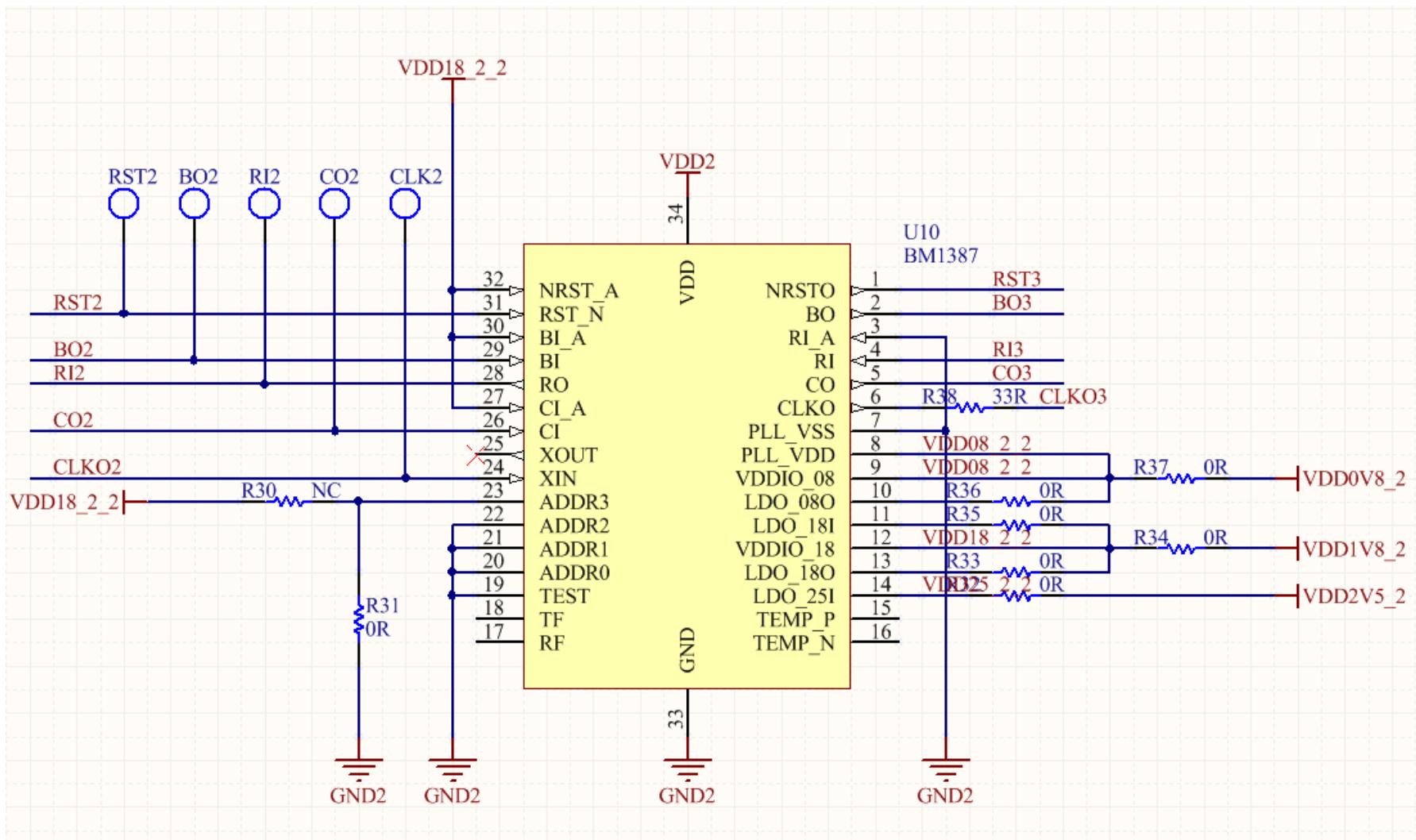


FIG 5, BM1387 circuit diagram

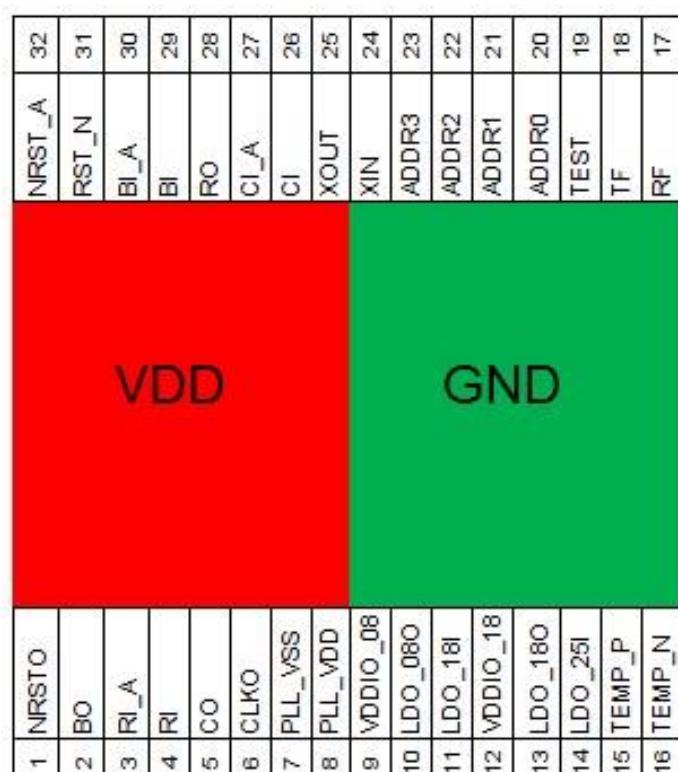


FIG. 6, BM1387 chip pin

Signal Description

	Name	I / O	Active Level	Description
1	NRSTO	O	L	Output to the chip of next level, for the loop
2	BO	O	H	Respond Busy Output
3	RI_A	I	N/A	Auxiliary Respond Input, add diode and pulldown

4	RI	I	N / A	Respond Input. Schmitt input and internal pullup
5	CO	O	N / A	Command Output
6	CLKO	O	N / A	Clock output to the chip of next level, for the loop Pin drive current: 16A
7	PLL_VSS			PLL ground
8	PLL_VDD			PLL power (0.8V), PLL digital and analog share the same supply
9	VDDIO_08			IO VDD pre-drive, 0.8v
10	LDO_08O			LDO 0.8v output, for PLL and IO pre-drive
11	LDO_18I			LDO power input voltage range: 1.62v ~ 1.98v
12	VDDIO_18			IO VDD post-drive, 1.8v
13	LDO_18O			LDO 1.8v output for IO
14	LDO_25I			LDO power input voltage range: 2.2v ~ 2.6v
15	TEMP_P			Temperature diode positive output, analog IO. Should be floating when no use.
16	TEMP_N			Temperature diode negative output, analog IO. Should be floating when no use.
17	RF	O		Function 1 : RO open drain output. Function 2 : SDA0.
18	TF	O		Function 1 : Respond Tx Flag. Function 2 : SCL0.
19	TEST	I	N / A	Internal pull down 0: Normal mode 1: Test mode
20	ADDR [0: 0]	I		Address Input. Internal pullup
twenty one	ADDR [1: 0]	I		
twenty two	ADDR [2: 0]	I		
twenty three	ADDR [3: 0]	I		
twenty four	YIN	I	N / A	
25	XOUT	O	N / A	Oscillator input
26	CI	I	N / A	Oscillator output
27	CI_A	I	N / A	Command Input. Schmitt input.
28	RO	O	N / A	Auxiliary Command Input, add diode and pullup
29	BI	I	H	Respond Busy Input
30	BI_A	I	H	Auxiliary Respond Busy Input, add diode and pullup
31	RST_N	I	L	Reset signal
32	NRST_A	I	L	Auxiliary Reset signal, add diode and pullup

- The above is BM1387 chip pin functions.

Maintenance, before and after the main test chip 10 tests (before and after each of five chips: CLK, CO, RI, BO, RST); CORE voltage; LDO-1.8V, PLL-0.8V,

DC-DC outputs, and the boosted voltage 14V. Detection Method: 1) IO signal line is not inserted, is inserted only when 12V: DC-DC output is about 9V, the output of the booster is about 14V. Test points must be LCK is 0.9V, RI is 1.8V

Voltage, each of the other test voltages are 0; 2) Plug IO lines, without pressing the test button, the step-up DC-DC voltage output are not; manufactured by press with the test button, the PIC to work after receiving the heartbeat signal, DC-DC case

PIC output system is provided with a good test program voltage; boosting work with. Along with an output system WORK, operation returns back plate NONC operation. At this point each test point normal voltage should be:

CLK : 0.9V

CO : 1.6-1.8V. When the system has just sent WORK, CO because it is negative, the case where the DC level will be pulled low, the instant voltage is about 1.5V.

RI : 1.6-1.8V. In operation, when the voltage is too low can lead to abnormal or abnormal operation panel or operator force is zero.

BO : When no operation is 0V. When operational, there will be a pulse beating between 0.1-0.3V.

RST : 1.8V. Pressing the test button will be made with the reset signal is output once again. Test point above state,

when the voltage is abnormal, please estimated fault point in accordance with the signal flow before and after the test point.

- Seen from the list:

CLK Signal: the chip **twenty four** Foot forward, **6** Foot out, the voltage across the time domain is connected, by a **6** 100NF foot out by connecting the input capacitor to the next chip **twenty four** foot.

TX Signal: the chip **27** Foot forward, **5** Foot out;

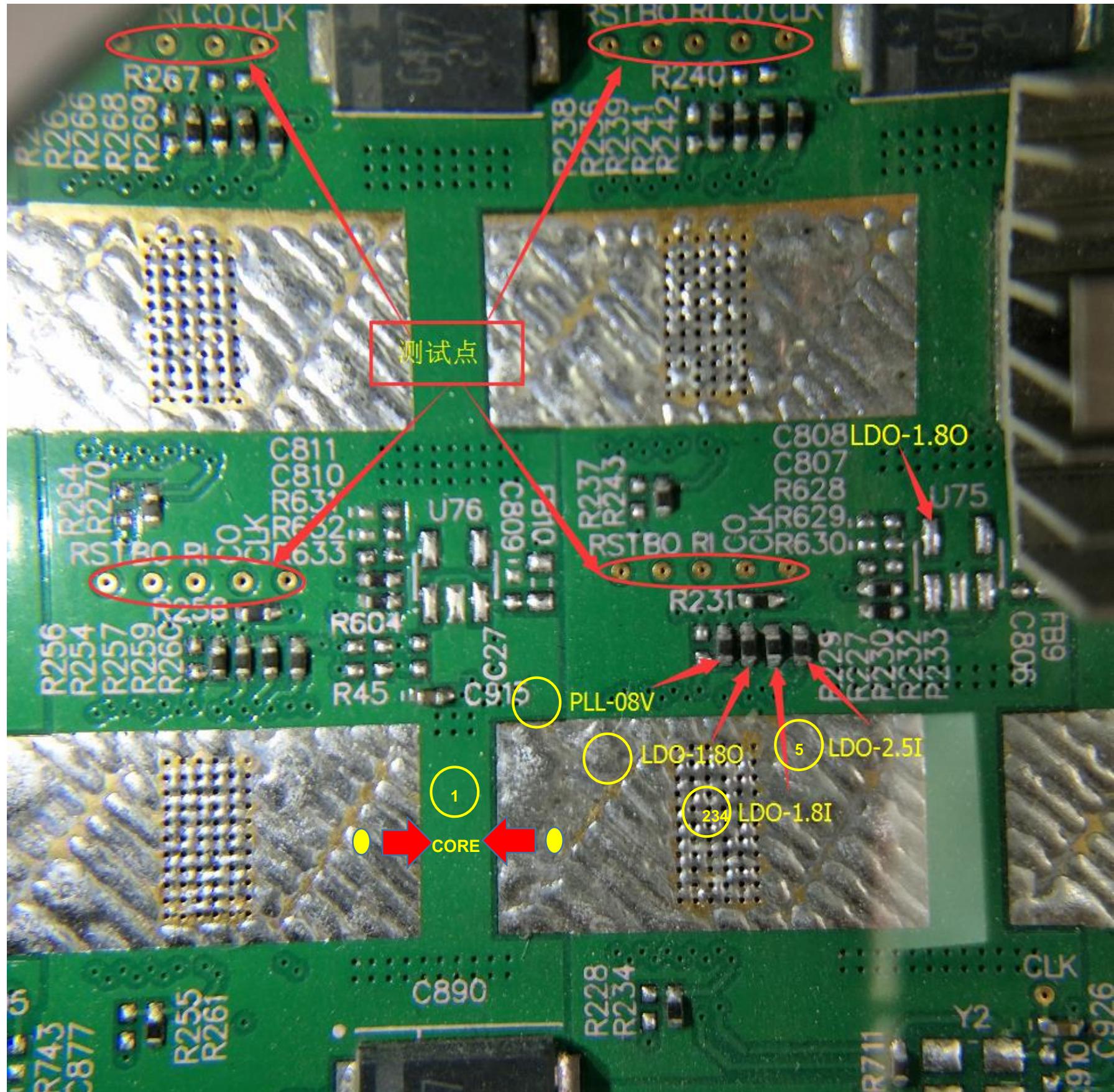
RX Signal: by the chip by the **4** Return leg, **28** Output pin;

BO Signal: the chip **30** Foot forward, **2** Output pin;

RST Signal: the chip **32** Foot forward, **1** Pin output.

7 shown below: quickly locate the chip directly on the board operation S9 respective signal voltages, CORE voltage, LDO-1.80, LDO-1.81, PLL-0.8, LDO-2.51 etc. Voltage:

- ① **CORE** : 0.4V --- When this voltage is abnormal, a short circuit is generally the chip voltage domain CORE
 - ② **LDO-1.80** : 1.8V --- When this voltage is abnormal, the chip LDO-1.80 or shorted or open LDO-1.8I
 - ③ **LDO-1.8I** : 1.8V --- When this voltage is abnormal, the chip LDO-1.80 or shorted or open LDO-1.8I
 - ④ **PLL-0.8** : 0.8V --- This abnormal voltage, which voltage domain has a PLL-08 power supply short circuit chip, or abnormal LDO-1.8.
 - ⑤ **LDO-2.5I** : 2.5V --- When this voltage is abnormal, the chip LDO-2.5I short or open.



7, the periphery of the chip with the voltage test point

3) The test system operator with information determining the print window plate operating state, the chip computing power, temperature flu

Running state

3, IO port: IO by a 2X9 pitch 2.0 PHSD 90 degrees double line composed. Which is defined

below each stitch shown in FIG 8:

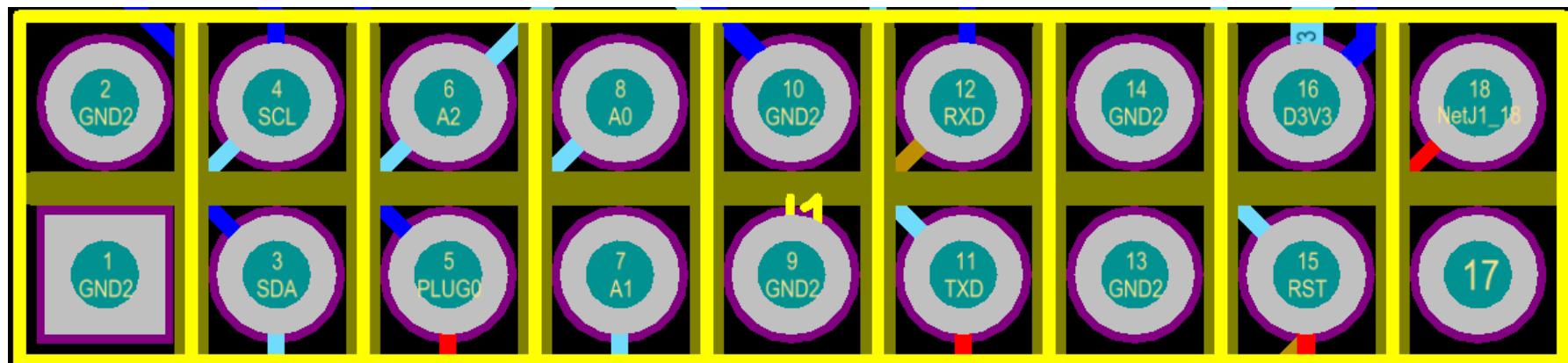


FIG. 8. IO port defined in each stitch

As shown in FIG:

1,2,9,10,13,14 foot : To GND.

3,4 feet (SDA, SCL) : Is a DC-DC PIC I2C bus, a PIC board communication connection, the control board which can be read by the PIC

Data, thereby controlling the supply voltage of the calculation plate.

5 feet (PLUG0) : When the arithmetic board identification signal, this signal is pulled by the operation panel 10K resistor to 3.3V, so the plug IO signal, the pin should HIGH 3V.

6,7,8 feet (A2, A1, A0) : Address signal for the PIC.

11, 12 feet (TXD, RXD) : Force is calculated on the end plate 3.3, through the resistor divider becomes TX (CO), RX (RI) signal,

IO port pins are terminals of the level is 3.3V, the resistive divider, it became 1.8V.

15 feet (RST) : 3.3V for the reset signal terminal, via the resistor divider reset signal becomes 1.8V RST.

16 feet (D3V3) : 3.3V power supply for the operation plate, which is provided by the control panel 3.3V, mainly to provide the PIC operating voltage.

Below 9, and voltage distribution shown in FIG. 10 is a longitudinal partial pressures of the pin IO.

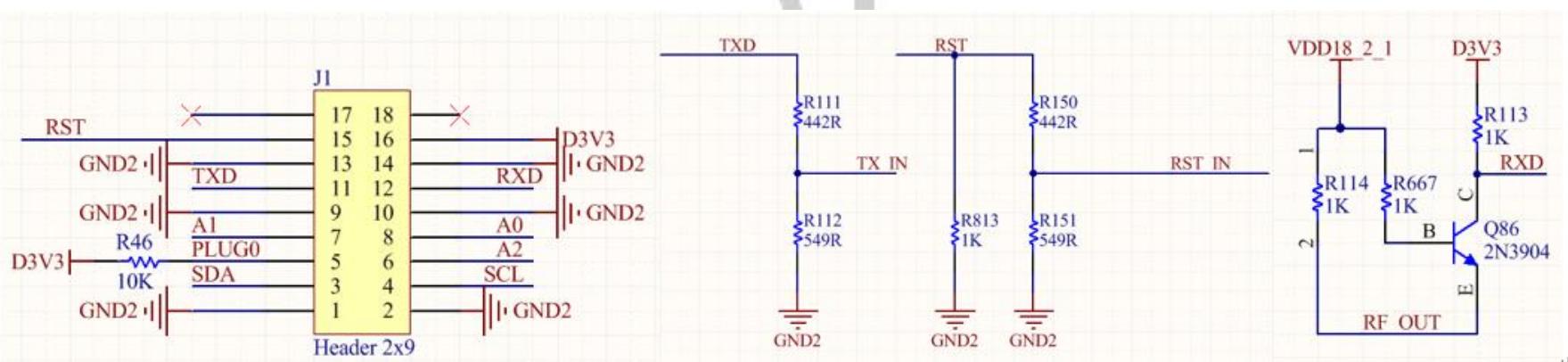


FIG. 9. IO signals of the respective divided voltages

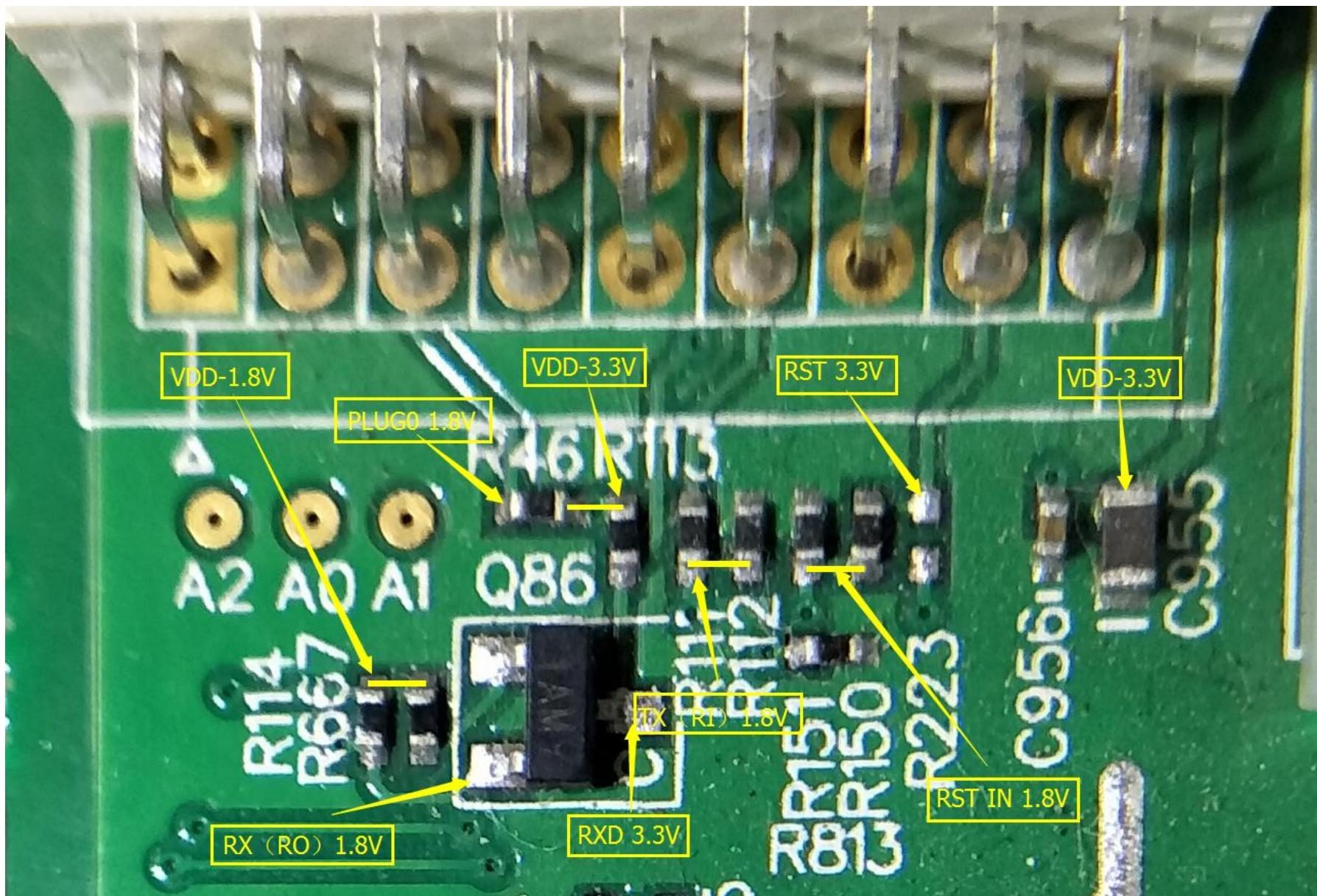
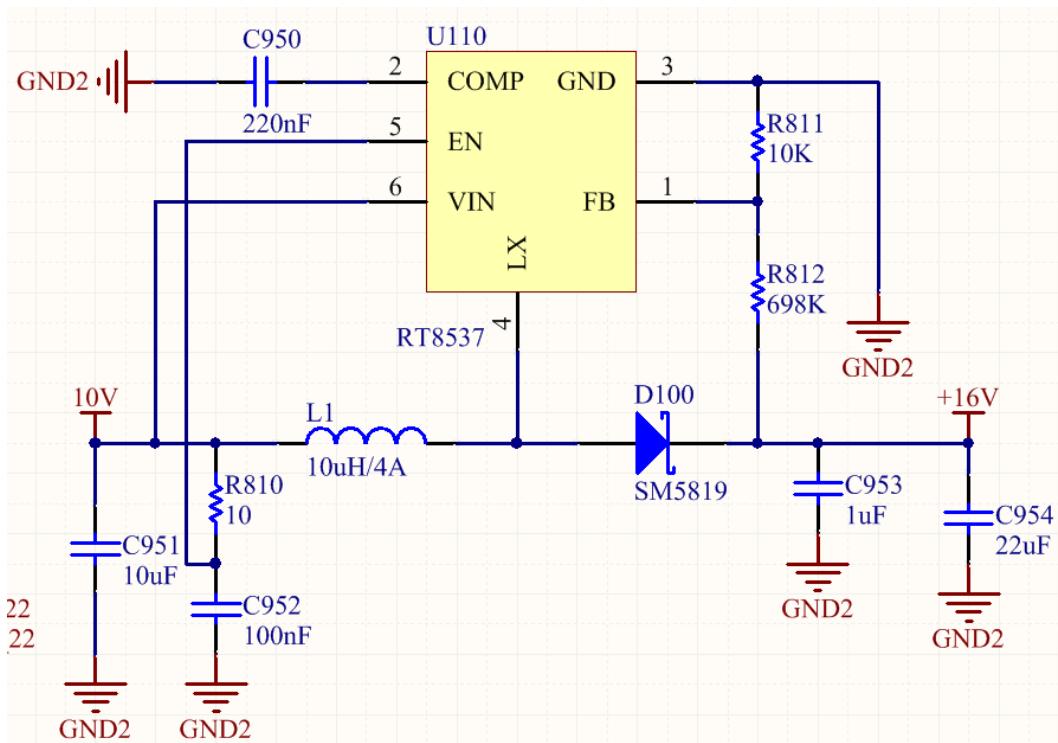


FIG. 10, IO piezoelectric sub signal

Press

4.14V boost circuit:

Responsible for DC-DC (8.3-9.2V) is 14V booster, the principle is U110 RT8537 switching power supplies 14 liters 9V voltage, the switching signal produced by U110 L1 inductive energy storage, then a boost rectifier diode D100 to C954 charge and discharge, the positive electrode to thereby obtain 14V C954. 11, Fig. 12:



Schematic diagram 11,14V boost

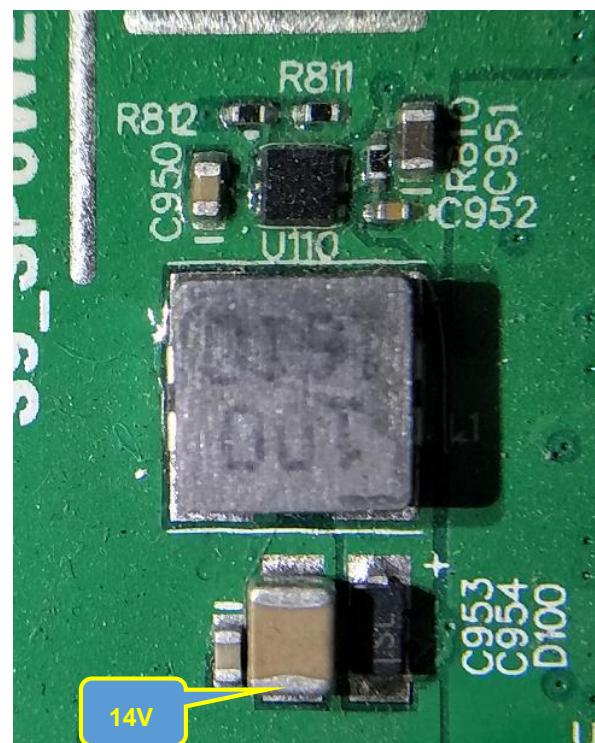


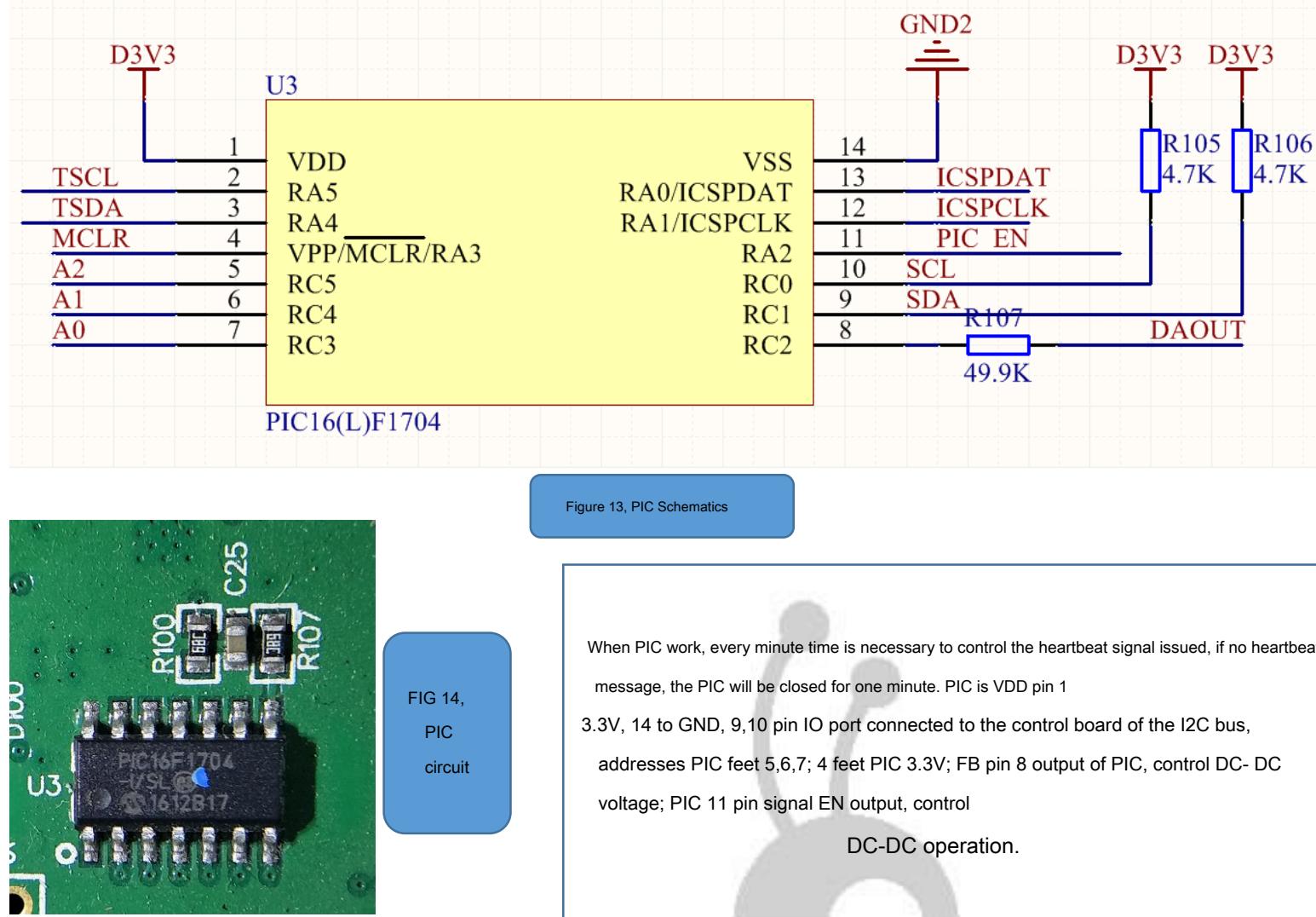
FIG boosting PCB 12,14V

Map

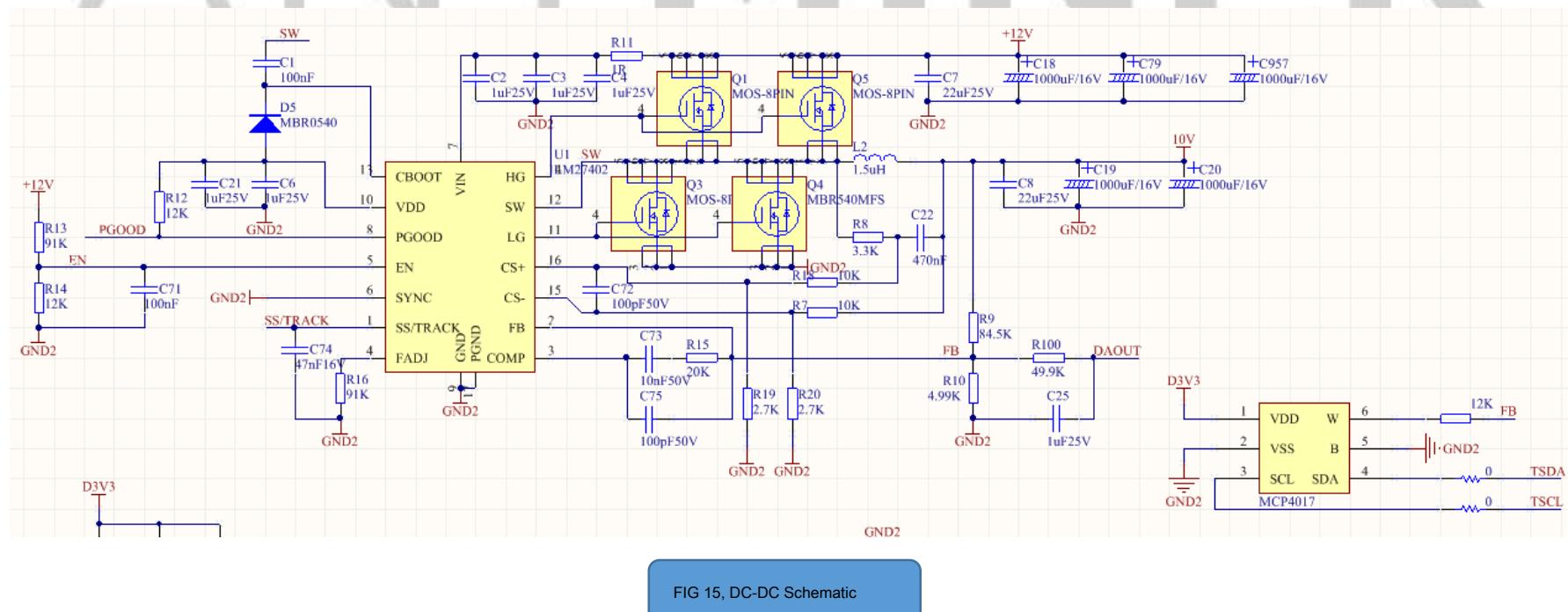
Note: a voltage booster circuit increases abnormally prone to damage last 6 LDO voltage domain arithmetic boards, can easily lead to damage to the chip. Boosted voltage abnormality mostly U110, R812, R811 peroxide.

5, DC-PIC: a PIC16 (L) consisting of F1704. 13 and FIG. 14:

The frequency information storage device and the voltage value of the arithmetic boards each chip, which can be controlled by the arithmetic board a DC-DC output voltage.



6, DC-DC circuit: and a CMOS transistor TPHR9003NL LM27402SQ composition. Below 15, as shown in Figure 16:



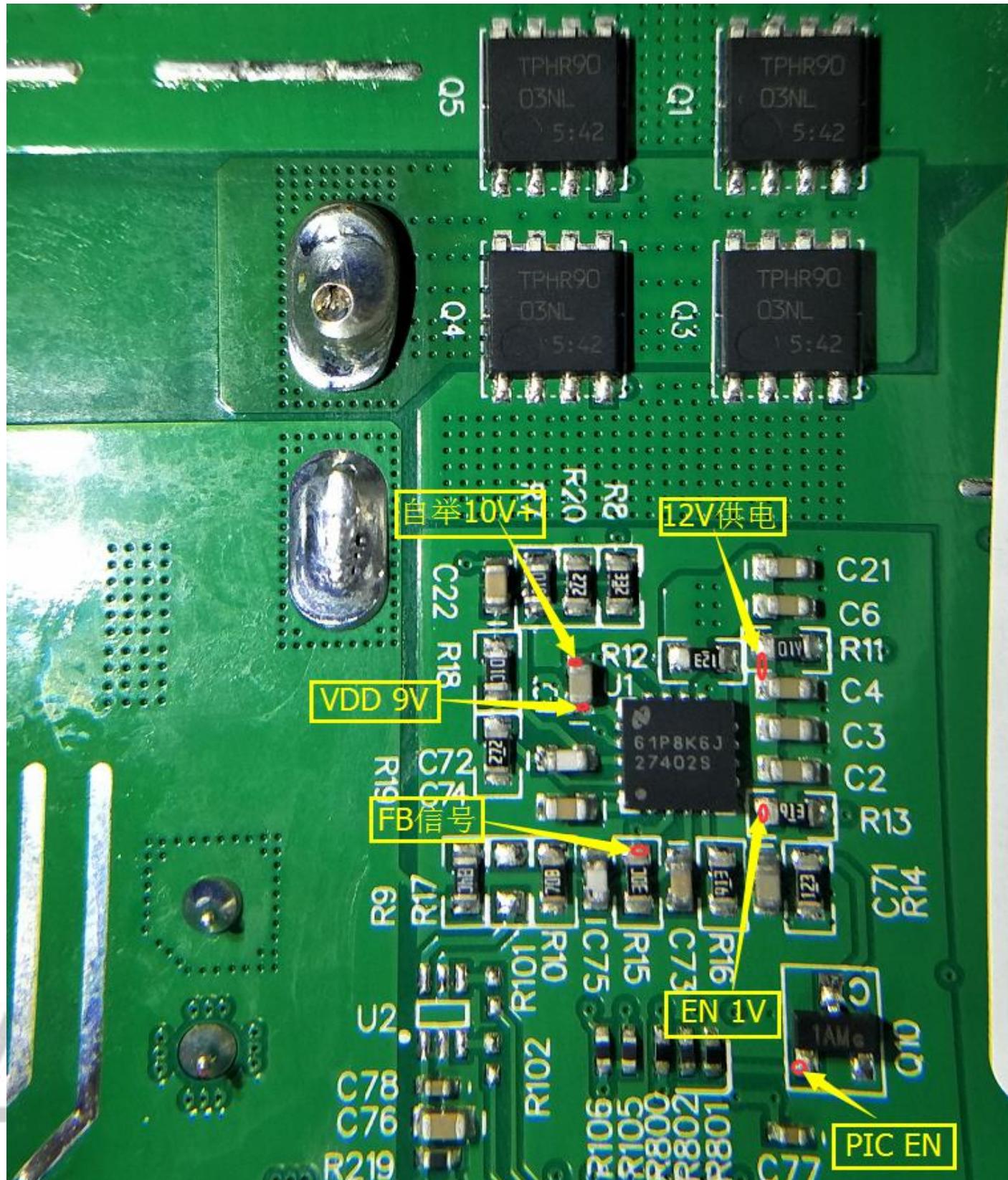


FIG 16, DC-DC circuit

Generating a PWM switching signal driving the upper and lower (two CMOS) LM27402SQ the voltage regulator, and an inductor L2 by energy storage, and then by C19, C20 filter.

LM27402SQ The main function of

the foot 7 foot: 12V power supply

the first 9.17: GND

Pin 2: FB feedback, PIC connector, a voltage determined by the PIC pin 8, 10 feet:

VRR

Foot 13: 10V + bootstrap capacitor pin

16: pin 13 pulses; the switch signal pin

14; the bridge drive pin 14; the bridge

11

| M27402SQ periphery:

If no DC-DC output voltage check EN R13, R14 around 1V, R11 12V voltage. PIC work is abnormal, if the normal reception to the I2C PIC signal control board.

Each operator force computing board a DC-DC output voltage

standard: 14T arithmetic boards: 8 3V-8 6V

13.5T arithmetic board: 8.4V-8.7V

13T arithmetic board: 8.4V-8.9V
 12.5T arithmetic board: 8.5V-9.1V 12T the
 arithmetic boards: 8.6-9.2V
 If outside this range, check the DC-DC circuit.

7.25M LCK by the Y 25MHZ 12pF and passive crystal composition: 17, 18 shown in FIG.

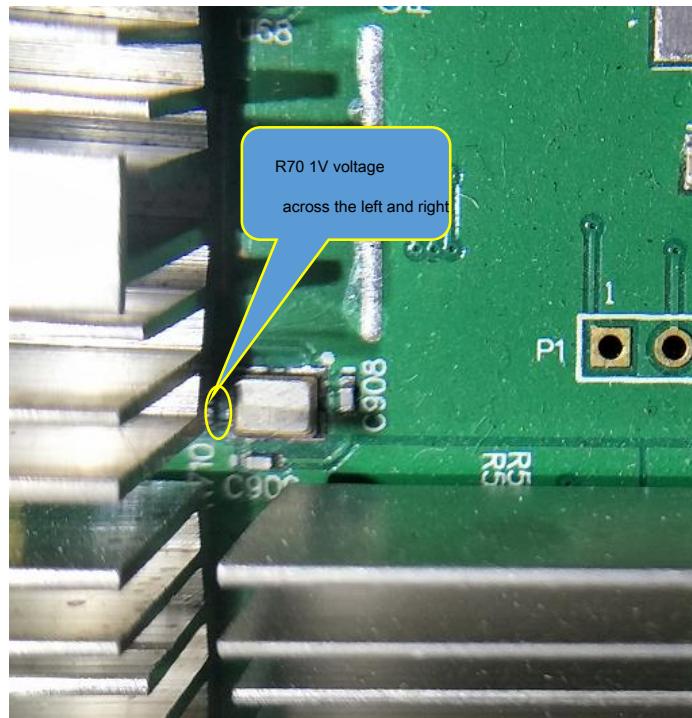


FIG 17,25M LCK circuit

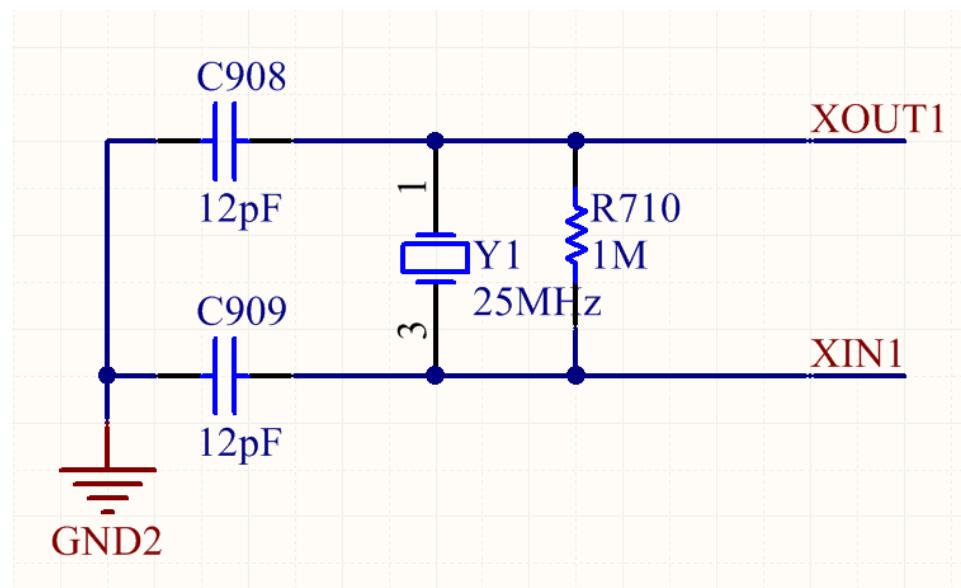


Figure 18,25M LCK principle

When normal, the voltage across R70 are each approximately 1V.

8,1.8V-LDO made 1.8VLDO SPX5205M5_L_1_8 components. Below 19, as shown in FIG. 20:

SPX5205M5 first pin 3 as an input, pin 5 is 1.8V output;

Note that: LDO power supply board has two operation S9. The first version is the operation of each voltage domain using a plate are external LDO SPX5205M5, voltage domain responsible for all three of the LDO chip; the other is only the last six voltage domain using external LDO, other voltage It is provided by a chip board LDO own; BM1387 LDO chips have built-in power supply circuit, by a pin 14 (LDO-25I) BM1387 input pin 10 (LDO-18O) outputs of each chip are independent 1.8V LDO and noninterference in each other. Finally LDO-25I supply voltage domain 6 are from 14V booster circuit; other voltage domain LDO-25I is a voltage CORE 6 resulting superimposed voltage domain ($6 * .04V = \text{about } 2.4$).

PLL-08 by the voltage LOD-1.8 obtained by the partial pressure of the two resistors.

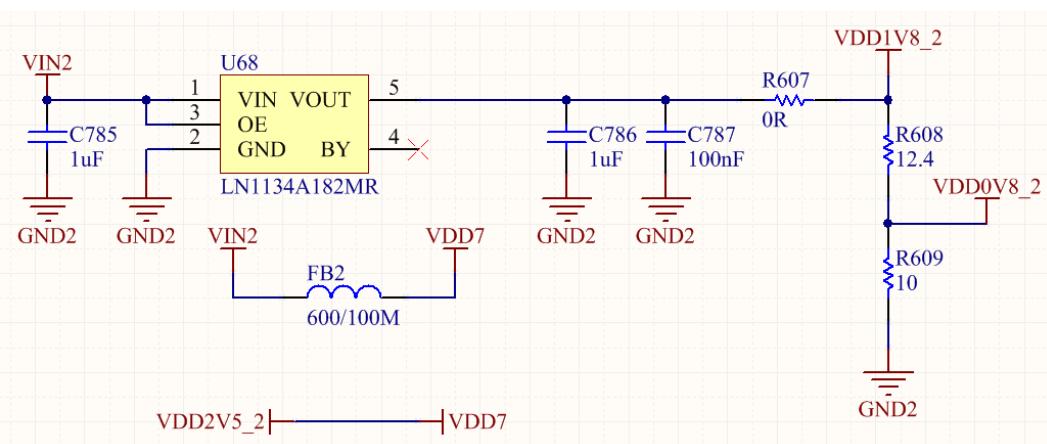


Figure 19, LDO-1.8V power supply principle

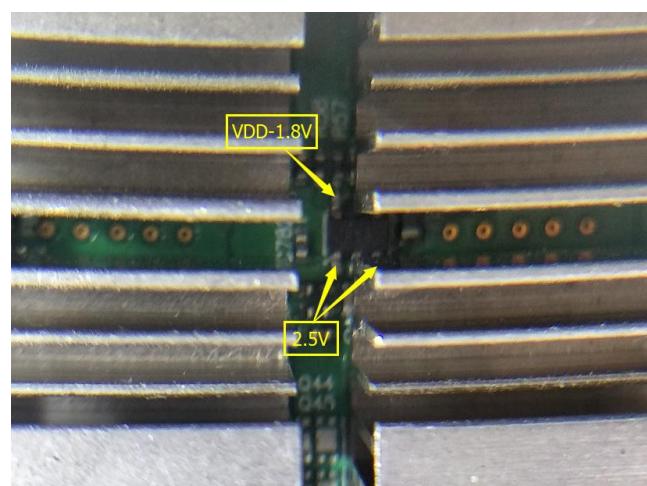
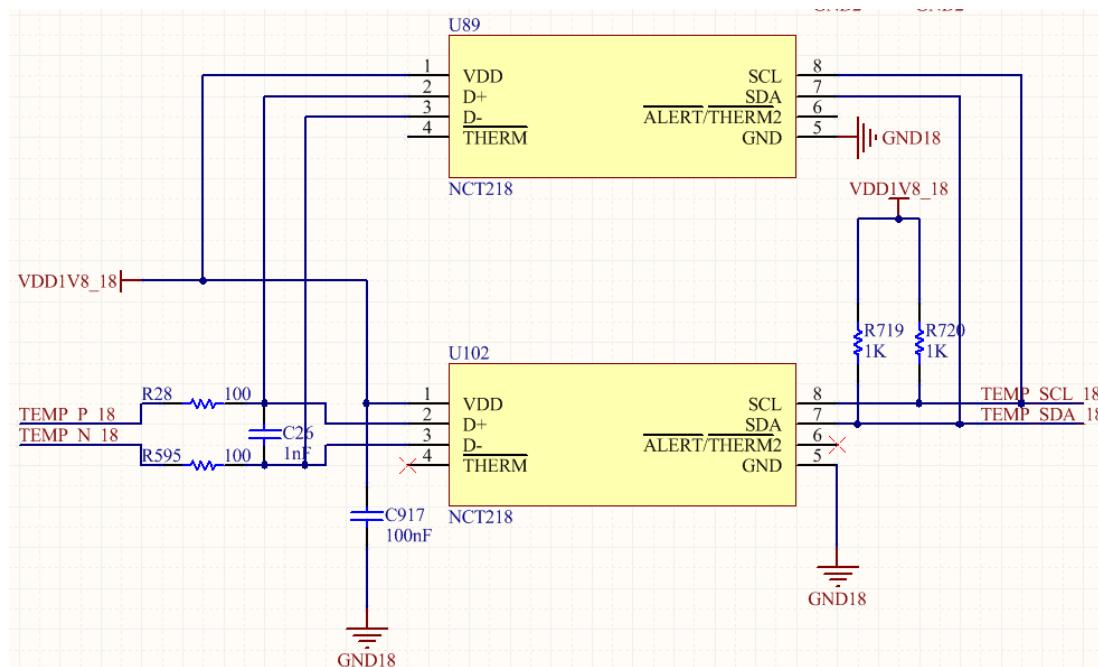


FIG 20, LDO-1.8V circuit

8, the temperature sensing circuit: has both a temperature sensitive, is a TEMP (PCB), this is

Constituted by the sensor IC NCT218; the other is TEMP (CHIP), that is built into the chip temperature sensitive transmission group (BM1387 15, 16 Feet), the two temperature sensitive parameters collected by BM1387 17th and final leg, returned to the control board by the RI of the FPGA; so operation of an operation panel affect the transmission chip damage temperature sensitive data. The principle shown in Figure 21:



screenshot 21, the temperature sensing schematics

- Fast fault troubleshooting methods:

 - Machine Troubleshooting:

1 , You can log monitoring interface (WEB). Most of these cause of the malfunction is the fault operation panel, due to a small number of operating environment, the fan, the external network, as a result of the firmware.

The following is a way to deal with a variety of common phenomenon:

1), Operator interface force without any configuration information. As shown below twenty two Below:

Approach:

• first check indicator mining machine, the mining machine such as red flashing state, indicating an abnormal state of the mining machine, the mining machine can first view the network, computer network plug mine machine

line, PIN Ore mining machine pool URL to see is whether PIN through.

The indicator → normal state. Most likely, the mining machine operation plate 3 are wrong, said comparison voltage PIC mining machine is rewritten.

• mining machine damaged firmware can be upgraded interface firmware upgrade to the latest firmware (before the upgrade is best to restore factory settings).

2),no GH / S (RT) A force calculation, the red light flash. As shown below twenty three Below:

Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
7d7m42s	0.000000	11,239.91	0	25,088,499	15.04	156,662.52	524507137

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	LSDiff	LSTime
0	stratum+tcp://stratum.gbmminers.com:3333	miningpunk.204x40	Alive	10.1K	20,030	0	151,142	0	1,572,384,287	3,096,594	0	321	322,531	50	10,148	3:35:42
1	stratum+tcp://vip001.bw.com:3333	gainbitcoin11.204x40	Alive	8.19K	80	1	595	0	4,874,240	8,192	0	1	1,167	0	8,192	108:19:14
2	stratum+tcp://stratum.f2pool.com:3333	gainbitcoin10.alex	Alive	1.02K	1	2	1	0	1,024	0	0	0	0	94	1,024	168:07:45
total					20,111		151,738	0	1,577,259,551	3,104,786	0	322	323,698	144		
HW		3075						0	0.0002%							

AntMiner

Chain#	ASIC#	Frequency(avg)	GH/S(ideal)	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status							
6	63	485.58	3,487.48	0.00000	51	54	82	oooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo							
7	63	600.42	4,312.27	0.00000	1586	61	98	oooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo							
8	63	515.34	3,701.23	0.00000	1438	48	59	oooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo							
Total	189	533.78	11,501.00	0.00											

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	0	0	3,000	0	0	2,280	0	0

FIG 23,25M LCK circuit

The above phenomenon, mining machine has been running for 7 Days, and GH / S (AVG) How much did not decline, indicating that the mining machine failure time is not long. The fan speed is double Low, and 8 Number plate TEMP (CHIP) Is very low, not long ago out of the board, such a phenomenon is generally able to restart normal. This phenomenon mining machine with the operating environment of great Relations, especially ambient temperature; such as mining machine in the northern winter, the probability of encountering sudden drop in temperature occurs in the case of larger.

Also, please check the network for ore mining machine pool connection is normal? External network instability This also occurs.

If the restart is not operating properly, the test system using the mining machine having three veneer boards of test operation, the plate is abnormal detection algorithm.

There is restore factory settings, update firmware.

3), Dropped calls, low plate, off the chip. As shown below twenty four Fig. 25 Fig. 26 Below:

Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
1d1h26m1s	5,361.679	2,189.48	0	780,338	6.53	30,395.78	142093530

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	LSDiff	LSTime
0	stratum+tcp://stratum.gbmminers.com:3333	miningpunk.51x71	Alive	4.9K	3,014	0	9,970	0	46,257,103	119,137	0	40	48,950	0	4,897	14:32:54
1	stratum+tcp://vip001.bw.com:3333	gainbitcoin11.51x71	Alive	8.19K	1	1	0	0	8,192	0	0	0	0	8	8,192	25:26:03
2	stratum+tcp://stratum.f2pool.com:3333	gainbitcoin10.alex	Alive	2.05K	2	2	0	0	0	0	0	0	0	0	0	Never
total					3,017		9,971	0	46,265,295	119,137	0	40	48,950	8		
HW		1423					0	0.0031%								

AntMiner

Chain#	ASIC#	Frequency(avg)	GH/S(ideal)	GH/S(RT)	HW	Temp(Chip)	ASIC status							
6	63	522.98	3,756.07	2,910.90	563	104	oooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo							
7	63	560.06	4,022.37	2,450.78	846	0	oooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo							
8	34	599.32	2,322.97		14	0	oooooooooooo ooooooooooooo ooooooooooooo ooooooooooooo oo							
Total	160	553.80	10,101.42	5,361.68										

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	0	0	1,800	0	0	1,680	0	0

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24, the phenomenon of chip off force plate count

Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
12m33s	7,865.712	7,876.84	0	21,822	2.23	146,309.44	7111637

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discard
0	stratum+tcp://10.11.11.3:3333	wuyuan+bitmain+s9+1185.75x212	Alive	65.5K	15	0	28	0	1,835,008	0	0	0	389
1	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.75x212	Alive		3	1	0	0	0	0	0	0	0
2	stratum+tcp://112.126.89.154:1800	wuyuanbitmains91185.75x212	Alive		2	2	0	0	0	0	0	0	0
total					20		28	0	1,835,008	0	0	0	389
HW								0	0.0040%				

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status							
7	63	550	3935.15	0	58	88	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
8	63	550	3930.57	73	61	91	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8						
Speed (r/min)	0	0	4,440	0	0	4,560	0	0						

25, the mining machine at least one operation plate phenomenon

Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
2m14s	4,662.136	4,792.90	0	2,337	23.37	60,743.59	65957

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discard
0	stratum+tcp://112.74.143.111:3333	deploymsms91400.136x132	Alive	4.1K	4	0	52	0	135,168	0	0	0	0
1	stratum+tcp://stratum.viabtc.com:3333	deploymsms91400.136x132	Alive	2.05K	1	1	0	0	0	0	0	0	0
2	stratum+tcp://10.20.2.200:3333	shimian+wy+s9+1400.2A2039A358C4	Dead		0	2	0	0	0	0	0	0	0
total					5		52	0	135,168	0	0	0	0
HW								0	0.0000%				

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status							
2	19	650	0	0	0	0	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
3	63	650	4662.14	0	68	98	XXXXXXXX XXXXXXXX XXX							
Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8						
Speed (r/min)	4,920	4,680	0	0	0	0	0	0						

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26, a small mining machine board, chip hit the X phenomenon

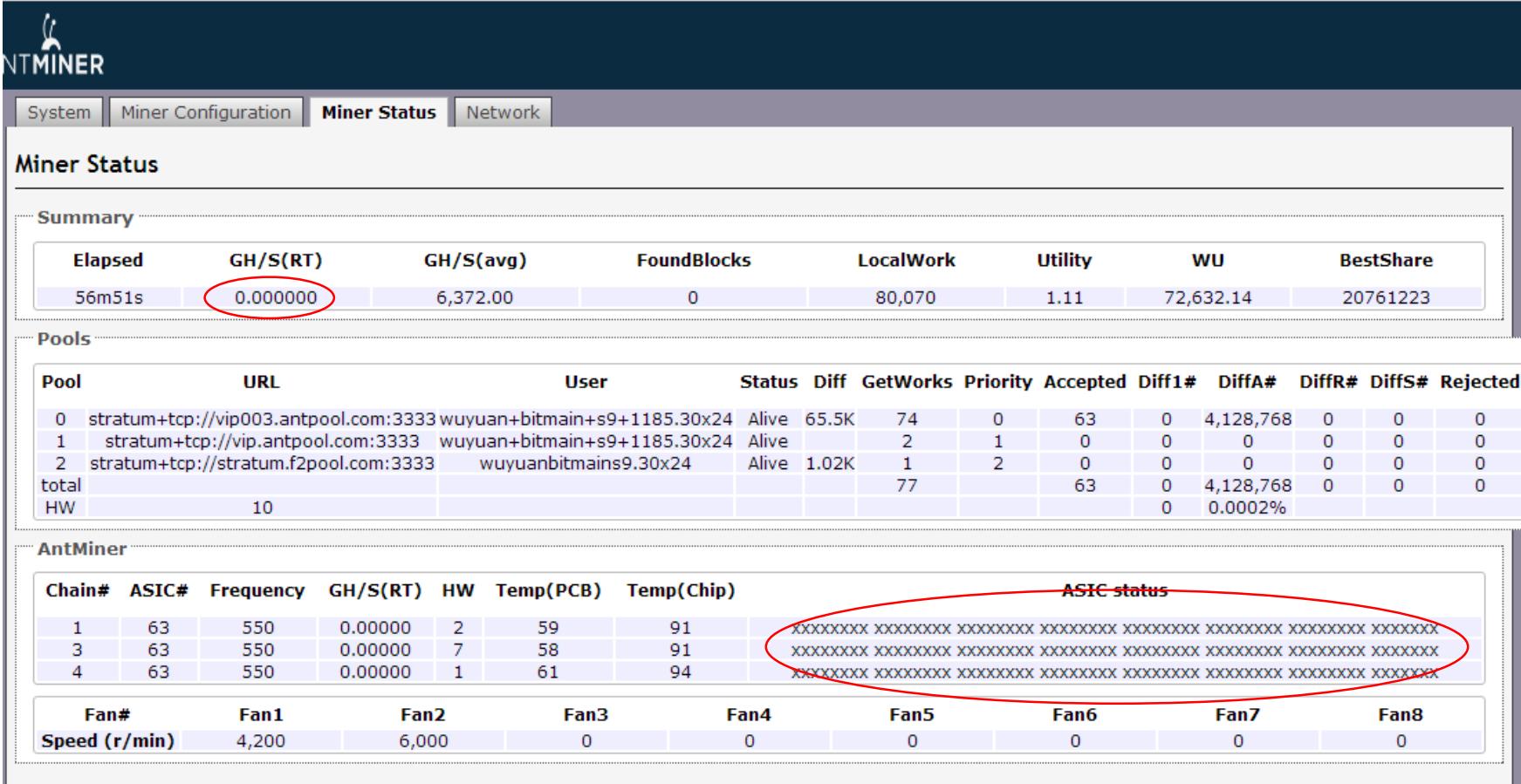
The above phenomenon is caused because the mining machine operation board failure. Map twenty three of 8 Board computing board only to find 34 Chips, for use with a system 8 Number plate veneer detectors, to find

Cause of the malfunction; Fig. twenty four Could not find 6 Number plate, please check 6 Corresponding to the number plate IO Cable, power cable is good contact. If there is no problem with using the system to test 6

Number plate test board; FIG. 25 Could not find 1 Number plate, 2 Only number plates 19 Chips and not up and running, check 1 No. IO And a power supply harness, and measuring

On trial with 1 , 2 Plate test board.

4),no GH / S (RT) Operators force, GH / S (AVG) Operator force is reduced, playing chips XX Phenomenon, the red light flash. Figure 27 Below:



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
56m51s	0.000000	6,372.00	0	80,070	1.11	72,632.14	20761223

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected
0	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.30x24	Alive	65.5K	74	0	63	0	4,128,768	0	0	0
1	stratum+tcp://vip.antpool.com:3333	wuyuan+bitmain+s9+1185.30x24	Alive		2	1	0	0	0	0	0	0
2	stratum+tcp://stratum.f2pool.com:3333	wuyuanbitmains9.30x24	Alive	1.02K	1	2	0	0	0	0	0	0
total					77		63	0	4,128,768	0	0	0
HW								0	0.0002%			

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
1	63	550	0.00000	2	59	91	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX
3	63	550	0.00000	7	58	91	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX
4	63	550	0.00000	1	61	94	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	4,200	6,000	0	0	0	0	0	0

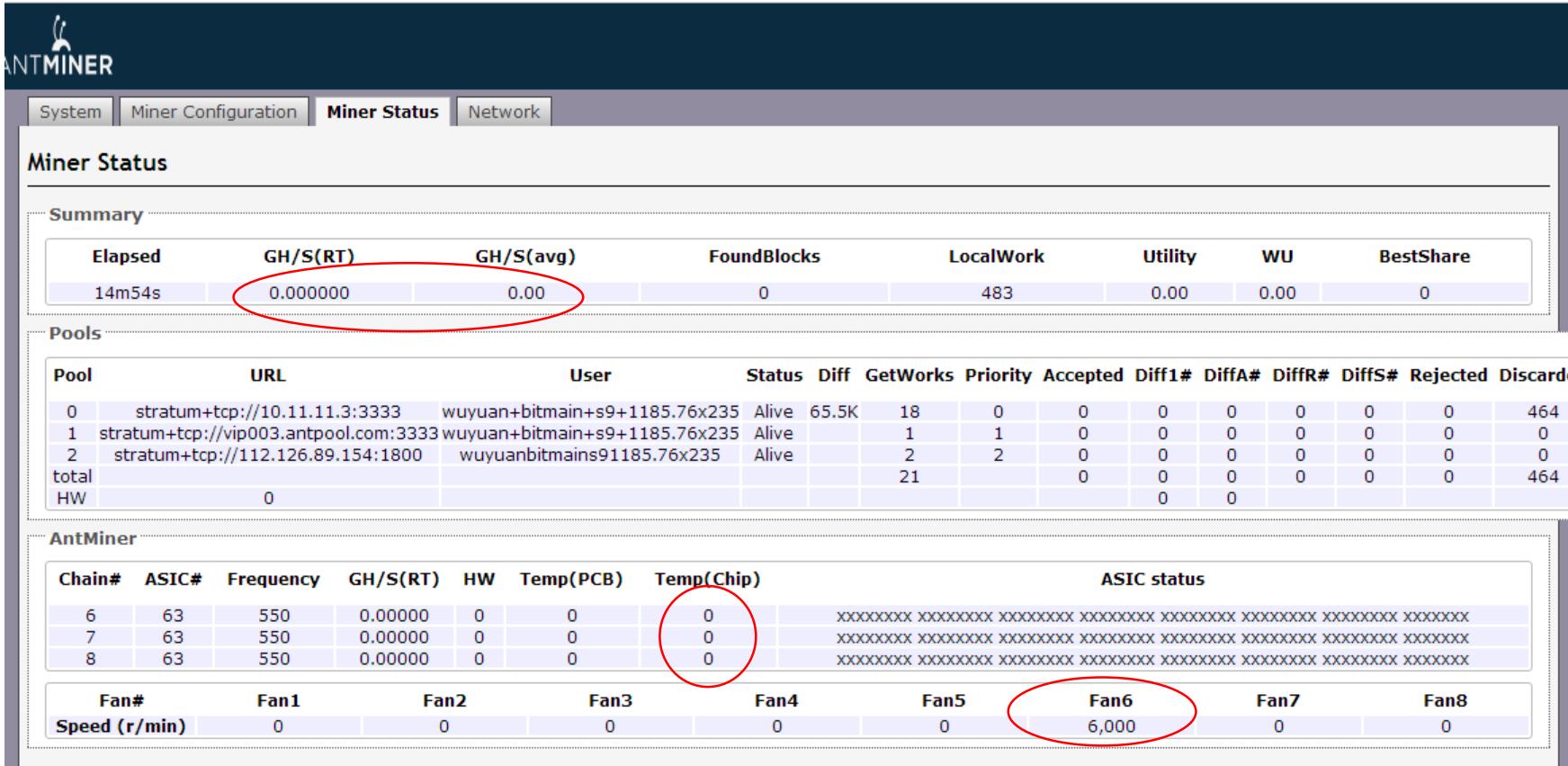
27, the chip-wide fight XX

Above phenomenon GH / S (RT) for 0 , GH / S (AVG) Operator force is reduced, all the chips hit XX Red light flash. This phenomenon is most disturbed after the mining machine, different control panel work

Often leads to. Check the shelves of mining machine, inserted row, 220V Power lines and AC-DC Grounding power supply, as well as static environmental issues.

If there is no static problems and grounded, please upgrade to the latest firmware and use the system for operation with veneer panels into the test.

5),no GH / S (RT) ,no GH / S (AVG), The red light flashes. As shown below 28



Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
14m54s	0.000000	0.00	0	483	0.00	0.00	0

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded
0	stratum+tcp://10.11.11.3:3333	wuyuan+bitmain+s9+1185.76x235	Alive	65.5K	18	0	0	0	0	0	0	0	464
1	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.76x235	Alive		1	1	0	0	0	0	0	0	0
2	stratum+tcp://112.126.89.154:1800	wuyuanbitmains91185.76x235	Alive		2	2	0	0	0	0	0	0	0
total					21		0	0	0	0	0	0	464
HW								0	0				

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
6	63	550	0.00000	0	0	0	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX
7	63	550	0.00000	0	0	0	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX
8	63	550	0.00000	0	0	0	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	0	0	0	0	0	6,000	0	0

28, detects only one fan

This phenomenon is even temperature is not, now can be seen from the figure, show only a fan, because the mining machine detects only a fan and protection. Check insert two fans

Line, or find a replacement at the normal fan.

6)Have GH / S (RT) , GH / S (AVG) Is low, the chip-wide fight X . Figure 29 Below:

ANTMINER

System | Miner Configuration | **Miner Status** | Network

Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
4h10m19s	11,716.92	3,097.42	0	649,923	0.78	51,053.29	3482588

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discard
0	stratum+tcp://10.11.11.3:3333	wuyuan+bitmain+s9+1185.118x44	Alive	65.5K	299	0	195	0	12,779,520	0	0	0	7,785
1	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.118x44	Alive		2	1	0	0	0	0	0	0	0
2	stratum+tcp://112.126.89.154:1800	wuyuanbitmains91185.118x44	Alive		2	2	0	0	0	0	0	0	0
total					303		195	0	12,779,520	0	0	0	7,785
HW	472302							0	3.6958%				

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status									
1	63	550	3904.96	156814	60	91	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
3	63	550	3901.86	158541	58	88	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
4	63	550	3910.10	156947	60	89	XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX									
Fan#	Fan1		Fan2		Fan3		Fan4		Fan5		Fan6		Fan7		Fan8	
Speed (r/min)	4,440		4,080		0		0		0		0		0		0	

FIG 29, GH / S (avg) low chip count full force hit X

run 4 Within hours, HW Reached 15 Million and more, this phenomenon first test with a test system with each operation panel, should the operation board test no problem, leave the configuration of more

New to the latest firmware.



7), GH / S (RT) Ultra-high. Figure 30 Below:

ANTMINER

System | Miner Configuration | **Miner Status** | Network

Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
11m17s	4,799,040. 4799040	11,652.86	0	29,655	2.39	156,843.43	522696

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	LSDiff	LSTime
0	stratum+tcp://vip003.antpool.com:3333	wuyuan+bitmain+s9+1185.30x26	Alive	65.5K	17	0	27	0	1,769,472	0	0	0	355	0	65,536	0:00:34
1	stratum+tcp://vip.antpool.com:3333	wuyuan+bitmain+s9+1185.30x26	Alive		2	1	0	0	0	0	0	0	0	0	0	Never
2	stratum+tcp://stratum.f2pool.com:3333	wuyuanbitmains9.30x26	Alive	1.02K	1	2	0	0	0	0	0	0	0	0	0	Never
total					20		27	0	1,769,472	0	0	0	355	0		
HW	12							0	0.0007%							

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status									
1	63	550	3929.60	7	65	95	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000									
3	63	550	4791205.955000	2	70	99	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000									
4	63	550	3908.57	3	62	93	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000									
Fan#	Fan1		Fan2		Fan3		Fan4		Fan5		Fan6		Fan7		Fan8	
Speed (r/min)	4,320		5,400		0		0		0		0		0		0	

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FIG 30, GH / S (avg) low chip count full force hit X

It can be seen from FIG: 3 Force plate count number reached 4791T This number is certainly good, because 3 Some signal number calculation board receiving plate does not result

Information to confusion. Please use test tools for system 3 No. veneer board test operation, it is necessary to please do stress tests, comparison 550M Operation board, with 600M The frequency of testing,

Low power chip count to find out, then replace the handle.

8)no GH / S (RT) A force calculation, alarm and red light flash. Figure 31 Below:

Miner Status

Summary

Elapsed	GH/S(RT)	GH/S(avg)	FoundBlocks	LocalWork	Utility	WU	BestShare
3h50m21s	0.000000	12,853.15	0	656,130	6.01	183,347.18	54161602

Pools

Pool	URL	User	Status	Diff	GetWorks	Priority	Accepted	Diff1#	DiffA#	DiffR#	DiffS#	Rejected	Discarded	Stale	
0	stratum+tcp://solo.antpool.com:3333	antminer_1	Alive	32.8K	286	0	1,384	0	42,234,880	0	0	0	0	7,215	0
1	stratum+tcp://stratum.antpool.com:3333	antminer_1	Alive		2	1	0	0	0	0	0	0	0	0	0
2	stratum+tcp://stratum.f2pool.com:3333	antminer.1	Alive	1.02K	1	2	0	0	0	0	0	0	0	0	0
total					289		1,384	0	42,234,880	0	0	0	0	7,215	0
HW								0	0.0008%						

AntMiner

Chain#	ASIC#	Frequency	GH/S(RT)	HW	Temp(PCB)	Temp(Chip)	ASIC status
1	63	600	0.00000	100	78	111	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
3	63	600	0.00000	89	84	116	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000
4	63	600	0.00000	145	87	119	00000000 00000000 00000000 00000000 00000000 00000000 00000000 00000000

Fan#	Fan1	Fan2	Fan3	Fan4	Fan5	Fan6	Fan7	Fan8
Speed (r/min)	6,120	4,800	0	0	0	0	0	0

31, no GH / S (RT) red alarm

Alarm phenomenon: Most network is abnormal, excessive temperature or the fan. As can be seen in FIG., A three-plate temperature has exceeded the Temp (chip) The upper limit protection

Alarm. Please check this air flow duct machine mine, whether duct obstructions? Are there broken fan? For dust between the operation plate fins interproximal?

2 , Can not login monitoring interface (WEB). Including mining machine can not find, can not find IP .

The vast majority of such phenomena are the control board issue, especially the firmware reason. Encountered this phenomenon, first of all restore the factory settings to see if can log back to normal,

If another firmware upgrade.

But the control panel, there are two ways to restore the factory settings are not the same.

One kind C5 Control Board (C5 The Dashboard is made IO Board and BB Plates) as shown in 32 Shown; the other is The XILINX (belonging to one board), as shown in FIG. 33.

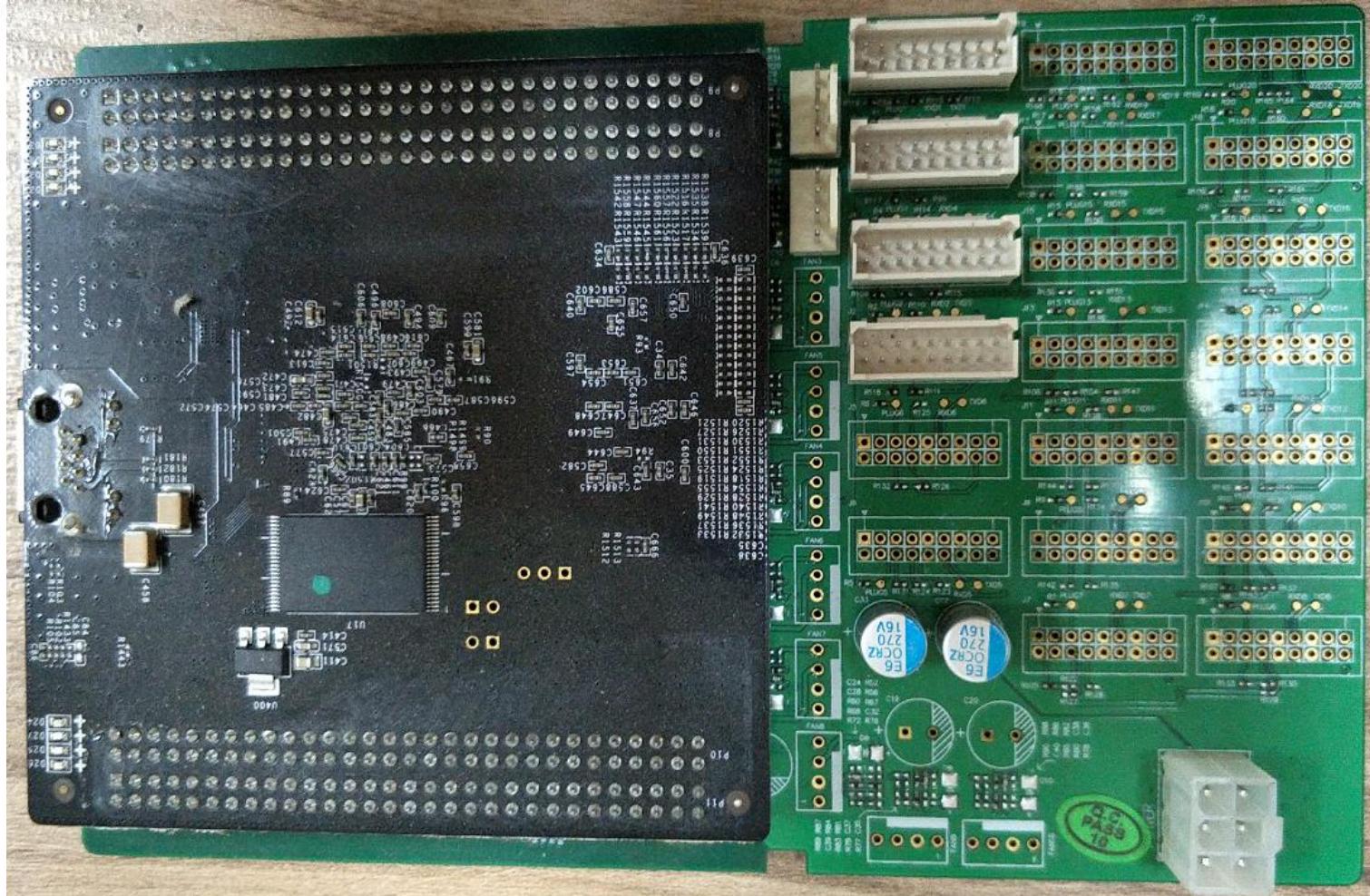


FIG 32, C5 control system

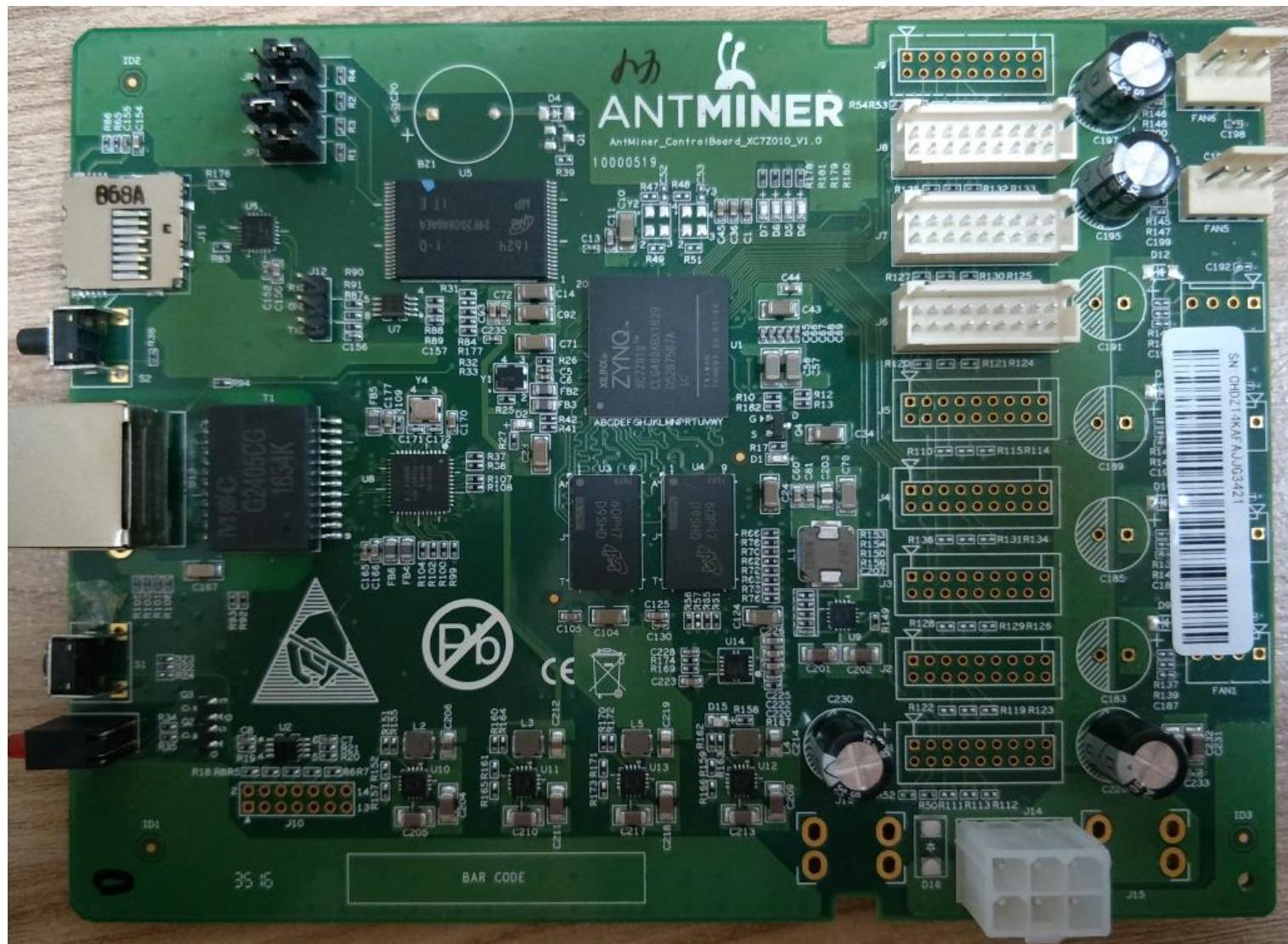


FIG 33, XILINX board

But I machine maintenance, repair, you can not see the overall structure of the control board. We can identify from the whole appearance: The C5 Network control panel lights to

Next, if the FIG. 34 Shown; XILINX The network interface board lights up, following FIG. 35 Fig.



FIG. 34. C5 panel appearance.



FIG. 35. XII INX panel appearance.

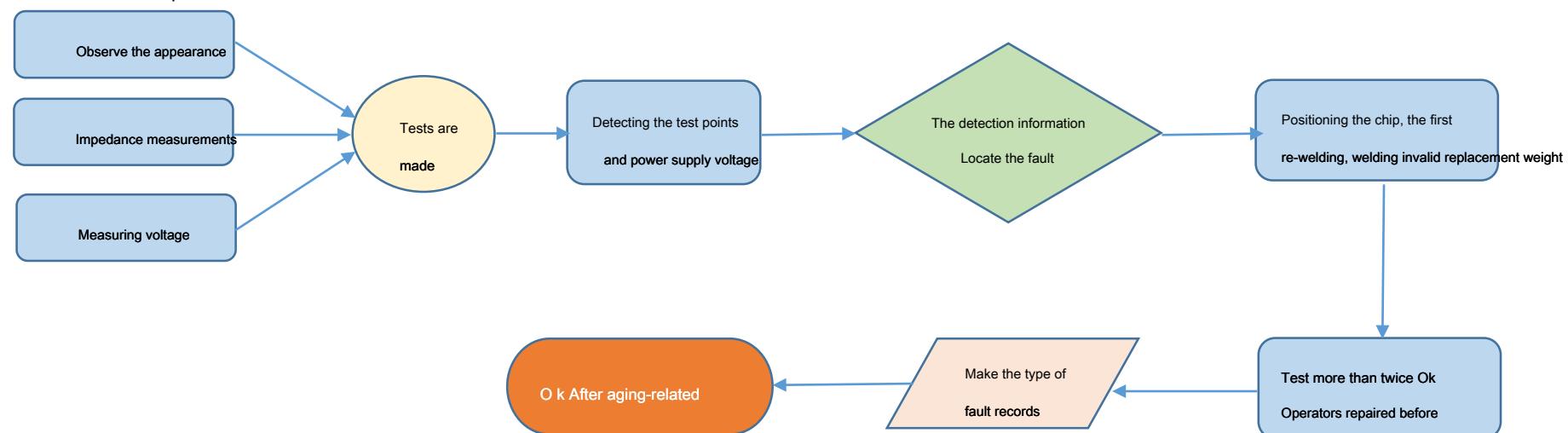
C5 Control panel to restore factory settings way is up and running after the mining machine, press RESET key 5 After the above second, red light long after the mining machine is reset to restart.

XILINX Control panel to restore factory settings way is turned off, press IP Report key 5 After more than second release, start the early recovery plant.

As described invalid restore factory settings, and then into the panel repair process.

Fourth, routine maintenance process:

- Reference steps:



1 , Routine testing: First, let's deal with the repair operation plate visually observe whether a small heat sink displacement, deformation, charred phenomenon? If must first treatment; small fins displaceable first

After the demolition removed, it washes away the gum, by maintenance and re-glue.

Secondly, after no visual problem, the first impedance of each voltage domain is detected, detects whether there is a short circuit or open circuit. If found, it will first deal. Again, to detect the voltage domain voltage is reached 0.4v Each voltage domain voltage shall not exceed the difference 0.05 . A voltage domain voltage is too high or too low, the adjacent circuit voltage domain generally exists anomalies. You must first investigation and the reasons.

2 , No problem after routine testing (short-circuit detection routine testing in general is necessary, so as not energized due to the short burn chips or other material), can be used for the test microarray cassette, and in accordance with Analyzing the test results of the detection cartridge positioning.

3 , The display of the results of the test cartridge detecting, from the vicinity of the chip failure, detection chip test points (CLK IN OUT / TX IN OUT / RX IN OUT / B IN OUT / RST IN OUT) And VDD VDD0V8 VDD1V8 VDD2V5 And other voltage.

4 , The signal then passed reverse flow RX signal (chip No. 63-1) In addition, several of the signal CLK CO BO RST forward transfer (1-63), to find the fault through the power supply abnormality order point.

5 , Locating the fault to the chip, the chip was redissolved need welding. Around the chip method is to add a flux (preferably a no-clean flux), the pins of each chip pad in a state heated to dissolve, the gently lower the left and right movement of the pressing die; chip pin and pad to promote re-engagement magic close tin. In order to achieve the re-tin effect. If after re-welding, or the same fault may be a direct replacement chip.

6 , After the repair operation plate, the test cartridge is detected, the necessary two or more. Twice before and after the test time: after the first, after the replacement of parts is completed, the arithmetic boards need to cool down, by testing After the adoption, first put aside. After the second, every few arithmetic bell plate completely cooled, and then tested. Although the two tests have a few time clock time, but this does not affect the work. The board aside repaired, repair continues to the second plate, the second plate and the like disposed repaired while cooling, and then the first block to be tested. This time just stagger, and not delayed long total.

7 , Repaired the board. You need to be fault classification, and record aspects of the replacement part number, location, and other reasons. To prepare for the feedback back to the production, sale, research and development.

8 , After the record is good, then loaded into a machine for regular aging.

Failure five types:

S9 Troubleshooting types are:

1 , Off the fins, fin shift variations; Power calculation does not allow the back of the front plate of the chip PCB Shift plate fins, collide, in particular different voltage fin. Fins of different voltage domains means a short circuit contact points may different voltage. And determining each of a good heat conductive fin operation plate, firmly fixed. Replacing or on a heat sink, the heat sink, adhesive residue on the chip need to clean and re-sizing, residual ethanol thermally conductive adhesive may be used to clean up.

2 , Each impedance unbalance voltage domain; When the impedance voltage domain deviates some normal, abnormal voltage field has been described an open circuit, short circuit parts. The possibility of general chip lead to the maximum. However, each chip has three voltage domain, often fault, only a problem. The chip problem to find out ways to detect impedance contrast to find outliers through the test points each chip.

Should encountered short circuit, the first heat sink may be on the same chip voltage Kazuya first removed, and then observed whether or even chip pin tin phenomenon. If you can not find the appearance of the short circuit, short-circuit point can find the current according to the resistance method or a method of closure.

3 , Voltage domain voltage imbalance;

When some voltage domain voltage is too high or too low, which is generally adjacent or abnormal voltage domain voltage domain present IO Abnormal signal, resulting in a voltage at a next field or abnormal operating state voltage unbalance. As long as you can identify outliers by signal and voltage test points are detected, the individual needs to find out outliers by comparing each test point impedance.

Particular attention, CLK Signals RST Signal, the two most likely to lead to abnormal voltage imbalance.

4 Lack of chips; The lack of chip test box during testing does not detect all 63 Chips, not real so often only detected multiple chips. The actual loss (undetectable) chip is not abnormal in display Position, then you need to accurately locate the abnormal chip tested.

Positioning method can be used TX Issued off mode, they found abnormal position of the chip. The chip is a TX Signals, for example: the first 50 A chip TX After the output voltage domain, the theoretically if all the chips in front of normal, the test box to be displayed is detected 50 Chips? If not detected 50 Chips, indicating abnormal in the first 50 Before chip; if it is detected 50 Chips, indicating abnormal chip in the first 50 After a chip. So dichotomy identify abnormal chip location.

5 , Chain scission:

Broken chain with a similar lack of chips, but not a chain scission vain to find the core chip are abnormal, but because one chip anomaly caused all the chips behind the abnormal chip failure. For example, a chip itself is able to work, but it will not be forwarded to other chip; in this case, the entire signal chain to an abrupt end here will lose a large part, is the chain scission.

Scission general test box is displayed, for example: In the test cartridge when detecting chip, detects only 14 Chips, test box if the number of chips less than a preset detection is not up and running, it will only show how much the chip is detected, this time as long as the display of digital "14" In the first 14 Detection voltage and impedance of each test point before and after the chips will be able to find the problem.

6 , Do not run:

Do not run the test cartridge means not detecting chip operation panel information, the display **NO hash board** ; This phenomenon is the most common situation, the failure scope is too wide.

1) A voltage domain voltage abnormalities caused by not running: You can identify problems by measuring the respective voltage domain voltage.

2) Caused by an abnormal chip Abnormality can be found by measuring the signal test points.

CLK signal: 0.9V ; Signal generated by the 00 No chip output to 62 No chips, but the current version is only a crystal, which as long as the abnormal signal LCK , Followed by the abnormal signal will all, according to the signal transmission direction sequential search.

TX signal: 1.8V ; This signal is generated by 00 , 01 ,..., 62 No chips, when a point forward dichotomy can detect abnormal.

RX signal: 1.8V ; This signal is generated by 62 ,..., 01 , 00 Number returned by the cause of the malfunction confirmation signal to the chip, S7 and S9 arithmetic board does not run the signal is the most priority, to find the signal.

BO signal: 0V , The letter The chip number is detected RI When the return signal is normal, in order to be pulled down to high, or high.

RST signal: 1.8V ; Plug in power operation and the plate IO After the signal, which will be from 00 , 01 ,..., direction 62 is transmitted to the last chip.

3) A chip VDD caused

By measuring the potential difference of each voltage domain is normal, under normal circumstances, when **VDD Voltage 0.4V** When each of the other test point voltage domain voltage is normal **0.4V** , In order to ensure that all electricity Pressure balance between domains .

4) A chip VDD1V8 Abnormal voltage

A test point is determined by measuring each voltage **VDD1V8 Voltage** is normal, under normal circumstances, **IO Voltage** determines the voltage of each test point, and when **IO Voltage 1.8V** When each of the other test point voltage domain voltage is normal **1.8V**

5) A chip VDD2V5 Abnormal voltage

Check the voltage is normal, abnormal and VDD Voltage is low correlation.

6) Step-down circuit and Boosting circuit caused by abnormal

Can directly measure the upper left corner of the arithmetic boards **C8 Output capacitance** Whether there is voltage across 8.27-9.07V between No need to upgrade or exceed U3 PIC; confirm PIC voltage is normal, the subject

Measurement **U100** Is there output 15V Voltage is not detected Parts and peripherals U100 itself.

7 , Low power calculation:

Low power calculation can be divided into:

- 1) When testing the test cassette, cassette received **Nonce** Enough, lack of power and display count **NG** . This phenomenon can be returned directly to each chip through the serial port to print information about the test case to see **Nonce** How much the number of judges, the general return **Nonce** Value lower than the set number of chips should troubleshooting, excluding non-Weld, peripherals outside reasons, direct replacement chip.
- 2) Test box test, but the count is low power installed after the machine appears. Such cooling conditions where a relationship is most related to the chip, each chip requires special attention with small plastic fins, and ventilation performance of the machine. Another reason is that the threshold voltage of a chip in, installed the machine, **12V** And power supply when the test force difference calculation results in the test run with a force deviation calculated, by using the lower test cassette test, slightly offset voltage **DC** Adjustable power supply **12V** After the output, and then test them to return **Nonce** The minimum number of voltage domains chips investigation.

8 , A chip NG :

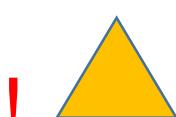
When referring to the test by testing the box, the box serial test information display returns some chips **Nonce** Or less than zero, with the exclusion of the peripheral element Weld problem than direct replacement chip.

- On maintenance:

- 1 , When servicing, maintenance staff must be familiar with the role and flowing to each test point, the normal voltage and impedance to ground values.
- 2 , You must be familiar with the die bonding, so as not to cause deformation or blistering PCB pin damaged.
- 3 , bm1387 Chip package, the chip 16 on both sides of the foot. Must be aligned with the polar coordinate welding, can not be misplaced.
- 4 , When replacing the chip, the thermal conductivity surrounding the die attach adhesive must be clean, so as not cause floating or heat the IC chip of the secondary damage to the welding.

- Precautions:

1. Other than due to the connection chip back side heat sink and the chip, the detection of a test point signal must be specially elongated leads, and leads except that the contact tip is exposed metal, the rest must Fengdiao insulated by heat-shrinkable tube, so as to avoid the test point, leads while contacting the heat sink and the test point. The voltage difference between the upper and lower rows particular circuit pressure is large, while contacting the ground different voltage domains (fins) and the test points are created artificially damaged chips, special attention.
2. Soldering, there is close to the backside of the die **PCB** Small fin plates, thermal faster. Therefore, the bottom welding necessary to use auxiliary heating (200 Degrees or so), can improve efficiency and reduce **PCB** Damage board. If there is no bottom heating means, when replacing the chip, the chip must first back surface **PCB** Small plate fin taken down before replacement.



There are new types of faults, please contact our engineering department in a timely manner, we will continue to analyze and update this content!