Q1	Q2	Q3	Q4	T

EE 306 Microprocessors Spring 2023 – 2024 Final Exam

Full Name and Student ID:	
Signature:	
Number of solution pages:	

Submit this booklet and extra solution sheet(s). All must have your full name and signature. Note that there are 4 questions. ***Good Luck!***

Q1. (15 pnt) Fill in the blanks, NO abbreviations.

A. CMP instruction performs a subtraction and updates the condition codes (flags); general purpose registers are not affected.

B. A feature of the ARM instruction set is that nearly all instructions are executable. Execution of these instructions depends on the current value of the flags in CPSR. This style of programming relies on the fact that status flags can be set optionally on some instructions.

C. A stack is a list of memory data elements, usually words, with the accessing restriction that elements can be added or removed at one end of the list only.

D. The processor enters in Supervisor Mode on reset or power-up.

E. The processor enters in IRQ Mode or FIQ Mode on a valid interrupt request, based on the type of the interrupt.

F. The GIC includes several memory-mapped registers that provide an application programmer's interface (API). The GIC architecture is divided into two main parts: Part 1) receives IRQ interrupt signals from I/O peripherals. Part 2) is responsible for sending IRQ requests received by the first part, to the processor. Who are they?

1) Distributor, 2) CPU Interface

G. The processor must inform the device that its request has been recognized so that it may remove its interrupt-request signal. So, a/an acknowledge signal is sent to the device through GIC.

H. Addresses generated by the processor core are virtual addresses. These addresses are translated into physical addresses by a combination of hardware and software actions. When an instruction or data is requested, the address translation is done by memory management unit.

I. Flynn's taxonomy is a classification of computer architectures. Give the four classifications defined by Flynn.

single instruction single data — multiple instruction syple data

" " multiple " — " " multiple "

Q2. (40 pnt) System Design

A prototype for a light decoration is built on DE1-SoC board. The system can control 8 red LEDs on the board and uses 2 switches (SW1 and SW0) to select the blinking mode. Mode selection is given in Figure 1. Blinking mode sets the pattern (P) and speed. SW0 is used to select the pace: "1" and "0" mean fast and slow, respectively. **Use the timer** to manage the delay.

SW1 selects the blinking pattern. The patterns are given in Figure 1. Necessary devices are given below.

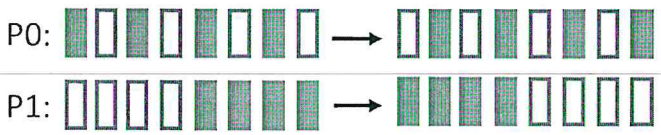

Figure 1: Blinking patterns.

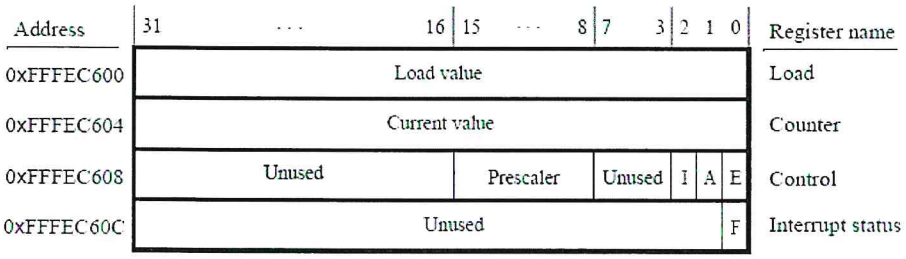

Figure 2: Timer

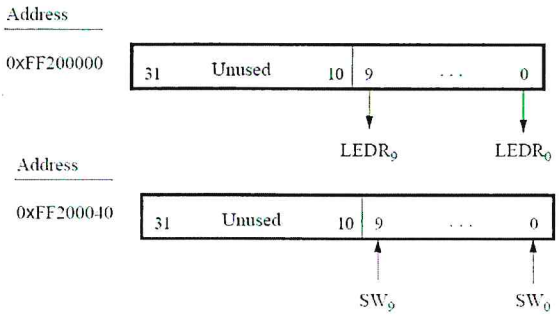

Figure 3: LEDs and SWs

```
LDR R0, =0xFFFEC600   } define base addresses
LDR R1, =0xFF200000   }
LDR R2, =0xFF200040   }
    MOV R3, #0b1010101010  } patterns (2)
    MOV R4, #0b1111        }
Begin: LDR R5, [R2]        }
    ANDS R5, #1            }
    MOVEQ R6, #R3          } set pattern
    MOVNE R6, R4           } (4)
    LDR R5, [R2]           }
    ANDS R5, #0b10         }
    MOVEQ R7, #100         } set speed
    MOVNE R7, #50          } value. (4)
    STR R7, [R0, #0]       }
    MOV R7, #0b011         } set timer
    STR R7, [R0, #8]       } (4)
    STR R6, [R1]  ------>  Leds (2)
wait0: LDR R7, [R0, #12]   }
    ANDS R7, #1            } wait
    BEQ wait0              } for a while. (5)
    STR R7 [R0, #12]       }
```

```
    MVN R6, R6             } flip (6)
    STR R6, [R1]           }
wait1: LDR R7, [R0, #12]   }
    ANDS R7, #1            } wait
    BEQ wait1              } (5)
    STR R7, [R0, #12]      }
    B Begin                } loop (4)
```

Continue Answer 2 here. Q3 is on the next page.

Q3. (30 pnt) Floating point

Consider the following 32-bit floating point format. The fifteen bits following the sign bit show exponent excess-4095. The rest of the bits (16 bits) are mantissa fraction.

sign, exp, exp-4095, conv.

A. Represent A in this format. A = -12.375

B. Write an assembly program to compare 2 floating point numbers A and B, which are stored in the memory at LOCA and LOCB, respectively. Use ARM v7 instruction set. Store the greater and smaller numbers into the memory location GREAT and SMALL, respectively. If the numbers are equal, contents of both memory locations will be the same.

$12.375 = 1100.011 = 1.100011 \times 2^3$ $\quad E = 3$, $E' = 3 + 4095 = 2 + 4096$

A) 1 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 . 1 0 0 0 1 1 0 0 0 0 0 0 0 0 0 0

B)

```
LDR  R0, [LOCA]
LDR  R1, [LOCB]
mov  R2, R0, LSL #1
mov  R2, R2, LSR #1
mov  R3, R1, LSL #1
mov  R3, R3, LSR #1
mov  R4, R0, LSR #31
mov  R5, R0, LSR #31
CMP  R4, #0
CMPEQ R5, #0
BEQ  BothPos
BNE  AGreater
CMP  R5, #0
BEQ  BGreater
BNE  BothNeg
```

2 — mag. A; mag. B; sign A and B — get sign and mag: 6

(A+) (A+, B+) (A+, B-) (A-) (A-, B+) (A-, B-) — decide on signs: 6

```
BothPos:    CMP  R3, R2
            BGE  BGreater

AGreater:   STR  R0, [GREAT]
            STR  R1, [SMALL]
            B    end

BothNeg:    CMP  R3, R2
            BGE  AGreater

BGreater:   STR  R0, [SMALL]
            STR  R1, [GREAT]
            B    end
```

write correct pos. 8 (correct branches)

Q4. (15 pnt) Memory

Draw a 2M × 32 memory module using 256K × 8 static memory chips. Do not forget the address decoder. Clearly show the important address bits.