Microprocessors

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Basic Processing Unit

Computer Organization and Embedded Systems, Hamacher et. al

Some Fundamental Concepts

- The *instruction register* (IR) holds the instruction that is currently being executed.

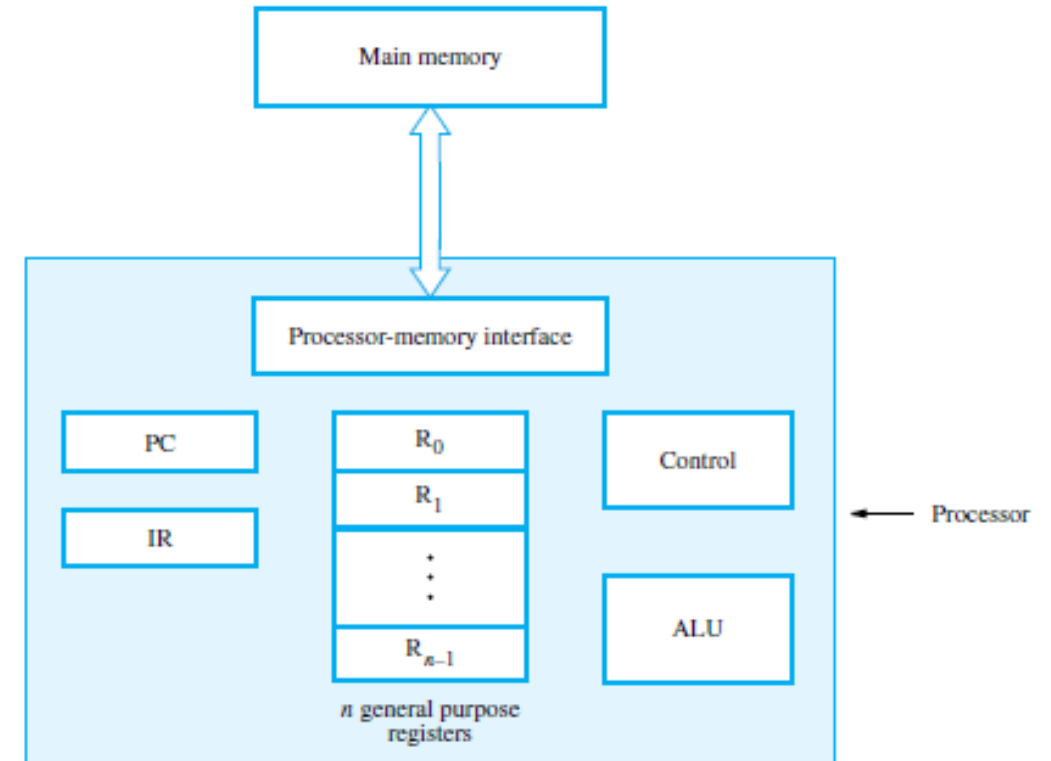- The *program counter* (PC) *points* to the next instruction that is to be fetched from the memory.

Figure 1.2 Connection between the processor and the main memory.

RISC (Reduced instruction set computing) style instruction set architecture

1. Fetch the contents of the memory location pointed to by the PC. The contents of this location are the instruction to be executed; hence they are loaded into the IR. In register transfer notation, the required action is

    $$IR \leftarrow [[PC]]$$

2. Increment the PC to point to the next instruction. Assuming that the memory is byte addressable, the PC is incremented by 4; that is

    $$PC \leftarrow [PC] + 4$$

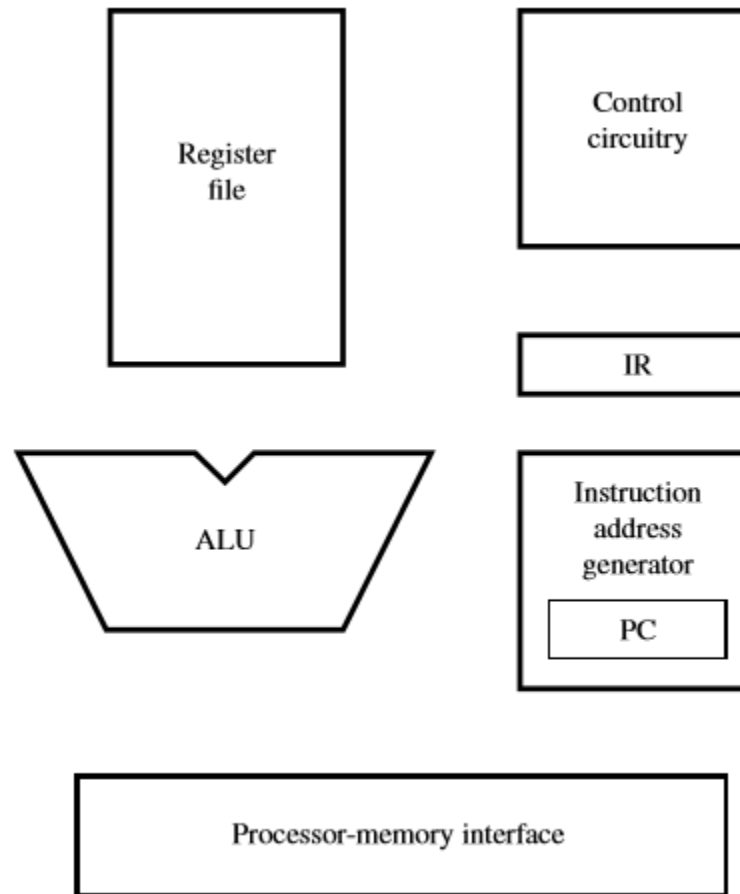3. Carry out the operation specified by the instruction in the IR.

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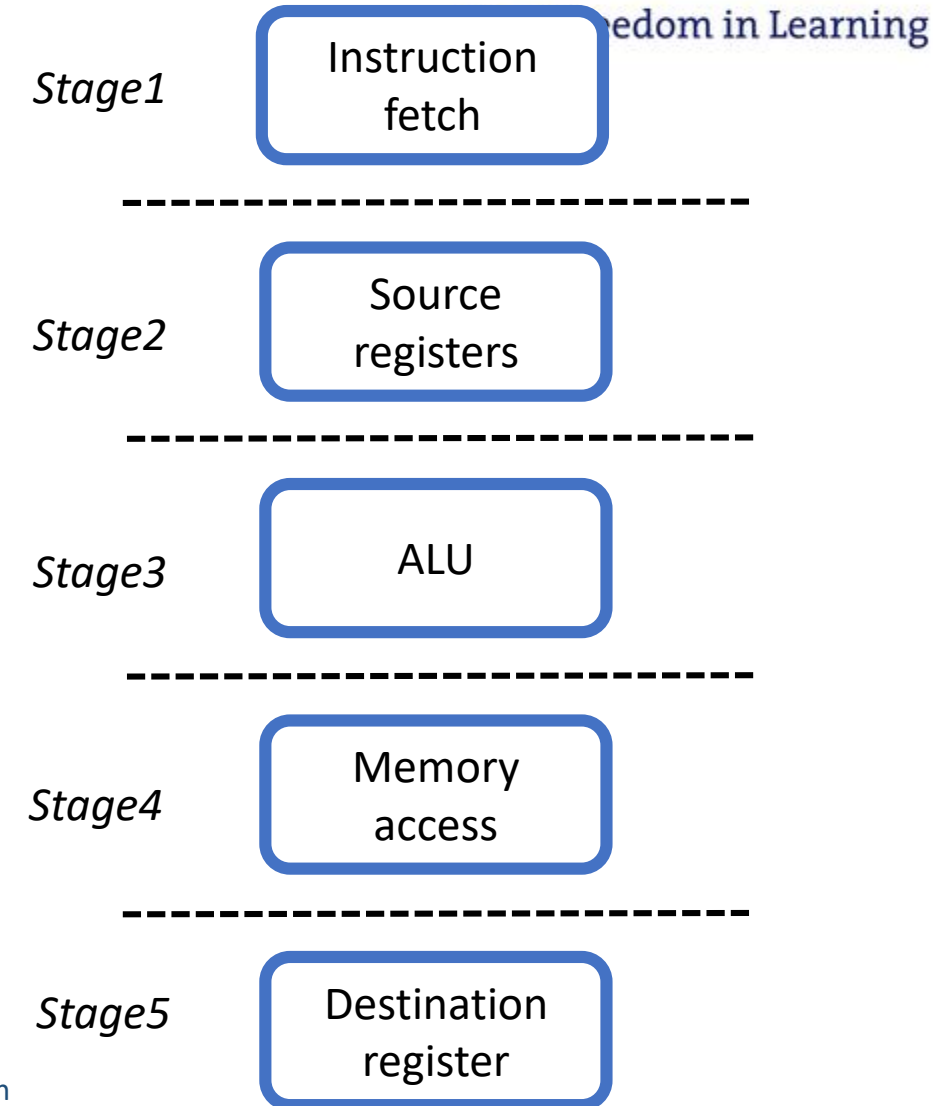Tuba Ayhan

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Data Processing Hardware

Computer Organization and Embedded Systems, Hamacher et. al
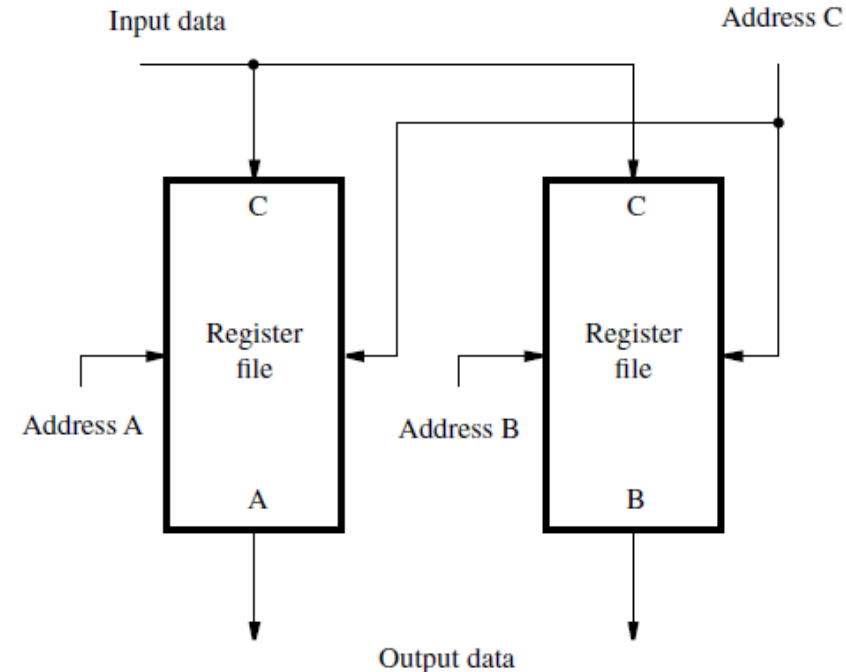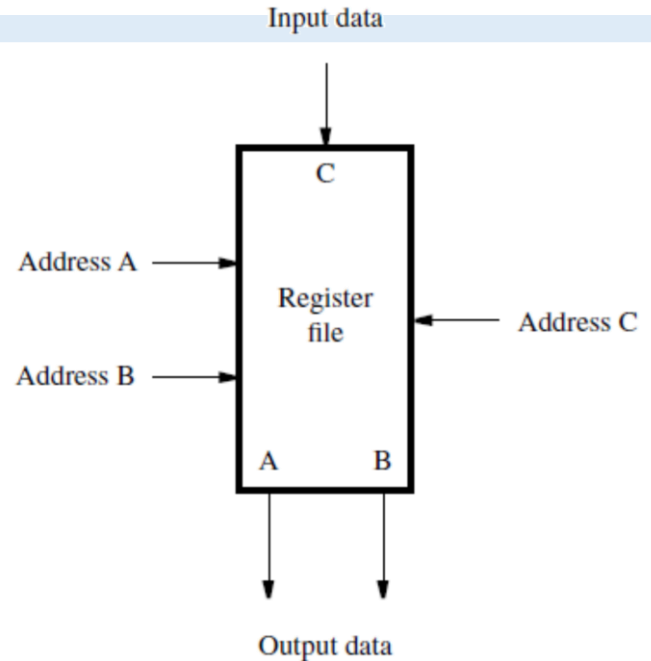
Data Processing Hardware

A five-step sequence to *fetch* and *execute*

Step	Action
1	Fetch an instruction and increment the program counter
2	Decode the instruction and read registers from the register file
3	Perform an ALU operation
4	Read or write memory data if the instruction involves a memory operand
5	Write the result into the destination register, if needed

Stage1 — Instruction fetch

- -

Stage2 — Source registers

- -

Stage3 — ALU

- -

Stage4 — Memory access

- -
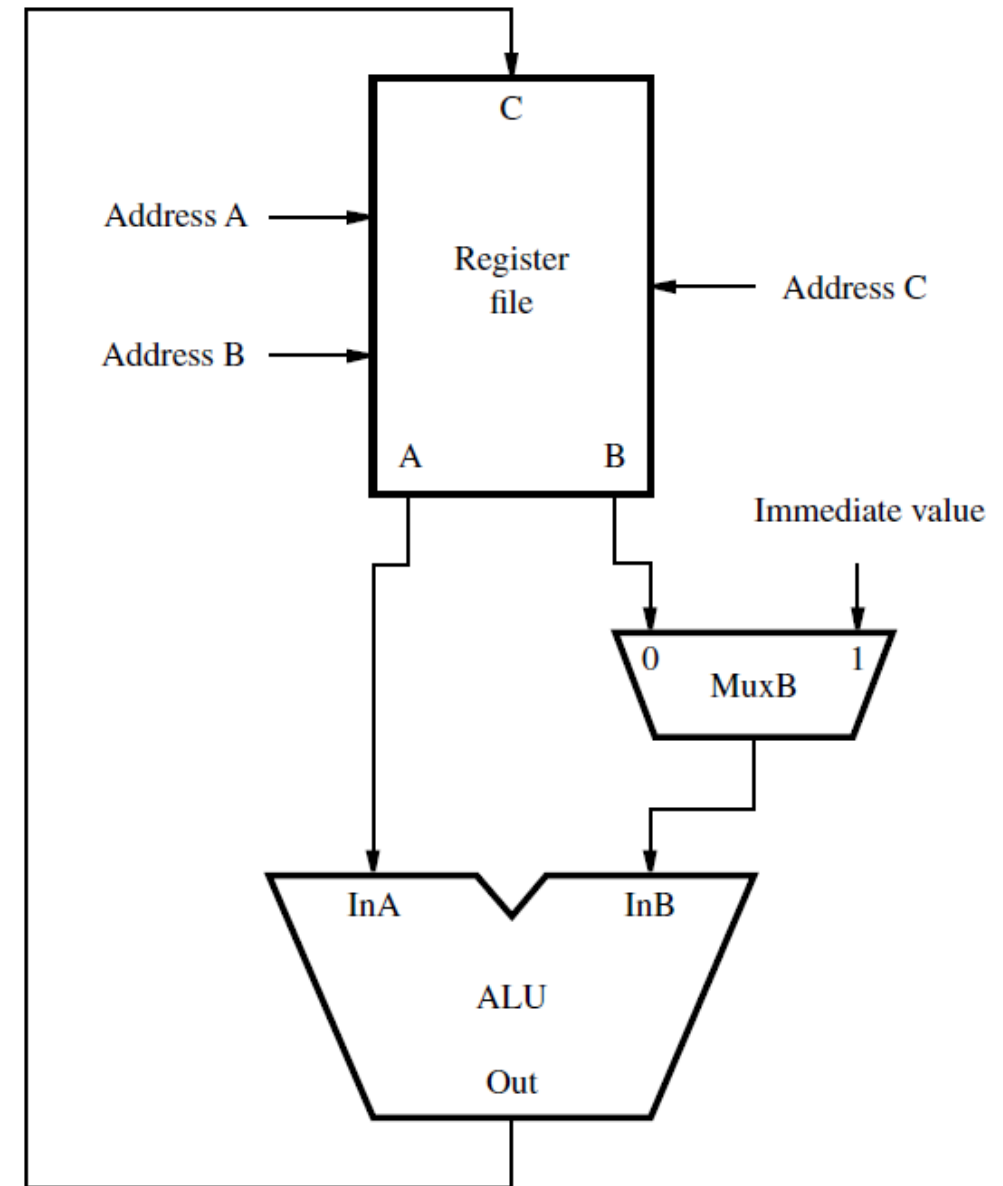
Stage5 — Destination register

Register File

- input and output *ports*: the inputs and outputs of any memory unit.
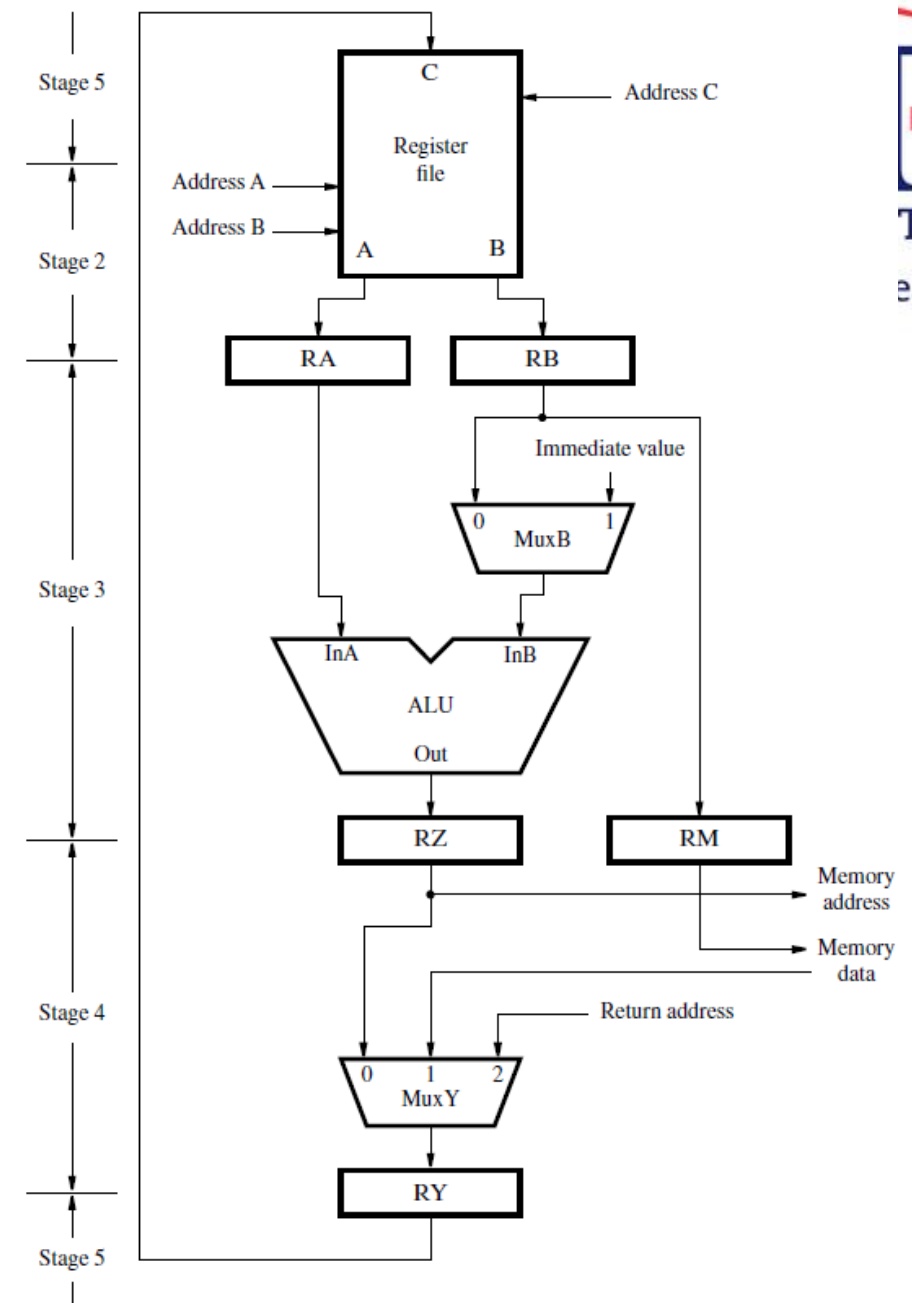- A memory unit that has two output ports is *dual-port*ed.

ALU (arithmetic and logic unit)

- Output A is connected directly to the first input of the ALU.

- Output B is connected to a multiplexer.

- The multiplexer selects either output B of the register file or the immediate value in the IR to be connected to the second ALU input.

Datapath

- Registers between stages
- Hold the results produced in one stage → use as inputs to the next stage
- RA: provides the data to input InA.
- Multiplexer MuxB: forwards either the contents of RB or the immediate value in the IR to InB.
- The ALU constitutes stage 3.
- The result is placed in register RZ. Multiplexer MuxY: selects register RZ to transfer the result of the computation to RY. The contents of RY are transferred to the register file in step 5.

Figure 5.8 Datapath in a processor.

Microprocessors

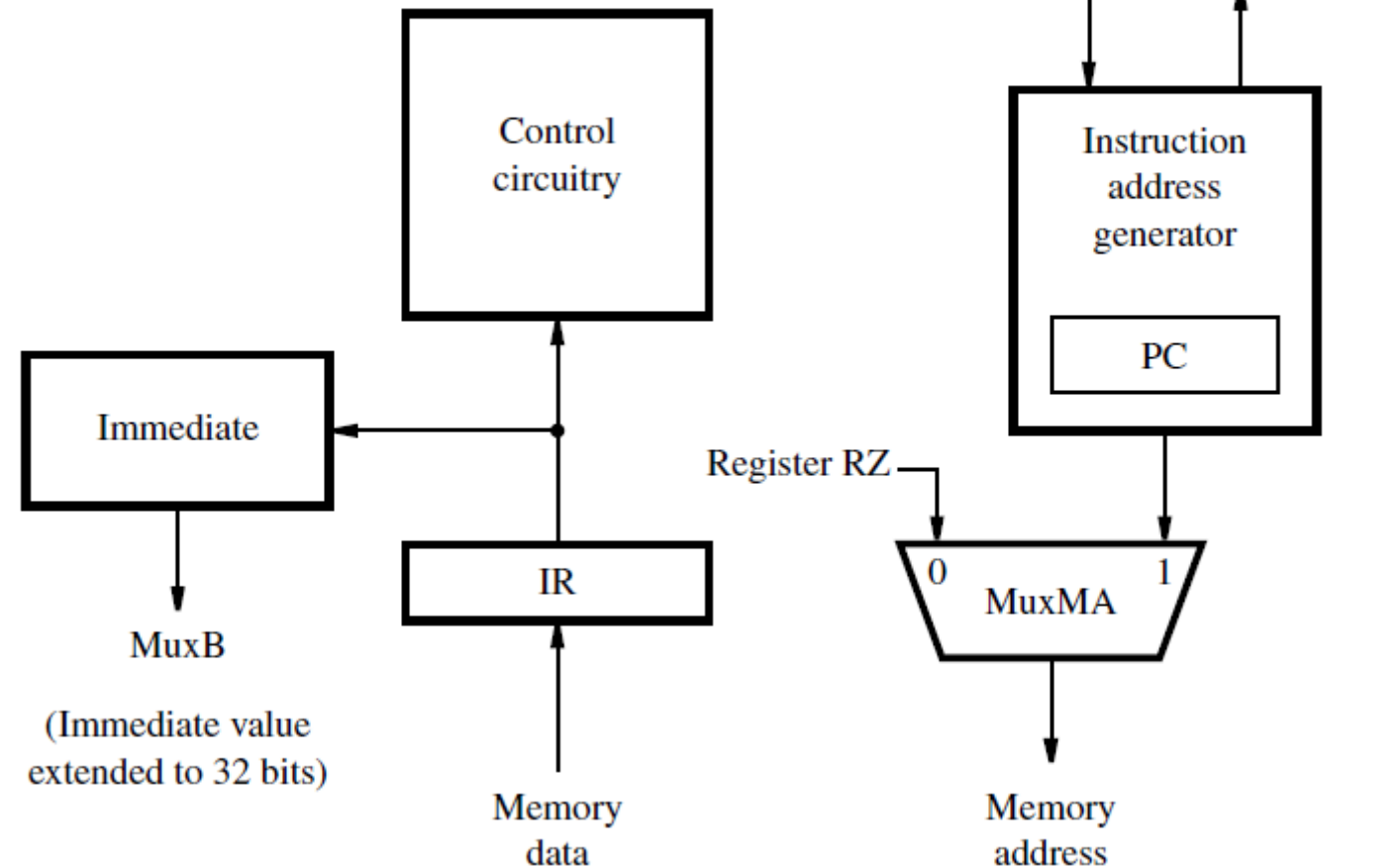Tuba Ayhan

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Data Processing Hardware
Instruction fetch and execution steps

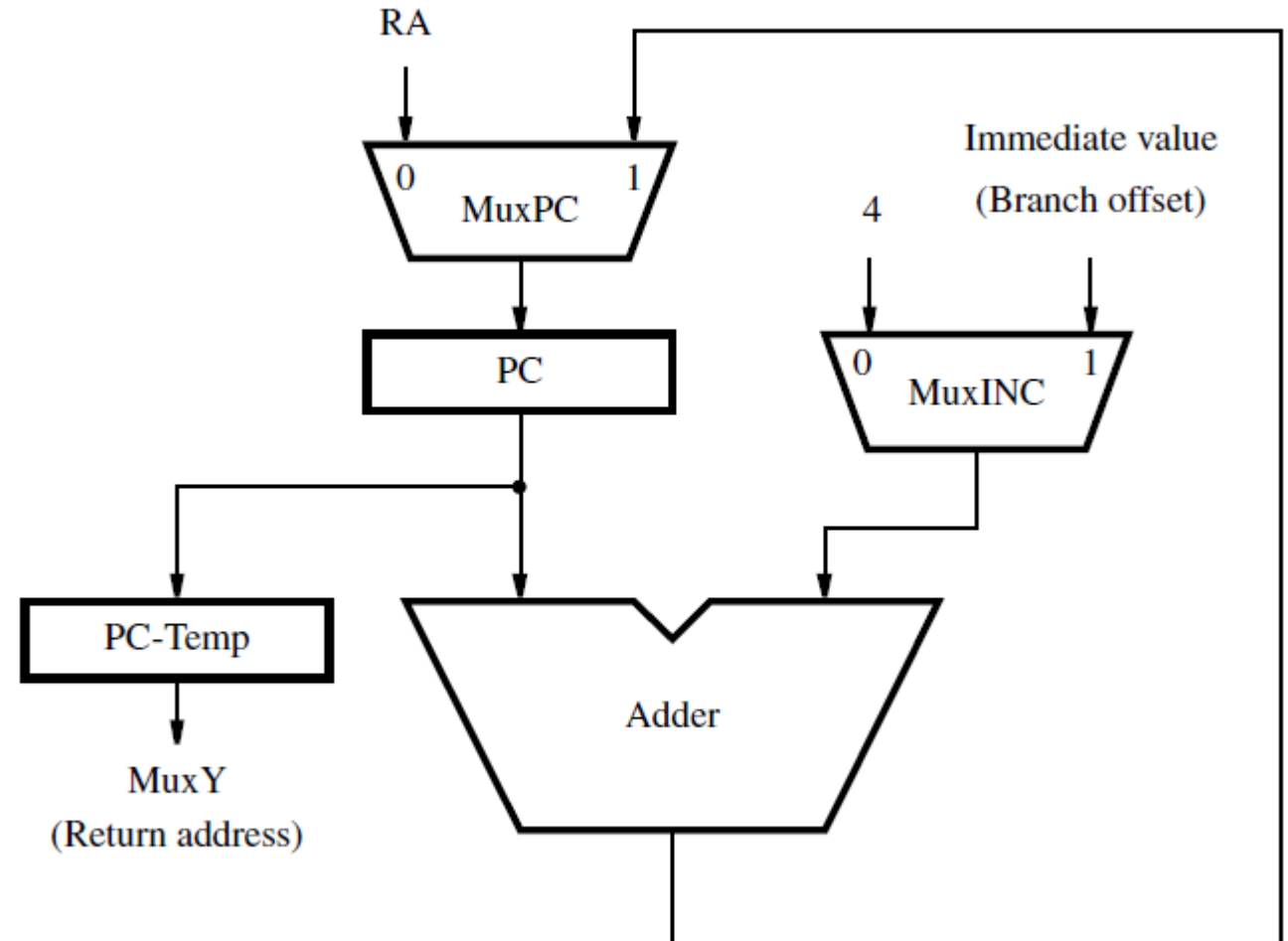Computer Organization and Embedded Systems, Hamacher et. al

Instruction Fetch Section

- Memory address
  - selected by MuxMA:
    - PC (accessing instruction)
    - RZ (accessing operands)
  - Send to the processor-memory interface
- The contents of the IR are examined by the control circuitry to generate the signals needed to control all the processor's hardware.

Register file

(via RA)   (via RY)

Control circuitry

Immediate

MuxB

(Immediate value extended to 32 bits)

IR

Memory data

Instruction address generator

PC

Register RZ

0   MuxMA   1

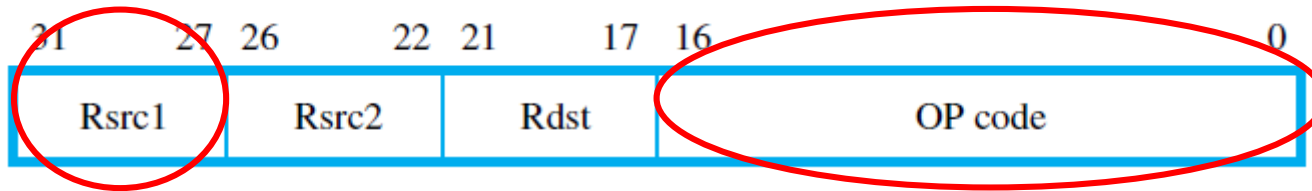Memory address

Instruction address generator

- **MuxINC: selects either**
  - the constant 4: Straight-line execution, or
  - the branch offset to be added to the PC.

- **MuxPC: selects either**
  - the adder output or
  - the output of register RA: executing subroutine linkage instructions.

- **Register PC-Temp: holds the contents of the PC temporarily during (saving the subroutine or interrupt return address)**

Encoding of Machine Instructions - 1

5bits for each address, if there are 32 registers

17 bits remain for OPcode

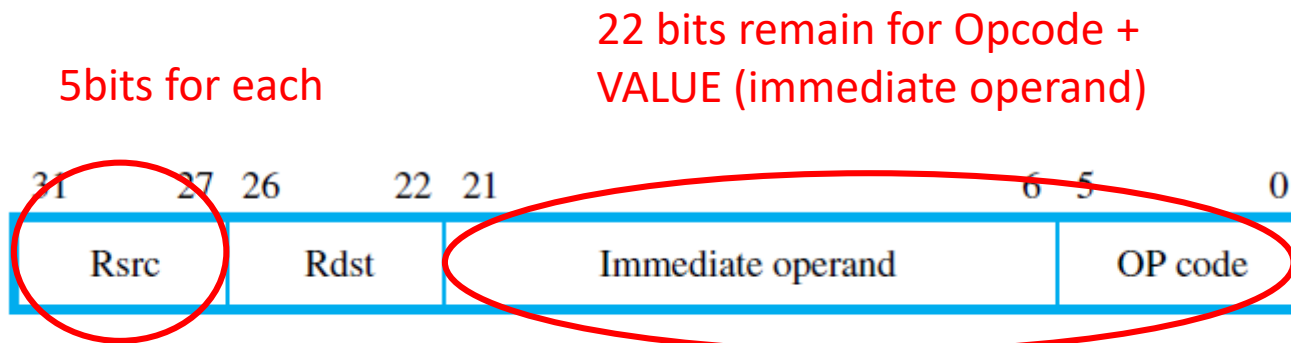| Rsrc1	Rsrc2	Rdst	OP code

31   27   26   22   21   17   16   0

(a) Register-operand format

Add Rdst, Rsrc1, Rsrc2

- Rdst: destination; Rsrc1, and Rsrc2: source of operands.

- OP code: indicates the operation to be performed.

Encoding of Machine Instructions - 2

Add Rdst, Rsrc, #Value

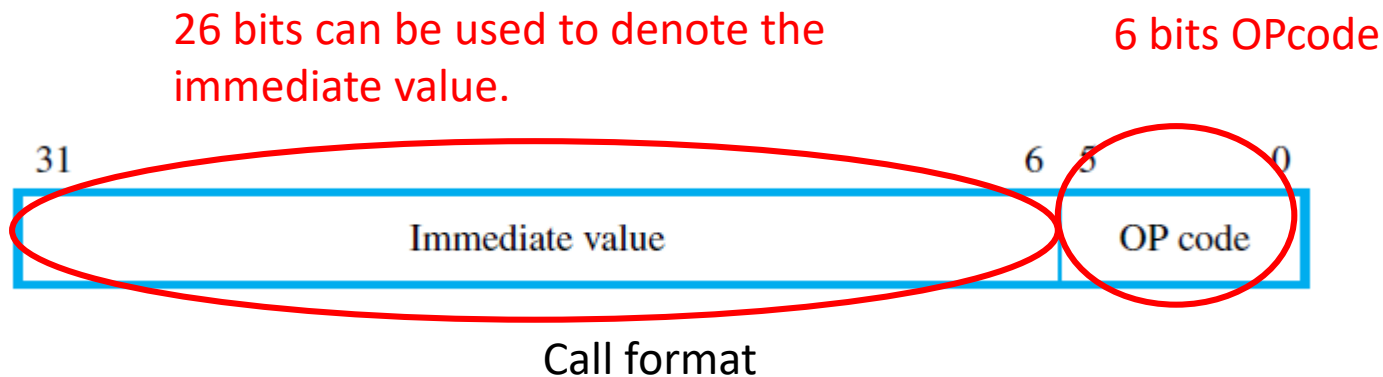useful sizes of immediate operands: are 32, **16**, and 8 bits.

22 bits remain for Opcode + VALUE (immediate operand)

5bits for each

31 27	26 22	21 6	5 0
Rsrc	Rdst	Immediate operand	OP code

(b) Immediate-operand format
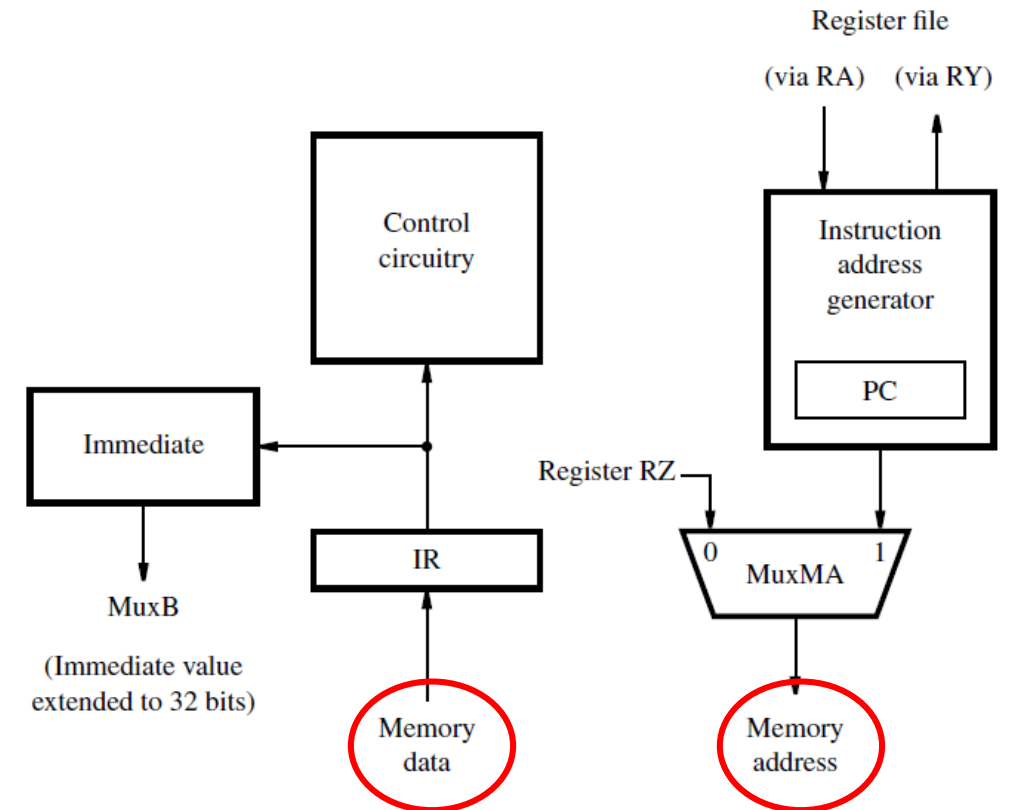
Encoding of Machine Instructions - 3

Call

is used to call a subroutine. It only needs to specify the OP code and an immediate value that is used to determine the
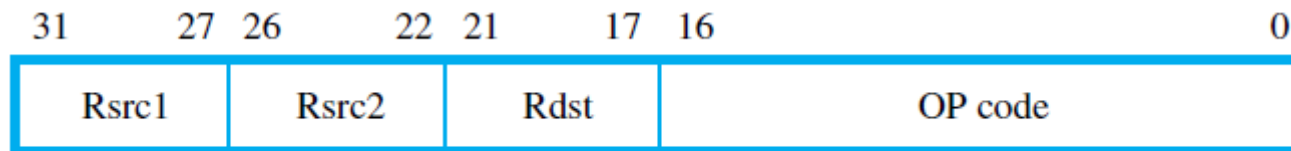
address of the first instruction in the subroutine.

26 bits can be used to denote the immediate value.

6 bits OPcode

31	6	5	0
Immediate value		OP code	

Call format

Add R3, R4, R5

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R4], RB ← [R5]
3	RZ ← [RA] + [RB]
4	RY ← [RZ]
5	R3 ← [RY]

Register file

(via RA)   (via RY)

Control circuitry

Instruction address generator

PC

Immediate

Register RZ

IR

MuxB

(Immediate value extended to 32 bits)

0   1

MuxMA

Memory data

Memory address

Add R3, R4, R5

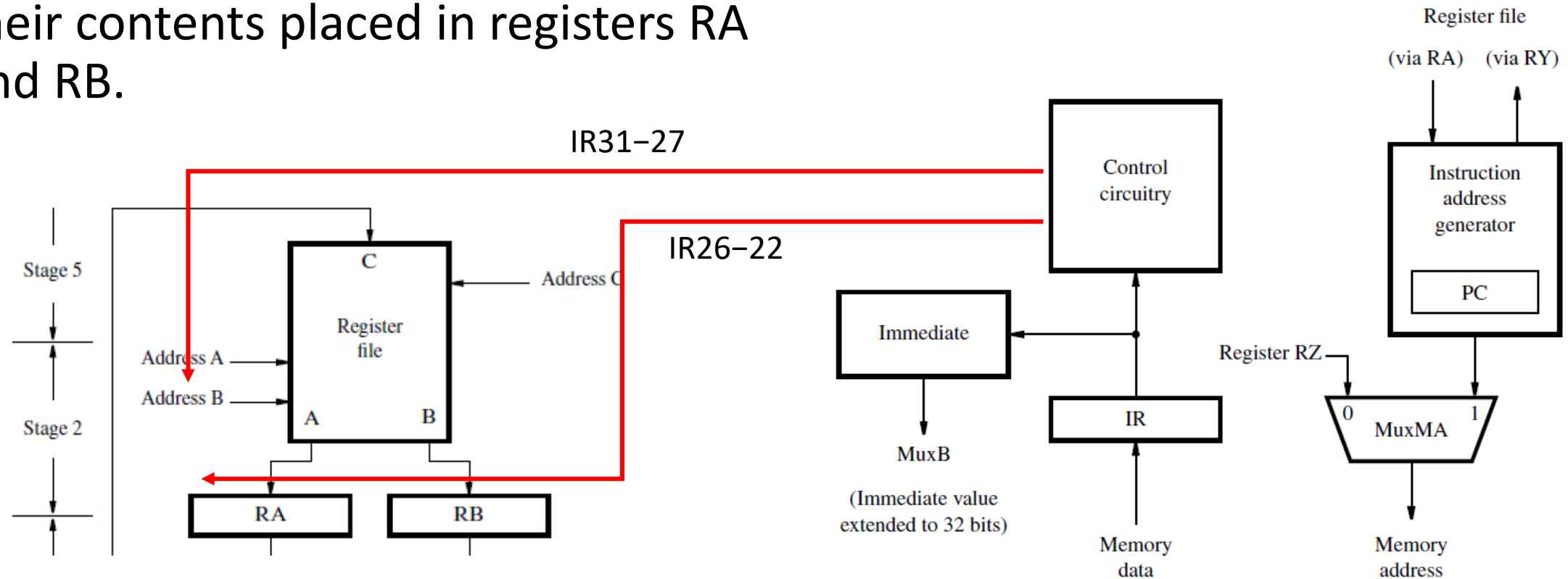| Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R4], RB ← [R5]
3	RZ ← [RA] + [RB]
4	RY ← [RZ]
5	R3 ← [RY]

The source register addresses are available in fields IR31–27 and IR26–22: address inputs for ports A and B of the register file.

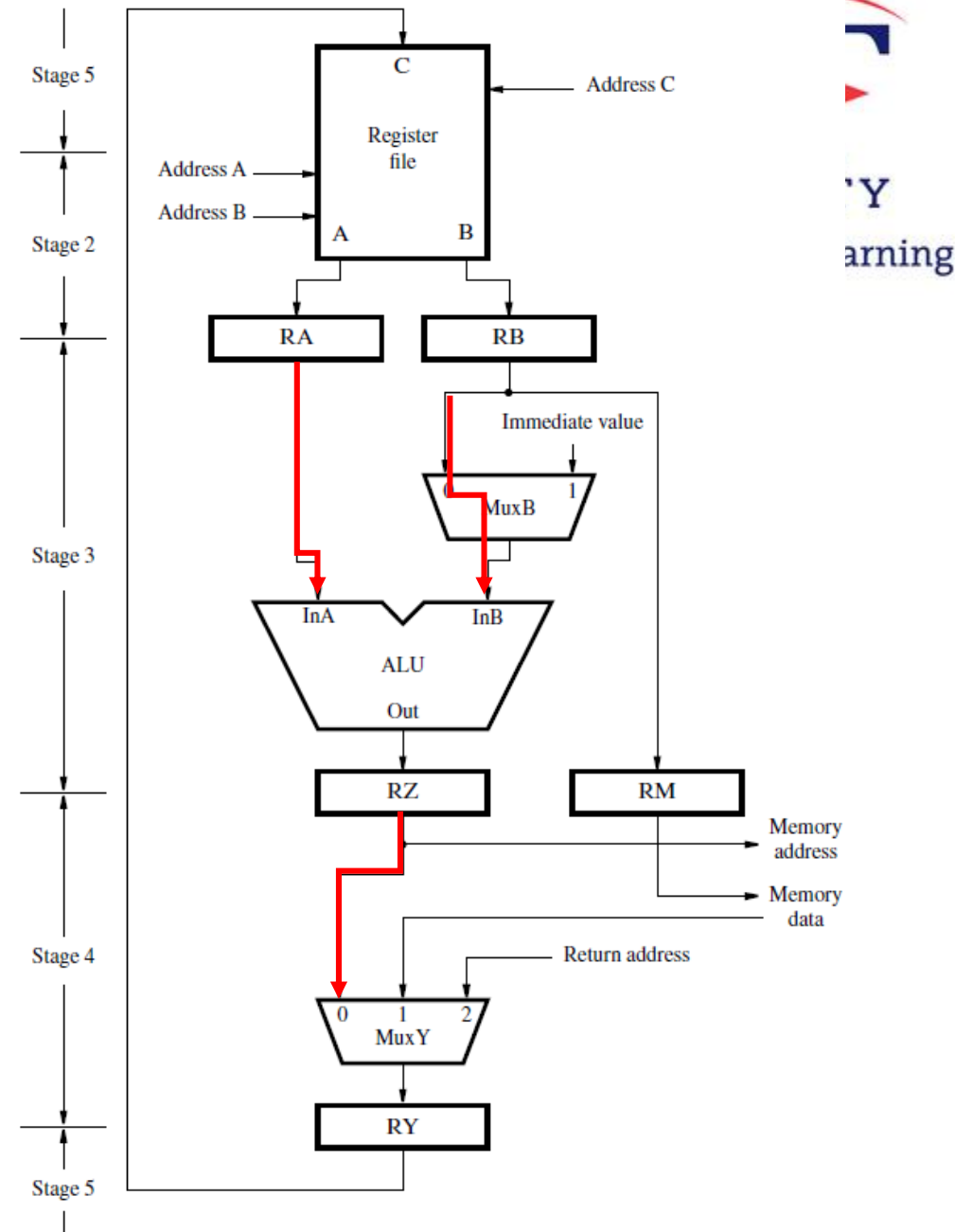| 31	27 26	22 21	17 16	0
Rsrc1	Rsrc2	Rdst	OP code	

(a) Register-operand format

Add R3, R4, R5

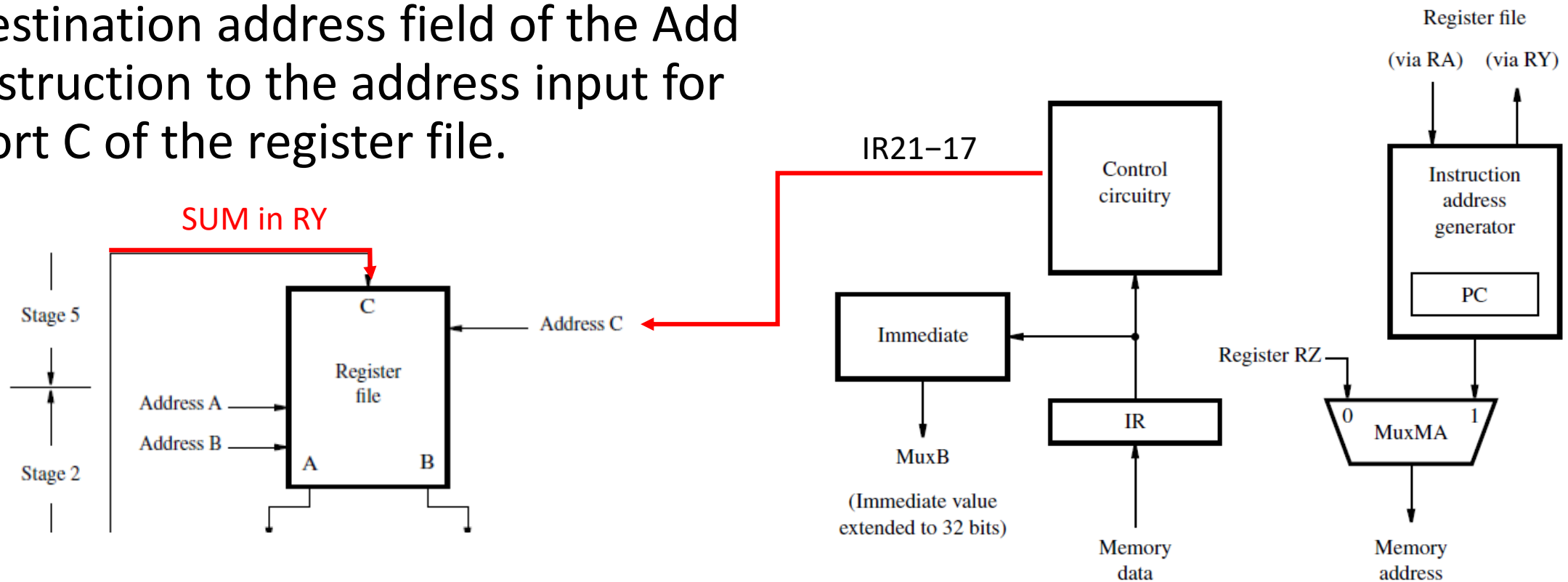- Registers R4 and R5 are read and their contents placed in registers RA and RB.

Add R3, R4, R5

- MuxB: register RB to input InB of the ALU

- RA is connected to input InA, the ALU produces the required sum [RA] + [RB], which is loaded into register RZ at the end of step 3.

- MuxY selects input 0: the contents of RZ is transferred to RY.

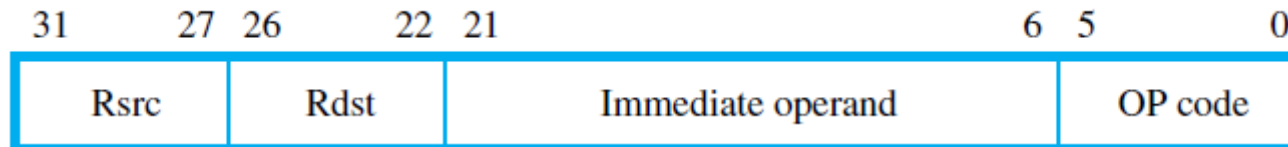**Figure 5.8** Datapath in a processor.

Add R3, R4, R5

- The control circuitry connects the destination address field of the Add instruction to the address input for port C of the register file.

Load R5, X(R7)

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R7]
3	RZ ← [RA] + Immediate value X
4	Memory address ← [RZ], Read memory, RY ← Memory data
5	R5 ← [RY]

31	27 26	22 21	6 5	0
Rsrc	Rdst	Immediate operand	OP code	

(b) Immediate-operand format

- the address of the destination register is given in bit field IR26–22.

Load R5, X(R7)

- Index mode addressing: X is given as an immediate value.

- The immediate field of IR, is selected by MuxB in step 3 and added to the contents of register RA. The resulting sum is the effective address of the operand.
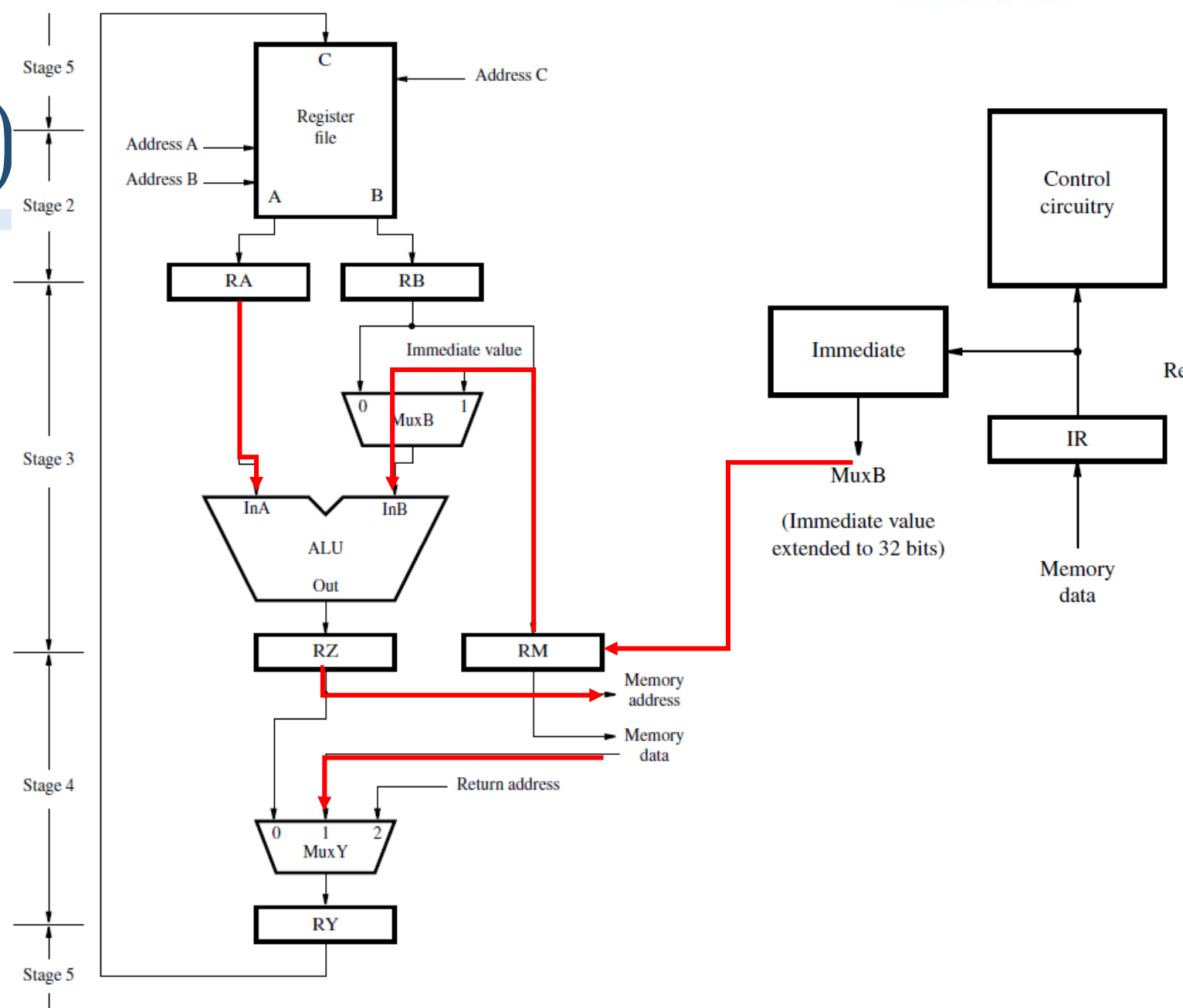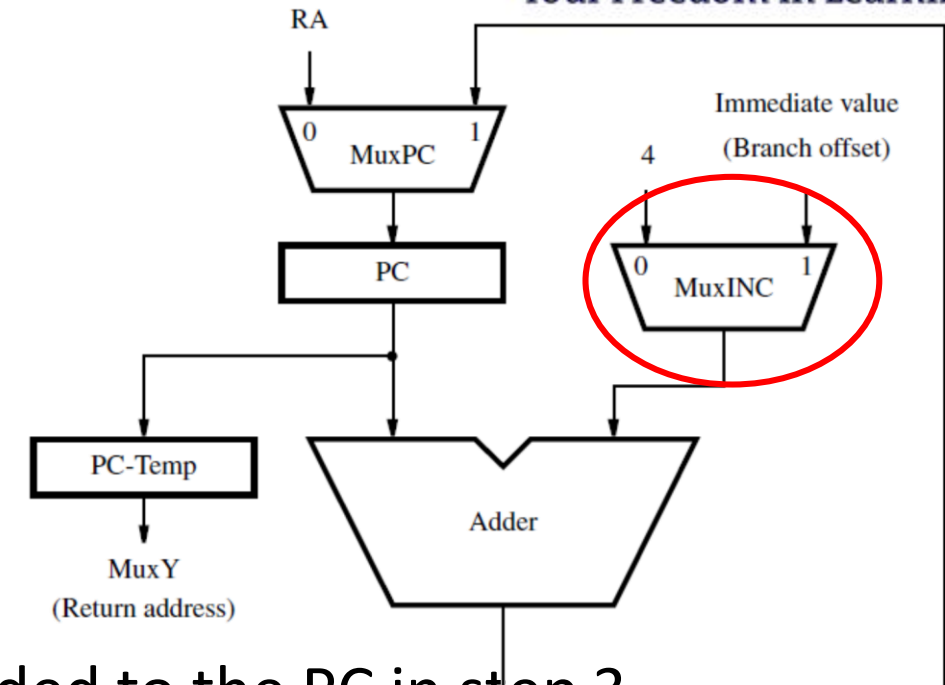

Figure 5.8 Datapath in a processor.

Branching

- Unconditional branch:

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction
3	PC ← [PC] + Branch offset
4	No action
5	No action

- MuxINC selects the **branch offset** in the IR to be added to the PC in step 3.
- **Branch offset**: the distance between the branch target and the memory location following the branch instruction
- Execution of a Branch instruction is completed in step 3.

Branching – Conditional

Branch_if_[R5]=[R6] LOOP

- branch if the contents of registers R5 and R6 are identical.

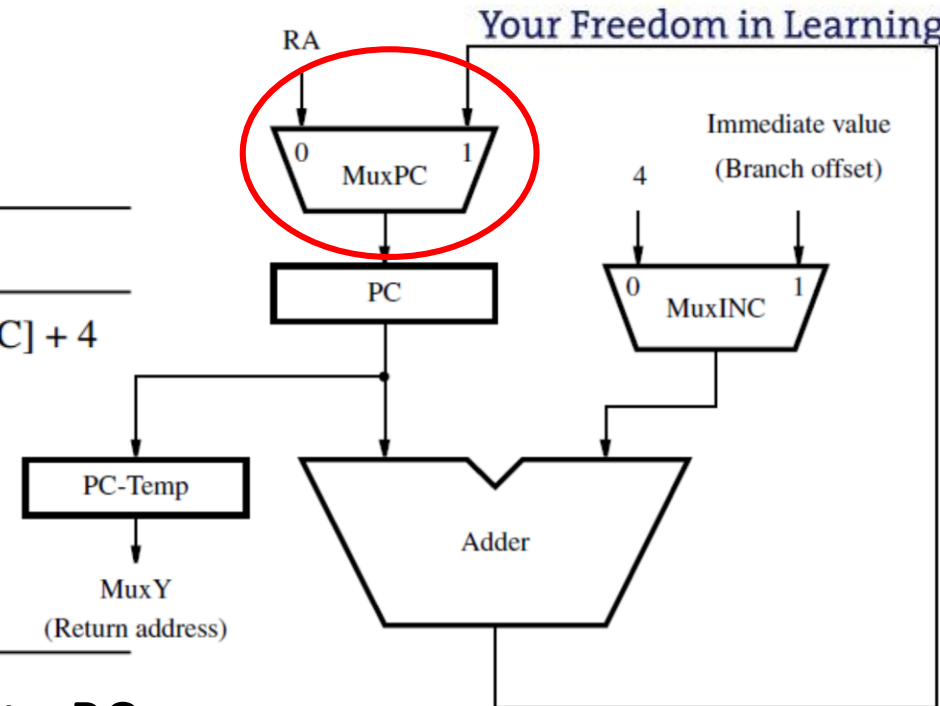| Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R5], RB ← [R6]
3	Compare [RA] to [RB], If [RA] = [RB], then PC ← [PC] + Branch offset
4	No action
5	No action

- Registers R5 and R6 are read in step 2 and compared in step 3:
  - Subtraction [R5] − [R6] in the ALU. The ALU generates signals that indicate whether the result is positive, negative, or zero. The ALU also indicate arithmetic overflow and carry out.
  - Examine the contents of registers RA and RB and produce the condition signals: greater than, equal, less than, etc

Branching Subroutine Call Instructions

Call_Register R9

- calls a subroutine whose address is in register R9.

Step	Action
1	Memory address ← [PC], Read memory, IR ← Memory data, PC ← [PC] + 4
2	Decode instruction, RA ← [R9]
3	PC-Temp ← [PC], PC ← [RA]
4	RY ← [PC-Temp]
5	Register LINK ← [RY]

- MuxPC selects its 0 input : content of RA is loaded into PC.
- Return address of the subroutine (previous contents of the PC) is saved in the register file (LINK).
- Subroutine return instruction: register LINK is read and its contents are placed in RA, then transferred to the PC via MuxPC.
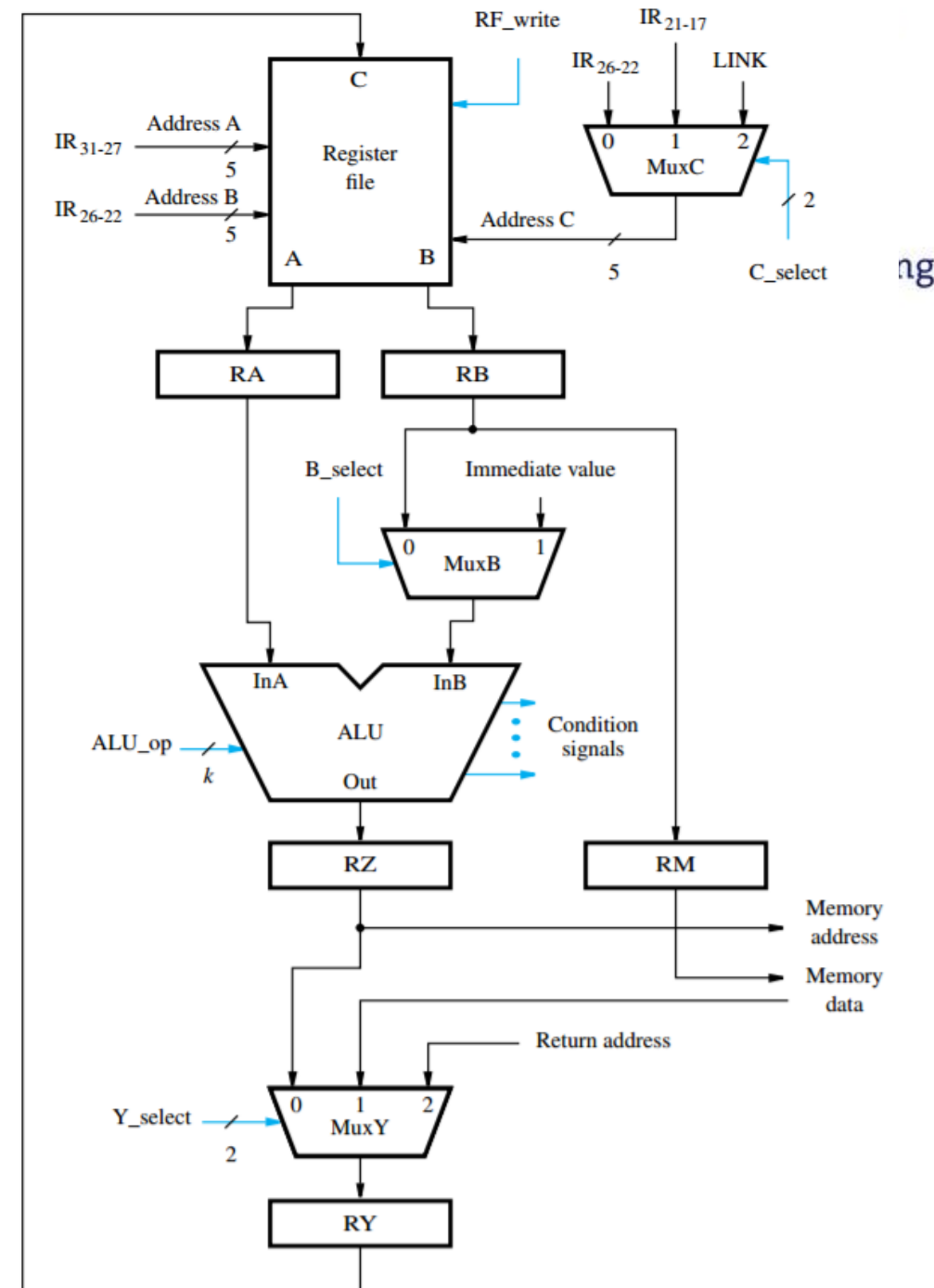
Microprocessors

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Data Processing Hardware
Control signals

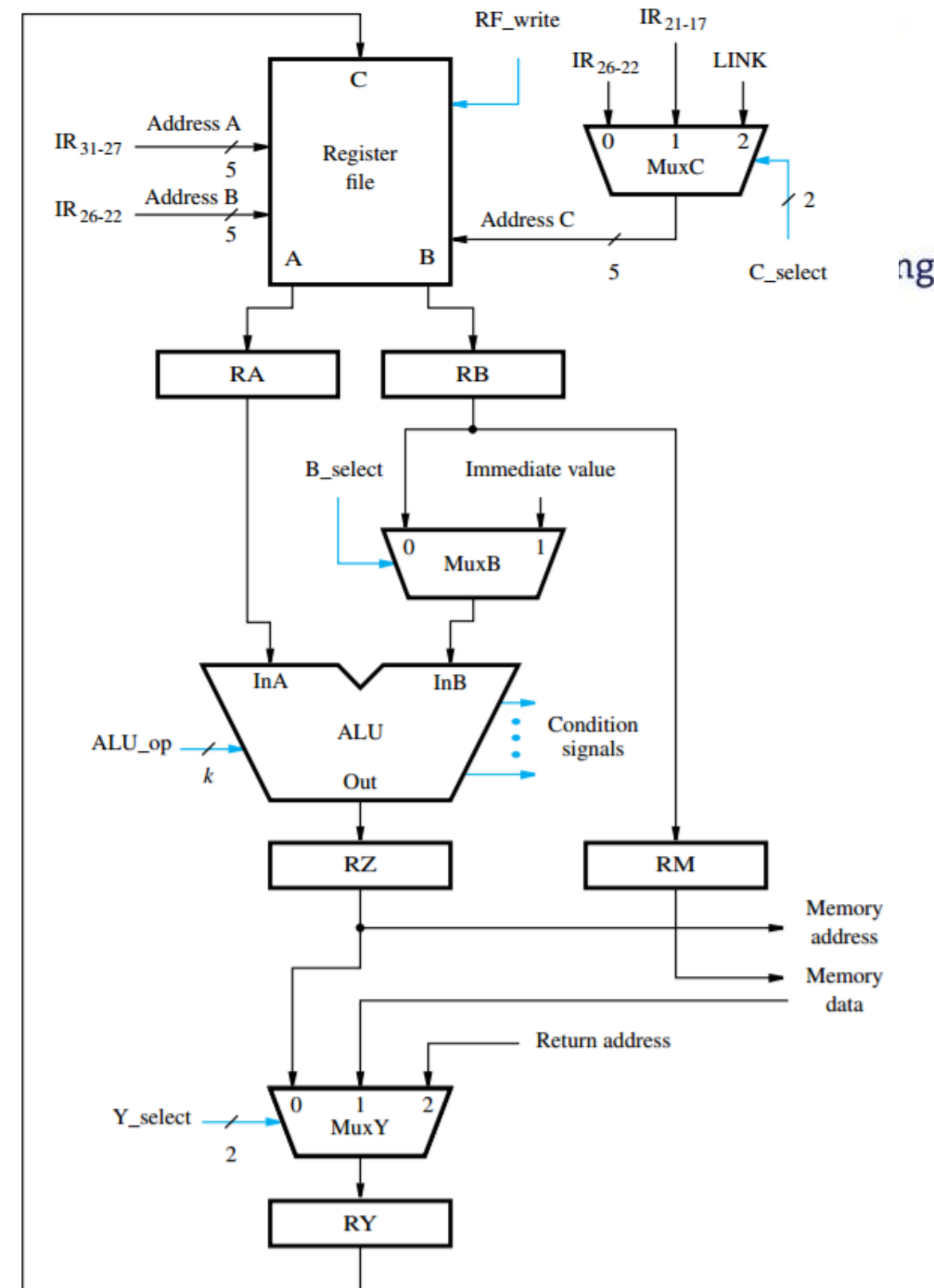Computer Organization and Embedded Systems, Hamacher et. al

Control signals – datapath

- Registers:
  - inter-stage registers (RA, RB, RZ, RY, RM, and PC-Temp) are always enabled: data are transferred from one stage to the next in every clock cycle.
  - PC, the IR, and the register file: New data are loaded only when called for in a particular processing step.
- MUX:
  - MuxB selects between an immediate source operand or offset to compute the effective address of a memory operand and RB. Works in step 3.
  - MuxY selects the PC as the source of the memory address during step 1, when a new instruction is being fetched. During step 4 of Load and Store instructions, it selects register RZ, which contains the effective address of the memory operand.
  - MuxC: Address C, selects the destination register. Three-register instructions use bits IR21–17 and other instructions use IR26–22 to specify the destination register. The address of the link register used in subroutine linkage instructions.
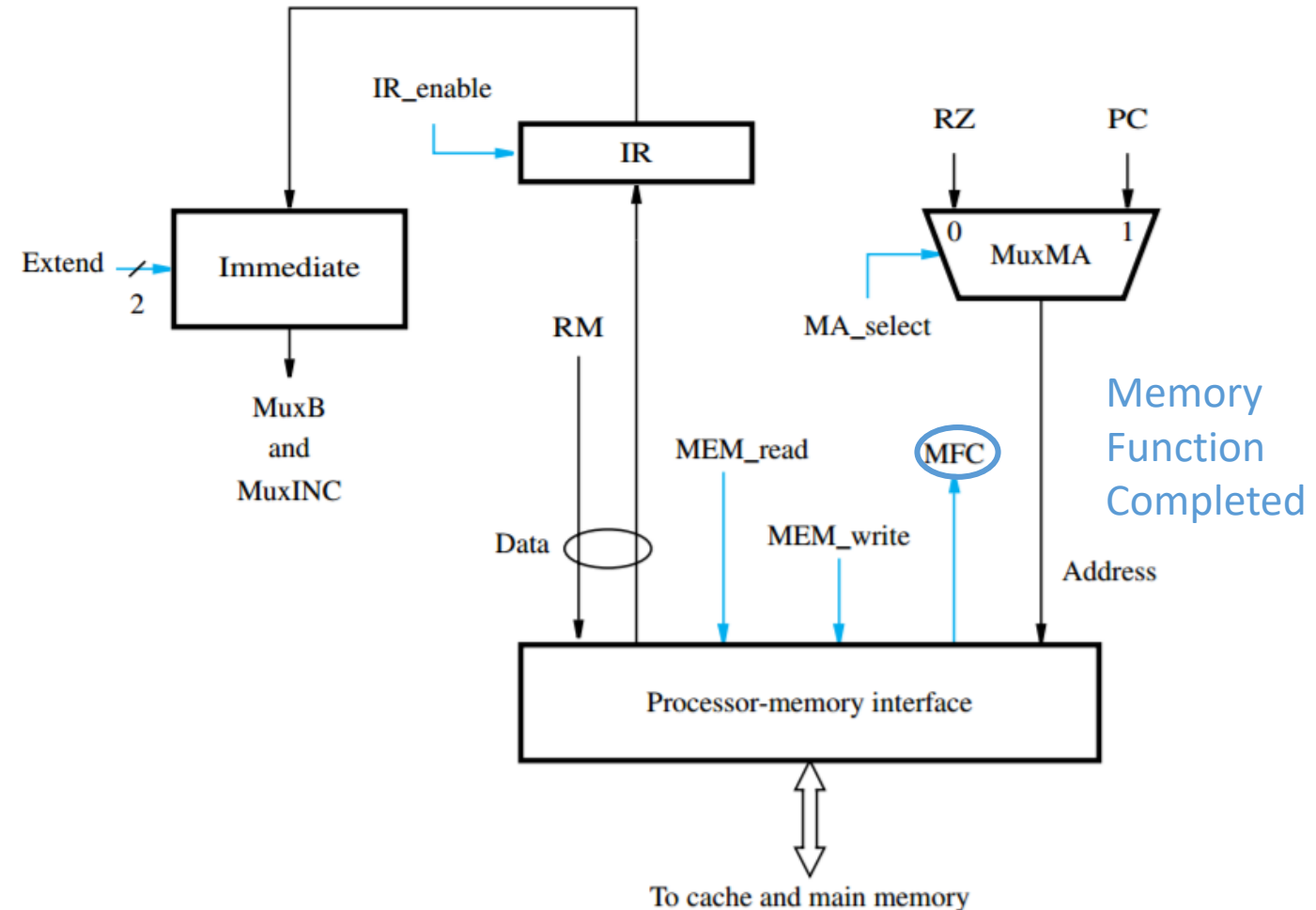
Control signals – datapath

- New data are loaded into the selected register only when the control signal **RF_write** is asserted.

- **ALU_op:** The operation performed by the ALU is determined by a k-bit control code which can specify up to 2k distinct operations (Add, Subtract, AND, OR, and XOR...)

- ALU generates **condition signals** that indicate the result of the comparison.
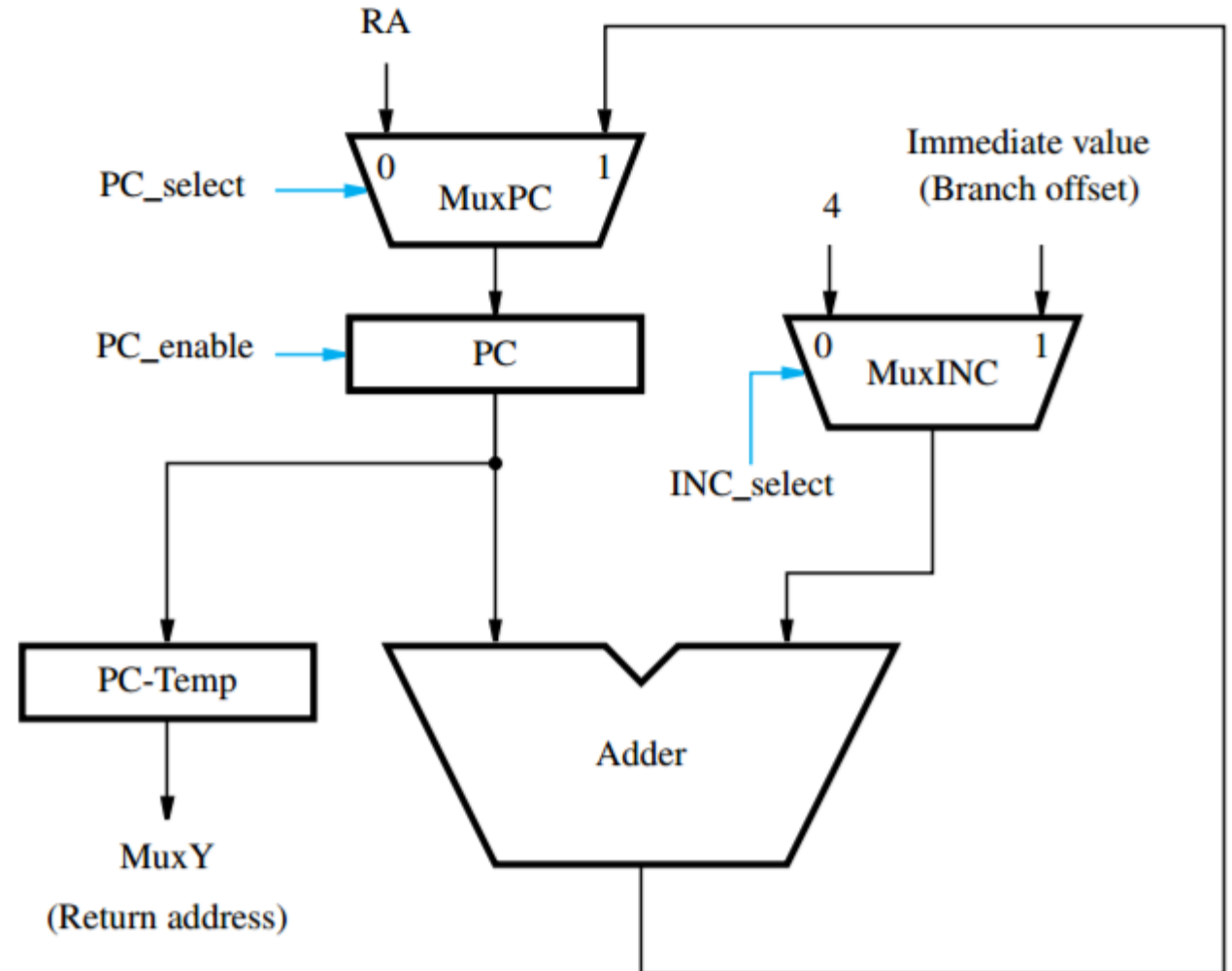
Control signals – Processor-memory interface and IR

- MEM_read and MEM_write are used to initiate a memory Read or a memory Write operation. Operation completed: the MFC signal is asserted.

- **IR_enable**: enables a new instruction to be loaded into the register. During a fetch step, it must be activated only after the MFC signal is asserted.

- **Immediate** block handles three possible formats for the immediate value: a sign-extended 16-bit value, a zero-extended 16-bit value, and a 26-bit value that is handled in a special way. **Extend**: comprises two bits.

Memory Function Completed

Control signals – instruction address generator

- The INC_select signal selects the value to be added to the PC, either the constant 4 or the branch offset specified in the instruction. The PC_select signal selects either the updated address or the contents of register RA to be loaded into the PC when the PC_enable control signal is activated.

Generation of control signals

- The **control signal generator** is a combinational circuit that produces the necessary control signals based on all its inputs.

- The **instruction decoder** interprets the OP-code and addressing mode information in the IR and asserts the corresponding INSi output.

- The **step counter** indicates the step from 1 to 5, every clock cycle.