1. Interrupt example: Ticking bomb

When a key is pressed, a bob is activated. If one writes the correct password and presses enter key in 3 minutes, the bomb is deactivated. After the bomb is activated, remaining time is shown on the seven-segment display. The system receives interrupts from 3 devices: KEYS, PRIV_TIMER and HPS_TIMER which are serviced by KEY_ISR, PRIV_ISR and HPS_ISR, respectively. When an interrupt occurs, the processors goes into IRQ mode and the following SERVICE_IRQ subroutine is executed. Complete the code and draw flowchart for this code piece.

```
SERVICE_IRQ:
/* save the first 8 general purpose registers and the link
register. */
     PUSH        {R0-R7, LR}

     /* Read the ICCIAR from the CPU interface */

     LDR         R4, =MPCORE_GIC_CPUIF

     LDR         R5, [R4, #ICCIAR]        // read the interrupt ID


PRIV_TIMER_CHECK:

     CMP         R4, #MPCORE_PRIV_TIMER_IRQ // check for priv.
timer interrupt

     /* If the interrupt source is private timer, go to the
private timer interrupt service routine then exit from IRQ mode.
Else, go check if the HPS timer requested an interrupt */


     BNE   HPS_TIMER_CHECK

     BL    PRIV_ISR

     B     EXIT_IRQ


HPS_TIMER_CHECK:
     /* check for HPS timer interrupt */

     CMP         R4, #HPS_TIMER0_IRQ

     /* If the interrupt source is HPS timer, go to its
interrupt service routine then exit from IRQ mode. Else, go
check if the KEY requested an interrupt */

     BNE   KEYS CHECK

     BL    HPS_ISR

     B     EXIT_IRQ
```

KEYS_CHECK:
/* check for KEYS interrupt. If the interrupt source is KEYS, go to its interrupt service routine then exit from IRQ mode. Else, the interrupt is not recognized, stop there */

```
UNEXPECTED:     BNE   UNEXPECTED

                BL    KEYS_ISR

                B     EXIT_IRQ
```

EXIT_IRQ:
/* Write to the End of Interrupt Register (ICCEOIR), bring the saved general purpose registers back and go back to the main routine. */

```
        STR       R5, [R4, #ICCEOIR]

        POP       {R0-R7, LR}
        SUBS      PC, LR, #4
```

2. Configure Timer: Ticking bomb

Configure the private timer to hold 3 minutes. The timer should be disabled until the bomb is activated. It should be configured to request interrupt and stop counting after reaching zero. Show how you calculate the load value and the control word. Write comments for your code.

Hints to survive the traps in this question:

a. 2^{32}=4.294.967.294

b. `MOV Rd, #imm16`   `imm16` is an immediate value in the range 0-65535. `imm16` can be 16 bit.

2.4.1 ARM A9 MPCore Timers

Figure 3 shows the registers in the programmer's interface for each A9 core private timer. These registers have the base address 0xFFFEC600, as shown in the figure, and can be read or written using word accesses. To use the timer, it is necessary to first write an initial count value into the *Load* register. The timer can then be started by setting the enable bit *E* in the *Control* register to 1, and it can be stopped by setting *E* back to 0. Once enabled the timer decrements its count value until reaching 0. When it reaches 0, the timer sets the *F* bit in the *Interrupt status* register. The *F* bit can be checked by software using polled-I/O to determine when the timer period has expired. The *F* bit can be reset to 0 by writing a 1 into it. Also, if bit *I* in the *Control* register is set to 1, then a processor interrupt can be generated when the timer reaches 0. Using interrupts with the timer is discussed in Section 3.

When it reaches 0, the timer will stop if the auto bit (*A*) in the control register is set to 0. But if bit *A* is set to 1, then the timer will automatically reload the value in the *Load* register and continue decrementing. The current value of the timer is available to software in the *Counter* register shown in Figure 3. The timer uses a clock frequency of 200 MHz. The *Prescaler* field in the *Control* register can be used to slow down the counting rate, as follows. The timer decrements each *Prescaler* +1 clock cycle. Therefore, if *Prescaler* = 0, then the timer decrements every clock cycle, if *Prescaler* = 1, the timer decrements every second clock cycle, and so on.

Address	31 · · · 16	15 · · · 8	7 3	2	1	0	Register name
0xFFFEC600	Load value						Load
0xFFFEC604	Current value						Counter
0xFFFEC608	Unused	Prescaler	Unused	I	A	E	Control
0xFFFEC60C	Unused					F	Interrupt status

Figure 3. ARM A9 private timer port.

With 200MHz, load value should be 36.000.000.000, which is approximately 9 times the maximum 32-bit load value. Load value can be 4.000.000.000 with a prescaler of 9. Interrupts should be enabled and auto bit should be cleared. The timer will be enabled after the bomb is activated, not at after configuration.

```
LDR R0, =0xFFFEC600    // timer base address
LDR R1, =4000000000    // load value
STR R1, [R0]           // write the load value
MOV R1,#0x0904         // control word 0b0000100100000100
STR R1, [R0, #8]       // write the control value
```

3. Floating point

You are asked to find the square root of a floating point number, approximately. The number is given in the excess-127 representation. Propose a method without using floating point co-processor. Plot the flowchart. Input is A with SA, E'A, and MA which are the sign, excess-127 exponent, and mantissa fraction, respectively. Square root of A is B with SB, E'B, and MB.

Hint 1: $\sqrt{(x)} = x^{\frac{1}{2}}$

Hint 2: $\sqrt{(negative\_numbers)} \rightarrow$ exception

$$\text{Value represented} = \pm 1.M \times 2^{E'-127}$$
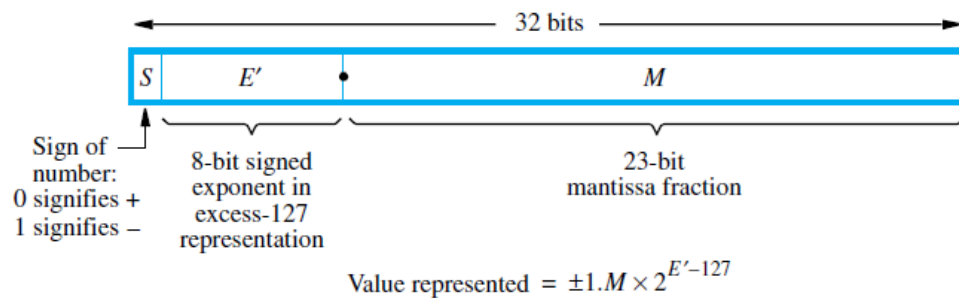
4. Fill in the blanks. Avoid abbreviations.

Bit line
Word line

A. A single transistor RAM cell is given in the figure. Information is stored in the form of a charge on a capacitor. This charge can be maintained for only tens of milliseconds. In order not to lose data, <u>REFRESH</u> _____ is required. Therefore, this type of RAM is called <u>DYNAMIC RAM</u>_____.

T

C
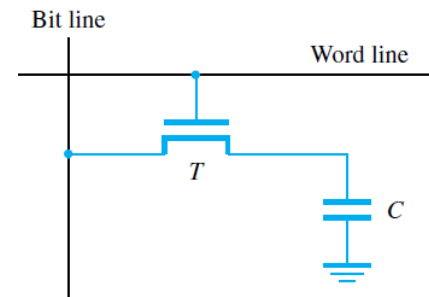
B. Figure shows a 512K × 8 static memory chip. How many of these chips are required to organize a 2M × 32 memory module?

____<u>16</u>_____

Which logic block is required to generate chip-select signals of the memory chips?

_____<u>2x4 DECODER</u>_____

512K × 8 memory chip

19-bit address → | | ← 8-bit data input/output

↑ Chip-select