Example 6-3 Examples of different ARM instructions showing a variety of operand 2 types:

```
add     R0, R1, #1              R0 = R2 + 1
add     R0, R1, R2              R0 = R1 + R2
add     R0, R1, R2, LSL #4      R0 = R1 + R2<<#4
add     R0, R1, R2, LSL R3      R0 = R1 + R2<<R3
```

Example 6-4 Examples of addressing modes

```
(1)  LDR     R0, [R1] @ address pointed to by R1
(2)  LDR     R0, [R1, R2] @ address pointed to by R1 + R2
(3)  LDR     R0, [R1, R2, LSL #2] @ address is R1 + (R2*4)
(4)  LDR     R0, [R1, #32]! @ address pointed to by R1 + 32, then R1:=R1 + 32
(5)  LDR     R0, [R1], #32 @ read R0 from address pointed to by R1, then R1:=R1 + 32
```

Table 6-1 Conditional execution suffixes

Suffix	Flags	Description
EQ	Z=1	zero (EQual to 0)
NE	Z=0	not zero (Not Equal to 0)
CS/HS	C=1	Carry Set / unsigned Higher or Same
CC/LO	C=0	Carry Clear / unsigned LOwer
MI	N=1	negative (MInus)
PL	N=0	positive or zero (PLus)
VS	V=1	sign overflow (oVerflow Set)
VC	V=0	no sign overflow (oVerflow Clear)
HI	C=1 AND Z=0	unsigned HIgher
LS	C=0 OR Z=1	unsigned Lower or Same
GE	N=V	signed Greater or Equal
LT	N != V	signed Less Than
GT	Z=0 AND N=V	signed Greater Than
LE	Z=1 OR N != V	signed Less or Equal
AL	-	ALways (default)

Table 6-3 Summary of data processing operations in assembly language

Opcode	Operands	Description	Function
Arithmetic operations			
ADC	Rd, Rn, Op2	Add with Carry	Rd = Rn + Op2 + C
ADD	Rd, Rn, Op2	Add	Rd = Rn + Op2
MOV	Rd, Op2	Move	Rd = Op2
MVN	Rd, Op2	Move NOT	Rd = ~Op2
RSB	Rd, Rn, Op2	Reverse Subtract	Rd = Op2 – Rn
RSC	Rd, Rn, Op2	Reverse Subtract with Carry	Rd = Op2 – Rn - !C
SBC	Rd, Rn, Op2	Subtract with carry	Rd = Rn – Op2 -!C
SUB	Rd, Rn, Op2	Subtract	Rd = Rn – Op2
Logical operations			
AND	Rd, Rn, Op2	AND	Rd = Rn & Op2
BIC	Rd, Rn, Op2	Bit Clear	Rd = Rn & ~ Op2
EOR	Rd, Rn, Op2	Exclusive OR	Rd = Rn ^ Op2
ORR	Rd, Rn, Op2	OR	Rd = Rn | Op2 (OR NOT) Rd = Rn | ~Op2
Flag Setting instructions			
CMP	Rn, Op2	Compare	Rn – Op2
CMN	Rn, Op2	Compare Negative	Rn + Op2
TEQ	Rn, Op2	Test EQuivalence	Rn ^ Op2
TST	Rn, Op2	Test	Rn & Op2

LDR{Type}
- B – unsigned Byte. (Zero extend to 32 bits on loads.)
- SB – signed Byte. (Sign extend to 32 bits.)
- H – unsigned Halfword. (Zero extend to 32 bits on loads.)
- SH – signed Halfword. (Sign extend to 32 bits.)

or omitted, for a Word load.

STR{Type}
- B – unsigned Byte
- H – unsigned Halfword

or omitted, for a Word store.